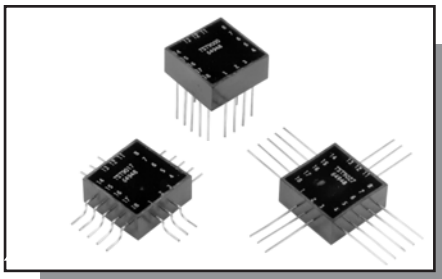
BETA TRANSFORMER
TECHNOLOGY CORPORATION
A Subsidiary of Data Device Corporation
40 Orville Drive, Bohemia, NY 11716-2529
Phone: (631) 244-7393; Fax: (631) 244-8893
Web site: www.bttc-beta.com

TST-9000 SERIES



TWIN-STACKED, 0.280" MAXIMUM HEIGHT, 1553 TRANSFORMERS CONSERVE BOARD SPACE

DESCRIPTION AND APPLICATIONS

The TST-9000 series of transformers provide the turns ratio configurations, component isolation, and common mode rejection ratio characteristics necessary for MIL-STD-1553A and B compliance.

The step-up and step-down ratios that are available with the TST-9000 series complement DDC's entire MIL-STD-1553 product line. These transformers are low-profile, dual modular units, made to couple into data bus redundant systems. They have excellent isolation within the dual package and are multi-tapped to accommodate existing system configurations.

Encapsulated in accordance with MIL-PRF-21038, their SN63 solder-dipped copper clad steel leads conveniently accommodate printed circuit board mounting. Sinusoidal or trapezoidal waveforms are accurately processed, making the TST-9000 series of transformers an excellent choice for any MIL-STD-1553A or B application.

FEATURES

- ***PC Mount***
- ***Flat Pack***
- ***Surface Mount***
- ***For Use with MIL-STD-1553A and B, MacAir A-5690, A-5232,and A-4905***
- ***-55°C to +130°C Operating Temperature Range***
- ***Built and Tested to MIL-PRF-21038 and MIL-STD-202***

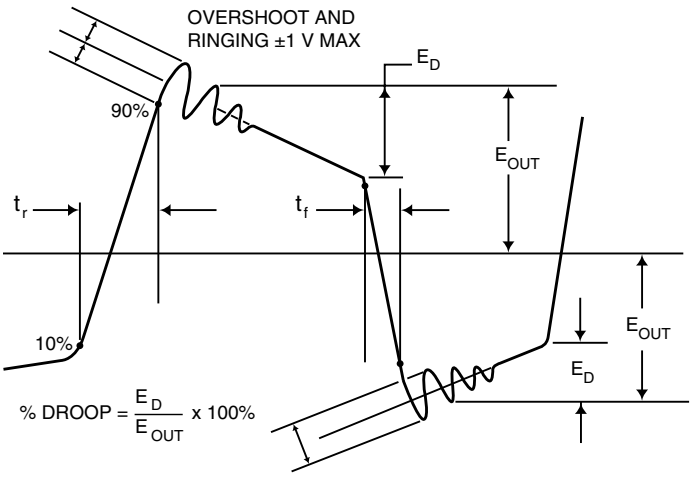
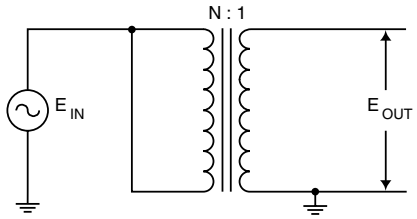


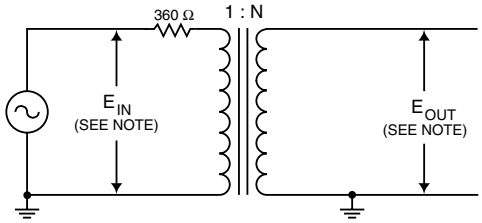
FIGURE 1. WAVEFORM INTEGRITY



E_{IN} = 10 V rms at 1 MHz

Calc: CMR = 20 log $\frac{E_{IN}}{E_{OUT}}$ (see note)

FIGURE 2. CIRCUIT FOR COMMON MODE REJECTION



E_{IN} = 250 kHz square wave, 27.0 volts peak-to-peak with a rise and fall time of 90nS ± 5nS

Calc : Droop = $\frac{E_D}{E_{OUT}}$ x 100%. (see figure 1 for E_D)

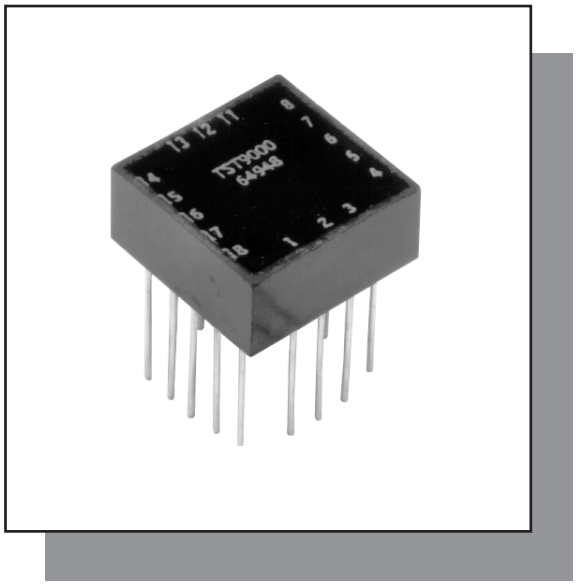
FIGURE 3. CIRCUIT FOR WAVEFORM INTEGRITY

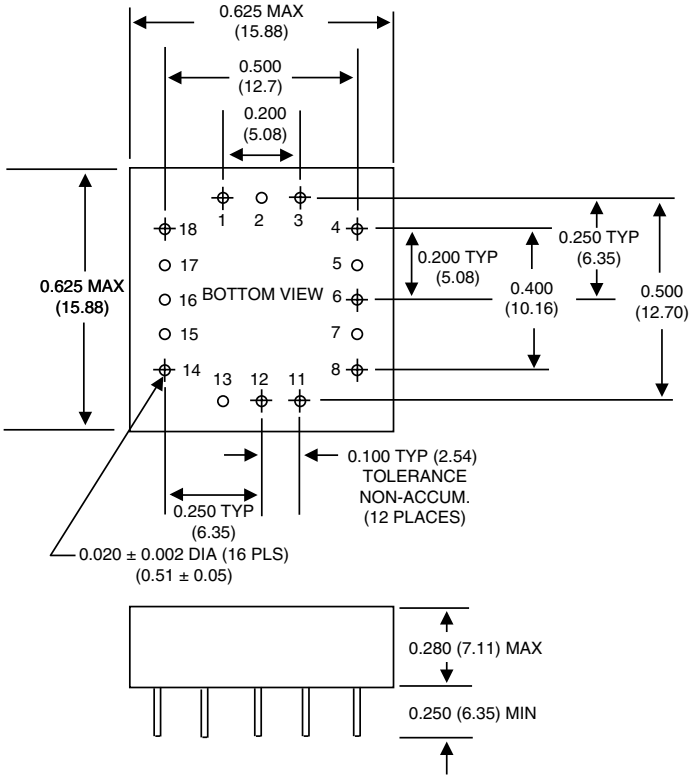
Note: Input to be applied and output to be measured for all dash numbers are as shown. N represents highest turns winding in each test.

TABLE 1. GENERAL SPECIFICATIONS

PARAMETER	UNIT	VALUE	REMARKS
Case	—	—	Flame Resistant, Diallyl Phthalate
Terminals	—	—	SN63 Solder-Dipped, Copper Clad Steel
Weight	gm	5	
Terminal Strength	lbs	2	2 pounds applied force, Method 211, MIL-STD-202, Test Condition A
Dielectric Withstanding Voltage	Vrms	100	Method 301, MIL-STD-202
Life (expectancy “X”)	Hrs	10,000 min.	In accordance with MIL-PRF-21038
Insulation Resistance	MΩ	1,000 min.	At 250 Vdc using Method 302, Test Condition B, MIL-STD-202
Pulse Width (Output Pulse)	µs	2	Tested using FIGURE 3 with resulting FIGURE 1 waveform.
Overshoot	V	± 1 max.	Tested using FIGURE 3 with resulting FIGURE 1 waveform.
Rise Time (of Output Pulse)	ns		Tested using FIGURE 3 with resulting FIGURE 1 waveform. See respective ELECTRICAL CHARACTERISTICS TABLE.
Common Mode Rejection	dB	45	Tested using FIGURE 2.
Operating Temperature Range	°C	-55° - +130°	See respective ELECTRICAL CHARACTERISTICS TABLE
Droop	%	≤ 20	Tested using FIGURE 3 with resulting FIGURE 1 waveform.
DC Resistance	Ω	—	See respective ELECTRICAL CHARACTERISTICS TABLE
Input Impedance	Ω	—	See respective ELECTRICAL CHARACTERISTICS TABLE.

CONFIGURATION A



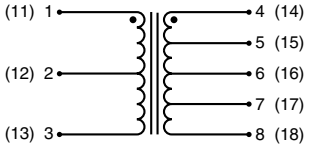


Notes:
(1) Dimensions are in inches (mm).
(2) Unless otherwise specified, tolerance is ±0.010 inches (0.25mm)

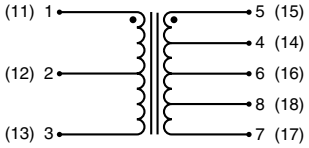
TABLE 2. ELECTRICAL CHARACTERISTICS - CONFIGURATION A

BETA P/N	TURNS RATIO	PRIMARY	SECONDARY	DC RESISTANCE Ω (MAX)	OUTPUT RISETIME (MAX)	IMPEDANCE Ω (MIN)
TST-9000	2:5 ±3% 4:7 ±3%	1-3 (11-13) 1-3 (11-13)	4-8 (14-18) 5-7 (15-17)	(1-3) (11-13) 3.5 (4-8) (14-18) 3.0	150 ns	(4-8) (14-18) 3,000
TST-9001	1:0.83 ±3% 1:0.60 ±3%	1-3 (11-13) 1-3 (11-13)	4-8 (14-18) 5-7 (15-17)	(1-3) (11-13) 3.0 (4-8) (14-18) 3.0	150 ns	(1-3) (11-13) 3,000
TST-9002	1.4:1 ±3% 2:1 ±3%	1-3 (11-13) 1-3 (11-13)	4-8 (14-18) 5-7 (15-17)	(1-3) (11-13) 3.5 (4-8) (14-18) 3.0	150 ns	(1-3) (11-13) 7,200
TST-9003	1:1 ±3% 1:0.707 ±3%	1-3 (11-13) 1-3 (11-13)	4-8 (14-18) 5-7 (15-17)	(1-3) (11-13) 3.0 (4-8) (14-18) 3.0	150 ns	(1-3) (11-13) 4,000
TST-9004	1.25:1 ±3% 1.66:1 ±3%	1-3 (11-13) 1-3 (11-13)	4-8 (14-18) 5-7 (15-17)	(1-3) (11-13) 3.2 (4-8) (14-18) 3.0	150 ns	(1-3) (11-13) 4,000
TST-9005	2.3:1 ±3% 3.2:1 ±3%	4-8 (14-18) 5-7 (15-17)	1-3 (11-13) 1-3 (11-13)	(1-3) (11-13) 1.2 (4-8) (14-18) 3.0	150 ns	(5-7) (15-17) 3,000
TST-9006	2.12:1 ±3% 1.5:1 ±3%	4-8 (14-18) 5-7 (15-17)	1-3 (11-13) 1-3 (11-13)	(1-3) (11-13) 1.1 (4-8) (14-18) 3.0	200 ns	(4-8) (14-18) 4,000
TST-9007	1:2.5 ±3% 1:1.79 ±3%	1-3 (11-13) 1-3 (11-13)	4-8 (14-18) 5-7 (15-17)	(1-3) (11-13) 3.5 (4-8) (14-18) 4.0	250 ns	(4-8) (14-18) 3,000

Note:
Wave soldering method shall preheat leads to a temperature of 100° C minimum and 140° C maximum at a rate of 2° C per second. Solder wave temperature to be 245°C nominal, 265°C maximum, with a nominal dwell time of 3 seconds and a maximum dwell time of 5 seconds.

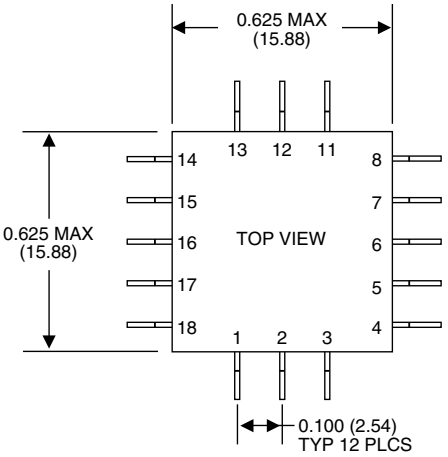


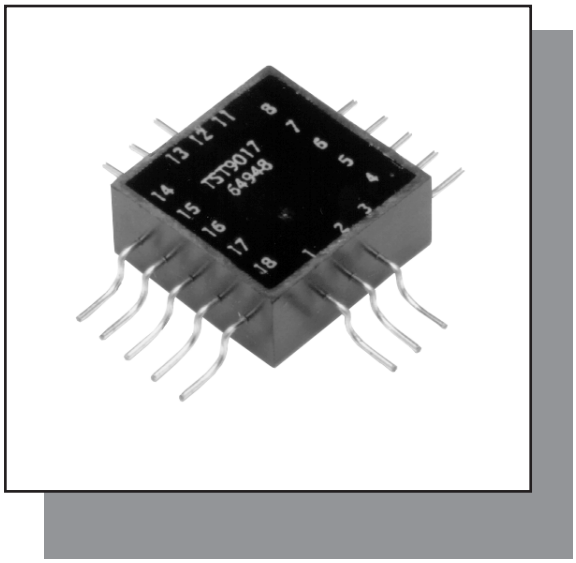
CIRCUIT DIAGRAM FOR TST-9000,
9001, 9002, 9003, 9004, 9006, 9007

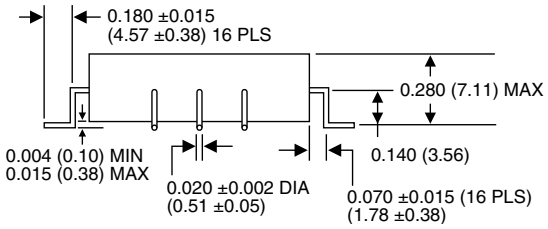


CIRCUIT DIAGRAM FOR
DASH NUMBER TST-9005

CONFIGURATION B





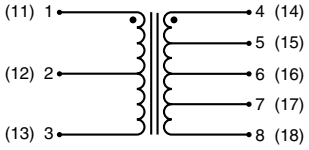


Notes:
(1) Dimensions are in inches (mm).
(2) Unless otherwise specified, tolerance is ±0.010 inches (0.25mm)

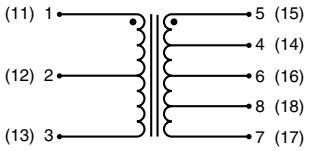
TABLE 3. ELECTRICAL CHARACTERISTICS - CONFIGURATION B

BETA P/N	TURNS RATIO	PRIMARY	SECONDARY	DC RESISTANCE Ω (MAX)	OUTPUT RISETIME (MAX)	IMPEDANCE Ω (MIN)
TST-9010	2:5 ±3% 4:7 ±3%	1-3 (11-13) 1-3 (11-13)	4-8 (14-18) 5-7 (15-17)	(1-3) (11-13) 3.5 (4-8) (14-18) 3.0	150 ns	(4-8) (14-18) 3,000
TST-9011	1:0.83 ±3% 1:0.60 ±3%	1-3 (11-13) 1-3 (11-13)	4-8 (14-18) 5-7 (15-17)	(1-3) (11-13) 3.0 (4-8) (14-18) 3.0	150 ns	(1-3) (11-13) 3,000
TST-9012	1.4:1 ±3% 2:1 ±3%	1-3 (11-13) 1-3 (11-13)	4-8 (14-18) 5-7 (15-17)	(1-3) (11-13) 3.5 (4-8) (14-18) 3.0	150 ns	(1-3) (11-13) 7,200
TST-9013	1:1 ±3% 1:0.707 ±3%	1-3 (11-13) 1-3 (11-13)	4-8 (14-18) 5-7 (15-17)	(1-3) (11-13) 3.0 (4-8) (14-18) 3.0	150 ns	(1-3) (11-13) 4,000
TST-9014	1.25:1 ±3% 1.66:1 ±3%	1-3 (11-13) 1-3 (11-13)	4-8 (14-18) 5-7 (15-17)	(1-3) (11-13) 3.2 (4-8) (14-18) 3.0	150 ns	(1-3) (11-13) 4,000
TST-9015	2.3:1 ±3% 3.2:1 ±3%	4-8 (14-18) 5-7 (15-17)	1-3 (11-13) 1-3 (11-13)	(1-3) (11-13) 1.2 (4-8) (14-18) 3.0	150 ns	(5-7) (15-17) 3,000
TST-9016	2.12:1 ±3% 1.5:1 ±3%	4-8 (14-18) 5-7 (15-17)	1-3 (11-13) 1-3 (11-13)	(1-3) (11-13) 1.1 (4-8) (14-18) 3.0	200 ns	(4-8) (14-18) 4,000
TST-9017	1:2.5 ±3% 1:1.79 ±3%	1-3 (11-13) 1-3 (11-13)	4-8 (14-18) 5-7 (15-17)	(1-3) (11-13) 3.5 (4-8) (14-18) 4.0	250 ns	(4-8) (14-18) 3,000

Note:
These transformers have been classified as Level 5A IPC-9503 and must be processed accordingly. To ensure product integrity and maintain the product warranty, these transformers require a 24 hour bake at +125°C prior to any solder reflow processing. Dried transformers must be reflowed within 24 hours. J-STD-033 preconditioning (dry-pack) can be provided by Beta upon request. Reflow process must not cause the peak body temperature of the device to exceed 225°C and must not expose the device to temperatures above 183°C for more than 90 seconds.

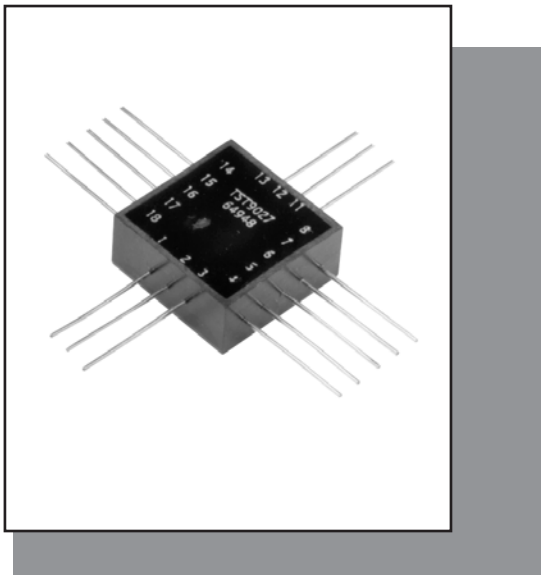


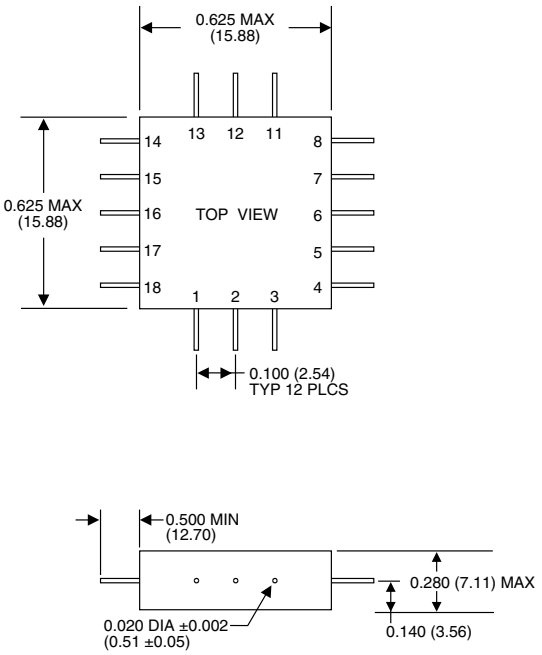
CIRCUIT DIAGRAM FOR TST-9010,
9111, 9012, 9013, 9014, 9016, 9017



CIRCUIT DIAGRAM FOR
DASH NUMBER TST-9015

CONFIGURATION C





Notes:
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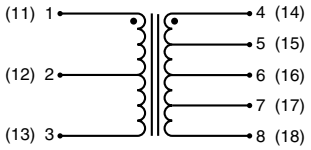
(2) Unless otherwise specified, tolerance is ±0.010 inches (0.25mm)

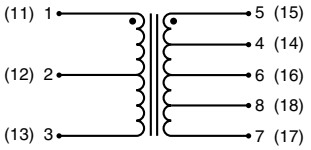
TABLE 4. ELECTRICAL CHARACTERISTICS - CONFIGURATION C

BETA P/N	TURNS RATIO	PRIMARY	SECONDARY	DC RESISTANCE Ω (MAX)	OUTPUT RISETIME (MAX)	IMPEDANCE Ω (MIN)
TST-9020	2:5 ±3% 4:7 ±3%	1-3 (11-13) 1-3 (11-13)	4-8 (14-18) 5-7 (15-17)	(1-3) (11-13) 3.5 (4-8) (14-18) 3.0	150 ns	(4-8) (14-18) 3,000
TST-9021	1:0.83 ±3% 1:0.60 ±3%	1-3 (11-13) 1-3 (11-13)	4-8 (14-18) 5-7 (15-17)	(1-3) (11-13) 3.0 (4-8) (14-18) 3.0	150 ns	(1-3) (11-13) 3,000
TST-9022	1.4:1 ±3% 2:1 ±3%	1-3 (11-13) 1-3 (11-13)	4-8 (14-18) 5-7 (15-17)	(1-3) (11-13) 3.5 (4-8) (14-18) 3.0	150 ns	(1-3) (11-13) 7,200
TST-9023	1:1 ±3% 1:0.707 ±3%	1-3 (11-13) 1-3 (11-13)	4-8 (14-18) 5-7 (15-17)	(1-3) (11-13) 3.0 (4-8) (14-18) 3.0	150 ns	(1-3) (11-13) 4,000
TST-9024	1.25:1 ±3% 1.66:1 ±3%	1-3 (11-13) 1-3 (11-13)	4-8 (14-18) 5-7 (15-17)	(1-3) (11-13) 3.2 (4-8) (14-18) 3.0	150 ns	(1-3) (11-13) 4,000
TST-9025	2.3:1 ±3% 3.2:1 ±3%	4-8 (14-18) 5-7 (15-17)	1-3 (11-13) 1-3 (11-13)	(1-3) (11-13) 1.2 (4-8) (14-18) 3.0	150 ns	(5-7) (15-17) 3,000
TST-9026	2.12:1 ±3% 1.5:1 ±3%	4-8 (14-18) 5-7 (15-17)	1-3 (11-13) 1-3 (11-13)	(1-3) (11-13) 1.1 (4-8) (14-18) 3.0	200 ns	(4-8) (14-18) 4,000
TST-9027	1:2.5 ±3% 1:1.79 ±3%	1-3 (11-13) 1-3 (11-13)	4-8 (14-18) 5-7 (15-17)	(1-3) (11-13) 3.5 (4-8) (14-18) 4.0	250 ns	(4-8) (14-18) 3,000

Note:
These transformers have been classified as Level 5A IPC-9503 and must be processed accordingly. To ensure product integrity and maintain the product warranty, these transformers require a 24 hour bake at +125°C prior to any solder reflow processing. Dried transformers must be reflowed within 24 hours. J-STD-033 preconditioning (dry-pack) can be provided by Beta upon request. Reflow process must not cause the peak body temperature of the device to exceed 225°C and must not expose the device to temperatures above 183°C for more than 90 seconds.

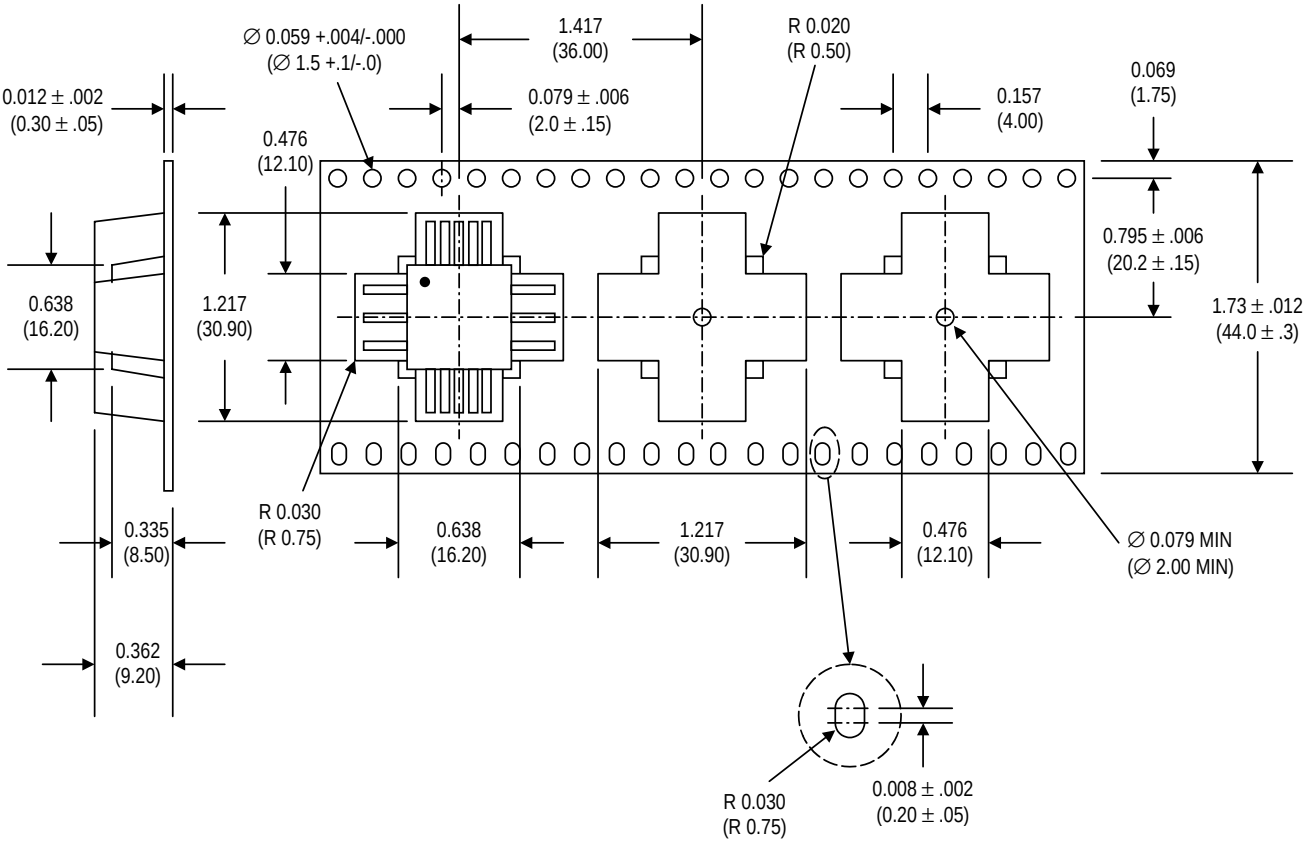


CIRCUIT DIAGRAM FOR TST-9020,
9021, 9022, 9023, 9024, 9026, 9027



CIRCUIT DIAGRAM FOR
DASH NUMBER TST-9025

(AVAILABLE) TAPE AND REEL PACKAGING



PARTS PACKAGED ON 13" DIAMETER REEL,
160 PARTS PER FULL REEL.

DIMENSIONS ARE IN
INCHES (MM)

TOLERANCES
.XXX (.XX) = ± .004 (0.10)

Visit our Web site at **www.bttc-beta.com** for the latest information.

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