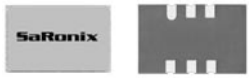
SaRonix™
A PERICOM® COMPANY

Crystal Clock Oscillator

3.3V, PECL, FR4

Technical Data

SEL481 / SEL482 Series



ACTUAL SIZE

Description

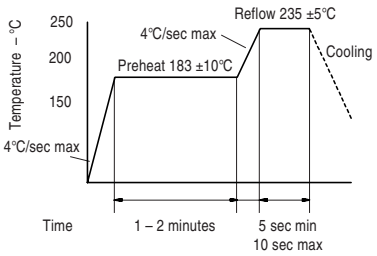
A crystal controlled, high frequency, highly stable oscillator, compatible with LVPECL logic. The output can be disabled to facilitate testing or combining with multiple clocks. The oscillator is packaged in leadless SMD FR4 SO20 available in four (4) or six (6) pad configurations (see part number builder) and achieves exceptional frequency stability. This oscillator is ideal for today's automated assembly environments.

Applications & Features

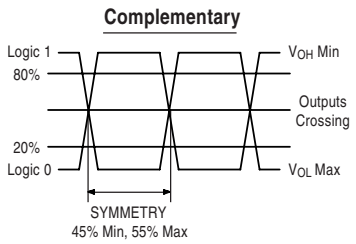
- SONET/SDH/DWDM linecards
- XGigE NICs
- Optical SOHO FTTC/FTTP OC-12 & STM-4 first/last mile networking
- 3.3V PECL (LVPECL) capability
- Frequency range from 200 to 670MHz
- Disable output feature available
- Economical and rugged FR4 package
- Guaranteed long-term aging available, consult SaRonix for details
- Designed for standard reflow and washing techniques
- Available on tape & reel; 16mm tape, 500pcs per reel
- See SEL393x Series for frequencies ≤ 200MHz
- See SEL381x Series for comparable performance in a smaller ceramic 5x7mm package
- See SDS3811 Series for new LVDS capability in a smaller ceramic 5x7mm package

Frequency Range:	200 MHz to 670 MHz
Frequency Stability:	±20, ±25, ±50 or ±100 ppm over all conditions: calibration tolerance, operating temperature, rated input (supply) voltage, load, *aging, shock and vibration.
***Aging:**	30 days (±7ppm in 10 years typical)
Temperature Range:	
Operating:	0 to +70°C or -40 to +85°C
Storage:	-55 to +125°C
Supply Voltage (V_{CC}):	+3.3V PECL
Supply Current:	85mA typ, 110mA max
Output Drive:	
Symmetry:	45/55% max @ V_{BB} or Complementary Outputs Crossing
Rise & Fall Times:	550ps typ, 850ps max, 20% to 80% of waveform
Logic 0:	≤ V_{CC} -1.620V (-40 to 85°C)
Logic 1:	≥ V_{CC} -1.025V (0 to +70°C), V_{CC} -1.085V (-40 to 85°C)
Load:	50Ω to V_{CC} -2V
Accumulated Jitter:	10ps RMS (1-sigma) max, accumulated in 20,000 adjacent periods
Phase Jitter:	3ps RMS (1-sigma) max, in 12kHz to 40MHz Freq. Band
Total Jitter:	50ps peak-to-peak max in 100,000 random periods
Output $\overline{\text{Enable}}$/$\overline{\text{Disable}}$ for SEL481x (n/a for SEL4810):	
Output $\overline{\text{Enable}}$ Voltage:	≤ Level 0 or open
$\overline{\text{Disable}}$ Voltage:	≥ Level 1 (Q & $\overline{Q}$ outputs disabled to High Impedance)
Output Enable/$\overline{\text{Disable}}$ for SEL482x:	
Output Enable:	≥ Level 1 or open
Output $\overline{\text{Disable}}$:	≤ Level 0 (Q & $\overline{Q}$ outputs disabled to High Impdeance)
Mechanical:	
Shock:	MIL-STD-883, Method 2002, Condition B
Solderability:	MIL-STD-883, Method 2003
Terminal Strength:	MIL-STD-883, Method 2004, Condition D
Vibration:	MIL-STD-883, Method 2007, Condition A
Resistance to Soldering Heat:	MIL-STD-202, Method 210, Condition I or J
Solvent Resistance:	MIL-STD-202, Method 215
Environmental:	
Thermal Shock:	MIL-STD-883, Method 1011, Condition A
Moisture Resistance:	MIL-STD-833, Method 1004

Solder Reflow Guide



Output Waveform



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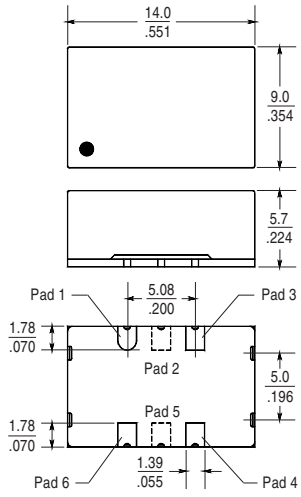
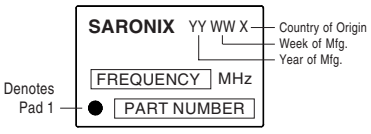
Package Details



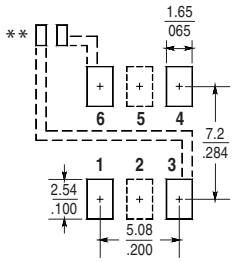
Pad Functions: See Part Numbering Guide for pad functions. Configurations include either four (4) or six (6) pads.

Marking Format*



*Exact location of items may vary

Recommended Land Pattern



**External high frequency power supply decoupling required.

Scale: None (Dimensions in $\frac{mm}{inches}$)

Part Numbering Guide

SEL48 1 0 B - 312.5000 (T)

Series
SaRonix, LVPECL FR4SO20

1 = 3.3V PECL, Hi-True Disable
2 = 3.3V PECL, Hi-True Enable

Connection Options

Packing Method
(T) = Tape & Reel
full reel increments only
Blank = Bulk

Frequency

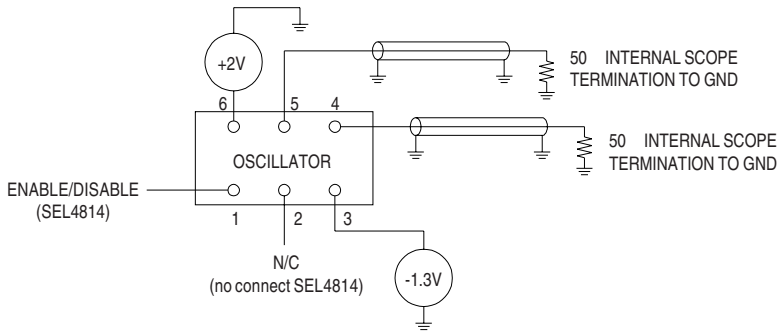
Stability
AA = ±20 ppm, 0 to +70°C
A = ±25 ppm, 0 to +70°C
B = ±50 ppm, 0 to +70°C
E = ±50 ppm, -40 to +85°C
F = ±100 ppm, -40 to +85°C

Pad:	1	2	3	4	5	6
*0 =	$\overline{OUT}$		V_{EE}	OUT		V_{CC}
1 =	E/D		V_{EE}	OUT		V_{CC}
2=	$\overline{OUT}$	E/D	V_{EE}	OUT	N/C	V_{CC}
3 =	$\overline{OUT}$	N/C	V_{EE}	OUT	E/D	V_{CC}
4 =	E/D	N/C	V_{EE}	OUT	$\overline{OUT}$	V_{CC}
5 =	N/C	E/D	V_{EE}	OUT	$\overline{OUT}$	V_{CC}

*Note: Use with SEL481X only

Test Circuit*

POSITIVE SUPPLY (LVPECL)



*Test circuit shown for SEL4814 configuration only. Test circuits for other configurations as per specified pad connections.

*All specfications subject to changes without notice