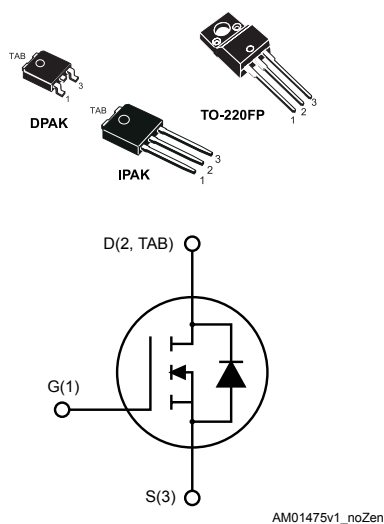


N-channel 600 V, 0.8 Ω typ., 5 A MDmesh™ II Power MOSFETs in DPAK, TO-220FP and IPAK packages



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	Package
STD7NM60N	600 V	0.9 Ω	5 A	DPAK
STF7NM60N				TO-220FP
STU7NM60N				IPAK

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using the second generation of MDmesh™ technology. These revolutionary Power MOSFETs associate a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. They are therefore suitable for the most demanding high-efficiency converters.

Product status link

[STD7NM60N](#)
[STF7NM60N](#)
[STU7NM60N](#)

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		DPAK, IPAK	TO-220FP	
V_{DS}	Drain-source voltage	600		V
V_{GS}	Gate-source voltage	± 25		V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	5	5 ⁽¹⁾	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	3	3 ⁽¹⁾	A
I_{DM} ⁽²⁾	Drain current (pulsed)	20	20 ⁽¹⁾	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	45	20	W
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat-sink ($t = 1\text{ s}$, $T_C = 25\text{ }^{\circ}\text{C}$)		2.5	kV
dv/dt ⁽³⁾	Peak diode recovery voltage slope	15		V/ns
T_J	Operating junction temperature range	-55 to 150		$^{\circ}\text{C}$
T_{stg}	Storage temperature range			

1. Limited by maximum junction temperature.

2. Pulse width limited by safe operating area.

3. $I_{SD} \leq 5\text{ A}$, $di/dt \leq 100\text{ A}/\mu\text{s}$, $V_{DSpeak} \leq V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$.

Table 2. Thermal data

Symbol	Parameter	Value			Unit
		DPAK	TO-220FP	IPAK	
$R_{thj-case}$	Thermal resistance junction-case	2.78	6.25	2.78	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient		62.5	100	$^{\circ}\text{C}/\text{W}$
$R_{thj-pcb}$ ⁽¹⁾	Thermal resistance junction-pcb	50			$^{\circ}\text{C}/\text{W}$

1. When mounted on 1inch² FR-4 board, 2 oz Cu.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AS} ⁽¹⁾	Avalanche current, repetitive or not-repetitive	2	A
E_{AS} ⁽²⁾	Single pulse avalanche energy	119	mJ

1. Pulse width limited by T_J max.

2. Starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AS}$, $V_{DD} = 50\text{ V}$.

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0 V	600			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 600 V			1	μA
		V _{GS} = 0 V, V _{DS} = 600 V, T _C = 125 °C ⁽¹⁾			100	μA
I _{GSS}	Gate body leakage current	V _{DS} = 0 V, V _{GS} = ±20 V			100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2	3	4	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10 V, I _D = 2.5 A		0.8	0.9	Ω

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 50 V, f = 1 MHz, V _{GS} = 0 V	-	363	-	pF
C _{oss}	Output capacitance			24.6		
C _{rss}	Reverse transfer capacitance			1.1		
C _{oss eq.} ⁽¹⁾	Equivalent capacitance time related	V _{DS} = 0 to 480 V, V _{GS} = 0 V	-	130	-	pF
R _G	Intrinsic gate resistance	f = 1 MHz open drain	-	5.4	-	Ω
Q _g	Total gate charge	V _{DD} = 480 V, I _D = 5 A, V _{GS} = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior)	-	14	-	nC
Q _{gs}	Gate-source charge			2.7		
Q _{gd}	Gate-drain charge			7.7		

1. C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 300 V, I _D = 2.5 A, R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	7	-	ns
t _r	Rise time			10		
t _{d(off)}	Turn-off delay time			26		
t _f	Fall time			12		

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I _{SD}	Source-drain current		-		5	A
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)				20	
V _{SD} ⁽²⁾	Forward on voltage	I _{SD} = 5 A, V _{GS} = 0 V	-		1.3	V
t _{rr}	Reverse recovery time	I _{SD} = 5 A, di/dt = 100 A/μs V _{DD} = 60 V (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	213		ns
Q _{rr}	Reverse recovery charge			1.5		μC
I _{RRM}	Reverse recovery current			14		A
t _{rr}	Reverse recovery time	I _{SD} = 5 A, di/dt = 100 A/μs V _{DD} = 60 V, T _j = 150 °C(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	265		ns
Q _{rr}	Reverse recovery charge			1.8		μC
I _{RRM}	Reverse recovery current			14		A

1. Pulse width limited by safe operating area.

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics curves

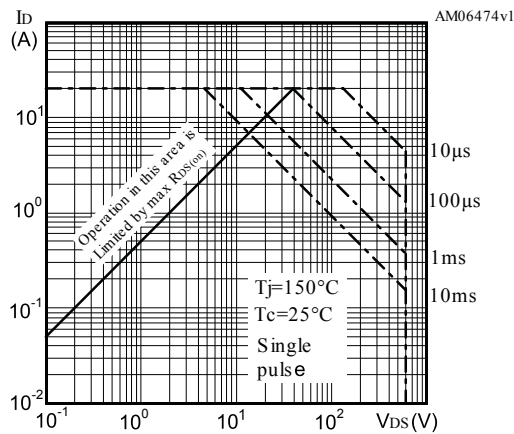
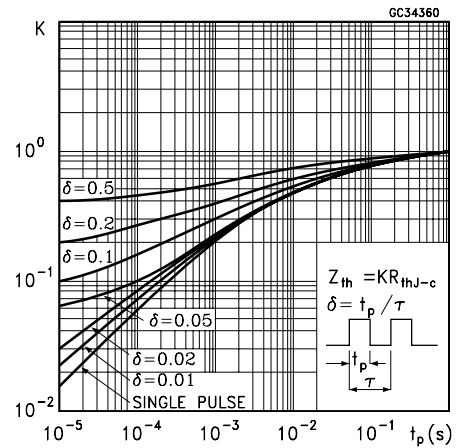
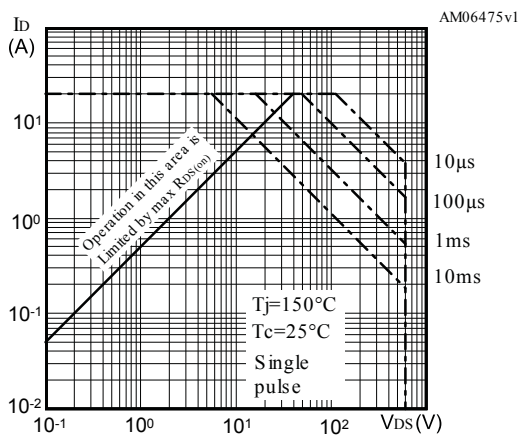
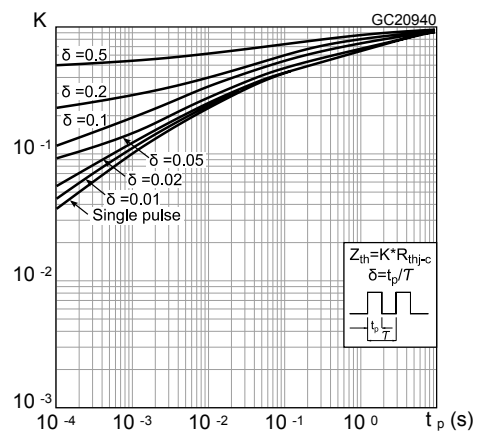
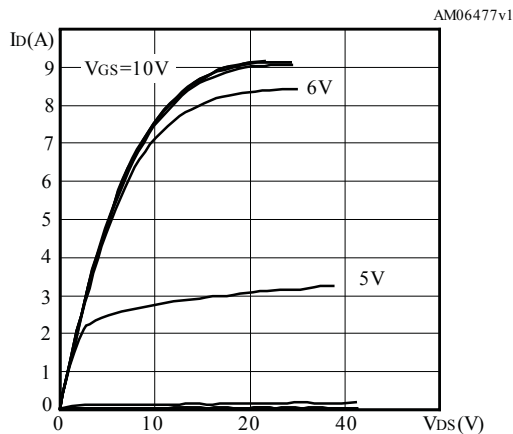
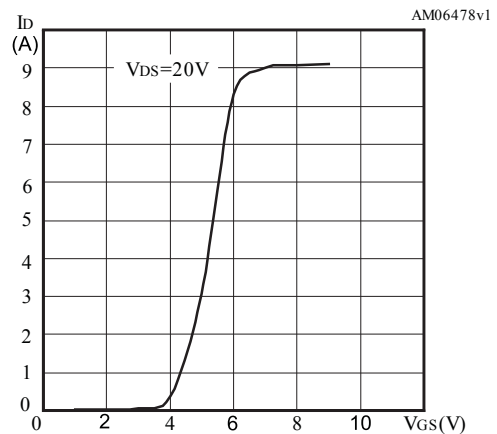
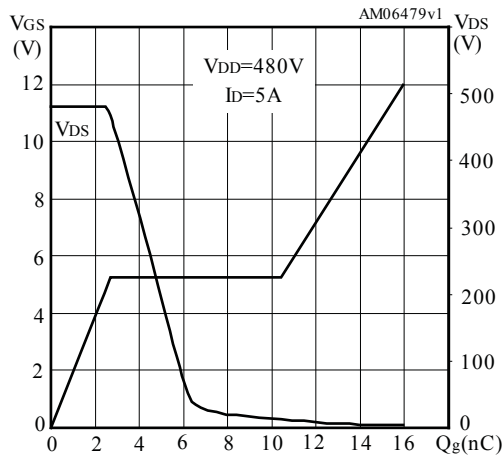
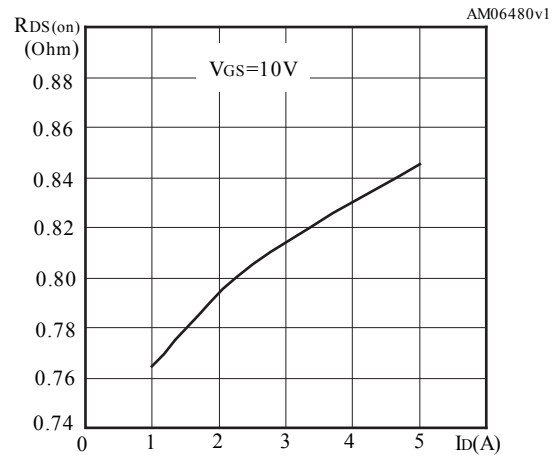
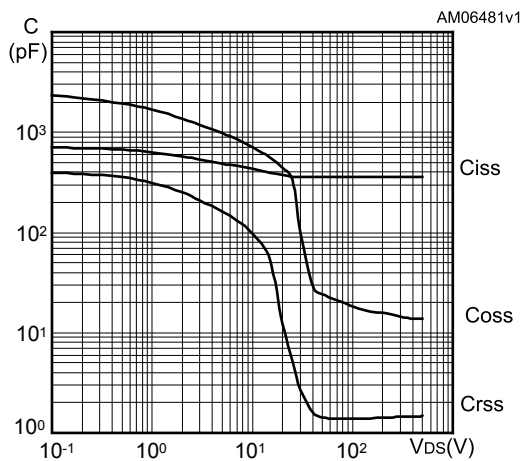
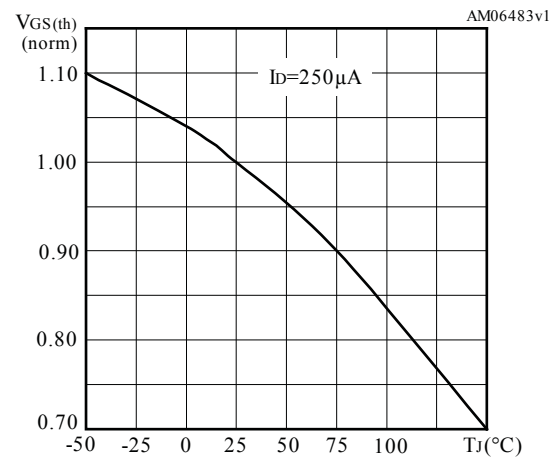
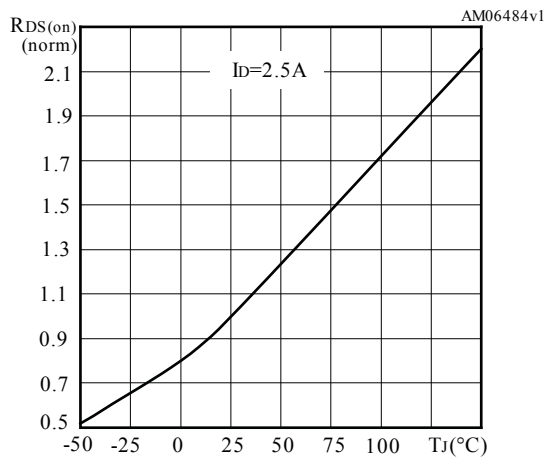
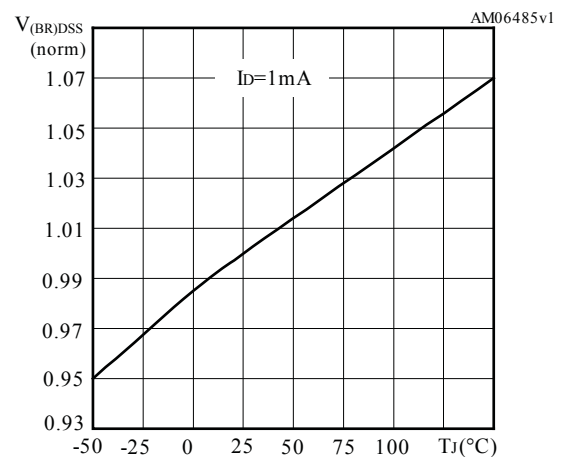
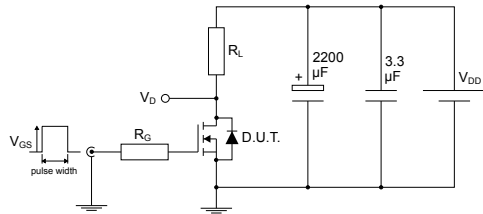
Figure 1. Safe operating area for DPAK and IPAK

Figure 2. Thermal impedance for DPAK and IPAK

Figure 3. Safe operating area for TO-220FP

Figure 4. Thermal impedance for TO-220FP

Figure 5. Output characteristics

Figure 6. Transfer characteristics


Figure 7. Gate charge vs gate-source voltage

Figure 8. Static drain-source on-resistance

Figure 9. Capacitance variations

Figure 10. Normalized gate threshold voltage vs temperature

Figure 11. Normalized on-resistance vs temperature

Figure 12. Normalized $V_{(BR)DSS}$ vs temperature


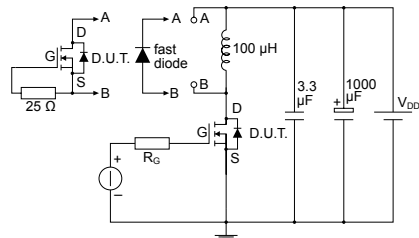
3 Test circuits

Figure 13. Test circuit for resistive load switching times


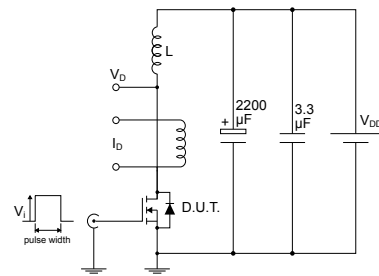
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Figure 14. Test circuit for gate charge behavior

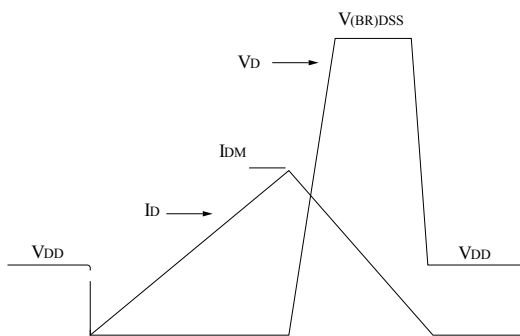

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Figure 15. Test circuit for inductive load switching and diode recovery times


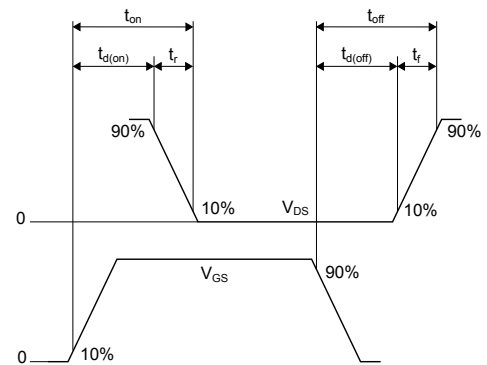
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Figure 16. Unclamped inductive load test circuit


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Figure 17. Unclamped inductive waveform


AM01472v1

Figure 18. Switching time waveform


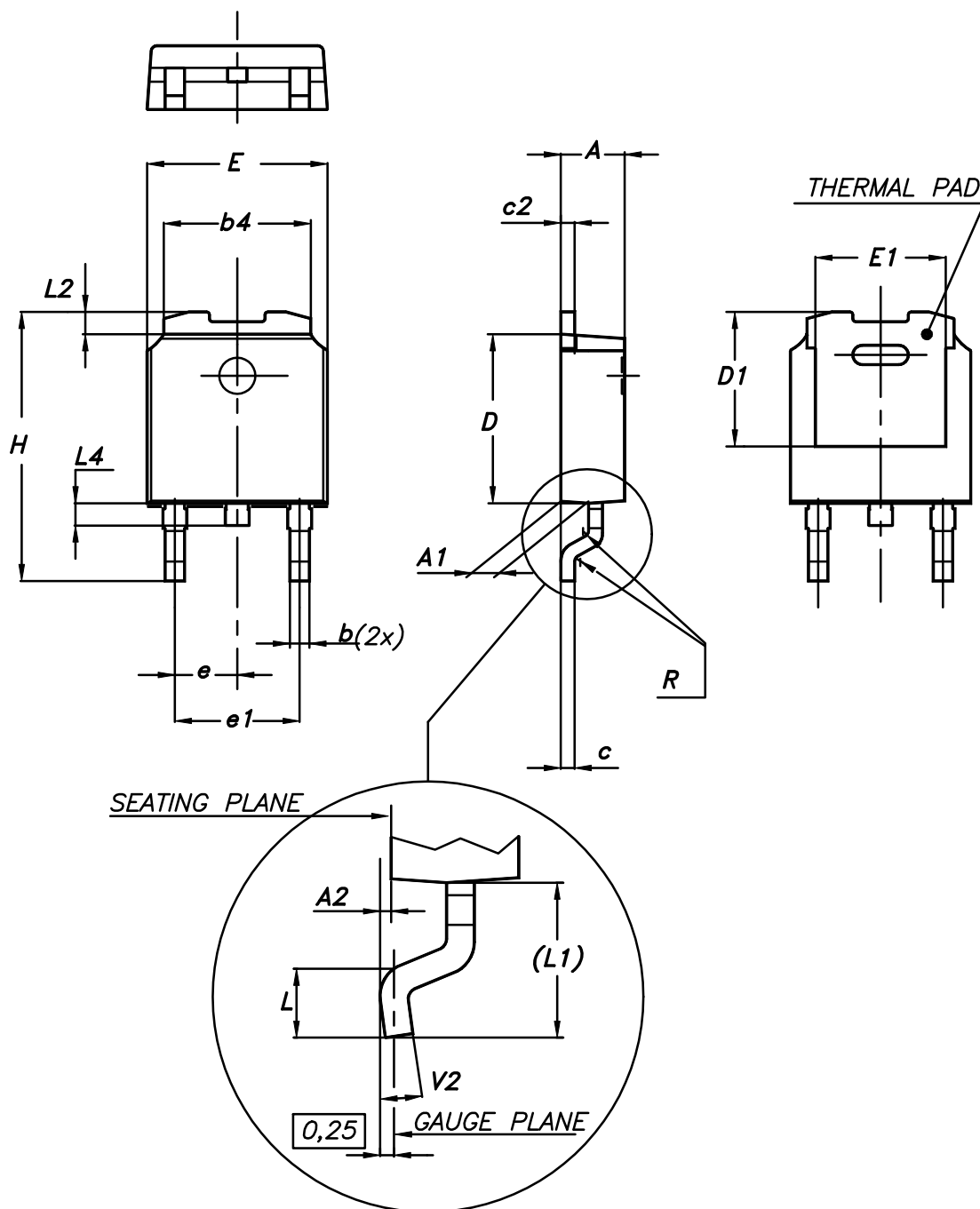
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 DPAK (TO-252) type A package information

Figure 19. DPAK (TO-252) type A package outline



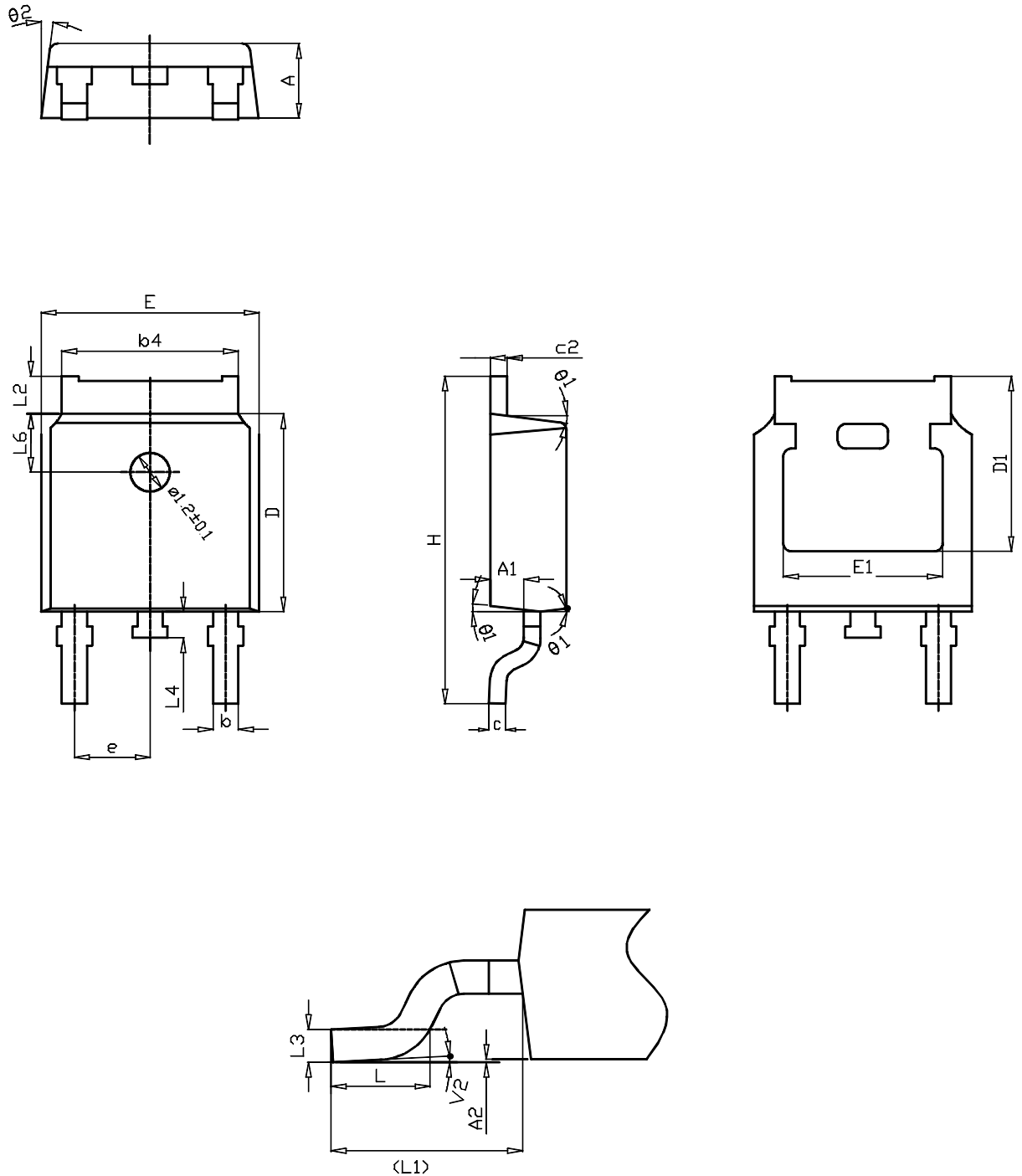
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Table 8. DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

4.2 DPAK (TO-252) type C package information

Figure 20. DPAK (TO-252) type C package outline



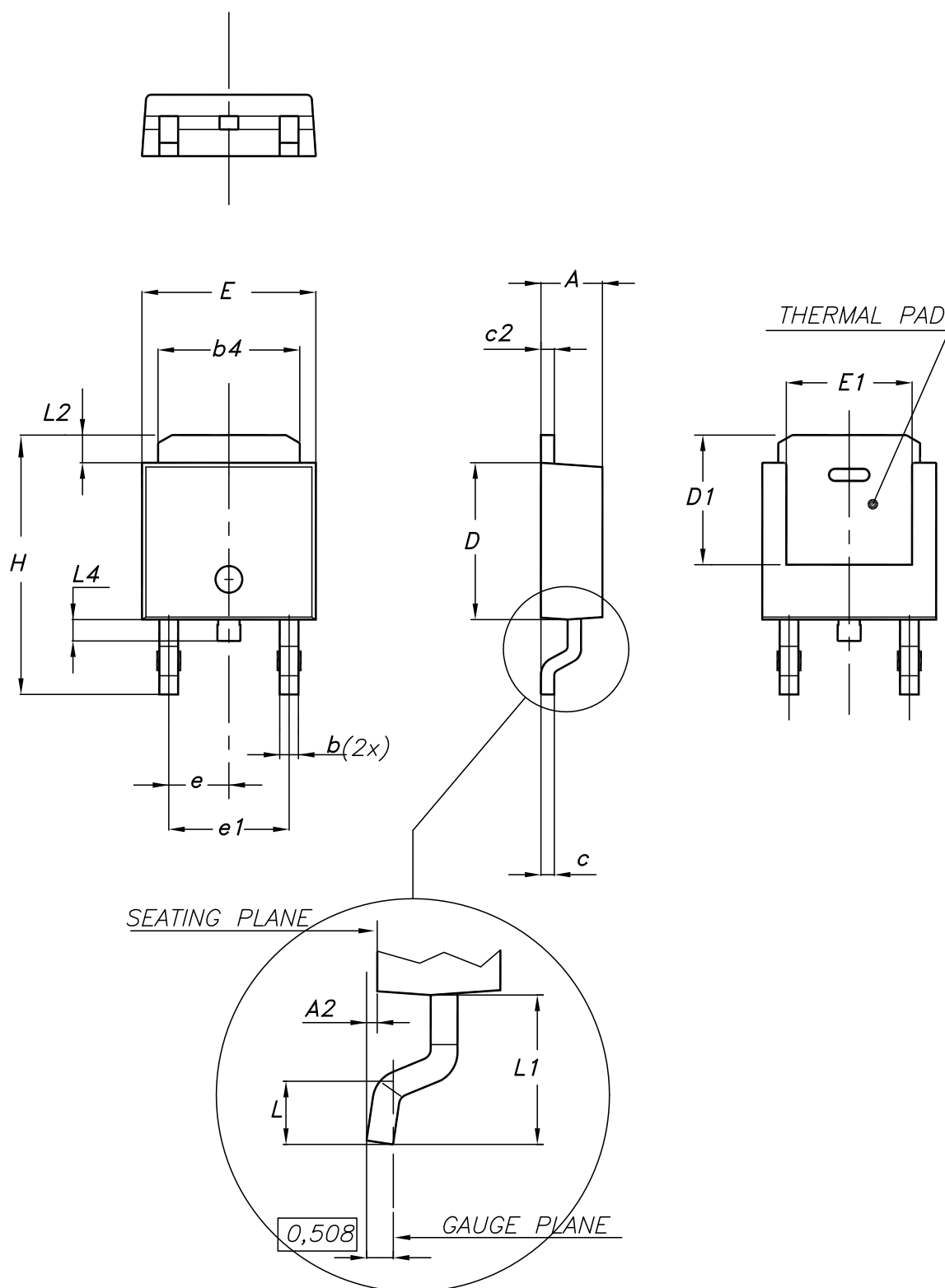
0068772_C_25

Table 9. DPAK (TO-252) type C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.25		
E	6.50	6.60	6.70
E1	4.70		
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.90		1.25
L3	0.51 BSC		
L4	0.60	0.80	1.00
L6	1.80 BSC		
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°

4.3 DPAK (TO-252) type E package information

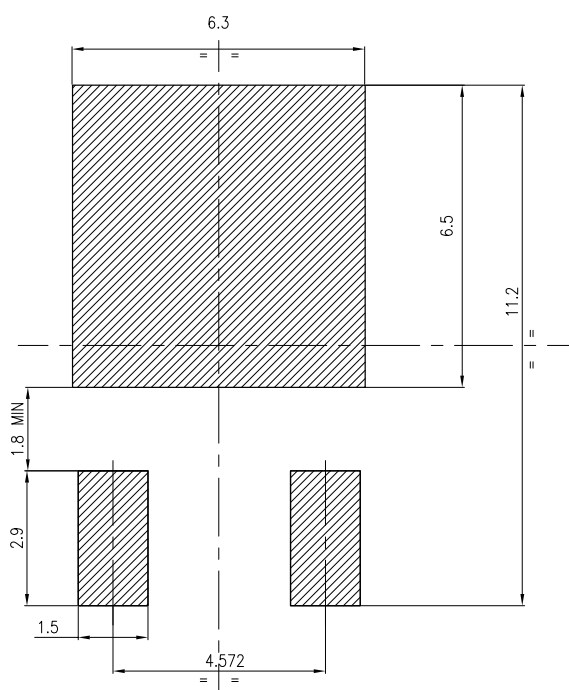
Figure 21. DPAK (TO-252) type E package outline



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Table 10. DPAK (TO-252) type E mechanical data

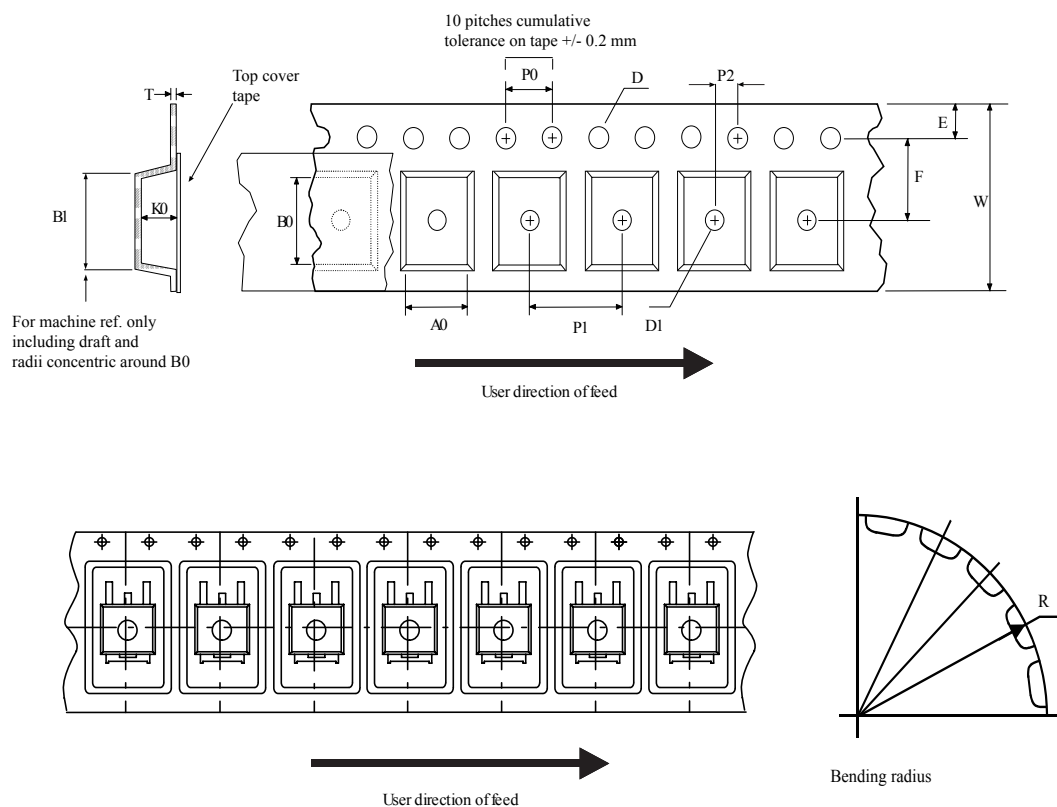
Dim.	mm		
	Min.	Typ.	Max.
A	2.18		2.39
A2			0.13
b	0.65		0.884
b4	4.95		5.46
c	0.46		0.61
c2	0.46		0.60
D	5.97		6.22
D1	5.21		
E	6.35		6.73
E1	4.32		
e		2.286	
e1		4.572	
H	9.94		10.34
L	1.50		1.78
L1		2.74	
L2	0.89		1.27
L4			1.02

Figure 22. DPAK (TO-252) recommended footprint (dimensions are in mm)


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4.4 DPAK (TO-252) packing information

Figure 23. DPAK (TO-252) tape outline



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Figure 24. DPAK (TO-252) reel outline

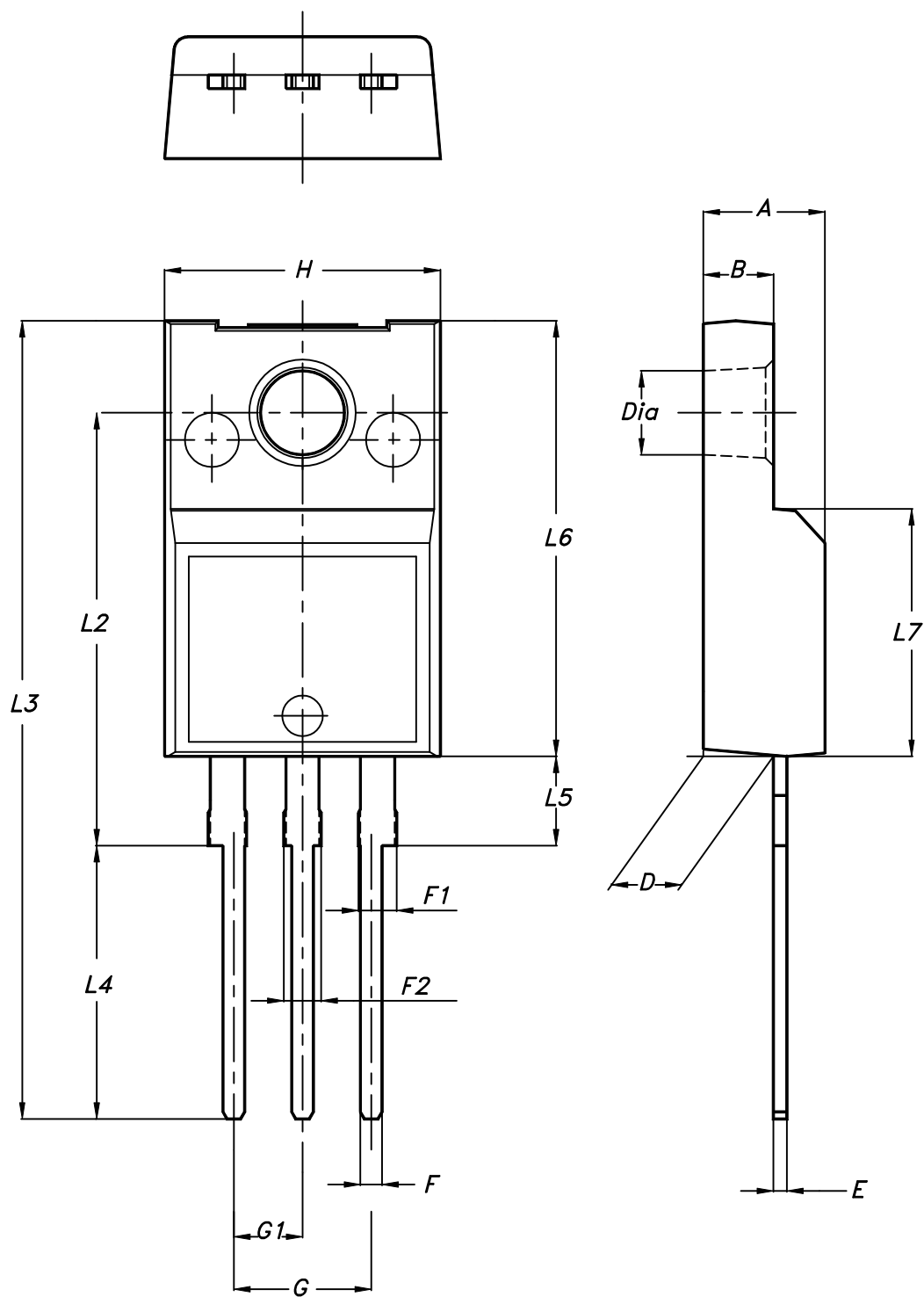

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Table 11. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

4.5 TO-220FP package information

Figure 25. TO-220FP package outline



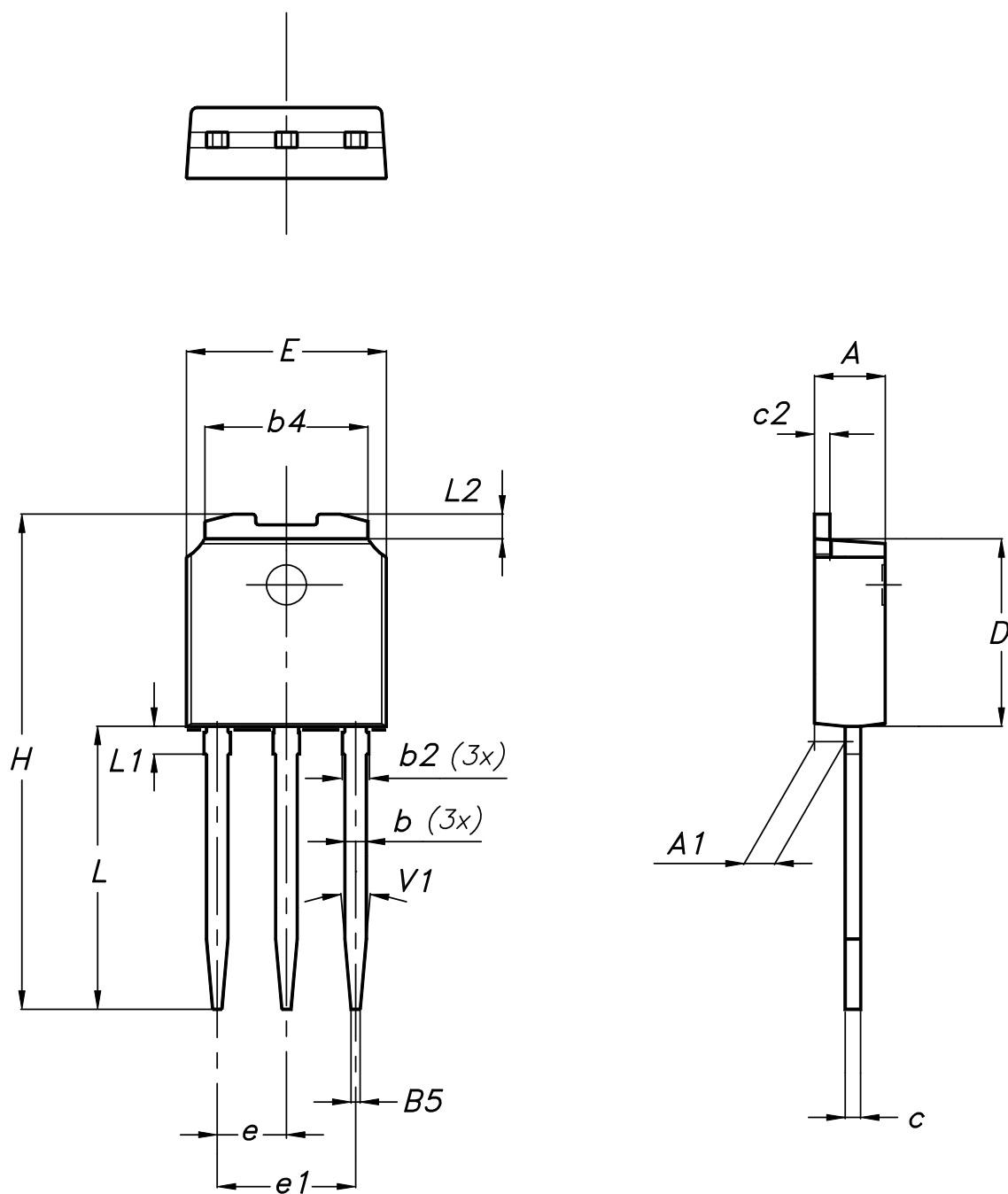
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Table 12. TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

4.6 IPAK (TO-251) type A package information

Figure 26. IPAK (TO-251) type A package outline



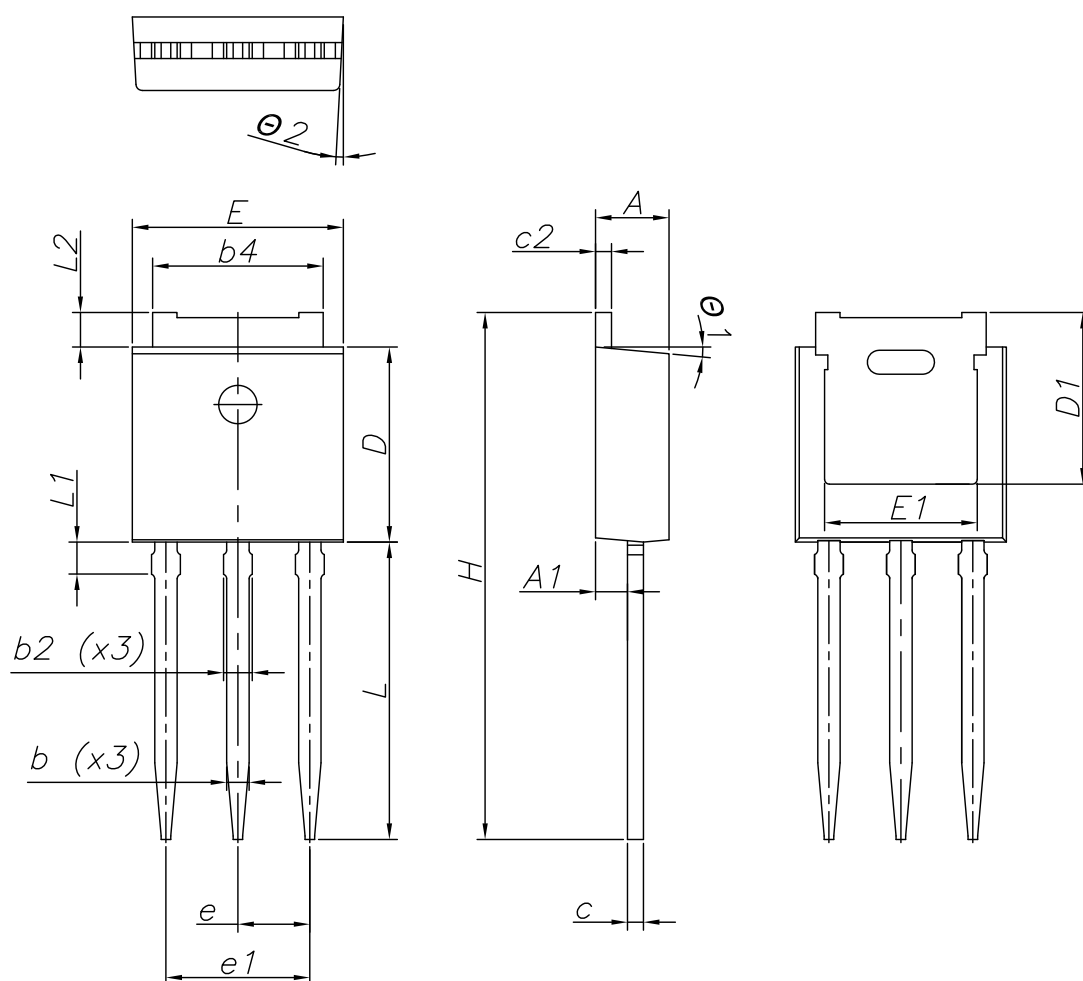
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Table 13. IPAK (TO-251) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

4.7 IPAK (TO-251) type C package information

Figure 27. IPAK (TO-251) type C package outline



0068771_IK_typeC_rev14

Table 14. IPAK (TO-251) type C package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.35
A1	0.90	1.00	1.10
b	0.66		0.79
b2			0.90
b4	5.23	5.33	5.43
c	0.46		0.59
c2	0.46		0.59
D	6.00	6.10	6.20
D1	5.20	5.37	5.55
E	6.50	6.60	6.70
E1	4.60	4.78	4.95
e	2.20	2.25	2.30
e1	4.40	4.50	4.60
H	16.18	16.48	16.78
L	9.00	9.30	9.60
L1	0.80	1.00	1.20
L2	0.90	1.08	1.25
θ1	3°	5°	7°
θ2	1°	3°	5°

5 Ordering information

Table 15. Order codes

Order code	Marking	Package	Packing
STD7NM60N	7NM60N	DPAK	Tape and reel
STF7NM60N		TO-220FP	Tube
STU7NM60N		IPAK	

Revision history

Table 16. Document revision history

Date	Version	Changes
29-Oct-2009	1	First release.
19-Jul-2010	2	Corrected values in Table 3: Thermal data.
11-Oct-2010	3	Inserted new value in Table 6: Dynamic
04-Nov-2010		Changed $R_{DS(on)}$ typical value.
05-Sep-2018		The part number STP7NM60N has been moved to a separate datasheet. Removed maturity status indication from cover page. The document status is production data. Updated title and features in cover page. Updated Section 1 Electrical ratings, Section 2 Electrical characteristics and Section 4 Package information. Minor text changes.

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