

SN54LVTR245, SN74LVTR245
3.3-V ABT OCTAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCAS428 – OCTOBER 1993

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Reduced Output Structure on A Port Minimizes V_{OHV}
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic DIPs (J)

description

These octal bus transceivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVTR245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so the buses are effectively isolated.

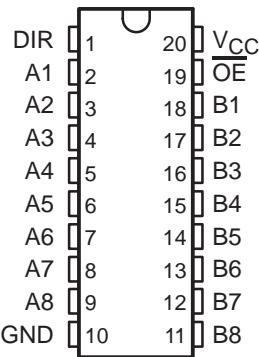
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The A port is designed to minimize the undershoot exhibited on high to low transition during simultaneous switching conditions.

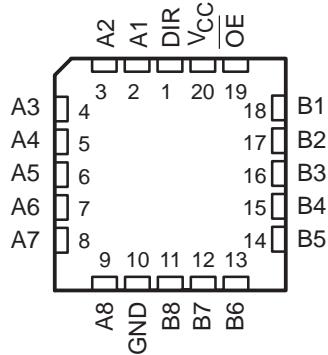
The SN74LVTR245 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVTR245 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTR245 is characterized for operation from -40°C to 85°C .

SN54LVTR245 . . . J PACKAGE
SN74LVTR245 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



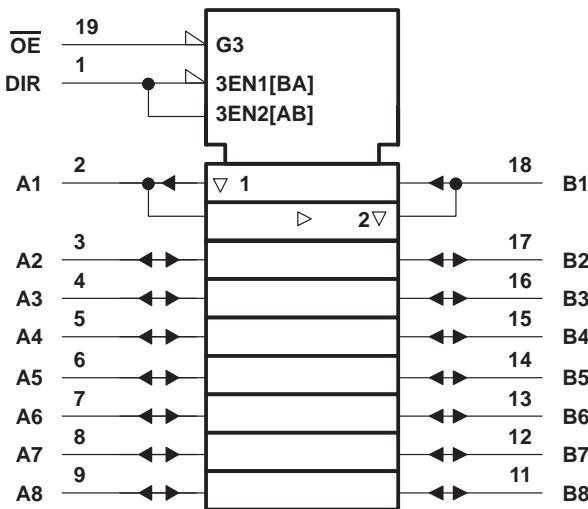
SN54LVTR245 . . . FK PACKAGE
(TOP VIEW)



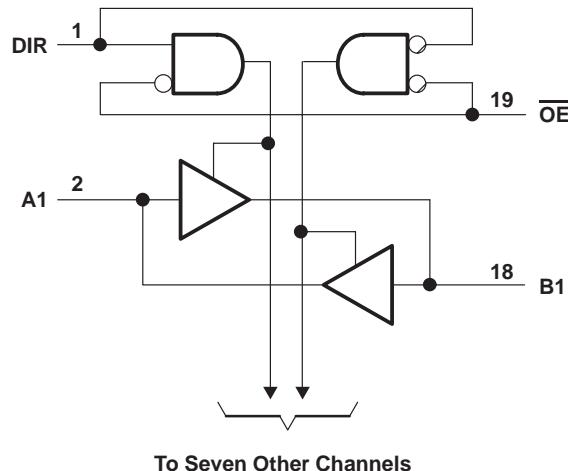
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logic symbol



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Current into any output in the low state, I_O : SN54LVTR245	96 mA
	SN74LVTR245
	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTR245	48 mA
	SN74LVTR245
	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DB package	0.65 W
	DW package
	0.85 W
	PW package
	0.6 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

		SN54LVTR245		SN74LVTR245		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage		5.5		5.5	V
I _{OH}	High-level output current	B port		-24		mA
		A port		-8		
I _{OL}	Low-level output current			24		mA
I _{OL} [†]	Low-level output current			48		mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10		ns/V
T _A	Operating free-air temperature		-55	125	-40	85
						°C

[†] Current duty cycle \leq 50%, $f \geq 1$ kHz

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54LVTR245			SN74LVTR245			UNIT
		MIN	TYPT†	MAX	MIN	TYPT†	MAX	
V_{IK}	$V_{CC} = 2.7 \text{ V}$, $I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = \text{MIN to MAX}^‡$, $I_{OH} = -100 \mu\text{A}$	B port	$V_{CC} - 0.2$		$V_{CC} - 0.2$			V
	$V_{CC} = 2.7 \text{ V}$, $I_{OH} = -8 \text{ mA}$		2.4		2.4			
	$V_{CC} = 3 \text{ V}$		$I_{OH} = -24 \text{ mA}$		2		2	
			$I_{OH} = -32 \text{ mA}$					
	$V_{CC} = \text{MIN to MAX}^‡$, $I_{OH} = -100 \mu\text{A}$		$V_{CC} - 0.2$		$V_{CC} - 0.2$			
	$V_{CC} = 2.7 \text{ V}$, $I_{OH} = -1 \text{ mA}$	A port	2.4		2.4			
	$V_{CC} = 3 \text{ V}$		$I_{OH} = -3 \text{ mA}$		2.4		2.4	
			$I_{OH} = -8 \text{ mA}$		2			
			$I_{OH} = -12 \text{ mA}$				2	
	$V_{CC} = 2.7 \text{ V}$		$I_{OL} = 100 \mu\text{A}$		0.2		0.2	
V_{OL}	$V_{CC} = 3 \text{ V}$	Control pins	$I_{OL} = 24 \text{ mA}$		0.5		0.5	V
			$I_{OL} = 16 \text{ mA}$		0.4		0.4	
			$I_{OL} = 32 \text{ mA}$		0.5		0.5	
			$I_{OL} = 48 \text{ mA}$		0.55			
			$I_{OL} = 64 \text{ mA}$				0.55	
	$V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC} \text{ or GND}$				± 1		± 1	
I_I	$V_{CC} = 0 \text{ or MAX}^‡$, $V_I = 5.5 \text{ V}$	A or B ports [§]			10		10	μA
	$V_{CC} = 3.6 \text{ V}$		$V_I = 5.5 \text{ V}$		100		20	
			$V_I = V_{CC}$		5		5	
			$V_I = 0$		-5		-5	
	$V_{CC} = 3 \text{ V}$		$V_I = 0.8 \text{ V}$	75		75		
$I_{I(\text{hold})}$	$V_{CC} = 3 \text{ V}$	A or B ports	$V_I = 2 \text{ V}$	-75		-75		μA
I_{OZH}	$V_{CC} = 3.6 \text{ V}$, $V_O = 3 \text{ V}$				1		1	μA
I_{OZL}	$V_{CC} = 3.6 \text{ V}$, $V_O = 0.5 \text{ V}$				-1		-1	μA
I_{CC}	$V_{CC} = 3.6 \text{ V}$, $I_O = 0$, $V_I = V_{CC} \text{ or GND}$	Outputs high		0.13	0.5	0.13	0.19	mA
			Outputs low	8.8	14	8.8	12	
			Outputs disabled	0.13	0.5	0.13	0.19	
$\Delta I_{CC}^¶$	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at $V_{CC} \text{ or GND}$			0.3		0.2		mA
C_I	$V_I = 3 \text{ V or } 0$			4		4		pF
C_{IO}	$V_O = 3 \text{ V or } 0$			10		10		pF

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ Unused pins at V_{CC} or GND

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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switching characteristics, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTR245 $T_A = -55^\circ\text{C}$ to 125°C				SN74LVTR245 $T_A = -40^\circ\text{C}$ to 85°C				UNIT	
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 2.7 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 2.7 \text{ V}$			
			MIN	MAX	MIN	MAX	MIN	TYPE [†]	MAX	MIN	MAX	
t_{PLH}	A	B	1.1	4.3		4.8	1.1	2.5	4.2		4.7	ns
	B	A	1.4	4.5		5.4	1.4	2.7	4.4		5.3	
t_{PHL}	A	B	1.1	4.7		5.9	1.1	2.6	4.6		5.8	ns
	B	A	1	4.2		5.3	1	2.3	4.1		5.1	
t_{PZH}	\overline{OE}	B	1.3	5.9		7	1.3	3.1	5.5		6.7	ns
		A	1.6	6.1		8.4	1.6	3.6	6		8.3	
t_{PZL}	\overline{OE}	B	2	6.7		8.1	2	3.9	6.6		8	ns
		A	1.8	6.5		7.7	1.8	3.8	6.4		7.6	
t_{PHZ}	\overline{OE}	B	2.7	6.5		7	2.7	4.2	6.1		6.7	ns
		A	2.5	6.2		6.8	2.5	4	5.8		6.4	
t_{PLZ}	\overline{OE}	B	2.4	5.6		5.6	2.4	3.7	5.2		5.4	ns
		A	2.4	5.5		5.6	2.4	3.7	5.2		5.3	

[†]All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

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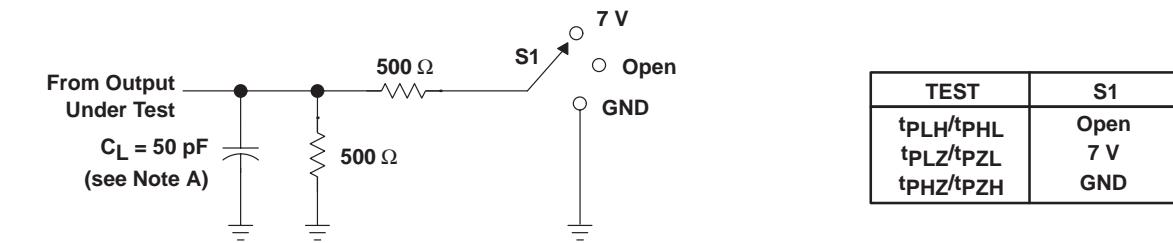


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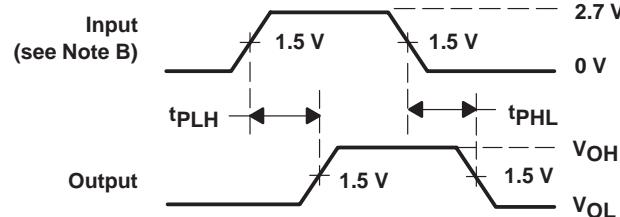
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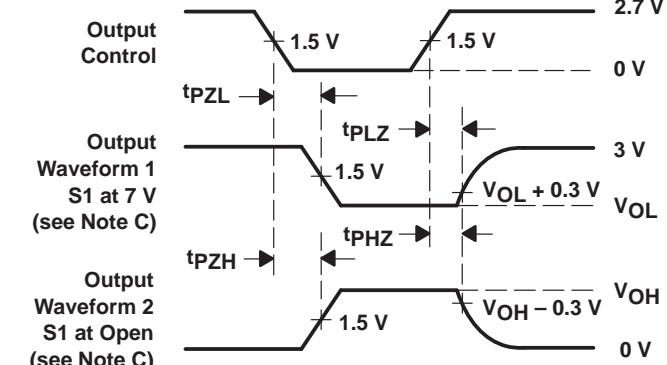
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR OUTPUTS



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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