

HD14006B

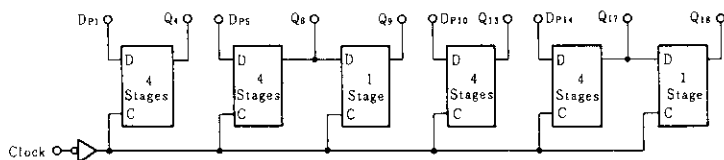
18-bit Static Shift Register

The HD14006B shift register is comprised of four separate shift register sections sharing a common clock: two sections have four stages and two sections have five stages with an output tap on both the fourth and fifth stages. This makes it possible to obtain a shift register of 4, 5, 8, 9, 10, 12, 13, 14, 16, 17 or 18 bits by appropriate selection of inputs and outputs. This part is particularly useful in serial shift registers and time delay circuits.

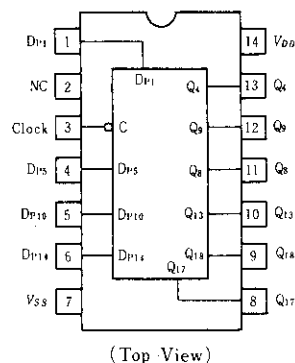
FEATURES

- Output Transitions Occur on the Falling Edge of the Clock Pulse
- Quiescent Current = 5nA/pkg typ @5V
- Fully Static Operation
- 8MHz Shift Rate Typical
- Can be Cascaded to Provide Longer Shift Register Lengths
- Supply Voltage Range = 3 to 18V
- Capable of Driving One Lowpower Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4006B and MC14006B

BLOCK DIAGRAM



PIN ARRANGEMENT

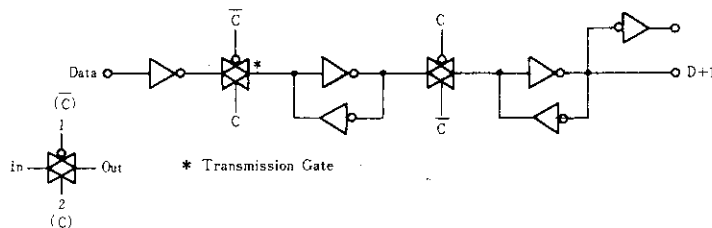


TRUTH TABLE

D_n	C	Q_{n+1}
0		0
1		1
X		Q_n

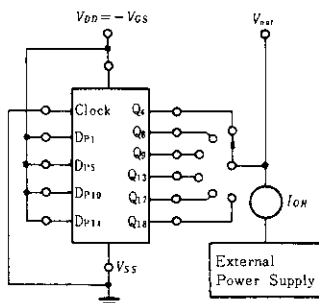
X : Don't Care

LOGIC DIAGRAM

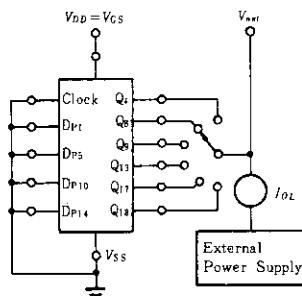


DC CHARACTERISTIC TEST CIRCUIT

● I_{OH}



● I_{OL}



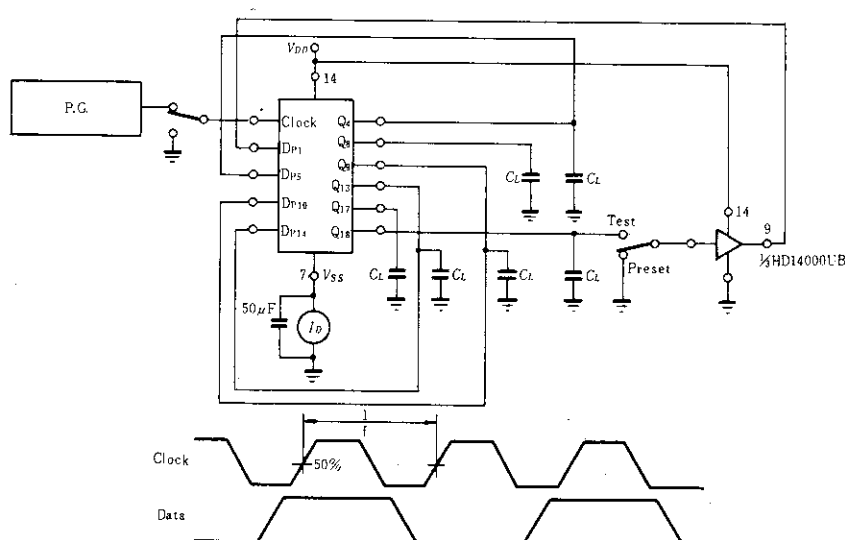
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	$V_{DD}(V)$	Test Conditions	-40°C		25°C			85°C		Unit
				min	max	min	typ	max	min	max	
Output Voltage	V_{OL}	5.0	$V_{in}=V_{DD}$ or 0	—	0.05	—	0	0.05	—	0.05	V
		10		—	0.05	—	0	0.05	—	0.05	
		15		—	0.05	—	0	0.05	—	0.05	
	V_{OH}	5.0	$V_{in}=0$ or V_{DD}	4.95	—	4.95	5.0	—	4.95	—	V
		10		9.95	—	9.95	10	—	9.95	—	
		15		14.95	—	14.95	15	—	14.95	—	
Input Voltage	V_{IL}	5.0	$V_{out}=4.5$ or 0.5V	—	1.5	—	2.25	1.5	—	1.5	V
		10	$V_{out}=9.0$ or 1.0V	—	3.0	—	4.50	3.0	—	3.0	
		15	$V_{out}=13.5$ or 1.5V	—	4.0	—	6.75	4.0	—	4.0	
	V_{IH}	5.0	$V_{out}=0.5$ or 4.5V	3.5	—	3.5	2.75	—	3.5	—	V
		10	$V_{out}=1.0$ or 9.0V	7.0	—	7.0	5.50	—	7.0	—	
		15	$V_{out}=1.5$ or 13.5V	11.0	—	11.0	8.25	—	11.0	—	
Output Drive Current	I_{OH}	5.0	$V_{OH}=2.5V$	-1.0	—	-0.8	-1.7	—	-0.6	—	mA
		5.0	$V_{OH}=4.6V$	-0.2	—	-0.16	-0.36	—	-0.12	—	
		10	$V_{OH}=9.5V$	-0.5	—	-0.4	-0.9	—	-0.3	—	
		15	$V_{OH}=13.5V$	-1.4	—	-1.2	-3.5	—	-1.0	—	
	I_{OL}	5.0	$V_{OL}=0.4V$	0.52	—	0.44	0.88	—	0.36	—	mA
		10	$V_{OL}=0.5V$	1.3	—	1.1	2.25	—	0.9	—	
		15	$V_{OL}=1.5V$	3.6	—	3.0	8.8	—	2.4	—	
Input Current	I_{in}	15		—	± 0.3	—	± 0.0001	± 0.3	—	± 1.0	μA
Input Capacitance	C_{in}	—	$V_{in}=0$	—	—	—	5.0	7.5	—	—	pF
Quiescent Current	I_{DD}	5.0	Zero Signal, per Package	—	20	—	0.005	20	—	150	μA
		10		—	40	—	0.010	40	—	300	
		15		—	80	—	0.015	80	—	600	
Total Supply Current*	I_T	5.0	Dynamic + I_{DD} ,	—	—	—	1.3	—	—	—	μA
		10	Per Gate,	—	—	—	2.6	—	—	—	
		15	$C_L=50pF$, $f=1kHz$	—	—	—	3.9	—	—	—	

* To calculate total supply current at frequency other than 1kHz.

@ $V_{DD}=5.0V$ $I_T = (1.3\mu A/kHz)f + I_{DD}$, @ $V_{DD}=10V$ $I_T = (2.6\mu A/kHz)f + I_{DD}$, @ $V_{DD}=15V$ $I_T = (3.9\mu A/kHz)f + I_{DD}$

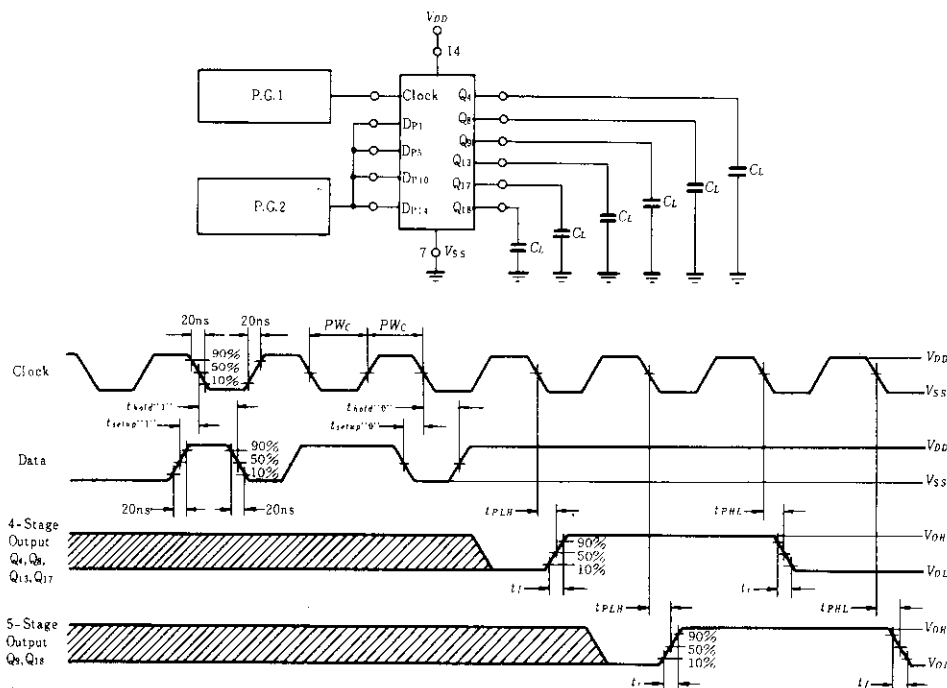
POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



SWITCHING CHARACTERISTICS ($C_L=50\text{pF}$, $T_a=25^\circ\text{C}$)

Characteristic	Symbol	V_{DD} (V)	min	typ	max	Unit
Output Rise Time	t_r	5.0	—	180	400	ns
		10	—	90	200	
		15	—	65	160	
Output Fall Time	t_f	5.0	—	100	200	ns
		10	—	50	100	
		15	—	37	80	
Propagation Delay Time	t_{PLH} , t_{PHL}	5.0	—	305	600	ns
		10	—	110	275	
		15	—	80	200	
Clock Pulse Width	PW_C	5.0	250	100	—	ns
		10	125	60	—	
		15	95	40	—	
Clock Pulse Frequency	PRF	5.0	—	5.0	2.0	MHz
		10	—	8.3	4.0	
		15	—	12	6.0	
Clock Pulse Rise and Fall Time	t_r , t_f	5.0	—	—	15	μs
		10	—	—	15	
		15	—	—	15	
Setup Time	t_{setup}	5.0	0	-50	—	ns
		10	0	-15	—	
		15	0	-8.0	—	
Hold Time	t_{hold}	5.0	220	75	—	ns
		10	110	25	—	
		15	90	20	—	

SWITCHING TIME TEST CIRCUIT



Output state can change since data previously clocked in might be in either state.



Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g

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