

100341

Low Power 8-Bit Shift Register

General Description

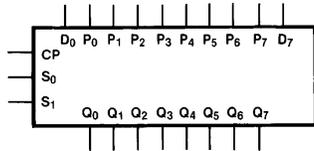
The 100341 contains eight edge-triggered, D-type flip-flops with individual inputs (P_n) and outputs (Q_n) for parallel operation, and with serial inputs (D_n) and steering logic for bidirectional shifting. The flip-flops accept input data a setup time before the positive-going transition of the clock pulse and their outputs respond a propagation delay after this rising clock edge.

The circuit operating mode is determined by the Select inputs S_0 and S_1 , which are internally decoded to select either "parallel entry", "hold", "shift left" or "shift right" as described in the Truth Table. All inputs have 50 k Ω pull-down resistors.

Features

- 35% power reduction of the 100141
- 2000V ESD protection
- Pin/function compatible with 100141
- Voltage compensated operating range = $-4.2V$ to $-5.7V$
- Available to industrial grade temperature range

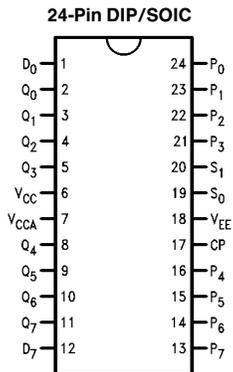
Logic Symbol



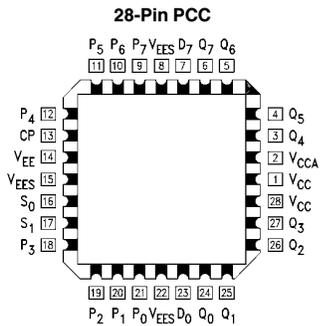
Pin Names	Description
CP	Clock Input
S_0, S_1	Select Inputs
D_0, D_7	Serial Inputs
P_0-P_7	Parallel Inputs
Q_0-Q_7	Data Outputs

TL/F/9880-1

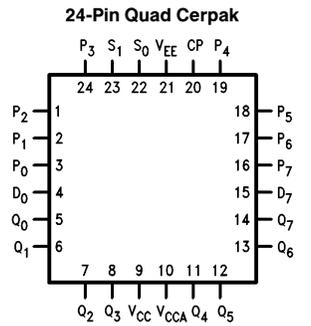
Connection Diagrams



TL/F/9880-2

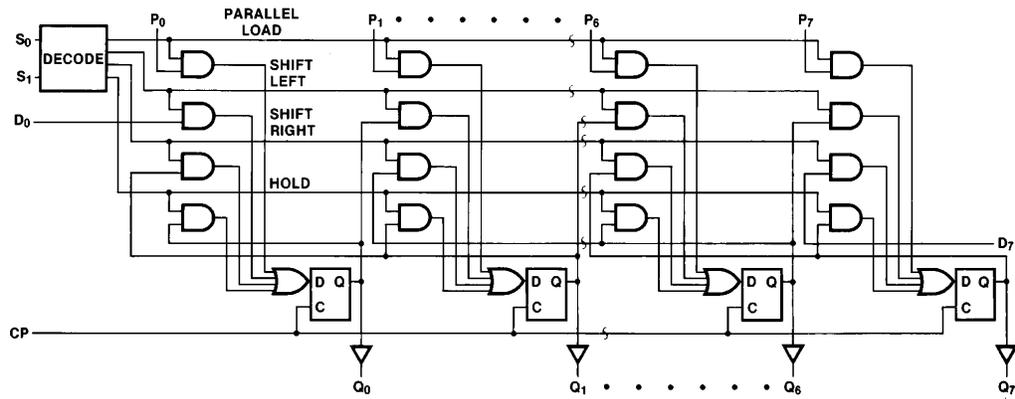


TL/F/9880-4



TL/F/9880-3

Logic Diagram



TL/F/9880-5

Truth Table

Function	Inputs					Outputs							
	D ₇	D ₀	S ₁	S ₀	CP	Q ₇	Q ₆	Q ₅	Q ₄	Q ₃	Q ₂	Q ₁	Q ₀
Load Register	X	X	L	L	↗	P ₇	P ₆	P ₅	P ₄	P ₃	P ₂	P ₁	P ₀
Shift Left	X	L	L	H	↗	Q ₆	Q ₅	Q ₄	Q ₃	Q ₂	Q ₁	Q ₀	L
Shift Left	X	H	L	H	↗	Q ₆	Q ₅	Q ₄	Q ₃	Q ₂	Q ₁	Q ₀	H
Shift Right	L	X	H	L	↗	L	Q ₇	Q ₆	Q ₅	Q ₄	Q ₃	Q ₂	Q ₁
Shift Right	H	X	H	L	↗	H	Q ₇	Q ₆	Q ₅	Q ₄	Q ₃	Q ₂	Q ₁
Hold	X	X	H	H	X	No Change							
Hold	X	X	X	X	H								
Hold	X	X	X	X	L								

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 ↗ = LOW-to-HIGH Transition

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG}) -65°C to $+150^{\circ}\text{C}$

Maximum Junction Temperature (T_J)
 Ceramic $+175^{\circ}\text{C}$
 Plastic $+150^{\circ}\text{C}$

V_{EE} Pin Potential to Ground Pin -7.0V to $+0.5\text{V}$

Input Voltage (DC) V_{EE} to $+0.5\text{V}$

Output Current (DC Output HIGH) -50mA

ESD (Note 2) $\geq 2000\text{V}$

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)
 Commercial 0°C to $+85^{\circ}\text{C}$
 Industrial -40°C to $+85^{\circ}\text{C}$
 Military -55°C to $+125^{\circ}\text{C}$
 Supply Voltage (V_{EE}) -5.7V to -4.2V

Commercial Version

DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$ to -5.7V , $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	-1025	-955	-870	mV	$V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$	Loading with 50Ω to -2.0V
V_{OL}	Output LOW Voltage	-1830	-1705	-1620	mV		
V_{OHC}	Output HIGH Voltage	-1035			mV	$V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$	Loading with 50Ω to -2.0V
V_{OLC}	Output LOW Voltage			-1610	mV		
V_{IH}	Input HIGH Voltage	-1165		-870	mV	Guaranteed HIGH Signal for all Inputs	
V_{IL}	Input LOW Voltage	-1830		-1475	mV	Guaranteed LOW Signal for all Inputs	
I_{IL}	Input LOW Current	0.50			μA	$V_{IN} = V_{IL}(\text{Min})$	
I_{IH}	Input HIGH Current			240	μA	$V_{IN} = V_{IH}(\text{Max})$	
I_{EE}	Power Supply Current	-157 -167		-75 -75	mA mA	Inputs Open $V_{EE} = -4.2\text{V}$ to -4.8V $V_{EE} = -4.2\text{V}$ to -5.7V	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version (Continued)

DIP AC Electrical Characteristics $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{max}	Max Clock Frequency	400		400		400		MHz	Figures 2 and 3
t_{PLH} t_{PHL}	Propagation Delay CP to Output	0.90	1.90	1.00	2.00	1.00	2.10	ns	Figures 1 and 3 (Note 1)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.30	0.35	1.30	0.35	1.30	ns	Figures 1 and 3
t_S	Setup Time D_n, P_n S_n	0.65 1.60		0.65 1.60		0.65 1.60		ns	Figure 4
t_H	Hold D_n, P_n S_n	0.80 0.60		0.80 0.60		0.80 0.60		ns	
$t_{pw(H)}$	Pulse Width HIGH CP	2.00		2.00		2.00		ns	Figure 3

Note 1: The propagation delay specified is for the switching of a single output. Delays may vary up to 0.40 ns if multiple outputs are switching simultaneously.

SOIC, PCC and Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{max}	Max Clock Frequency	425		425		425		MHz	Figures 2 and 3
t_{PLH} t_{PHL}	Propagation Delay CP to Output	0.90	1.70	1.00	1.80	1.00	1.90	ns	Figures 1 and 3 (Note 2)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.20	0.35	1.20	0.35	1.20	ns	Figures 1 and 3
t_S	Setup Time D_n, P_n S_n	0.55 1.50		0.55 1.50		0.55 1.50		ns	Figure 4
t_H	Hold Time D_n, P_n S_n	0.70 0.50		0.70 0.50		0.70 0.50		ns	
$t_{pw(H)}$	Pulse Width HIGH CP	2.00		2.00		2.00		ns	Figure 3
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Clock to Output Path	200		200		200		ps	PCC Only (Note 1)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Clock to Output Path	200		200		200		ps	PCC Only (Note 1)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Clock to Output Path	250		250		250		ps	PCC Only (Note 1)
t_{ps}	Maximum Skew Pin (Signal) Transition Variation Clock to Output Path	250		250		250		ps	PCC Only (Note 1)

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{ps} guaranteed by design

Note 2: The propagation delay specified is for the switching of a single output. Delays may vary up to 0.40 ns if multiple outputs are switching simultaneously.

Industrial Version

PCC DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -40^\circ C$ to $+85^\circ C$ (Note 1)

Symbol	Parameter	$T_C = -40^\circ C$		$T_C = 0^\circ C$ to $+85^\circ C$		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	-1085	-870	-1025	-870	mV	$V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$	Loading with 50Ω to $-2.0V$
V_{OL}	Output LOW Voltage	-1830	-1575	-1830	-1620	mV		
V_{OHC}	Output HIGH Voltage	-1095		-1035		mV	$V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$	Loading with 50Ω to $-2.0V$
V_{OLC}	Output LOW Voltage		-1565		-1610	mV		
V_{IH}	Input HIGH Voltage	-1170	-870	-1165	-870	mV	Guaranteed HIGH Signal for all Inputs	
V_{IL}	Input LOW Voltage	-1830	-1480	-1830	-1475	mV	Guaranteed LOW Signal for all Inputs	
I_{IL}	Input LOW Current	0.50		0.50		μA	$V_{IN} = V_{IL}(\text{Min})$	
I_{IH}	Input HIGH Current		240		240	μA	$V_{IN} = V_{IH}(\text{Max})$	
I_{EE}	Power Supply Current	-157	-75	-157	-75	mA	Inputs Open	
		-167	-75	-167	-75	mA	$V_{EE} = -4.2V$ to $-4.8V$ $V_{EE} = -4.2V$ to $-5.7V$	

Note 1: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Industrial Version (Continued)

PCC AC Electrical Characteristics

$$V_{EE} = -4.2V \text{ to } -5.7V, V_{CC} = V_{CCA} = GND$$

Symbol	Parameter	$T_C = -40^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{max}	Max Clock Frequency	425		425		425		MHz	Figures 2 and 3
t_{PLH} t_{PHL}	Propagation Delay CP to Output	0.90	1.80	1.00	1.80	1.00	1.90	ns	Figures 1 and 3 (Note 1)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.30	1.90	0.35	1.20	0.35	1.20	ns	Figures 1 and 3
t_s	Setup Time D_n, P_n S_n	0.60		0.55		0.55		ns	Figure 4
		1.70		1.50		1.50			
t_h	Hold Time D_n, P_n S_n	0.90		0.70		0.70		ns	
		0.50		0.50		0.50			
$t_{pw(H)}$	Pulse Width HIGH CP	2.00		2.00		2.00		ns	Figure 3

Note 1: The propagation delay specified is for the switching of a single output. Delays may vary up to 0.40 ns if multiple outputs are switching simultaneously.

Military Version

DC Electrical Characteristics

$$V_{EE} = -4.2V \text{ to } -5.7V, V_{CC} = V_{CCA} = GND, T_C = -55^\circ C \text{ to } +125^\circ C$$

Symbol	Parameter	Min	Max	Units	T_C	Conditions	Notes	
V_{OH}	Output HIGH Voltage	-1025	-870	mV	$0^\circ C \text{ to } +125^\circ C$	$V_{IN} = V_{IH} \text{ (Max)}$ or $V_{IL} \text{ (Min)}$	Loading with 50Ω to $-2.0V$	1, 2, 3
		-1085	-870	mV	$-55^\circ C$			
V_{OL}	Output LOW Voltage	-1830	-1620	mV	$0^\circ C \text{ to } +125^\circ C$	$V_{IN} = V_{IH} \text{ (Min)}$ or $V_{IL} \text{ (Max)}$	Loading with 50Ω to $-2.0V$	1, 2, 3
		-1830	-1555	mV	$-55^\circ C$			
V_{OHC}	Output HIGH Voltage	-1035		mV	$0^\circ C \text{ to } +125^\circ C$	$V_{IN} = V_{IH} \text{ (Min)}$ or $V_{IL} \text{ (Max)}$	Loading with 50Ω to $-2.0V$	1, 2, 3
V_{OLC}	Output LOW Voltage		-1610	mV	$0^\circ C \text{ to } +125^\circ C$			
			-1555	mV	$-55^\circ C$			
V_{IH}	Input HIGH Voltage	-1165	-870	mV	$-55^\circ C \text{ to } +125^\circ C$	Guaranteed HIGH Signal for All Inputs	1, 2, 3, 4	
V_{IL}	Input LOW Current	-1830	-1475	mV	$-55^\circ C \text{ to } +125^\circ C$	Guaranteed LOW Signal for All Inputs	1, 2, 3, 4	
I_{IL}	Input LOW Current	0.50		μA	$-55^\circ C \text{ to } +125^\circ C$	$V_{EE} = -4.2V$ $V_{IN} = V_{IL} \text{ (Min)}$	1, 2, 3	
I_{IH}	Input High Current		240	μA	$0^\circ C \text{ to } +125^\circ C$	$V_{EE} = -5.7V$ $V_{IN} = V_{IH} \text{ (Max)}$	1, 2, 3	
			340	μA	$-55^\circ C$			
I_{EE}	Power Supply Current	-168	-55	mA	$-55^\circ C \text{ to } +125^\circ C$	Inputs Open $V_{EE} = -4.2V \text{ to } -4.8V$ $V_{EE} = -4.2V \text{ to } -5.7V$	1, 2, 3	
		-178	-55	mA				

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specifications which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at $-55^\circ C$, $+25^\circ C$ and $+125^\circ C$, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at $-55^\circ C$, $+25^\circ C$, and $+125^\circ C$, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL} .

Military Version (Continued)

AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -55^\circ C$		$T_C = +25^\circ C$		$T_C = +125^\circ C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
f_{max}	Max Clock Frequency	400		400		300		MHz	Figures 2 and 3	4
t_{PLH} t_{PHL}	Propagation Delay CP to Output	0.50	2.50	0.70	2.30	0.70	2.80	ns	Figures 1 and 3	1, 2, 3, 5
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.30	1.90	0.30	1.80	0.30	1.90	ns		
t_s	Setup Time D_n, P_n S_n	0.60 1.70		0.60 1.60		0.60 2.40		ns	Figure 4	4
t_h	Hold Time D_n, P_n S_n	0.90 0.50		0.90 0.50		0.90 0.50		ns		
$t_{pw(H)}$	Pulse Width HIGH CP	2.00		2.00		2.00		ns	Figure 3	

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately after power-up. This provides "cold start" specifications which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at $+25^\circ C$ temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table 1) on each manufactured lot at $+25^\circ C$, Subgroup A9, and at $+125^\circ C$ and $-55^\circ C$ temperatures, Subgroups A10 and A11.

Note 4: Not tested at $+25^\circ C$, $+125^\circ C$ and $-55^\circ C$ temperature (design characterization data).

Note 5: The propagation delay specified is for the switching of a single output. Delays may vary up to 0.40 ns if multiple outputs are switching simultaneously.

Test Circuitry

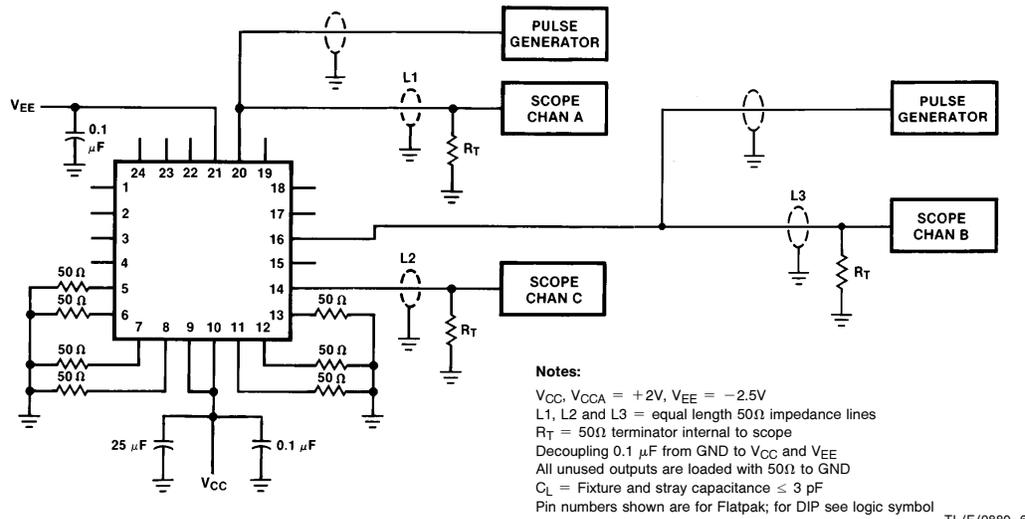


FIGURE 1. AC Test Circuit

TL/F/9880-6

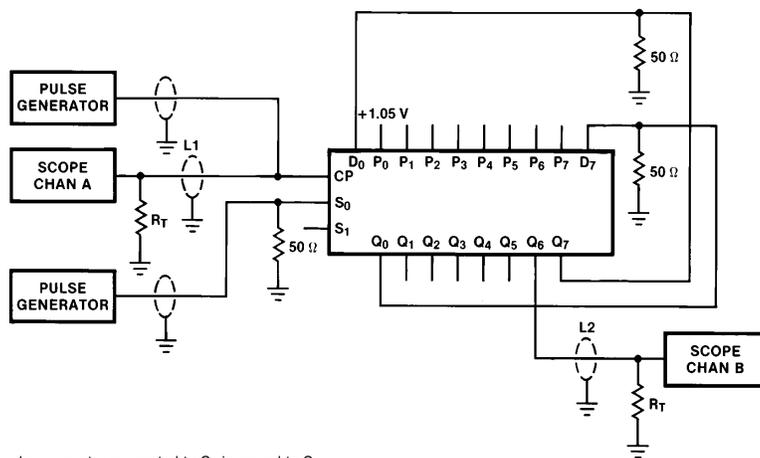
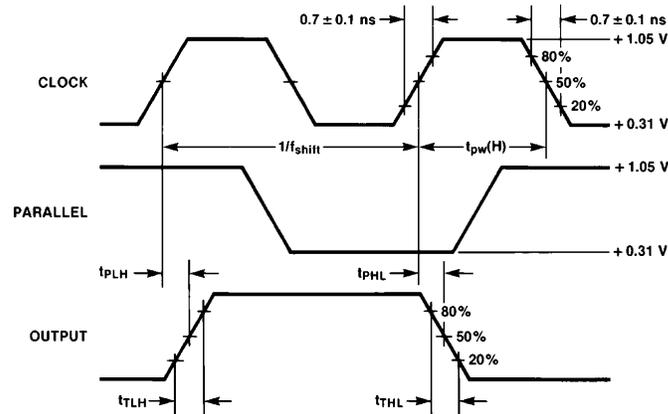


FIGURE 2. Shift Frequency Test Circuit (Shift Left)

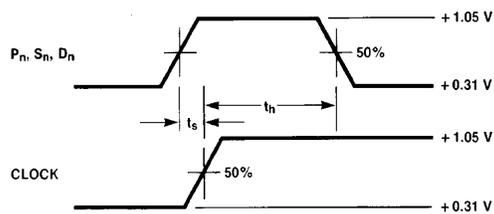
TL/F/9880-7

Switching Waveforms



TL/F/9880-8

FIGURE 3. Propagation Delay and Transition Times



Notes:

t_s is the minimum time before the transition of the clock that information must be present at the data input.

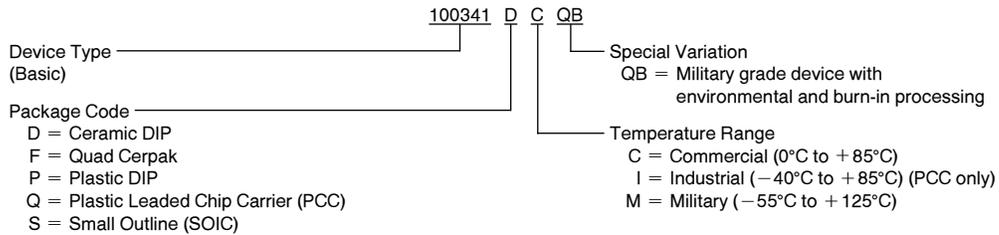
t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

TL/F/9880-9

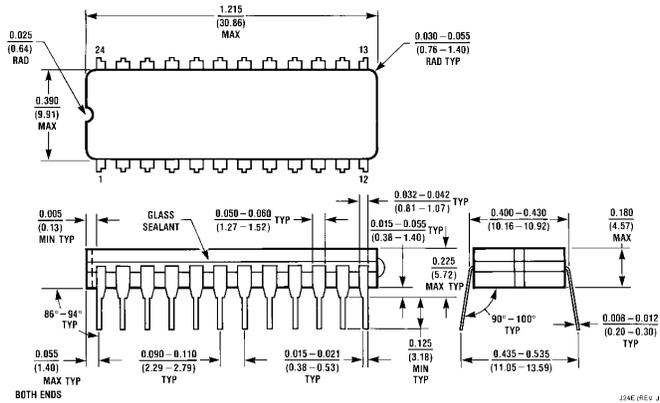
FIGURE 4. Setup and Hold Times

Ordering Information

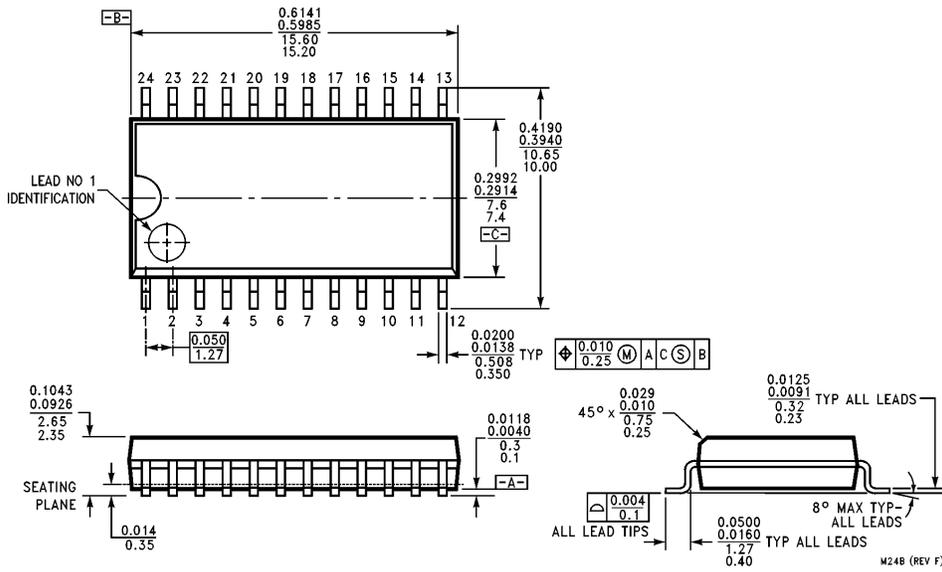
The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:



Physical Dimensions inches (millimeters)

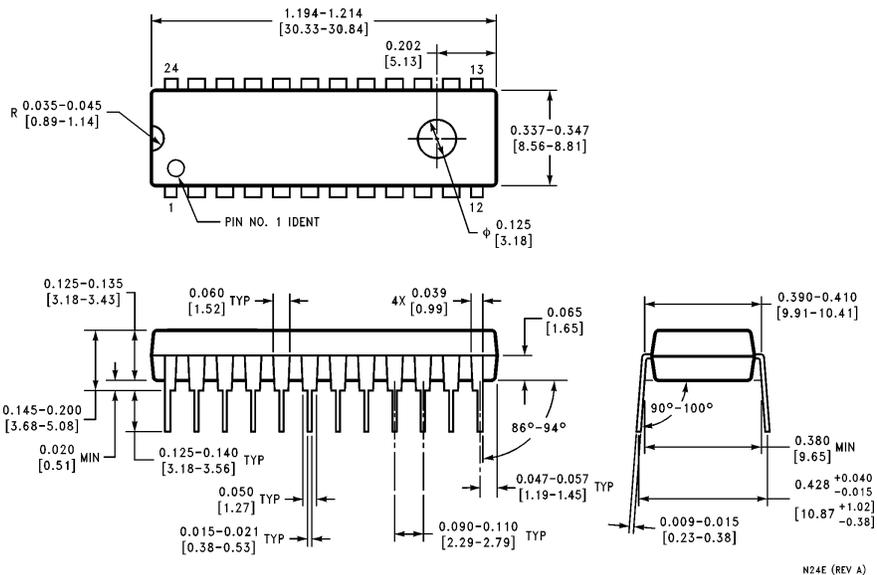


24-Lead Ceramic Dual-In-Line Package (0.400" Wide) (D)
NS Package Number J24E

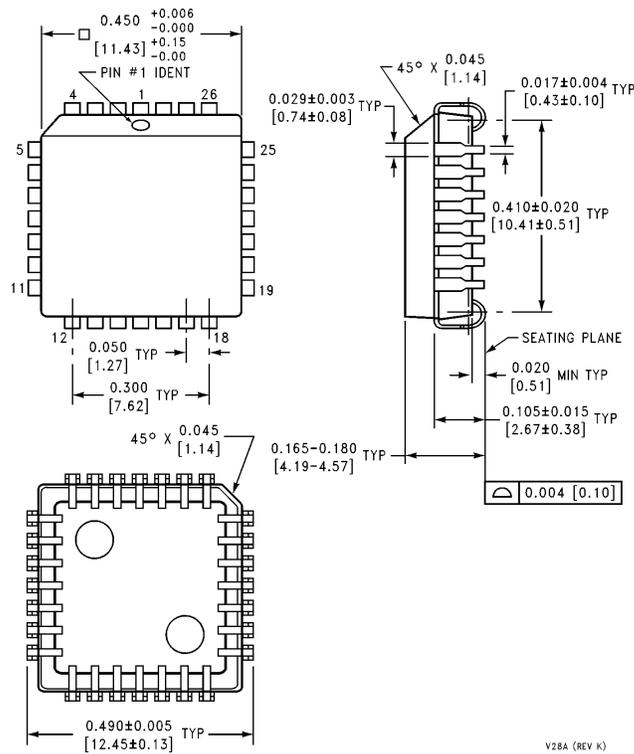


24-Lead Molded Package (0.300" Wide) (S)
NS Package Number M24B

Physical Dimensions inches (millimeters) (Continued)



24-Lead Plastic Dual-In-Line Package (P)
NS Package Number N24E

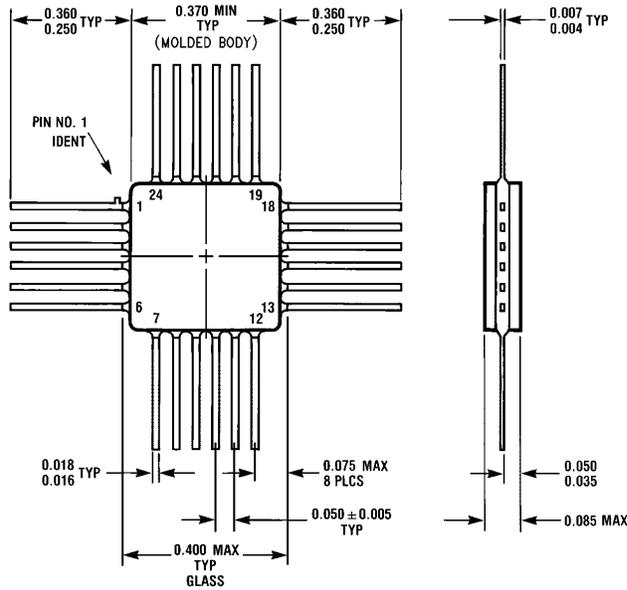


28-Lead Plastic Chip Carrier (Q)

NS Package Number V28A

Physical Dimensions inches (millimeters) (Continued)

Lit. # 114915



W24B (REV D)

**24-Lead Quad Cerpak (F)
NS Package Number W24B**

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National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
19th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
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