

AZ10LVEL33 AZ100LVEL33

ECL/PECL $\div 4$ Divider

FEATURES

- Operating Range of 3.0V to 5.5V
- 470ps Propagation Delay
- 4.0GHz Toggle Frequency
- Internal Input Pulldown Resistors
- Direct Replacement for ON Semiconductor MC10EL33, MC100EL33 and MC100LVEL33
- Transistor Count = 91 Devices

PACKAGE AVAILABILITY

PACKAGE	PART NO.	MARKING
MLP 16	AZ10/100LVEL33L	AZML33
MLP 16	AZ10/100LVEL33LR1	AZML33
MLP 16	AZ10/100LVEL33LR2	AZML33
SOIC 8	AZ10LVEL33D	AZM10LVEL33
SOIC 8 T&R	AZ10LVEL33DR1	AZM10LVEL33
SOIC 8 T&R	AZ10LVEL33DR2	AZM10LVEL33
SOIC 8	AZ100LVEL33D	AZM100LVEL33
SOIC 8 T&R	AZ100LVEL33DR1	AZM100LVEL33
SOIC 8 T&R	AZ100LVEL33DR2	AZM100LVEL33
TSSOP 8	AZ10LVEL33T	AZTLV33
TSSOP 8 T&R	AZ10LVEL33TR1	AZTLV33
TSSOP 8 T&R	AZ10LVEL33TR2	AZTLV33
TSSOP 8	AZ100LVEL33T	AZHLV33
TSSOP 8 T&R	AZ100LVEL33TR1	AZHLV33
TSSOP 8 T&R	AZ100LVEL33TR2	AZHLV33

DESCRIPTION

The AZ10/100LVEL33 is an integrated $\div 4$ divider. The reset pin is asynchronous and clears the output (Q Low, $\bar{Q}$ High) on the rising edge. Upon power-up, the internal flip-flop will be in a random logic state; the reset allows for the synchronization of multiple LVEL33's in a system.

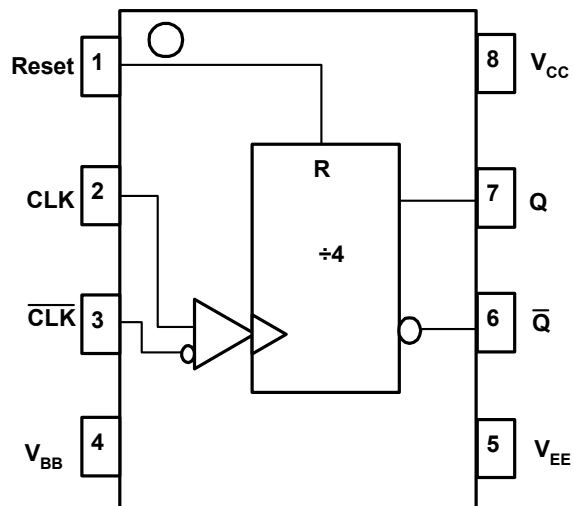
The LVEL33 provides a V_{BB} output for single-end use or a DC bias reference for AC coupling to the device. For single-ended input applications, the V_{BB} reference should be connected to one side of the CLK/ $\bar{CLK}$ differential input pair. The input signal is then fed to the other CLK/ $\bar{CLK}$ input. The V_{BB} pin can support 1.0mA sink/source current. When used, the V_{BB} pin should be bypassed to ground via a 0.01 μ F capacitor.

NOTE: Specifications in the ECL/PECL tables are valid when thermal equilibrium is established.

LOGIC DIAGRAM AND PINOUT ASSIGNMENT

PIN DESCRIPTION

PIN	FUNCTION
CLK, $\bar{CLK}$	Clock Inputs
Reset	Asynch Reset
V_{BB}	Reference Voltage Output
Q, $\bar{Q}$	Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply



AZ10LVEL33

AZ100LVEL33

Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Rating	Unit
V_{CC}	PECL Power Supply ($V_{EE} = 0V$)	0 to +8.0	Vdc
V_I	PECL Input Voltage ($V_{EE} = 0V$)	0 to +6.0	Vdc
V_{EE}	ECL Power Supply ($V_{CC} = 0V$)	-8.0 to 0	Vdc
V_I	ECL Input Voltage ($V_{CC} = 0V$)	-6.0 to 0	Vdc
I_{OUT}	Output Current --- Continuous --- Surge	50 100	mA
T_A	Operating Temperature Range	-40 to +85	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C

10K ECL DC Characteristics ($V_{EE} = -3.0V$ to $-5.5V$, $V_{CC} = GND$)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage ¹	-1080		-890	-1020		-840	-980		-810	-910		-720	mV
V_{OL}	Output LOW Voltage ¹	-1950		-1650	-1950		-1630	-1950		-1630	-1950		-1595	mV
V_{IH}	Input HIGH Voltage	-1230		-890	-1170		-840	-1130		-810	-1060		-720	mV
V_{IL}	Input LOW Voltage	-1950		-1500	-1950		-1480	-1950		-1480	-1950		-1445	mV
V_{BB}	Reference Voltage	-1430		-1300	-1380		-1270	-1350		-1250	-1310		-1190	mV
I_{IL}	Input LOW Current	-150			-150			-150			-150			μA
I_{IH}	Input HIGH Current			150			150			150			150	μA
I_{EE}	Power Supply Current		27	33		27	33		27	33		27	33	mA

- Each output is terminated through a 50Ω resistor to $V_{CC} - 2V$.

10K LVPECL DC Characteristics ($V_{EE} = GND$, $V_{CC} = +3.3V$)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage ^{1,2}	2220		2410	2280		2460	2320		2490	2390		2580	mV
V_{OL}	Output LOW Voltage ^{1,2}	1350		1650	1350		1670	1350		1670	1350		1705	mV
V_{IH}	Input HIGH Voltage ¹	2070		2410	2130		2460	2170		2490	2240		2580	mV
V_{IL}	Input LOW Voltage ¹	1350		1800	1350		1820	1350		1820	1350		1855	mV
V_{BB}	Reference Voltage ¹	1870		2000	1920		2030	1950		2050	1990		2110	mV
I_{IL}	Input LOW Current	-150			-150			-150			-150			μA
I_{IH}	Input HIGH Current			150			150			150			150	μA
I_{EE}	Power Supply Current		27	33		27	33		27	33		27	33	mA

- For supply voltages other than 3.3V, use the ECL table values and ADD supply voltage value.
- Each output is terminated through a 50Ω resistor to $V_{CC} - 2V$.

10K PECL DC Characteristics ($V_{EE} = GND$, $V_{CC} = +5.0V$)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage ^{1,2}	3920		4110	3980		4160	4020		4190	4090		4280	mV
V_{OL}	Output LOW Voltage ^{1,2}	3050		3350	3050		3370	3050		3370	3050		3405	mV
V_{IH}	Input HIGH Voltage ¹	3770		4110	3830		4160	3870		4190	3940		4280	mV
V_{IL}	Input LOW Voltage ¹	3050		3500	3050		3520	3050		3520	3050		3555	mV
V_{BB}	Reference Voltage ¹	3570		3700	3620		3730	3650		3750	3690		3810	mV
I_{IL}	Input LOW Current	-150			-150			-150			-150			μA
I_{IH}	Input HIGH Current			150			150			150			150	μA
I_{EE}	Power Supply Current		27	33		27	33		27	33		27	33	mA

- For supply voltages other than 5.0V, use the ECL table values and ADD supply voltage value.
- Each output is terminated through a 50Ω resistor to $V_{CC} - 2V$.

AZ10LVEL33

AZ100LVEL33

100K ECL DC Characteristics ($V_{EE} = -3.0V$ to $-5.5V$, $V_{CC} = GND$)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage ¹	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	-1025	-955	-880	mV
V_{OL}	Output LOW Voltage ¹	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	-1810	-1705	-1620	mV
V_{IH}	Input HIGH Voltage	-1165		-880	-1165		-880	-1165		-880	-1165		-880	mV
V_{IL}	Input LOW Voltage	-1810		-1475	-1810		-1475	-1810		-1475	-1810		-1475	mV
V_{BB}	Reference Voltage	-1380		-1260	-1380		-1260	-1380		-1260	-1380		-1260	mV
I_{IL}	Input LOW Current	-150			-150			-150			-150			μA
I_{IH}	Input HIGH Current			150			150			150			150	μA
I_{EE}	Power Supply Current		27	33		27	33		27	33		31	37	mA

- Each output is terminated through a 50Ω resistor to $V_{CC} - 2V$.

100K LVPECL DC Characteristics ($V_{EE} = GND$, $V_{CC} = +3.3V$)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage ^{1,2}	2215	2295	2420	2275	2345	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage ^{1,2}	1470	1605	1745	1490	1595	1680	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage ¹	2135		2420	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage ¹	1490		1825	1490		1825	1490		1825	1490		1825	mV
V_{BB}	Reference Voltage ¹	1920		2040	1920		2040	1920		2040	1920		2040	mV
I_{IL}	Input LOW Current	-150			-150			-150			-150			μA
I_{IH}	Input HIGH Current			150			150			150			150	μA
I_{EE}	Power Supply Current		27	33		27	33		27	33		31	37	mA

- For supply voltages other than 3.3V, use the ECL table values and ADD supply voltage value.
- Each output is terminated through a 50Ω resistor to $V_{CC} - 2V$.

100K PECL DC Characteristics ($V_{EE} = GND$, $V_{CC} = +5.0V$)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage ^{1,2}	3915	3995	4120	3975	4045	4120	3975	4045	4120	3975	4045	4120	mV
V_{OL}	Output LOW Voltage ^{1,2}	3170	3305	3445	3190	3295	3380	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage ¹	3835		4120	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage ¹	3190		3525	3190		3525	3190		3525	3190		3525	mV
V_{BB}	Reference Voltage ¹	3620		3740	3620		3740	3620		3740	3620		3740	mV
I_{IL}	Input LOW Current	-150			-150			-150			-150			μA
I_{IH}	Input HIGH Current			150			150			150			150	μA
I_{EE}	Power Supply Current		27	33		27	33		27	33		31	37	mA

- For supply voltages other than 5.0V, use the ECL table values and ADD supply voltage value.
- Each output is terminated through a 50Ω resistor to $V_{CC} - 2V$.

AZ10LVEL33

AZ100LVEL33

AC Characteristics ($V_{EE} = -3.0V$ to $-5.5V$; $V_{CC} = GND$ or $V_{EE} = GND$; $V_{CC} = +3.0V$ to $+5.5V$)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency	3.4	4.0		3.8	4.0		3.8	4.0		3.8	4.0		GHz
t_{PLH} / t_{PHL}	Propagation Delay CLK to Q	360	450	540	320	460	550	380	470	560	400	490	580	ps
	Reset to Q	310	460	610	340	460	580	360	460	560	380	480	580	
t_{RR}	Reset Recovery	300			300			300			300			ps
t_{skew}	Within-Device Skew			20			20			20			20	ps
$V_{PP} (AC)$	Minimum Input Swing ¹	150			150			150			150			mV
V_{CMR}	Common Mode Range ²	$V_{EE} +$		$V_{CC} -$	$V_{EE} +$		$V_{CC} -$	$V_{EE} +$		$V_{CC} -$	$V_{EE} +$		$V_{CC} -$	V
	$V_{pp} < 500mV$	1.2		0.4	1.1		0.4	1.1		0.4	1.1		0.4	
	$V_{pp} \geq 500mV$	1.4		0.4	1.3		0.4	1.3		0.4	1.3		0.4	
t_r / t_f	Output Rise/Fall Times Q (20% - 80%)	100		260	100		260	100		260	100		260	ps

- V_{PP} is the minimum peak-to-peak differential input swing for which AC parameters are guaranteed.
- The V_{CMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and peak to peak voltage lies between $V_{PP}(\min)$ and 1V.

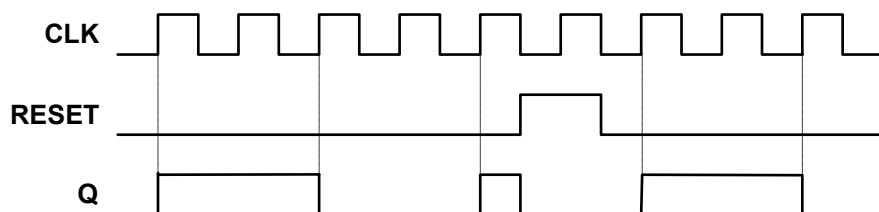
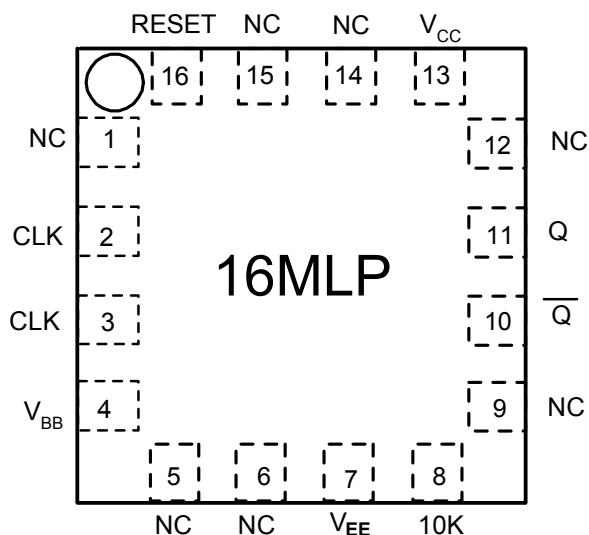
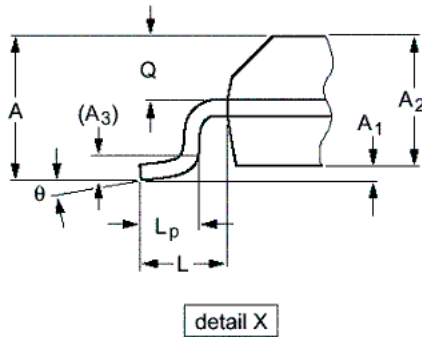
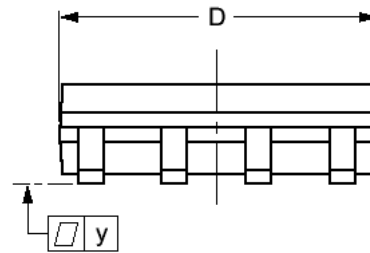
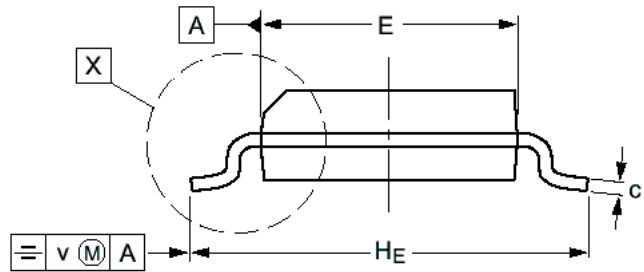
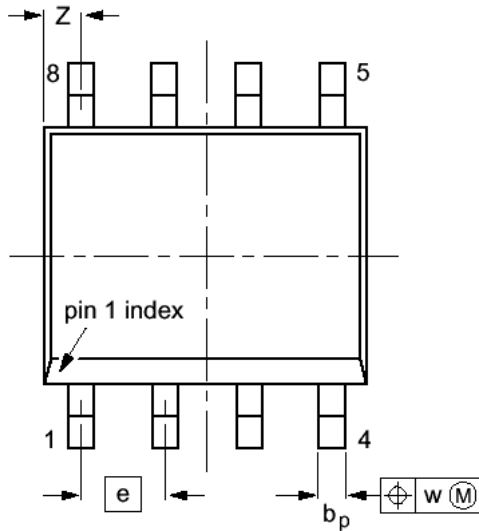


Figure 1. Timing Diagram



**PACKAGE DIAGRAM
SOIC 8**

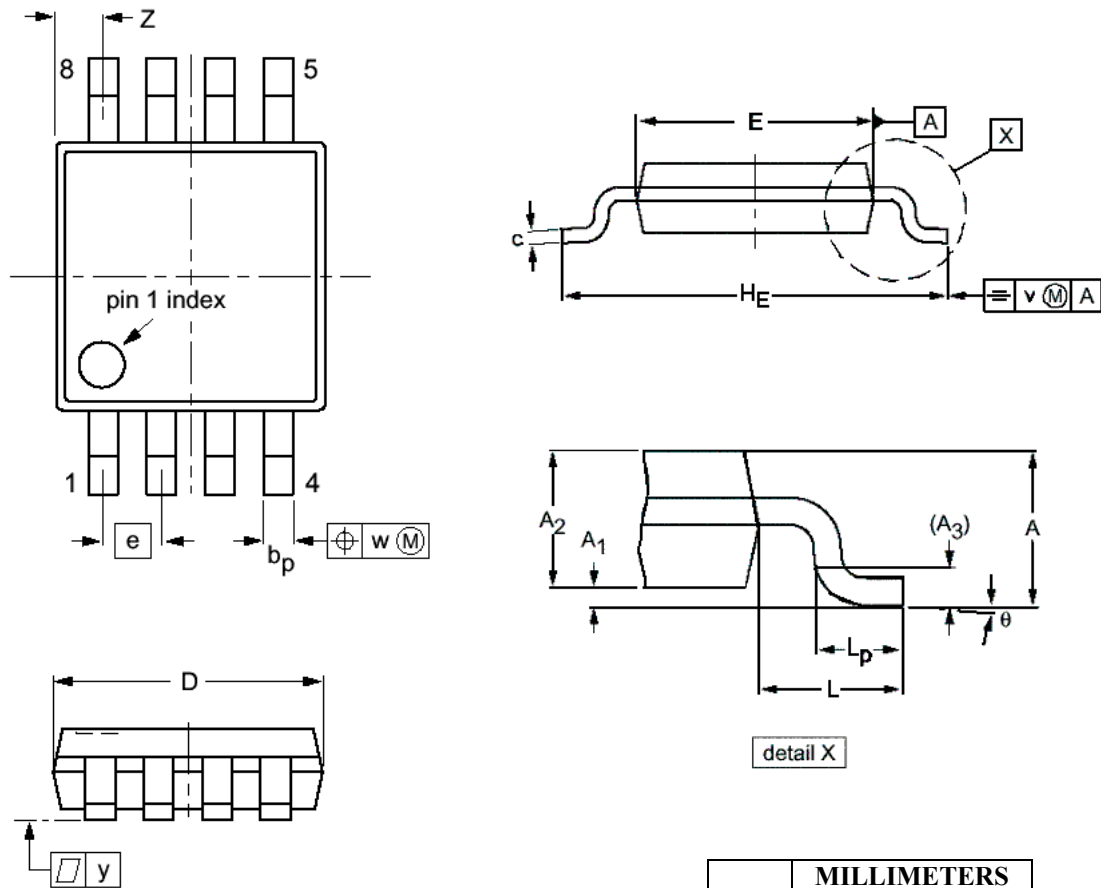


NOTES:

1. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
2. MAXIMUM MOLD PROTRUSION FOR D IS 0.15mm.
3. MAXIMUM MOLD PROTRUSION FOR E IS 0.25mm.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A		1.75		0.069
A ₁	0.10	0.25	0.004	0.010
A ₂	1.25	1.45	0.049	0.057
A ₃	0.25		0.01	
b _p	0.36	0.49	0.014	0.019
c	0.19	0.25	0.0075	0.0100
D	4.8	5.0	0.19	0.20
E	3.8	4.0	0.15	0.16
e	1.27		0.050	
H _E	5.80	6.20	0.228	0.244
L	1.05		0.041	
L _p	0.40	1.00	0.016	0.039
Q	0.60	0.70	0.024	0.028
v	0.25		0.01	
w	0.25		0.01	
y	0.10		0.004	
Z	0.30	0.70	0.012	0.028
θ	0°	8°	0°	8°

**PACKAGE DIAGRAM
TSSOP 8**

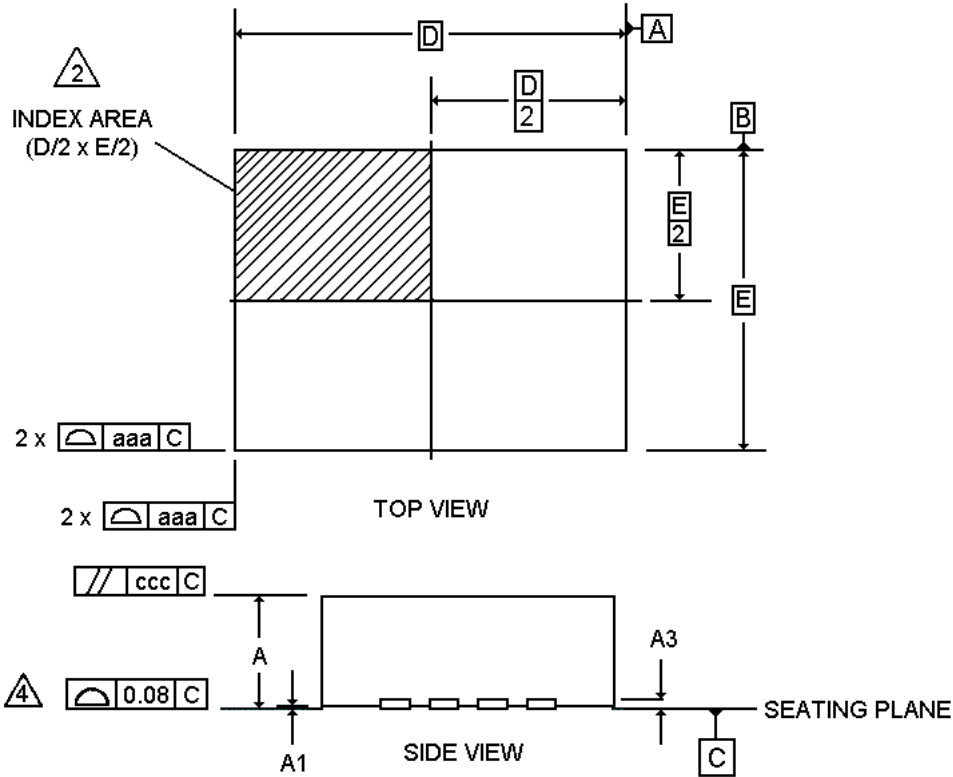


NOTES:

1. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
2. MAXIMUM MOLD PROTRUSION FOR D IS 0.15mm.
3. MAXIMUM MOLD PROTRUSION FOR E IS 0.25mm.

DIM	MILLIMETERS	
	MIN	MAX
A		1.10
A ₁	0.05	0.15
A ₂	0.80	0.95
A ₃	0.25	
b _p	0.25	0.45
c	0.15	0.28
D	2.90	3.10
E	2.90	3.10
e	0.65	
H _E	4.70	5.10
L	0.94	
L _p	0.40	0.70
v	0.10	
w	0.10	
y	0.10	
Z	0.35	0.70
θ	0°	6°

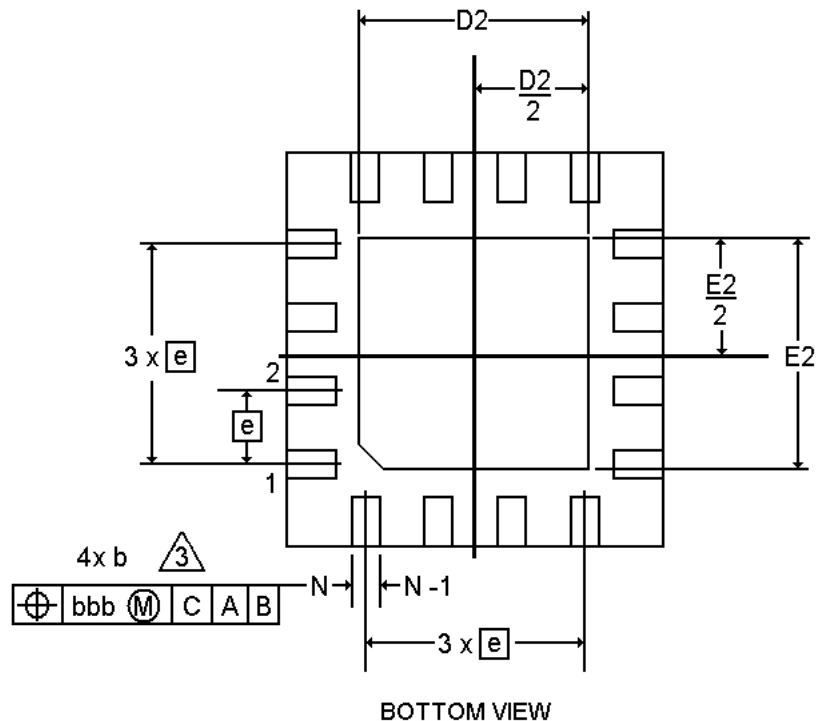
PACKAGE DIAGRAM
MLP 16



NOTES

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME T14-1994.
2. THE TERMINAL #1 AND PAD NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012.
3. DIMENSION b APPLIES TO METALLIC PAD AND IS MEASURED BETWEEN PAD AND IS 0.30mm FROM PAD TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.25 REF	
b	0.18	0.30
D	2.90	3.10
D2	0.25	1.95
E	2.90	3.10
E2	0.25	1.95
e	0.50 BSC	
L	0.30	0.50
aaa	0.25	
bbb	0.10	
ccc	0.10	



AZ10LVEL33
AZ100LVEL33

Arizona Microtek, Inc. reserves the right to change circuitry and specifications at any time without prior notice. Arizona Microtek, Inc. makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Arizona Microtek, Inc. assume any liability arising out of the application or use of any product or circuit and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Arizona Microtek, Inc. does not convey any license rights nor the rights of others. Arizona Microtek, Inc. products are not designed, intended or authorized for use as components in systems intended to support or sustain life, or for any other application in which the failure of the Arizona Microtek, Inc. product could create a situation where personal injury or death may occur. Should Buyer purchase or use Arizona Microtek, Inc. products for any such unintended or unauthorized application, Buyer shall indemnify and hold Arizona Microtek, Inc. and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Arizona Microtek, Inc. was negligent regarding the design or manufacture of the part.