TOSHIBA

TOSHIBA BIPOLAR DIGITAL INTEGRATED CIRCUIT   SILICON MONOLITHIC

TD62445FN

LOW−SATURATION−TYPE SINK DRIVER WITH 4−CIRCUIT OVER−CURRENT DETECTION FUNCTION

The TD62445FN is a sink driver with over−current detector circuits. Each of four circuits can setting the limit current. Using an internal comparator, the TD62445FN detects over−current by comparing the current output through the external resistors as voltage. Over current detection is detected by the ERR terminal which is an open collector, comes on. Construct a system so that the input signal turns off immediately the ERR pin comes on.

SSOP18-P-225-0.65

Weight: 0.08 g (Typ.)

FEATURES

- Includes current limiter circuits:
  By connecting external resistors, each bit can be set to any limit current value.
- Includes an error detection signal filter pin:
  Connecting any capacitor between the LP pin and the GND filters the internal comparator detection signal and outputs this to the ERR pin.
- Over−current monitor detection output:
  Includes an ERR pin output to warn when current exceeds the limit. Construct a system so that the input signal turns off immediately the ERR pin comes on (open collector).
- Common input pin (CO−IN (pin 4)) :
  Using this pin, the four over−current detector circuits can be forcibly turned off together.
- Low−saturation−type output (open collector):
  The voltage drop between the collector and emitter is V_{OL1} = 0.4 V (max) @ I_O = 100 mA.
- Supply voltage   : V_{CC} = 4.5 to 5.5
- Input is TTL compatible.
- Ultra−compact package   : SSOP 18 pins (0.65mm pitch)
- Output rating   : V_{CEO} = 30 V, I_O = 150 mA / ch
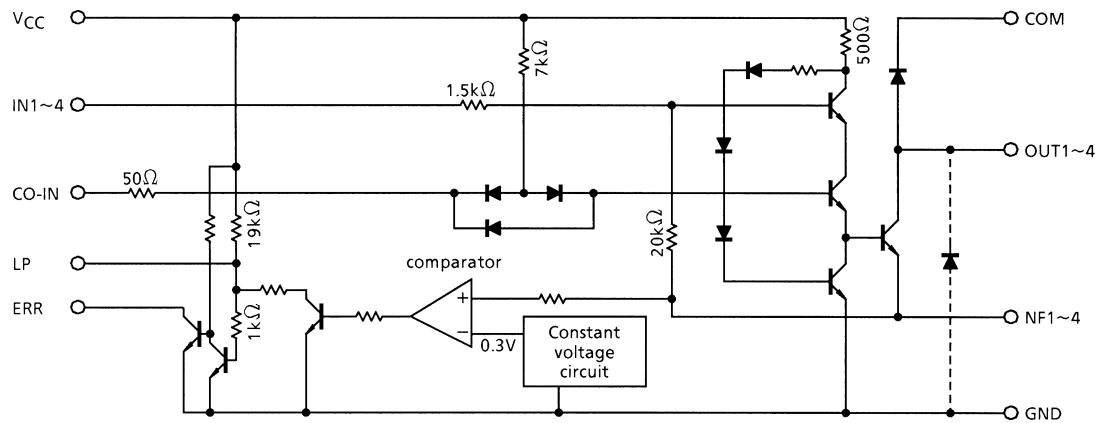- Packing   : Embossed taping only
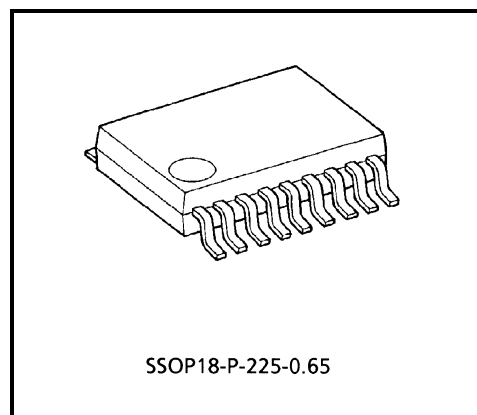
PIN CONNECTION (TOP VIEW)
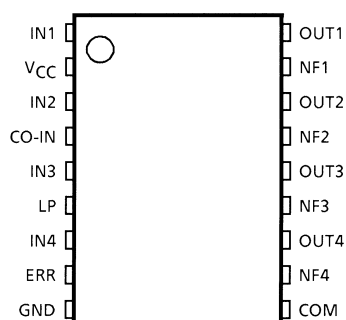
EQUIVALENT CIRCUIT DIAGRAM (Showing One Circuit)

- When the output pins of this IC are connected to the load power supply, over−current may flow to the outputs. While the device includes an over−current detection function, the device is not designed for applications where the output pins and load power supply are intentionally connected.

- Be sure to use the device with the NF1 to 4 and the GND pins connected via resistors or directly connected. Do not use with the NF1 to 4 pins open.
  This also applies to unused channels. If the pins are not connected, the operation of the over−current detection function is unstable.
  Note that if the NF1 to 4 and GND pins are directly connected, the over−current detection function does not operate.

- A parasitic diode is installed between the GND and output pins. While current is supplied to this diode, other circuit outputs may come on or be otherwise affected.   If this phenomenon adversely affects the operation of the device, Toshiba recommends connecting an external diode.

TRUTH TABLE

IN1~4	CO−IN	OUT1~4	VOLTAGE BETWEEN NF1 TO 4 AND GND	ERR
L	H	OFF	0 V	OFF
H	H	ON	0.3 V max	OFF
H	H	ON	0.3 V min	ON
X	L	OFF	0 V	OFF

Note: The above comparator circuit assumes some resistance connected between the NF1 to 4 and GND pins when the circuit operates.

2001-07-04

PIN DESCRIPTION

PIN No.	PIN NAME	FUNCTION
1, 3, 5, 7	IN1 to 4	Driver input pins. TTL compatible input level. At high level the output is on; at low level the output is off.
2	V_{CC}	Power supply voltage pin.
4	CO−IN	Output control pin. When high the output operates in accordance with input logic; when low the output is forcibly turned off regardless of the input logic.
6	LP	CR filter circuit pin. Connecting a capacitor to the GND creates a filter for the over−current detection signal from the comparator. When not in use, leave open.
8	ERR	Over−current detection signal output pin. Comes on when excess current is detected. Normally, set to high impedance.
9	GND	GND pin.
10	COM	Clamp diode's common cathode pin.
17, 15, 13, 11	NF1 to 4	Resistor connecting pins for over−current detection setting. By connecting resistors between these pins and GND, the detection level can be set separately for each circuit.
18, 16, 14, 12	OUT1 to 4	Open collector output pins.

MAXIMUM RATINGS

CHARACTERISTICS	SIGNAL	RATING	UNIT
Power Supply Voltage	V_{CC}	7.0	V
COM Pin Voltage	V_{COM}	30.0	V
Output Voltage	V_{CEO}	30.0	V
ERR Pin Output Voltage	V_{ERR}	7.0	V
Output Sink Current	I_{OUT}	0~150	mA
ERR Pin Sink Current	I_{ERR}	10	mA
Input Voltage	V_{IN}	$-0.3~V_{CC} + 0.3$	V
NF Pin Voltage	$V_{IN\,(NF)}$	−0.3~1.0	V
LP Pin Voltage	$V_{IN\,(LP)}$	$-0.3~V_{CC} + 0.3$	V
Clamp Diode Reverse Voltage	V_{r1}	30	V
Clamp Diode Forward Current	I_{f1}	150	mA
Output Parasitic Diode Forward Current	I_{f2}	100	mA
Power Dissipation	P_D (Note)	960	mW
Operating Temperature	T_{opr}	−10~85	°C
Storage Temperature	T_{stg}	−55~150	°C

Note: When the device is mounted on a PCB (with one surface 50 × 50 × 1.6 mm Cu 40% glass epoxy)
When operating at an ambient temperature of 25°C or higher, derate the power dissipation at 7.6 mW / °C.

RECOMMENDED OPERATING CONDITIONS
(Unless otherwise specified, V_{CC} = 5.0 V, Ta = −10 to 85°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Power Supply Voltage	V_{CC}	—	4.5	5.0	5.5	V
Output Voltage	V_{CEO}	OUT1~4	0	—	30.0	V
	V_{ERR}	ERR	0	—	V_{CC} + 0.3	V
Output Current	I_{OUT}	—	0	—	120	mA
	I_{ERR}	ERR	0	—	8	mA
Input Voltage	V_{IN}	V_{CC} = 5.0V : IN1~4, CO−IN, LP	0	—	V_{CC}	V
Power Dissipation	P_{D1}	Ta = 60°C	—	—	0.69	W / IC
	P_{D2}	Ta = 85°C	—	—	0.50	W / IC

ELECTRICAL CHARACTERISTICS
(Unless otherwise specified, V_{CC} = 5.0 V ± 10%, Ta = −10 to 85°C, $V_{IN (NF)}$ = GND)

| CHARACTERISTIC	SYMBOL	TEST CIR−CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Operating Power Supply Voltage	V_{CC}	—	—	4.5	5.0	5.5	V
Output Leakage Current	I_{Oleak1}	1	V_{CE} = 30 V, V_{IN} = 0 V, Ta=25°C: OUT1~4	0	—	100	μA
	I_{Oleak2}	1	V_{CE} = 7.0V, V_{NF} = 0 V, Ta = 25°C : ERR	0	—	50	
Output Saturation Voltage	V_{OL1}	2	I_{OUT} = 100 mA, R_{NF} = 0 : OUT1~4	0	0.15	0.40	V
	V_{OL2}	3	I_{OL} = 10 mA : ERR	0	0.20	0.60	
Input Voltage	V_{I+}	3	V_{ERR} = "L", Ta = −10~85°C : NF1~4	0.25	0.30	0.35	V
	V_{IH}	2	IN1~4, CO−IN	2.50	—	—	
	V_{IL}	1	NF1~4, CO−IN	—	—	0.70	
Input Current	I_{IH}	2	V_{IN} = 2.5 V, Ta = 25°C: IN1~4	—	+0.5	+0.1	mA
	I_{IL1}	1	V_{IN} = 0.7 V, Ta = 25°C: IN1~4	—	+0.1	+0.1	
	I_{IL2}	1	V_{IN} = 0.7 V, Ta = 25°C: CO−IN	—	−1.0	−3.4	
Power Supply Current When Not Operating	I_{CC}	4	V_{IN} = 0.7 V: CO−IN, IN1~4, Ta = 25°C All outputs off	—	8	10	mA / IC
Power Supply Current When Operating	I_{CCopr}	4	V_{IN} = 2.5 V, I_{OUT} = 150 mA, Ta = 25°C All outputs on	—	40	70	mA / IC
Clamp Diode Forward Voltage	V_{f1}	5	If = 100 mA: OUT1~4 to COM	—	1.20	2.00	V
Clamp Diode Reverse Voltage	V_{r1}	1	Ir = 100 μA: COM to OUT1~4	30	—	—	V
Input / Output Delay Time	t_{PDIO1} (t_{pLH})	6	Ta = 25°C, V_{CE} = 30 V, I_{OUT} = 150 mA, C_L = 10 pF: IN1~4 to OUT1~4	—	(Note) 0.25	(Note) 1.25	μs
	t_{PDIO1} (t_{pHL})	6		—	(Note) 0.40	(Note) 2.00	

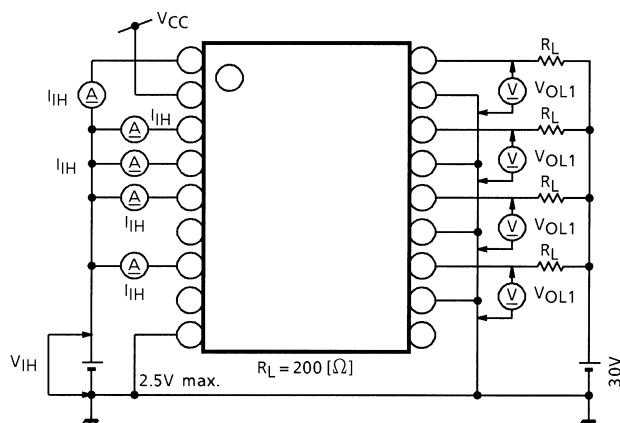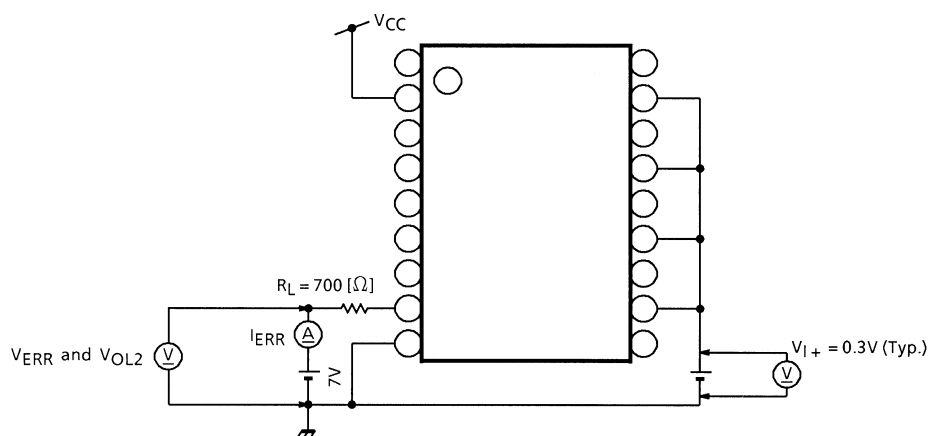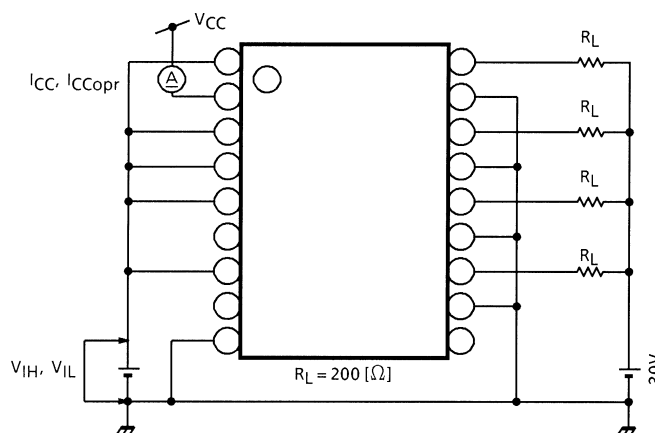Note: The switching characteristic values indicate the guaranteed design limits.

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Input / Output Delay Time	t_{PDIO2} (t_{pLH})	7	Ta = 25°C, V_{ERR} = 5.0 V, I_{OL} = 10 mA, C_L = 10 pF, V_{NF}=0 to 0.4 V: NF1~4 to ERR	—	(Note) 0.30	(Note) 1.50	µs
	t_{PDIO2} (t_{pHL})	7		—	(Note) 5.00	(Note) 15.0	
	t_{PDIO3} (t_{pLH})	6	Ta = 25°C, V_{CE} = 30 V, I_{OUT} = 150 mA, C_L = 50 pF: CO−IN to OUT1~4	—	(Note) 0.25	(Note) 1.25	
	t_{PDIO3} (t_{pHL})	6		—	(Note) 0.40	(Note) 2.00	
Output Rise Time	(t_{pLH})	6	Ta = 25°C, V_{CE} = 30 V, I_{OUT} = 150 mA, C_L = 50 pF, 10%−90%: OUT1~4	—	(Note) 0.40	(Note) 1.00	µs
	t_{rERR}	7	Ta = 25°C, V_{ERR} = 5.0 V, I_{OL} = 10 mA, C_L = 10 pF, 10%−90%: ERR	—	(Note) 0.40	(Note) 1.00	
Output Fall Time	t_{fOUT}	6	Ta=25°C, V_{CE} = 30 V, IOUT = 150 mA, C_L = 50 pF, 90%−10%: OUT1~4	—	(Note) 0.10	(Note) 1.00	µs
	t_{fERR}	7	Ta = 25°C, V_{ERR} = 5.0 V, I_{OL} = 10 mA, C_L = 10 pF, 90%−10%: ERR	—	(Note) 0.02	(Note) 1.00	

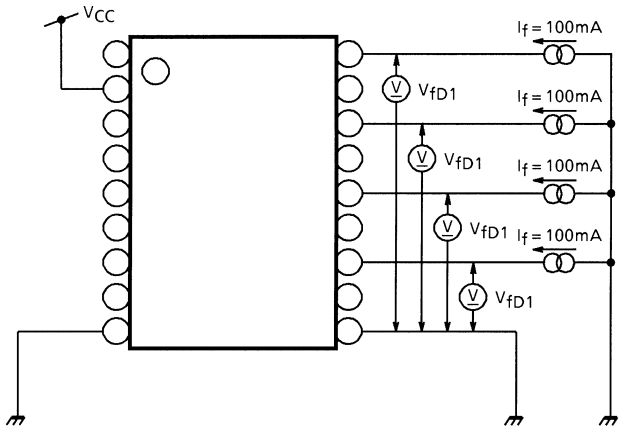Note: The switching characteristic values indicate the guaranteed design limits.

TEST CIRCUIT

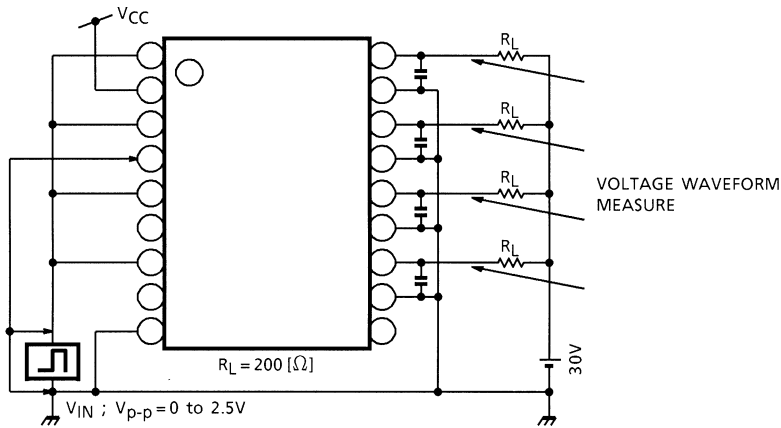**(1)** V_{IL}, $I_{IL1~2}$, V_{r1}, V_{CEO}, I_{Oleak1}, I_{Oleak2}
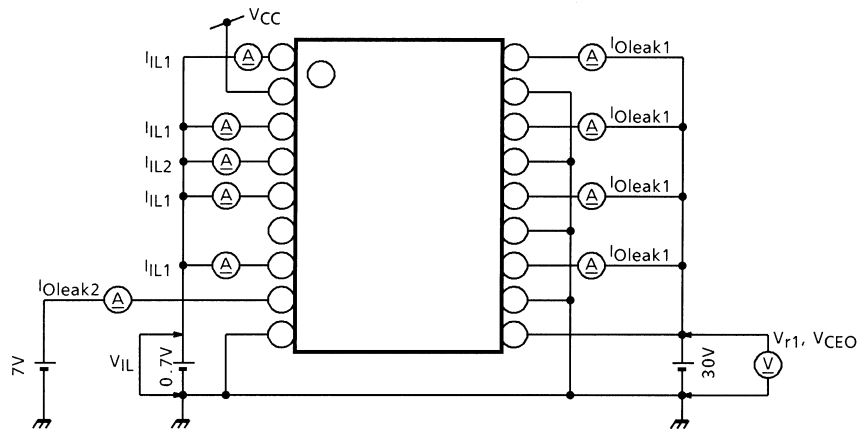
(2) V_{IH}, I_{IH}, V_{OL1}

(3) V_{I+}, V_{ERR}, I_{ERR}, V_{OL2}

(4) I_{CC}, I_{CCopr}

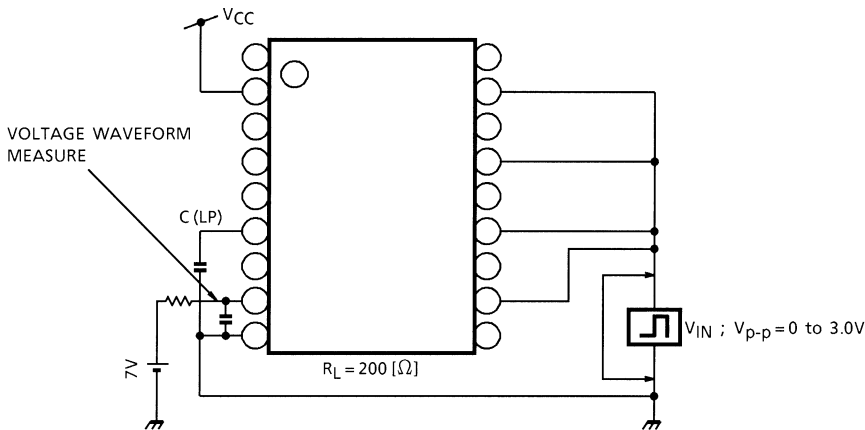**(5) V_f1**

(6) t_PDIO1, t_PDIO3, t_rOUT, t_fOUT

(7) t_PDIO2, t_rERR, t_fERR, C (LP)

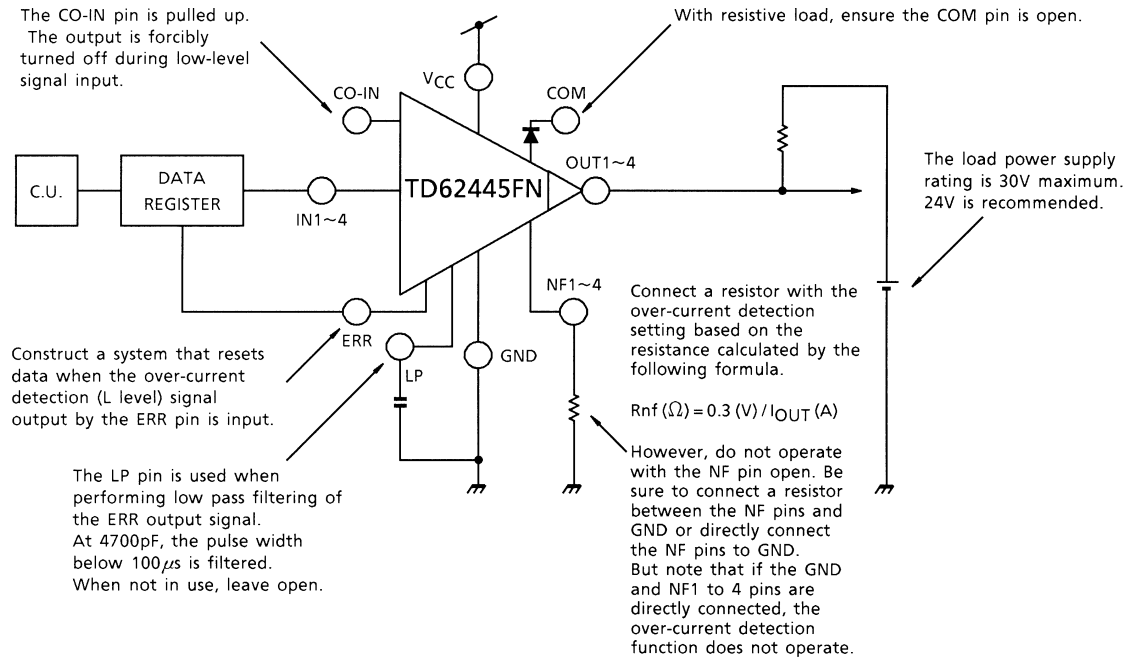## SWITCHING WAVEFORM

[$t_{PDIO1, 3}$, t_{rOUT}, t_{fOUT}]

[t_{PDIO2}, t_{rERR}, t_{fERR}]

APPLICATION CIRCUIT

1. Using resistive load drive

The CO-IN pin is pulled up.
The output is forcibly
turned off during low-level
signal input.

With resistive load, ensure the COM pin is open.

CO-IN

V_{CC}

COM

OUT1~4

C.U. — DATA REGISTER — TD62445FN

IN1~4

The load power supply
rating is 30V maximum.
24V is recommended.

NF1~4

ERR

LP

GND

Construct a system that resets
data when the over-current
detection (L level) signal
output by the ERR pin is input.

Connect a resistor with the
over-current detection
setting based on the
resistance calculated by the
following formula.

$$Rnf\,(\Omega) = 0.3\,(V) / I_{OUT}\,(A)$$

The LP pin is used when
performing low pass filtering of
the ERR output signal.
At 4700pF, the pulse width
below 100μs is filtered.
When not in use, leave open.

However, do not operate
with the NF pin open. Be
sure to connect a resistor
between the NF pins and
GND or directly connect
the NF pins to GND.
But note that if the GND
and NF1 to 4 pins are
directly connected, the
over-current detection
function does not operate.

2. Using inductive load (eg, relay) drive

The CO-IN pin is pulled up. The output is forcibly turned off during low-level signal input.

With inductive load, connect the COM pin to the load power supply.

The load power supply rating is 30V maximum. 24V is recommended.

CO-IN V_{CC} COM

TD62445FN

OUT1~4

IN1~4

NF1~4

ERR

LP   GND

C.U. — DATA REGISTER

$V_f = <0.7V$

Construct a system that resets data when the over-current detection (L level) signal output by the ERR pin is input.

The LP pin is used when performing low pass filtering of the ERR output signal. At 4700pF, the pulse width below $100 \mu s$ is filtered.
When not in use, leave open.

Connect a resistor with the over-current detection setting based on the resistance calculated by the following formula.

$$Rnf\,(\Omega) = 0.3\,(V) / I_{OUT}\,(A)$$

However, do not operate with the NF pin open. Be sure to connect a resistor between the NF pins and GND or directly connect the NF pins to GND.
But note that if the GND and NF1 to 4 pins are directly connected, the over-current detection function does not operate.

Depending on the load, when it is necessary to inductively guarantee the negative potential of the output pin, for example, where mutual inductance occurs, Toshiba recommends connecting external diodes.

PRECAUTIONS for USING

This IC does not integrate protection circuits such as overcurrent and overvoltage protectors.
Thus, if excess current or voltage is applied to the IC, the IC may be damaged. Please design the IC so that excess current or voltage will not be applied to the IC.
Utmost care is necessary in the design of the output line, V_{CC}, COMMON and GND line since IC may be destroyed due to short−circuit between outputs, air contamination fault, or fault by improper grounding.
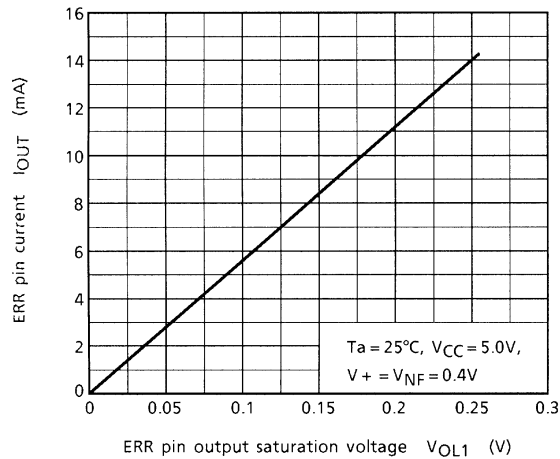
detectable pulse width
(At Ta = 25°C, ERR pin outputs a low-level pulse width of 1μs.)

ERR detectable pulse width (μs)
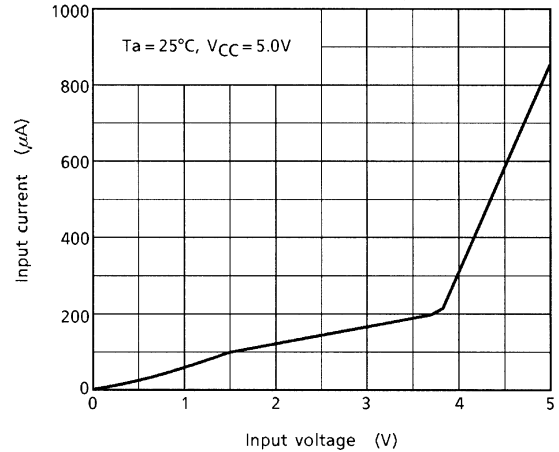
$V_{CC} = 5.0V$
$V_{CC} = 5.5V$
$V_{CC} = 4.5V$

50.00
30.00
20.00
10.00
5.00
3.00

100pF   4700pF   6800pF   10000pF   22000pF   100000pF

Capacitor between LP and GND pins (pF)
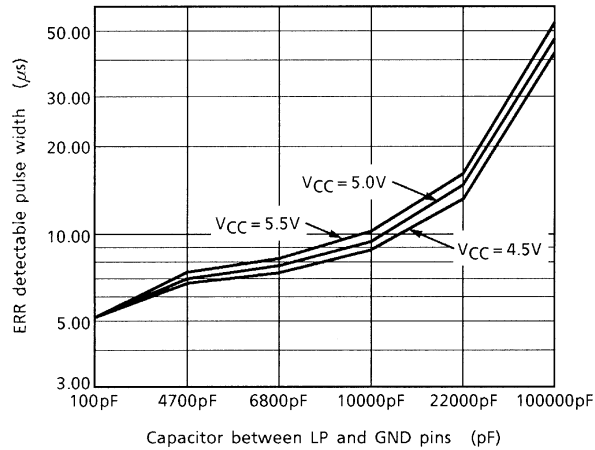
Output pin OUTn
Output saturation voltage vs Output pin current

Output current I_{OUT} (mA)

160 140 120 100 80 60 40 20 0

Ta = 25°C, $V_{CC} = 5.0V$, $V_{IN} = 2.5V$,
CO-IN = OPEN, NF1~4 = GND = 0V

0   0.02   0.04   0.06   0.08   0.1   0.12   0.14

Output saturation voltage V_{OL1} (V)

ERR pin
Output saturation voltage vs Output pin current

ERR pin current I_{OUT} (mA)

16 14 12 10 8 6 4 2 0

Ta = 25°C, $V_{CC} = 5.0V$,
$V+ = V_{NF} = 0.4V$

0   0.05   0.1   0.15   0.2   0.25   0.3

ERR pin output saturation voltage V_{OL1} (V)
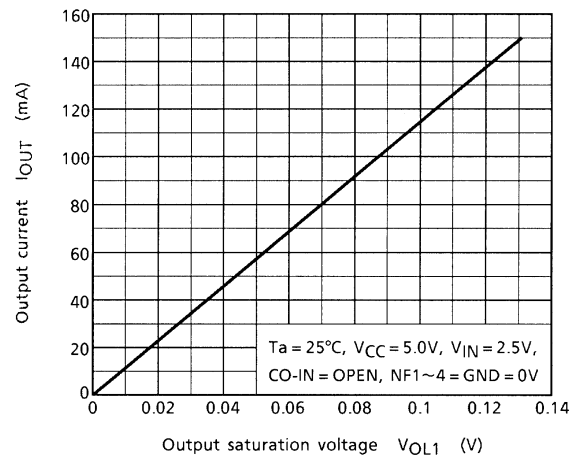
Input pin INn
Input pin voltage vs Input pin current

Input current (μA)

1000 800 600 400 200 0

Ta = 25°C, $V_{CC} = 5.0V$

0   1   2   3   4   5

Input voltage (V)

Clamp diode COM
Forward voltage Vf vs Forward current If characteristics

Clamp diode forward current (mA)

200 150 100 50 0

Ta = 25°C, $V_{CC} = 5.0V$

0   0.2   0.4   0.6   0.8   1   1.2   1.4
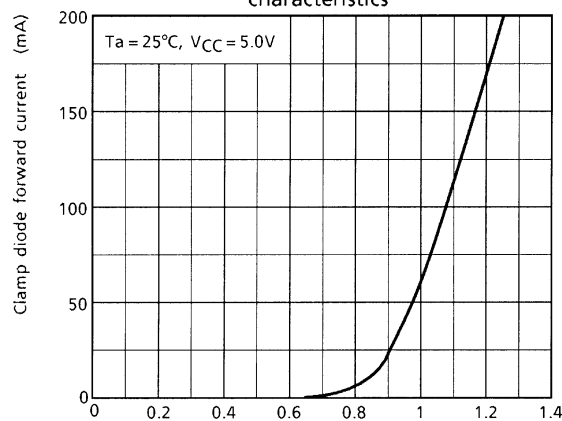
Power supply voltage V_{CC}
Applied power supply voltage V_{CC} vs Power supply current during operation I_{CCopr}

Power supply current during operation I_{CCopr} (mA)

20 15 10 5 0

$V_{IN} = 5.0V$
$I_{OUT} = 150mA/ch$,
CO-IN = OPEN

Ta = −10°C
Ta = 25°C

0   1   2   3   4   5   6   7

Power supply voltage V_{CC} (V)
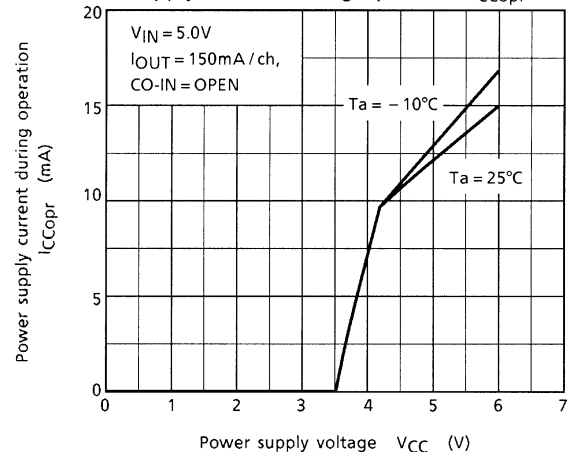
PACKAGE DIMENSIONS

SSOP18−P−225−0.65   Unit: mm

18   10

4.4±0.1

6.4±0.2

5.72

(225mil)

1   9

0.65TYP

0.24±0.08

0.13 (M)

0.65

6.8MAX

6.5±0.1

1.2±0.1

1.55MAX

0.1±0.05

0.1

0.17±0.07

0.45±0.2
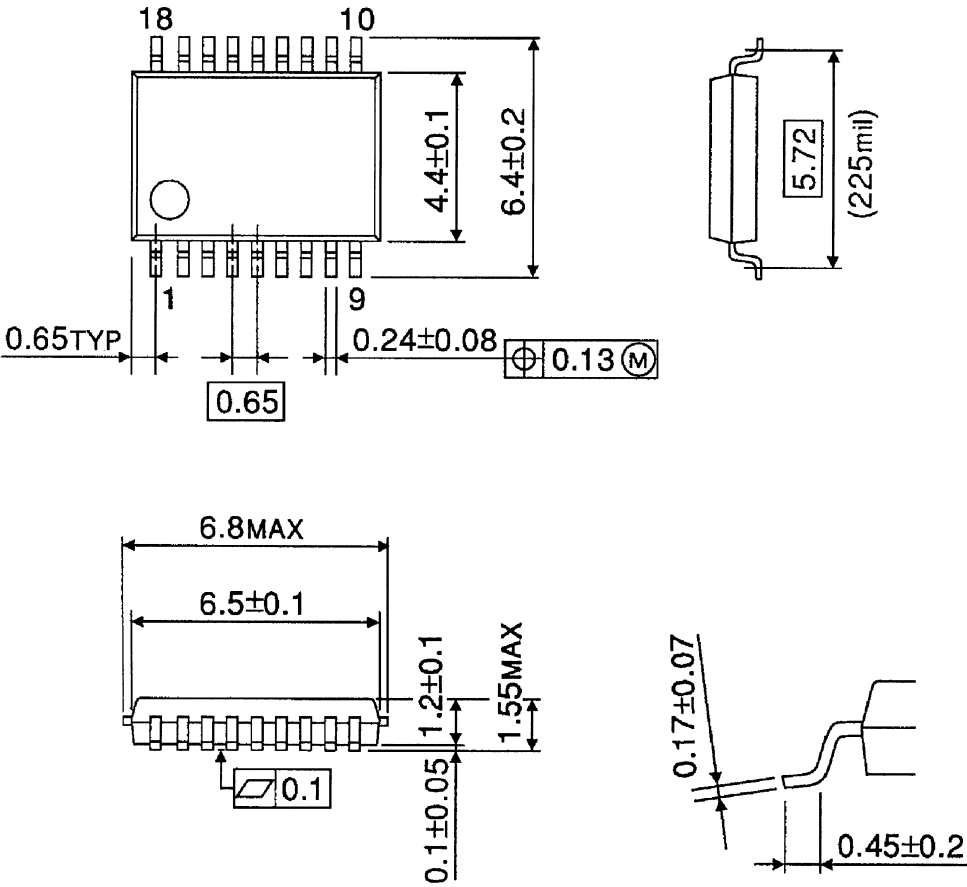
Weight: 0.08 g (Typ.)

RESTRICTIONS ON PRODUCT USE

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