ICs for Communications

Acoustic Echo Canceller
ACE

PSB 2170 Version 2.1

Preliminary Data Sheet 10.99

DS 2

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1 Overview

The PSB 2170, Version 2.1 provides a full-duplex speakerphone for analog and digital featurephones. To assure excellent speech quality even in noisy environments like cars, the PSB 2170 provides acoustic echo cancellation, comfort noise insertion, and noise reduction adaptive to the environment. Depending on the requirements on the runtime delay, this can be performed in fullband or subband mode.

Furthermore the , Version 2.1 features a caller ID decoder (Bellcore compliant), DTMF recognition and generation and call progress tone detection.

The frequency response of cheap microphones or loudspeakers can be corrected by two programmable equalizers.

The provides an IOM®-2 compatible interface with up to three channels for speech data.

Alternatively to the IOM®-2 compatible interface, the supports a simple serial data interface (SSDI) with separate strobe signals for each direction (linear PCM data, one channel).

A separate interface is used for a glueless connection to the PSB 4851 (dual codec).

The chip is programmed by a simple four wire serial control interface and can inform the microcontroller of new events by an interrupt signal.

The supports interface pins to +5 V input levels.

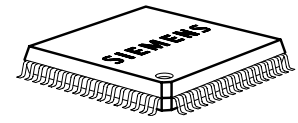
Acoustic Echo Canceller
ACE

PSB 2170

Version 2.1

CMOS

1.1 Features



P-MQFP-80

- Two modes of acoustic echo cancellation:
  20 dB ERLE[1] @16-80 ms, 0.25-2 ms delay
  30 dB ERLE[1] @60-159 ms, 35 ms delay
- Fast adaptation without learning tone
- Two noise reduction blocks
- Comfort noise generator
- Line echo cancellation without learning tone
- DTMF tone generation
- Flexible ringing generation
- Programmable side gain
- Two transducer correction filters (equalizer)
- DTMF tone detector
- Call progress tone detector
- Universal tone detector
- Caller ID decoder
- General purpose parallel port (16 bits)
- Independent gain for all channels
- Serial control interface for programming
- 3.3V power supply, 5V interface
- IOM®-2 interface (three data channels)
- Interface to PSB 4851
- Interface to Burst Mode Controllers

[1] ERLE: Echo Return Loss Enhancement

Type	Package
PSB 2170	P-MQFP-80

1.2 Pin Configuration

(top view)

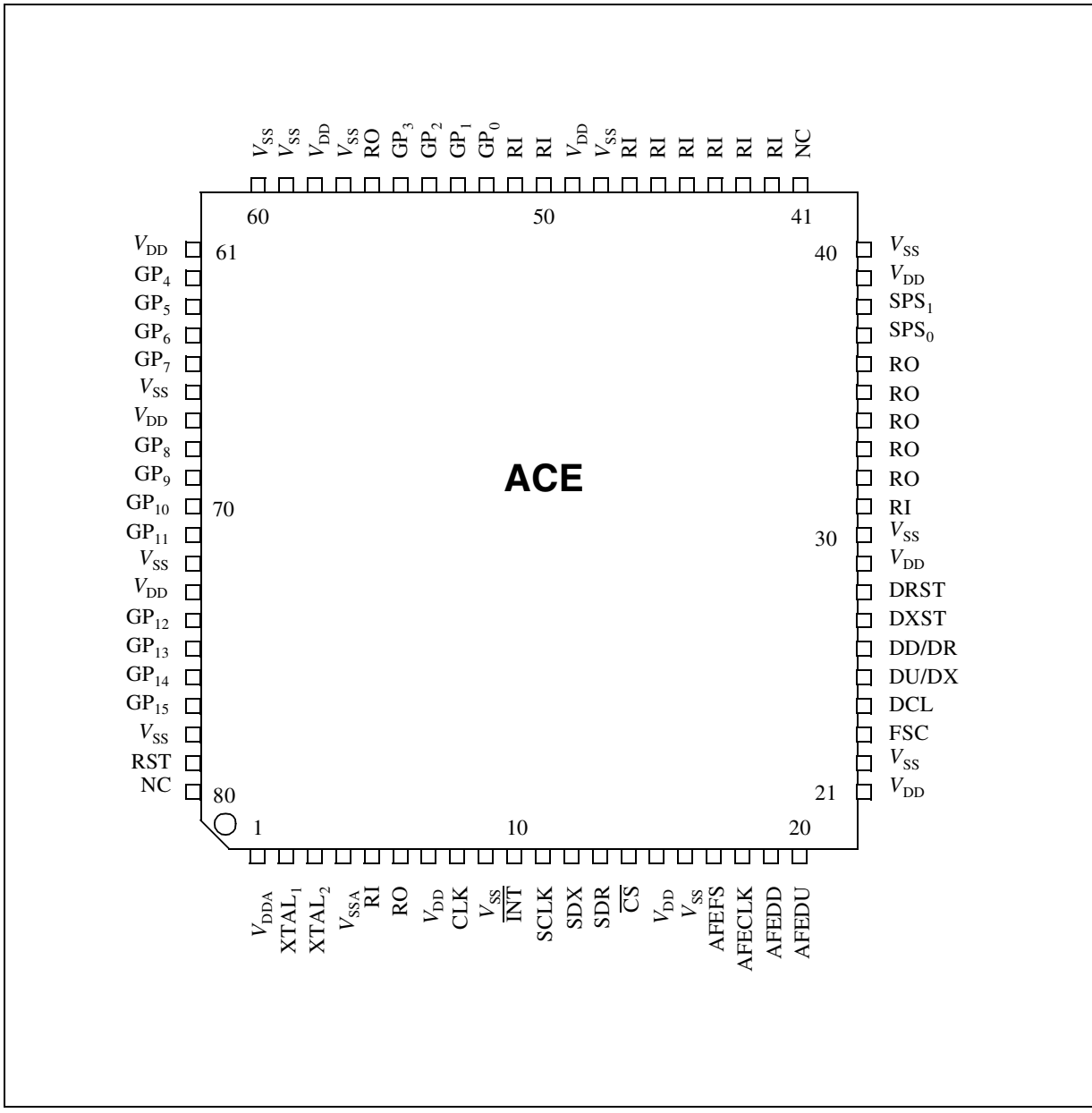


Figure 1 Pin Configuration

1.3 Pin Definitions and Functions

Table 1 Pin Definitions and Functions

Pin No. P-MQFP-80	Symbol	Dir.[1)]	Reset	Function
7, 15, 21, 29, 39, 49, 58, 61, 67, 73	V_{DD}	-	-	**Power supply (3.3V ±5 %)** Power supply for logic.
1	V_{DDA}	-	-	**Power supply (3.3V ±5 %)** Power supply for clock generator.
4	V_{SSA}	-	-	**Power supply (0 V)** Ground for clock generator.
9, 16, 22, 30, 40, 48, 57, 59, 60, 78, 66, 72	V_{SS}	-	-	**Power supply (0 V)** Ground for logic and interface.
17	AFEFS	O	L	**Analog Frontend Frame Sync:** 8 kHz frame synchronization signal for communication with the analog frontend.
18	AFECLK	O	L	**Analog Frontend Clock:** Clock signal for the analog frontend (6.912 MHz).
19	AFEDD	O	L	**Analog Frontend Data Downstream:** Data output to the analog frontend.
20	AFEDU	I	-	**Analog Frontend Data Upstream:** Data input from the analog frontend.
79	RST	I	-	**Reset:** Active high reset signal.
23	FSC	I	-	**Data Frame Synchronization:** 8 kHz frame synchronization signal (IOM®-2 and SSDI mode).
24	DCL	I	-	**Data Clock:** Data Clock of the serial data of the IOM®-2 compatible and the SSDI interface.

Table 1 Pin Definitions and Functions

26	DD/DR	**I**/OD I	-	**IOM®-2 Compatible Mode:** Receive data from IOM®-2 controlling device. **SSDI Mode:** Receive data of the strobed serial data interface.
25	DU/DX	**I**/OD O/ OD	-	**IOM®-2 Compatible Mode:** Transmit data to IOM®-2 controlling device. **SSDI Mode:** Transmit data of the strobed serial data interface.
27	DXST	O	L	**DX Strobe:** Strobe for DX in SSDI interface mode.
28	DRST	I	-	**DR Strobe:** Strobe for DR in SSDI interface mode.
14	$\overline{CS}$	I	-	**Chip Select:** Select signal of the serial control interface (SCI).
11	SCLK	I	-	**Serial Clock:** Clock signal of the serial control interface (SCI).
13	SDR	I	-	**Serial Data Receive:** Data input of the serial control interface (SCI).
12	SDX	O/ **OD**	H	**Serial Data Transmit:** Data Output of the serial control interface (SCI).
10	$\overline{INT}$	O/ **OD**	H	**Interrupt** New status available.
8	CLK	I	-	**Alternative AFECLK Source** 13,824 MHz
2 3	$XTAL_1$ $XTAL_2$	I O	- Z	**Oscillator:** $XTAL_1$: External clock or input of oscillator loop. $XTAL_2$: output of oscillator loop for crystal.
37 38	SPS_0 SPS_1	O O	L L	**Speakerphone State:** Current speakerphone unit state, general purpose outputs or status register output

Table 1 Pin Definitions and Functions

52 53 54 55 62 63 64 65 68 69 70 71 74 75 76 77	GP_0 GP_1 GP_2 GP_3 GP_4 GP_5 GP_6 GP_7 GP_8 GP_9 GP_{10} GP_{11} GP_{12} GP_{13} GP_{14} GP_{15}	I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O**	L[2)] L[2)] L[2)] L[2)] L[2)] L[2)] L[2)] L[2)] L[2)] L[2)] L[2)] L[2)] L[2)] L[2)] L[2)] L[2)]	**General Purpose Parallel Port 0-15:** General purpose I/O.
6, 32, 33, 34, 35, 36, 56	RO	O	-	**Reserved Output:** Do not connect.
5, 31, 42, 43, 44, 45, 46, 47, 50, 51	RI	I	-	**Reserved Input:** Connect to V_{ss}.
41, 80	NC	-	-	**Not connected**

[1)] I = Input
O = Output
OD = Open Drain

[2)] These lines are driven low with 102 µA (typical) during reset.

1.4 Logic Symbol

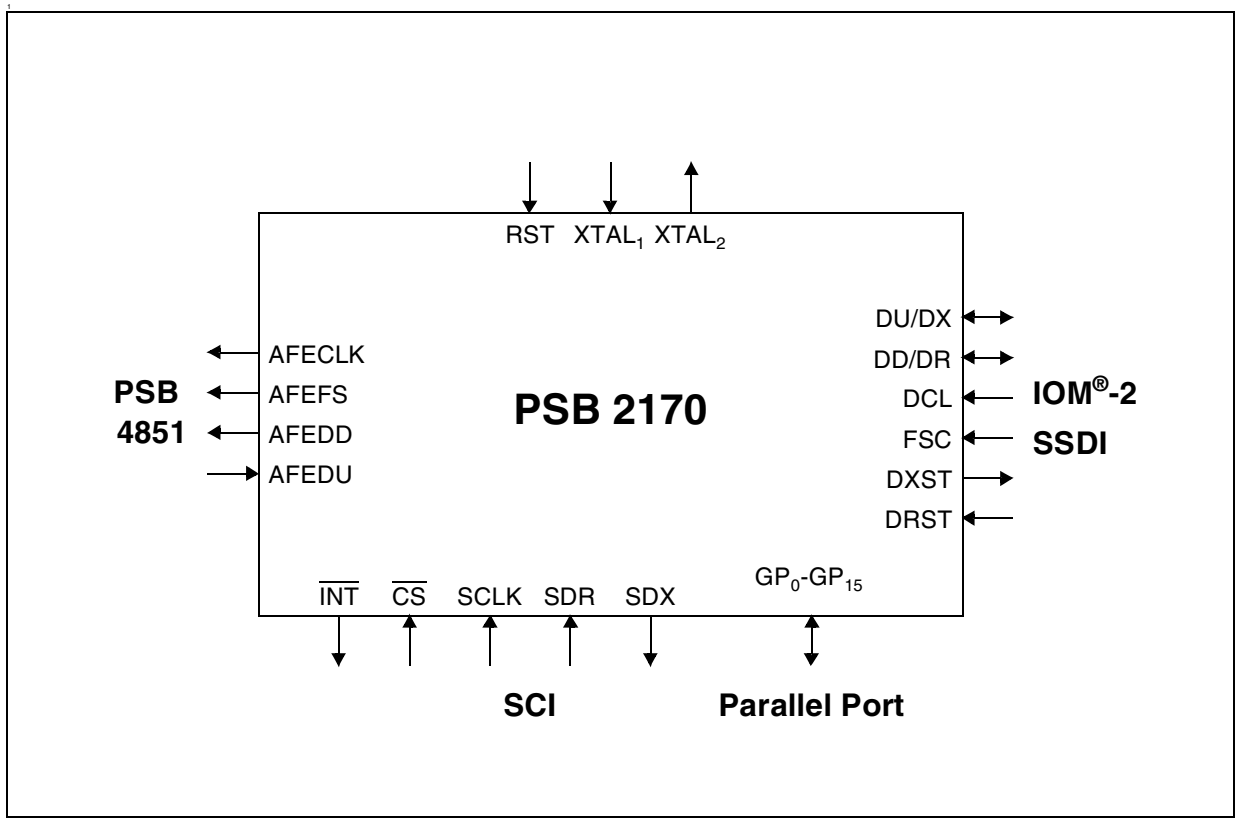


Figure 2 Logic Symbol

1.5 Functional Block Diagram

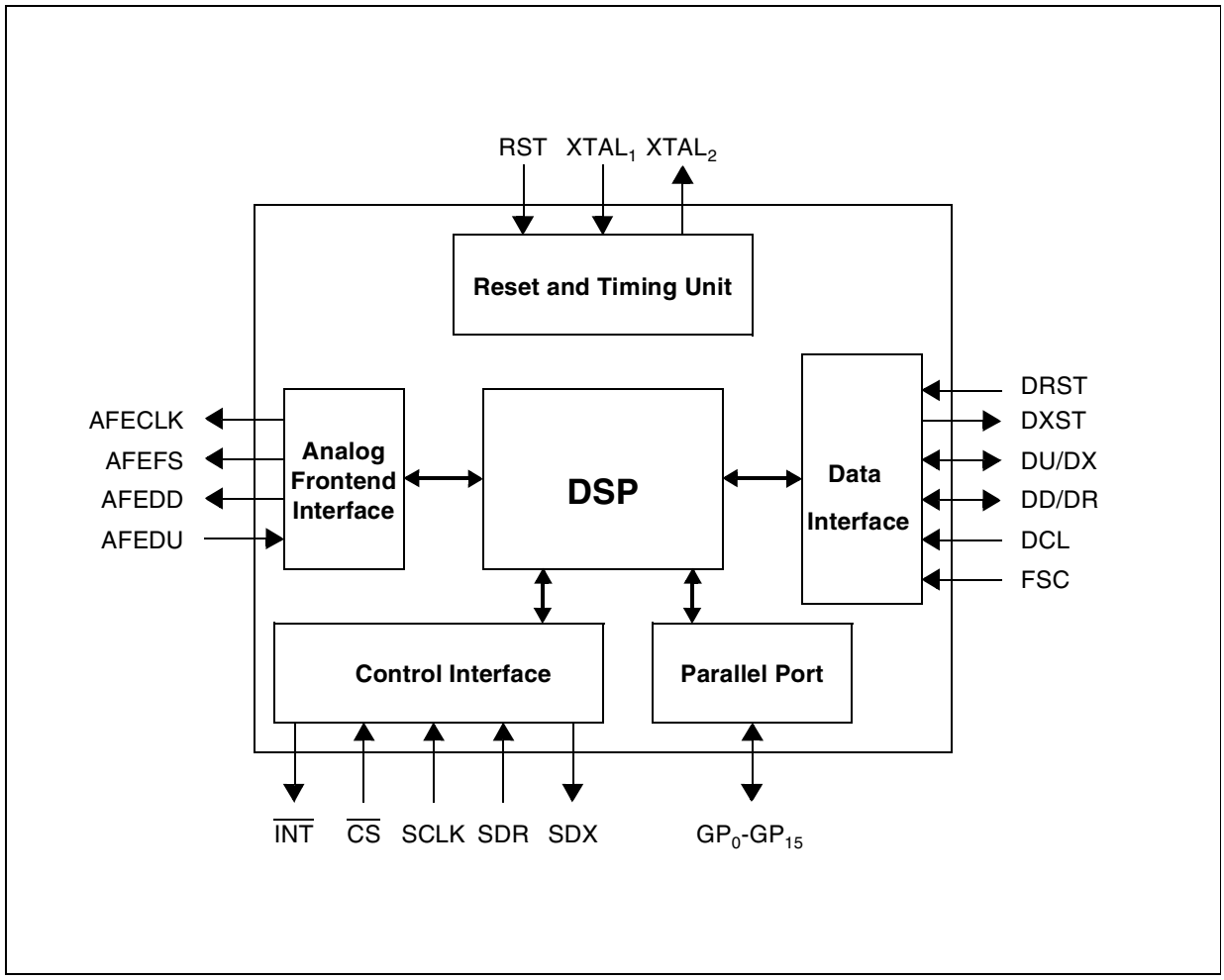


Figure 3 PSB 2170 - Block Diagram

1.6 System Integration

The PSB 2170 provides a full-duplex speakerphone in a variety of applications. Some applications are given in the following sections.

1.6.1 Full-Duplex Speakerphone for ISDN Terminal

Figure 4 shows an example of an ISDN featurephone with the PSB 2170 providing a full-duplex speakerphone.

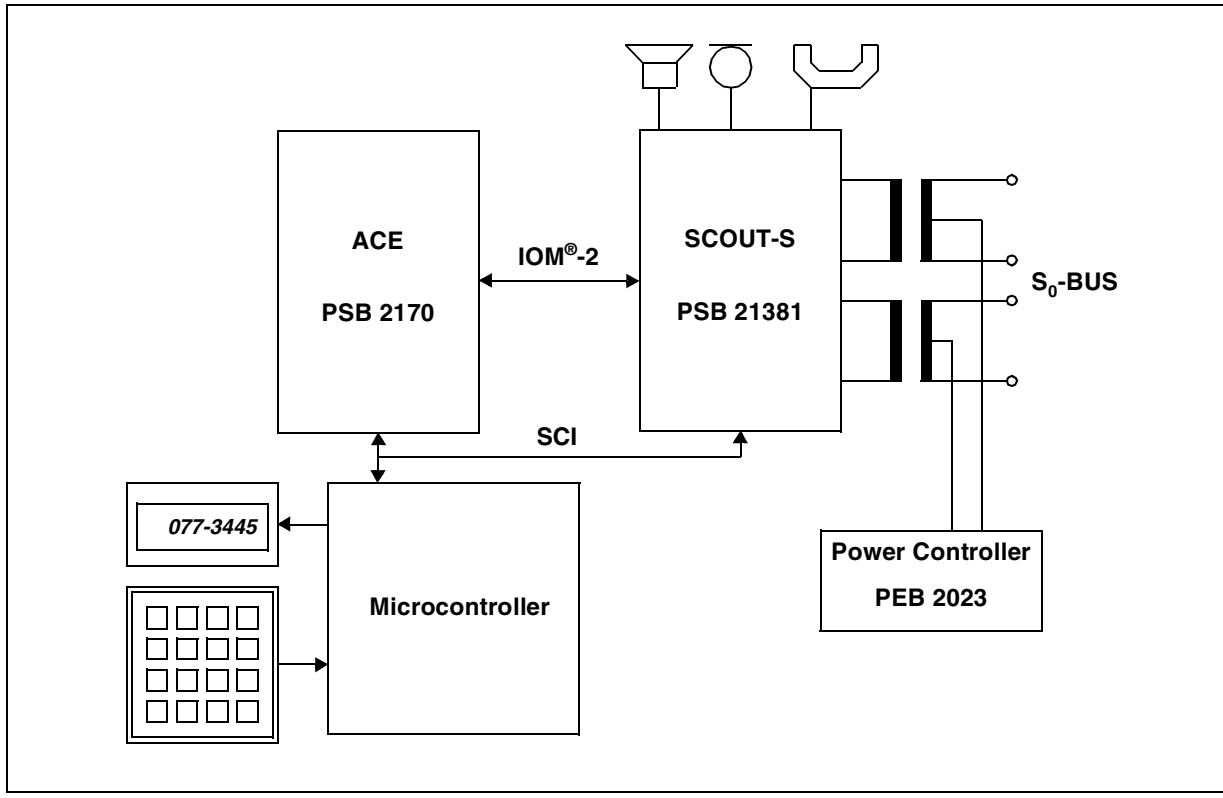


Figure 4 Full-Duplex Featurephone for ISDN Terminal

1.6.2 Full-Duplex Speakerphone for PBX Terminal

Figure 5 shows an example of a PBX phone with the PSB 2170 providing a full-duplex speakerphone.

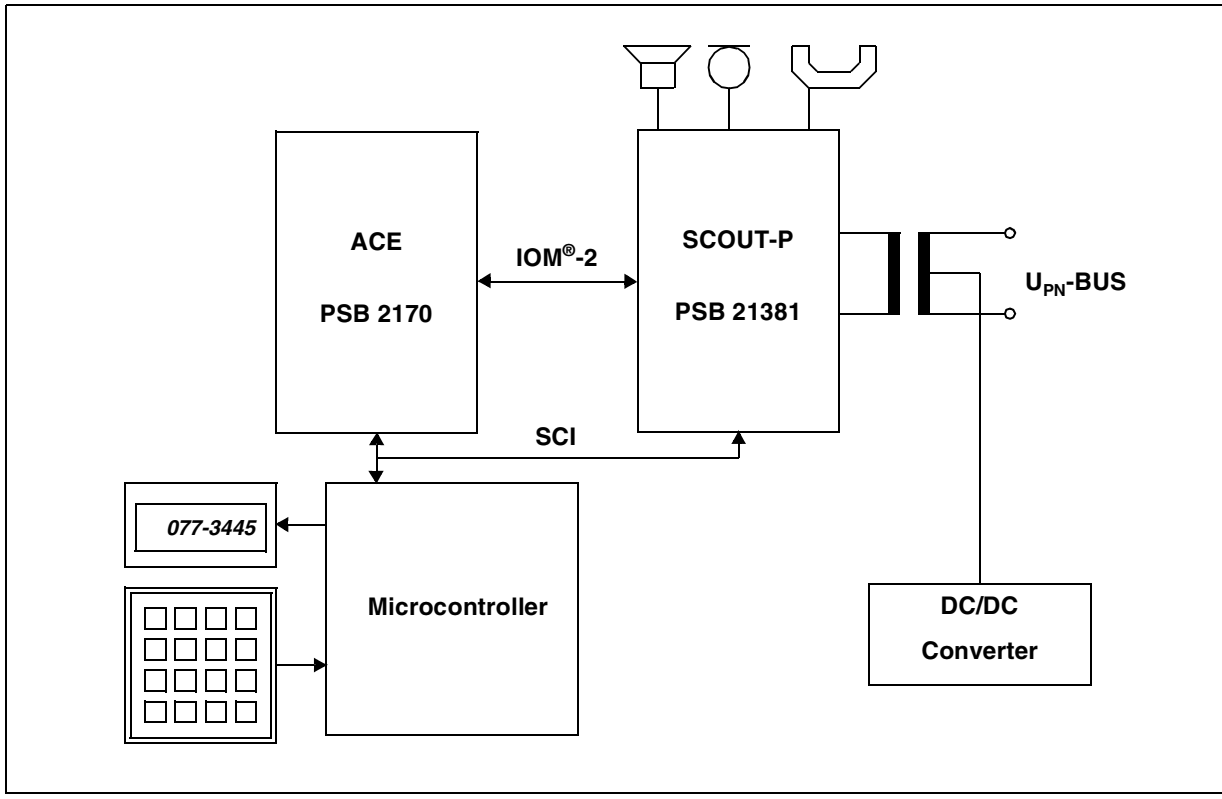


Figure 5 Full-Duplex Featurephone for PBX Terminal

1.6.3 DECT Basestation with Full-Duplex Speakerphone

Figure 6 shows a DECT basestation with acoustic echo cancellation based on the PSB 2170. The full-duplex speakerphone can be switched to the basestation or a mobile handset dynamically. For programming, the serial control interface (SCI) is used while voice data is transferred via the strobed serial data interface (SSDI).

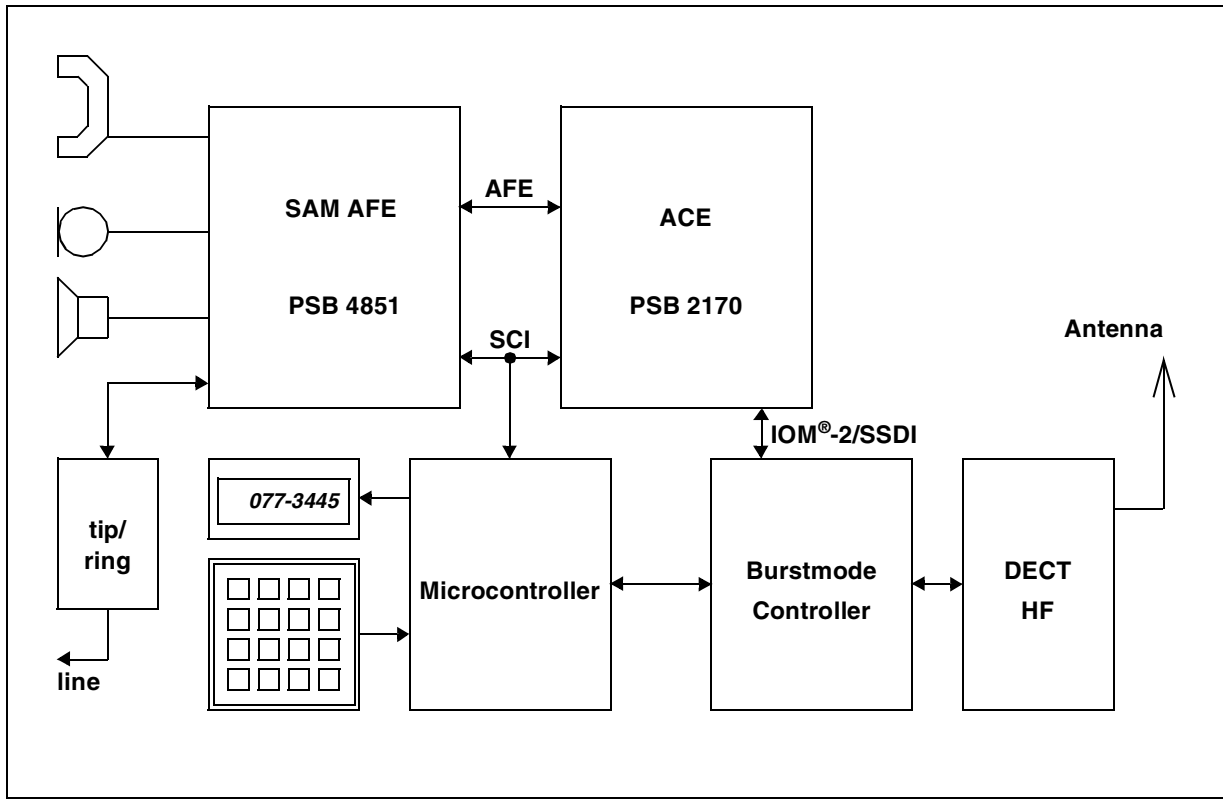


Figure 6 DECT Basestation with Full-Duplex Speakerphone

1.6.4 Videophone with External Line Interface

A videophone using an external line interface with the PSB 2170 providing a full-duplex speakerphone is shown in figure 7.

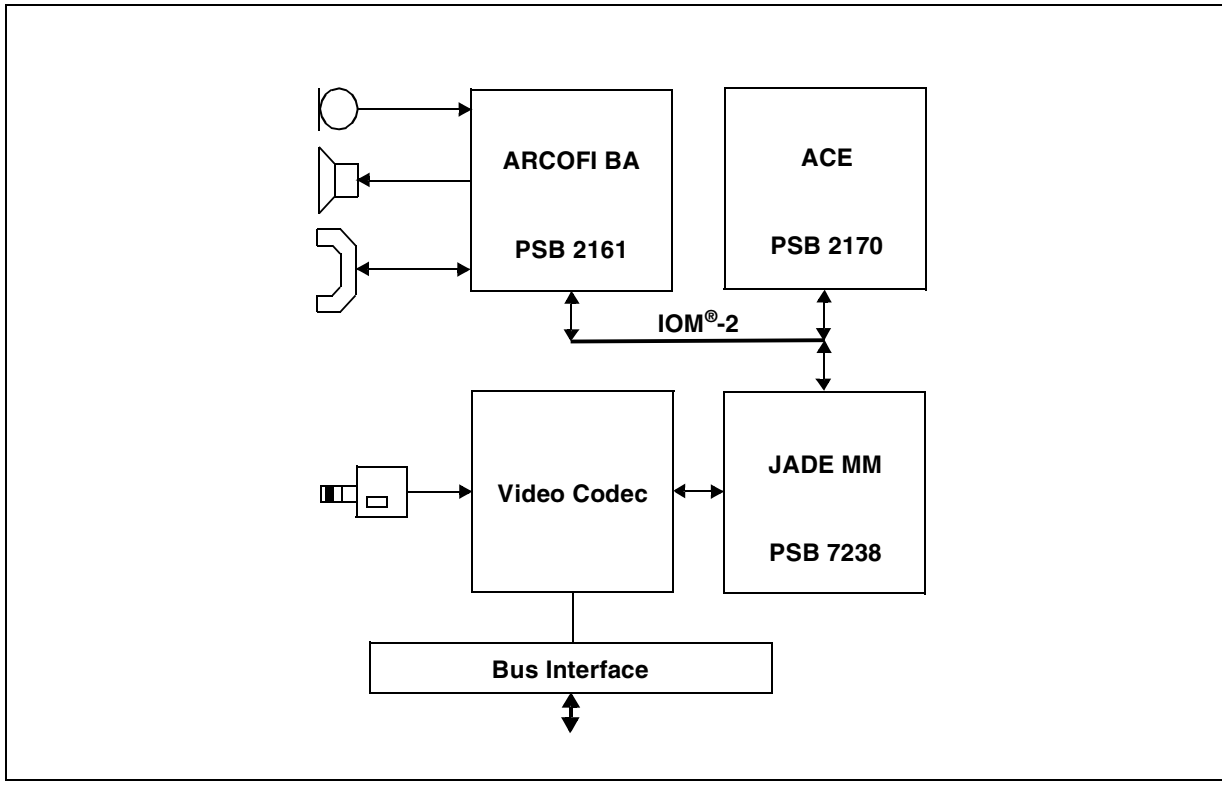


Figure 7 Videophone with External Line Interface (Hardware Video Codec)

In transmit direction the PSB 2161 (ARCOFI BA) provides the uncompressed audio data from the microphone to the acoustic echo canceller (PSB 2170). The acoustic echo canceller provides the echo-free data to the audio compression device JADE MM (PSB 7238). The JADE MM offers all necessary compression algorithms to cover H.320/323/324 applications, i.e. ITU-T G.711, G.722, G.723 and G.728. The compressed data is then multiplexed into the audio/video data stream by the video codec. The video codec in turn sends the combined data via the bus interface to a host unit (e.g. the CPU in a PC) which passes it to the line interface (e.g. ISAC-S TE for ISDN, V.34bis modem for POTS or an Ethernet adapter for LAN). In receive direction the same signal path is used in the other direction.

The off-board line interface offers the advantage of one videophone board applicable to different lines such as ISDN (H.320), LAN (H.323) or POTS (H.324, plain old telephone system) by just exchanging the line interface card and some control software on the PC.

1.6.5 Videophone with Software Video Compression

A videophone using software video compression with the PSB 2170 providing a full-duplex speakerphone is shown in figure 8.

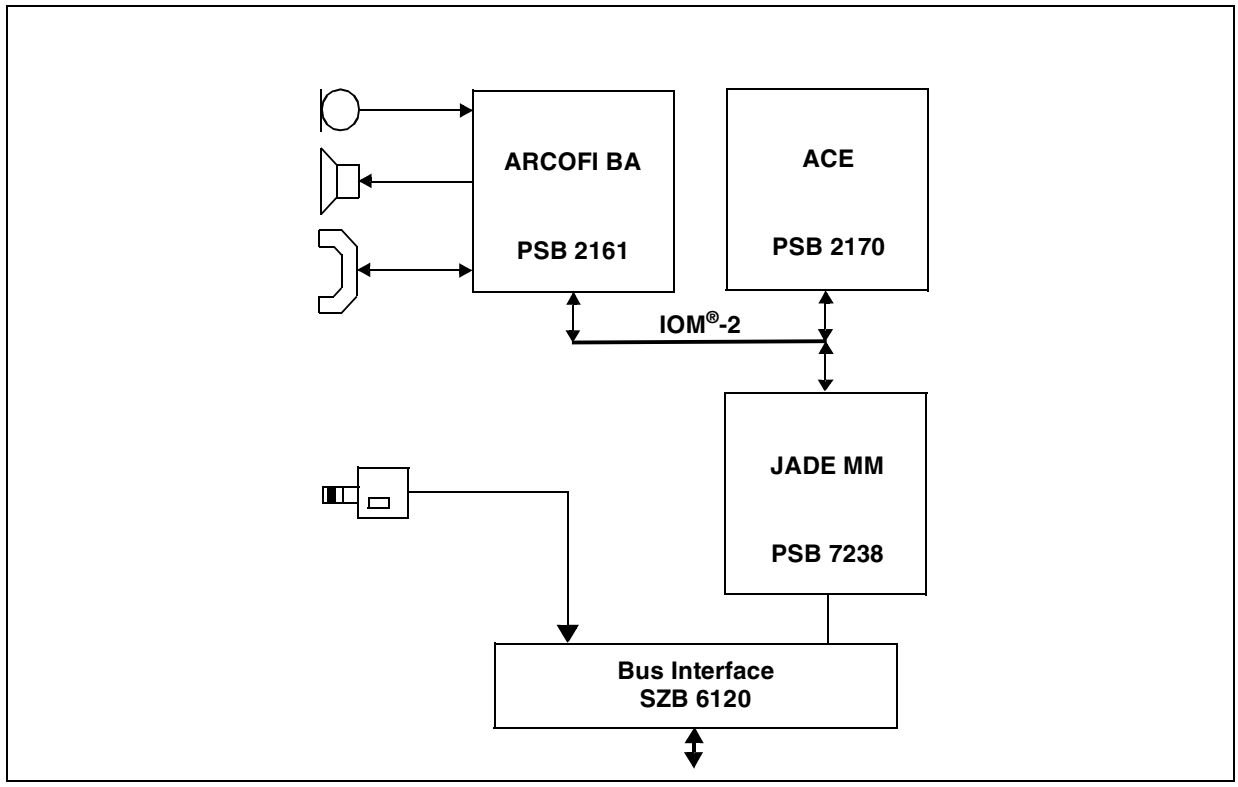


Figure 8 Videophone with External Line Interface (Software Video Codec)

In transmit direction the PSB 2161 (ARCOFI BA) provides the uncompressed audio data from the microphone to the acoustic echo canceller (PSB 2170). The acoustic echo canceller provides the echo-free data to the audio compression device JADE MM (PSB 7238). The JADE MM offers all necessary compression algorithms to cover H.320/323/324 applications, i.e. ITU-T G.711, G.722, G.723 and G.728. The compressed data is then transmitted to the host processor via the bus interface (e.g. using the PCI interface SZB 6120). The host processor also captures the uncompressed video data through the same bus interface and does the video compression and multiplexing by software. The multiplexed data stream is then passed to the corresponding line interface (e.g. ISAC-S TE for ISDN, V.34bis modem for POTS or an Ethernet adapter for LAN). In receive direction the same signal path is used in the other direction.

If only H.324 (POTS) videophones shall be supported, the JADE MM (PSB 7238) may be substituted by the JADE AN (PSB 7230), which offers only the ITU-T G.723.1 compression needed for H.324. A combi-design of JADE MM and JADE AN is also possible, thus offering both solutions by assembly options. See JADE AN data sheet for details.

The off-board line interface offers the advantage of one videophone board applicable to different lines such as ISDN (H.320), LAN (H.323) or POTS (H.324, plain old telephone system) by just exchanging the line interface card and some control software on the PC.

Due to the limited computational power of the host processor (e.g. Intel Pentium), the video quality using software compression usually does not reach the quality of a separate video processor. Nevertheless, if accepted by the customer this offers a very low cost solution for videoconferencing.

1.6.6 Full-Duplex Speakerphone in Car Environment

The has several special provisions for operation in noisy environments like cars. Most important are two noise reduction blocks. One is built in the transmit path of the speakerphone. The other one is a free module that can be inserted into any path.

Figure 9 shows an application where the provides a full-duplex speakerphone for a mobile communications unit in a car.

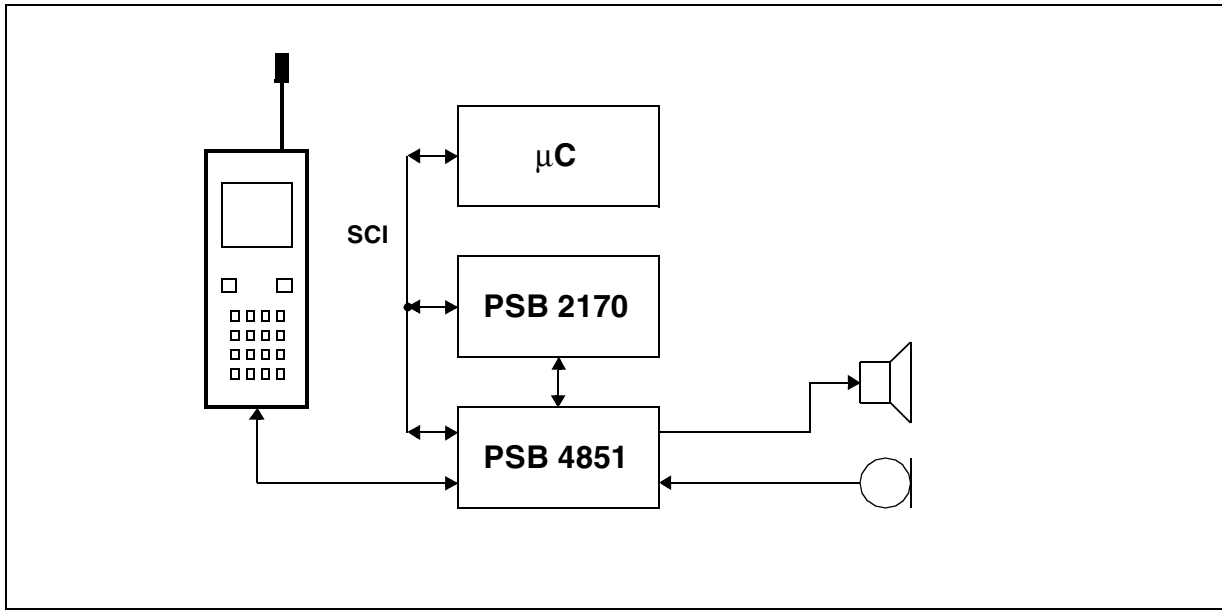


Figure 9 Full-Duplex Speakerphone in Car Environment

The receives (transmits) analog data from (to) the mobile communications unit via the first codec of the PSB 4851. The microphone and the loudspeaker of the mobile communications unit are muted. Instead of them the loudspeaker and microphone mounted in the car are used. They are connected directly to the second channel of the PSB 4851.

1.7 Backward Compatibility

The PSB 2170 Version 2.1 is backwards compatible with the PSB 2170 Version 1.1 with respect to:

- Pin Configuration
- Supply Voltage
- Signal Levels
- Start-up Sequence after Reset
- Register Definition of all modules with exception of the speakerphone

The speakerphone has significantly changed and improved. Some registers have become obsolete, others have been added. Therefore, not all registers of the speakerphone are compatible to the PSB 2170 Version 1.1.

All of the other additional features of the PSB 2170 Version 2.1 are enabled by previously unused bits of the Hardware Configuration Registers or the Read/Write Registers or by additional registers.

Furthermore, the status bits are updated faster which should have no impact on backwards compatibility.

2 Functional Units

The PSB 2170 contains several functional units that can be combined with almost no restrictions to perform a given task. Figure 10 shows the functional units available within the ACE.

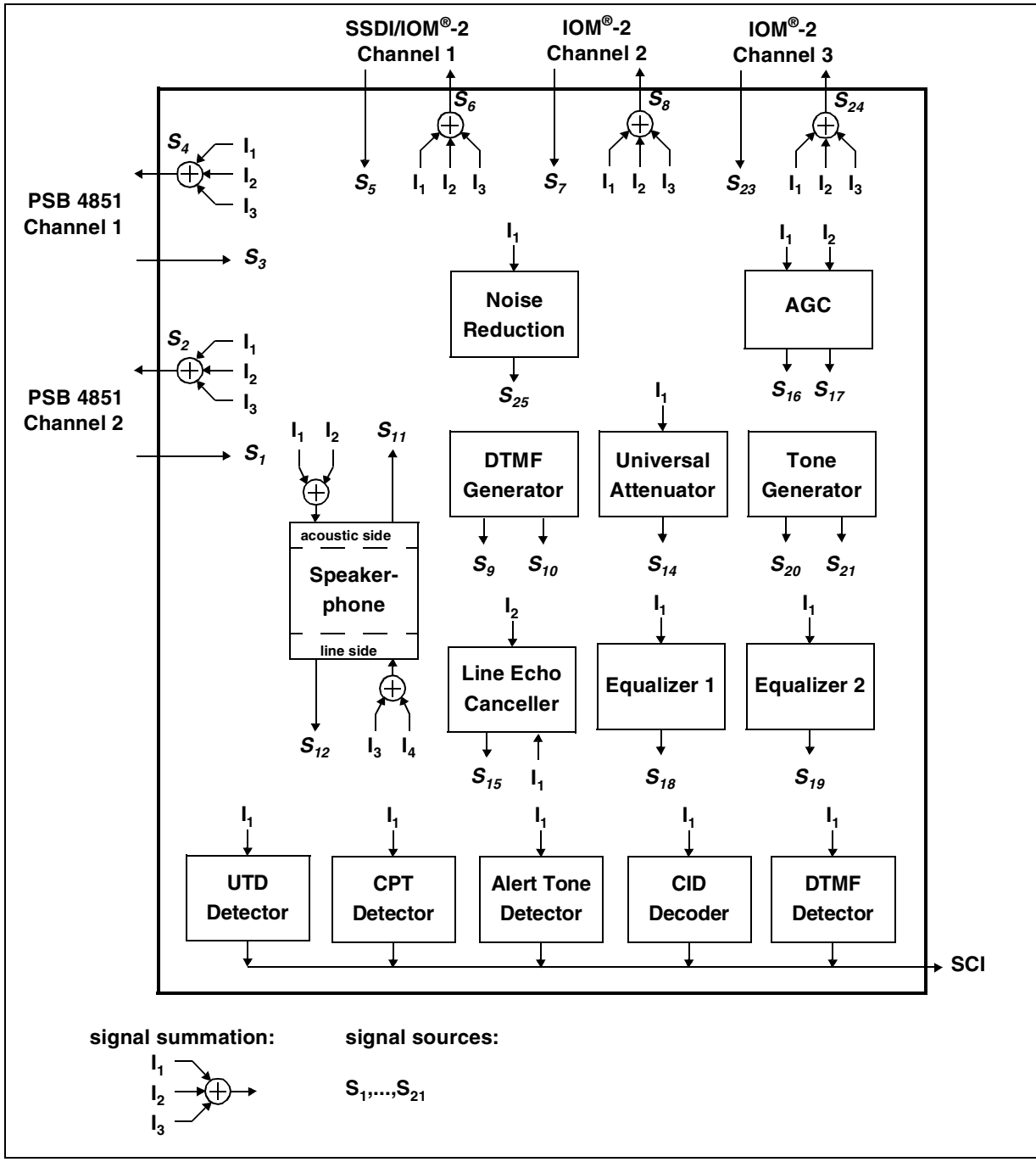


Figure 10 Functional Units - Overview

Each unit has one or more signal inputs (denoted by I). Most units have at least one signal output (denoted by S). Any input I can be connected to any signal output S. In addition to the signals shown in figure 10 there is also the signal S_0 (silence), which is useful at signal summation points. Table 2 lists the available signals within the according to their reference points.

Table 2 Signal Summary

Signal	Description
S_0	Silence
S_1	Analog line input (Channel 1 of PSB 4851 interface)
S_2	Analog line output (Channel 1 of PSB 4851 interface)
S_3	Microphone input (Channel 2 of PSB 4851 interface)
S_4	Loudspeaker/Handset output (Channel 2 of PSB 4851 interface)
S_5	Serial interface input, Channel 1
S_6	Serial interface output, Channel 1
S_7	Serial interface input, Channel 2
S_8	Serial interface output, Channel 2
S_9	DTMF generator output
S_{10}	DTMF generator auxiliary output
S_{11}	Speakerphone output (acoustic side)
S_{12}	Speakerphone output (line side)
S_{13}	reserved
S_{14}	Universal attenuator output
S_{15}	Line echo canceller output
S_{16}	Automatic gain control output (after gain stage)
S_{17}	Automatic gain control output (before gain stage)
S_{18}	Equalizer 1 output
S_{19}	Equalizer 2 output
S_{20}	Tone generator output 1
S_{21}	Tone generator output 2
S_{22}	reserved
S_{23}	Serial interface input, channel 3
S_{24}	Serial interface output, channel 3
S_{25}	NR output

The following sections describe the functional units in detail.

Figure 11 gives an example of how the units may be combined when a hands-free phone conversation is in progress. Units that are not needed are not shown. Unused inputs are connected to S_0 which provides silence (denoted as 0). The equalizers are used to improve the quality of the microphone and the loudspeaker. The alert tone detector recognizes an alert tone of an off-hook caller id request while the CID decoder then decodes the actually transmitted data.

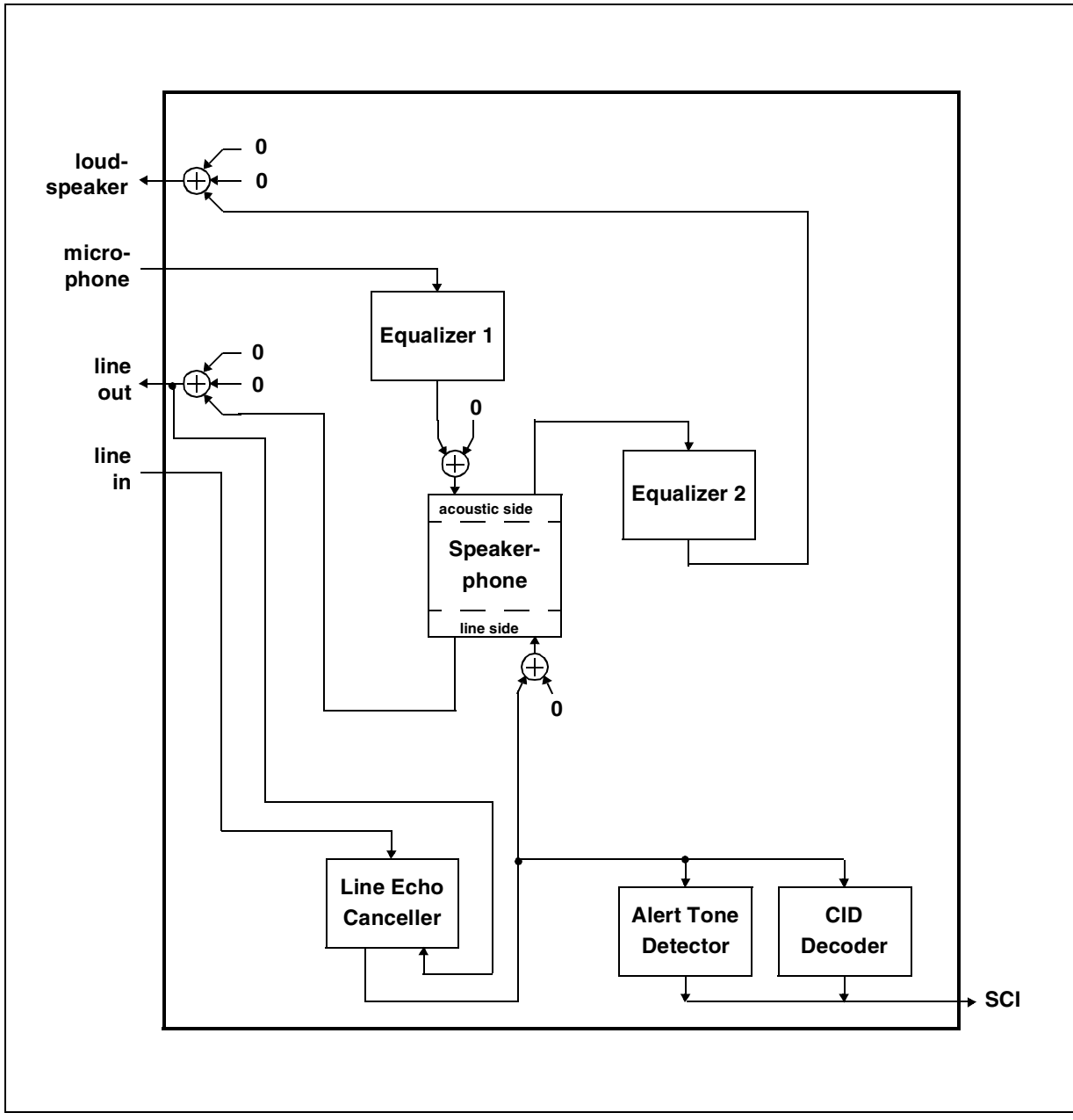


Figure 11 Functional Units - Speakerphone

2.1 Full-Duplex Speakerphone

The speakerphone unit (figure 12) is attached to four signals (microphone, loudspeaker, line out and line in). The two input signals (microphone, line in) are preceded by a signal summation point.

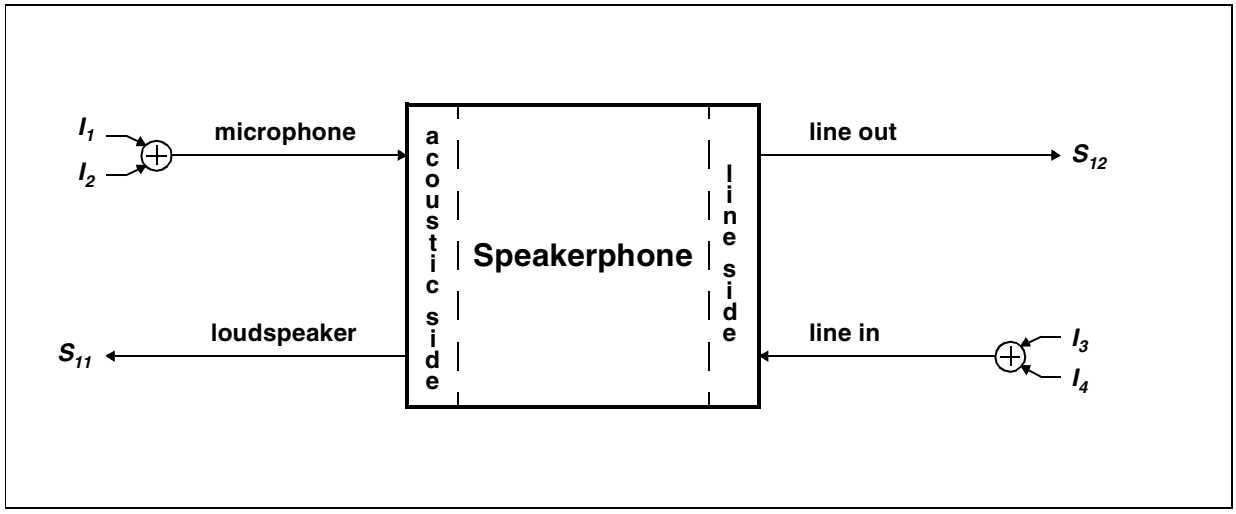


Figure 12 Speakerphone - Signal Connections

Internally, this unit can be divided into an echo cancellation unit and an echo suppression unit (figure 13). The echo cancellation unit provides the attenuation G_c while the echo suppression unit provides the attenuation G_s. The total attenuation ATT of the speakerphone is therefore $ATT=G_C+G_s$.

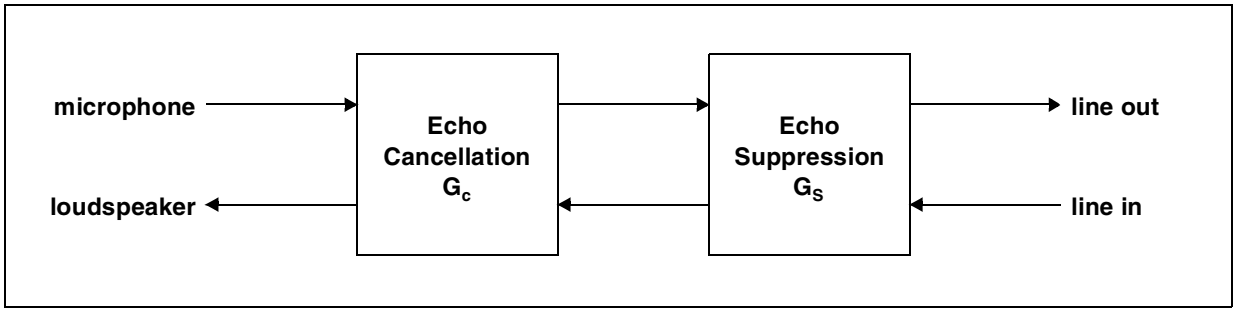


Figure 13 Speakerphone - Block Diagram

The echo cancellation unit estimates that part of the signal at the microphone that originates from the loudspeaker. This part is then subtracted from the signal at the microphone. This technique allows a full-duplex speakerphone. Furthermore, the echo cancellation unit has a built-in noise reduction unit for better sound quality at the line side.

The echo suppression unit attenuates the receive or transmit path dependent on what path is active. Without the echo cancellation unit and by using a high attenuation of the echo suppression unit, the echo suppression unit provides a half-duplex speakerphone.

If the echo cancellation unit is active but cannot provide all of the required attenuation itself, the echo suppression unit can be used to provide additional attenuation.

2.1.1 Echo Cancellation Unit

The echo cancellation unit has two operating modes: fullband and subband mode. Table 3 shows the basic differences of the two modes.

Table 3 Echo Cancellation Modes

	fullband mode	subband mode
max. G_c	20 dB	30 dB
echo length	16-80 ms	50-159 ms
delay	0.25-2 ms	35 ms

The selection between the modes is performed with the parameter QU as summarized in table 4. The different modi are described in the sequel.

Table 4 AEC Mode (QU) Encoding

QU_2	QU_1	QU_0	Acoustic Echo Cancellation Modes
0	0	0	Echo cancellation disabled (half duplex)
0	0	1	Subband, RNR
0	1	0	Fullband mode one (similar to PSB 2170 Version 1.1)
0	1	1	Fullband mode two
1	0	0	Subband, reduced filter length (car kit application)
1	0	1	Subband, analog line mode
1	1	0	Subband, ISDN mode
1	1	1	Subband, enhanced mode

2.1.1.1 Echo Cancellation (Fullband Mode)

A simplified block diagram of the fullband echo cancellation unit is shown in figure 14.

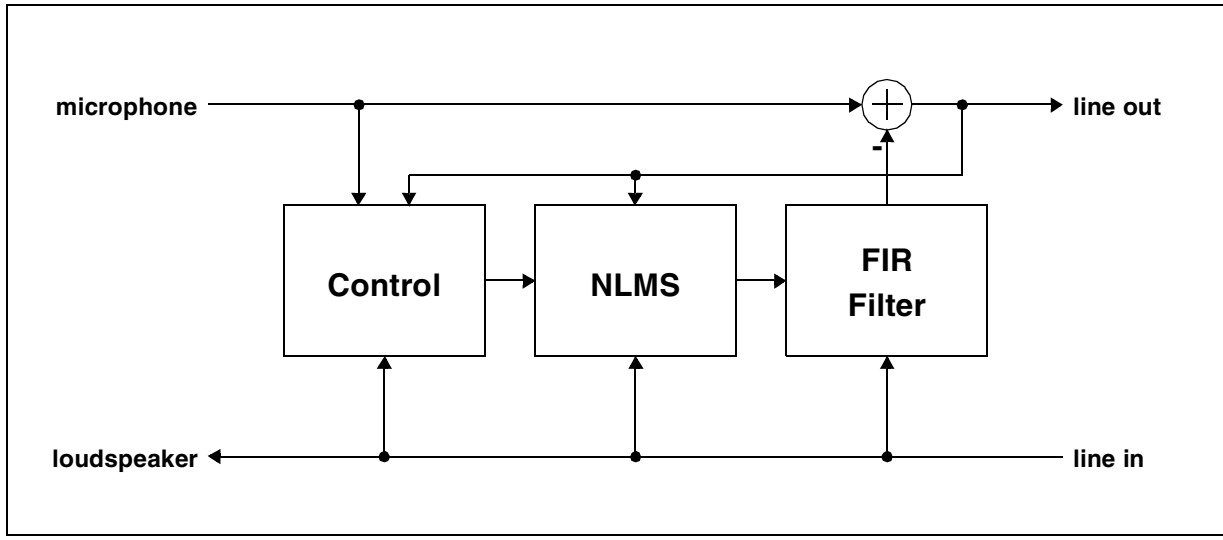


Figure 14 Echo Cancellation Unit (Fullband Mode) - Block Diagram

The echo cancellation unit consists of a finite impulse response filter (FIR) that models the expected acoustic echo, an NLMS based adaptation unit and a control unit. The expected echo is subtracted from the actual input signal from the microphone. If the model is exact and the echo does not exceed the length of the filter, then the echo can be cancelled completely. However, even if this ideal state can be achieved for one given moment, the acoustic echo usually changes over the time. Therefore the NLMS unit continuously adapts the coefficients of the FIR filter. This adaptation process is steered by the control unit. As an example, the adaptation is inhibited as long as double talk is detected by the control unit. Furthermore the control unit informs the echo suppression unit about the achieved echo return loss. The length of the FIR can be programmed by the parameters FBLEN.

With the parameter QU, the echo cancellation unit can be set into two different fullband modes (section 2.1.1). The fullband mode one is similar to the mode provided in the PSB 2170 Version 1.1. In this mode, the noise reduction (chapter 2.1.2) cannot be enabled. The delay added in this mode is 0.25 ms. In the fullband mode two, the delay is shorter than 2 ms. If this delay is not acceptable, the delay can be reduced to less than 1 ms by setting the bit ERD. The performance of the fullband mode may suffer in this reduced mode but please note that enabling the noise reduction will add some additional delay (section 2.1.2).

In order to detect double talk, the remaining speech signal after the echo cancellation (signal after summation point in figure 14) is compared to the signal expected by the echo cancellation unit (after the signal summation point in figure 14). The difference of the energy of these signals is considered. If this energy is greater than allowed by the parameter AECDTM, double talk is detected.

When double talk is detected, the attenuation of the echo cancellation is reduced since the echo is less noticeable anyway and any possible signal distortion from the echo cancellation is reduced. The parameter AECDTR determines the maximal reduction of the attenuation during double talk. The rate how fast the attenuation reduction gets active after double talk detection or inactive after the end of double talk is determined by the parameters AECDTI and AECDTD, respectively.

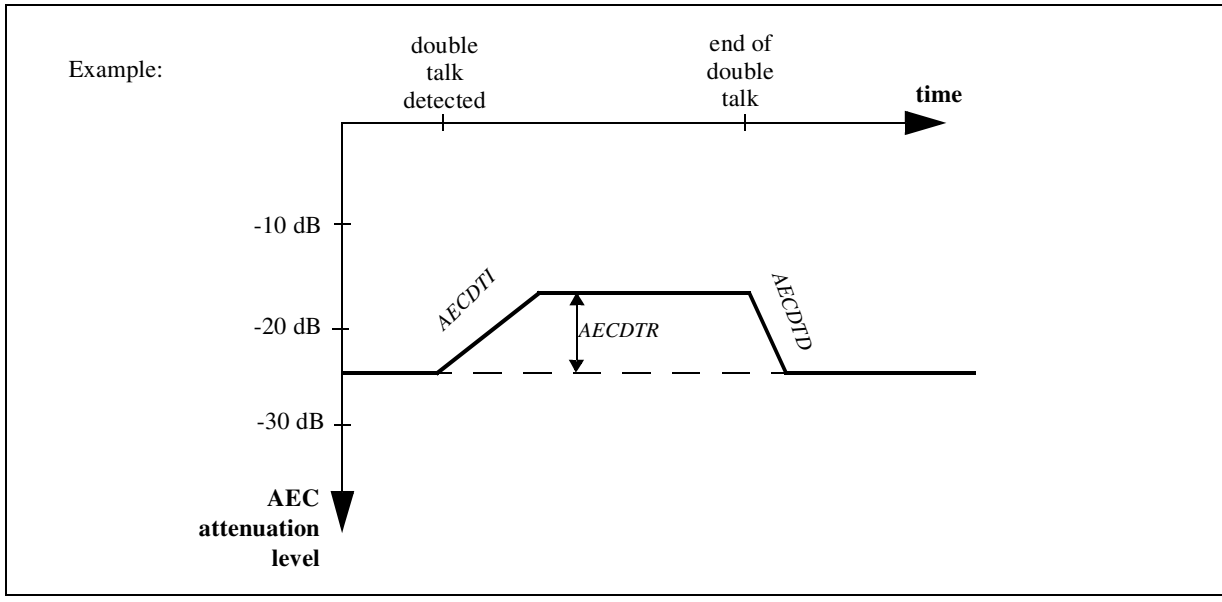


Figure 15 Echo Cancellation Unit - Double Talk Reduction

The echo cancellation unit reports its current attenuation to the echo suppression unit. This has the following reason: If the echo cancellation does not provide enough attenuation, the echo suppression can be used additionally. The attenuation of the echo cancellation unit may be insufficient when the echo cancellation unit is not yet well adapted. In case of a significant change of the characteristics of the acoustics, the attenuation reported by the echo cancellation unit may be too high until it discovers that it has to adapt itself again. If, in addition, double talk reduction is in effect, then the echo suppression unit might not attenuate enough to avoid echoes. Therefore a maximal echo return loss reported by the echo cancellation unit to the echo suppression unit can be programmed by the parameter AECLIM.

In fullband mode two, the number of FIR parameters that are adapted every 125 us can be programmed by the parameter FBADA. The maximum number of taps that get their parameters adapted is 256. If for example the number of taps used by the FIR is 512 and

FBADA is 256, the parameters of the lower 256 taps and of the upper 256 taps get updated alternately. The value of FBADA has therefore the following two effects: First, the higher FBADA the faster the FIR and thus the echo canceller is adapted. Second, with increasing FBADA, the comutational costs increase. If affordable from the computational costs (see chapter 3.7), FBADA should be set to its maximum value.

Table 5 shows the registers associated with the echo cancellation unit in fullband mode.

Table 5 Echo Cancellation Unit Registers

Register	# of Bits	Name	Comment
SCTL	3	QU	Determine AEC modes (see table 4)
SCTL	1	ERD	Enable reduced delay for new fullband mode.
SAELEN	10	FBLEN	Length of FIR filter.
SAEAW	9	FBADA	Length of adaption window. (FB mode two only)
SAEEL	15	AECLIM	Maximum attenuation reported by the AEC unit.
SAEDTR	15	AECDTR	AEC attenuation reduction during double-talk.
SAEDTL	15	AECDTM	Minimum energy to detect double talk.
SAEDTI	15	AECDTI	How fast the attenuation reduction gets incremented.
SAEDTD	15	AECDTD	How fast the attenuation reduction gets decremented.

The length of the FIR filter for the echo compensation can be varied from 63 up to

- 542 taps (~68 ms) if comfort noise (chapter 2.1.4) is enabled
- 639 taps (~80 ms) if fullband mode one is used and comfort noise is disabled
- 645 taps (~80 ms) if fullband mode two is used and comfort noise is disabled
- 768 taps (~96 ms) if fullband mode two is used and the same module as in subband ISDN mode are disabled (chapter 3.7).

The length of the adaption window can be varied from 64 to 256 taps (8 ms to 32 ms).

2.1.1.2 Echo Cancellation (Subband Mode)

A simplified block diagram of the subband echo cancellation unit is shown in figure 16. The signal coming from the microphone and the signal from the line side are analyzed into several subbands. Then for each subband, the block diagram of figure 16 is identical to the block diagram of the fullband mode. After the echo cancellation of each subband, the subbands are synthesized. Finally and additionally to the fullband mode, in the subband mode an optional Wiener filter (called WF in figure 16) is provided.

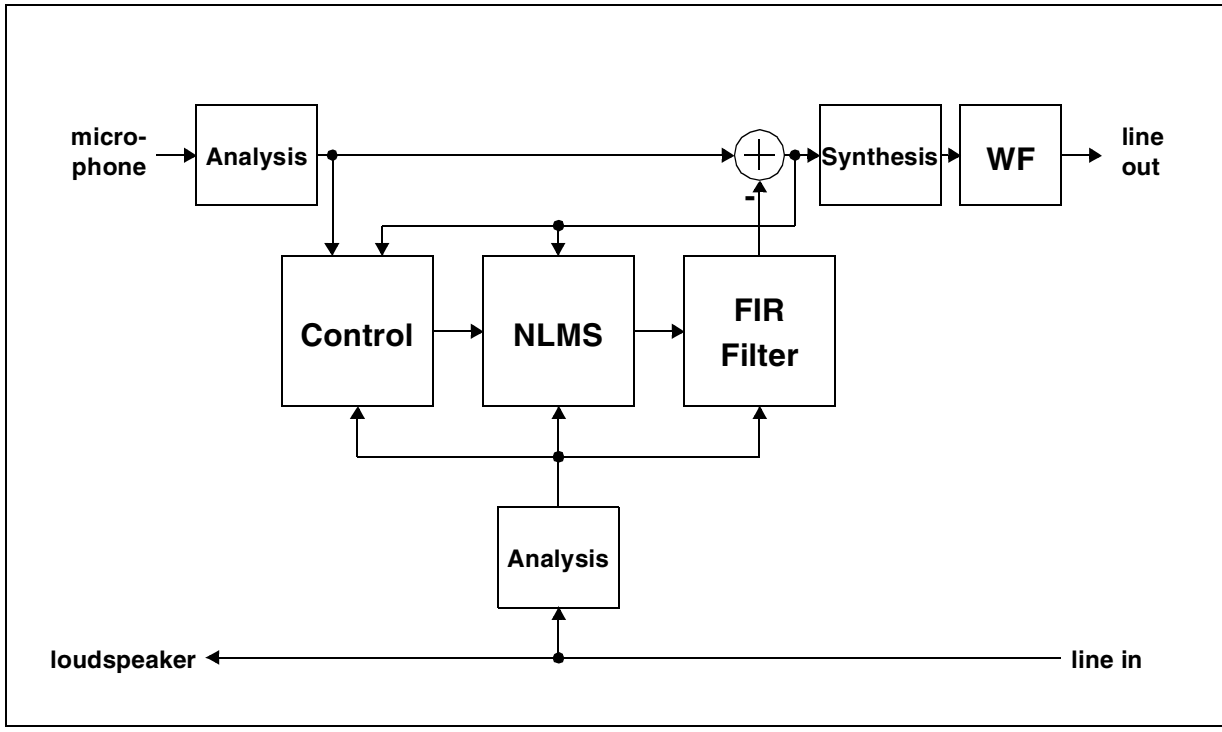


Figure 16 Echo Cancellation Unit (Subband Mode) - Block Diagram

The subband mode can be enabled in five different submodes. These submodes offer a trade-off between the maximum echo length and the functional units that can be run simultaneously (see chapter 3.7). All units that cannot be run simultaneously must be disabled before the subband echo cancellation unit is enabled. After the subband echo cancellation unit is disabled, the parameters for the affected units must be rewritten by the microcontroller.

For the optional Wiener filter, the maximum attenuation can be programmed with the parameter WFATT. If the Wiener filter is enabled, it is only active while there is no speech detected on the near side (microphone).

As shown in figure 13 the total attenuation provided by the speakerphone consists of the attenuation G_C (provided by the echo cancellation unit) and G_S (provided by the echo suppression unit). In subband mode the attenuation G_C is further split into G_A (provided by the adaptive filter) and G_W (provided by the Wiener filter).

If G_A already exceeds WFATT due to good adaptation then the Wiener filter is deactivated and $G_C=G_A$. Otherwise WFATT limits the attenuation G_W of the Wiener filter such that $G_C=G_A+G_W$ never exceeds WFATT.

Table 6 shows the registers associated with the subband echo cancellation unit. The parameters AECATT, AECLIM, AECDTM, AECDTI and AECDTD have the same meaning as in fullband mode. Note that the reported echo loss and parameter AECLIM cover the complete echo cancellation unit including the Wiener filter.

Table 6 Subband Mode Registers

Register	# of Bits	Name	Comment
SCTL	3	QU	Determine AEC modes
SCTL	1	EWF	Wiener filter enable (subband only)
SAEWFL	15	WFATT	Wiener filter attenuation limit
SAEDTR	15	AECATT	AEC attenuation reduction during double-talk
SAEEL	15	AECLIM	Upper limit of the attenuation of the AEC
SAEDTL	15	AECDTM	Minimum energy to detect double talk
SAEDTI	15	AECDTI	How fast the attenuation gets incremented.
SAEDTD	15	AECDTD	How fast the attenuation gets decremented.

As shown in table 4, with the control bits QU different modes of the acoustic echo cancellation unit can be selected. In subband mode, four different modes are provided. With increasing number of QU, the considered echo length increases and so does the computational effort. Before selecting a mode, the incompatibilities described in chapter 3.7 must be considered.

2.1.2 Noise Reduction

The PSB 2170 offers a noise reduction block built in the echo cancellation unit. This noise reduction suppresses noise before the signal is output to the line side. This makes conversation more pleasant for the person at the line side.

In fullband mode, the noise reduction can only be enabled if the fullband mode two is used. The noise reduction is performed after the echo cancellation and can thus be considered as an additional block after the echo cancellation as shown in figure 14. Note that the noise reduction adds about 1 ms delay to the signal. If the bit SCTL:ERD is set, then the delay for echo cancellation and noise reduction is still below 2 ms.

In subband mode, the noise suppression is performed for each subband. Figure 16 shows how the noise reduction block (called NR) matches in the echo cancellation unit. The noise reduction adds no delay to the signal.

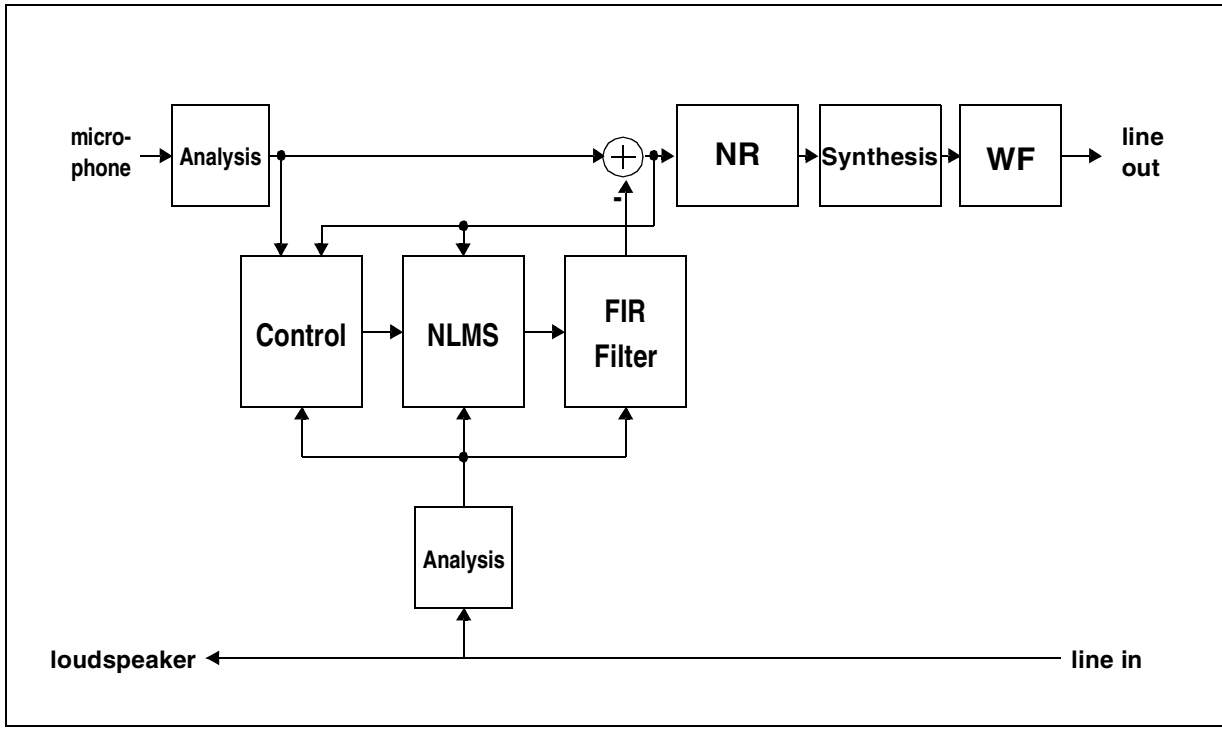


Figure 17 Echo Cancellation with Noise Reduction (Subband Mode)

The parameter NRATT determines the maximum attenuation provided by the noise reduction unit for frequencies with noise. Note that NRATT determines a upper limit. With decreasing level of the background noise, the attenuation of the noise reduction unit decreases as well.

In subband mode, if the Wiener filter is enabled and if no speech is detected at the microphone, the Wiener filter provides attenuation of the signal from the microphone. If noise is present at the microphone and thus the noise reduction unit changes the signal coming from the microphone, then the additional attenuation of the Wiener filter can cause modulations audible at the line side. Therefore, a coupling of the noise reduction unit and the Wiener filter is provided. In case no noise is present at the near end, the Wiener filter attenuates as programmed with the parameter SWATT:WFATT. In case significant noise is present at the near end, the Wiener filter only attenuates so much that the attenuation of the noise reduction plus the attenuation of the Wiener filter never exceeds NRATT. This is controlled with two parameters:

The parameter NRUP determines the noise energy at which the coupling between the noise reduction and the Wiener filter gets active. The parameter NRLOW determines the noise energy at which the coupling gets inactive. This value should be lower than NRUP in order to avoid frequent activation and deactivation, when the noise energy is around the level of NRUP as illustrated in figure 18.

Table 7 Noise Reduction Registers

Register	# of Bits	Name	Comment
SCTL	1	NR	Enable noise reduction
SNRATT	15	NRATT	Maximal attenuation of frequencies with noise.
SNRLNL	15	NRLOW	Lower limit to deactivate coupling.
SNRUNL	15	NRUP	Upper limit to activate coupling.

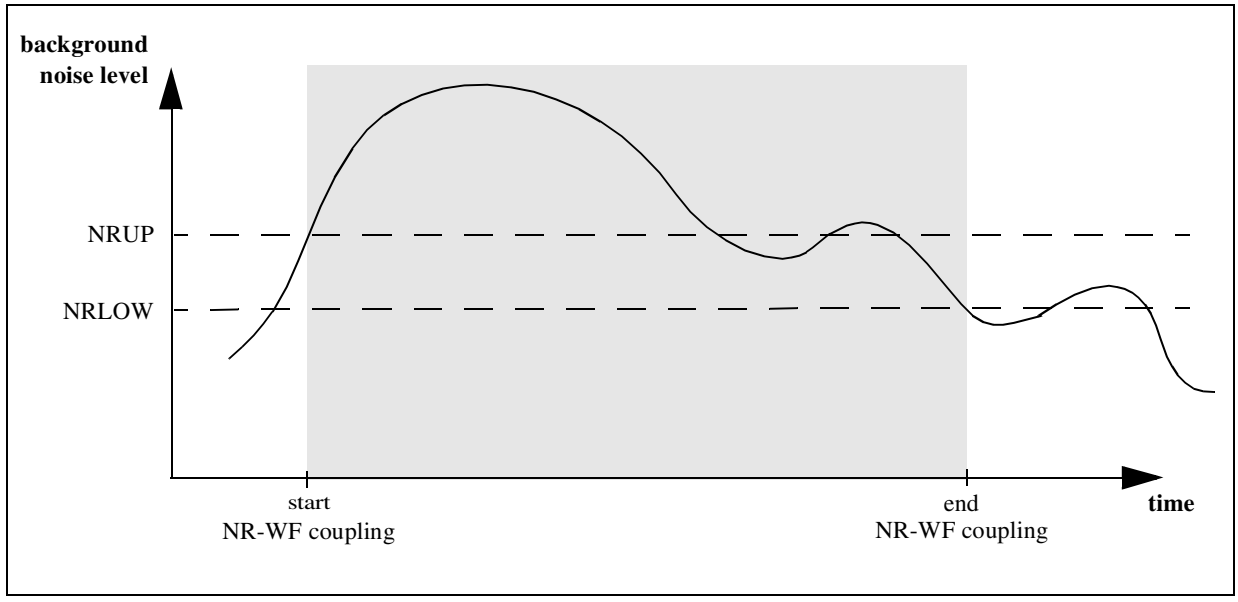


Figure 18 Coupling NR with WF

2.1.3 Echo Suppression

The echo suppression unit can be in one of three states:

- transmit state
- receive state
- idle state

In transmit state the microphone signal drives the line output while the line input is attenuated. In receive state the loudspeaker signal is driven by the line input while the microphone signal is attenuated. In idle state both signal paths are active with evenly distributed attenuation.

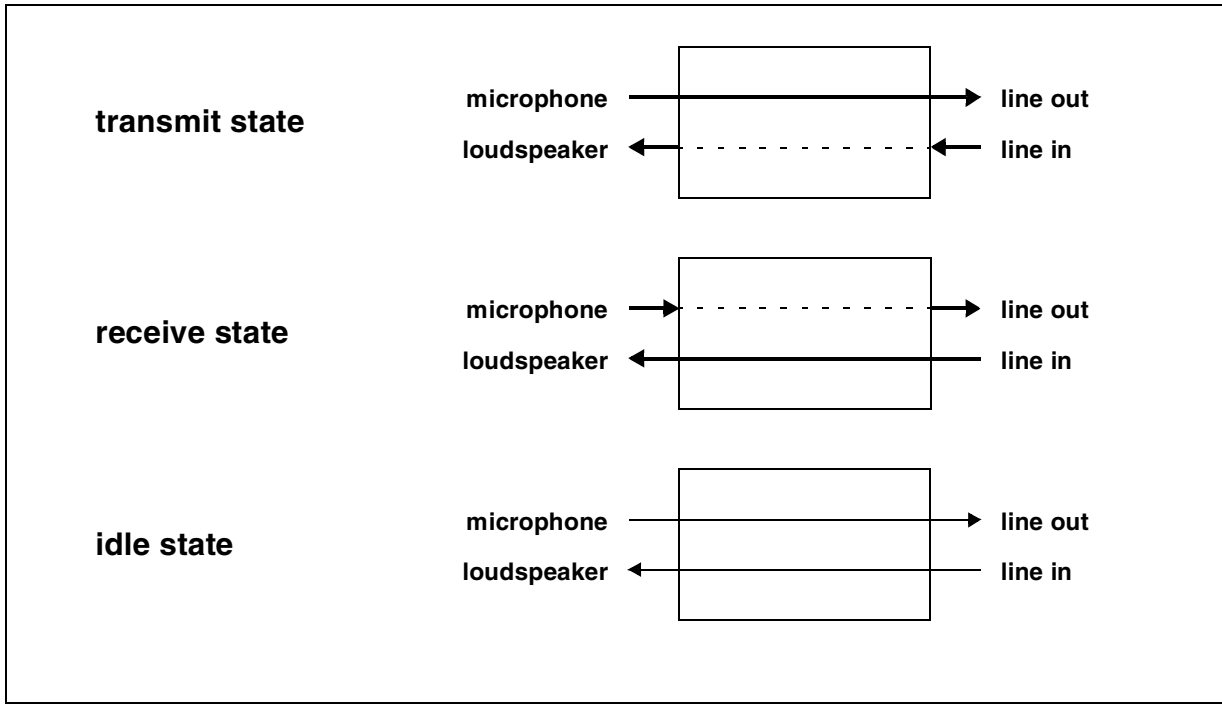


Figure 19 Echo Suppression Unit - States of Operation

Figure 20 shows the signal flow graph of the echo suppression unit in more detail.

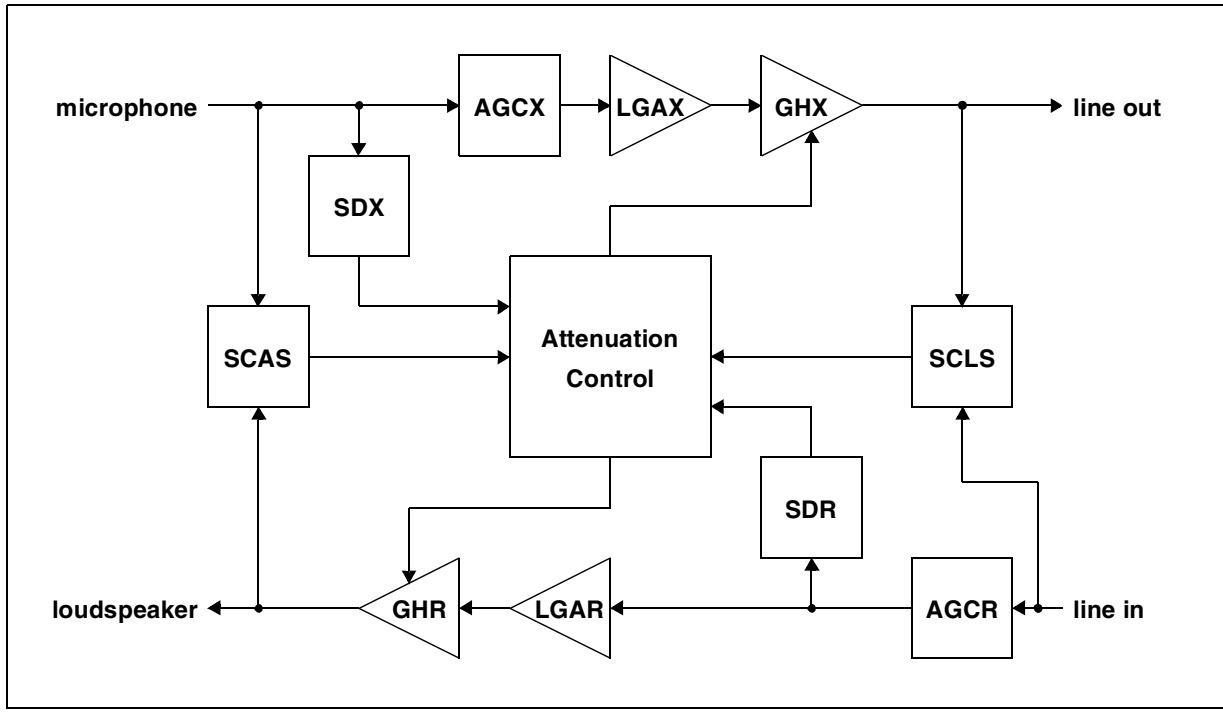


Figure 20 Echo Suppression Unit - Block Diagram

The Attenuation Control performs the switching between the three possible states by using the attenuation stages GHX and GHR. Actually, state switching is controlled by the speech comparators SCAS and SCLS and by the speech detectors SDX and SDR. The gain control units AGCX, AGCR, LGAX, and LGAR are used to achieve proper signal levels for each state.

All blocks are programmable. Thus, the telephone set can be optimized and adjusted to the particular geometrical and acoustical environment. The following sections discuss the blocks of the echo suppression unit in detail.

2.1.3.1 Speech Detector

For each signal source a speech detector (SDX, SDR) is available. The speech detectors are identical but can be programmed individually. Figure 21 shows the signal flow graph of a speech detector.

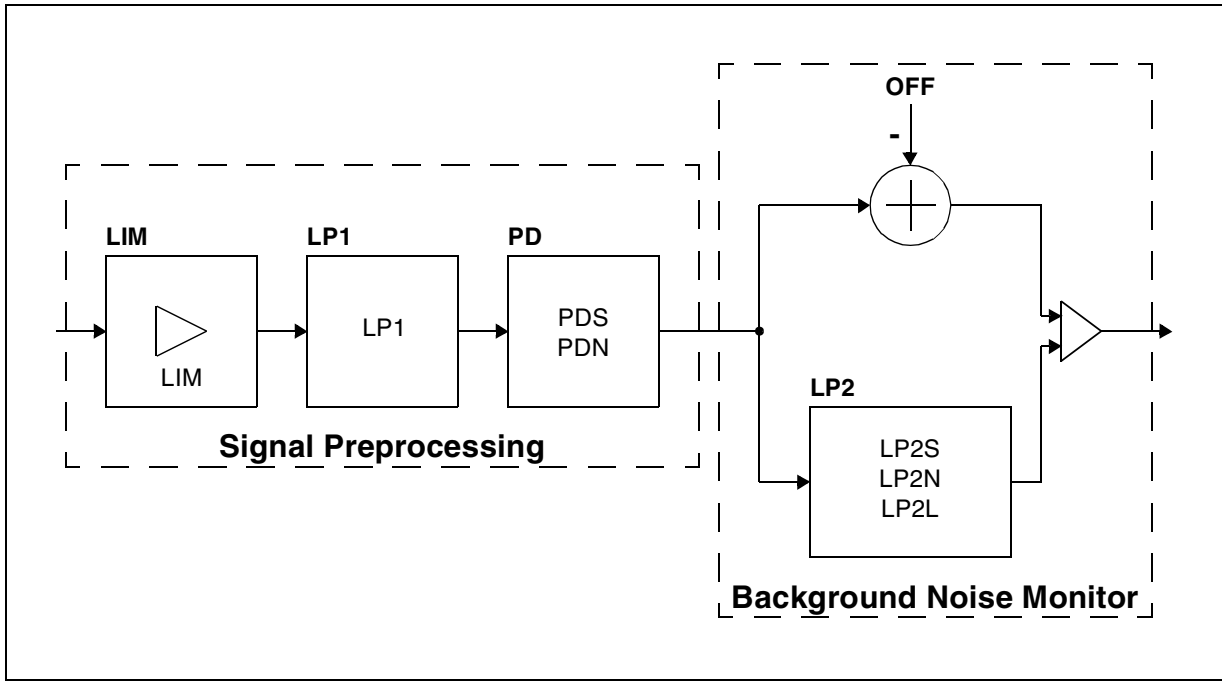


Figure 21 Speech Detector - Block Diagram

The first three units (LIM, LP1, PD) are used for preprocessing the signal while the actual speech detection is performed by the background noise monitor.

Background Noise Monitor

The tasks of the noise monitor are to differentiate voice signals from background noise, even if it exceeds the voice level, and to recognize voice signals without any delay. Therefore the Background Noise Monitor consists of the Low-Pass Filter 2 (LP2) and the offset in two separate branches. Basically it works on the burst-characteristic of the speech: voice signals consist of short peaks with high power (bursts). In contrast, background noise can be regarded approximately stationary from its average power.

Low-Pass Filter 2 provides different time constants for noise (non-detected speech) and speech. It determines the average of the noise reference level. In case of background noise the level at the output of LP2 is approximately the level of the input. As in the other branch an additional offset OFF is added to the signal, the comparator signals noise. At speech bursts the digital signals arriving at the comparator via the offset branch change faster than those via the LP2-branch. If the difference exceeds the offset OFF, the

comparator signals speech. Therefore the output of the background noise monitor is a digital signal indicating speech (1) or noise (0).

A small fade constant (LP2N) enables fast settling of LP2 to the average noise level after the end of speech recognition. However, a too small time constant for LP2N can cause rapid charging to such a high level that after recognizing speech the danger of an unwanted switching back to noise exists. It is recommended to choose a large rising constant (LP2S) so that speech itself charges the LP2 very slowly. Generally, it is not recommended to choose an infinite LP2S because then approaching the noise level is disabled. During continuous speech or tones the LP2 will be charged until the limitation LP2L is reached. Then the value of LP2 is frozen until a break discharges the LP2. This limitation permits transmission of continuous tones and “music on hold”.

The offset stage represents the estimated difference between the speech signal and averaged noise.

Signal Preprocessing

As described in the preceding chapter, the background noise monitor is able to discriminate between speech and noise. In very short speech pauses e.g. between two words, however, it changes immediately to non-speech, which is equal to noise. Therefore a peak detection is required in front of the Noise Monitor.

The main task of the Peak Detector (PD) is to bridge the very short speech pauses during a monolog so that this time constant has to be long. Furthermore, the speech bursts are stored so that a sure speech detection is guaranteed. But if no speech is recognized the noise low-pass LP2 must be charged faster to the average noise level. In addition, the noise edges are to be smoothed. Therefore two time constants are necessary. As the peak detector is very sensitive to spikes, the low-pass LP1 filters the incoming signal containing noise in a way that main spikes are eliminated. Due to the programmable time constant it is possible to refuse high-energy sibilants and noise edges.

To compress the speech signals in their amplitudes and to ease the detection of speech, the signals have to be companded logarithmically. Hereby, the speech detector should not be influenced by the system noise which is always present but should discriminate between speech and background noise. The limitation of the logarithmic amplifier can be programmed via the parameter LIM. LIM is related to the maximum PCM level. A signal exceeding the limitation defined by LIM is getting amplified logarithmically, while very smooth system noise below is neglected. It should be the level of the minimum system noise which is always existing; in the transmit path the noise generated by the telephone circuitry itself and in receive direction the level of the first bit which is stable without any speech signal at the receive path. Table 8 shows the parameters for the speech detector.

Table 8 Speech Detector Parameters

Parameter	# of bytes	Range	Comment
LIM	1	0 to -95 dB	Limitation of log. amplifier
OFF	1	0 to 95 dB	Level offset up to detected noise
PDS	1	1 to 2000 ms	Peak decrement PD1 (speech)
PDN	1	1 to 2000 ms	Peak decrement PD1 (noise)
LP1	1	1 to 2000 ms	Time constant LP1
LP2S	1	2 to 250 s	Time constant LP2 (speech)
LP2N	1	1 to 2000 ms	Time constant LP2 (noise)
LP2L	1	0 to 95 dB	Maximum value of LP2

The input signal of the speech detector can be connected to either the input signal of the echo suppression unit (as shown for SDX) or the output of the associated AGC (as shown for SDR).

2.1.3.2 Speech Comparators (SC)

The echo suppression unit has two identical speech comparators (SCAS, SCLS). Each comparator can be programmed individually to accommodate the different system characteristics of the acoustic interface and the line interface. As SCAS and SCLS are identical, the following description holds for both SCAS and SCLS.

The SC has two input signals SX and SR, which map to microphone/loudspeaker for SCAS and line in/line out for SCLS.

The speech comparator decides whether the signal coming in on SR is only an echo from the signal outgoing on SX or a real speech activity. The result is then interpreted by the Attenuation Control of figure 20. In general, the SC works according to the following equation:

$$\text{if} \quad SX > SR + V \text{ then switch state}$$

Therefore, SCAS controls the switching to transmit state and SCLS controls the switching to receive state. Switching is done only if SX exceeds SR by at least the expected acoustic level enhancement V. This level enhancement is divided into two parts: G and GD. A block diagram of the SC is shown in figure 22.

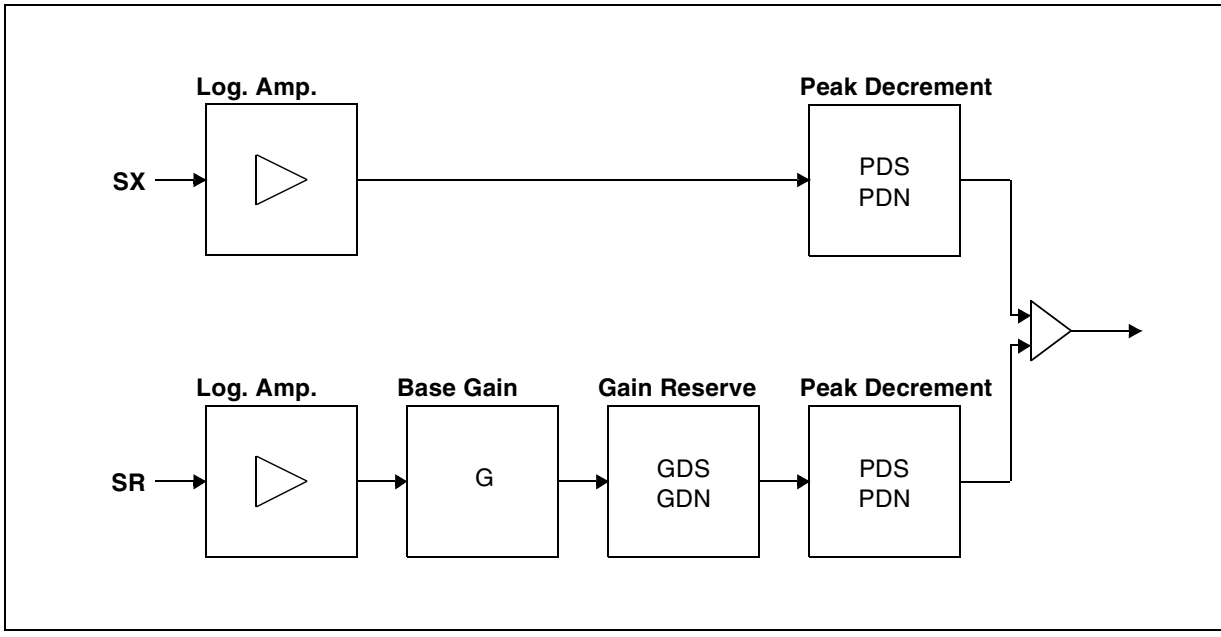


Figure 22 Speech Comparator - Block Diagram

At both inputs, logarithmic amplifiers compress the signal range. Hence, only logarithmic levels are on both paths and after the signals have been processed, logarithmic levels on both paths are compared.

The main task of the comparator is to control the echo. The internal coupling due to the direct sound and mechanical resonances is covered by G. The external coupling, mainly caused by the acoustic feedback, is controlled by GD/PD. An example for direct sound (1) and acoustic feedback (2) is illustrated in figure 23.

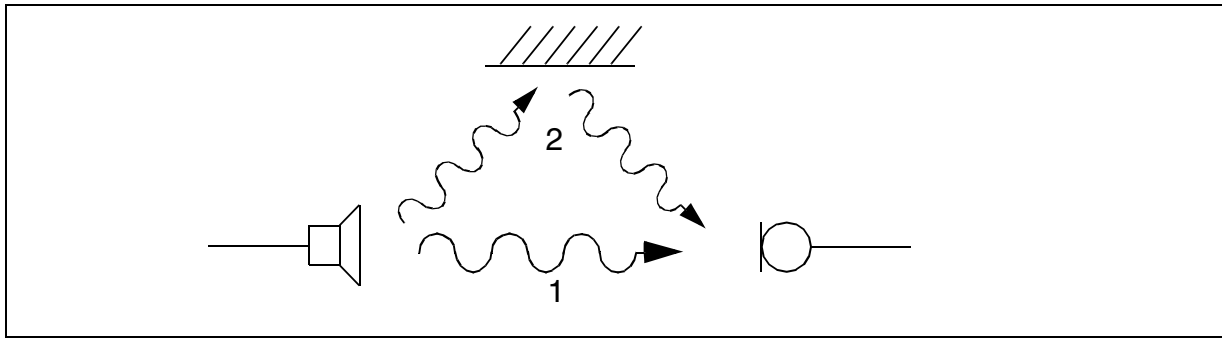


Figure 23 Speech Comparator - Acoustic Echoes

The base gain G corresponds to the terminal couplings of the complete telephone. Thus, G is the measured or calculated level enhancement between the receive and the transmit inputs of the SC.

To control the acoustic feedback two parameters are necessary: GD represents the actual reserve on the measured G. Together with the Peak Decrement (PD), the echo behavior at the acoustic side is modeled: After speech has ended there is a short time during which hard couplings through the mechanics and resonances and the direct echo are present. Till the end of that time (Δt), the level enhancement V must be at least equal to G to prevent clipping caused by these internal couplings. After that time (Δt), only the acoustic feedback is present. This coupling, however, is reduced by air attenuation. For this in general the longer the delay, the smaller the echo being valid. This echo behavior is taken care of by the decrement rate PD.

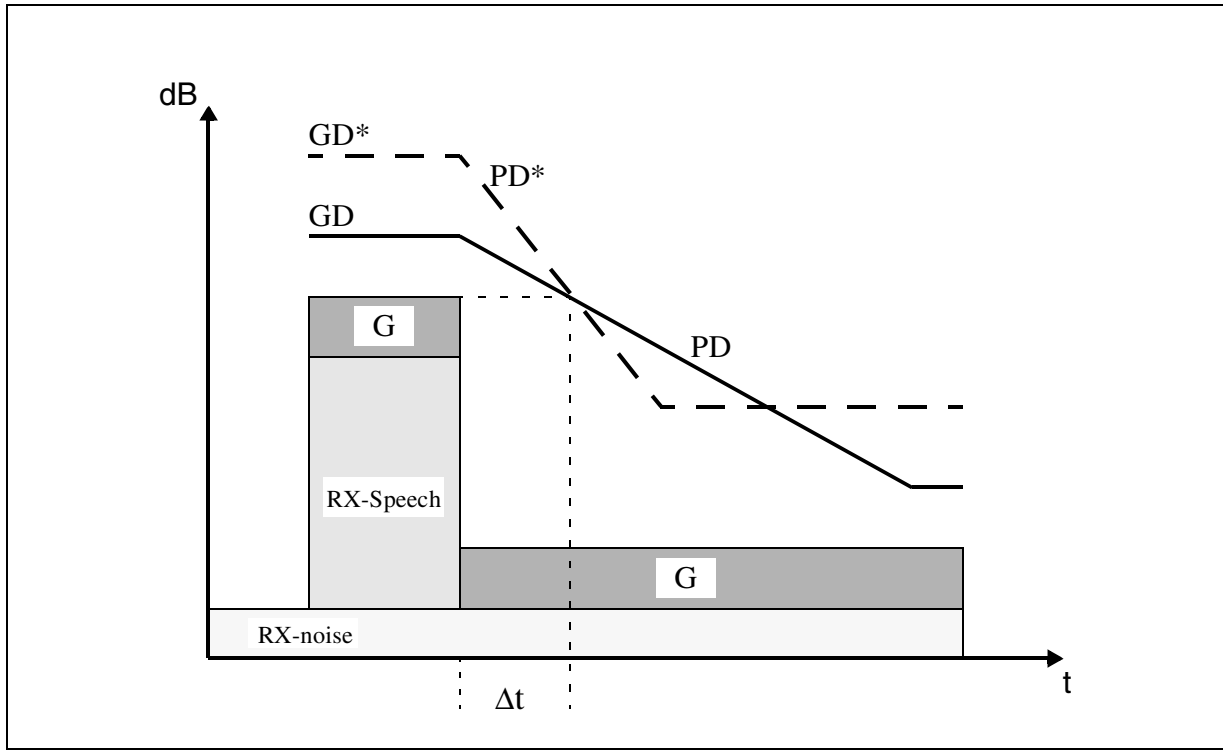


Figure 24 Speech Comparator - Interdependence of Parameters

According to figure 24, a compromise between the reserve GD and the decrement PD has to be made: a smaller reserve (GD) above the level enhancement G requires a longer time to decrease (PD). It is easy to overshout the other side but the intercommunication is harder because after the end of the speech, the level of the estimated echo has to be exceeded. In contrary, with a higher reserve (GD*) it is harder to overshout continuous speech or tones, but it enables a faster intercommunication because of a stronger decrement (PD*).

Two pairs of coefficients, GDS/PDS when speech is detected, and GDN/PDN in case of noise, offer a different echo handling for speech and non-speech. With speech, even if very strong resonances are present, the performance will not be worsened by the high GDS needed. Only when speech is detected, a high reserve prevents clipping.

The time ET [ms] after speech ends, the parameters of the comparator are switched to the “noise” values. If both sets of the parameters are equal, ET has no effect.

Table 9 Speech Comparator Parameters

Parameter	# of bytes	Range	Comment
G	1	– 48 to + 48 dB	Base Gain
GDS	1	0 to 48 dB	Gain Reserve (Speech)
PDS	1	0.025 to 6 dB/ms	Peak Decrement (Speech)

Table 9 Speech Comparator Parameters

Parameter	# of bytes	Range	Comment
GDN	1	0 to 48 dB	Gain Reserve (Noise)
PDN	1	0.025 to 6 dB/ms	Peak Decrement (Noise)
ET	1	0 to 992 ms	Time to Switch from speech to noise parameters

2.1.3.3 Attenuation Control

The attenuation control unit performs state switching by controlling the attenuation stages GHX and GHR. In receive state, the attenuation G is completely switched to GHX. In transmit state, the attenuation G is completely switched to GHR. In idle state, both GHX and GHR attenuate by G/2. State switching depends on the signals of one speech comparator and the corresponding speech detector.

The attenuation G is programmable. The attenuation G actually provided by the attenuation stages GHR and GHX is the attenuation determined by the parameter ATT minus the attenuation reported by the echo cancellation unit ($G = ATT - G_C$).

Additional (fixed) attenuation on the transmit and receive path is also influenced by the automatic gain control stages AGCX and AGCR, respectively.

While each state is associated with the programmed attenuation, the time T_{SW} it takes to reach the steady-state attenuation after a state switch can be programmed. The time T_{SW} depends on a programmable decay rate SW and the current attenuation G by the formula $T_{SW} = SW \times G$.

If the current state is either transmit or receive and no speech on either side has been detected for time T_{TW} then the idle state is entered. To smoothen the transition, the attenuation is incremented (decremented) by DS until the evenly distribution G/2 for both GHX and GHR is reached.

Table 10 summarizes the parameters for the attenuation unit.

Table 10 Attenuation Control Parameters

Parameter	# of bytes	Range	Comment
TW	1	16 ms to 4 s	T_{TW} to return to idle state
ATT	1	0 to 95 dB	Attenuation for GHX and GHR
DS	1	0.6 to 680 ms/dB	Decay Speed (to idle state)
SW	1	0.0052 to 10 ms/dB	Decay Rate (used for T_{SW})

Note: In addition, attenuation is also influenced by the Automatic Gain Control stages (AGCX, AGCR) in order to keep the total loop attenuation constant.

Note: By programming parameter DS to 0xFF idle mode is disabled and the speakerphone will remain in the last state. This parameter must be set before enabling the speakerphone.

2.1.3.4 Echo Suppression Status Output

The PSB 2170 can report the current state of the echo suppression unit to ease the optimization of the parameter set of the echo suppression unit. In this case the SPS_0 and SPS_1 pins are set according to table 11.

Table 11 SPS Encoding

SPS_0	SPS_1	Echo Suppression Unit State
0	0	no echo suppression operation
0	1	receive
1	0	transmit
1	1	idle

Furthermore the controller can read the current value of the SPS pins by reading register SPSCTL.

2.1.3.5 Loudhearing

The speakerphone unit can also be used for controlled loud-hearing. This is enabled by setting bit MD in register SCTL. If loud-hearing mode is enabled, the loudspeaker amplifier of the PSB 4851 (ALS) is used instead of GHR (figure 20) when appropriate to avoid oscillation. To use this feature, the PSB 4851 must be programmed to allow ALS override. The ALS field within the AFE control register AFECTL defines the value sent to the PSB 4851 if attenuation is necessary (see specification of the PSB 4851).

2.1.3.6 Automatic Gain Control

The echo suppression unit has two identical automatic gain control units AGCX and AGCR both referred to as AGC in this section.

Whether the automatic gain control AGC amplifies or attenuates depends on whether the signal level is above or below the threshold level defined by parameter COM. The threshold is relative to the maximum PCM-value and thus negative. The parameters AG_GAIN and AG_ATT determine the maximal amplification and attenuation, respectively. The bold line in figure 25 gives an example for the steady-state output level of the AGC as a function of the input level.

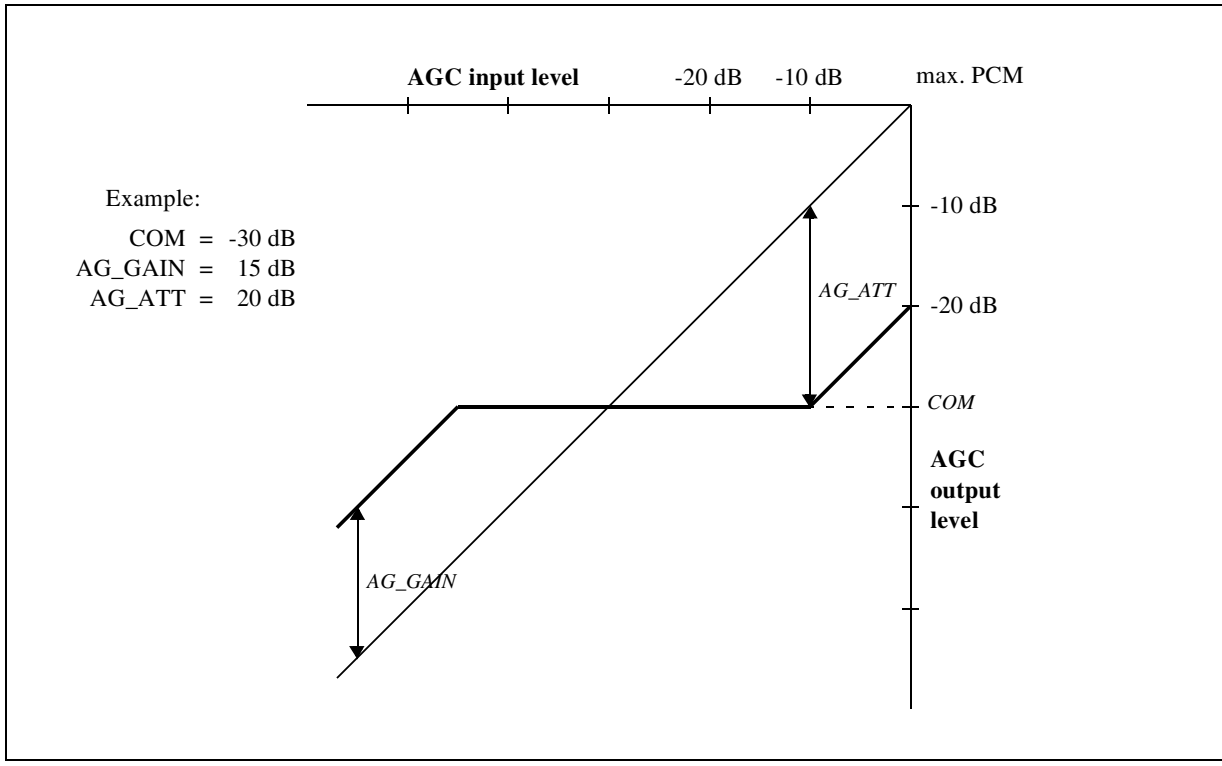


Figure 25 Echo Suppression Unit - Automatic Gain Control

For reasons of physiological acceptance, the AGC gain is automatically reduced in case of continuous background noise (e.g. by ventilators). The reduction is programmed via the NOIS parameter. When the noise level exceeds the threshold determined by NOIS, the amplification will be reduced by the same amount the noise level is greater than the threshold.

The regulation speed is controlled by SPEEDH for signal amplitudes above the threshold and SPEEDL for amplitudes below. Usually SPEEDH will be chosen to be at least 10 times faster than SPEEDL. An additional low pass with time constant LP is provided to avoid an immediate response of the AGC to very short signal bursts. The time constant of the low pass should not be selected longer than 4 ms in order to avoid unstable behavior.

If the speech detector SDX detects noise or the receive path is active, AGCX freezes its current attenuation and the last gain setting is used. Regulation starts with this value as soon as SDX detects speech and the receive path is inactive. Likewise, if SDR detects noise or the transmit path is active, AGCR freezes its current attenuation and the last gain setting is used. Regulation starts with this value as soon as SDR detects speech and the transmit path is inactive.

The current gain/attenuation of the AGC can be read at any time (AG_CUR). When the AGC has been disabled, the initial gain used immediately after enabling the AGC can be programmed. Table 12 shows the parameters of the AGC.

Table 12 Automatic Gain Control Parameters

Parameter	# of Bytes	Range	Comment
AG_INIT	1	-95 dB to 95dB	Initial AGC gain/attenuation
COM	1	0 to – 95 dB	Compare level rel. to max. PCM-value
AG_ATT	1	0 to -95 dB	Attenuation range
AG_GAIN	1	0 to 95 dB	Gain range
AG_CUR	1	-95 dB to 95 dB	Current gain/attenuation
SPEEDL	1	0.25 to 62.5 dB/s	Change rate for lower levels
SPEEDH	1	0.25 to 62.5 dB/s	Change rate for higher levels
NOIS	1	0 to – 95 dB	Threshold for AGC-reduction by background noise
LPA	1	0.025 to 4 ms	AGC low pass time constant

Note: There are two sets of parameters, one for AGCX and one for AGCR.

Note: By setting AG_GAIN to 0 dB a limitation function can be realized with the AGC.

2.1.3.7 Fixed Gain

Each signal path features an additional amplifier (LGAX, LGAR) that can be set to a fixed gain. These amplifiers should be used for the basic amplification in order to avoid saturation in the preceding stages. Table 13 shows the only parameter of this stage.

Table 13 Fixed Gain Parameters

Parameter	# of Bytes	Range	Comment
LGA	1	-12 dB to 12 dB	always active

2.1.3.8 Mode Control

Table 14 shows the registers used to determine the signal sources and the mode.

Table 14 Speakerphone Registers

Register	# of Bits	Name	Comment
SCTL	1	ENS	Echo suppression unit enable
SCTL	3	QU	Echo cancellation unit enable
SCTL	1	MD	Speakerphone or loudhearing mode
SCTL	1	AGX	AGCX enable

Table 14 Speakerphone Registers

SCTL	1	AGR	AGCR enable
SCTL	1	SDX	SDX input tap
SCTL	1	SDR	SDR input tap
AFECTL	4	ALS	ALS value for loudhearing
SSRC1	5	I1	Input signal 1 (microphone)
SSRC1	5	I2	Input signal 2 (microphone)
SSRC2	5	I3	Input signal 3 (line in)
SSRC2	5	I4	Input signal 4 (line in)

2.1.4 Comfort Noise Generator

The full duplex speakerphone can be extended by a comfort noise generator which can enhance the performance of the speakerphone in noisy environments. The purpose of the comfort noise is to reduce signal modulation when the echo suppression unit switches the attenuation. The operation is as follows:

As long as the echo suppression unit is in transmit state no additional noise is added to the outgoing signal. In this state there is already the natural noise transmitted to the line.

In addition the comfort noise generator estimates the noise at the microphone input when no speech is detected by either of the three speech detectors (SD, SDX, SDR).

Once the echo suppression unit switches to receive or idle state the comfort noise generator generates noise similar to the external noise and adds this noise to the outgoing signal. Figure 26 shows the integration of the comfort noise generator into the speakerphone.

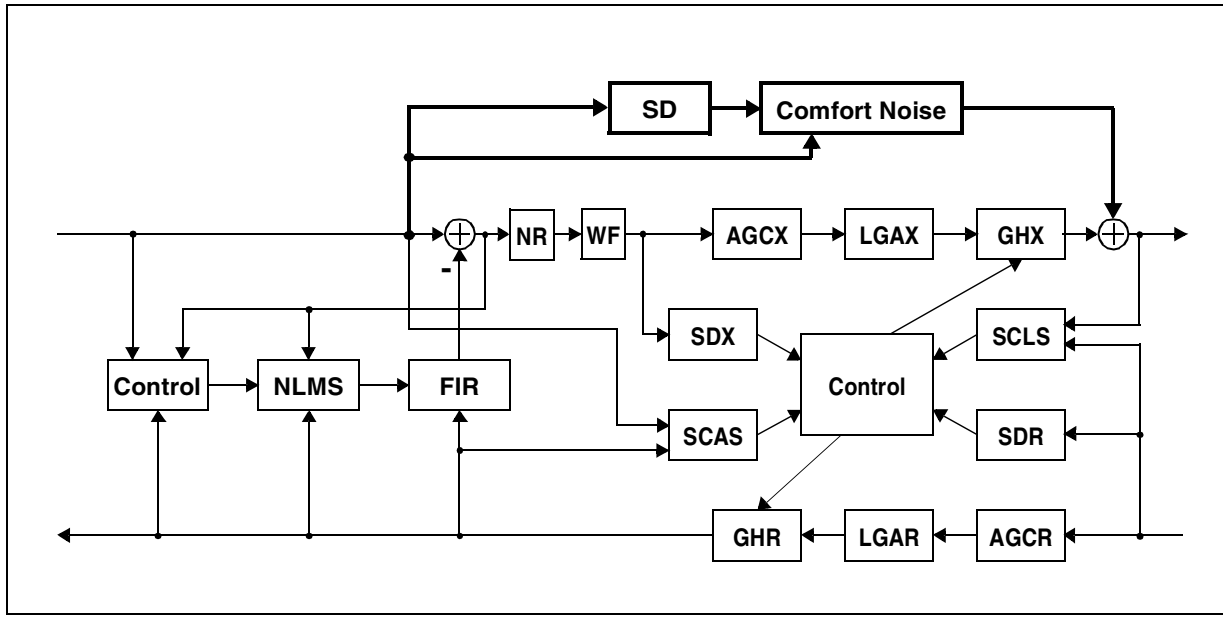


Figure 26 Comfort Noise Generator - Integration into Speakerphone

If the new blocks SD and Comfort Noise are removed the remaining blocks resemble the speakerphone as shown in figures 16 and 20. Therefore the comfort noise generator can be considered an optional extension to the speakerphone.

The new speech detector SD works as the speech detectors SDX and SDR described in section 2.1.3.1. The parameters of the speech detector are thus the same as shown in table 8.

The comfort noise generator adapts itself to the currently present noise at the input signal with respect to the energy level and the spectrum. Furthermore it is possible to program a constant noise level which is always present (even if there is no noise at the input signal present).

The comfort noise generator is enabled with the bit CN in the control register SCTL. Note that in order to use the comfort noise generator, the noise controlled adaption must be enabled as well. The noise controlled adaptation is described in the next section.

There are three parameters for comfort noise generator:

1. The adaptation speed LP
2. The constant noise level CONST which determines a noise level that is always added.
3. The factor FAC by which the present noise is scaled for the output of the noise generator.

Table 15 shows the associated registers.

Table 15 Comfort Noise Generator Registers

Register	# of Bits	Name	Comment
SCTL	1	CN	Comfort Noise enable (bit NAD must be set)
SCCN1	15	CONST	Level of Constant Noise
SCCN2	15	FAC	Factor for Multiplication
SCCN3	15	LP	Adaptation Time Constant

As described in chapter 3.7 in detail, several modules must be disabled before the comfort noise generator is enabled. Also some parameters of the disabled modules are overwritten by the noise controlled adaptation. This means that if these disabled modules are going to be enabled after the comfort noise generator has been used, these parameters must be set again.

2.1.5 Noise Controlled Adaptation

Several quantities that are important for the full-duplex speakerphone depend on the level of the background noise. An easy example is the correlation between the signal at the microphone and the signal at the loudspeaker in case of single talk from the line side. Obviously, if no noise is present at the near end side, the signal at the microphone is only generated by the acoustic echo of the signal from the loudspeaker and thus very similar to the signal from the loudspeaker. In case of noise at the near end side, the similarity of the signals is minor. Since such quantities as this correlation depend on the noise level at the near end side, some parameters must depend on the noise level in order to ensure true full-duplex speakerphone quality. This is meant with the term “noise controlled adaption”.

The noise controlled adaptation is enabled by setting the bit NAD in the control register SCTL.

The adjustments described in the sequel depend on the level of the noise at the near end side. The noise level is determined as follows. In case the speech detector SD, which is described in section 2.1.4, indicates that no speech is present, then the energy of the microphone signal filtered by a low pass is called the noise level *L*. In case the speech detector SD indicates speech, then the last output of the low pass is called noise level *L*. The time constant of the low pass is programmable with the parameter TC as shown in table 16.

Table 16 general Noise Control Adaption Register

Register	# of Bits	Name	Comment
SCTL	1	NAD	Noise adaptation enable
SCLPT	15	TC	Time constant for the low pass

2.1.5.1 Correlation Adaptation

The control block (figures 14 and 16) of the echo cancellation unit monitors the correlation between the loudspeaker signal and the microphone signal. Only when the correlation of the loudspeaker and microphone signal exceeds a threshold *T*, the attenuation achieved by the echo cancellation unit is measured. In a noisy environment the correlation will decrease even if the echo cancellation unit is fully adapted. Therefore the threshold *T* might not be exceeded in this situation. As a result the echo cancellation unit would not report any achieved echo return loss enhancement and thus the echo suppression unit would have to provide all of the desired attenuation.

To avoid this situation the threshold *T* can be adjusted dynamically with the noise level *L*. Figure 27 shows the available parameters for the adaptation of the threshold.

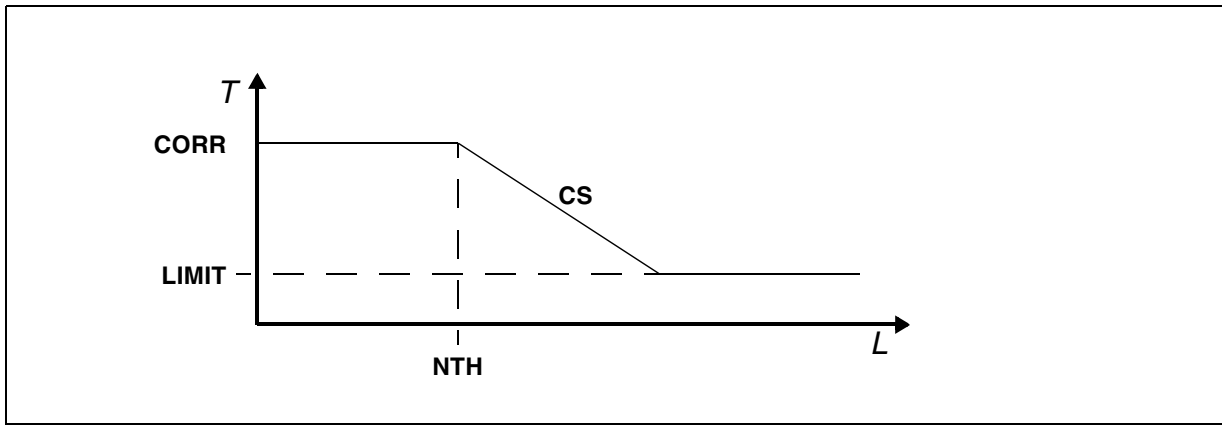


Figure 27 Correlation Adaptation

As long as the noise level *L* is less than the threshold NTH the threshold *T* remains at its programmed value CORR. This parameter has only an effect when the noise controlled adaption is enabled (SCTL:NAD is set). If the noise controlled adaption is disabled, a default value is used instead.

With enabled noise controlled adaption, once the threshold NTH is exceeded, the correlation threshold decreases with the programmable slope CS. However, the threshold will not fall below the programmable limit LIMIT even if the noise level *L* increases further. Table 17 shows the registers associated with the correlation adaptation.

Table 17 Correlation Adaptation Registers

Register	# of Bits	Name	Comment
SCCR	14	CORR	Factor C
SCCRN	15	NTH	Noise Threshold
SCCRS	12	CS	Slope
SCCRL	14	LIMIT	Limit for C

2.1.5.2 Double Talk Detection Adaptation

During double talk the necessary echo return loss for comfortable full duplex conversation may be reduced. The provides the parameter SAEDTR:AECDTR for this purpose. Double talk is detected when the difference between the signal before and after the echo cancellation (subtraction point) suddenly decreases by an amount *D*.

The noisier the environment gets the smaller the amount *D* should be. Otherwise the echo cancellation would fail to detect the relatively smaller change that indicates a double talk detection. Figure 28 shows the provisions made by the for an adaptive double talk detection.

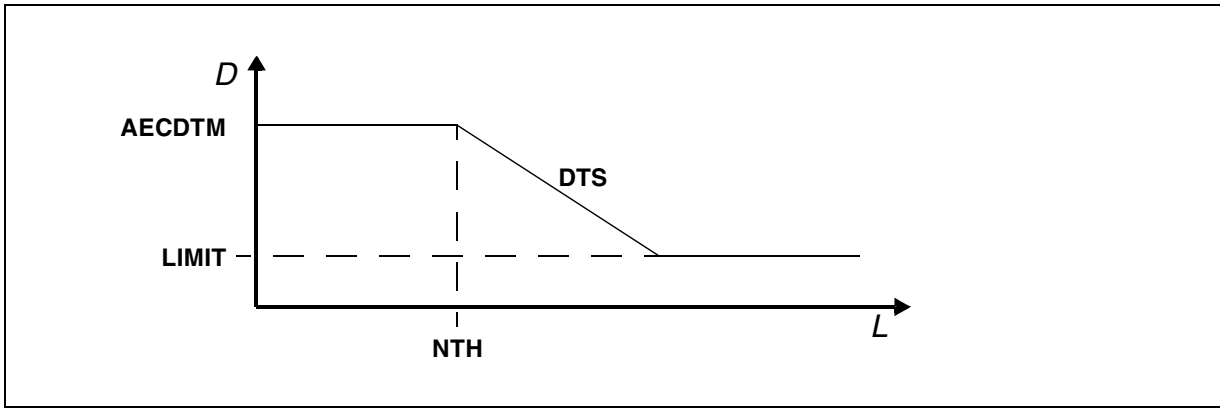


Figure 28 Double Talk Detection Adaptation

As long as the noise level *L* is less than the threshold NTH the necessary difference *D* remains at its programmed value AECDTM. Once the threshold is exceeded, *D* decreases with the programmable slope DTS. However, it will not fall below the programmable limit LIMIT even if the noise level *L* increases further. Table 18 shows the registers associated with the double talk detection adaptation.

Table 18 Double Talk Detection Adaptation Registers

Register	# of Bits	Name	Comment
SAEDTL	15	AECDTM	Minimum energy to detect double talk.
SCDTN	15	NTH	Noise Threshold
SCDTS	12	DTS	Slope
SCDTL	15	LIMIT	Limit for DTD

2.1.5.3 Adaptive Attenuation Reduction

In noisy environments it is acceptable to reduce the total attenuation ATT (chapter 2.1) as the noise level increases. This is due to the fact that the noise already presents some kind of local talk. Hence an increased echo is not perceived as disturbing as in a silent environment.

In order to exploit this, the provides an attenuation decrease dependent on the noise level: ATT = A_{sofar} - ATR, where A_{sofar} is the attenuation provided by the echo cancellation and echo suppression as described in chapters 2.1.1 to 2.1.3. Figure 29 shows the attenuation reduction provided by the .

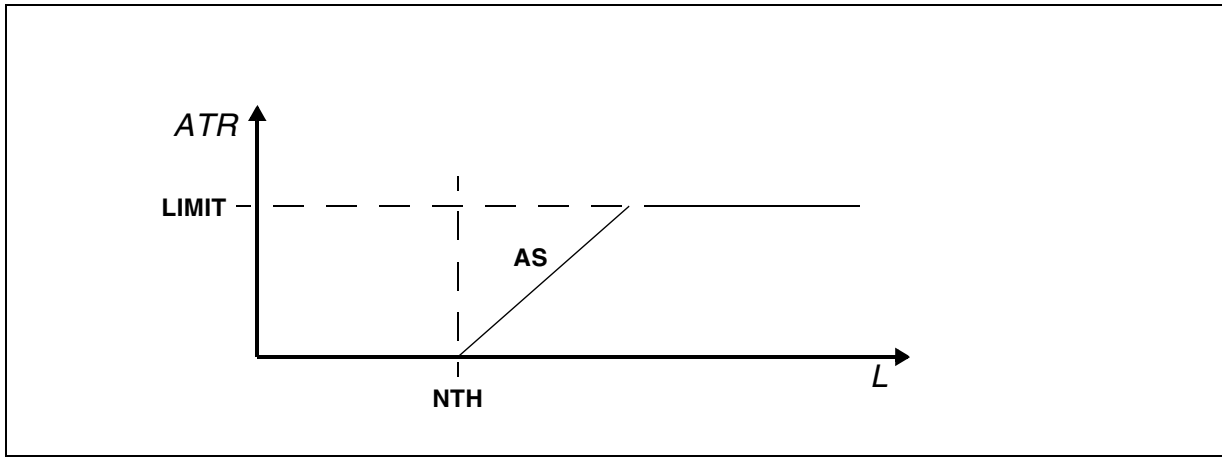


Figure 29 Adaptive Attenuation Reduction

As long as the noise level L is less than the threshold NTH the total attenuation is not reduced at all. Once the threshold exceeded, the total attenuation is decreased more and more by increasing ATR. The sensitivity is programmable by the parameter AS. However, ATR will not exceed the programmable limit LIMIT even if the noise level *L* increases further. Table 19 shows the registers associated with the adaptive attenuation reduction.

Table 19 Adaptive Attenuation Reduction Registers

Register	# of Bits	Name	Comment
SCATTN	15	NTH	Noise Threshold
SCATTS	15	AS	Attenuation Sensitivity
SCATTL	15	LIMIT	Limit for DTD

The adaptive attenuation reduction influences the attenuation provided by GHX and GHR. Thus if the attenuation of the stages is set to 0 dB, the adaptive attenuation reduction has no influence as the attenuation of GHX or GHR can never drop below 0 dB.

2.1.5.4 Loudspeaker Gain Adaptation

In noisy environments it is useful to automatically increase the signal level of the loudspeaker output with increasing noise level. The features such an automatic gain adaptation by adding additional gain to the module LGAR described in section 2.1.3.7. Figure 30 illustrates the additional gain provided by the .

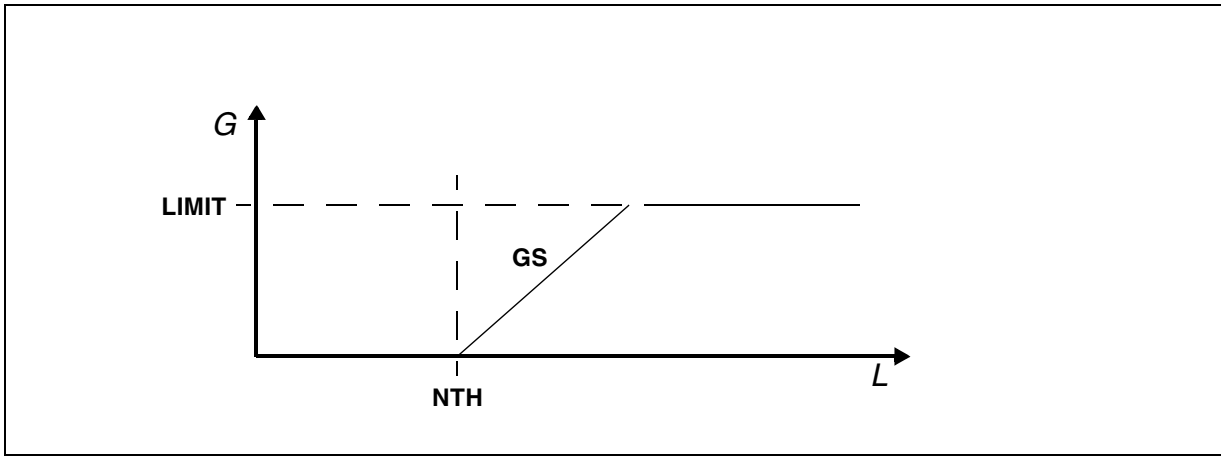


Figure 30 Loudspeaker Gain Adaptation

As long as the noise level *L* is less than the threshold NTH there is no additional gain. Once the threshold is exceeded, the gain G is increased with the programmable sensitivity GS. However, it will not exceed the programmable limit LIMIT even if the noise level *L* increases further. Table 20 shows the registers associated with the loudspeaker gain adaptation.

Table 20 Loudspeaker Gain Adaptation Registers

Register	# of Bits	Name	Comment
SCLSPN	15	NTH	Noise Threshold
SCLSPS	15	GS	Gain Sensitivity
SCLSPL	15	LIMIT	Limit for G

Note: The total attenuation programmed for the speakerphone in register SATT1:ATT is not automatically increased when the loudspeaker gain adaptation increases. Therefore, the adaptive attenuation reduction (chapter 2.1.5.3) should be reduced accordingly.

2.2 Line Echo Cancellation Unit

The contains an adaptive line echo cancellation unit for the cancellation of near end echoes. The unit has three modes: The two modes normal mode and superior mode consider up to 4 ms echo length. In superior mode, a shadow filter is used additionally to the normal mode in order to improve the echo cancellation quality. The third mode is the extended mode. It works basically like the superior mode but considers line echoes of up to 8 ms echo length.

The line echo cancellation unit is especially useful in front of the various detectors (DTMF, CPT, etc.). A block diagram is shown in figure 31.

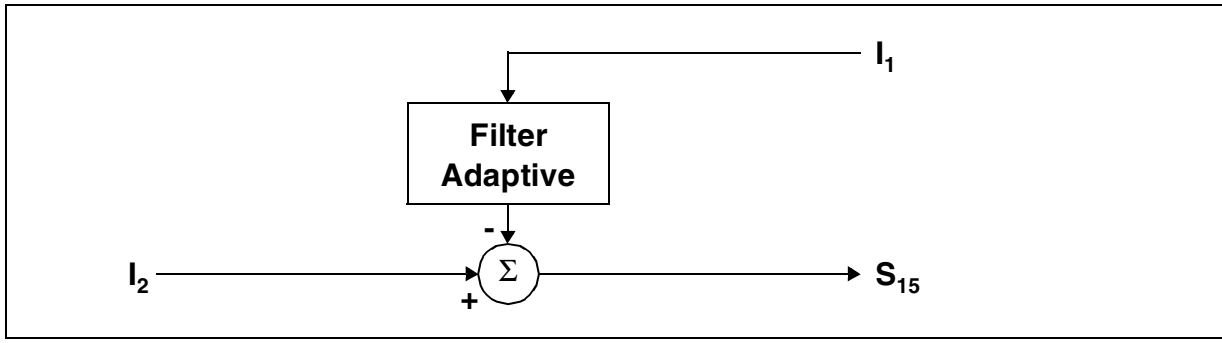


Figure 31 Line Echo Cancellation Unit - Block Diagram

Input I_2 is usually connected to the line input while input I_1 is connected to the outgoing signal.

In **normal mode** the adaptation process is controlled by the three parameters MIN, ATT and MGN. Adaptation takes place only if both of the following conditions hold:

1. I1 > MIN
2. I1 – ATT + MGN > I2

With the first condition, adaptation to weak signals can be avoided. The second condition avoids adaptation during double talk. The parameter ATT represents the echo loss provided by external circuitry. The adaptation stops if the power of the received signal (I2) exceeds the power of the expected signal (I1-ATT) by more than the margin MGN.

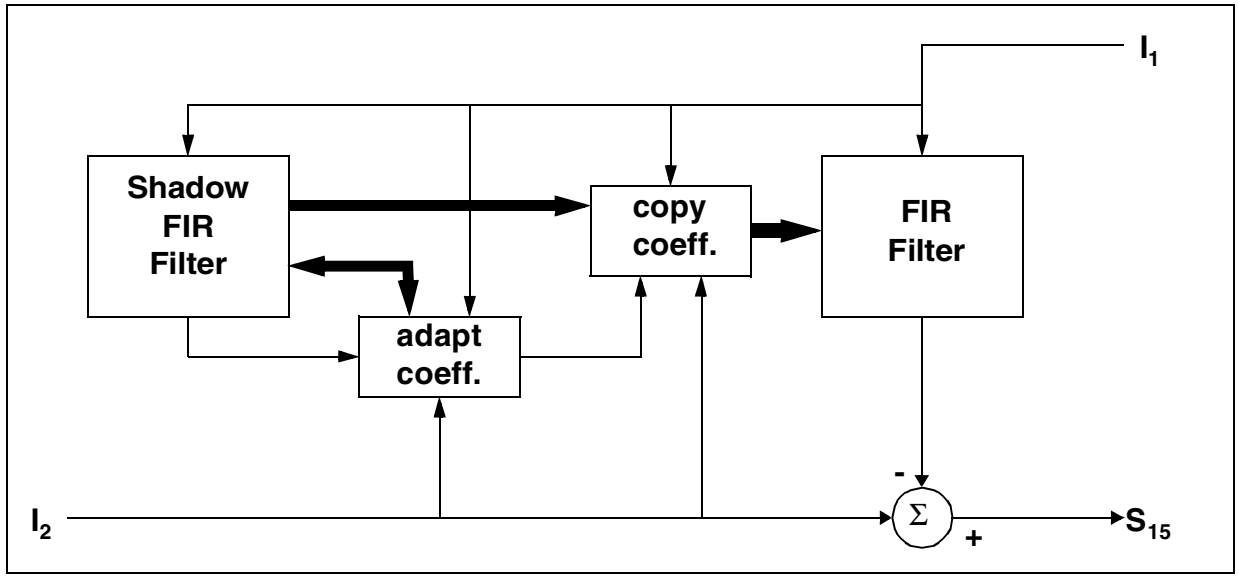


Figure 32 Line Echo Cancellation Unit - Superior Mode with Shadow FIR

The basic idea of the **superior mode** is shown in figure 32. The shadow FIR filter on the left hand side gets its coefficients adapted similarly to the adaptive filter of the Line Echo Canceller in normal mode. For cancelling the line echo, however, the FIR filter on the right hand side is used. When the quality of this FIR filter is excelled by the quality of the shadow FIR filter, the coefficients of the shadow FIR filter are copied to the FIR on the right hand side. More formally, the coefficients of the shadow FIR filter are adapted (see unit “adapt coeff” in figure 32) if similar to normal mode, the following two conditions hold:

1. $I1 > MIN$
2. $I1 - I2 - ATT > 0$

In this case, ATT is already the difference between external echo loss and margin ($ATT_{superior} = ATT_{normal} - MGN_{normal}$) so that the condition is actually the same as for normal mode. The parameter ATT should be adjusted accordingly. Note that ATT can now be negative.

The coefficients are copied from the shadow FIR filter to the actually used FIR filter (see unit “copy coeff.” in figure 32) if

1. currently the adaptation of the shadow FIR filter is in progress

and at least one of the following two conditions holds:.

2. $ATTS - ATTA > MGN$
   The attenuation of the shadow FIR filter ATTS is better than the attenuation of the actually used FIR filter ATTA by a margin MGN. Note that in superior mode, the parameter MGN has a different meaning than in normal mode
3. $TTS(t) > max(ATTS(t-1), \ldots, ATTS(\text{last time condition 2 has been valid}))$
   The current attenuation ATTS of the shadow FIR is better than at any time since the last update according to condition 2.

The **extended mode** works like the superior mode but the FIR considers line echoes of up to 8 ms echo length. Since the computational effort increases with increasing FIR length, the parameter SP offers a trade-off between adaptation speed and computational costs. With SP set, all shadow FIR parameters are adapted every 125 us and thus the adaptation speed is as in superior mode. With SP cleared, half the shadow FIR parameters are updated every 125 us in such a way that one half of the parameters and the other half are updated alternately. As indicated in table 50, the computational costs decrease and so does the adaptation speed of the line echo canceller.

Table 21 shows the registers associated with the line echo canceller.

Table 21 Line Echo Cancellation Unit Registers

Register	# of Bits	Name	Comment	Relevant Mode
LECCTL	1	EN	Line echo canceller enable	all
LECCTL	2	CM	00: Normal mode 01: Superior mode 10: Extended mode 11: reserved	all
LECCTL	1	AS	Adaptation stop	all
LECCTL	1	SP	Adaptation speed	extended
LECCTL	5	I2	Input signal selection for I_2	all
LECCTL	5	I1	Input signal selection for I_1	all
LECLEV	15	MIN	Minimal power for signal I_1	all
LECATT	15	ATT	Externally provided attenuation (I_1 to I_2)	all
LECMGN	15	MGN	Margin	all

The adaptation of the coefficients can be stopped by setting bit AS in register LECCTL. This holds for all three modes of the Line Echo Canceller. Furthermore for superior and extended mode, also copying the coefficients from the shadow FIR is disabled.

2.3 DTMF Detector

The contains an DTMF detector that recognizes the sixteen standard DTMF tones. Figure 33 shows a block diagram of the DTMF detector. The results of the detector are available in the status and a dedicated result register. These registers can be read by the external controller via the serial control interface (SCI).

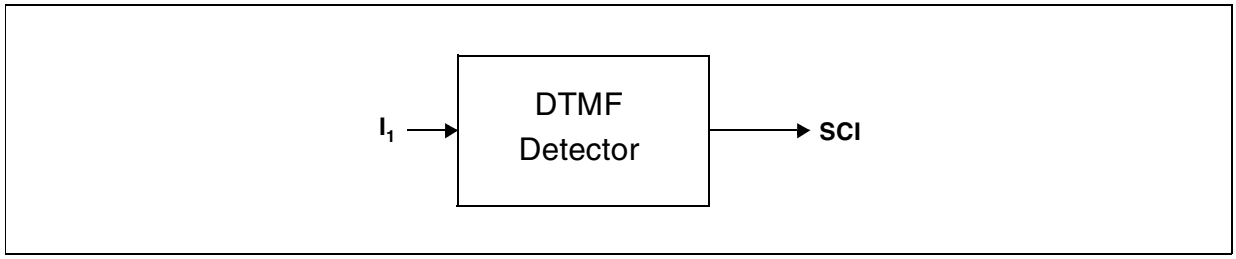


Figure 33 DTMF Detector - Block Diagram

Table 22 to 24 show the associated registers.

Table 22 DTMF Detector Control Register

Register	# of Bits	Name	Comment
DDCTL	1	EN	DTMF detector enable
DDCTL	5	I1	Input signal selection

As soon as a valid DTMF tone is recognized, the status word and the DTMF tone code are updated (table 23).

Table 23 DTMF Detector Results

Register	# of Bits	Name	Comment
STATUS	1	DTV	DTMF code valid
DDCTL	5	DTC	DTMF tone code

DTV is set when a DTMF tone is currently recognized and cleared when no DTMF tone is recognized or the detector is disabled. The code for the DTMF tone is provided in register DDCTL. DTC is valid when DTV is set and until the next incoming DTMF tone. The registers DDTW and DDLEV contain the parameters for detection (table 24).

Table 24 DTMF Detector Parameters

Register	# of Bits	Name	Comment
DDTW	15	TWIST	Twist for DTMF recognition
DDLEV	6	MIN	Minimum signal level to detect DTMF tones

2.4 Call Progress Tone Detector

The selected signal is monitored continuously for a call progress tone. The CPT detector consists of a band-pass and an optional timing checker (figure 34).

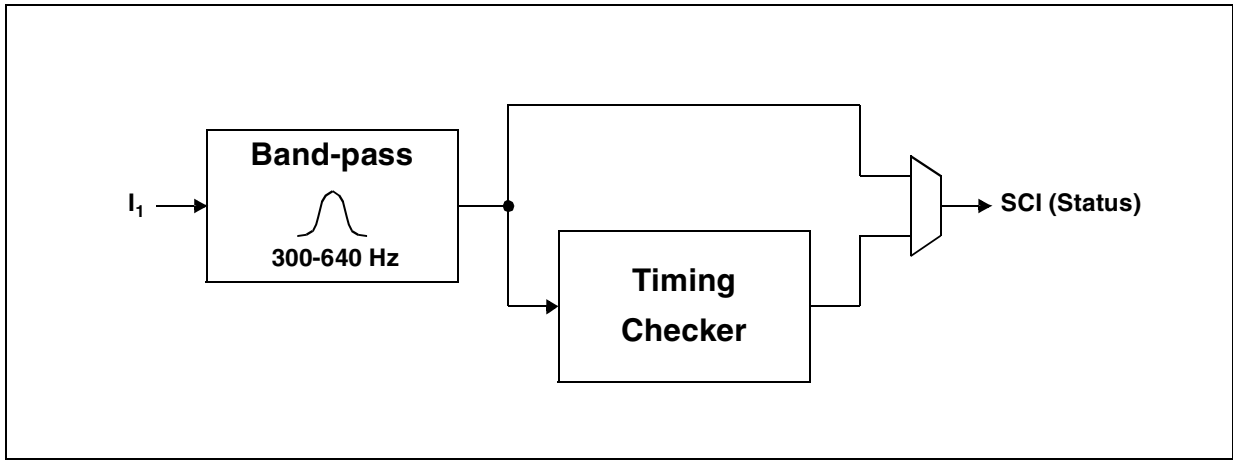


Figure 34 Call Progress Tone Detector - Block Diagram

The CPT detector can be used in two modes: raw and cooked. In raw mode, the occurrence of a signal within the frequency, time and energy limits is directly reported. The timing checker is bypassed and therefore the does not interpret the length or any interval of the signal.

In cooked mode, the number and duration of signal bursts are interpreted by the timing checker. A signal burst followed by a gap is called a cycle. Cooked mode requires a minimum of two cycles. The CPT flag is set with the first burst after the programmed number of cycles has been detected. The CPT flag remains set until the unit is disabled or speech is detected, even if the conditions are not met anymore. In this mode the CPT is modelled as a sequence of identical bursts separated by gaps with identical length. The can be programmed to accept a range for both the burst and the gap. It is also possible to specify a maximum aberration of two consecutive bursts and gaps. Figure 35 shows the parameters for a single cycle (burst and gap).

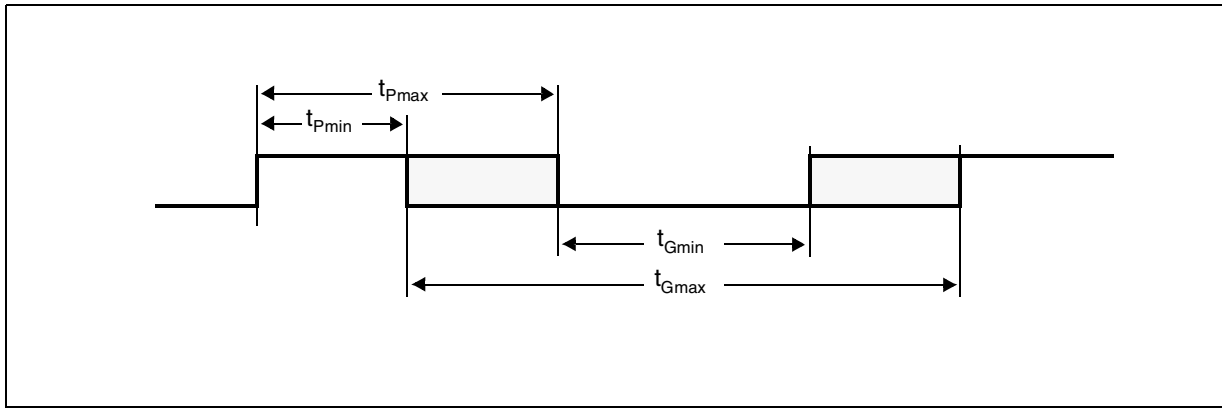


Figure 35 Call Progress Tone Detector- Cooked Mode

The status bit is defined as follows:

Table 25 Call Progress Tone Detector Results

Register	# of Bits	Name	Comment
STATUS	1	CPT	CP tone currently detected [340 Hz; 640 Hz]

CPT is not affected by reading the status word. It is automatically reset when the unit is disabled. Table 26 shows the control register for the CPT detector.

Table 26 Call Progress Tone Detector Registers

Register	# of Bits	Name	Comment
CPTCTL	1	EN	Unit enable
CPTCTL	1	MD	Mode (cooked, raw)
CPTCTL	5	I1	Input signal selection
CPTMN	8	MINB	Minimum time of a signal burst (t_{Pmin})
CPTMN	8	MING	Minimum time of a signal gap (t_{Gmin})
CPTMX	8	MAXB	Maximum time of a signal burst (t_{Pmax})
CPTMX	8	MAXG	Maximum time of a signal gap (t_{Gmax})
CPTDT	8	DIFB	Maximum difference between consecutive bursts
CPTDT	8	DIFG	Maximum difference between consecutive gaps
CPTTR	3	NUM	Number of cycles (cooked mode), 0 (raw mode)
CPTTR	8	MIN	Minimum signal level to detect tones
CPTTR	4	SN	Minimal signal-to-noise ratio

If any condition is violated during a sequence of cycles the timing checker is reset and restarts with the next valid burst.

Note: In cooked mode CPT is set with the first burst after the programmed number of cycles has been detected. If CPTTR:NUM = 2, then CPT is set with the third signal burst.

Note: The number of cycles must be set to zero in raw mode.

2.5 Alert Tone Detector

The alert tone detector can detect the standard alert tones (2130 Hz and 2750 Hz) for caller id protocols. The results of the detector are available in the status register and register ATDCTL0. These registers can be read by the external controller via the serial control interface (SCI).

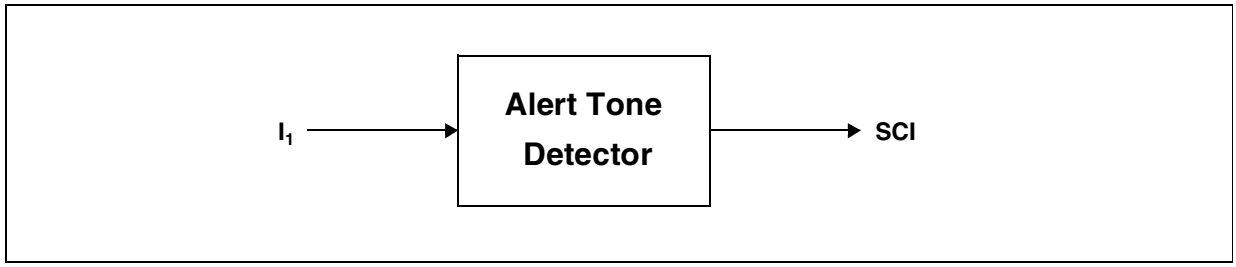


Figure 36 Alert Tone Detector - Block Diagram

Table 27 Alert Tone Detector Registers

Register	# of Bits	Name	Comment
ATDCTL0	1	EN	Alert Tone Detector Enable
ATDCTL0	5	I1	Input signal selection
ATDCTL1	1	MD	Detection of dual tones or single tones
ATDCTL1	1	ONH	On hook mode
ATDCTL1	1	DEV	Maximum deviation (0.5% or 1.1%)
ATDCTL1	8	MIN	Minimum signal level to detect alert tones

As soon as a valid alert tone is recognized, the status word of the and the code for the detected combination of alert tones are updated (table 28). With On Hook mode selected, the end of the alert tone can be detected faster. On Hook mode assumes that there is no speech signal present.

Table 28 Alert Tone Detector Results

Register	# of Bits	Name	Comment
STATUS	1	ATV	Alert tone detected
ATDCTL0	2	ATC	Alert tone code

2.5.1 Universal Tone Detector

The universal tone detector can be used instead of the CPT detector to detect special tones which are not covered by the standard CPT band-pass. Figure 37 shows the functional block diagram.

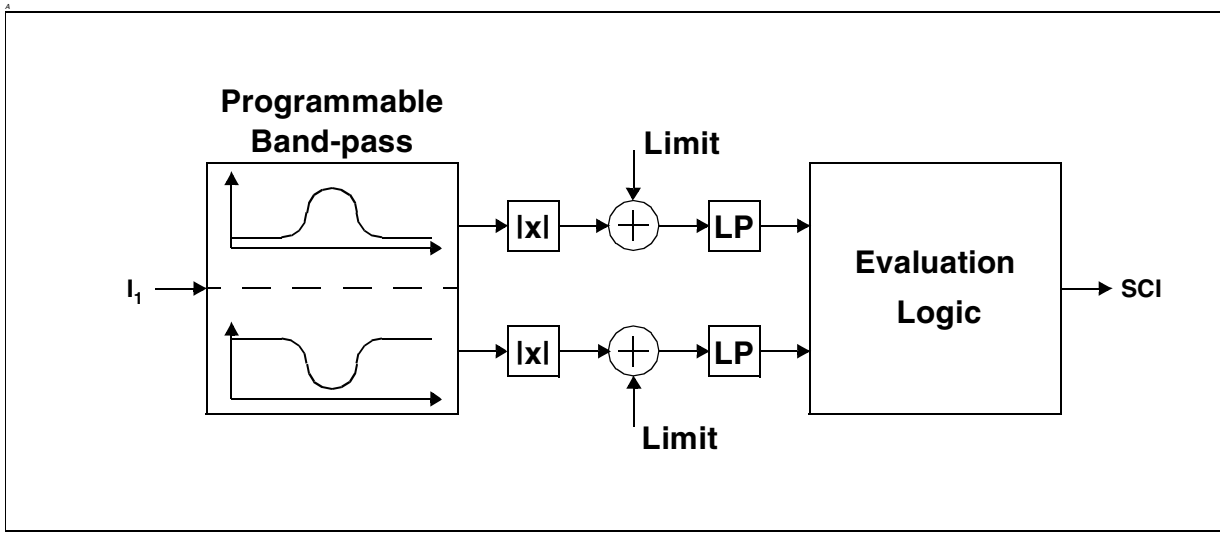


Figure 37 Universal Tone Detector - Block Diagram

Initially, the input signal is filtered by a programmable band-pass (center frequency *CF* and band width *BW*). Both the in-band signal (upper path) and the out-of-band signal are determined (lower path) and the absolute value is calculated. Both signals are furthermore filtered by a limiter and a low-pass. All signal samples (absolute values) below a programmable limit *LIM* are set to zero and all other signal samples are diminished by *LIM*. The purpose of the limiter is to increase noise robustness. After the limiter stages both signals are filtered by a fixed low pass.

The evaluation logic block determines when to set and when to reset the status bit STATUS:UTD.

The status bit will be set if both of the following conditions hold for at least time *TTONE* without breaks exceeding time *TB1*:

1. the in-band signal exceeds a programmable level *LEV*
2. the difference of the in-band and the out-of-band signal exceeds *DELTA*

The status bit will be reset if at least one of these conditions is violated by at least time *TGAP* without breaks exceeding *TB2*.

The times TB1 and TB2 help to reduce the effects of sporadic dropouts.

Example:

TTONE is set to 100 ms and TB1 is set to 4 ms.

The conditions are met for 30ms, then violated for 3ms and then met again for 80 ms. In this case the break of 3ms is ignored, because it does not exceed the allowed break time TB1. Therefore the status bit will be set after 100 ms.

Table 29 summarizes the associated registers.

Table 29 Universal Tone Detector Registers

Register	# of Bits	Name	Comment
UTDCTL	1	EN	UTD detector enable
UTDCTL	5	I1	Input signal selection
UTDBW	15	BW	Bandwidth of band-pass
UTDCF	15	CF	Center frequency of band-pass
UTDLIM	15	LIM	Limiter level
UTDLEV	15	LEV	Minimum signal level (in-band)
UTDDLT	15	DELTA	Minimum difference (in-band, out-of-band)
UTDTMT	8	TTONE	Minimum time to set status bit
UTDTMT	8	TB1	Maximum break time for TTONE
UTDTMG	8	TGAP	Minimum time to reset status bit
UTDTMG	8	TB2	Maximum break time for TGAP

The result is available in the status register (table30).

Table 30 Universal Tone Detector Results

Register	# of Bits	Name	Comment
STATUS	1	UTD	Tone detected

Note: The UTD bit is at the same position as the CPT bit. Therefore the CPT detector and the programmable band-pass must not run at the same time.

2.6 Caller ID Decoder

The caller ID decoder is basically a 1200 baud modem (FSK, demodulation only). The bit stream is formatted by a subsequent UART and the data is available in a data register along with status information (figure 38).

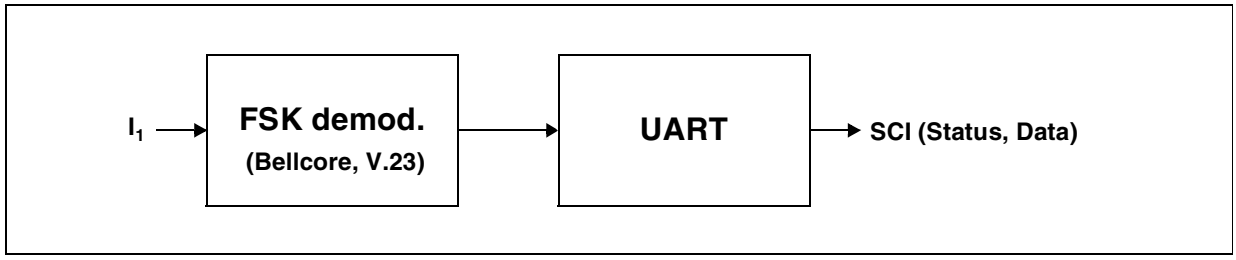


Figure 38 Caller ID Decoder - Block Diagram

The FSK demodulator supports two modes according to table 31. The appropriate mode is detected automatically.

Table 31 Caller ID Decoder Modes

Mode	Mark (Hz)	Space (Hz)	Comment
1	1200	2200	Bellcore
2	1300	2100	V.23

The CID decoder does not interpret the data received. Each byte received is placed into the CIDCTL register (table 33). The status byte of the is updated (table 32).

Table 32 Caller ID Decoder Status

Register	# of Bits	Name	Comment
STATUS	1	CIA	CID byte received
STATUS	1	CD	Carrier Detected

CIA and CD are cleared when the unit is disabled. In addition, CIA is cleared when CIDCTL0 is read.

Table 33 Caller ID Decoder Registers

Register	# of Bits	Name	Comment
CIDCTL0	1	EN	Unit enable
CIDCTL0	1	DOT	Drop out tolerance during mark or seizure sequence
CIDCTL0	1	CM	Compatibility mode
CIDCTL0	5	I1	Input signal selection
CIDCTL0	8	DATA	Last CID data byte received
CIDCTL1	5	NMSS	Number of mark/space sequences necessary for successful detection of carrier.
CIDCTL1	5	NMB	Number of mark bits necessary before space of first byte after carrier detected.
CIDCTL1	6	MIN	Minimum signal level for CID detection.

When the CID unit is enabled, it waits for a programmable number of continuous mark bits (CIDCTL1:NMB). These mark bits may optionally be preceded by a channel seizure signal consisting of a series of alternating space and mark signals. If such a channel

seizure sequence is present it must consist of at least CIDCTL1:NMSS alternating mark and space bits.

Once the programmed number of continuous mark bits has been received the sets the carrier detect bit STATUS:CD.

The interpretation of the data, including message type, length and checksum is completely left to the controller. The CID unit should be disabled as soon as the complete information has been received as it cannot detect the end of the transmission by itself.

There are two alternative Caller ID Decoders. With bit CM cleared, the standard Caller ID Decoder is selected, which is compatible to PSB 2170 version 1.1. The standard Called ID Decoder requires a seizure sequence. With CM set to 1, the improved Caller ID Decoder is selected, which provides a higher twist tolerance, does not require a seizure sequence, and allows to select the drop out tolerance. The drop out tolerance is selected by bit DOT of register CIDCTL0. Then, drop outs during a mark sequence do not necessarily cause that the CID detection looses its carrier sequence, but the received mark sequence can be recognized although there are drop outs. The same holds for a seizure sequence. This behavior meets the Bellcore test specification.

If drop out tolerance is enabled, the six registers CIDMF1 to CIDMF6 have to be programmed prior to use of this feature. Note that these registers are undefined after reset. The registers CIDMF1 to CIDMF6 must contain all possible message formats, which can be transmitted after the mark sequence, and these registers must not contain any other value. For Bellcore for example, the valid message formats are 04_h, 06_h, 80_h and 82_h so that registers CIDMF1 to CIDMF6 may contain 04_h, 06_h, 80_h, 82_h, 82_h and 82_h.

Note: Some caller ID mechanism may require additional external components for DC decoupling. These tasks must be handled by the controller.

Note: The controller is responsible for selecting and storing parts of the CID as needed.

2.7 DTMF Generator

The DTMF generator can generate single or dual tones with programmable frequency and gain. This unit is primarily used to generate the common DTMF tones but can also be used for signalling or other user defined tones. A block diagram is shown in figure 39.

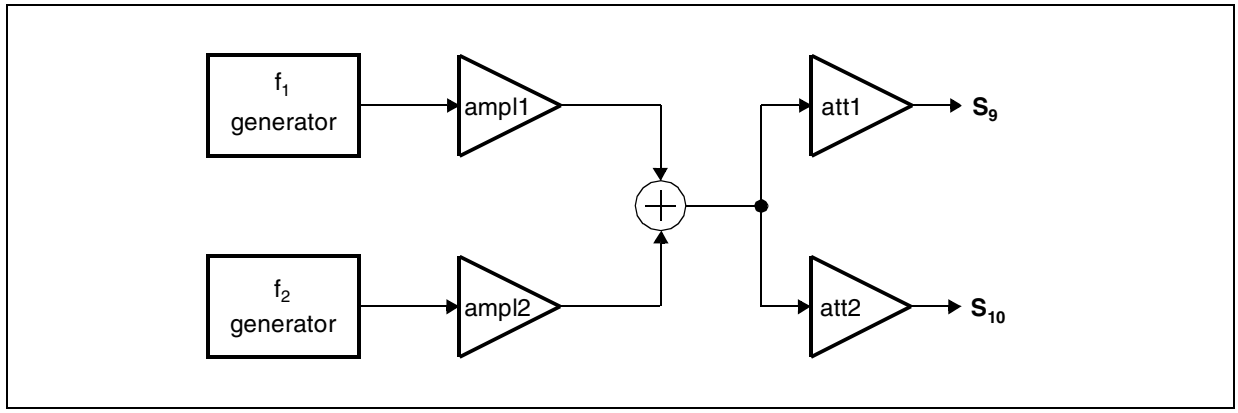


Figure 39 DTMF Generator - Block Diagram

Both generators and amplifiers are identical. There are two modes for programming the generators, cooked mode and raw mode. In cooked mode, DTMF tones are generated by programming a single 4 bit code. In raw mode, the frequency of each generator/ amplifier can be programmed individually by a separate register. The unit has two outputs which provide the same signal but with individually programmable attenuation. Table 34 shows the parameters of this unit.

Table 34 DTMF Generator Registers

Register	# of Bits	Name	Comment
DGCTL	1	EN	Enable for generators
DGCTL	1	MD	Mode (cooked/raw)
DGCTL	4	DTC	DTMF code (cooked mode)
DGF1	15	FRQ1	Frequency of generator 1
DGF2	15	FRQ2	Frequency of generator 2
DGL	7	LEV1	Level of amplifier for generator 1
DGL	7	LEV2	Level of amplifier for generator 2
DGATT	8	ATT1	Attenuation of S_9
DGATT	8	ATT2	Attenuation of S_{10}

Note: DGF1 and DGF2 are undefined when cooked mode is used and must not be written.

2.8 Analog Interface

There are two identical interfaces to the analog side (i.e., the analog fronend described in chapter 4.3) as shown in figure 40. These interfaces must be connected to a double codec like the PSB 4851.

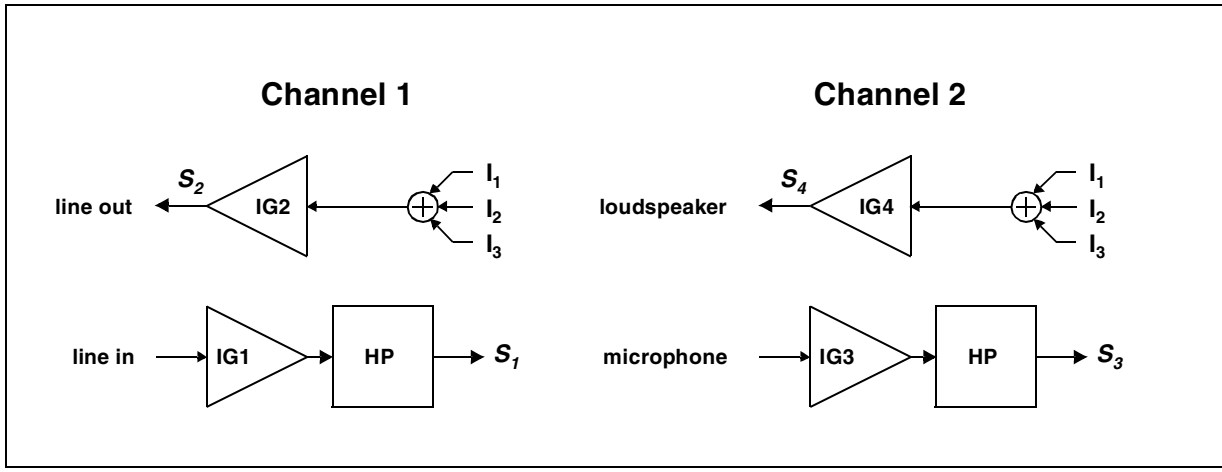


Figure 40 Analog Frontend Interface - Block Diagram

For each signal an amplifier is provided for level adjustment. The ingoing signals can be passed through an optional high-pass (HP) to get rid of any dc part. Furthermore, up to three signals can be mixed in order to generate the outgoing signals (S_2,S_4). Table 35 shows the associated registers.

Table 35 Analog Frontend Interface Registers

Register	# of Bits	Name	Comment
IFG1	16	IG1	Gain for IG1
IFG2	16	IG2	Gain for IG2
IFS1	1	HP	High-pass for S_1
IFS1	5	I1	Input signal 1 for IG2
IFS1	5	I2	Input signal 2 for IG2
IFS1	5	I3	Input signal 3 for IG2
IFG3	16	IG3	Gain for IG3
IFG4	16	IG4	Gain for IG4
IFS2	1	HP	High-pass for S_3
IFS2	5	I1	Input signal 1 for IG4
IFS2	5	I2	Input signal 2 for IG4
IFS2	5	I3	Input signal 3 for IG4

2.9 Digital Interface

There are two almost identical interfaces to the digital side (i.e., the SSDI/IOM®-2 interface described in chapters 4.1 and 4.2) as shown in figure 41. The only difference between these two interfaces is that only channel 1 supports the SSDI mode.

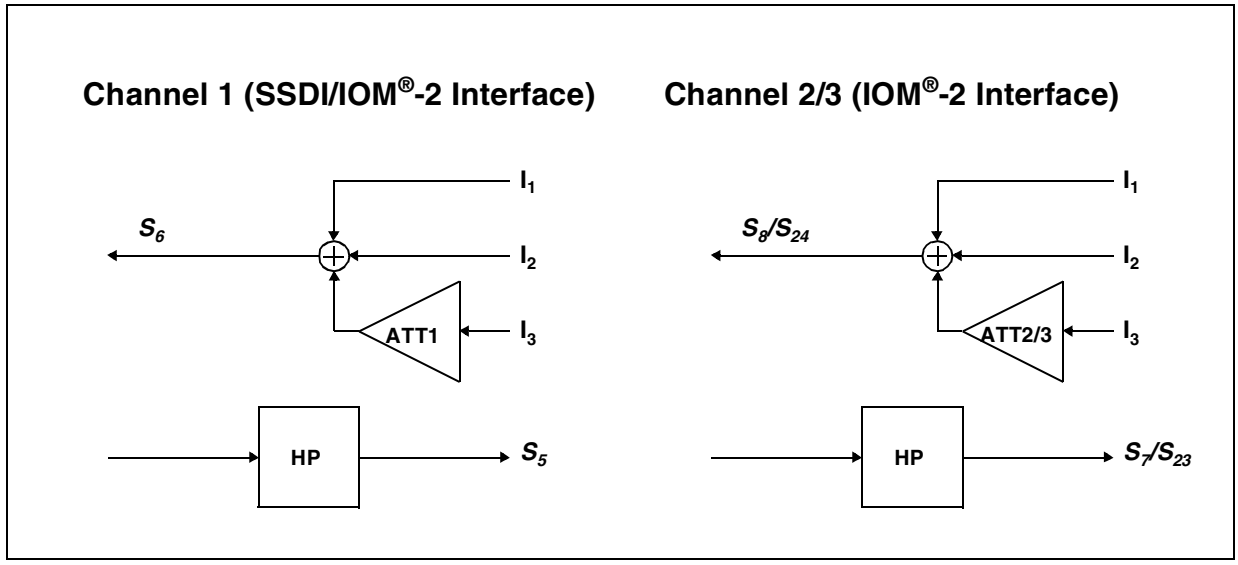


Figure 41 Digital Interface - Block Diagram

Each outgoing signal can be the sum of two signals with no attenuation and one signal with programmable attenuation (ATT). The attenuator can be used for artificial echo loss. Each input can be passed through an optional high-pass (HP) to get rid of any dc part. Channel 2 of the IOM®-2 can be split into two consecutive 8 bit channels with independent data streams (A-law or µ-law). It is therefore possible to use either two 16 bit linear channels, a 16 bit channel and an 8 bit channel, a 16 bit channel and two 8 bit channels or three 8 bit channels.

The associated registers are shown in table 36.

Table 36 Digital Interface Registers

Register	# of Bits	Name	Comment
IFS3	5	I1	Input signal 1 for S_6
IFS3	5	I2	Input signal 2 for S_6
IFS3	5	I3	Input signal 3 for S_6
IFS3	1	HP	High-pass for S_5
IFS4	5	I1	Input signal 1 for S_8
IFS4	5	I2	Input signal 2 for S_8
IFS4	5	I3	Input signal 3 for S_8
IFS4	1	HP	High-pass for S_7
IFS4	5	I1	Input signal 1 for S_{24}
IFS4	5	I2	Input signal 2 for S_{24}

Table 36 Digital Interface Registers

Register	# of Bits	Name	Comment
IFS4	5	I3	Input signal 3 for S_{24}
IFS4	1	HP	High-pass for S_{23}
IFG5	8	ATT1	Attenuation for input signal I3 (Channel 1)
IFG5	8	ATT2	Attenuation for input signal I3 (Channel 2)
IFG5	8	ATT3	Attenuation for input signal I3 (Channel 3)

2.10 Universal Attenuator

The contains an universal attenuator that can be connected to any signal (e.g. for sidetone gain in ISDN applications).

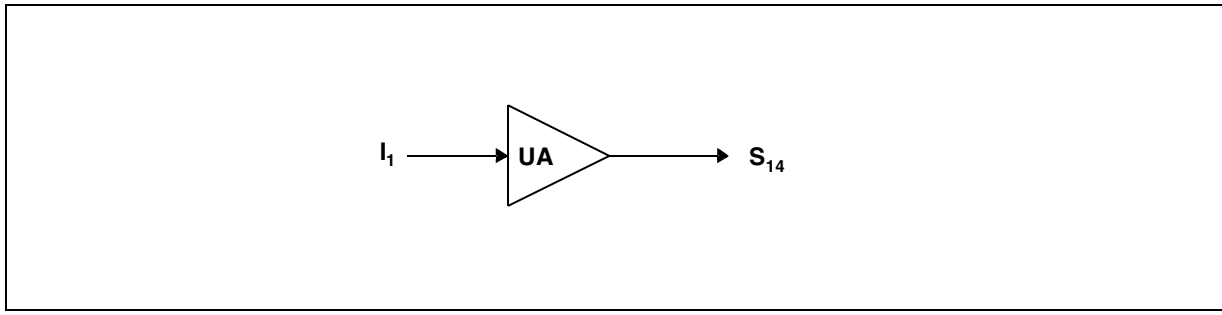


Figure 42 Universal Attenuator - Block Diagram

Table 37 shows the associated register.

Table 37 Universal Attenuator Registers

Register	# of Bits	Name	Comment
UA	8	ATT	Attenuation for UA
UA	5	I1	Input signal for UA

2.11 Automatic Gain Control Unit

In addition to the universal attenuator with programmable but fixed gain the contains an amplifier with automatic gain control (AGC). The AGC is preceded by a signal summation point for two input signals. One of the input signals can be attenuated.

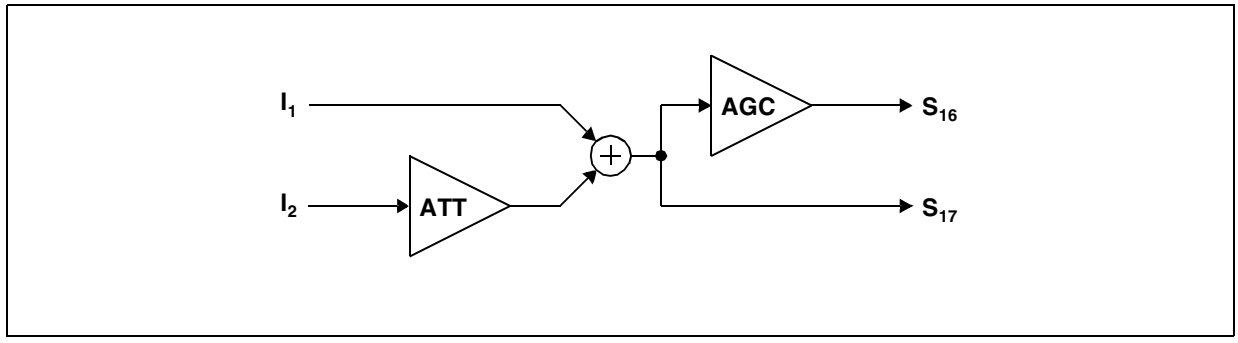


Figure 43 Automatic Gain Control Unit - Block Diagram

The operation of the AGC is similar to AGCX (ACCR) of the speakerphone. The differences are as follows:

- No NOIS parameter
- Separate enable/disable control
- Slightly different coefficient format

Furthermore the AGC contains a comparator that starts and stops the gain regulation. The signal after the summation point (S17) is filtered by a peak detector with time constant DEC for decay. Then the signal is compared to a programmable limit LIM. Regulation takes only place when the filtered signal exceeds the limit.

Table 38 shows the associated registers.

Table 38 Automatic Gain Control Registers

Register	# of Bits	Name	Comment
AGCCTL	1	EN	Enable
AGCCTL	5	I1	Input signal 1 for AGC
AGCCTL	5	I2	Input signal 2 for AGC
AGCATT	15	ATT	Attenuation for I_2
AGC1	8	AG_INIT	Initial AGC gain/attenuation
AGC1	8	COM	Compare level rel. to max. PCM-value
AGC2	8	SPEEDL	Change rate for lower levels
AGC2	8	SPEEDH	Change rate for higher level
AGC3	7	AG_ATT	Attenuation range
AGC3	8	AG_GAIN	Gain range
AGC4	7	DEC	Time constant for decay rate of peak detector
AGC4	8	LIM	Comparator minimal signal level
AGC5	7	LP	AGC low pass time constant

2.12 Noise Reduction Unit

Additionally to the noise reduction block built in the speakerphone, another noise reduction block is available as configurable module. It can be useful for reducing the noise coming in the receive path from the line side.

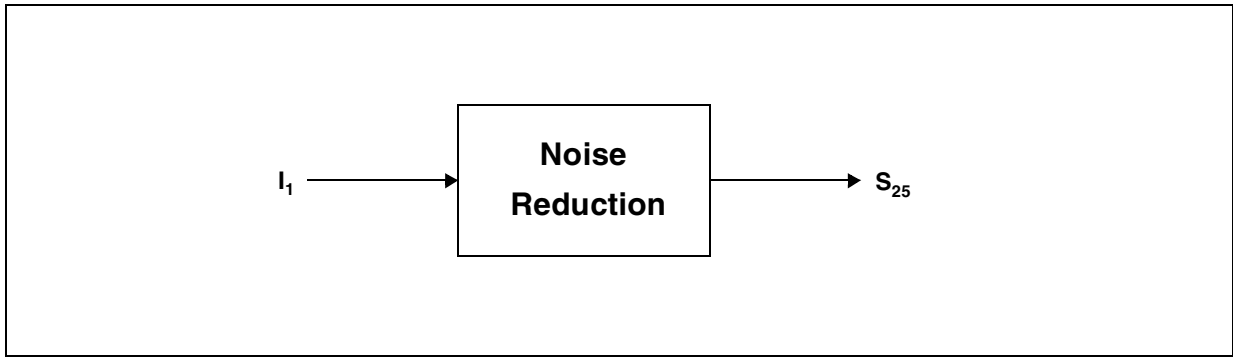


Figure 44 Noise Reduction - Block Diagram

The noise reduction unit attenuates frequencies with a great ratio of the noise energy level to the level of the speach signal. The maximal attenuation of the noise reduction unit can be programmed by the parameter NRATT.

There are some restrictions for the simultaneous selection of the speakerphone. Different trade-offs can be selected with the parameter MD.

Table 39 Noise Reduction Registers

Register	# of Bits	Name	Comment
NRCTL	1	EN	Noise Reduction Unit Enable
NRCTL	2	MD	Select restriction of speakerphone
NRCTL	5	I1	Input signal selection
NRATT	15	NRATT	Maximal attenuation of the noise reduction unit.

2.13 Equalizer

The contains two identical equalizers which can be programmed individually. Each equalizer can be inserted into any signal path. The main application for the equalizer is the correction of the frequency characteristics of the microphone, transducer or loudspeaker.

Each equalizer consists of an IIR filter followed by an FIR filter as shown in figure 45.

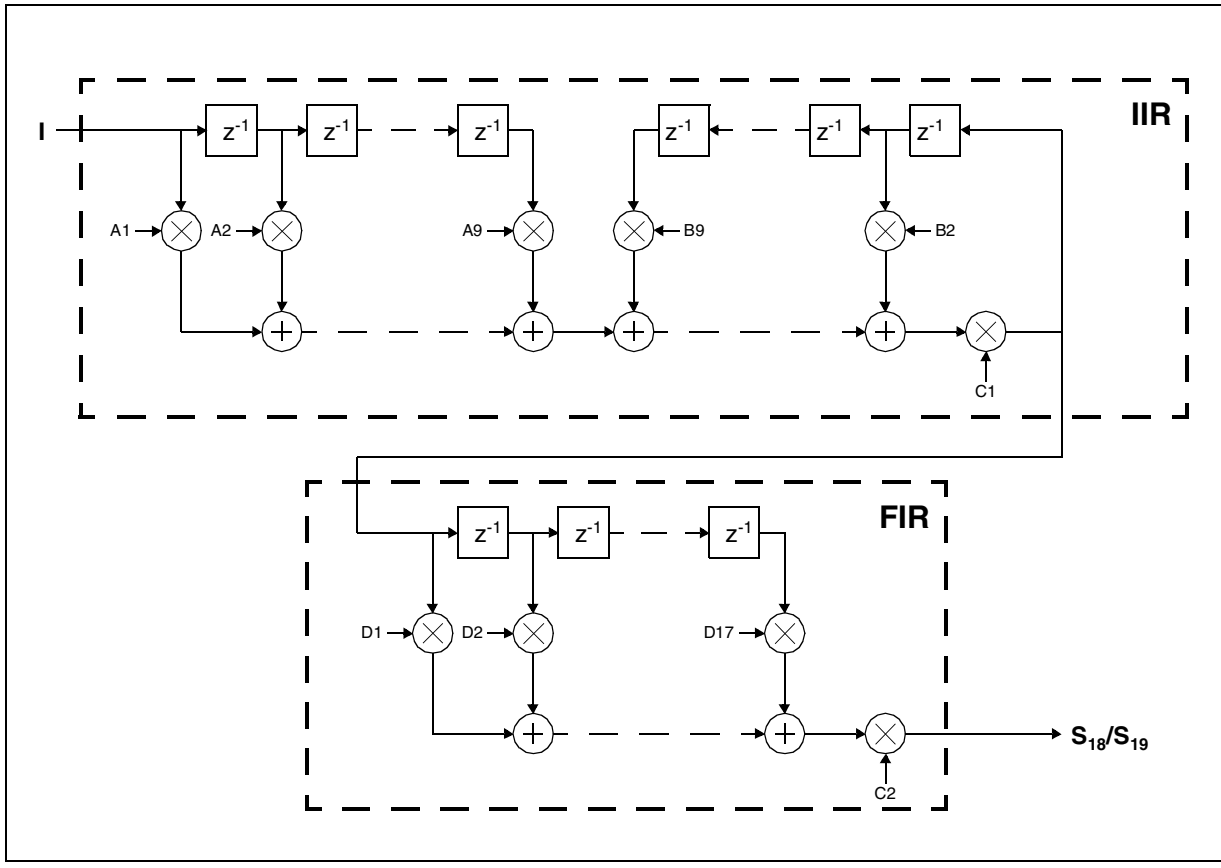


Figure 45 Equalizer - Block Diagram

The coefficients A_1-A_9, B_2-B_9 and C_1 belong to the IIR filter, the coefficients D_1-D_{17} and C_2 belong to the FIR filter. Table 40 shows the registers associated with the first equalizer (S_{18}). The second equalizer (S_{19}) is programmed by the registers FCFCTL2 and FCFCOF2, respectively

Table 40 Equalizer Registers

Register	# of Bits	Name	Comment
FCFCTL1	1	EN	Enable
FCFCTL1	5	I	Input signal for equalizer
FCFCTL1	6	ADR	Filter coefficient address
FCFCOF1	16	V	Filter coefficient data

Due to the multitude of coefficients the PSB 2170 uses an indirect addressing scheme for reading or writing an individual coefficient. The address of the coefficient is given by ADR and the actual value is read or written to register FCFCOF1.

In order to ease programming the automatically increments the address ADR after each access to FCFCOF1.

Note: Any access to an out-of-range address automatically resets FCFCTL1:ADR.

2.14 Tone Generator

The contains a universal tone generator which can be used for tone alerting, call progress tones or other audible feedback tones. Figure 46 shows a block diagram of this unit.

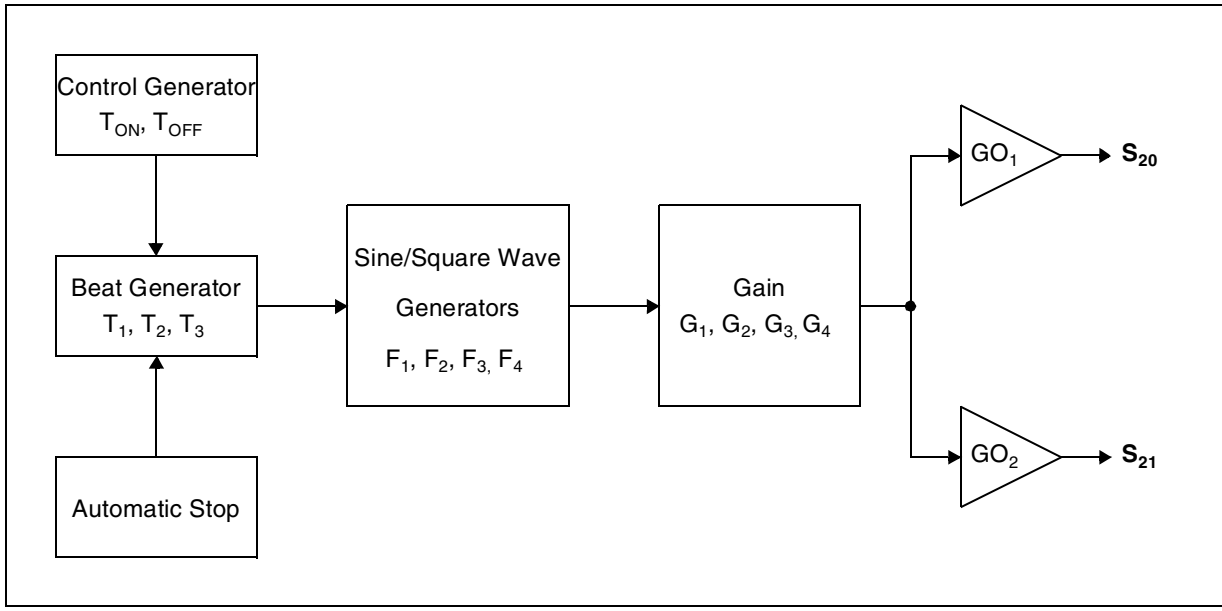


Figure 46 Tone Generator - Block Diagram

The heart of this unit are the four independent sine/square wave generators that can generate individually programmable frequencies (F_1, F_2, F_3, F_4). Each generator has an associated amplifier (G_1, G_2, G_3, G_4). The dynamic behavior of the tone generator is controlled by the beat generator.

If the beat generator is enabled, then the output is either a three tone cadence or a two tone caddence as shown in figure 47.

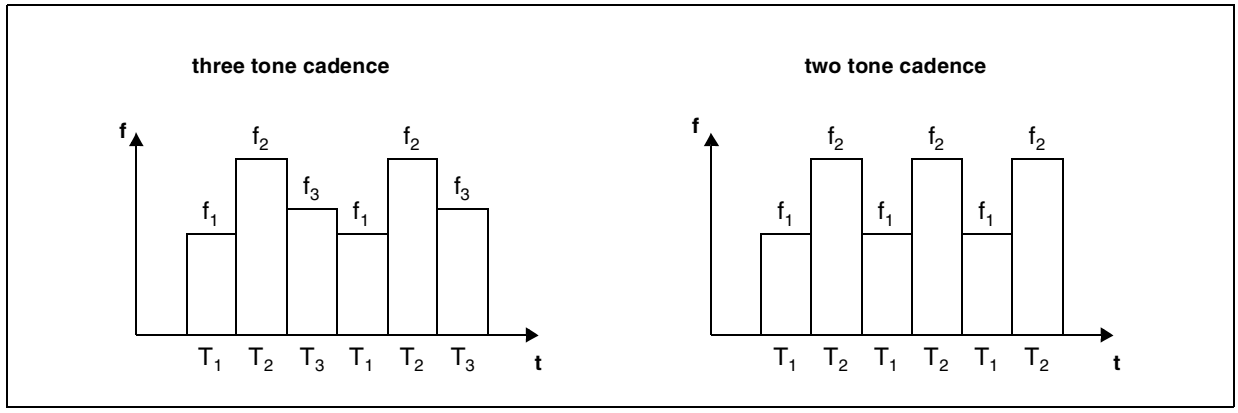


Figure 47 Tone Generator - Tone Sequences

The duration of each frequency is defined by T_1, T_2 and T_3. For each timeslot either the associated frequency can be generated or a frequency pair (table 41).

Table 41 Tone Generator Modes

Timeslot	Option 1	Option 2
T_1	F_1	F_1+F_4
T_2	F_2	F_2+F_4
T_3	F_3	F_3+F_4

If the beat generator is disabled, then the output is a continuous signal of either F_1, F_2, F_1+F_4, F_2+F_4 or silence.

The control generator is used to enable the beat generator (during T_{ON}) and disable it during T_{OFF}. With the automatic stop feature, the cadence generation of the beat generator stops not immediately but after the end of a cadence (either T_2 or T_3). This avoids unpleasant sounds when stopping the tone generator unit.

Table 42 shows the registers associated with the tone and ringing generator.

Table 42 Tone Generator Registers

Register	# of Bits	Name	Comment
STATUS	1	TG	Status bit (Tone Generator on/off)
TGCTL	2	CGM	Control generator mode
TGCTL	1	DT	Dual tone enable (F4 on/off)
TGCTL	2	BGM	Beat generator mode (F1, F2, F1/F2 or F1/F2/F3)
TGCTL	1	SM	Stop mode (immediate or automatic)
TGCTL	1	WF	Waveform (sine or square)

Table 42 Tone Generator Registers

Register	# of Bits	Name	Comment
TGTON	16		T_{ON}
TGTOFF	16		T_{OFF}
TGT1	16		T_1
TGT2	16		T_2
TGT3	16		T_3
TGF1	15		F_1
TGF2	15		F_2
TGF3	15		F_3
TGF4	15		F_4
TGG1	15		G_1
TGG2	15		G_2
TGG3	15		G_3
TGG4	15		G_4
TGGO1	15		GO_1
TGGO2	15		GO_2

This unit has two outputs (S_{20} and S_{21}). The signal level of these outputs can be programmed individually by the preceding gain stages (GO_1 and GO_2).

2.15 Peak Detector

The peak detector (figure 48) provides an easy means to verify the minimum or maximum signal level of any signal S_i within the . It is, however, usually not used in normal operation. The peak detector stores either the maximum or the minimum signal value of the observed signal I_1 in the register PDDATA since the last read access to this register. Therefore it is not only possible to determine the absolute level of the signal but it can also be checked whether a DC offset is present. This can be done by first scanning for the maximum and then for the minimum value. If the minimum value is not (approximately) the negated maximum value then a DC offset is present. The peak detector should be disabled if not needed.

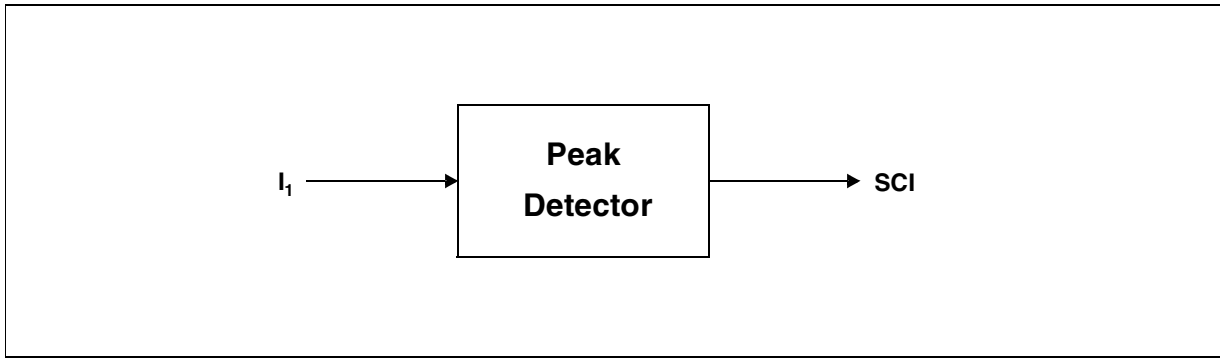


Figure 48 Peak Detector - Block Diagram

The register PDDATA gives the maximum or minimum integer depending on the mode selected by bit MM. As an example it may be assumed that the detection of the maximum is selected. Then with enabling the detector and with each read access to register PDDATA, PDDATA is set to the smallest possible value, which is the negative maximum integer. With each new maximum detected on signal I1, this maximum is provided by PDDATA.

Table 43 Peak Detector Registers

Register	# of Bits	Name	Comment
PDCTL	1	EN	Peak Detector Enable
PDCTL	1	MM	Minimum/Maximum selection
PDCTL	5	I1	Input signal selection
PDDATA	16		Min/Max signal value since last read access

3 Miscellaneous

3.1 Reset and Power Down Mode

The PSB 2170 can be in either reset mode, power down mode or active mode. During reset the PSB 2170 clears the hardware configuration registers and stops both internal and external activity. With the first access to a read/write register the PSB 2170 enters active mode. In this mode the main oscillator is running and normal operation takes place. The PSB 2170 can be brought to power down mode by setting the power down bit (PD).

Table 44 Power Down Bit

Register	# of Bits	Name	Comment
CCTL	1	PD	power down mode

In power down mode the main oscillator is stopped. The PSB 2170 enters active mode again upon an access to a read/write register. Figure 49 shows a state chart of the modes of the PSB 2170.

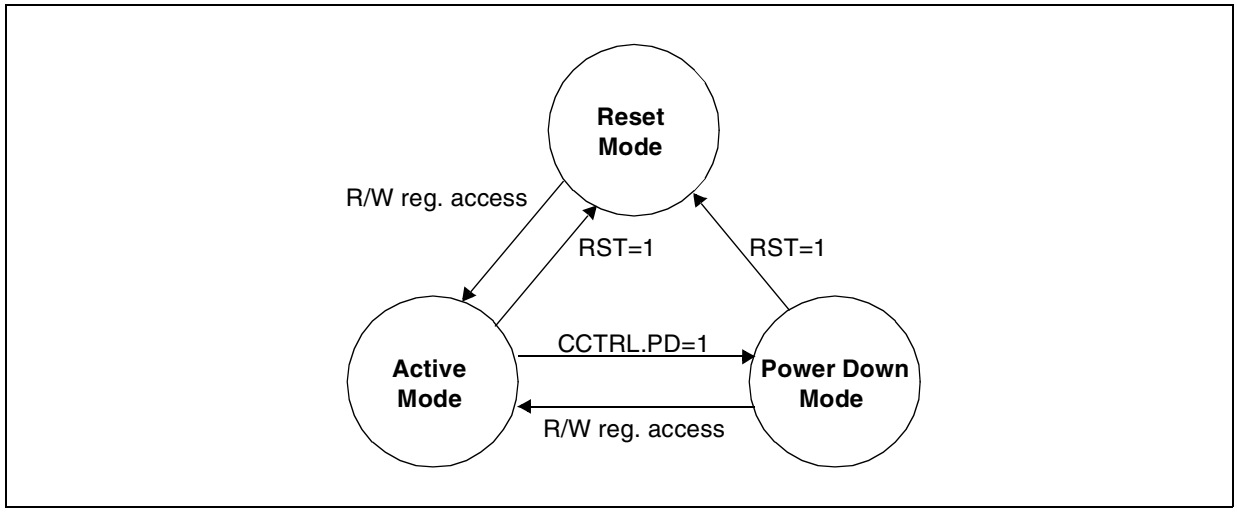


Figure 49 Operation Modes - State Chart

3.2 SPS Control Register

The two SPS outputs (SPS_0, SPS_1) can be used either as general purpose outputs, speakerphone status outputs or as status register outputs. This is programmed with the bits MODE. Table 45 shows the associated register.

Table 45 SPS Register

SPSCTL	1	SP0	Output Value of SPS_0
SPSCTL	1	SP1	Output Value of SPS_1
SPSCTL	3	MODE	Mode of Operation
SPSCTL	4	POS	Position for status register window

When used as status register outputs, the status register bit at position POS appears at SPS_0 and the bit at position POS+1 appears at SPS_1. This mode of operation can be used for debugging purposes or direct polling of status register bits. The RDY bit cannot be observed via SP0 or SP1.

3.3 Interrupt

The can generate an interrupt to inform the host of an update of the STATUS register according to table 46. An interrupt mask register (INTM) can be used to disable or enable the interrupting capability of each bit of the STATUS register individually.

Table 46 Interrupt Source Summary

STATUS (old)	STATUS (new)	Set by	Reset by
RDY=0	RDY=1	Command completed	Command issued
CIA=0	CIA=1	New Caller ID byte available	CIDCTL0 read or EN=0[1)]
CD=0	CD=1	Carrier detected	Carrier lost or EN=0
CD=1	CD=0	Carrier lost or EN=0	Carrier detected
TG=1	TG=0	Tone generator active	Tone sequence finished or EN=0
DTV=0	DTV=1	DTMF tone detected	DTMF tone lost or EN=0
DTV=1	DTV=0	DTMF tone lost or EN=0	DTMF tone detected
ATV=0	ATV=1	Alert tone detected	Alert tone lost or EN=0
ATV=1	ATV=0	Alert tone lost or EN=0	Alert tone detected
CPT/UTD=0	CPT/UTD=1	CPT or UT detected	CPT or UT lost
CPT/UTD=1	CPT/UTD=0	CPT or UT lost	CPT or UT detected
PPI=0	PPI=1	Event at APP input pin detected	Register DHOLD read
ABT=0	ABT=1	Exception (non-maskable)	Write to REV Register

[1)] EN=0 denotes unit disable

An interrupt is internally generated if any combination of these events occurs and the interrupt is not masked. The interrupts are issued immedeately after the status register update. The status register update for the event set bit CIA, CD, DTV, ATV, APT, UTD, PPI or ABT is performed immediately after the event occurs that causes the bit to be set. For the event clear bit CD, DTV, ATV, CPT or UTD, the status register update is performed with the next update of the RDY bit, i.e., up to 125 us after the event occurs that causes the bit to be set. For the event clear bit TG, the status register update is performed 125 us after the update of the RDY bit as the latest.

This internal interrupt is cleared only when the host executes the *Data Read Access with Interrupt Acknowledge* command. In this case, the internal interrupt is cleared when the first bit of the STATUS register is output. If a new event occurs while the host reads the status register, the status register is updated *after* the current access is terminated and a new interrupt is internally generated immediately after the access has ended.

3.4 Abort

If the detects a corrupted configuration (e.g. due to a transient loss of power) it stops operation and initializes all read/write registers to their reset state. The discards all commands with the exception of a write command to the revision register while ABT is set. Only after the write command to the revision register (with any value) the ABT bit is reset and a reinitialization can take place.

3.5 Revision Register

The contains a revision register. This register is read only and does not influence operation in any way. A write to the revision register clears the ABT bit of the STATUS register but does not alter the content of the revision register.

3.6 Hardware Configuration

The can be adapted to various external hardware configurations by two special registers: HWCONFIG0 and HWCONFIG1. These registers are written once during initialization and must not be changed while the is in active mode.

3.6.1 Frame Synchronization

The locks itself to either an externally supplied frame sync signal or generates the frame sync signal itself. This internal reference frame sync signal is called master frame sync (MFSC). Table 47 shows how AFECLK and MFSC are derived by the . The bits ACT and MFS are contained in the hardware configuration registers. The bit MFS controls whether the frame sync is taken from external or generated internally. The bit ACT enables the clock tracking and is explained in the sequel section.

Table 47 Frame Synchronization Selection

ACT	MFS	AFECLK	MFSC	Application
0	0	XTAL	AFEFSC	Analog featurephone
0	1	-	FSC	ISDN stand-alone
1	1	XTAL	FSC	DECT

3.6.2 Clock Tracking

The can adjust AFECLK and AFEFSC dynamically to a slightly varying FSC if AFECLK and AFEFSC are derived from the main oscillator (XTAL). This mode requires that both AFEFSC and FSC are nominally running at the same frequency (8 kHz). It is enabled with the bit ACT in the hardware configuration registers.

This feature is especially useful when the FSC signal is not derived from the same clock source as AFECLK (ISDN application).

3.6.3 AFE Clock Source

The can also derive its AFECLK from an externally provided clock CLK. This can be enabled with the bit ACS in the hardware configuration registers. The external clock CLK is expected to run at 13.824 MHz.

3.6.4 AFE Used for Clock and Frame Sync Gereration

If the AFE is not used but a clock and frame sync is required, the can generate such a clock and frame sync at the AFE interface. To use this feature, the AFE must be disabled and the HWCONF3 register (bits CM1 and CM0) can be used for configuration.

3.7 Restrictions and Mutual Dependencies of Modules

There are some restrictions concerning the modules that can be enabled at the same time (table 48). A checked cell indicates that the two modules (defined by the row and the column of the cell) must not be enabled at the same time.

Table 48 Dependencies of Modules

	Subband (normal)	Subband (ISDN)	Subband (enhanced)	Subband (reduced)	Fullband mode one	Fullband mode two (< 542 taps)	Fullband mode two (> = 542 taps)	Comfort Noise	Noise Adaptation	DTMF Detector	Caller ID (standard)	Caller ID (improved)	Alert Tone Detector	CPT Detector	Universal Tone Detector	Line Echo Canceller	Equalizer, DTMF, Tone
Subband (normal)		X	X	X	X	X	X	X									
Subband (ISDN)	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	
Subband (enhanced)	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X
Subband (reduced)	X	X	X		X	X	X			1)							
FB one	X	X	X	X													
FB two (< 542 taps)	X	X	X	X													
FB two (>= 542 taps)	X	X	X	X				X									
Comfort Noise	X	X	X				X			X	X	X	X	X	X	X	
Noise Adaptation		X	X								X	X		X	X		
DTMF Detector		X	X	1)				X				X					
Caller ID (standard)		X	X					X	X				X				
Caller ID (improved)		X	X					X	X	X			X				
Alert Tone Detector		X	X					X			X	X					
CPT Detector		X	X					X	X						X		
UT Detector		X	X					X	X					X			
Line Echo Canceller		X	X					X									
Equalizer 1/2, DTMF/Tone Generator			X														

1) Modules can be enabled at the same time. However, deactivation requires proper sequence: First the echo cancellation unit must be disabled, then the DTMF detector.

Some incompatible modules share the same internal memory space. If this is for example the case for the incompatible modules A and B, and both modules are going to be used at different times, then the following scenario appears: Module A has to be programmed prior to use. After a while, it is disabled, module B is programed and module B is enabled. At a later time, module B is disabled. Before module A is enabled, the

parameters of module A must be reprogrammed. This reprograming is necessary for all combination listed in table 49.

Table 49 Reprogram parameters

After use of this	The parameter of these must be reprogrammed
AEC fullband mode two which number of taps > 645	DTMF decoder, caller ID decoder, alert tone detector, CPT detector, universal tone detector and line echo canceller
AEC subband mode "ISDN"	DTMF decoder, caller ID decoder, alert tone detector, CPT detector, universal tone detector and line echo canceller
AEC subband mode "Enhanced"	DTMF decoder, caller ID decoder, alert tone detector, CPT detector, universal tone detector, line echo canceller, equalizers, tone detectors and tone generator
Comfort noise	DTMF decoder, caller ID decoder, alert tone detector, CPT detector, universal tone detector and line echo canceller
Free noise reduction module with NRCTL:MD=10	DTMF decoder, caller ID decoder, alert tone detector, CPT detector, universal tone detector and line echo canceller
CPT detector	Universal tone detector
DTMF detector	Registers CIDMF1 to CIDMF6 of CID decoder (improved)

For the fullband mode two of the echo cancellation unit, a detailed list of the maximal FIR length under certain restriction can be found in chapter 2.1.1.1.

The freely configurable noise reduction unit (chapter 2.12) has some restrictions not stated in table 48. A detailed description of the restrictions is provided with the register description of register NRCTL.

A further restriction may occur because of the resource costs of the simultaneously applied modules. Each module currently in use takes up some resources. The percentage a module needs from the totally available resources is listed in table 50. The sum of resources all applied modules must never exceed 100. The amounts listed on table 50 are valid for 34.560 MHz operating frequency. If the PSB 2170 runs at a higher or lower frequency, the resource costs decrease or increase accordingly.

Thus, it may be necessary to restrict the length of the FIR filter of the echo cancellation unit if several other units are operating at the same time.

Table 50 Module Weights

Module	Weight	Comment
CPT Detector	5.03	
Caller ID Decoder	3.73 / 9.75	CM = 0 / CM = 1
Alert Tone Detector	2.45 / 3.15	off hook / on hook
DTMF Detector	6.05	
UT Detector	3.24	
DTMF Generator	1.92	
Equalizer	2.50	
Speakerphone	10.93	
AGCX	1.92	
AGCR	1.94	
Acoustic Echo Cancellation Fullband mode one	32.25 / 41.90 / 51.55 / 61.20 / 70.86	256 taps / 384 taps / 512 taps / 640 taps / 768 taps FIR length.
Acoustic Echo Cancellation Fullband mode two	40.03 / 42.99 / 45.96 / 48.92 / 51.88	256 taps / 384 taps / 512 taps / 640 taps / 768 taps FIR length. Adaption window: 256 taps
Acoustic Echo Cancellation Fullband mode two	25.22	FIR length: 128 taps. Adaption window: 128 taps
Noise Reduction of FB AEC	5.03	
Acoustic Echo Cancellation Subband mode (incl. NR)	32.19 / 33.88 / 35.17 / 37.93 / 39.24	Mode: NRN / reduced / normal / ISDN / enhanced
Noise Reduction Module	7.70	
Noise Controlled Adaption	5.07	
Comfort Noise	7.45	
Line Echo Cancellation	11.50 / 13.02	normal mode / superior mode
	21.60 / 17.04	extended mode, SP = 1/ SP = 0
Universal Attenuator	0.16	
Digital Interface	1.46	channel 1 or SSDI
	1.46 / 3.03	channel 2 / channel 2+3
Analog Interface	2.11	
Clock Tracking	0.53	
Miscellaneous	7.70	always active

4 Interfaces

This section describes the interfaces of the . The supports both an IOM®-2 interface with single and double clock mode and a strobed serial data interface (SSDI). However, these two interfaces cannot be used simultaneously as they share some pins. Both interfaces are for data transfer only and cannot be used for programming the . The is slave and the frame synchronization as well as the data clock are inputs. Table 51 lists the features of the two alternative interfaces.

Table 51 SSDI vs. IOM®-2 Interface

	IOM®-2	SSDI
Signals	4	6
Channels (bidirectional)	3	1
Code	linear PCM (16 bit), A-law, µ-law (8 bit)	linear PCM (16 bit)
Synchronization within frame	by timeslot (programmable)	by signal (DXST, DRST)

4.1 IOM®-2 Interface

The data stream is partitioned into packets called frames. Each frame is divided into a fixed number of timeslots. Each timeslot is used to transfer 8 bits. Figure 50 shows a commonly used terminal mode (three channels ch_0, ch_1 and ch_2 with four timeslots each). The first timeslot (in figure 50: B1) is denoted by number 0, the second one (B2) by 1 and so on.

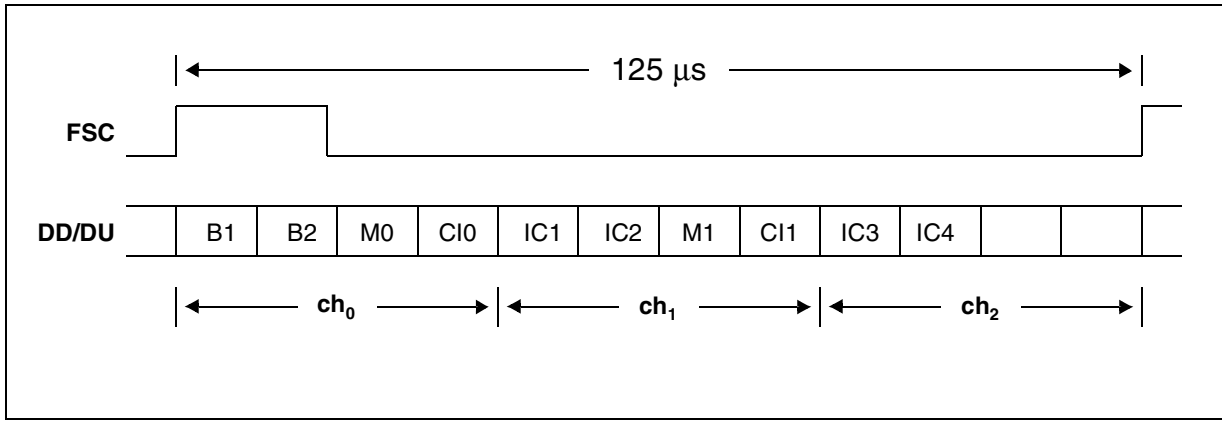


Figure 50 IOM®-2 Interface - Frame Structure

The signal FSC is used to indicate the start of a frame. Figure 51 shows as an example two valid FSC-signals (FSC, FSC*) which both indicate the same clock cycle as the first clock cycle of a new frame (T_1).

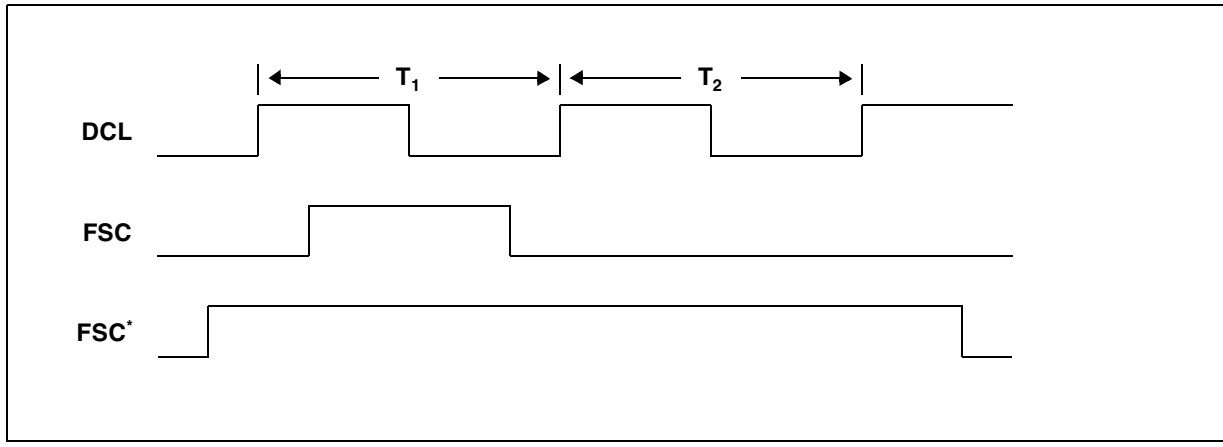


Figure 51 SSDI/IOM®-2 Interface - Frame Start

The supports both single clock mode and double clock mode. In single clock mode, the bit rate is equal to the clock rate. Bits are shifted out with the rising edge of DCL and sampled at the falling edge. In double clock mode, the clock runs at twice the bit rate. Therefore for each bit there are two clock cycles. Bits are shifted out with the rising edge of the first clock cycle and sampled with the falling edge of the second clock cycle. Figure 52 shows the timing for single clock mode and figure 53 shows the timing for double clock mode.

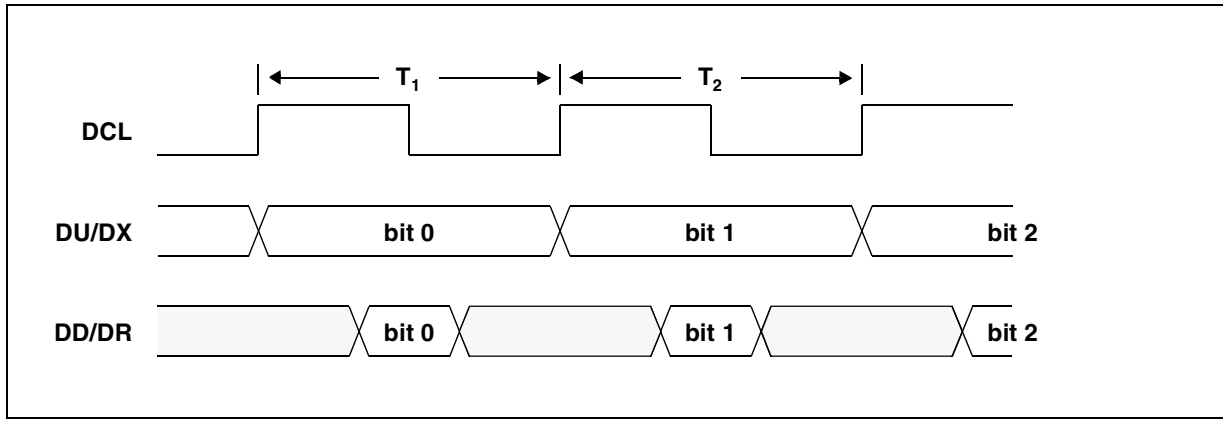


Figure 52 IOM®-2 Interface - Single Clock Mode

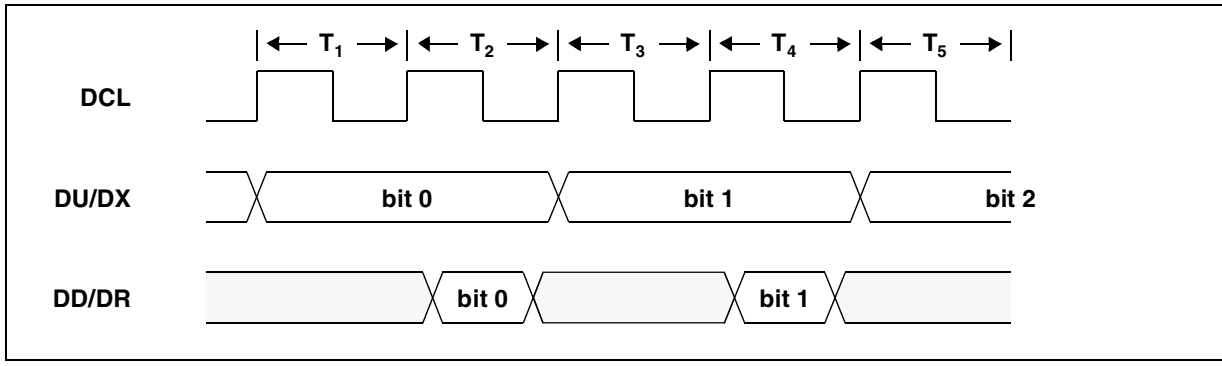


Figure 53 IOM®-2 Interface - Double Clock Mode

The supports up to three channels simultaneously for data transfer. If only two channels are used, then both the coding (PCM A-law, PCM µ-law or linear) and the data direction (DD/DU assignment for transmit/receive) can be programmed individually. The PSB 2170 supports a third channel by simply splitting the second 16 bit channel into two 8 bit channels.Therefore the following restrictions occur for channel 2 and 3 in this case:

1. Channel two as well as three must use PCM coding (both either A-law or µ-law)
2. Channel three is on an even timeslot
3. Channel two is on the following odd timeslot

To enabled the channel splitting, bit SDCHN2:CS must be set and bit SDCHN2:PCM cleared. The selection of bit SDCHN2:PCD holds then for both channels.

Table 52 shows the registers used for configuration of the IOM®-2 interface.

Table 52 IOM®-2 Interface Registers

Register	# of Bits	Name	Comment
SDCONF	1	EN	Interface enable
SDCONF	1	DCL	Selection of clock mode (double/single clock)
SDCONF	6	NTS	Number of timeslots within frame
SDCHN1	1	EN	Channel 1 enable
SDCHN1	6	TS	First timeslot (channel 1)
SDCHN1	1	DD	Data Direction (channel 1)
SDCHN1	1	PCM	8 bit code or 16 bit linear PCM (channel 1)
SDCHN1	1	PCD	8 bit code (A-law or µ-law, channel 1)
SDCHN2	1	EN	Channel 2 enable
SDCHN2	1	CS	Channel 2 split (into two contiguous 8 bit channels)
SDCHN2	6	TS	First timeslot (channel 2)
SDCHN2	1	DD	Data Direction (channel 2)

Table 52 IOM®-2 Interface Registers

Register	# of Bits	Name	Comment
SDCHN2	1	PCM	8 bit code or 16 bit linear PCM (channel 2)
SDCHN2	1	PCD	8 bit code (A-law or µ-law, channel 2)

In A-law or µ-law mode, only 8 bits are transferred and therefore only one timeslot is needed for a channel. In linear mode, 16 bits are needed for a single channel. In this mode, two consecutive timeslots are used for data transfer. Bits 8 to 15 are transferred within the first timeslot and bits 0 to 7 are transferred within the next timeslot. The first timeslot must have an even number. Figure 54 shows as an example a single channel in linear mode occupying timeslots 2 and 3. Each frame consists of six timeslots and single clock mode is used.

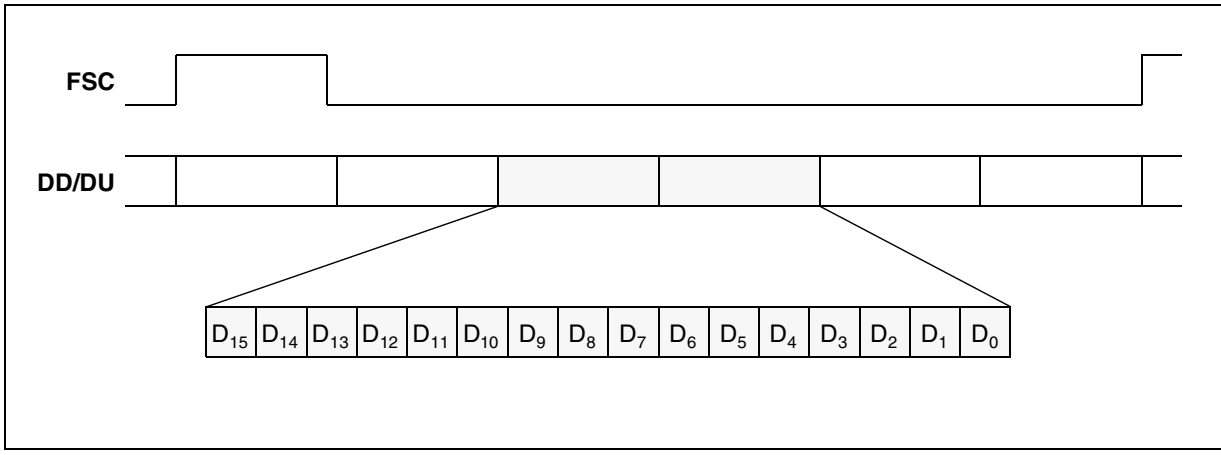


Figure 54 IOM®-2 Interface - Channel Structure

At this rate the data is shifted out with the rising edge of the clock and sampled at the falling edge. The data clock runs at 384 kHz (six timeslots with 8 bit each within 125 µs).

4.2 SSDI Interface

The SSDI interface is intended for seamless connection to low-cost burst mode controllers (e.g. PMB 27251) and supports a single channel in each direction. The data stream is partitioned into frames. Within each frame one 16 bit value can be sent and received by the PSB 2170. The start of a frame is indicated by the rising edge of FSC. Data is always latched at the falling edge of DCL and output at the rising edge of DCL.

The SSDI transmitter and receiver are operating independently of each other except that both use the same FSC and DCL signal.

4.2.1 SSDI Interface - Transmitter

The PSB 2170 indicates outgoing data (on signal DX) by activating DXST for 16 clocks. The signal DXST is activated with the same rising edge of DCL that is used to send the first bit (Bit 15) of the data. DXST is deactivated with the first rising edge of DCL after the last bit has been transferred. The PSB 2170 drives the signal DX only when DXST is activated. Figure 55 shows the timing for the transmitter.

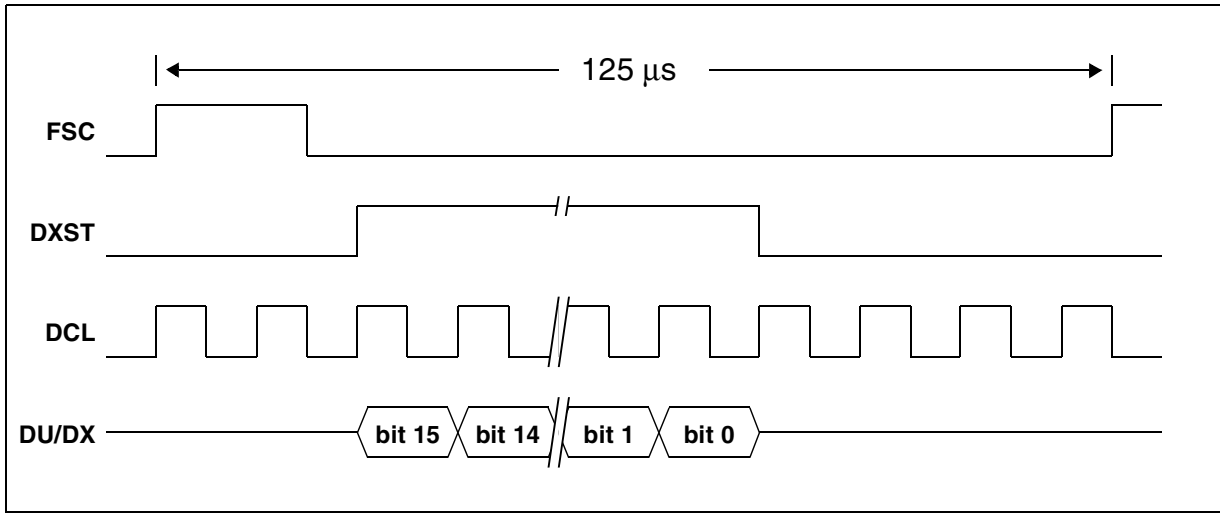


Figure 55 SSDI Interface - Transmitter Timing

4.2.2 SSDI Interface - Receiver

Valid data is indicated by an active DRST pulse. Each DRST pulse must last for exactly 16 DCL clocks. As there may be more than one DRST puls within a single frame the PSB 2170 can be programmed with the parameter NAS to listen to the n-th pulse with n ranging from 1 to 16. In order to detect the first pulse properly, DRST must not be active at the rising edge of FSC. In figure 57 the PSB 2170 is listening to the third DRST pulse (n=3).

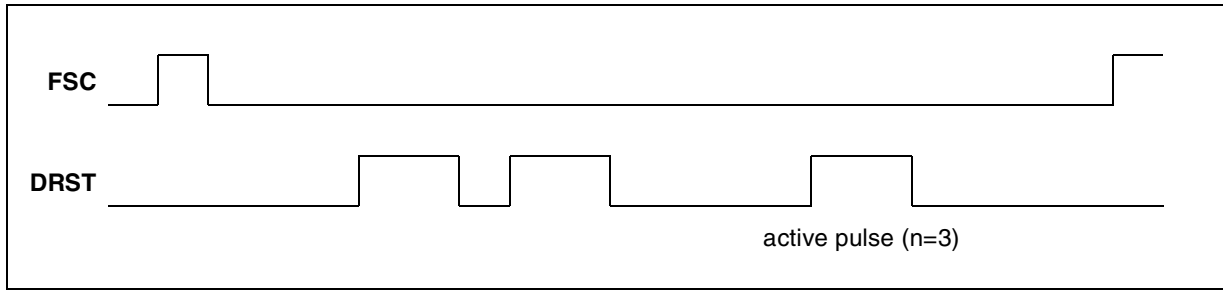


Figure 56 SSDI Interface - Active Pulse Selection

Figure 57 shows the timing for the SSDI receiver.

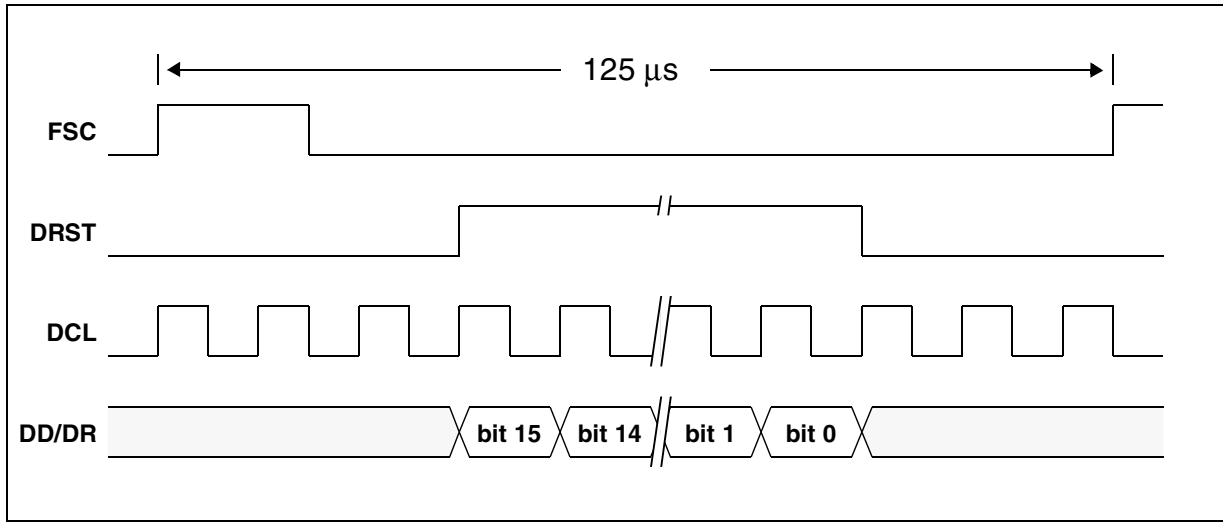


Figure 57 SSDI Interface - Receiver Timing

Table 53 shows the registers used for configuration of the SSDI interface.

Table 53 SSDI Interface Register

Register	# of Bits	Name	Comment
SDCHN1	4	NAS	Number of active DRST strobe

4.3 Analog Front End Interface

The uses a four wire interface similar to the IOM®-2 interface to exchange information with the analog front end (PSB 4851). The main difference is that all timeslots and the channel assignments are fixed as shown in figure 58. The is master of this interface and provides AFEFS as well as AFECLK.

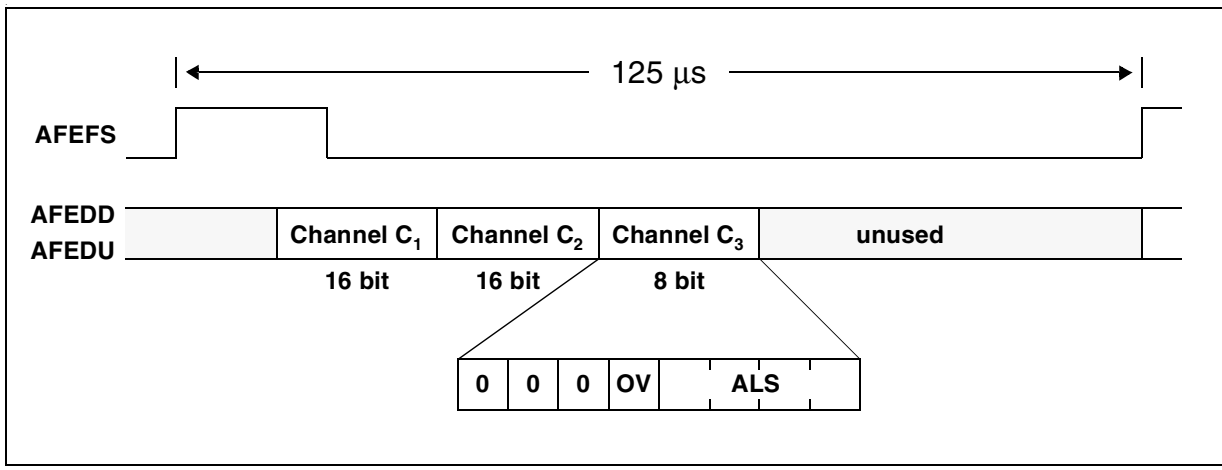


Figure 58 Analog Front End Interface - Frame Structure

Voice data is transferred in 16 bit linear coding in two bidirectional channels C_1 and C_2. An auxiliary channel C_3 is used to transfer the current setting of the loudspeaker amplifier ALS to the . The remaining bits are fixed to zero. In the other direction C_3 transfers an override value for ALS from the to the PSB 4851. An additional override bit OV determines if the currently transmitted value should override the AOAR:LSC[1)] setting. The AOAR:LSC setting is not affected by C_3:ALS override. Table 54 shows the source control of the gain for the ALS amplifier.

Table 54 Control of ALS Amplifier

AOPR:OVRE	C_3:OV	Gain of ALS amplifier
0	-	AOAR:LSC
1	0	AOAR:LSC
1	1	C_3:ALS

Furthermore the AFE interface can be enabled or disabled according to table 55.

Table 55 Analog Front End Interface Register

Register	# of Bits	Name	Comment
AFECTL	1	EN	Interface enable

1) See specification of PSB 4851

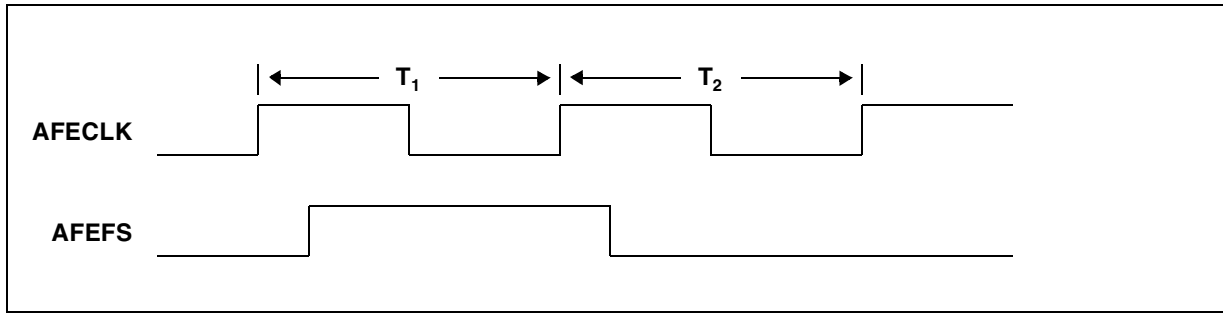


Figure 59 Analog Front End Interface - Frame Start

Figure 59 shows the synchronization of a frame by AFEFS. The first clock of a new frame (T_1) is indicated by AFEFS switching from low to high before the falling edge of T_1. AFEFS may remain high during subsequent cycles up to T_{32}.

Please see also chapter 3.6.2 for additional information on the frame synchronization.

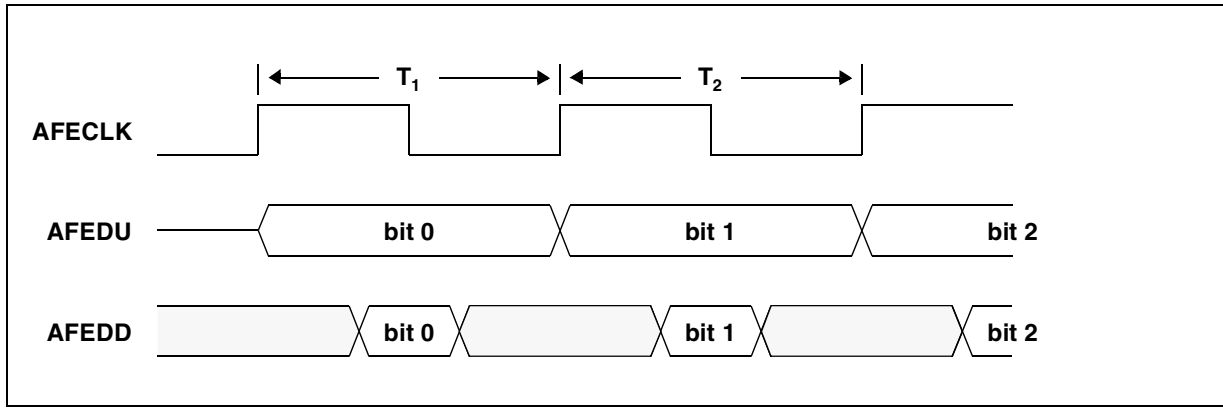


Figure 60 Analog Front End Interface - Data Transfer

The data is shifted out with the rising edge of AFECLK and sampled at the falling edge of AFECLK (figure 60). If AOPR:OVRE is not set, the channel C_3 is not used by the PSB 4851. All values (C_1, C_2, C_3:ALS) are transferred MSB first. The data clock (AFECLK) rate is fixed at 6.912 MHz. Table 56 shows the clock cycles used for the three channels.

Table 56 Analog Front End Interface Clock Cycles

Clock Cycles	AFEDD (driven by)	AFEDU (driven by PSB 4851)
T_1-T_{16}	C_1 data	C_1 data
T_{17}-T_{32}	C_2 data	C_2 data
T_{33}-T_{40}	C_3 data	C_3 data
T_{41}-T_{864}	0	tristate

4.4 Serial Control Interface

The serial control interface (SCI) uses four lines: SDR, SDX, SCLK and $\overline{CS}$. Data is transferred by the lines SDR and SDX at the rate given by SCLK. The falling edge of $\overline{CS}$ indicates the beginning of an access. Data is sampled by the at the rising edge of SCLK and shifted out at the falling edge of SCLK. Each access must be terminated by a rising edge of $\overline{CS}$. The accesses to the can be divided into four classes:

1. Configuration Read/Write
2. Register Read/Write
3. Status/Data Read
4. Status/Data Read with Interrupt Acknowledge

If the is in power down mode, a read access to the status register does not deliver valid data with the exception of the RDY bit (RDY=0). After the status has been read the access can be either terminated or extended to read data from the . A register read/write access can only be performed when the is ready. The RDY bit in the status register provides this information.

Any access to the starts with the transfer of 16 bits to the over line SDR. This first word specifies the access class, access type (read or write) and, if necessary, the register accessed. Two access types terminate after the first word: configuration register write and register read. If the configuration register is written, the first word also includes the data and the access is terminated. After an access register read, an access of type data read is necessary to obtain the register data. However, the data is valid only when STATUS:RDY=1.

With a second word, all accesses beside configuration register write and register read deliver the status register from the via line SDX. After the second word, the access status register read terminates while all other accesses transfer data with a third word and terminate then.

Figures 63 to 61 show the timing diagrams for the different access classes and types to the .

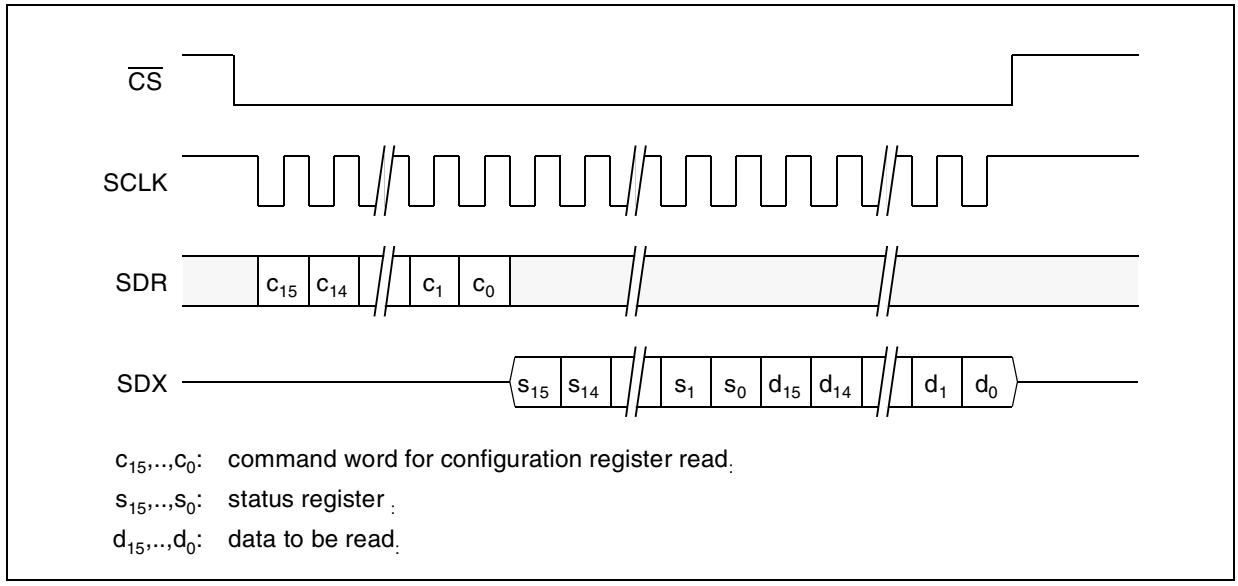


Figure 61 Configuration Register Read Access

Configuration registers at even adresses use bit positions d_7-d_0 while configuration registers at odd adresses use bit positions d_{15}-d_8.

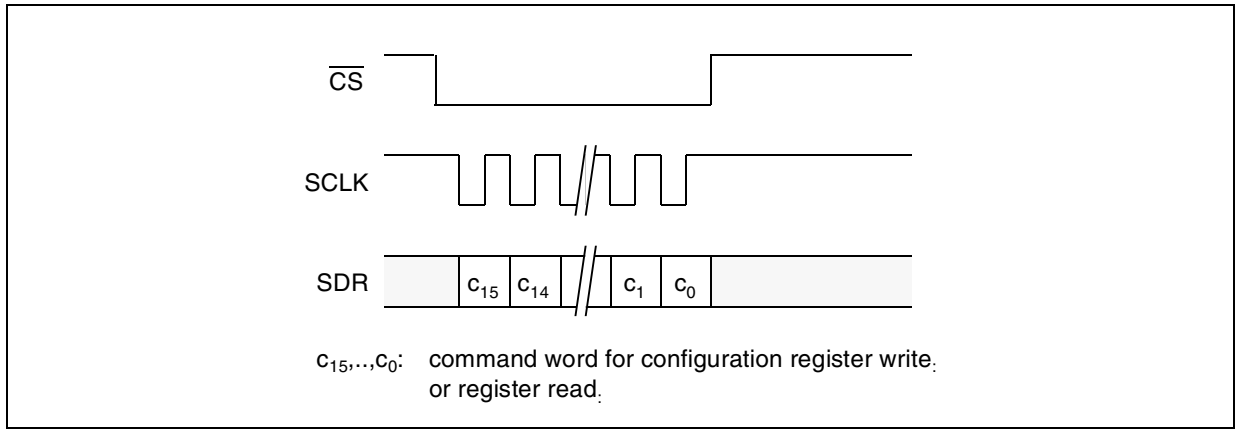


Figure 62 Configuration Register Write Access or Register Read Command

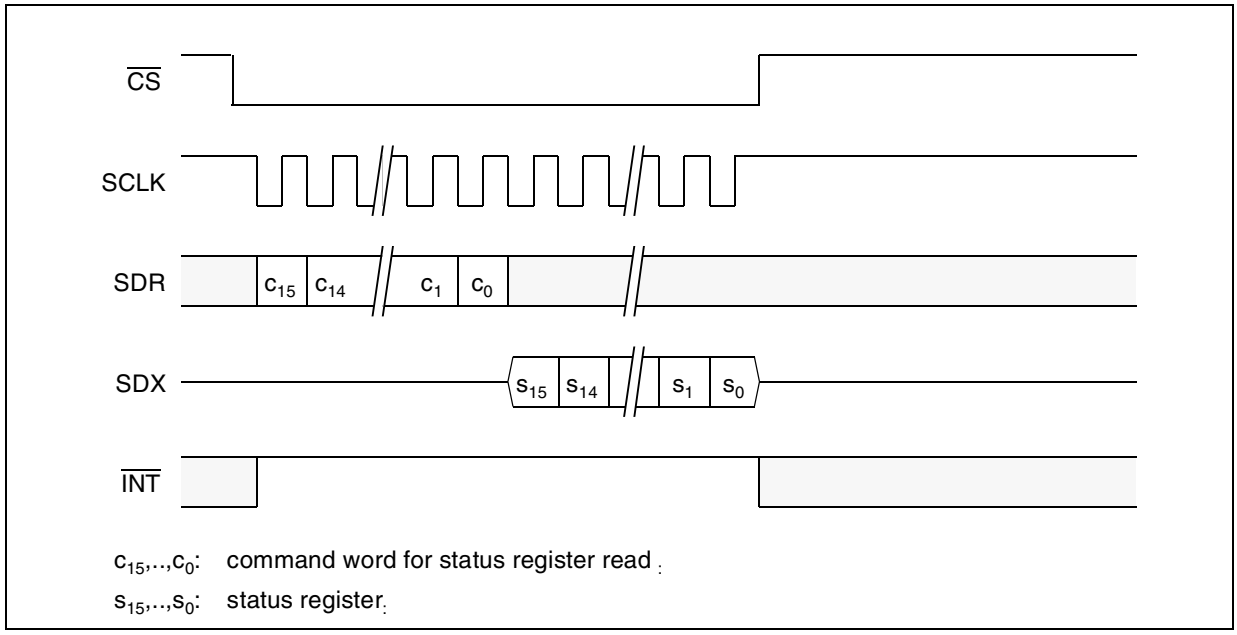


Figure 63 Status Register Read Access

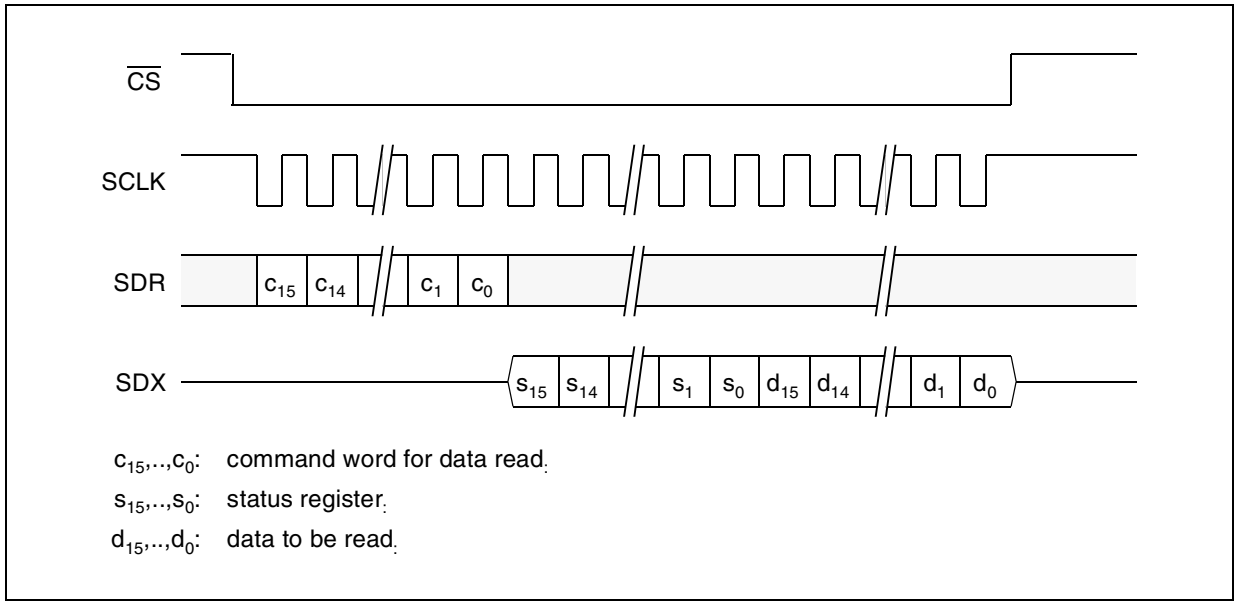


Figure 64 Data Read Access

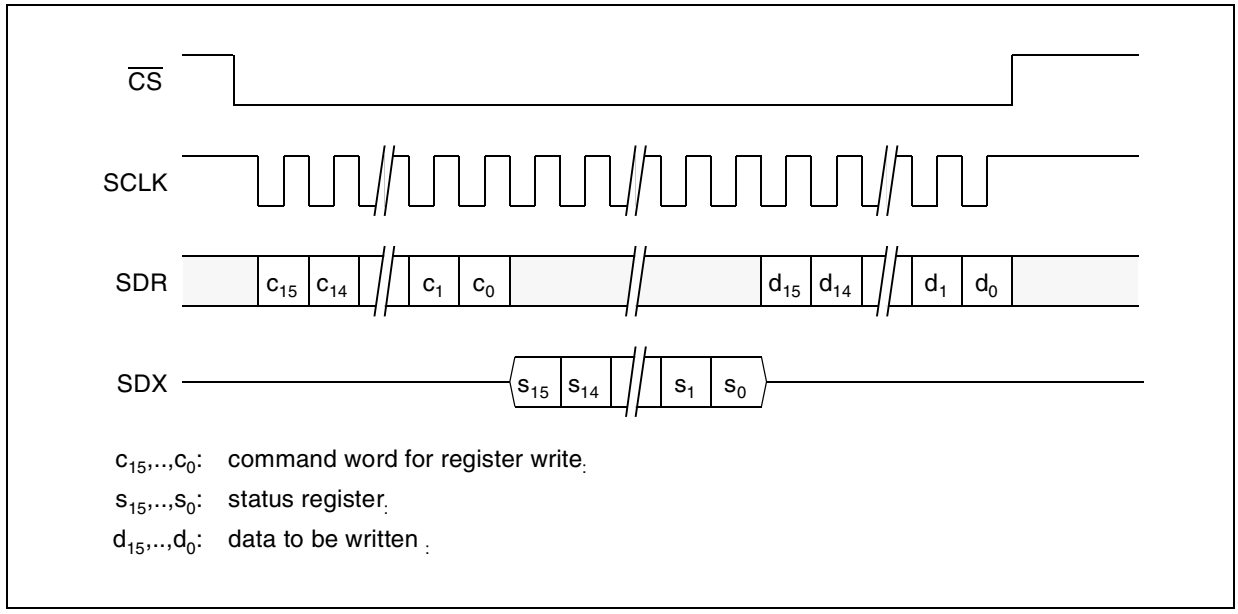


Figure 65 Register Write Access

For all commands the external signal $\overline{INT}$ is deactivated as long as the chip is selected ($\overline{CS}$ is low). For a detailed discussion about the behavior of the interrupt signal please see Chapter 3.3. Table 57 shows the formats of the different command words. All other command words are reserved. Note that interrupts are only acknowledged (cleared) if the command read status/data with interrupt acknowledge is issued.

Table 57 Command Words for Register Access

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Status Register or Data Read Access (interrupt acknowledge)	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Read Status Register or Data Read Access[1)]	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Read Register[1)]	0	1	0	1	REG											
Write Register[1)]	0	1	0	0	REG											
Read Configuration Reg.	0	1	1	1	0	0	R	0	0	0	0	0	0	0	0	0
Write Configuration Reg.	0	1	1	0	0	0	W		DATA							

[1)] Does not acknowledge interrupt.

In case of a configuration register write, W determines what configuration register is to be written (table 58):

Table 58 Address Field W for Configuration Register Write

9	8	Register
0	0	HWCONFIG 0
0	1	HWCONFIG 1
1	0	HWCONFIG 2
1	1	HWCONFIG 3

In case of a configuration register read, R determines what pair of configuration registers is to be read (table 59):

Table 59 Address Field R for Configuration Register Read

9	Register pair
0	HWCONFIG 0 / HWCONFIG 1
1	HWCONFIG 2 / HWCONFIG 3

Note: Reading any register except the status register or a hardware configuration register requires at least two accesses. The first access is a register read command (figure 62). With this access the register address is transferred to the . After that access data read accesses (figure 64) must be executed. The first data read access with STATUS:RDY=1 delivers the value of the register.

4.5 General Purpose Parallel Port

The provides a general purpose parallel port (GP_0 to GP_{15}). The general purpose parallel port has two modes: static mode and multiplex mode. In both modes, the can generate an interrupt on specific input pins and specific signal edges. Each input pin can be masked individually. The events that generated an interrupt are collected in a hold register.

Table 60 shows the registers for mode selection.

Table 60 General Purpose Parallel Port Mode Registers

Register	Name	Comment
HWCONFIG1	APP	Mode selection (static/multiplex)

4.5.1 Static Mode

In static mode all pins of the general purpose parallel port interface have identical functionality. Any pin can be configured as an output or an input. Pins configured as outputs provide a static signal as programmed by the controller. Pins configured as inputs are monitoring the signal continuously without latching. The controller always reads the current value. Table 61 shows the registers used for static mode.

Table 61 Static Mode Registers

Register	# of bits	Comment
DOUT3	16	Output signals (for pins configured as outputs)
DIN	16	Input signals (for pins configured as inputs)
DDIR	16	Pin direction

4.5.2 Multiplex Mode

In multiplex mode, the multiplexes either four output registers or three output register and one input to GP_0-$GP_{11.}$ For this, GP_{12}-GP_{15} are used to distinguish four timeslots. Each timeslot has a duration of approximately 2 ms. The timeslots are separated by a gap of approximately 125 µs, in which none of the signals GP_{12}-GP_{15} are active. The multiplexes three output registers to GP_0-GP_{11} in timeslots 0, 1 and 2. In timeslot 3, the direction of the pins can be programmed. For input pins, the signal is latched with the falling edge of GP_{12}. Table 62 shows the registers used for multiplex mode.

This mode is useful for scanning keys or controlling seven segment LED displays.

Table 62 Multiplex Mode Registers

Register	# of bits	Comment
DOUT0	12	Output signals on GP_0-GP_{11} while GP_{15}=1
DOUT1	12	Output signals on GP_0-GP_{11} while GP_{14}=1
DOUT2	12	Output signals on GP_0-GP_{11} while GP_{13}=1
DOUT3	12	Output signals (for pins configured as outputs) while GP_{12}=1
DIN	12	Input signals (for pins configured as inputs) at falling edge of GP_{12}
DDIR	12	Pin direction during GP_{12}=1

Figure 66 shows the timing diagram for multiplex mode.

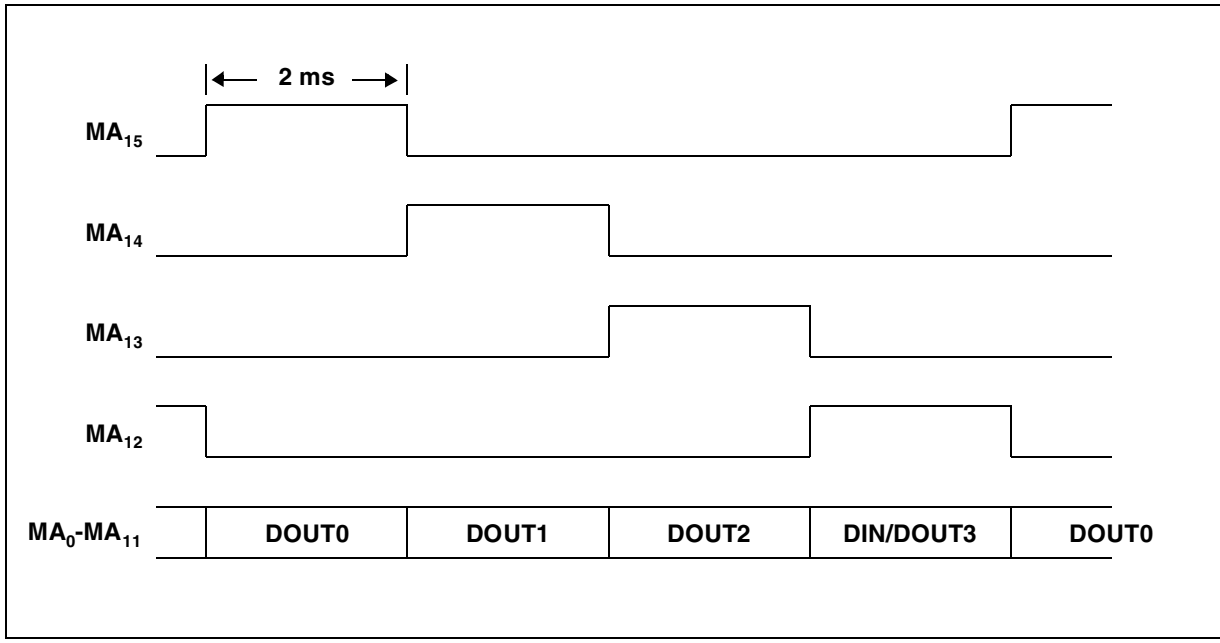


Figure 66 General Purpose Parallel Port - Multiplex Mode

Note: In either mode the voltage at any pin (GP_0 to GP_{15}) must not exceed V_{DD}.

4.5.3 Interrupt Generation

For each pin configured as an input, the compares the current value to the previous value. In static mode, the previous value is the value 1.5 ms ago (static mode). In multiplex mode, the previous value is the value sampled during the previous input timeslot. In both modes, the exact sampling point cannot be defined. For a reliable detection of a specific value, it is therefore necessary that a value must be stable at least 2 ms (static mode) or 8 ms (multiplex mode).

For each input pin the can be programmed to detect the following changes individually (table 63).

Table 63 Interrupt Mask Definition for Parallel Port

DMASK1	DMASK2	Prev. Value	Cur. Value	Remark
0	0	-	-	disabled
0	1	0	1	rising edge
1	0	1	0	falling edge
1	1	0 (1)	1 (0)	both edges

Whenever an input pin meets the specified condition then the sets the corresponding bit within the register DHOLD and also the IPP bit of the STATUS register. Therefore the register DHOLD collects all input pins that have met the programmed condition while the STATUS register collects all events at any pin. The change of bit STATUS:PPI can also trigger an external interrupt depending on the mask register INTM. The bit STATUS:IPP is reset when the register DHOLD is read by the controller. The register DHOLD is also cleared at this time (i.e. when it is read).

Note: The edge detection can be stopped by writing 0 to the register DHOLD. Writing any other value to DHOLD starts the edge detection according to the programmed masks. Edge detection must be started after a wake-up as it is disabled by default.

5 Detailed Register Description

The has a single status register (read only) and an array of data registers (read/write). The purpose of the status register is to inform the external microcontroller of important status changes of the and to provide a handshake mechanism for data register reading or writing. If the generates an interrupt, the status register contains the reason of the interrupt.

5.1 Status Register

RDY Ready

15															0
RDY	ABT	0	0	CIA	CD	CPT UTD	0	0	0	0	DTV	ATV	TG	0	PPI

RDY Ready

0: The last command (if any) is still in progress.

1: The last command has been executed.

ABT Abort

0: No exception during operation

1: An exception caused the to abort any operation currently in progress. The ABT bit is cleared by writing the revision register. No other command is accepted by the while ABT is set.

CIA Caller ID Available

0: No new data for caller ID

1: New caller ID byte available

CD Carrier Detect

0: No carrier detected

1: Carrier detected

CPT Call Progress Tone

0: Currently no call progress tone detected or pause detected (raw mode)

1: Currently a call progress tone is detected

UTD Universal Tone Detected

0: Currently no tone is being detetced

1: Currently a tone is being detected

DTV DTMF Tone Valid

0: No new DTMF code available

1: New DTMF code available in DDCTL

ATV Alert Tone Valid

0: No new alert tone code available

1: New alert tone code available in ATDCTL0

TG Tone Generator Status

0: Tone Generator not running

1: Tone Generator running

PPI Parallel Port Interrupt

0: No unmasked change at input ports of parallel port

1: At least one unmasked input has changed at the parallel port

5.2 Hardware Configuration Registers

HWCONFIG 0 - Hardware Configuration Register 0

7							0
PD	ACS	0	0	PPSDI	0	PPINT	PPSDX

PPSDX Push/Pull for SDX

0: The SDX pin has open-drain characteristic

1: The SDX pin has push/pull characteristic

PPINT Push/Pull for $\overline{\text{INT}}$

0: The $\overline{\text{INT}}$ pin has open-drain characteristic

1: The $\overline{\text{INT}}$ pin has push/pull characteristic

PPSDI Push/Pull for SDI interface

0: The DU and DD pins have open-drain characteristic

1: The DU and DD pins have push/pull characteristic

ACS **AFE Clock Source**

0: AFECLK is derived from the main oscillator

1: AFECLK is derived from the CLK input

PD **Power Down (read only)**

0: The is in active mode

1: The is in power down mode

HWCONFIG 1 - Hardware Configuration Register 1

7					0
GPP	ACT	ADS	MFS	XTAL	SSDI

GPP General Purpose Parallel Port

7	6	Description
0	0	reserved
0	1	APP static mode
1	0	APP multiplex mode
1	1	reserved

ACT AFE Clock Tracking

0: AFECLK tracking disabled

1: AFECLK tracking enabled

MFS Master Frame Sync Selection

0: AFEFSC

1: FSC

XTAL XTAL Frequency

2	1	Factor p[1)]	Description
0	0	5	34.560 MHz
0	1	4.5	31.104 MHz
1	0	4	27.648 MHz
1	1	reserved	reserved

1) The factor p is needed to calculate the clock frequency at AFECLK.

SSDI SSDI Interface Selection

0: IOM®-2 Interface

1: SSDI Interface

HWCONFIG 2 - Hardware Configuration Register 2

7							0
0	ESDX	ESDR	0	0	$\overline{0}$	0	0

ESDX Edge Select for DX

0: DX is transmitted with the rising edge of DCL

1: DX is transmitted with the falling edge of DCL

ESDR Edge Select for DR

0: DR is latched with the falling edge of DCL

1: DR is latched with the rising edge of DCL

HWCONFIG 3 - Hardware Configuration Register 3

7							0
0	0	0	0	0	0	CM1	CM0

CM1 **Clock Master 1**

0: Clock and FS generation at AFECLK and AFEFS disabled

1: Clock and FS generation at AFECLK and AFEFS enabled

CM0 **Clock Master 0**

0: 512 kHz (AFECLK)

1: 1.536 MHz (AFECLK)

00_h REV Revision

15															0
0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0

The revision register can be read only.

Note: A write access to the revision register does not change its content. It does, however, clear the ABT bit of the STATUS register.

01_h CCTL Chip Control

15															0
0	0	0	0	0	0	0	PD	0	0	0	0	0	0	0	0
Reset Value															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PD Power Down

0: is in active mode

1: enter power-down mode

02_h INTM Interrupt Mask Register

15															0
RDY	1	0	0	CIA	CD	CPT UTD	0	0	0	0	DTV	ATV	TG	0	PPI
Reset Value															
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

If a bit of this register is reset (set to 0), the corresponding bit of the status register does not generate an interrupt.

If a bit is set (set to 1), an external interrupt can be generated by the corresponding bit of the status register.

03_h AFECTL Analog Front End Interface Control

15												0
0	0	0	0	ALS	0	0	0	0	0	0	0	EN
Reset Value												
0	0	0	0	0	0	0	0	0	0	0	0	0

ALS Loudspeaker Amplification

This value is transferred on channel C3 of the AFE interface. If the PSB 4851 is used it represents the amplification of the loudspeaker amplifier.

EN Interface Enable

0: AFE interface disabled

1: AFE interface enabled

04_h IFS1 Interface Select 1

15			0
HP	I1	I2	I3
Reset Value			
0	0	0	0

The signal selection fields I1, I2 and I3 of IFS1 determine the outgoing signal of channel 1 of the analog interface. For the PSB 4851 this is usually the line out signal.

The HP bit enables a high-pass for the incoming signal of channel 1 of the analog interface. For the PSB 4851 this is usually the line in signal.

HP **High-Pass for S_1**

0: Disabled

1: Enabled

I1 **Input signal 1 for IG2**

I2 **Input signal 2 for IG2**

I3 **Input signal 3 for IG2**

Note: As all sources are always active, unused sources must be set to 0 (S_0).

05_h IFG1 Interface Gain 1

15		0
0	IG1	

Reset Value

0	8192 (0 dB)

IFG1 is associated with the incoming signal of channel 1 of the analog interface. For the PSB 4851 this is usually the line in signal.

IG1

In order to obtain a gain *G* the parameter IG1 can be calculated by the following formula:

$$IG1 = 32768 \times 10^{(G - 12.04\ dB)/20\ dB}$$

06_h IFG2 Interface Gain 2

15		0
0	IG2	

Reset Value

0	8192 (0 dB)

IFG2 is associated with the outgoing signal of channel 1 of the analog interface. For the PSB 4851 this is usually the line out signal.

IG2 Gain of Amplifier IG2

In order to obtain a gain *G* the parameter IG2 can be calculated by the following formula:

$$IG2 = 32768 \times 10^{(G - 12.04\ dB)/20\ dB}$$

07_h IFS2 Interface Select 2

15			0
HP	I1	I2	I3
Reset Value			
0	0	0	0

The signal selection fields I1, I2 and I3 of IFS2 determine the outgoing signal of channel 2 of the analog interface. For the PSB 4851 this is usually the loudspeaker signal.

The HP bit enables a high-pass for the incoming signal of channel 2 of the analog interface. For the PSB 4851 this is usually the microphone signal.

HP **High-Pass for S_3**

0: Disabled

1: Enabled

I1 **Input signal 1 for IG4**

I2 **Input signal 2 for IG4**

I3 **Input signal 3 for IG4**

Note: As all sources are always active, unused sources must be set to 0 (S_0).

08_h IFG3 Interface Gain 3

15		0
0	IG3	

Reset Value

0	8192 (0 dB)

IFG3 is associated with the incoming signal of channel 2 of the analog interface. For the PSB 4851 this is usually the microphone signal.

IG3 Gain of Amplifier IG3

In order to obtain a gain *G* the parameter IG3 can be calculated by the following formula:

$$IG3 = 32768 \times 10^{(G - 12.04\ dB)/20\ dB}$$

09_h IFG4 Interface Gain 4

15		0
0	IG4	

Reset Value

0	8192 (0 dB)

IFG4 is associated with the outgoing signal of channel 2 of the analog interface. For the PSB 4851 this is usually the loudspeaker signal.

IG4 Gain of Amplifier IG4

In order to obtain a gain *G* the parameter IG4 can be calculated by the following formula:

$$IG4 = 32768 \times 10^{(G - 12.04\ dB)/20\ dB}$$

$0A_h$ SDCONF Serial Data Interface Configuration

15										0
0	0	NTS	0	0	0	0	0	DCL	0	EN
Reset Value										
0	0	0	0	0	0	0	0	0	0	0

NTS Number of Timeslots

11	10	9	8	7	6	Description
0	0	0	0	0	0	1
0	0	0	0	0	1	2
...	...	...	...	...	...	...
1	1	1	1	1	1	64

DCL Double Clock Mode

0: Single Clock Mode

1: Double Clock Mode

EN Enable Interface

0: Interface is disabled (both channels)

1: Interface is enabled (depending on separate channel enable bits)

$0B_h$ SDCHN1 Serial Data Interface Channel 1

15							0
NAS	0	0	PCD	EN	PCM	DD	TS
Reset Value							
0	0	0	0	0	0	0	0

NAS Number of active DRST strobe (SSDI interface mode)

15	14	13	12	Description
0	0	0	0	1
...	...	...	...	...
1	1	1	1	16

PCD PCM Code

0: A-law

1: µ-law

EN Enable Interface

0: Interface is disabled

1: Interface is enabled if SDCONF:EN=1

PCM PCM Mode

0: 16 bit Linear Coding (two timeslots)

1: 8 bit PCM Coding (one timeslot)

DD Data Direction

0: DD: Data Downstream, DU: Data Upstream

1: DD: Data Upstream, DU: Data Downstream

TS Timeslot for Channel 1

5	4	3	2	1	0	Description
0	0	0	0	0	0	0
...	...	...	...	...	...	...
1	1	1	1	1	1	63

Note: If PCM=0 then TS denotes the first timeslot of the two consecutive timeslots used. Only even timeslots are allowed in this case.

$0C_h$ IFS3 Interface Select 3

15			0
HP	I1	I2	I3
Reset Value			
0	0	0	0

The signal selection fields I1, I2 and I3 of IFS3 determine the outgoing signal of channel 1 of the IOM®-2/SSDI-interface.

The HP bit enables a high-pass for the incoming signal of channel 1 of the analog IOM®-2/SSDI-interface.

HP **High-Pass for S_5**

0: Disabled

1: Enabled

I1 **Input signal 1 for S_6**

I2 **Input signal 2 for S_6**

I3 **Input signal 3 for S_6**

Note: As all sources are always active, unused sources must be set to 0 (S_0).

0D$_h$ SDCHN2 Serial Data Interface Channel 2

15										0
CS	0	0	0	0	0	PCD	EN	PCM	DD	TS
Reset Value										
0	0	0	0	0	0	0	0	0	0	0

CS Channel Split

0: Single 16 bit or single 8 bit channel

1: Two adjacent 8 bit channels (SDCHN2:PCM must be set to 0)

PCD PCM Code

0: A-law

1: µ-law

EN Enable Interface

0: Interface is disabled

1: Interface is enabled if SDCONF:EN=1

PCM PCM Mode

0: 16 Bit Linear Coding (two timeslots)

1: 8 Bit PCM Coding (one timeslot)

DD Data Direction

0: DD: Data Downstream, DU: Data Upstream

1: DD: Data Upstream, DD: Data Downstream

TS Timeslot for Channel 2

5	4	3	2	1	0	Description
0	0	0	0	0	0	0
0	0	0	0	0	1	1
...	...	...	...	...	...	...
1	1	1	1	1	1	63

Note: If PCM=0 then TS denotes the first timeslot of the two consecutive timeslots used. Only even timeslots are allowed in this case.

$0E_h$ IFS4 Interface Select 4

15			0
HP	I1	I2	I3
Reset Value			
0	0	0	0

The signal selection fields I1, I2 and I3 of IFS4 determine the outgoing signal of channel 2 of the IOM®-2/SSDI-interface. The HP bit enables a high-pass for the incoming signal of channel 2 of the IOM®-2/SSDI interface.

HP **High-Pass for S_7**

0: Disabled

1: Enabled

I1 **Input signal 1 for S_8**

I2 **Input signal 2 for S_8**

I3 **Input signal 3 for S_8**

Note: As all sources are always active, unused sources must be set to 0 (S_0).

$0F_h$ IFG5 Interface Gain 5

15	0
ATT1	ATT2
Reset Value	
255 (0 dB)	255 (0 dB)

ATT1 Attenuation for I3 (Channel 1)

In order to obtain an attenuation *A* at I3 of channel 1 of the IOM®-2/SSDI interface, the parameter ATT1 can be calculated by the following formula:

$$ATT1 = 256 \times 10^{A/20\ dB}$$

ATT2 Attenuation for I3 (Channel 2)

In order to obtain an attenuation *A* at I3 of channel 2 of the IOM®-2/SSDI interface, the parameter ATT2 can be calculated by the following formula:

$$ATT2 = 256 \times 10^{A/20\ dB}$$

10_h UA Universal Attenuator

15				0
ATT	0	0	0	I1
Reset Value				
0 (96 dB)	0	0	0	0

ATT Attenuation for UA

For a given attenuation *A* [dB] the parameter ATT can be calculated by the following formula:

$$ATT = 256 \times 10^{-A/20\ dB}$$

I1 Input Selection for UA

11_h DGCTL DTMF Generator Control

15												0
EN	MD	0	0	0	0	0	0	0	0	0	0	DTC
Reset Value												
0	0	0	0	0	0	0	0	0	0	0	0	0

EN **Generator Enable**

0: Disabled

1: Enabled

MD **Mode**

0: raw

1: cooked

DTC **Dial Tone Code (cooked mode)**

3	2	1	0	Digit	Frequency
0	0	0	0	1	697/1209
0	0	0	1	2	697/1336
0	0	1	0	3	697/1477
0	0	1	1	A	697/1633
0	1	0	0	4	770/1209
0	1	0	1	5	770/1336
0	1	1	0	6	770/1477
0	1	1	1	B	770/1633
1	0	0	0	7	852/1209
1	0	0	1	8	852/1336
1	0	1	0	9	852/1477
1	0	1	1	C	852/1633
1	1	0	0	*	941/1209
1	1	0	1	0	941/1336
1	1	1	0	#	941/1477
1	1	1	1	D	941/1633

12_h DGF1 DTMF Generator Frequency 1

15															0
0	FRQ														

FRQ Frequency of Generator 1

The parameter FRQ for a given frequency *f* [Hz] can be calculated by the following formula:

$$FRQ = 32768 \times \frac{f}{4000Hz}$$

13_h DGF2 DTMF Generator Frequency 2

15		0
0	FRQ	

FRQ Frequency of Generator 2

he parameter FRQ for a given frequency *f* [Hz] can be calculated by the following formula:

$$FRQ = 32768 \times \frac{f}{4000\,Hz}$$

14_h DGL DTMF Generator Level

15			0
0	LEV2	0	LEV1

LEV2 Signal Level of Generator 2

In order to obtain a signal level *L* (relative to the PCM maximum value) for generator 2 the value of LEV2 can be calculated according to the following formula:

$$LEV2 = 128 \times 10^{L/20\ dB}$$

LEV1 Signal Level of Generator 1

In order to obtain a signal level *L* (relative to the PCM maximum value) for generator 1 the value of LEV1 can be calculated according to the following formula:

$$LEV1 = 128 \times 10^{L/20\ dB}$$

15_h DGATT DTMF Generator Attenuation

15	0
ATT2	ATT1

ATT2 Attenuation of Signal S_{10}

In order to obtain attenuation *A* the parameter ATT2 can be calculated by the formula:

$$ATT2 = \begin{cases} 128 + 1024 \times 10^{-A/20\ dB} & ;A > 18,1\ dB \\ 128 \times 10^{-A/20\ dB} & ;A < 18,1\ dB \end{cases}$$

ATT1 Attenuation of Signal S_9

In order to obtain attenuation *A* the parameter ATT1 can be calculated by the formula:

$$ATT1 = \begin{cases} 128 + 1024 \times 10^{-A/20\ dB} & ;A > 18,1\ dB \\ 128 \times 10^{-A/20\ dB} & ;A < 18,1\ dB \end{cases}$$

$1A_h$ ATDCTL0 Alert Tone Detection 0

15										0
EN	0	0	I1	0	0	0	0	0	0	ATC
Reset Value										
0	0	0	0	0	0	0	0	0	0	-[1]

[1] undefined

EN **Enable alert tone detection**

0: The alert tone detection is disabled

1: The alert tone detection is enabled

I1 **Input signal selection**

ATC **Alert Tone Code**

1	0	Description
0	0	no tone
0	1	2130
1	0	2750
1	1	2130/2750

$1B_h$ ATDCTL1 Alert Tone Detection 1

15								0
MD	0	0	DEV	0	0	0	ONH	MIN

MD **Alert tone detection mode**

0: Only a dual tone is detected

1: Either a dual or a single tone is detected

DEV **Maximum frequency deviation for alert tone**

0: 0.5%

1: 1.1%

ONH **On Hook**

0: Off hook

1: On hook

MIN **Minimum level of alert tone signal**

For a minimum signal level *min* the parameter MIN is given by the following formula:

$$MIN = 2560 \times 10^{min/20\ dB}$$

$1C_h$ CIDCTL0 Caller ID Control 0

15				0
EN	DOT	CM	I1	DATA
Reset Value				
0	0	0	0	0

EN **CID Enable**

0: Disabled

1: Enabled

DOT **Drop Out Tolerance**

0: Drop out during mark or seizure sequence aborts recognition

1: Drop out tolerance during mark or seizure sequence.

CM **Compatibilitiy Mode**

0: Standard Caller ID Decoder

1: Improved Caller ID Decoder (Bellcore compliant)

I1 **Input signal selection**

DATA **Last received data byte**

1D$_h$ CIDCTL1 Caller ID Control 1

15		0
NMB	NMSS	MIN

NMB Minimum Number of Mark Bits

15	14	13	12	11	Description
0	0	0	0	0	0
0	0	0	0	1	10
0	0	0	1	0	20
...	...	...	...	...	...
1	1	1	1	1	310

NMSS Minimum Number of Mark/Space Sequences

10	9	8	7	6	Description
0	0	0	0	0	1
0	0	0	0	1	11
0	0	0	1	0	21
...	...	...	...	...	
1	1	1	1	1	311

MIN Minimum Signal Level for CID Decoder

For a minimum signal level *min* the parameter MIN is given by the following formula:

$$MIN = 640 \times 10^{min/20\ dB}$$

$1E_h$ IFS5 Interface Select 5

15			0
HP	I1	I2	I3
Reset Value			
0	0	0	0

The signal selection fields I1, I2 and I3 of IFS5 determine the outgoing signal of channel 3 of the IOM/SSDI-interface. The HP bit enables a high-pass for the incoming signal of channel 3.

HP **High-Pass for S_{23}**

0: Disabled

1: Enabled

I1 **Input signal 1 for S_{24}**

I2 **Input signal 2 for S_{24}**

I3 **Input signal 3 for S_{24}**

As all sources are always active, unused sources must be set to 0 (S_0).

$1F_h$ IFG6 Interface Gain 6

15							0
ATT3	0	0	0	0	0	0	0
Reset Value							
255 (0 dB)	0	0	0	0	0	0	0

ATT3 Attenuation for I3 (Channel 3)

In order to obtain an attenuation *A* the parameter ATT3 can be calculated by the following formula:

$$ATT3 = 256 \times 10^{A/20\ dB}$$

20_h CPTCTL Call Progress Tone Control

15											0
EN	MD	0	0	0	0	0	0	0	0	0	I1
Reset Value											
0	0	0	0	0	0	0	0	0	0	0	0

EN **CPT Detector Enable**

0: Disabled

1: Enabled

MD **CPT Mode**

0: raw

1: cooked

I1 **Input signal selection**

21_h CPTTR Call Progress Tone Thresholds

15			0
NUM	0	SN	MIN

NUM Number of Cycles

15	14	13	cooked mode	raw mode
0	0	0	reserved	0
0	0	1	2	reserved
...	...	...	...	reserved
1	1	1	8	reserved

SN Minimal Signal-to-Noise Ratio

11	10	9	8	Description
1	1	1	1	9 dB
1	0	0	0	12 dB
0	1	0	0	15 dB
0	0	1	0	18 dB
0	0	0	0	22 dB

MIN Minimum Signal Level for CPT Detector

Value	Description
64_h	-30 dB
60_h	-32 dB
$7A_h$	-34 dB
74_h	-36 dB
70_h	-38 dB
89_h	-40 dB
85_h	-42 dB
80_h	-44 dB
$9A_h$	-46 dB
95_h	-48 dB
90_h	-50 dB

22_h CPTMN CPT Minimum Times

15	0
MINB	MING

MINB Minimum Time for CPT Burst

The parameter MINB for a minimal burst time *TBmin* can be calculated by the following formula:

$$MINB = \frac{TBmin - 32\ ms}{4}$$

MING Minimum Time for CPT Gap

The parameter MING for a minimal gap time *TGmin* can be calculated by the following formula:

$$MING = \frac{TGmin - 32\ ms}{4}$$

23_h CPTMX CPT Maximum Times

15	0
MAXB	MAXG

MAXB Maximum Time for CPT Burst

The parameter MAXB for a maximal burst time of *TBmax* can be calculated by the following formula:

$$MAXB = \frac{TBmax - TBmin}{8}$$

MAXG Maximum Time for CPT Gap

The parameter MAXG for a maximal burst time of *TGmax* can be calculated by the following formula:

$$MAXG = \frac{TGmax - TGmin}{8}$$

24_h CPTDT CPT Delta Times

15	0
DIFB	DIFG

DIFB Maximum Time Difference between consecutive Bursts

The parameter DIFB for a maximal difference of *t* ms of two burst durations can be calculated by the following formula:

$$DIFB = \frac{t}{2\ ms}$$

DIFG Maximum Time Difference between consecutive Gaps

The parameter DIFG for a maximal difference of *t* ms of two gap durations can be calculated by the following formula:

$$DIFG = \frac{t}{2\ ms}$$

25_h LECCTL Line Echo Cancellation Control

15						0
EN	CM	AS	SP	0	I1	I2
Reset Value						
0	0	0	0	0	0	0

EN Enable

0: Disabled

1: Enabled

CM Line Echo Canceller Mode

14	13	Line echo canceller mode
0	0	Normal mode
0	1	Superior mode
1	0	Extended mode
1	1	Reserved

AS Adaptation Stop

0: Adation enabled

1: Adation stopped

SP Adaptation Speed

0: Fast adaptation (extended mode only)

1: Slow adaptation (extended mode only)

I1 Input signal selection for I_1

I2 Input signal selection for I_2

26_h LECLEV Minimal Signal Level for Line Echo Cancellation

15		0
0	MIN	

MIN

The parameter MIN for a minimal signal level *L* (dB) can be calculated by the following formula:

$$MIN = \frac{512 \times (96.3 + L)}{5 \times \log 2}$$

27_h LECATT Externally Provided Attenuation

15		0
0	ATT	

ATT

The parameter ATT for an externally provided attenuation *A* (dB) can be calculated by the following formula:

$$ATT = \frac{512 \times A}{5 \times \log 2}$$

ATT has a slightly different meaning in normal and in superior mode. In normal mode, it represents just the externally provided attenunation while in superior mode, it represents the externally provided attenuation minus a threshold. The formula above holds in both cases.

In superior mode, the parameter ATT is implemented in two's complement.

In normal mode, the parameter ATT is not allowed to be negative, i.e., the MSB (bit 15) must be 0.

28_h LECMGN Margin for Double Talk Detection

15		0
0	MGN	

MGN

The parameter MGN for a margin of *L* (dB) can be calculated by the following formula:

$$MGN = \frac{512 \times L}{5 \times \log 2}$$

Note: MGN has a different meaning in normal and in superior mode. The formula above holds in any mode, though.

29_h DDCTL DTMF Detector Control

15							0
EN	0	0	I1	0	0	0	DTC[1)]
Reset Value							
0	0	0	0	0	0	0	-[2)]

1) The DTC code remains valid until a new DTMF tone has been detected.

2) undefined

EN Enable DTMF tone detection

0: The DTMF detection is disabled

1: The DTMF detection is enabled

I1 Input signal selection

DTC DTMF Tone Code

4	3	2	1	0	Frequency	Digit
1	0	0	0	0	941 / 1633	D
1	0	0	0	1	697 / 1209	1
1	0	0	1	0	697 / 1336	2
1	0	0	1	1	697 / 1477	3
1	0	1	0	0	770 / 1209	4
1	0	1	0	1	770 / 1336	5
1	0	1	1	0	770 / 1477	6
1	0	1	1	1	852 / 1209	7
1	1	0	0	0	852 / 1336	8
1	1	0	0	1	852 / 1477	9
1	1	0	1	0	941 / 1336	0
1	1	0	1	1	941 / 1209	*
1	1	1	0	0	941 / 1477	#
1	1	1	0	1	697 / 1633	A
1	1	1	1	0	770 / 1633	B
1	1	1	1	1	852 / 1633	C

$2A_h$ DDTW DTMF Detector Signal Twist

15		0
0	TWIST	

TWIST Signal twist for DTMF tone

In order to obtain a minimal signal twist *T* the parameter TWIST can be calculated by the following formula:

$$\text{TWIST} = 32768 \times 10^{(-(0.5\ \text{dB}+T))/10\ \text{dB}}$$

Note: TWIST must be in the range [4096,20480]

$2B_h$ DDLEV DTMF Detector Minimum Signal Level

15										0
1	1	1	1	1	1	1	1	1	1	MIN

MIN Minimum Signal Level

5	4	3	2	1	0	Description
0	0	1	1	1	0	-50 dB
0	0	1	1	1	1	-49 dB
...	...	...	...	...	...	...
1	0	0	0	0	1	-31 dB
1	0	0	0	1	0	-30 dB

Note: Values outside the given range are reserved and must not be used.

$2C_h$ FCFCTL1 Equalizer 1 Control

15						0
EN	0	ADR	0	0	0	I1
Reset Value						
0	0	0	0	0	0	0

EN Enable equalizer 1

0: The equalizer is disabled

1: The equalizer is enabled

ADR Coefficient address

13	12	11	10	9	8	Coefficient
0	0	0	0	0	0	A1
0	0	0	0	0	1	A2
0	0	0	0	1	0	A3
0	0	0	0	1	1	A4
0	0	0	1	0	0	A5
0	0	0	1	0	1	A6
0	0	0	1	1	0	A7
0	0	0	1	1	1	A8
0	0	1	0	0	0	A9
0	0	1	0	0	1	B2
0	0	1	0	1	0	B3
0	0	1	0	1	1	B4
0	0	1	1	0	0	B5
0	0	1	1	0	1	B6
0	0	1	1	1	0	B7
0	0	1	1	1	1	B8
0	1	0	0	0	0	B9
0	1	0	0	0	1	C1
0	1	0	0	1	0	D1
0	1	0	0	1	1	D2
0	1	0	1	0	0	D3
0	1	0	1	0	1	D4
0	1	0	1	1	0	D5

13	12	11	10	9	8	Coefficient
0	1	0	1	1	1	D6
0	1	1	0	0	0	D7
0	1	1	0	0	1	D8
0	1	1	0	1	0	D9
0	1	1	0	1	1	D10
0	1	1	1	0	0	D11
0	1	1	1	0	1	D12
0	1	1	1	1	0	D13
0	1	1	1	1	1	D14
1	0	0	0	0	0	D15
1	0	0	0	0	1	D16
1	0	0	0	1	0	D17
1	0	0	0	1	1	C2

I1 Input signal selection

$2D_h$ FCFCOF1 Equalizer 1 Coefficient Data

15															0
V															

V Coefficient value

For the coefficients A_1-A_9, B_2-B_9 and D_1-D_{17}, the following formula can be used, where V denotes the coefficient value of the coefficient *c*:

$$V = 32768 \times c \qquad ; -1 \leq c < 1$$

For the coefficients C_1 and C_2, the following formula can be used, where V denotes the coefficient value of the coefficient *c*:

$$V = 128 \times c \qquad ; 1 \leq c < 256$$

$2E_h$ FCFCTL2 Equalizer 2 Control

15						0
EN	0	ADR	0	0	0	I1
Reset Value						
0	0	0	0	0	0	0

EN **Enable equalizer 1**

0: The equalizer is disabled

1: The equalizer is enabled

ADR **Coefficient address**

13	12	11	10	9	8	Coefficient
0	0	0	0	0	0	A1
0	0	0	0	0	1	A2
0	0	0	0	1	0	A3
0	0	0	0	1	1	A4
0	0	0	1	0	0	A5
0	0	0	1	0	1	A6
0	0	0	1	1	0	A7
0	0	0	1	1	1	A8
0	0	1	0	0	0	A9
0	0	1	0	0	1	B2
0	0	1	0	1	0	B3
0	0	1	0	1	1	B4
0	0	1	1	0	0	B5
0	0	1	1	0	1	B6
0	0	1	1	1	0	B7
0	0	1	1	1	1	B8
0	1	0	0	0	0	B9
0	1	0	0	0	1	C1
0	1	0	0	1	0	D1
0	1	0	0	1	1	D2
0	1	0	1	0	0	D3
0	1	0	1	0	1	D4
0	1	0	1	1	0	D5

13	12	11	10	9	8	Coefficient
0	1	0	1	1	1	D6
0	1	1	0	0	0	D7
0	1	1	0	0	1	D8
0	1	1	0	1	0	D9
0	1	1	0	1	1	D10
0	1	1	1	0	0	D11
0	1	1	1	0	1	D12
0	1	1	1	1	0	D13
0	1	1	1	1	1	D14
1	0	0	0	0	0	D15
1	0	0	0	0	1	D16
1	0	0	0	1	0	D17
1	0	0	0	1	1	C2

I1 Input signal selection

$2F_h$ FCFCOF2 Equalizer 2 Coefficient Data

15															0
V															

V Coefficient value

For the coefficients A_1-A_9, B_2-B_9 and D_1-D_{17}, the following formula can be used, where V denotes the coefficient value of the coefficient *c*:

$$V = 32768 \times c \quad ; -1 \leq c < 1$$

For the coefficients C_1 and C_2, the following formula can be used, where V denotes the coefficient value of the coefficient *c*:

$$V = 128 \times c \quad ; 1 \leq c < 256$$

30_h TGCTL Tone Generator Control

15													0
0	0	0	0	0	0	0	0	0	CGM	DT	BGM	SM	WF
Reset Value													
0	0	0	0	0	0	0	0	0	0	0	0	0	0

CGM Control Generator Mode

6	5	Description
0	0	Tone Generator off
0	1	Tone Generator on
1	-	Tone Generator enabled/disabled by Control Generator

DT Dual Tone

0: F4 not added (option 1)

1: F4 added (option 2)

BGM Beat Generator Mode

3	2	Description
0	0	Continuous Tone F1
0	1	Continuous Tone F2
1	0	two tone cadence
1	1	three tone sequence

SM Stop Mode

0: Immediate

1: Controlled

WF Waveform

0: Sine Wave

1: Square Wave

31_h TGTON Tone Generator Time TON

15		0
TM		TE

TM Mantissa of TON

The mantissa TM for a time *t* ([ms]) can be calculated by the following formula:

$$TM = \frac{t}{2^{TE}}$$

TE Exponent of TON

The exponent TE for a time *t* ([ms]) can be calculated by the following formula:

$$TE = \log_2 t$$

Note: TE > 0

32_h TGTOFF Tone Generator Time TOFF

15		0
TM		TE

TM Mantissa of TOFF

The mantissa TM for a time *t* ([ms]) can be calculated by the following formula:

$$TM = \frac{t}{2^{TE}}$$

TE Exponent of TOFF

The exponent TE for a time *t* ([ms]) can be calculated by the following formula:

$$TE = \log_2 t$$

Note: TE > 0

33_h TGT1 Tone Generator Time T1

15															0
TIME															

TIME

The parameter TIME for a time *t* ([ms]) can be calculated by the following formula:

$$TIME = \frac{t}{8}$$

34_h TGF1 Tone Generator Frequency F1

15															0
0	F														

F Frequency

The parameter F for a frequency *f* ([Hz]) can be calculated by the following formula:

$$F = 8.192 \times f$$

Note: If a sine waveform is selected, the frequency f is output. If a square waveform is selected the next lower frequency that is a harmonic frequency is output.

35_h TGG1 Tone Generator Gain G1

15		0
0	G	

G Gain

The parameter G for a gain *g* ([dB]) can be calculated by the following formula:

$$F = 32768 \times 10^{g/20}$$

36_h TGT2 Tone Generator Time T2

15															0
TIME															

TIME

The parameter TIME for a time *t* ([ms]) can be calculated by the following formula:

$$\text{TIME} = \frac{t}{8}$$

37_h TGF2 Tone Generator Frequency F2

15		0
0	F	

F Frequency

The parameter F for a frequency *f* ([Hz]) can be calculated by the following formula:

$$F = 8.192 \times f$$

Note: If a sine waveform is selected, the frequency f is output. If a square waveform is selected the next lower frequency that is a harmonic frequency is output.

38_h TGG2 Tone Generator Gain G2

15		0
0	G	

G Gain

The parameter G for a gain *g* ([dB]) can be calculated by the following formula:

$$F = 32768 \times 10^{g/20}$$

39_h TGT3 Tone Generator Time T3

15															0
TIME															

TIME

The parameter TIME for a time *t* ([ms]) can be calculated by the following formula:

$$TIME = \frac{t}{8}$$

$3A_h$ TGF3 Tone Generator Frequency F3

15															0
0	F														

F Frequency

The parameter F for a frequency *f* ([Hz]) can be calculated by the following formula:

$$F = 8.192 \times f$$

Note: If a sine waveform is selected, the frequency f is output. If a square waveform is selected the next lower frequency that is a harmonic frequency is output.

$3B_h$ TGG3 Tone Generator Gain G3

15		0
0	G	

G Gain

The parameter G for a gain *g* ([dB]) can be calculated by the following formula:

$$F = 32768 \times 10^{g/20}$$

$3C_h$ TGF4 Tone Generator Frequency F4

15		0
0	F	

F Frequency

The parameter F for a frequency *f* ([Hz]) can be calculated by the following formula:

$$F = 8.192 \times f$$

Note: If a sine waveform is selected, the frequency f is output. If a square waveform is selected the next lower frequency that is a harmonic frequency is output.

$3D_h$ TGG4 Tone Generator Gain G4

15		0
0	G	

G Gain

The parameter G for a gain *g* ([dB]) can be calculated by the following formula:

$$F = 32768 \times 10^{g/20}$$

$3E_h$ TGGO1 Tone Generator Gain Output 1

15															0
0	G														

G Gain

The parameter G for a gain *g* ([dB]) can be calculated by the following formula:

$$F = 32768 \times 10^{g/20}$$

$3F_h$ TGGO2 Tone Generator Gain Output 2

15		0
0	G	

G Gain

The parameter G for a gain *g* ([dB]) can be calculated by the following formula:

$$F = 32768 \times 10^{g/20}$$

45_h PDCTL Peak Detector Control

15											0
EN	MM	0	0	0	0	0	0	0	0	0	I1
Reset Value											
0	0	0	0	0	0	0	0	0	0	0	0

EN **Peak Detector Enable**

0: Disabled

1: Enabled

MM **Min/Max**

0: Maximum

1: Minimum

I1 **Input signal selection**

46_h PDDATA Peak Detector Data

15															0
DATA															

DATA

Maximum or minimum value of signal since last read access.

Note: This register can only be read.

47h SPSCTL SPS Control

15										0
POS	0	0	0	0	0	0	0	MODE	SP1	SP0
Reset Value										
0	0	0	0	0	0	0	0	0	-[1]	-[1]

[1] undefined

POS Position of Status Register Window

15	14	13	12	SPS_0	SPS_1
0	0	0	0	Bit 0	Bit 1
0	0	0	1	Bit 1	Bit 2
...	...	...	...	...	...
1	1	1	0	Bit 14	undefined

MODE Mode of SPS Interface

4	3	2	Description
0	0	0	Disabled (SPS_0 and SPS_1 zero)
0	0	1	Output of SP1 and SP0
1	0	0	Output of speakerphone state at SP1 and SP0
1	1	0	Output of STATUS register at SP1 and SP0

SP1 Direct Control for SPS_1

0: SPS_1 set to 0

1: SPS_1 set to 1

SP0 Direct Control for SPS_0

0: SPS_0 set to 0

1: SPS_0 set to 1

Note: If mode 1 has been selected prior to power-down, both mode 1 and the values of SP1 and SP0 are retained during power-down and wake-up. Other modes are reset to 0 during power down.

$4A_h$ DOUT0 Data Out (Timeslot 0)

15					0
0	0	0	0	DATA	
Reset Value					
0	0	0	0	0	

DATA Output Data

Output data for pins GP_0-GP_{11} while GP_{12}=1 (only if HWCONFIG1:GPP=10).

$4B_h$ DOUT1 Data Out (Timeslot 1)

15					0
0	0	0	0	DATA	
Reset Value					
0	0	0	0	0	

DATA Output Data

Output data for pins GP_0-GP_{11} while GP_{13}=1 (only if HWCONFIG1:GPP=10).

$4C_h$ DOUT2 Data Out (Timeslot 2)

15					0
0	0	0	0	DATA	

Reset Value				
0	0	0	0	0

DATA Output Data

Output data for pins GP_0-GP_{11} while GP_{14}=1 (only if HWCONFIG1:GPP=10).

$4D_h$ DOUT3 Data Out (Timeslot 3 or Static Mode)

15	0
DATA	

Reset Value

0

DATA Output Data

Output data for pins GP_0-GP_{11} while GP_{15}=1 (only if HWCONFIG1:GPP=10).

Output data for pins GP_0-GP_{15} (only if HWCONFIG1:GPP=01)

$4E_h$ DIN Data In (Timeslot 3 or Static Mode)

15															0
DATA															

DATA Input Data

Input data for pins GP_0-GP_{11} at falling edge of GP_{12} (only if HWCONFIG1:GPP=10).

Input data for pins GP_0-GP_{15} (only if HWCONFIG1:GPP=01)

$4F_h$ DDIR Data Direction (Timeslot 3 or Static Mode)

15															0
DIR															
Reset Value															
0 (all inputs)															

DIR Port Direction

Port direction during GP_{12}=1 or in static mode.

0: input

1: output

50_h DMASK1 Data In Mask 1 (Timeslot 3 or Static Mode)

15															0
MASK															

MASK Bit mask for falling edge detection

If a bit of the mask is set and the corresponding pin is configured as an input, a falling edge at this input will set the PPI bit of the STATUS register.

51_h DMASK2 Data In Mask 2 (Timeslot 3 or Static Mode)

15															0
MASK															

MASK Bit mask for rising edge detection

If a bit of the mask is set and the corresponding pin is configured as an input, a rising edge at this input will set the PPI bit of the STATUS register.

52_h DHOLD Data In Hold (Timeslot 3 or Static Mode)

15	0
DATA	

DATA

All events, which were not masked by DMASK1 or DMASK2 register, are collected in this register since the last read access. Whenever this register is read it is reset to zero. A bit is subsequently set if an unmasked event happens at the corresponding input pin.

58_h AGCCTL AGC Control

15							0
EN	0	0	0	0	0	I1	I2
Reset Value							
0	0	0	0	0	0	0	0

EN **Enable**

0: Disabled

1: Enabled

I1 **Input signal selection for I_1**

I2 **Input signal selection for I_2**

59_h AGCATT Automatic Gain Control Attenuation

15		0
0	ATT	

ATT

The parameter ATT for an attenuation *A* ([dB]) can be calculated by the following formula:

$$ATT = 32768 \times 10^{\frac{-A}{20}}$$

$5A_h$ AGC1 Automatic Gain Control 1

15	0
COM	AG_INIT

COM

The parameter COM for a signal level *L* ([dB]) can be calculated by the following formula:

$$COM = \begin{cases} 128 + 10^{\frac{L + 66,22}{20}} & ;L < -42,14\ dB \\ 10^{\frac{L + 42,14}{20}} & ;L > -42,14\ dB \end{cases}$$

AG_INIT

In order to obtain an initial gain *G* ([db]) the parameter AG_INIT can be calculated by the following formula:

$$AG\_INIT = \begin{cases} 128 + 10^{\frac{G + 18,06}{20}} & ;G < 6,02\ dB \\ 10^{\frac{G - 6,02}{20}} & ;G > 6,02\ dB \end{cases}$$

$5B_h$ AGC2 Automatic Gain Control 2

15	0
SPEEDL	SPEEDH

SPEEDL

The parameter SPEEDL for a multiplication factor *M* is given by the following formula:

$$SPEEDL = M \times 8192$$

SPEEDH

The parameter SPEEDH for a multiplication factor *M* is given by the following formula:

$$SPEEDH = M \times 256$$

$5C_h$ AGC3 Automatic Gain Control 3

15	0
AG_GAIN	AG_ATT

AG_GAIN

The parameter AG_GAIN for a gain *G* ([dB]) can be calculated by the following formula:

$$AG\_GAIN = \begin{cases} 128 + 10^{\frac{G + 18.06}{20}} & ;G < 24\ dB \\ 10^{\frac{G - 6.02}{20}} & ;G > 24\ dB \end{cases}$$

AG_ATT

The parameter AG_ATT for an attenuation *A* ([dB]) can be calculated by the following formula:

$$AG\_ATT = 10^{\frac{A + 42.14}{20}}$$

$5D_h$ AGC4 Automatic Gain Control 4

15	0
DEC	LIM

DEC

The parameter DEC for a time constant *t* ([1/ms]) is given by the following formula:

$$DEC = \frac{256}{t}$$

LIM

The parameter LIM for a signal level *L* ([dB]) can be calculated by the following formula:

$$LIM = \begin{cases} 128 + 10^{\frac{L+90.3}{20}} & ;L < -50\ dB \\ 10^{\frac{L+66.22}{20}} & ;-25 > L > -50\ dB \end{cases}$$

$5E_h$ AGC5 Automatic Gain Control 5

15								0
0	0	0	0	0	0	0	0	LP

LP

The parameter LP for a time constant *t* ([1/ms]) is given by the following formula:

$$LP = \frac{16}{t}$$

Note: The value for LP should be at least 80_h (i.e., t<4ms) in order to avoid that the AGC becomes instable.

60_h SCTL Speakerphone Control

15													0
ENS	QU		EWF	NAD	NR	CN	MD	SDR	SDX	ERD	0	AGR	AGX	0
Reset Value														
0	0		0	0	0	0	0	0	0	0	0	0	0	0

ENS Enable Echo Suppression

0: The echo suppression unit is disabled

1: The echo suppression unit is enabled

QU Echo Cancellation Quality Mode

14	13	12	Description
0	0	0	Echo cancellation disabled (half duplex)
0	0	1	Subband, RNR
0	1	0	Fullband mode one (similar to PSB 2170 Version 1.1)
0	1	1	Fullband mode two
1	0	0	Subband, reduced filter length
1	0	1	Subband, analog line mode
1	1	0	Subband, ISDN mode
1	1	1	Subband, enhanced mode

EWF Enable Wiener Filter

0: The Wiener filter is disabled

1: The Wiener filter is enabled (in subband mode only)

NAD Noise Adaptation

0: Noise adaptation is disabled.

1: Noise adaptation is enabled.

NR Noise Reduction Enable

0: Noise reduction disabled

1: Noise reduction enabled

CN **Comfort Noise**

0: The comfort noise generator is disabled.

1: The comfort noise generator is enabled.

MD **Mode**

0: Speakerphone mode

1: Loudhearing mode

SDR **Signal Source of SDR**

0: after AGCR

1: before AGCR

SDX **Signal Source of SDX**

0: after AGCX

1: before AGCX

ERD **Enable Reduced Delay**

0: Normal operation in fullband mode two

1: The delay of fullband mode two is reduced

AGR **AGCR Enable**

0: AGCR disabled

1: AGCR enabled

AGX **AGCX Enable**

0: AGCX disabled

1: AGCX enabled

62_h SSRC1 Speakerphone Source 1

15							0
0	0	0	0	0	0	I1	I2
Reset Value							
0	0	0	0	0	0	0	0

I1 **Input Signal Selection (Acoustic Source 1)**

I2 **Input Signal Selection (Acoustic Source 2)**

63_h SSRC2 Speakerphone Source 2

15							0
0	0	0	0	0	0	I3	I4
Reset Value							
0	0	0	0	0	0	0	0

I3 **Input Signal Selection (Line Source 1)**

I4 **Input Signal Selection (Line Source 2)**

64_h SSDX1 Speech Detector (Transmit) 1

15			0
0	LP2L	0	LIM

Reset Value

$1B3A_h$

LP2L

The parameter LP2L for a saturation level *L* ([dB]) can be calculated by the following formula:

$$LP2L = \frac{2 \times L}{5 \times \log 2}$$

Reset and default value for *L*: 20 dB

LIM

The parameter LIM for a minimum signal level *L* ([dB], relative to PCM max. value) can be calculated by the following formula:

$$LIM = \frac{2 \times (96.3 - L)}{5 \times \log 2}$$

Reset and default value for *L*: -52 dB

65_h SSDX2 Speech Detector (Transmit) 2

15		0
LP1	0	OFF

Reset Value

1006_h

LP1

The parameter LP1 for a time *t* ([ms]) can be calculated by the following formula:

$$LP1 = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

Reset and default value for *t*: 4 ms

OFF

The parameter OFF for a level offset of *O* ([dB]) can be calculated by the following formula:

$$OFF = \frac{2 \times O}{5 \times \log 2}$$

Reset and default value for *O*: 4.5 dB

66_h SSDX3 Speech Detector (Transmit) 3

15		0
PDN	LP2N	

Reset Value

$C0C0_h$

PDN

The parameter PDN for a time *t* ([ms]) can be calculated by the following formula:

$$PDN = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

Reset and default value for *t*: 32 ms

LP2N

The parameter LP2N for a time *t* ([ms]) can be calculated by the following formula:

$$LP2N = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

Reset and default value for *t*: 32 ms

67_h SSDX4 Speech Detector (Transmit) 4

15		0
PDS	0	LP2S

Reset Value

9428_h

PDS

The parameter PDS for a time *t* ([ms]) can be calculated by the following formula:

$$PDS = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

Reset and default value for *t*: 102 ms

LP2S

The parameter LP2S for a time *t* ([ms]) can be calculated by the following formula:

$$LP2S = \frac{262144}{t}$$

Reset and default value for *t*: 6.5 s

68_h SSDR1 Speech Detector (Receive) 1

15			0
0	LP2L	0	LIM

Reset Value

1437_h

LP2L

The parameter LP2L for a saturation level *L* ([dB]) can be calculated by the following formula:

$$LP2L = \frac{2 \times L}{5 \times \log 2}$$

Reset and default value for *L*: 15 dB

LIM

The parameter LIM for a minimum signal level *L* ([dB], relative to PCM max. value) can be calculated by the following formula:

$$LIM = \frac{2 \times (96.3 - L)}{5 \times \log 2}$$

Reset and default value for *L*: -55 dB

69_h SSDR2 Speech Detector (Receive) 2

15		0
LP1	0	OFF

Reset Value

1006_h

LP1

The parameter LP1 for a time *t* ([ms]) can be calculated by the following formula:

$$LP1 = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

Reset and default value for *t*: 4 ms

OFF

The parameter OFF for a level offset of *O* ([dB]) can be calculated by the following formula:

$$OFF = \frac{2 \times O}{5 \times \log 2}$$

Reset and default value for *O*: 4.5 dB

$6A_h$ SSDR3 Speech Detector (Receive) 3

15	0
PDN	LP2N

Reset Value

$C0C0_h$

PDN

The parameter PDN for a time *t* ([ms]) can be calculated by the following formula:

$$PDN = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

Reset and default value for *t*: 32 ms

LP2N

The parameter LP2N for a time *t* ([ms]) can be calculated by the following formula:

$$LP2N = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

Reset and default value for *t*: 32 ms

$6B_h$ SSDR4 Speech Detector (Receive) 4

15		0
PDS	0	LP2S

Reset Value

9428_h

PDS

The parameter PDS for a time *t* ([ms]) can be calculated by the following formula:

$$PDS = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

Reset and default value for *t*: 102 ms

LP2S

The parameter LP2S for a time *t* ([ms]) can be calculated by the following formula:

$$LP2S = \frac{262144}{t}$$

Reset and default value for *t*: 6.5 s

$6C_h$ SSCAS1 Speech Comparator (Acoustic Side) 1

15		0
G	ET	

Reset Value

0800_h

G

The parameter G for a gain *A* ([dB]) can be calculated by the following formula:

$$G = \frac{2 \times A}{5 \times \log 2}$$

Reset and default value for *A*: 6 dB

Note: The parameter G is interpreted in two's complement.

ET

The parameter ET for a time *t* ([ms]) can be calculated by the following formula:

$$ET = \frac{t}{4}$$

Reset and default value for *t*: 0 ms

$6D_h$ SSCAS2 Speech Comparator (Acoustic Side) 2

15		0
0	GDN	PDN

Reset Value

1006_h

GDN

The parameter GDN for a gain *G* ([dB]) can be calculated by the following formula:

$$GDN = \frac{4 \times G}{5 \times \log 2}$$

Reset and default value for *G*: 6 dB

PDN

The parameter PDN for a decay rate *R* ([ms/dB]) can be calculated by the following formula:

$$PDN = \frac{64}{5 \times \log 2 \times R}$$

Reset and default value for *R*: 7 ms/dB

$6E_h$ SSCAS3 Speech Comparator (Acoustic Side) 3

15		0
0	GDS	PDS

Reset Value

1006_h

GDS

The parameter GDS for a gain *G* ([dB]) can be calculated by the following formula:

$$GDS = \frac{4 \times G}{5 \times \log 2}$$

Reset and default value for *G*: 6 dB

PDS

The parameter PDS for a decay rate *R* ([ms/dB]) can be calculated by the following formula:

$$PDS = \frac{64}{5 \times \log 2 \times R}$$

Reset and default value for *R*: 7 ms/dB

$6F_h$ SSCLS1 Speech Comparator (Line Side) 1

15		0
G	ET	

Reset Value

0000_h

G

The parameter G for a gain *A* ([dB]) can be calculated by the following formula:

$$G = \frac{2 \times A}{5 \times \log 2}$$

Reset and default value for *A*: 0 dB

Note: The parameter G is interpreted in two's complement.

ET

The parameter ET for a time t ([ms]) can be calculated by the following formula:

$$ET = \frac{t}{4}$$

Reset and default value for *t*: 0dB

70_h SSCLS2 Speech Comparator (Line Side) 2

15		0
0	GDN	PDN

Reset Value

2002_h

GDN

The parameter GDN for a gain *G* ([dB]) can be calculated by the following formula:

$$GDN = \frac{4 \times G}{5 \times \log 2}$$

Reset and default value for *G*: 12 dB

PDN

The parameter PDN for a decay rate *R* ([ms/dB]) can be calculated by the following formula:

$$PDN = \frac{64}{5 \times \log 2 \times R}$$

Reset and default value for *R*: 21.3 ms/dB

71_h SSCLS3 Speech Comparator (Line Side) 3

15		0
0	GDS	PDS

Reset Value

2002_h

GDS

The parameter GDS for a gain *G* ([dB]) can be calculated by the following formula:

$$GDS = \frac{4 \times G}{5 \times \log 2}$$

Reset and default value for *G*: 12 dB

PDS

The parameter PDS for a decay rate *R* ([ms/dB]) can be calculated by the following formula:

$$PDS = \frac{64}{5 \times \log 2 \times R}$$

Reset and default value for *R*: 21.3 ms/dB

72_h SATT1 Attenuation Unit 1

15		0
0	ATT	SW

Reset Value

$2C6A_h$

ATT

The parameter ATT for an attenuation *A* ([dB]) can be calculated by the following formula:

$$ATT = \frac{2 \times A}{5 \times \log 2}$$

Reset and default value for *A*: 36 dB

SW

The parameter SW for a switching rate *R* ([ms/dB]) can be calculated by the following formula:

$$SW = \begin{cases} 128 + \frac{1}{5 \times \log 2 \times R} & ;0.0053 < R < 0.66 \\ \frac{16}{5 \times \log 2 \times R} & ;0.66 < R < 0.63 \end{cases}$$

Reset and default value for *R*: 0.1 ms/dB

73_h SATT2 Attenuation Unit 2

15		0
TW	DS	

Reset Value

$0AFF_h$

TW

The parameter TW for a time *t* ([ms]) can be calculated by the following formula:

$$TW = \frac{t}{16}$$

DS

The parameter DS for a decay rate *R* ([ms/dB]) can be calculated by the following formula:

$$DS = \frac{5 \times \log2 \times R - 1}{4}$$

Note: The value 0xFF for the parameter DS specifies an infinite decay rate. Therefore the speakerphone will not return to the idle state in the absence of speech signals. It will remain in the current state until a speech signal is detected and a state change is necessary. This is also the reset and default value.

74_h SAGX1 Automatic Gain Control (Transmit) 1

15		0
AG_INIT	0	COM

Reset Value

$005F_h$

AG_INIT

The parameter AG_INIT for a gain *G* ([dB]) can be calculated by the following formula:

$$AG\_INIT = \frac{-2 \times G}{5 \times \log 2}$$

Reset and default value for *G*: 0 dB

Note: This parameter is interpreted in two's complement.

COM

The threshold COM for a level *L* ([dB]) can be calculated by the following formula:

$$COM = \frac{2 \times (96.3 + L)}{5 \times \log 2}$$

Reset and default value for *L*: -24 dB

75_h SAGX2 Automatic Gain Control (Transmit) 2

15		0
0	AG_ATT	SPEEDH

Reset Value

$7FFF_h$

AG_ATT

The parameter AG_ATT for an attenuation *A* ([dB]) can be calculated by the following formula:

$$AG\_ATT = \frac{-2 \times A}{5 \times \log 2}$$

Reset and default value for *G*: 96 dB

SPEEDH

The parameter SPEEDH for the regulation speed *R* (ms/dB) can be calculated by the following formula:

$$SPEEDH = \frac{512}{D \times R}$$

The variable D denotes the aberration ([dB]).

Reset and default value for *R*: 2 ms/dB

76_h SAGX3 Automatic Gain Control (Transmit) 3

15	0
AG_GAIN	SPEEDL

Reset Value

0014_h

AG_GAIN

The parameter AG_GAIN for a gain *G* ([dB]) can be calculated by the following formula:

$$AG\_GAIN = \frac{-2 \times G}{5 \times \log 2}$$

Reset and default value for *G*: 0 dB

SPEEDL

The parameter SPEEDL for the regulation speed *R* ([ms/dB]) can be calculated by the following formula:

$$SPEEDL = \frac{4096}{D \times R}$$

The variable D denotes the aberration ([dB]).

Reset and default value for *R*: 160 ms/dB

77_h SAGX4 Automatic Gain Control (Transmit) 4

15			0
0	NOIS	0	LPA

Reset Value

4020_h

NOIS

The parameter NOIS for a threshold level *L* ([dB]) can be calculated by the following formula:

$$NOIS = \frac{2 \times (96.3 + L)}{5 \times \log 2}$$

Reset and default value for *L*: -48 dB

LPA

The parameter LPA for a low pass time constant *T* ([ms]) can be calculated by the following formula:

$$LPA = \frac{16}{T}$$

Reset and default value for *T*: 2 ms

78_h SAGX5 Automatic Gain Control (Transmit) 5

15								0
AG_CUR	0	0	0	0	0	0	0	0

AG_CUR

The current gain *G* of the AGCX can be derived from the parameter Parameter AG_CUR by the following formula:

$$G = \frac{-5 \times \log 2 \times AG\_CUR}{2}$$

Note: AG_CUR is interpreted in two's complement.

79_h SAGR1 Automatic Gain Control (Receive) 1

15	0
AG_INIT	COM

Reset Value
$006F_h$

AG_INIT

The parameter AG_INIT for a gain *G* ([dB]) can be calculated by the following formula:

$$\text{AG\_INIT} = \frac{-2 \times G}{5 \times \log 2}$$

This parameter is interpreted in two's complement.

Reset and default value for *G*: 0 dB

COM

The parameter COM for a threshold *L* ([dB]) can be calculated by the following formula:

$$\text{COM} = \frac{2 \times (96.3 + L)}{5 \times \log 2}$$

This parameter is interpreted in two's complement.

Reset and default value for *L*: -12 dB

$7A_h$ SAGR2 Automatic Gain Control (Receive) 2

15		0
0	AG_ATT	SPEEDH

Reset Value

$7FFF_h$

AG_ATT

The parameter AG_ATT for a gain *G* ([dB]) can be calculated by the following formula:

$$AG\_ATT = \frac{-2 \times G}{5 \times \log 2}$$

Reset and default value for *G*: 96 dB

SPEEDH

The parameter SPEEDH for the regulation speed *R* ([ms/dB]) can be calculated by the following formula:

$$SPEEDH = \frac{512}{D \times R}$$

The variable D denotes the aberration ([dB]).

Reset and default value for *R*: 2 ms/dB

$7B_h$ SAGR3 Automatic Gain Control (Receive) 3

15	0
AG_GAIN	SPEEDL

Reset Value

$001A_h$

AG_GAIN

The parameter AG_GAIN for a gain *G* ([dB]) can be calculated by the following formula:

$$AG\_GAIN = \frac{-2 \times G}{5 \times \log 2}$$

Reset and default value for *G*: 0 dB

SPEEDL

The parameter SPEEDL for the regulation speed *R* ([ms/dB]) can be calculated by the following formula:

$$SPEEDL = \frac{4096}{D \times R}$$

The variable D denotes the aberration ([dB]).

Reset and default value for *R*: 200 ms/dB

$7C_h$ SAGR4 Automatic Gain Control (Receive) 4

15			0
0	NOIS	0	LPA

Reset Value

4020_h

NOIS

The parameter NOIS for a threshold level *L* ([dB]) can be calculated by the following formula:

$$NOIS = \frac{2 \times (96.3 + L)}{5 \times \log 2}$$

Reset and default value for *L*: -48 dB

LPA

The parameter LPA for a low pass time constant *T* ([ms]) can be calculated by the following formula:

$$LPA = \frac{16}{T}$$

Reset and default value for *T*: 2 ms

$7D_h$ SAGR5 Automatic Gain Control (Receive) 5

15								0
AG_CUR	0	0	0	0	0	0	0	0

AG_CUR

The current gain *G* of the AGCR can be derived from the parameter Parameter AG_CUR by the following formula:

$$G = \frac{-5 \times \log 2 \times AG\_CUR}{2}$$

AG_CUR is interpreted in two's complement.

$7E_h$ SLGA Line Gain

15			0
0	LGAR	0	LGAX

Reset Value

4040_h

LGAR

The parameter LGAR for a gain *G* ([dB]) is given by the following formula:

$$LGAR = 128 \times 10^{(G-12)/20}$$

Reset and default value for *G*: 6 dB

LGAX

The parameter LGAX for a gain *G* ([dB]) is given by the following formula:

$$LGAX = 128 \times 10^{(G-12)/20}$$

Reset and default value for *G*: 6 dB

$7F_h$ SAELEN Acoustic Echo Cancellation Length

15							0
0	0	0	0	0	0	FBLEN	

Reset Value

0200_h

FBLEN

LEN denotes the number of FIR-taps used in fullband mode.

80_h SAEAW Acoustic Echo Cancellation Adaptation Window

15							0
0	0	0	0	0	0	0	FBADA

Reset Value

0100_h

FBADA

FBADA denotes the number of FIR-taps changed adaptively in full band mode.

81_h SAEEL Acoustic Echo Cancellation Reported Attenuation Limit

15		0
0	AECLIM	

Reset Value
$7FFFF_h$

AECLIM

The maximum value for an attenuation *A* ([dB]) of the echo cancellation unit reported to the echo suppression unit given by the following formula:

$$\text{AECLIM} = \frac{512 \times A}{5 \times \log 2}$$

Reset and default value is the maximum value for *A*.

82_h SAEDTR Acoustic Echo Cancellation Double Talk Reduction

15		0
0	AECATT	

Reset Value
1400_h

AECATT

The parameter AECATT for an attenuation reduction *A* ([dB]) during double talk is given by the following formula:

$$AECATT = \frac{512 \times A}{5 \times \log 2}$$

Reset and default value for *A*: 15 dB

83_h SAEDTL Acoustic Echo Cancellation Double Talk Limit

15	0
0	AECDTM

Reset Value
1800_h

AECDTM

The parameter AECDTM for a minimum energy *A* ([dB]) during double talk is given by the following formula:

$$AECDTM = \frac{512 \times A}{5 \times \log 2}$$

Reset and default value for *A*: 16 dB

84_h SAEDTI Acoustic Echo Cancellation Double Talk Increment

15		0
0	AECDTI	

Reset Value
0100_h

AECDTI

AECDTI determines the rate the attenuation reduction RED ([dB/s]) of the AEC is incremented with when double talk is detected:

$$AECDTI = \frac{RED}{8.192}$$

Reset and default value for *A*: 31.6 dB/s

85_h SAEDTD Acoustic Echo Cancellation Double Talk Decrement

15		0
0	AECDTD	

Reset Value
0062_h

AECDTD

AECDTD determines the rate the attenuation reduction *RED* of the AEC is decremented with when double talk is detected:

$$AECDTD = \frac{RED}{8.192}$$

Reset and default value for *RED*: 12 dB/s

86_h SAEWFL Wiener Filter Limit Attenuation

15		0
0	WFATT	

Reset Value
5000_h

AFATT

The parameter WFATT for a maximal attenuation *A* ([dB]) of the Wiener filter is given by the following formula:

$$LIMIT = \frac{512 \times A}{5 \times \log 2}$$

Reset and default value for *A*: 60 dB

87_h SNRATT Noise Reduction Attenuation

15		0
0	NRATT	

Reset Value

2800_h

NRATT Noise Reduction Attenuation

The maximum attenuation *A* of frequencies with a high noise to signal ratio performed by the noise reduction unit can be calculated by the following formula:

$$NRATT = 32768 \times 10^{-A\frac{dB}{20}}$$

Reset and default value for *A*: 15 dB

88_h SNRLNL Noise Reduction Lower Noise Limit

15		0
0	NRLOW	

Reset Value

4000_h

NRLOW Noise Reduction Lower Limit

The level *L* ([dB]) of the noise to deactive the coupling between the Wiener filter and the noise reduction unit can be calculated by the following formula:

$$NRLOW = \frac{512 \times (96.3 + L)}{5 \times \log 2}$$

Reset and default value for *L*: -48 dB

89_h SNRUNL Noise Reduction Upper Noise Limit

15		0
0	NRUP	

Reset Value

5000_h

NRUP Noise Reduction Upper Limit

The level L ([dB]) of the noise to active the coupling between the Wiener filter and the noise reduction unit can be calculated by the following formula:

$$NRUP = \frac{512 \times (96.3 + L)}{5 \times \log 2}$$

Reset and default value for *L*: -36 dB

90_h SCSD1 Speech Detector (Comfort Noise) 1

15			0
0	LP2L	0	LIM

Reset Value

$7F29_h$

LP2L

The parameter LP2L for a saturation level *L* ([dB]) can be calculated by the following formula:

$$LP2L = \frac{2 \times L}{5 \times \log 2}$$

Reset and default value for *L*: 25 dB

LIM

The parameter LIM for a minimum signal level *L* ([dB], relative to PCM max. value) can be calculated by the following formula:

$$LIM = \frac{2 \times (96.3 + L)}{5 \times \log 2}$$

Reset and default value for *L*: -65 dB

91_h SCSD2 Speech Detector (Comfort Noise) 2

15		0
LP1	0	OFF

Reset Value

1006_h

LP1

The parameter LP1 for a time *t* ([ms]) can be calculated by the following formula:

$$LP1 = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

Reset and default value for *t*: 4 ms

OFF

The parameter OFF for a level offset of *O* ([dB]) can be calculated by the following formula:

$$OFF = \frac{2 \times O}{5 \times \log 2}$$

Reset and default value for *O*: 4.5 dB

92_h SCSD3 Speech Detector (Comfort Noise) 3

15	0
PDN	LP2N

Reset Value

0202_h

PDN

The parameter PDN for a time *t* ([ms]) can be calculated by the following formula:

$$PDN = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

Reset and default value for *t*: 32 ms

LP2N

The parameter LP2N for a time *t* ([ms]) can be calculated by the following formula:

$$LP2N = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

Reset and default value for *t*: 32ms

93_h SCSD4 Speech Detector (Comfort Noise) 4

15		0
PDS	0	LP2S

Reset Value

9457_h

PDS

The parameter PDS for a time *t* ([ms]) can be calculated by the following formula:

$$PDS = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

Reset and default value for *t*: 203 ms

LP2S

The parameter LP2S for a time *t* ([ms]) can be calculated by the following formula:

$$LP2S = \frac{262144}{t}$$

Reset and default value for *t*: 3 s

94_h SCLPT Low Pass Time Constant

15		0
0	TC	

Reset Value

0020_h

TC

The parameter TC for a time constant *t* ([ms]) can be calculated by the following formula:

$$TC = \frac{65534}{t}$$

Reset and default value for *t*: 2 s

Note: TC must be greater than zero.

95_h SCCR Correlation

15			0
0	1	CORR	

Reset Value

$7C28_h$

CORR

The parameter CORR for a linear correlation *C* is given by:

$$CORR = 32768 \times C$$

Reset and default value for *C*: 0.97

Note: CORR must be greater than 0x4FFF. This means that a 1 has to be programmed to bit 14.

96_h SCCRN Correlation Noise Threshold

15		0
0	NTH	

Reset Value
3000_h

NTH

The parameter NTH for a threshold *L* ([dB], relative to PCM max. value) can be calculated by the following formula:

$$NTH = \frac{512 \times (96.3 + L)}{5 \times \log 2}$$

Reset and default value for *L*: -60 dB

97_h SCCRS Correlation Sensitivity

15					0
1	1	1	1	CS	
Reset Value					
$FCCD_h$					

CS

The parameter CS for a sensitivity *SE* ([1/dB]) can be calculated by the following formula:

$$CS = 655350 \times \log(2) \times SE$$

Reset and default value for *SE*: -0.00425 1/dB

Note: The parameter CS is interpreted in two's complement.

Note: The bits 12 to 15 have to be set to 1.

98_h SCCRL Correlation Limit

15			0
0	1	LIMIT	

Reset Value

$6CCC_h$

LIMIT

The parameter LIMIT for a correlation limit *L* is given by:

$$LIMIT = 32768 \times L$$

Reset and default value for *L*: 0.850 dB

Note: L must be greater than 0x4FFF. Thus, bit 14 must be set to 1.

99_h SCDTN Double Talk Detection Threshold

15		0
0	NTH	

Reset Value

2200_h

NTH

The parameter NTH for a noise threshold *L* ([dB], relative to PCM max. value) can be calculated by the following formula:

$$NTH = \frac{512 \times (96.3 + L)}{5 \times \log 2}$$

Reset and default value for *L*: -60 dB

$9A_h$ SCDTS Double Talk Sensitivity

15					0
1	1	1	1	DTS	

Reset Value

$FD9A_h$

DTS

The parameter DTS for a sensitivity *SE* ([1/dB]) can be calculated by the following formula:

$$S = 2048 \times SE$$

Reset and default value for *SE*: -0.3 dB/dB

Note: The parameter SE is interpreted in two's complement.

Note: The bits 12 to 15 have to be set to 1.

$9B_h$ SCDTL Double Talk Limit

15		0
0	LIMIT	

Reset Value

1000_h

LIMIT

The parameter LIMIT for a level *L* ([dB], relative to PCM max. value) can be calculated by the following formula:

$$\text{LIMIT} = \frac{512 \times L}{5 \times \log 2}$$

Reset and default value for *L*: 12 dB

Note: LIMIT must be greater than 0x7FF.

$9C_h$ SCATTN Attenuation Noise

15		0
0	NTH	

Reset Value

3000_h

NTH

The parameter NTH for a threshold *L* ([dB], relative to PCM max. value) can be calculated by the following formula:

$$NTH = \frac{512 \times (96.3 + L)}{5 \times \log 2}$$

Reset and default value for *L*: -60 dB

$9D_h$ SCATTS Attenuation Sensitivity

15		0
0	AS	

Reset Value

0800_h

AS

The parameter AS for a sensitivity *SE* ([1/dB]) can be calculated by the following formula:

$$AS = 2048 \times SE$$

Reset and default value for *SE*: 1 dB/dB

$9E_h$ SCATTL Attenuation Limit

15		0
0	LIMIT	

Reset Value
3800_h

LIMIT

The parameter LIMIT for a level *L* ([dB], relative to PCM max. value) can be calculated by the following formula:

$$LIMIT = \frac{512 \times L}{5 \times \log 2}$$

Reset and default value for *L*: 42 dB

Note: LIMIT must be greater than 0x7FF.

9F$_h$ SCLSPN Loudspeaker Noise

15		0
0	NTH	

Reset Value

442A$_h$

NTH

The parameter NTH for a threshold *L* ([dB], relative to PCM max. value) can be calculated by the following formula:

$$NTH = \frac{512 \times (96.3 + L)}{5 \times \log 2}$$

Reset and cautious value for *L*: -44 dB

$A0_h$ SCLSPS Loudspeaker Sensitivity

15		0
0	GS	

Reset Value

0200_h

GS

The parameter GS for a sensitivity *SE* ([1/dB]) can be calculated by the following formula:

$$GS = 2048 \times SE$$

Reset and cautious value for *SE*: 0.25 dB/dB

$A1_h$ SCLSPL Loudspeaker Limit

15		0
0	LIMIT	

Reset Value
0800_h

LIMIT

The parameter LIMIT for a level *L* ([dB], relative to PCM max. value) can be calculated by the following formula:

$$LIMIT = \frac{512 \times L}{5 \times \log 2}$$

Reset and cautious value for *L*: 6 dB

Note: LIMIT must be greater than 0x7FF.

$A2_h$ SCCN1 Comfort Noise Constant Level

15		0
0	CONST	

Reset Value
0000_h

CONST

The parameter CONST controls the level of the comfort noise. The range is from 0 (off) to 32767 (max.). The parameter has linear behavior.

$A3_h$ SCCN2 Comfort Noise Multiplication Factor

15		0
0	FAC	

Reset Value

0600_h

FAC

The parameter FAC for a factor *f* can be calculated by the following formula:

$$FAC = 2048 \times f$$

$A4_h$ SCCN3 Comfort Noise Low Pass

15		0
0	LP	

Reset Value

0800_h

LP

The parameter LP for a time constant *TS* ([1/ms]) can be calculated by the following formula:

$$LP = \frac{983.025}{TS}$$

A6$_h$ NRCTL Noise Reduction Control

15										0
EN	MD	0	0	0	0	0	0	0	0	I1
Reset Value										
0	0	0	0	0	0	0	0	0	0	0

EN Noise Reduction Enable

0: Disabled

1: Enabled

MD Speakerphone Mode Dependence

14	13	Speakerphone Mode	Description
0	0	Fullband mode one	Number of taps must be restricted to 447
		Fullband mode two	Not allowed
		Subband mode	Not allowed
0	1	Fullband mode one	Not allowed
		Fullband mode two	Number of taps must be reduced to 414
		Subband mode	Mode "RNR" must be selected
1	0	Fullband mode one	There must be disabled (ISDN mode): DTMF, AT, CPT, UT detectors, CID, NA, CN and LEC
		Fullband mode two	Number of taps up to 645, but there must be disabled (ISDN mode): DTMF, AT, CPT, UT detectors, CID, NA, CN and LEC
		Subband mode	Subband modes "Normal", "Reduced" or "RNR" are allowed, but there must be disabled (ISDN mode): DTMF, AT, CPT, UT detectors, CID, NA, CN and LEC
1	1		reserved

I1 Input signal selection

$A7_h$ NRATT Noise Reduction Attenuation

15		0
0	NRATT	

NRATT Noise Reduction Attenuation

The maximum attenuation *A* ([dB]) of noisy frequencies performed by the noise reduction unit can be calculated by the following formula:

$$NRATT = 32768 \times 10^{-\frac{A}{20}}$$

$A8_h$ UTDCTL Universal Tone Detector Control

15											0
EN	0	0	0	0	0	0	0	0	0	0	I1
Reset Value											
0	0	0	0	0	0	0	0	0	0	0	0

EN **UTD Detector Enable**

0: Disabled

1: Enabled

I1 **Input signal selection**

$A9_h$ UTDCF Center Frequency for UTD

15															0
CF															

CF

The parameter CF for a center frequency *f* (Hz) can be calculated by the following formula:

$$CF = 32768 \times \cos\left(\frac{2 \times \pi \times f}{8000}\right)$$

AA_h UTDBW Band Width for UTD

15		0
0	BW	

BW

The parameter BW for a band width *B* (Hz) can be calculated by the following formula:

$$BW = 65536 \times \frac{\tan(\pi \times B/8000)}{1 + \tan(\pi \times B/8000)}$$

AB_h UTDLIM Limiter Limit for UTD

15		0
0	LIM	

LIM Signal Limit

The parameter LIM for a limit of *L[dB]* can be calculated by the following formula:

$$LIM = 32768 \times 10^{L/20}$$

AC_h UTDLEV Minimal Signal Level for UTD

15		0
0	LEV	

LEV Minimal level of signal

The parameter LEV for a minimum in-band signal level of *L[dB]* can be calculated by the following formula:

$$LEV = 32768 \times 10^{L/20}$$

AD_h UTDDLT Minimum Difference for UTD

15															0
DELTA															

DELTA Minimal difference between in-band signal and out-of-band signal

The parameter DELTA for a signal difference of *d [dB]* can be calculated by the following formula:

$$DELTA = sgn(d) \times 32768 \times 10^{-(|d|)/20}$$

AE_h UTDTMT Tone Times for UTD

15	0
TTONE	TB1

TTONE Minimum Time for Activation

The parameter TTONE for a minimal activation time *t [ms]* can be calculated by the following formula:

$$TTONE = \frac{t}{8}$$

TB1 Maximum Break Time for TTONE

The parameter TB1 for a maximum break time is given in milliseconds.

AF_h UTDTMG Gap Times for UTD

15	0
TGAP	TB2

TGAP Minimum Time for Deactivation

The parameter TGAP for a minimal deactivation time *t [ms]* can be calculated by the following formula:

$$TGAP = \frac{t}{8}$$

TB2 Maximum Break Time for TGAP

The parameter TB2 for a maximum break time is given in milliseconds.

$B0_h$ CIDMF1 Caller ID Message Format

15															0
0															MF
Reset Value															
0															0

MF Message Format

Valid start byte.

$B1_h$ CIDMF2 Caller ID Message Format

15															0
0															MF
Reset Value															
0															0

MF Message Format

Valid start byte.

$B2_h$ CIDMF3 Caller ID Message Format

15															0
0															MF
Reset Value															
0															0

MF Message Format

Valid start byte.

$B3_h$ CIDMF4 Caller ID Message Format

15															0
0															MF
Reset Value															
0															0

MF Message Format

Valid start byte.

$B4_h$ CIDMF5 Caller ID Message Format

15	0
0	MF
Reset Value	
0	0

MF Message Format

Valid start byte.

$B5_h$ CIDMF6 Caller ID Message Format

15	0
0	MF
Reset Value	
0	0

MF Message Format

Valid start byte.

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias	T_A	-20 to 85	°C
Storage temperature	T_{STG}	– 65 to125	°C
Supply Voltage	V_{DD}	-0.5 to 4.2	V
Supply Voltage	V_{DDA}	-0.5 to 4.2	V
Voltage of pin with respect to ground: $XTAL_1$, $XTAL_2$	V_S	-0.3 to 3.6	V
Voltage on any pin with respect to ground (except $XTAL_1$, $XTAL_2$)	V_S	- 0.5 to 5.5[1)]	V

[1)] The difference from the minumum to the maximum value for $V_S/V_{DD}/V_{SS}$ at any pin must never exceed 5.5 V.

ESD integrity (according MIL-Std. 883D, method 3015.7): 2 kV

Note: Conditions: Maximum ratings are stress ratings only, and functional operation and reliability under conditions beyond those defined in the "recommended operating conditions" is not guaranteed. Stresses above the maximum ratings are likely to cause permant damage.

6.2 DC Characteristics

V_{DD}/V_{DDA} = 3.3 V ± 0.3 V; V_{SS}/V_{SSA} = 0 V; T_A = 0 to 70 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Input leakage current	I_{IL}	– 1.0		1.0	µA	0 V ≤ V_{IN} ≤ V_{DD}
H-input level (except $XTAL_1$)	V_{IH1}	2.0		5.5	V	
H-input level ($XTAL_1$)	V_{IH2}	0.8 V_{DD}		V_{DDA} + 0.3	V	
L-input level (except $XTAL_1$)	V_{IL1}	– 0.3		0.8	V	
L-input level ($XTAL_1$)	V_{IL2}	– 0.3		0.2 V_{DDA}	V	
H-output level (except DU/DX, DD/DR, GP_0-GP_{15}, SPS_0, SPS_1, $\overline{INT}$)	V_{OH1}	V_{DD} – 0.45			V	I_O = 2 mA
H-output level (SPS_0, SPS_1, SDX, GP_0-GP_{15}, $\overline{INT}$)	V_{OH2}	V_{DD} – 0.6			V	I_O = 2mA
H-output level (DU/DX, DD/DR)	V_{OH4}	V_{DD} – 0.6			V	I_O = 7 mA

V_{DD}/V_{DDA} = 3.3 V ± 0.3 V; V_{SS}/V_{SSA} = 0 V; T_A = 0 to 70 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
L-output level (except DU/DX, DD/DR, MA_0-MA_{15})	V_{OL1}			0.45	V	I_O = – 2 mA
L-output level (GP_0-GP_{15})	V_{OL2}			0.45	V	I_O = – 5 mA
L-output current (GP_0-GP_{15}) (after reset)	I_{LO}	55	102	160	µA	RST=1
L-output level (DU/DX, DD/DR)	V_{OL3}			0.45	V	I_O = – 7 mA
Input capacitance	C_I			10	pF	
Output capacitance	C_O			15	pF	
V_{DD}+V_{DDA} supply current (powerdown)	I_{DDS1}		10	50	µA	
V_{DD}+V_{DDA} supply current (operating)	I_{DDO}		40	70	mA	V_{DD} = 3.3 V

6.3 AC Characteristics

Digital inputs are driven to 2.4 V for a logical “1” and to 0.45 V for a logical “0”. Timing measurements are made at 2.0 V for a logical “1” and 0.8 V for a logical “0”. The AC-testing input/output waveforms are shown below.

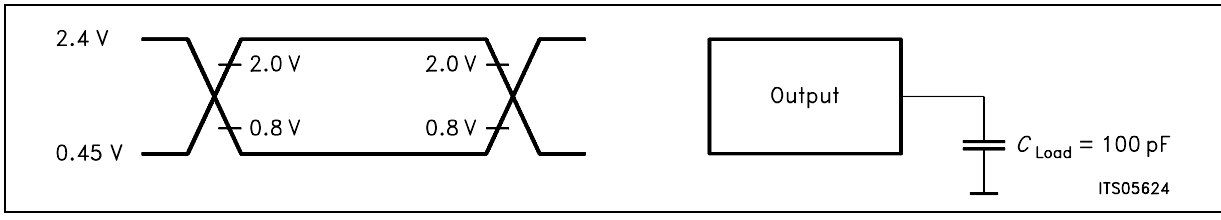


Figure 67 Input/Output Waveforms for AC-Tests

DTMF Detector

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Frequency deviation accept		-1.5		1.5	%	
Frequency deviation reject		3.5		-3.5	%	
Acceptance level		-45		0	dB	rel. to max. PCM
Rejection level				-50	dB	rel. to max. PCM
Twist deviation accept		+/-2		+/-8	dB	programmable
Noise Tolerance				12	dB	
Signal duration accept		40			ms	
Signal duration reject				19	ms	
Gap duration accept				23	ms	

Caller ID Decoder

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Frequency deviation accept		-2		2	%	
Acceptance level		-45		0	dB	rel. to max. PCM
Transmission rate		1188	1200	1212	baud	
Noise Tolerance				12	dB	

Echo Cancellation Unit (subband mode)

subband (Hz)		filter length (ms)				
lower limit	upper limit	RNR	reduced	analog	ISDN	enhanced
0	250	45	60	97	118	126
250	750	50	66	111	159	159
750	1250	50	64	87	109	123
1250	1750	45	60	60	76	88
1750	2250	40	54	60	76	88
2250	2750	36	48	57	72	82
2750	3250	34	42	30	43	54
3250	3750	33	42	30	43	54

Alert Tone Detector

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Frequency deviation accept		-0.5		0.5	%	ATDCTL1:DEV=0
Frequency deviation accept		-1.1		1.1	%	ATDCTL1:DEV=1
Frequency deviation reject		3.5		-3.5	%	
Acceptance level		-40		0	dB	rel. to max. PCM
Rejection level				-5	dB	rel. to acceptance level
Twist deviation accept				+/-7	dB	
Noise Tolerance				20	dB	
Signal duration accept		75			ms	
Gap duration accept		40			ms	ATDCTL1:GT=0
Gap duration accept		12			ms	ATDCTL1:GT=1

Status Register Update Time

The individual bits of the STATUS register may change due to an event (like a recognized DTMF tone) or a command. The timing can be divided into four classes

Table 64 Status Register Update Timing

Class	Timing		Comment
	Min.	Max.	
I	0	0	Immediately after command has been issued
A	0	150 µs	Command has been accepted
D	125 µS	250 µs	Deactivation time after command has been issued
E	-	-	Associated event has happened

With these definitions the timing of the individual bits in the STATUS register can be given as shown in the following table:

Bit	RDY	ABT	CIA	CD	CPT	CNG	DTV	ATV	ATC
0->1	A	E	E	E	E	E	E	E	A
1->0	I	A	A,D	E,D	E,D	D	E,D	E,D	E,D

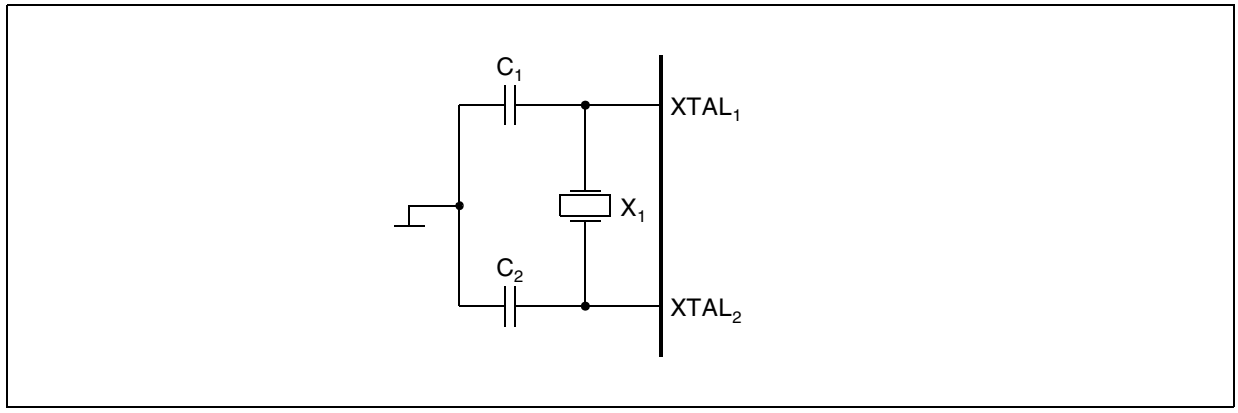


Figure 68 Oscillator Circuit

Recommended / Maximum Values Oscillator Circuit	Value			Unit
	Min	Typ	Max	
Crystal Load Capacity C_L		12		pF
Ext. Capacitors C_1= C_2 @ 34.560MHz	5	8.2	12	pF
Ext. Capacitors C_1= C_2 @ 31.104MHz	5	10	15	pF
Static (parallel) capacitance X_1			7	pF
Resonance resistance X_1			40	Ω
Frequency deviation			500[1)]	ppm

[1)] The frequency deviation must not exceed 500 ppm if AFE clock tracking (bit ACT in register HWCONFIG1) is enabled.

Note: This generally recommended circuity and the values must be verified for each board design. Please use the appropriate Application Note for doing so. Furthermore, the provider of the crystal must be consulted for verification of the circuitry.

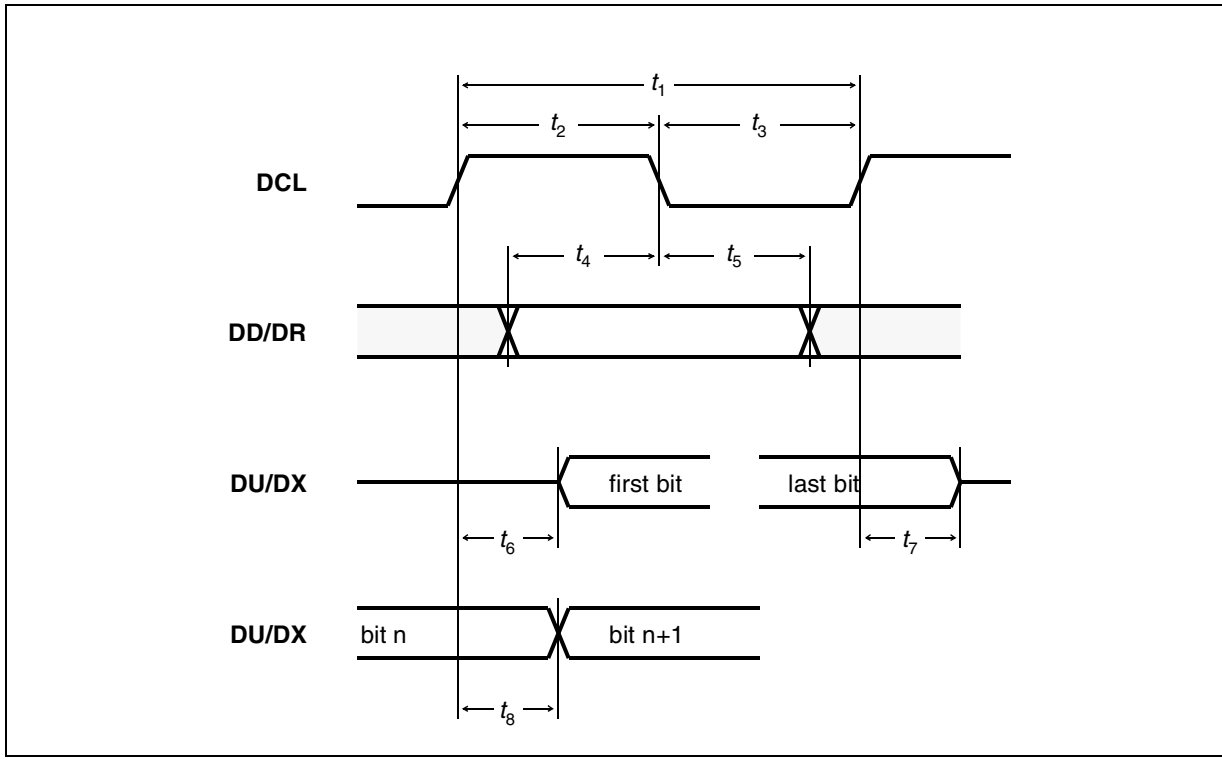


Figure 69 SSDI/IOM®-2 Interface - Bit Synchronization Timing

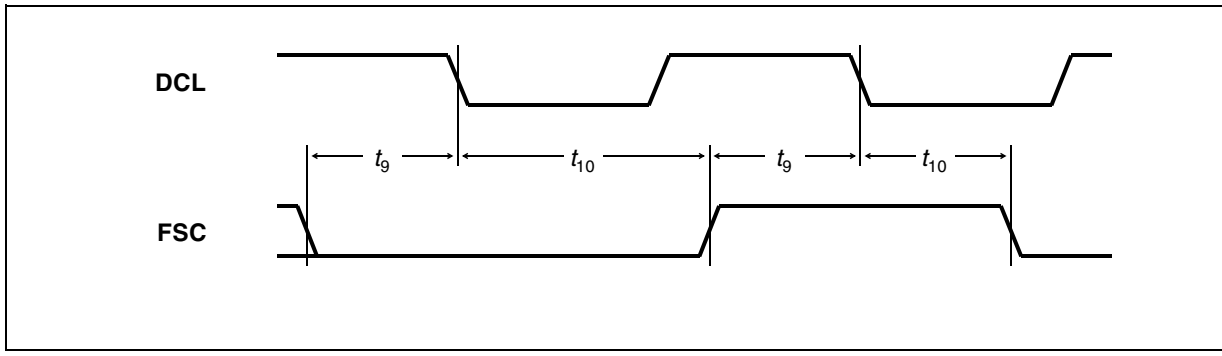


Figure 70 SSDI/IOM®-2 Interface - Frame Synchronization Timing

Parameter SSDI/IOM®-2 Interface	Symbol	Limit values		Unit
		Min	Max	
DCL period	t_1	90		ns
DCL high	t_2	35		ns
DCL low	t_3	35		ns
Input data setup	t_4	20		ns
Input data hold	t_5	10		ns

Parameter SSDI/IOM®-2 Interface	Symbol	Limit values		Unit
		Min	Max	
Output data from high impedance to active (FSC high or other than first timeslot)	t_6		30	ns
Output data from active to high impedance	t_7		30	ns
Output data delay from clock	t_8		30	ns
FSC setup	t_9	40		ns
FSC hold	t_{10}	40		ns
FSC jitter (deviation per frame)		-200	200	ns

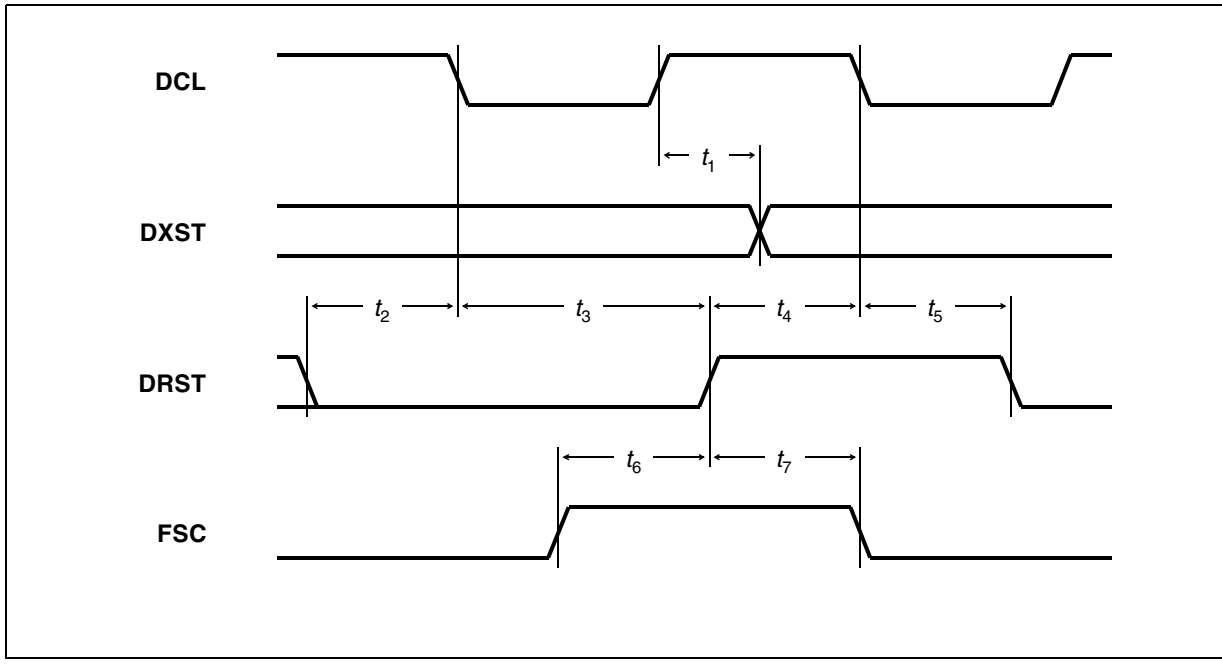


Figure 71 SSDI Interface - Strobe Timing

Parameter SSDI Interface	Symbol	Limit values		Unit
		Min	Max	
DXST delay	t_1		20	ns
DRST inactive setup	t_2	20		ns
DRST inactive hold	t_3	20		ns
DRST active setup	t_4	20		ns
DRST active hold	t_5	20		ns
FSC setup	t_6	8		DCL cycles
FSC hold	t_7	40		ns

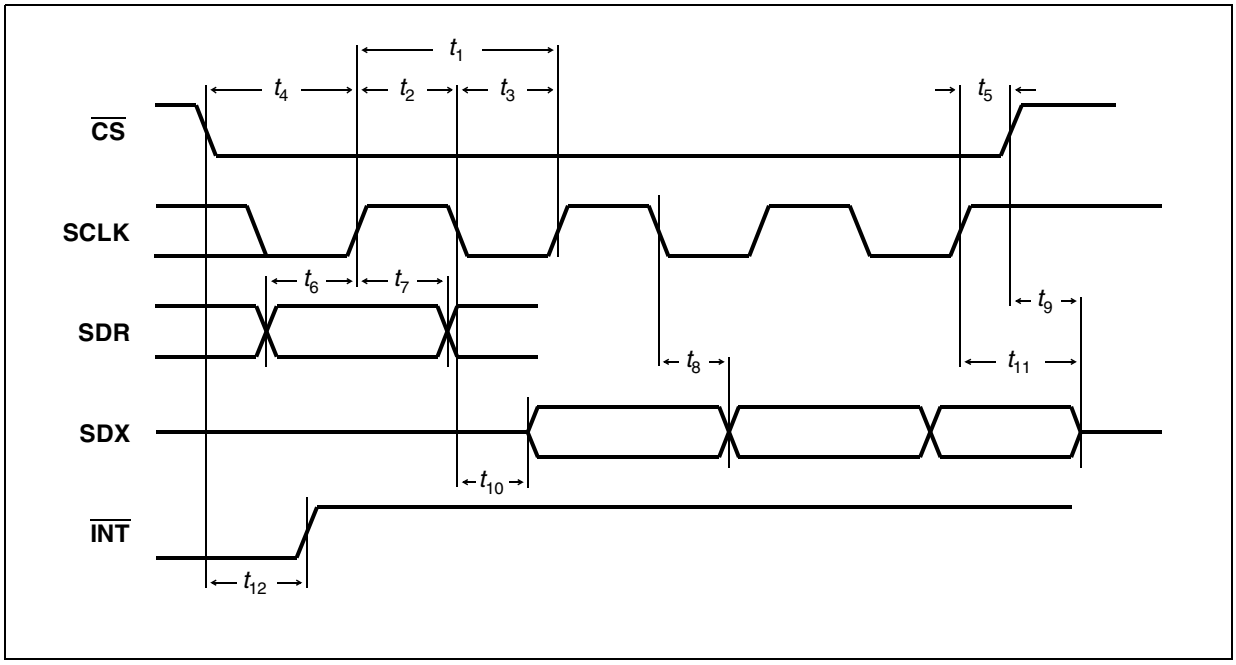


Figure 72 SCI Interface

Parameter SCI Interface	Symbol	Limit values		Unit
		Min	Max	
SCLK cycle time	t_1	500		ns
SCLK high time	t_2	100		ns
SCLK low time	t_3	100		ns
$\overline{CS}$ setup time	t_4	40		ns
$\overline{CS}$ hold time	t_5	10		ns
SDR setup time	t_6	40		ns
SDR hold time	t_7	40		ns
SDX data out delay	t_8		80	ns
$\overline{CS}$ high to SDX tristate	t_9		40	ns
SCLK to SDX active	t_{10}		80	ns
SCLK to SDX tristate	t_{11}		40	ns
$\overline{CS}$ to $\overline{INT}$ delay	t_{12}		80	ns

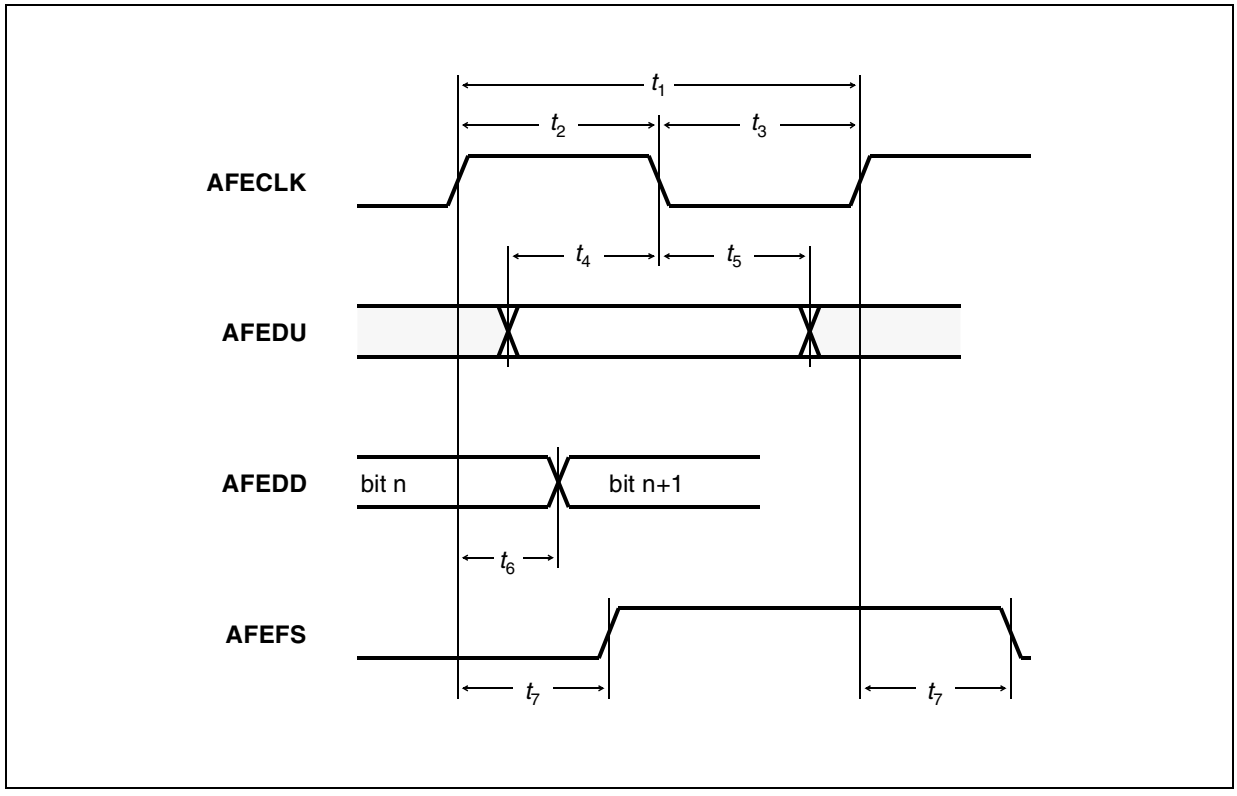


Figure 73 Analog Front End Interface

Parameter AFE Interface	Symbol	Limit values		Unit
		Min	Max	
AFECLK period (HWCONFIG3:CM0=0)	t_1	$13.5*p^{1)}/f_{XTAL}$ -10	$13.5*p/f_{XTAL}$ +10	ns
AFECLK period (HWCONFIG3:CM0=1)	t_1	$4.5*p/f_{XTAL}$ -10	$4.5*p/f_{XTAL}$ +10	ns
AFECLK high	t_2	4		$1/f_{XTAL}$
AFECLK low	t_3	4		$1/f_{XTAL}$
AFEDU setup	t_4	20		ns
AFEDU hold	t_5	20		ns
AFEDD output delay	t_6		30	ns
AFEFS output delay	t_7		30	ns

[1] The factor *p* is determined by HWCONFIG1:XTAL (see register description)

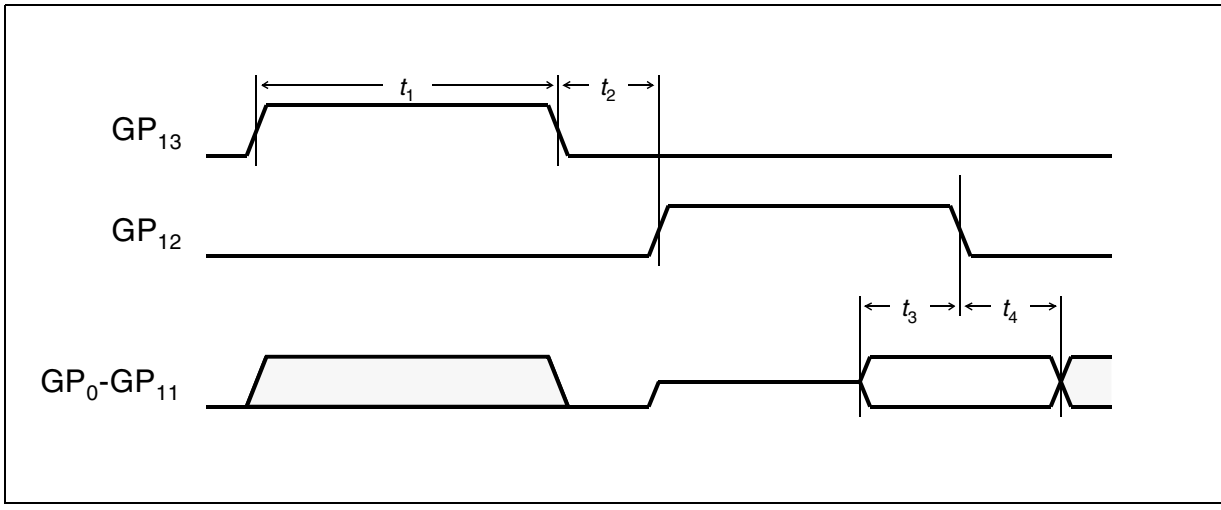


Figure 74 General Purpose Parallel Port - Multiplex Mode

Parameter General Purpose Parallel Port - Multiplex Mode	Symbol	Limit values			Unit
		Min	Typ	Max	
Active time (GP_0-GP_{15})	t_1		2		ms
Gap time (GP_0-GP_{15})	t_2		125		µs
Data setup time	t_3	50			ns
Data hold time	t_4	0			ns

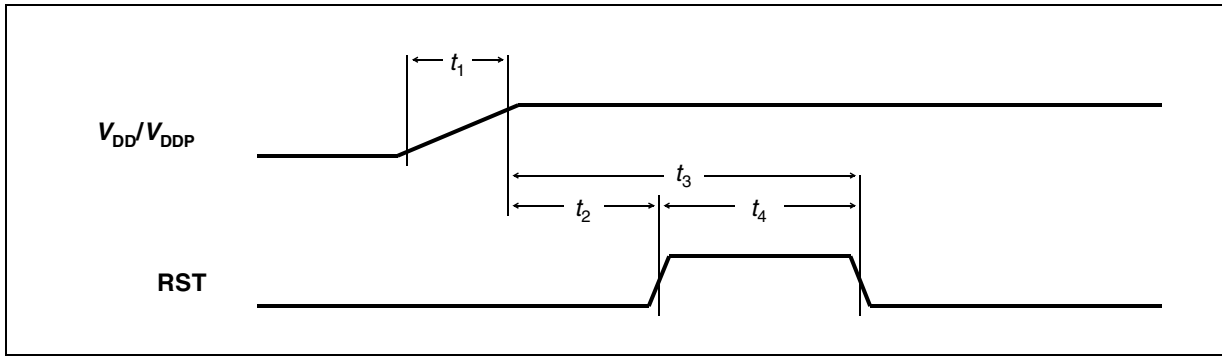
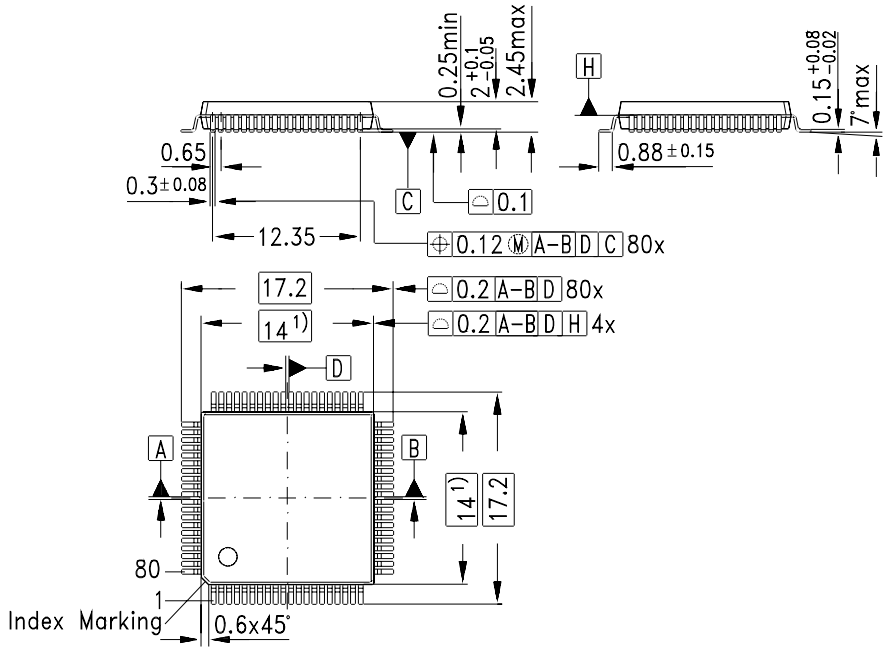


Figure 75 Reset Timing

Parameter Reset Timing	Symbol	Limit values		Unit
		Min	Max	
V_{DD}/V_{DDA} rise time 5%-95%	t_1		20	ms
Supply voltages stable to RST high	t_2	0		ns
Supply voltages stable to RST low	t_3	0.1		ms
RST high time	t_4	1000		ns

7 Package Outlines

Plastic Package, P-MQFP-80 (SMD)
(Plastic Metric Quad Flat Package)



1) Does not include plastic or metal protrusions of 0.25 max per side

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our

SMD = Surface Mounted Device

Dimensions in mm