MCR12DCM, MCR12DCN

Preferred Device

Silicon Controlled Rectifiers

Reverse Blocking Thyristors

Designed for high volume, low cost, industrial and consumer applications such as motor control; process control; temperature, light and speed control.

Features

- Small Size
- Passivated Die for Reliability and Uniformity
- Low Level Triggering and Holding Characteristics
- Epoxy Meets UL 94 V−0 @ 0.125 in
- ESD Ratings: Human Body Model, 3B > 8000 V
  Machine Model, C > 400 V
- Pb−Free Packages are Available

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off−State Voltage (Note 1) (T_J = −40 to 125°C, Sine Wave, 50 to 60 Hz, Gate Open) MCR12DCM MCR12DCN	V_{DRM}, V_{RRM}	 600 800	V
On−State RMS Current (180° Conduction Angles; T_C = 90°C)	$I_{T(RMS)}$	12	A
Average On−State Current (180° Conduction Angles; T_C = 90°C)	$I_{T(AV)}$	7.8	A
Peak Non-Repetitive Surge Current (1/2 Cycle, Sine Wave 60 Hz, T_J = 125°C)	I_{TSM}	100	A
Circuit Fusing Consideration (t = 8.3 msec)	I^2t	41	A^2sec
Forward Peak Gate Power (Pulse Width ≤ 1.0 μsec, T_C = 90°C)	P_{GM}	5.0	W
Forward Average Gate Power (t = 8.3 msec, T_C = 90°C)	$P_{G(AV)}$	0.5	W
Forward Peak Gate Current (Pulse Width ≤ 1.0 μsec, T_C = 90°C)	I_{GM}	2.0	A
Operating Junction Temperature Range	T_J	−40 to 125	°C
Storage Temperature Range	T_{stg}	−40 to 150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. V_{DRM} for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the device are exceeded.

ON Semiconductor®

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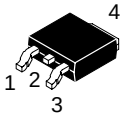
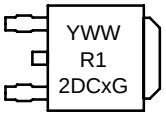
SCRs
12 AMPERES RMS
600 − 800 VOLTS



DPAK
CASE 369C
STYLE 4

MARKING DIAGRAM



Y = Year
WW = Work Week
R12DCx = Device Code
x= M or N
G = Pb−Free Package

PIN ASSIGNMENT	
1	Cathode
2	Anode
3	Gate
4	Anode

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

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THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance − Junction−to−Case − Junction−to−Ambient − Junction−to−Ambient (Note 2)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	2.2 88 80	°C/W
Maximum Lead Temperature for Soldering Purposes (Note 3)	T_L	260	°C

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Peak Repetitive Forward or Reverse Blocking Current (V_{AK} = Rated V_{DRM} or V_{RRM}, Gate Open)	 T_J = 25°C T_J = 125°C	I_{DRM}, I_{RRM}	 − −	 − −	 0.01 5.0	mA
ON CHARACTERISTICS						
Peak Forward On−State Voltage (Note 4) (I_{TM} = 20 A)		V_{TM}	−	1.3	1.9	V
Gate Trigger Current (Continuous dc) (V_D = 12 V, R_L = 100 Ω)	 T_J = 25°C T_J = −40°C	I_{GT}	 2.0 −	 7.0 −	 20 40	mA
Gate Trigger Voltage (Continuous dc) (V_D = 12 V, R_L = 100 Ω)	 T_J = 25°C T_J = −40°C	V_{GT}	 0.5 −	 0.65 −	 1.0 2.0	V
Gate Non−Trigger Voltage (V_D = 12 V, R_L = 100 Ω)	 T_J = 125°C	V_{GD}	0.2	−	−	V
Holding Current (V_D = 12 V, Initiating Current = 200 mA, Gate Open)	 T_J = 25°C T_J = −40°C	I_H	 4.0 −	 22 −	 40 80	mA
Latching Current (V_D = 12 V, I_G = 20 mA, T_J = 25°C) (V_D = 12 V, I_G = 40 mA, T_J = −40°C)		I_L	 4.0 −	 22 −	 40 80	mA
DYNAMIC CHARACTERISTICS						
Critical Rate of Rise of Off−State Voltage (V_D = Rated V_{DRM}, Exponential Waveform, Gate Open, T_J = 125°C)		dv/dt	 50	 200	 −	V/μs

2. These ratings are applicable when surface mounted on the minimum pad sizes recommended.
3. 1/8″ from case for 10 seconds.
4. Pulse Test: Pulse Width ≤ 2.0 msec, Duty Cycle ≤ 2%.

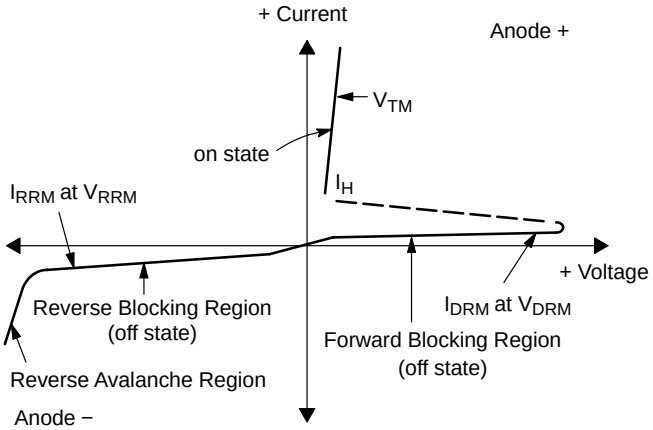
ORDERING INFORMATION

Device	Package	Shipping†
MCR12DCMT4	DPAK	2500 / Tape and Reel
MCR12DCMT4G	DPAK (Pb−Free)	2500 / Tape and Reel
MCR12DCNT4	DPAK	2500 / Tape and Reel
MCR12DCNT4G	DPAK (Pb−Free)	2500 / Tape and Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Voltage Current Characteristic of SCR

Symbol	Parameter
V_{DRM}	Peak Repetitive Off−State Forward Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Off−State Reverse Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Peak On−State Voltage
I_H	Holding Current



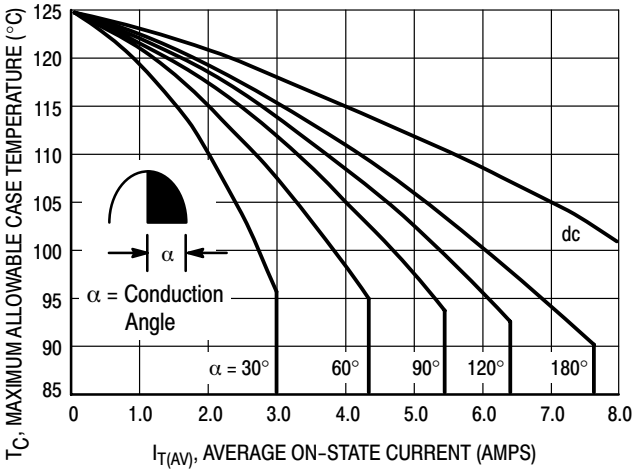


Figure 1. Average Current Derating

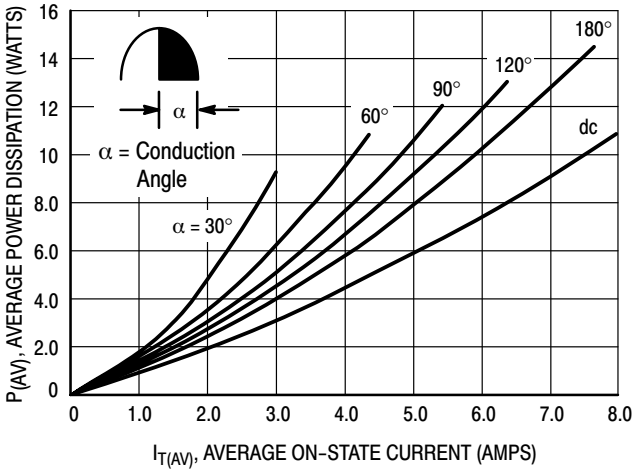


Figure 2. On−State Power Dissipation

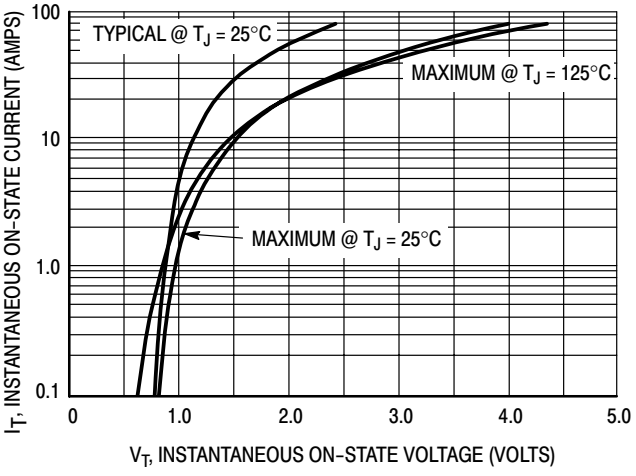


Figure 3. On−State Characteristics

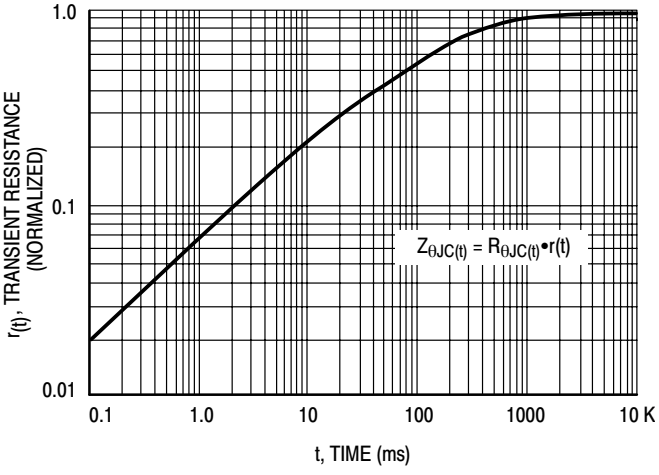


Figure 4. Transient Thermal Response

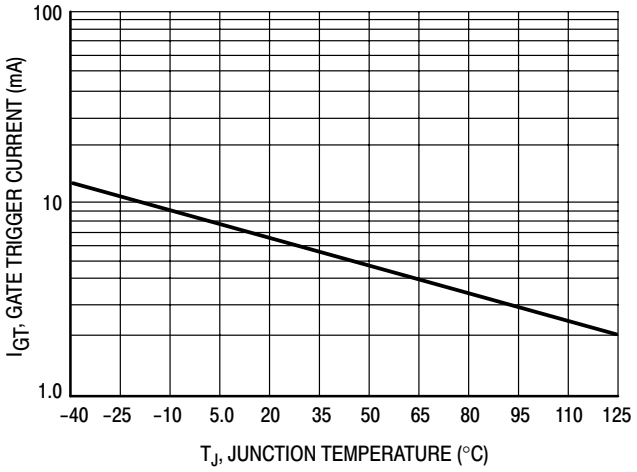


Figure 5. Typical Gate Trigger Current versus Junction Temperature

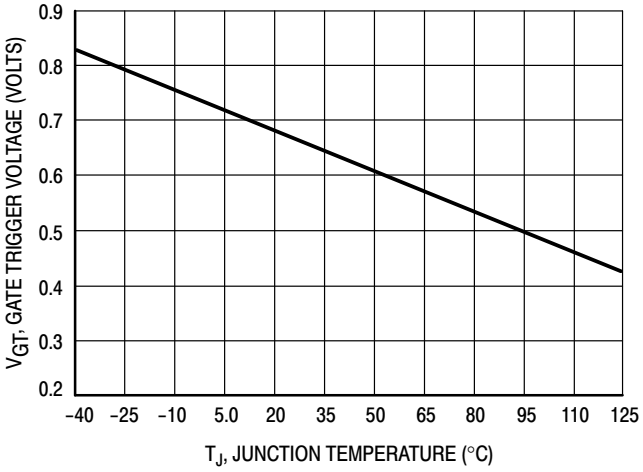


Figure 6. Typical Gate Trigger Voltage versus Junction Temperature

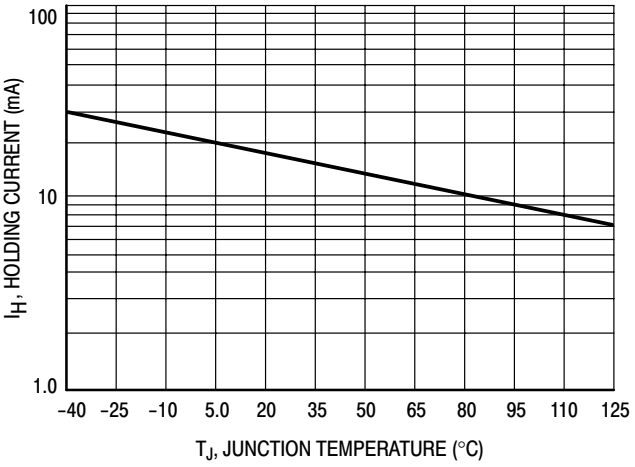


Figure 7. Typical Holding Current versus Junction Temperature

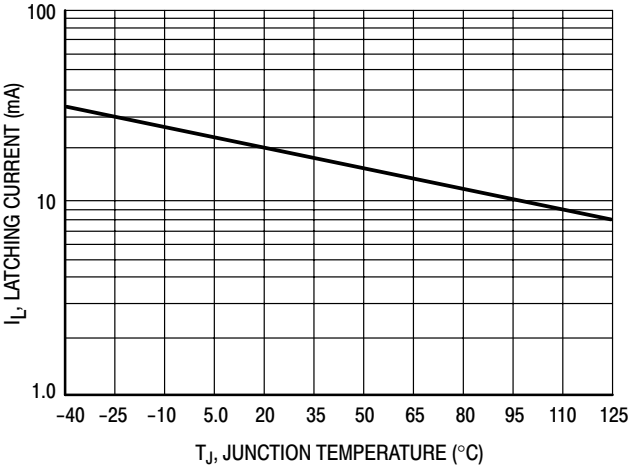


Figure 8. Typical Latching Current versus Junction Temperature

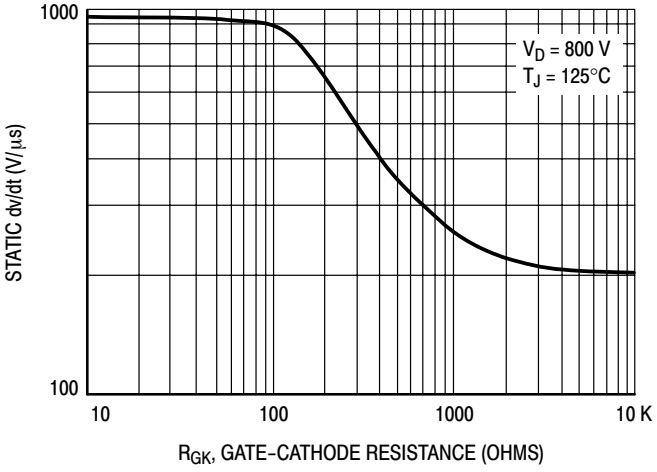
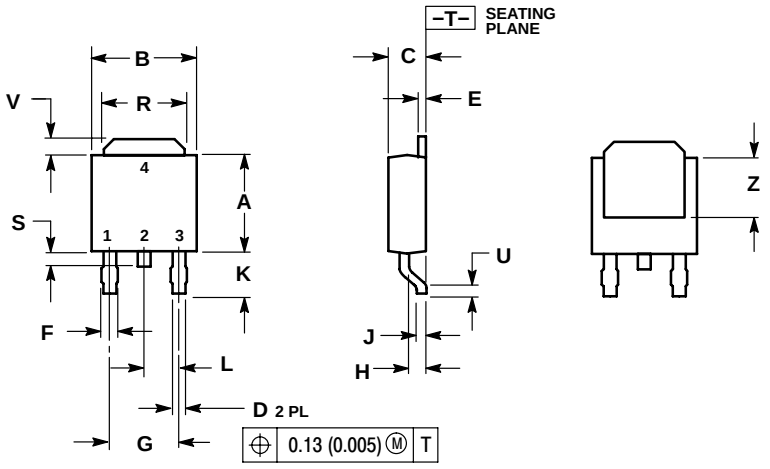


Figure 9. Exponential Static dv/dt versus Gate−Cathode Resistance

PACKAGE DIMENSIONS

DPAK
CASE 369C
ISSUE O

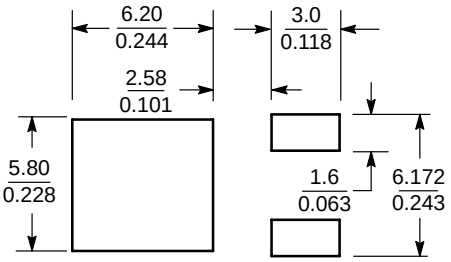


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	−−−	0.51	−−−
V	0.035	0.050	0.89	1.27
Z	0.155	−−−	3.93	−−−

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

SOLDERING FOOTPRINT*



SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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