Am26LS32B

Quad Differential Line Receiver

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- ±120 mV sensitivity over V_{IN} range of 0 V to 5 V
- ±200 mV sensitivity over V_{CM} range
- –7 V to +12 V input voltage range – differential or common mode
- Guaranteed input voltage hysteresis limits
  - 65 mV minimum
  - 240 mV maximum
- 3 V maximum open circuit input voltage
- Three-state outputs disabled during power-up and power-down
- Maximum guarantees for t_{PD} skew
- All AC and DC parameters guaranteed over COM'L and MIL operating temperature ranges
- Single +5 V supply
- Advanced low-power Schottky processing

GENERAL DESCRIPTION

The Am26LS32B is a quad line receiver designed to meet the requirements of RS-422 and RS-423, CCITT V.10 and V.11, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

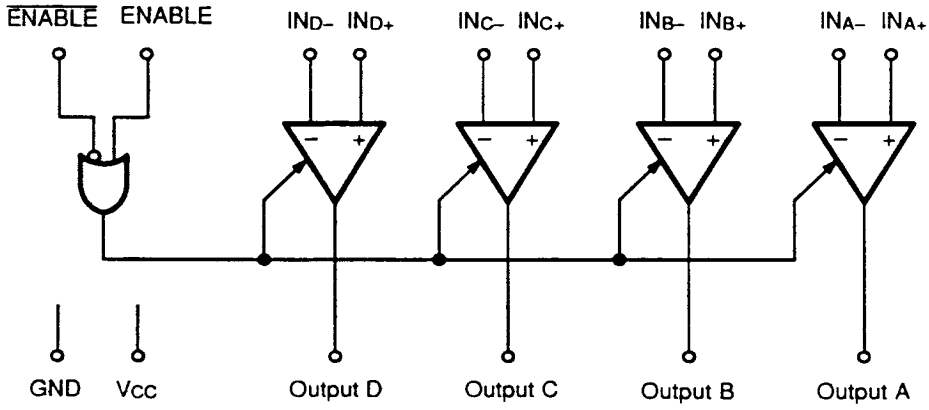
The Am26LS32B features an input sensitivity of 200 mV over the common mode input voltage range of –7 V to +12 V.

The Am26LS32B is the first device in the Am26LS32 configuration to guarantee minimum hysteresis and propagation delay skew while maintaining better propagation delay guarantees than the Am26LS32. This allows a more critical analysis of performance in high noise environments and better performance in terms of signal quality, resulting in better system performance.

The Am26LS32B provides an enable and disable function common to all four receivers. It features three-state outputs with 24 mA sink capability and incorporates a fail safe input-output relationship which keeps the outputs high when the inputs are open.

The Am26LS32B is contructed using Advanced Low-Power Schottky processing.

BLOCK DIAGRAM



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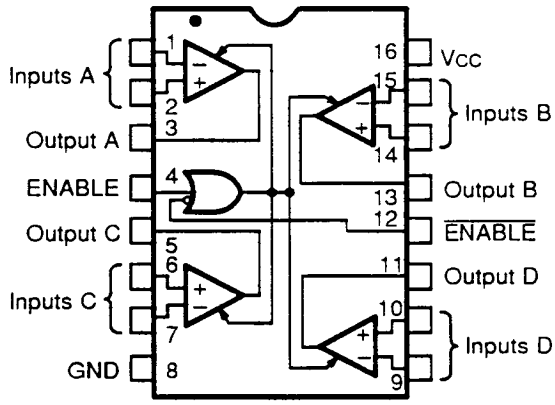
RELATED AMD PRODUCTS

Part No.	Description
26LS29	Quad Three-State Single Ended RS-423 Line Driver
26LS30	Dual Differential RS-422 Party Line/Quad Single Ended RS-423 Line Driver
26LS33	Quad Differential Line Receiver

Publication# 01024 Rev. B Amendment/0
Issue Date: May 1991

CONNECTION DIAGRAMS
Top View

DIP



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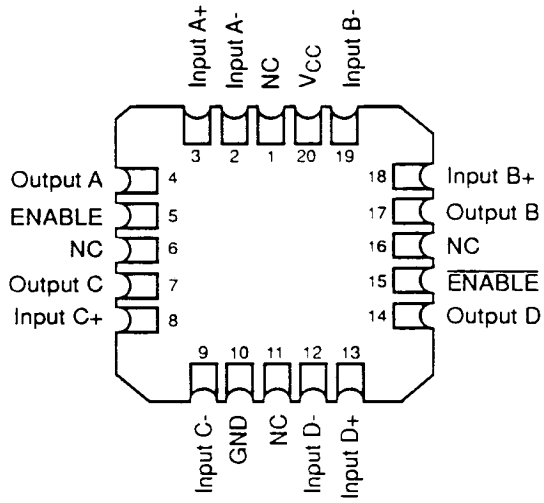
LCC



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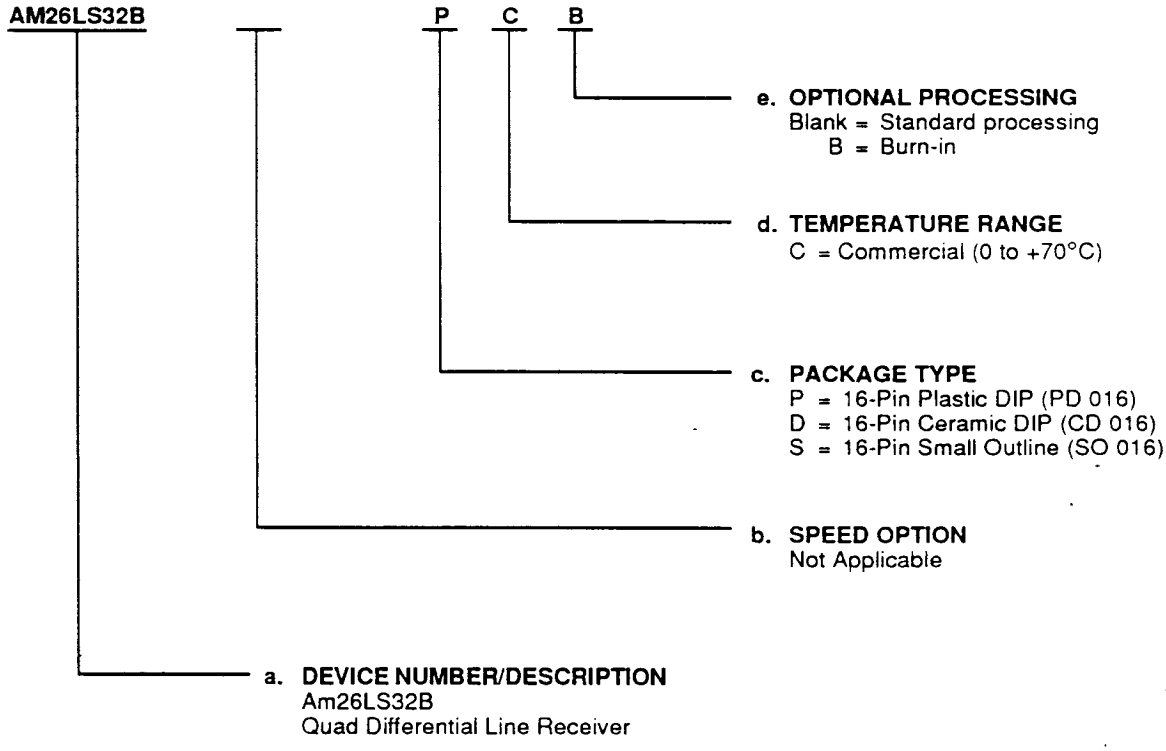
Note:
Pin 1 is marked for orientation.

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM26LS32B	PC, PCB, DC, DCB, SC

Valid Combinations

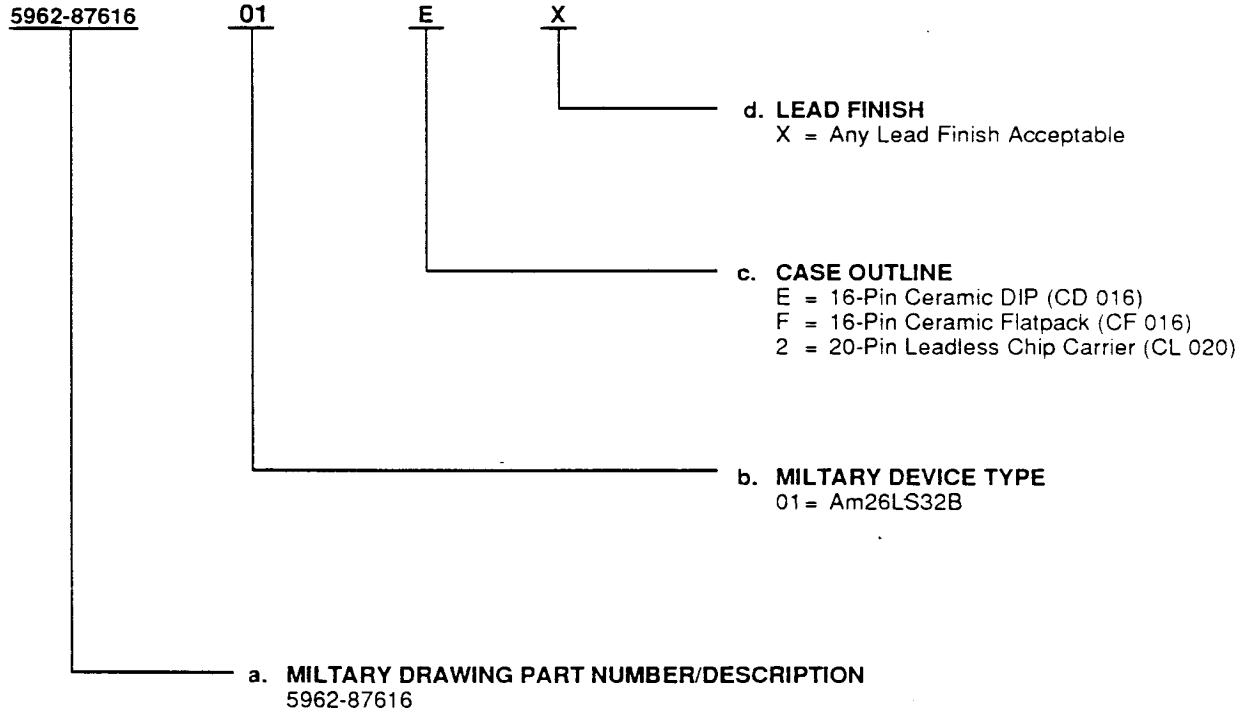
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

Standard Military Drawing (SMD)/DESC Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. Standard Military Drawing (SMD)/DESC products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for SMD/DESC products is formed by a combination of:

a. **Military Drawing Part Number**
b. **Military Device Type**
c. **Case Outline**
d. **Lead Finish**



Valid Combinations	
5962-87616-01	EX, FX, 2X

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

Group A Tests

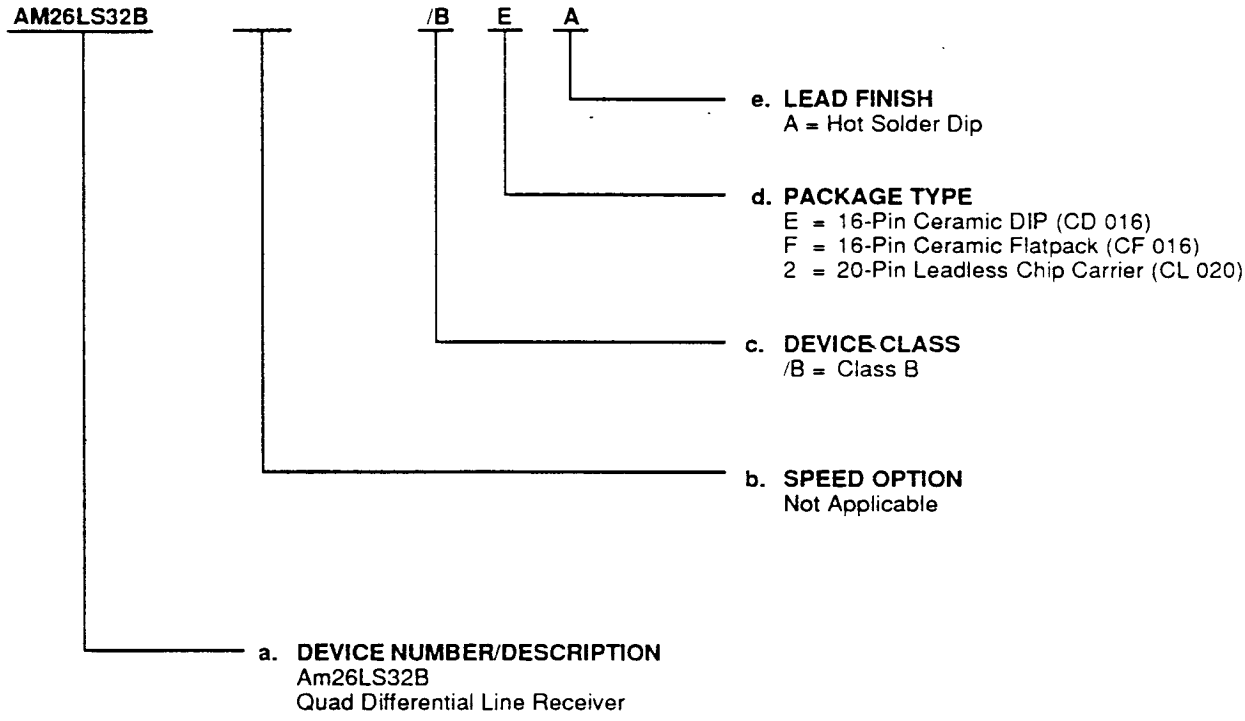
Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. **Device Number**
b. **Speed Option (if applicable)**
c. **Package Type**
d. **Temperature Range**
e. **Optional Processing**



Valid Combinations	
AM26LS32B	/BEA, /BFA, /B2A

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	7.0 V
Common Mode Range	±25 V
Differential Input Voltage	±25 V
Enable Voltage	7.0 V
Output Sink Current	50 mA
Storage Temperature Range	−65 to +165°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Temperature	0 to +70°C
Supply Voltage	+4.5 V to +5.5 V

Military (M) Devices

Temperature	−55 to +125°C
Supply Voltage	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Unit
V_{TH}	Differential Input Voltage (Note 5)	$V_{OUT} = V_{OL}$ or V_{OH}	$0 \le V_{CM} \le +5$ V	−100	±60	100	mV
			-7 V $\le V_{CM} \le +12$ V	−200		200	
V_{HYST}	Input Hysteresis	V_{CC} = 5.0 V		65		240	mV
V_{IOC}	Open Circuit Input Voltage			1.5		3.0	V
R_{IN}	Input Resistance (Note 4)	-15 V $\le V_{CM} \le +15$ V (One input AC ground)		6.0	9.8		kΩ
I_{IN}	Input Current (Under Test)	$V_{IN} = +15$ V, Other Input -15 V $\le V_{IN} \le +15$ V				2.3	mA
I_{IN}	Input Current (Under Test)	$V_{IN} = -15$ V, Other Input -15 V $\le V_{IN} \le +15$ V				−2.8	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., $\Delta V_{IN} = +1.0$ V, $\overline{V_{ENABLE}} = 0.8$ V	$I_{OH} = -12$ mA	2.0			V
			$I_{OH} = -1$ mA	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = Min., $\Delta V_{IN} = -1.0$ V, $\overline{V_{ENABLE}} = 0.8$ V	I_{OL} = 16 mA			0.4	V
			I_{OL} = 24 mA			0.5	
V_{IL}	Enable LOW Voltage	(Note 2)				0.8	V
V_{IH}	Enable HIGH Voltage	(Note 2)		2.0			V
V_{IC}	Enable Clamp Voltage	V_{CC} = Min., $I_{IN} = -18$ mA				−1.5	V
I_O	Off-State (High Impedance) Output Current	V_{CC} = Max.	V_O = 2.4 V			50	µA
			V_O = 0.4 V			−50	
I_{IL}	Enable LOW Current	V_{IN} = 0.4 V, V_{CC} = Max.			−0.2	−0.36	mA
I_{IH}	Enable HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max.				20	µA
I_I	Enable Input High Current	V_{IN} = 5.5 V, V_{CC} = Max.				100	µA
I_{SC}	Output Short Circuit Current	V_O = 0 V, V_{CC} = Max., $\Delta V_{IN} = +1.0$ V (Note 3)		−30	−65	−120	mA
I_{CC}	Power Supply Current	V_{CC} = Max., All V_{IN} = GND, Outputs Disabled			52	70	mA

Notes:

1. All typical values are V_{CC} = 5.0 V, T_A = 25°C.
2. Input thresholds are tested during DC tests and may be done in combination with testing of other DC parameters.
3. Not more than one output should be shorted at a time. Duration of short circuit test should not exceed one second.
4. R_{IN} is not directly tested but is correlated. (See Attachment I)
5. Input voltage is not tested directly due to tester accuracy limitations but is tester correlated. (See Attachment II)

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0 V)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
t_{PLH}	Propagation Delay, Input to Output	C_L = 50 pF See test circuit		16	21	ns
t_{PHL}				17	21	ns
t_{SKEW}	Propagation Delay Skew, $t_{PLH} - t_{PHL}$			1.5	3.0	ns
t_{ZL}	Output Enable Time, ENABLE to Output			16	22	ns
t_{ZH}				10	16	ns
t_{LZ}	Output Disable Time, ENABLE to Output	C_L = 5 pF See test circuit		11	18	ns
t_{HZ}				13	18	ns

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay, Input to Output	C_L = 50 pF See test circuit		26		26	ns
t_{PHL}				26		26	ns
t_{SKEW}	Propagation Delay Skew, $t_{PLH} - t_{PHL}$			4.0		4.0	ns
t_{ZL}	Output Enable Time, ENABLE to Output			33		33	ns
t_{ZH}				22		22	ns
t_{LZ}	Output Disable Time, ENABLE to Output	C_L = 5 pF See test circuit		27		27	ns
t_{HZ}				27		27	ns

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
Tristate Delays for $\overline{\text{ENABLE}}$ (T_A = +25°C)						
t_{PZH}	Propagation Delay From $\overline{\text{ENABLE}}$ to Output	C_L 50 pF, R_{L1} = 1 kΩ, R_{L2} = 280 Ω			26	ns
t_{PZL}	Propagation Delay From $\overline{\text{ENABLE}}$ to Output	C_L 50 pF, R_{L1} = 1 kΩ, R_{L2} = 280 Ω			33	ns
t_{PHZ}	Propagation Delay From $\overline{\text{ENABLE}}$ to Output	C_L 5 pF, R_{L1} = 1 kΩ, R_{L2} = 280 Ω			20	ns
t_{PLZ}	Propagation Delay From $\overline{\text{ENABLE}}$ to Output	C_L 5 pF, R_{L1} = 1 kΩ, R_{L2} = 280 Ω			20	ns
Tristate Delays for $\overline{\text{ENABLE}}$ (–55°C to +125°C)						
t_{PZH}	Propagation Delay From $\overline{\text{ENABLE}}$ to Output	C_L 50 pF, R_{L1} = 1 kΩ, R_{L2} = 280 Ω			39	ns
t_{PZL}	Propagation Delay From $\overline{\text{ENABLE}}$ to Output	C_L 50 pF, R_{L1} = 1 kΩ, R_{L2} = 280 Ω			49	ns
t_{PHZ}	Propagation Delay From $\overline{\text{ENABLE}}$ to Output	C_L 5 pF, R_{L1} = 1 kΩ, R_{L2} = 280 Ω			30	ns
t_{PLZ}	Propagation Delay From $\overline{\text{ENABLE}}$ to Output	C_L 5 pF, R_{L1} = 1 kΩ, R_{L2} = 280 Ω			30	ns

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance "Off" State

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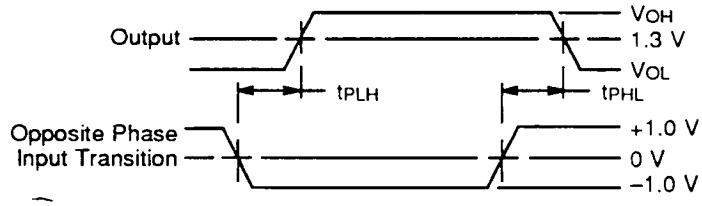
SWITCHING WAVEFORMS



Propagation Delay (Notes 1 and 3)

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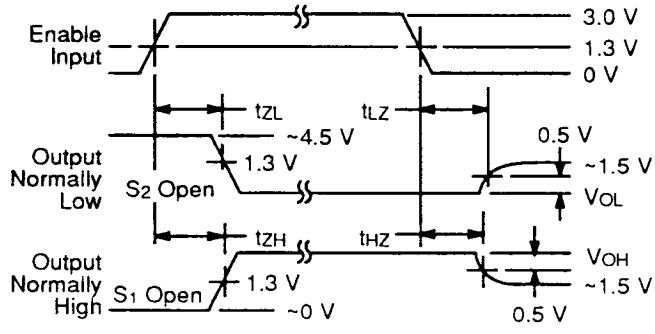

Enable and Disable Times (Notes 2 and 3)

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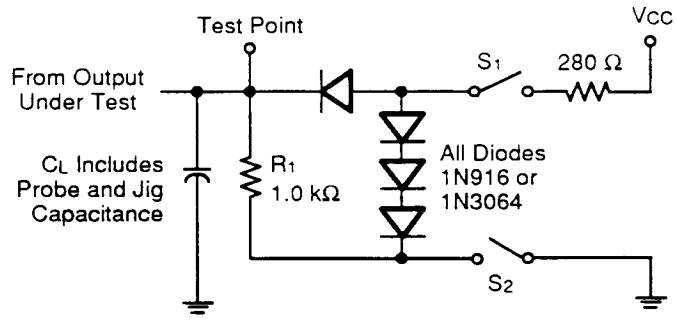
Notes:

1. Diagram shown for ENABLE LOW.
2. S_1 and S_2 of Load Circuit are closed except where shown.
3. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Z_O = 50 Ω; t_r ≤ 2.5 ns; t_f ≤ 2.5 ns.

SWITCHING TEST CIRCUIT FOR THREE-STATE OUTPUTS



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Am26LS32/32B/33/34 Input Resistance and Input Current (Attachment I)

Input resistance measurement for differential inputs on line receivers are generally not measured directly. Instead they are correlated to an input current measurement and to the process resistor temperature coefficient. The assumptions made include 1) Process resistor temperature coefficient is known and 2) The open input bias voltage for the input is known or measured within the same test sequence.

Under the above assumptions R_{IN} can be correlated to the input current measured. The expression

$$R_{IN} = \frac{(V_{ICM} - V_{IN})\ (R_T)}{(I_{IN})\ (R25)},$$

where V_{ICM} is the open input bias voltage of the Line Receiver. When applying this correlation to the 26LS32 die, the following criteria have been set.

1) V_{ICM} and I_{IN} are the values screened at wafer sort.
2) Temperature coefficients are for 800 ohm/square which gives 0.96 at 0°C and 0.93 at –55°C.

When setting limits, characterized values for V_{ICM} have been used instead of the test programmed limit value. R_{IN} (dif) is R_{IN} (dif) = 2 R_{IN}.

For the Am26LS32/32B/33/34

$$R_{IN}\ \text{Min.} = \frac{(2.56 - -15)\ 0.96}{I_{IN}\ (\text{Max.})} = 16.8/I_{IN}\ (\text{Max.})\ \text{Comm.},$$

and

R_{IN} Min. = 16.3/I_{IN} (Max.) Mil.

Worst Case Measurement for Input Current

Two considerations have been used to determine the test condition for input current of the data path for the Am26LS32 Line Receiver.

1) Input current is tested on the 26LS32 with the pin under test at one end of the range (+15 V for example) and the untested pin at the opposite extreme of the input range under test. If both pins were at the same test voltage the internal bias generator would have a lower output voltage for tests at –15 V V_{IN} and a higher output voltage at +15 V V_{IN}. This would produce test currents less than maximum.
2) For the 26LS32, breakdown of the differential inputs is the primary failure to the data sheet specification. Hence, both breakdown voltage and input current are tested during the input current tests.

Test Documentation For Am26LS32/32B/34 V_{TH} (Attachment II)

Input threshold (V_{TH}) for the Am26LS32/32B/34 is described by the equation,

V_{TH} = (N+1) (1+R1/R) K*T/Q (1+Rh/(m (Rc+Rh))) /(1–Rh/ (M(Rc+Rh))).

Where N+1 is the attenuator ratio, R1/R is the attenuator ratio mismatch, M is the ratio of the input stage current to hysteresis stage current, and Rh and Rc are input stage loads. For Am26LS32 – 34 devices which pass function tests, V_{OH} and V_{OL} tests, thresholds for all inputs within the operating range of the circuit.

The Test system is unable to force input thresholds within the accuracy required for the Am26LS32 – 34 specifications. Figure 1 plots the expected values for V_{TH}, the worst case values at 25°C and 155°C. Also shown are the test values for V_{TH} at the –1.5 V input (V_{IN}). In addition, the test voltage at –7 V V_{IN} is shown. For the figure it is seen that the worst case value for the test limit shown would be +/–165 mV, where +/– 102 mV is expected for process parameters and the equation for V_{TH}. Further the 25 mV negative guardband used for –7 V testing is less than half the machine uncertainty of 60 mV.

When QA testing for Am26LS32/32B/34 is done, thresholds are screened for V_{CM} other than –1.5 V. These additional tests are considered functional tests only, and the precision threshold tests which insure compliance with data sheet limits are those tests performed where the inputs are tested near –1.5 V.

The actual threshold tests are done as a sequence where a setup is performed which preconditions the DUT to a logic one state, then the threshold correlation for a logic zero is tested followed by a threshold correlation for logic one to complete the sequence. The limit values for the setup (Vt SET), logic zero test (Vt "–"), and logic one test (Vt "+") are listed under V_{TH} for supply value of 5.0 V.

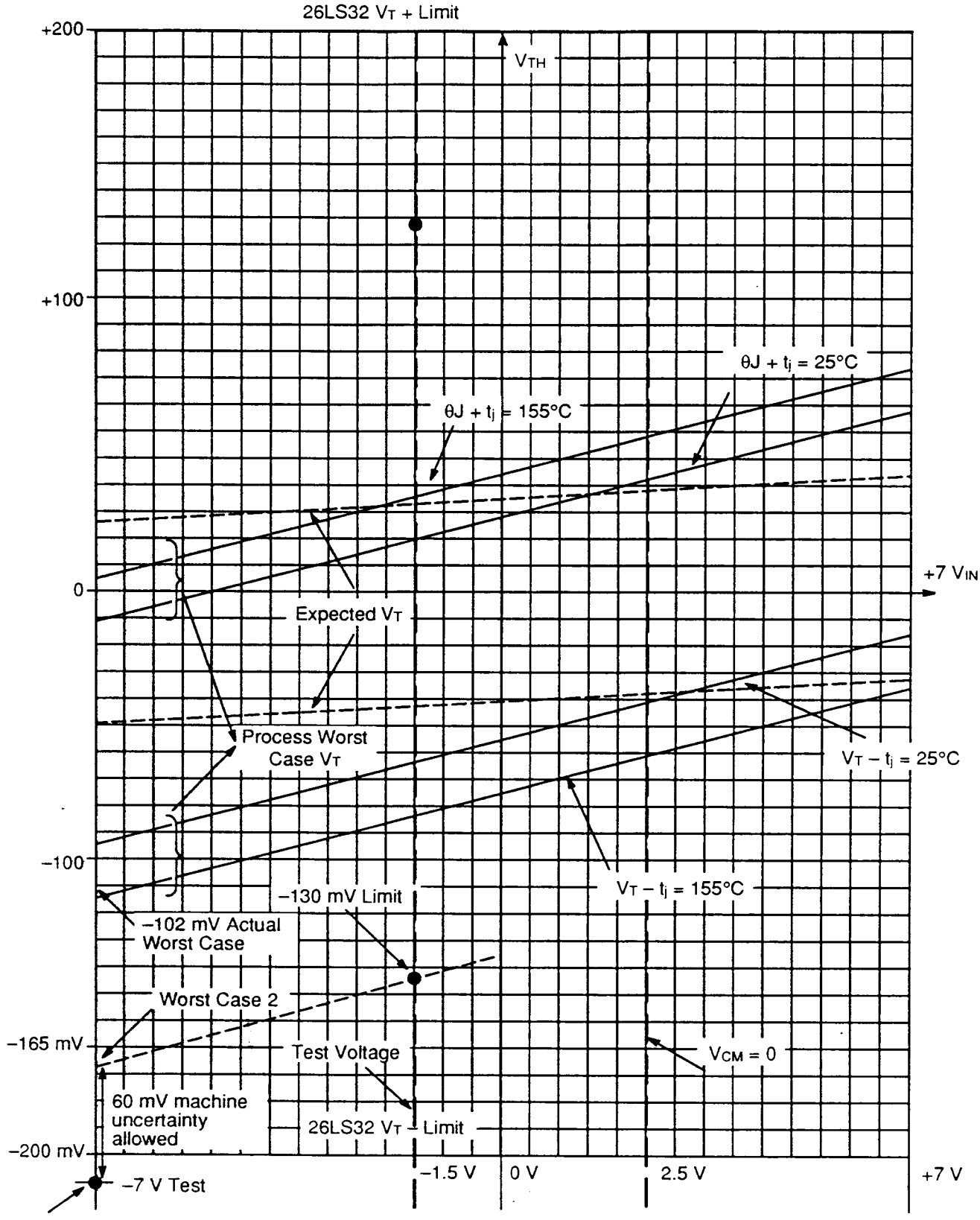
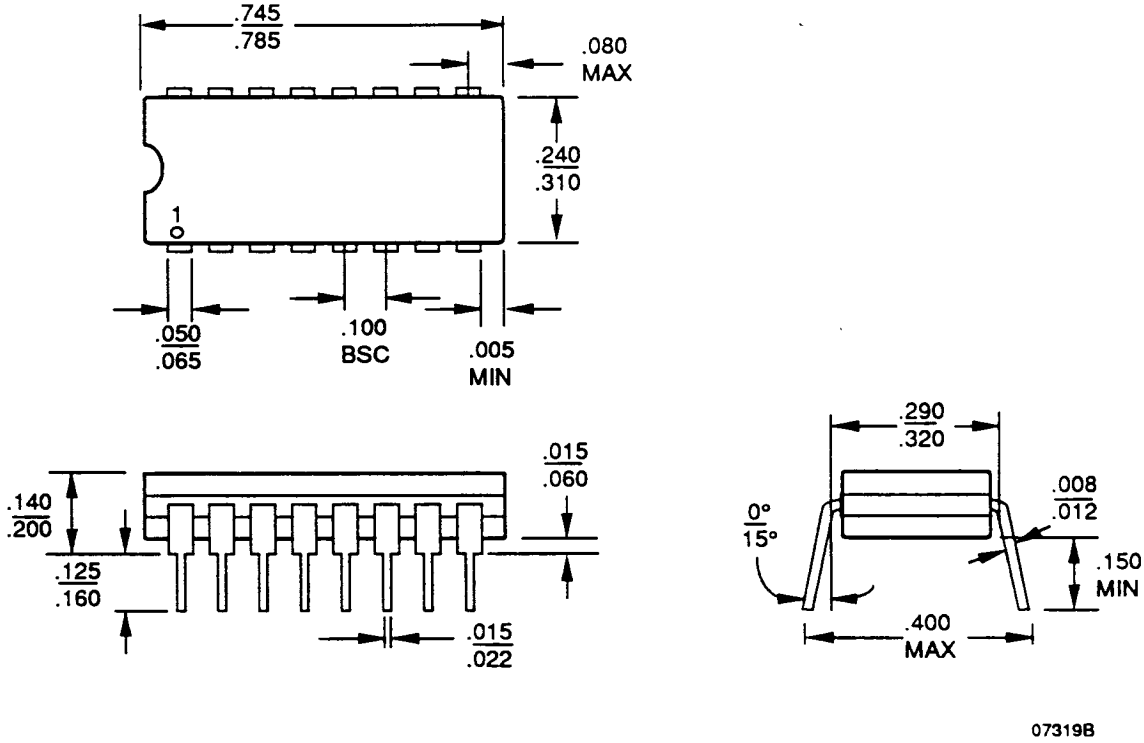


Figure 1. 26LS32 Input Threshold V_T vs. Input Voltage V_{IN}

PHYSICAL DIMENSIONS*

CD 016



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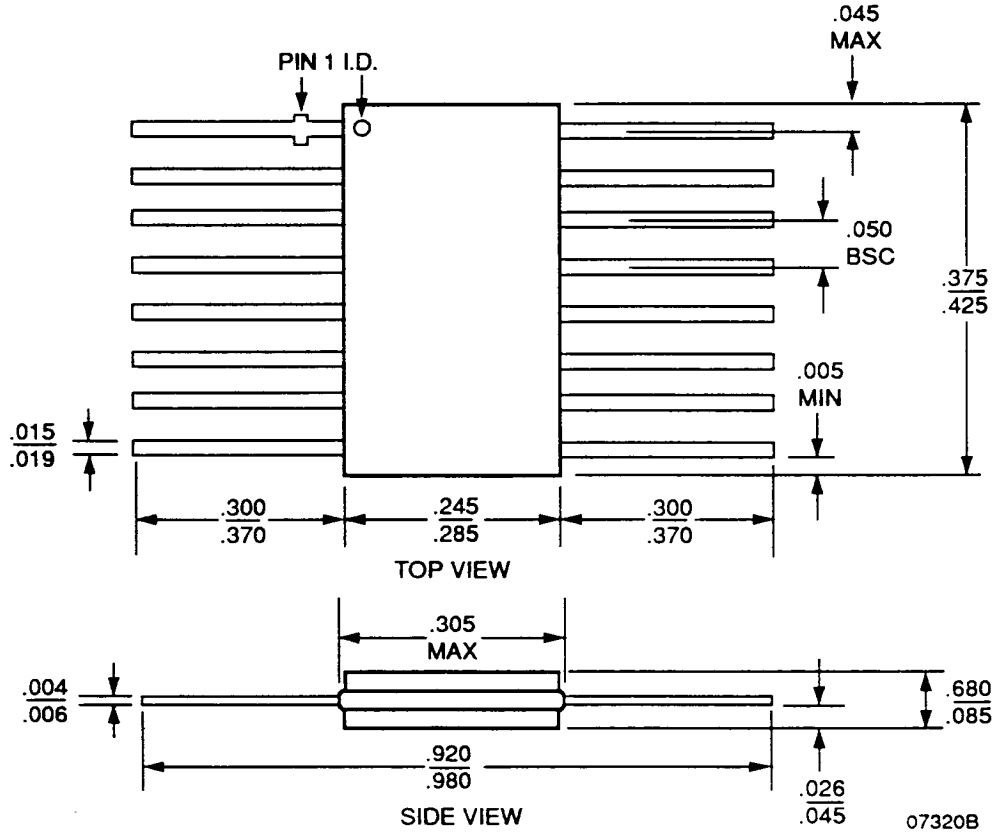
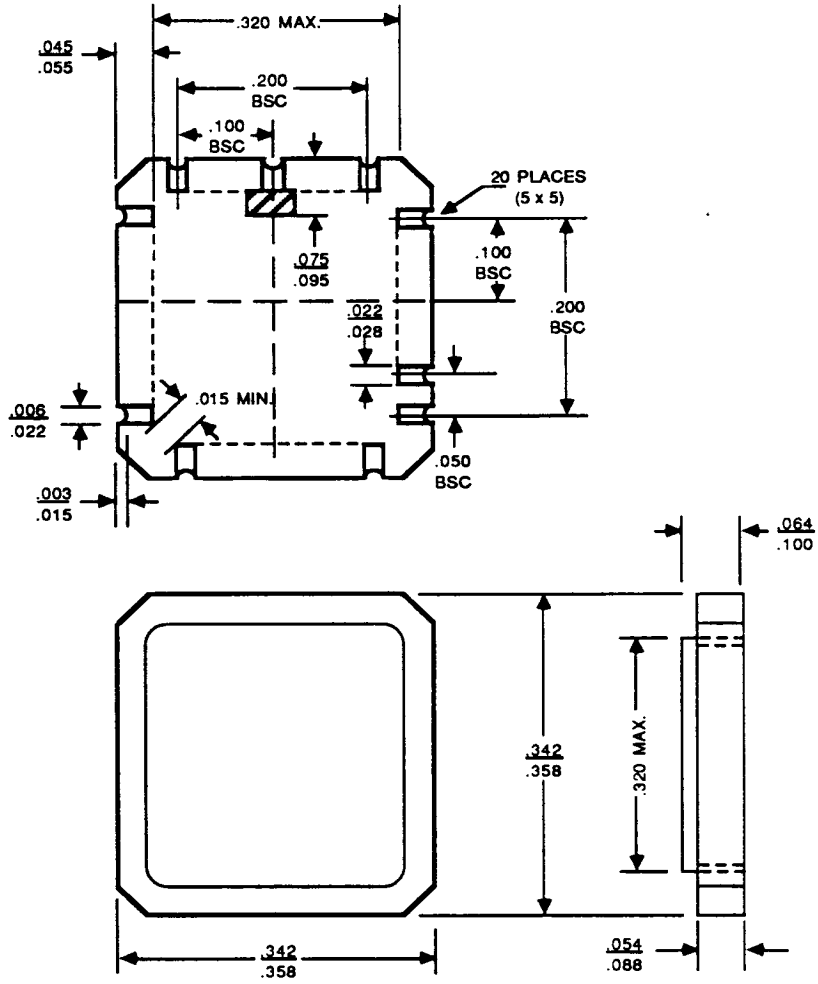


*For reference only. All dimensions are measured in inches, unless otherwise noted. BSC is an ANSI standard for Basic Space Centering.

PHYSICAL DIMENSIONS*
CL 020



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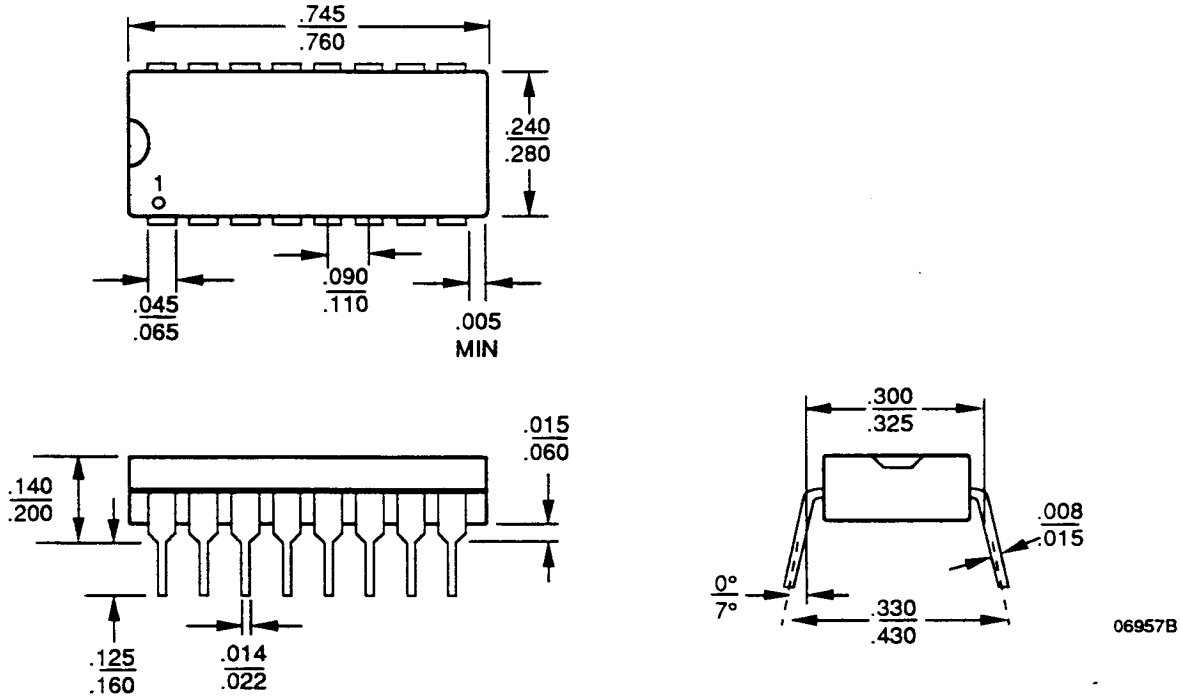
PHYSICAL DIMENSIONS*

PD 016



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