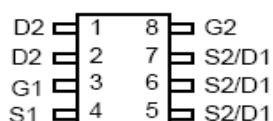
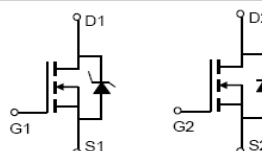


AO4926
Asymmetric Dual N-Channel Enhancement Mode Field Effect Transistor
SRFET™
General Description

The AO4926 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. The two MOSFETs make a compact and efficient switch and synchronous rectifier combination for use in DC-DC converters. A monolithically integrated Schottky diode in parallel with the synchronous MOSFET to boost efficiency further. *Standard Product AO4926 is Pb-free (meets ROHS & Sony 259 specifications).*

Features
FET1
 $V_{DS} (V) = 30V$
 $I_D = 9.5A$
 $R_{DS(ON)} < 13.5m\Omega$
 $R_{DS(ON)} < 16m\Omega$
FET2
 $V_{DS}(V) = 30V$
 $I_D = 7.3A \quad (V_{GS} = 10V)$
 $< 24m\Omega \quad (V_{GS} = 10V)$
 $< 29m\Omega \quad (V_{GS} = 4.5V)$
UIS TESTED!
Rg, Ciss, Coss, Crss Tested
SOIC-8

SRFET™

Soft Recovery MOSFET:
Integrated Schottky Diode


Absolute Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Parameter	Symbol	Max FET1	Max FET2	Units
Drain-Source Voltage	V_{DS}	30	30	V
Gate-Source Voltage	V_{GS}	± 12	± 12	V
Continuous Drain Current ^A	$T_A = 25^\circ C$	9.5	7.3	A
	$T_A = 70^\circ C$	7.8	5.9	
Pulsed Drain Current ^B	I_{DM}	40	40	A
Avalanche Current ^B	I_{AR}	22	12	A
Repetitive avalanche energy $L = 0.3mH$ ^B	E_{AR}	73	22	mJ
Power Dissipation	$T_A = 25^\circ C$	2.0	2.0	W
	$T_A = 70^\circ C$	1.3	1.3	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	-55 to 150	$^\circ C$

Thermal Characteristics FET1

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	48	62.5	$^\circ C/W$
Maximum Junction-to-Ambient ^A		74	90	$^\circ C/W$
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	32	40	$^\circ C/W$

Thermal Characteristics FET2

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	48	62.5	$^\circ C/W$
Maximum Junction-to-Ambient ^A		74	90	$^\circ C/W$
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	32	40	$^\circ C/W$

FET1 Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=30\text{V}$, $V_{GS}=0\text{V}$ $T_J=125^\circ\text{C}$		0.02 10	0.1 20	mA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 12\text{V}$			0.1	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1.5	1.8	2.4	V
$I_{D(ON)}$	On state drain current	$V_{GS}=4.5\text{V}$, $V_{DS}=5\text{V}$	40			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$, $I_D=9.5\text{A}$ $T_J=125^\circ\text{C}$		11 17.1	13.5 21.3	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}$, $I_D=7\text{A}$		13	16.0	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=9.5\text{A}$		78		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}$, $V_{GS}=0\text{V}$		0.38	0.5	V
I_S	Maximum Body-Diode + Schottky Continuous Current				4	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=15\text{V}$, $f=1\text{MHz}$		1980	2574	pF
C_{oss}	Output Capacitance			317		pF
C_{rss}	Reverse Transfer Capacitance			111		pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$		1.3	2.0	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}$, $V_{DS}=15\text{V}$, $I_D=9\text{A}$		33.0	43	
$Q_g(4.5\text{V})$	Total Gate Charge			15.0	20	nC
Q_{gs}	Gate Source Charge			5.3		nC
Q_{gd}	Gate Drain Charge			6.0		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=10\text{V}$, $V_{DS}=15\text{V}$, $R_L=1.6\Omega$, $R_{GEN}=3\Omega$		5.5		ns
t_r	Turn-On Rise Time			5.5		ns
$t_{D(off)}$	Turn-Off DelayTime			27.0		ns
t_f	Turn-Off Fall Time			4.3		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=9.5\text{A}$, $dI/dt=300\text{A}/\mu\text{s}$		11	13	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=9.5\text{A}$, $dI/dt=300\text{A}/\mu\text{s}$		7		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1 in ² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The value in any given application depends on the user's specific board design.

B: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=150^\circ\text{C}$.

C: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.

D: The static characteristics in Figures 1 to 6 are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in ² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The SOA curve provides a single pulse rating.

F: The current rating is based on the $t \leq 10\text{s}$ thermal resistance rating.

Rev1: June 2007

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FET1 TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

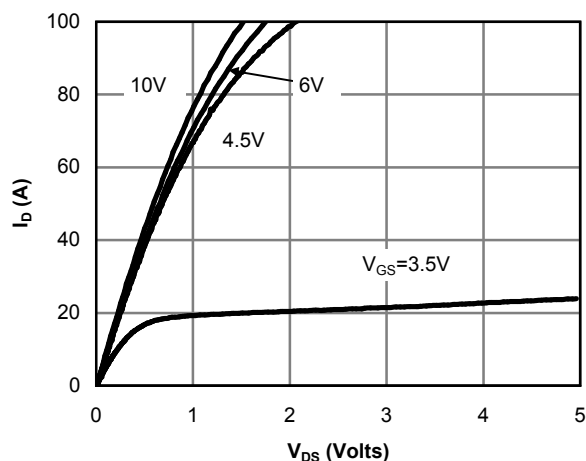


Figure 1: On-Region Characteristics

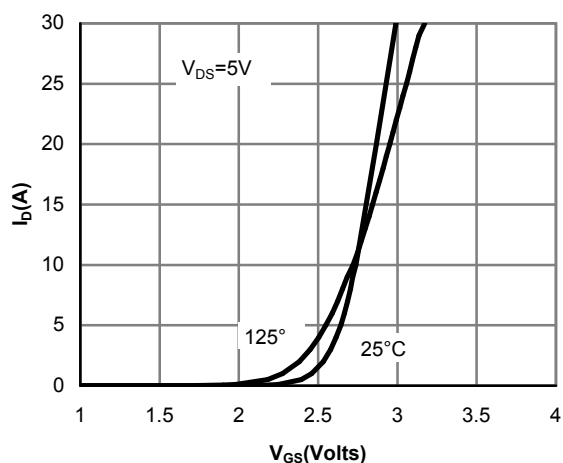


Figure 2: Transfer Characteristics

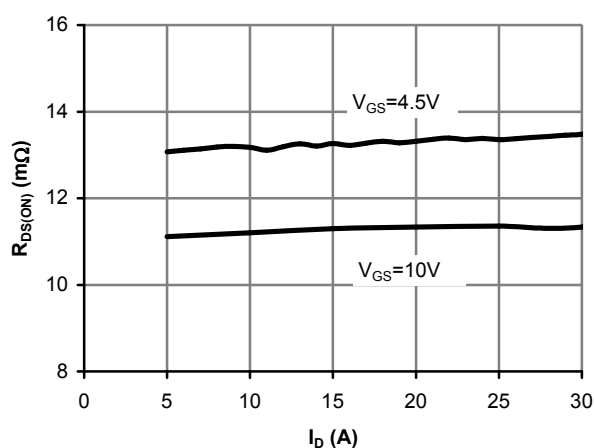


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

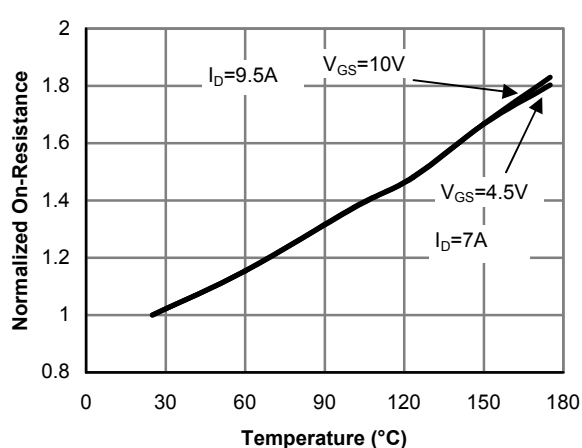


Figure 4: On-Resistance vs. Junction Temperature

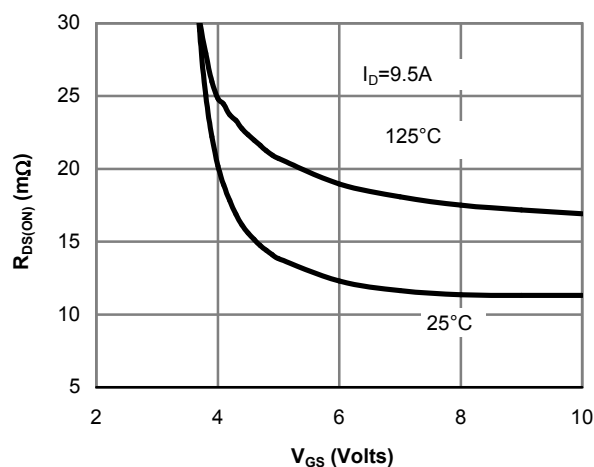


Figure 5: On-Resistance vs. Gate-Source Voltage

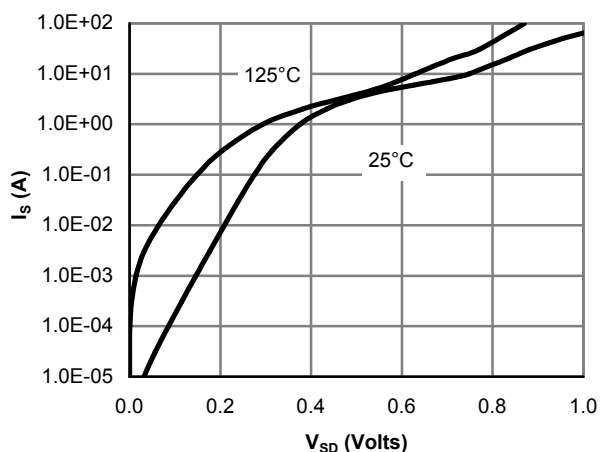


Figure 6: Body-Diode Characteristics

FET1 TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

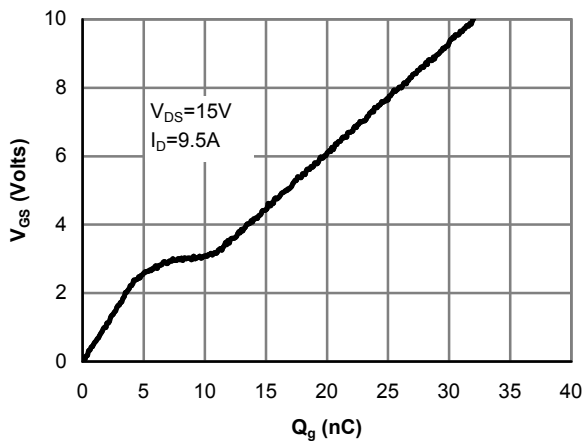


Figure 7: Gate-Charge Characteristics

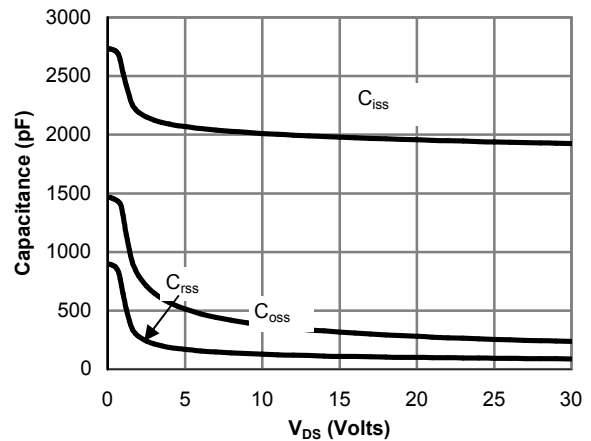


Figure 8: Capacitance Characteristics

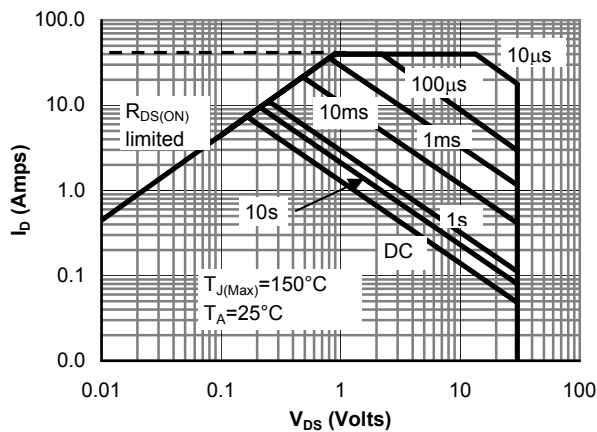


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

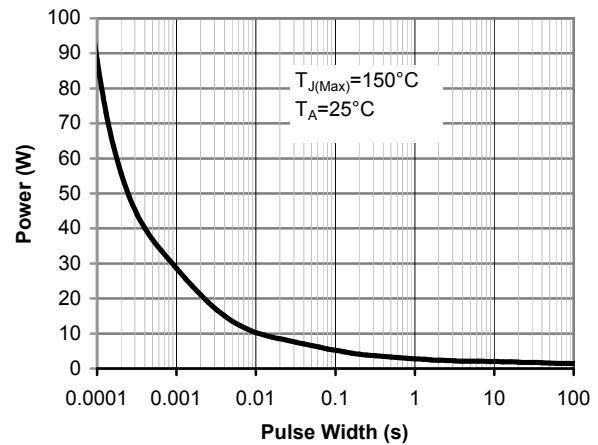


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

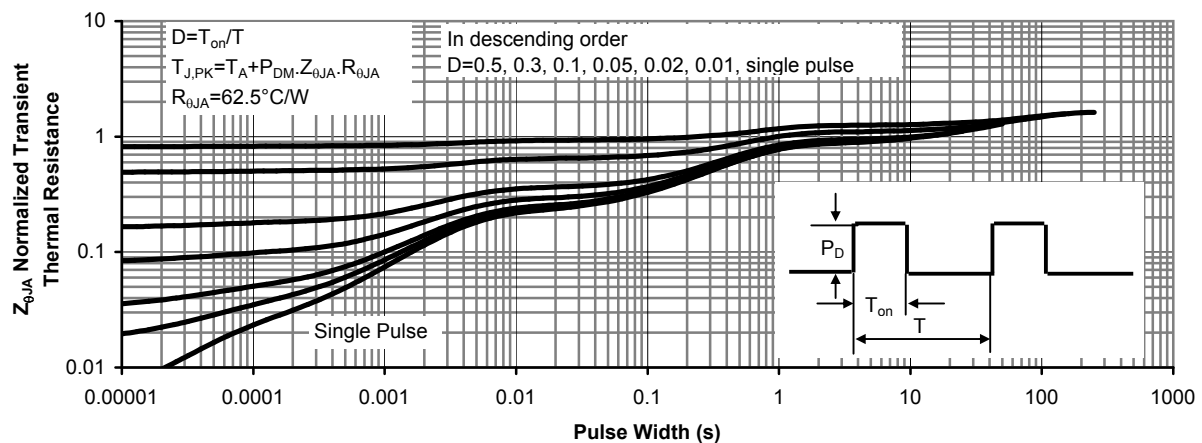


Figure 11: Normalized Maximum Transient Thermal Impedance (Note E)

FET1 TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

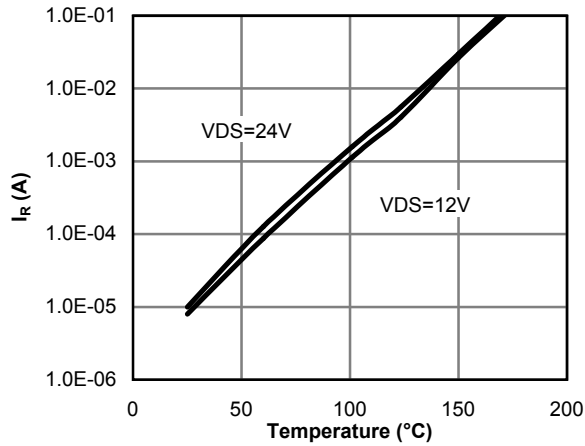


Figure 12: Diode Reverse Leakage Current vs. Junction Temperature

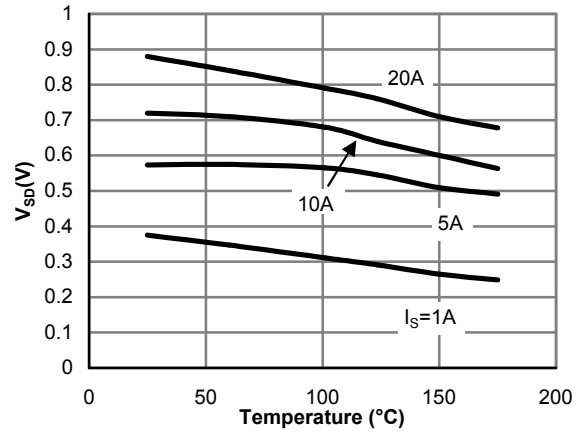


Figure 13: Diode Forward voltage vs. Junction Temperature

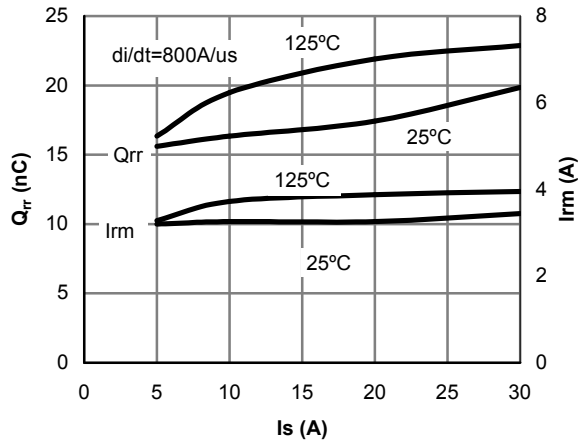


Figure 14: Diode Reverse Recovery Charge and Peak Current vs. Conduction Current

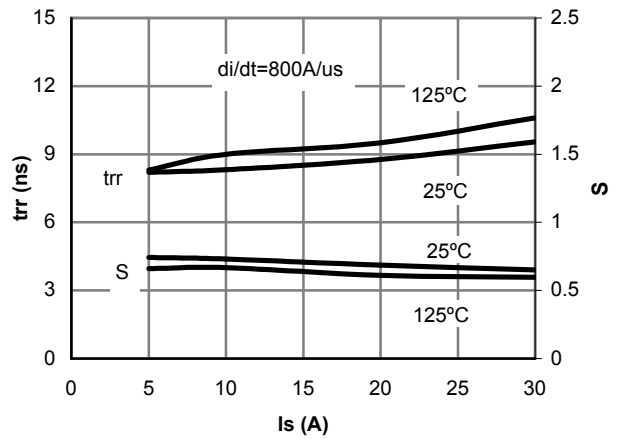


Figure 15: Diode Reverse Recovery Time and Soft Coefficient vs. Conduction Current

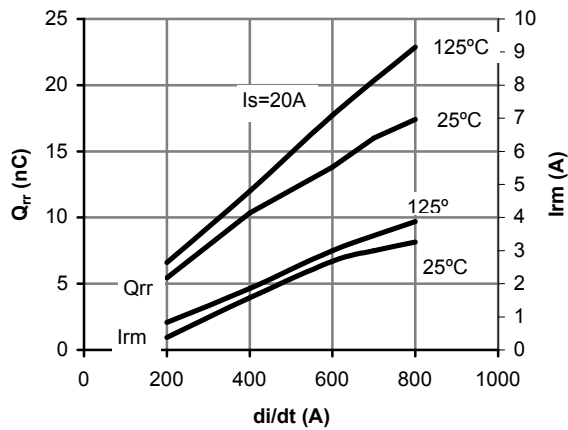


Figure 16: Diode Reverse Recovery Charge and Peak Current vs. di/dt

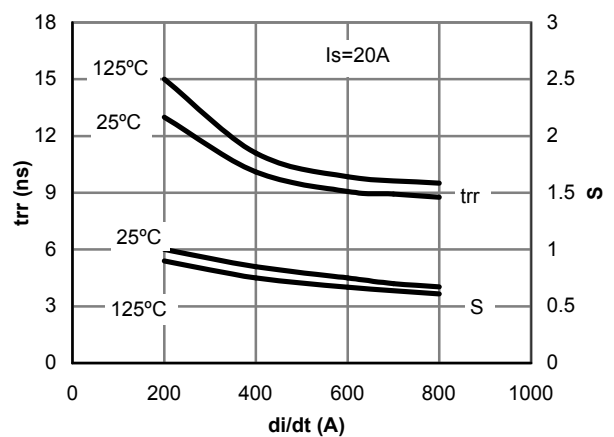


Figure 17: Diode Reverse Recovery Time and Soft Coefficient vs. di/dt

FET2 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V T _J =55°C		0.002	1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±12V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =250μA	0.7	1	1.5	V
I _{D(ON)}	On state drain current	V _{GS} =4.5V, V _{DS} =5V	40			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =7.3A T _J =125°C		20 28	24 35	mΩ
		V _{GS} =4.5V, I _D =6A		23.5	29	mΩ
		V _{GS} =2.5V, I _D =5A		34.7	48	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =7.3A		26		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.71	1	V
I _S	Maximum Body-Diode Continuous Current				2.8	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz		900	1100	pF
C _{oss}	Output Capacitance			88		pF
C _{rss}	Reverse Transfer Capacitance			65		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		0.95	1.5	Ω
SWITCHING PARAMETERS						
Q _g	Total Gate Charge	V _{GS} =4.5V, V _{DS} =15V, I _D =7.3A		10	12	nC
Q _{gs}	Gate Source Charge			1.8		nC
Q _{gd}	Gate Drain Charge			3.75		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =2Ω, R _{GEN} =6Ω		3.2		ns
t _r	Turn-On Rise Time			3.5		ns
t _{D(off)}	Turn-Off DelayTime			21.5		ns
t _f	Turn-Off Fall Time			2.7		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =7.3A, dI/dt=100A/μs		16.8	21	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =7.3A, dI/dt=100A/μs		8		nC

A: The value of R_{θJA} is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t_{θJA} ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C: The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

D: The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

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FET2 TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

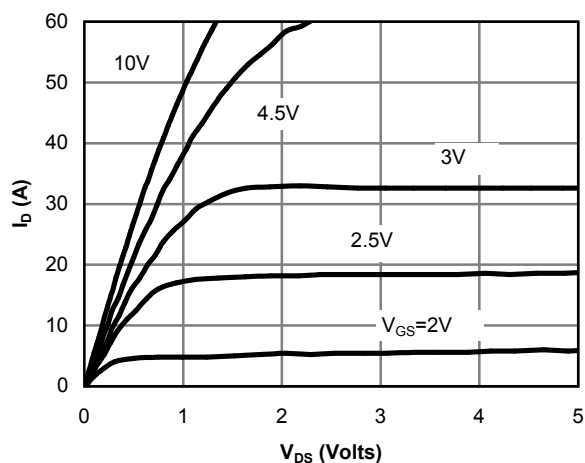


Figure 1: On-Region Characteristics

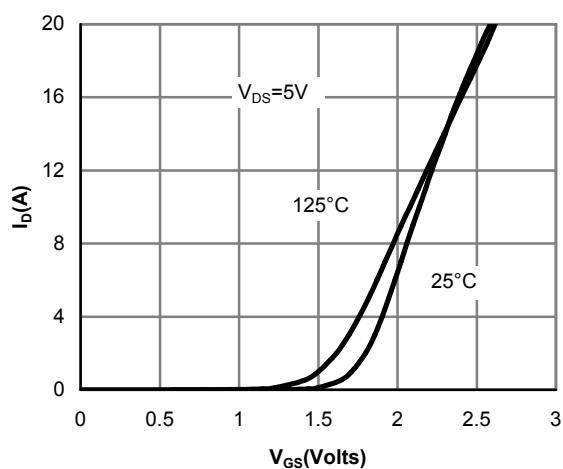


Figure 2: Transfer Characteristics

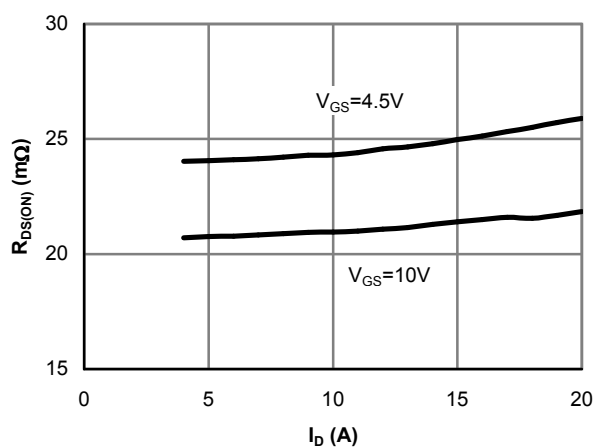


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

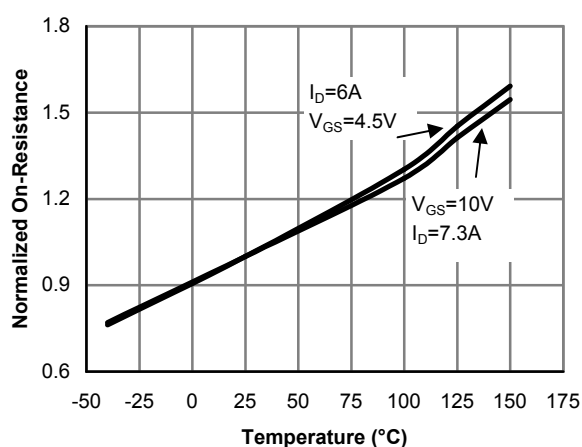


Figure 4: On-Resistance vs. Junction Temperature

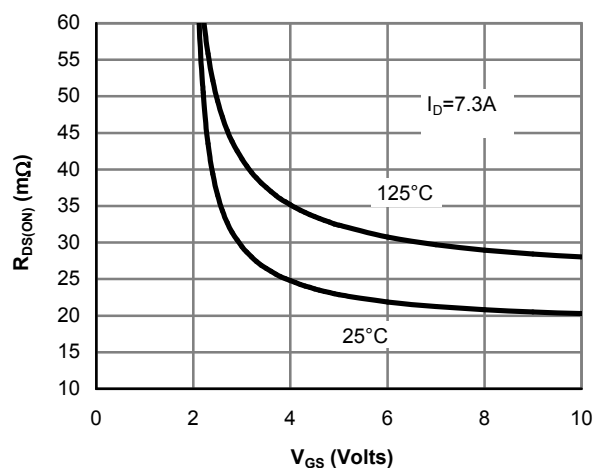


Figure 5: On-Resistance vs. Gate-Source Voltage

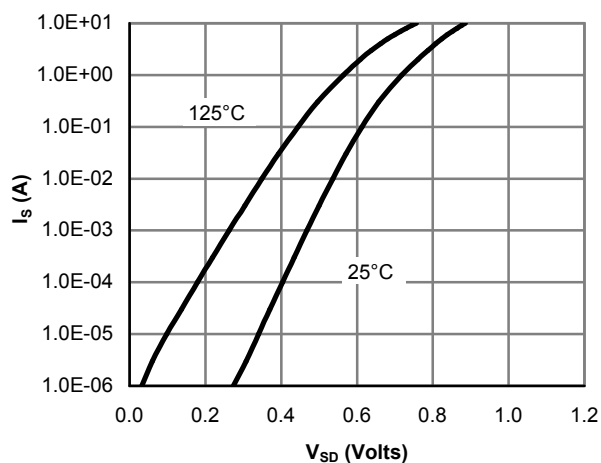


Figure 6: Body-Diode Characteristics

FET2 TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

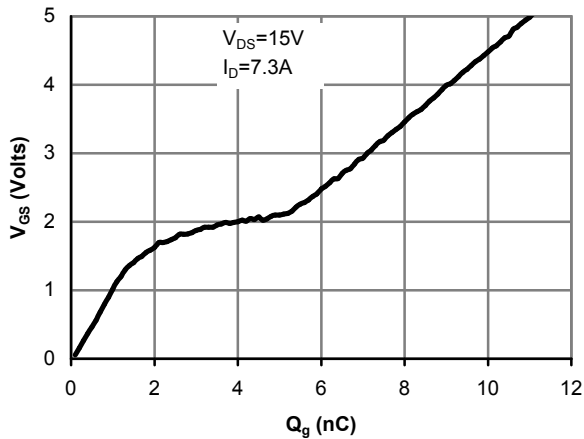


Figure 7: Gate-Charge Characteristics

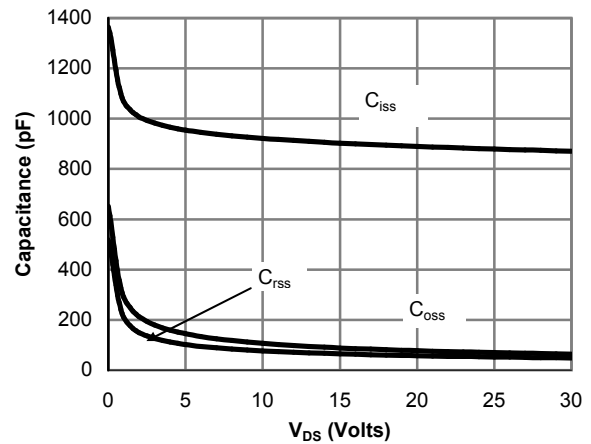


Figure 8: Capacitance Characteristics

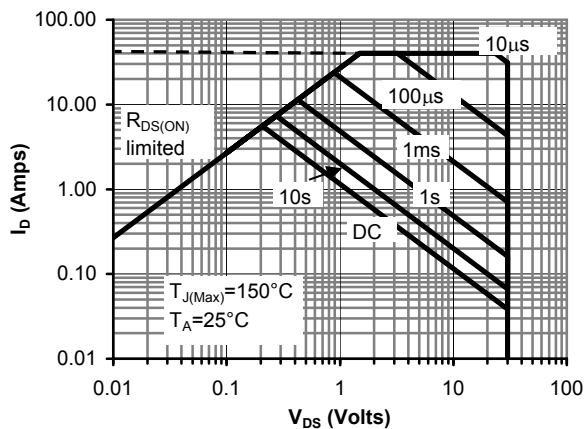


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

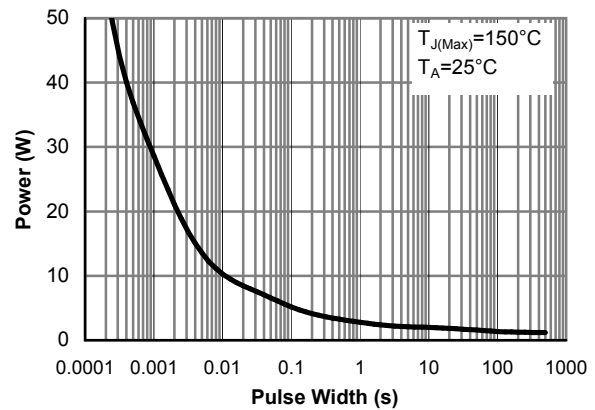


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

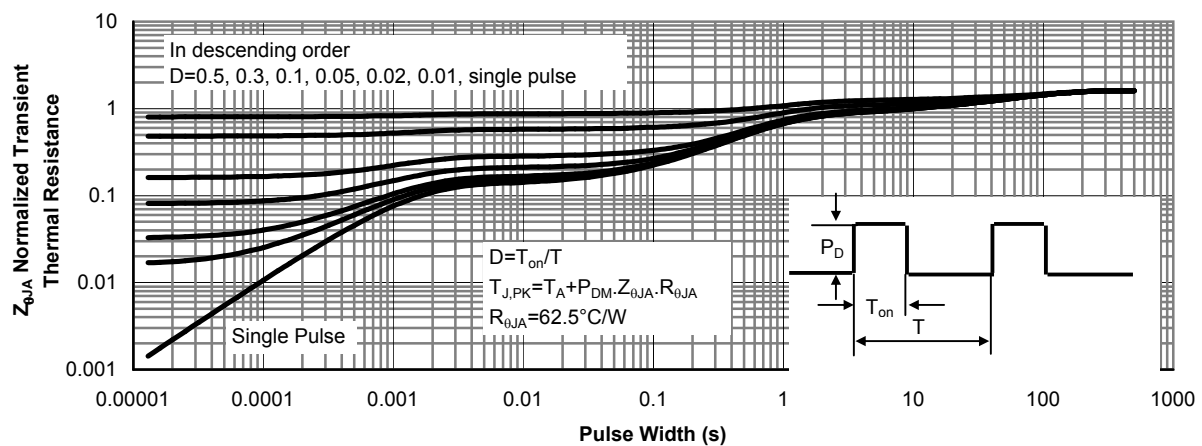


Figure 11: Normalized Maximum Transient Thermal Impedance (Note E)