FEATURES

* 0.4 inch (10.5 mm) DIGIT HEIGHT
* NINE-DIGIT, RIGHT HAND DECIMAL
* SOLID STATE RELIABILITY
* STACKABLE HORIZONTALLY
* CATEGORIZED FOR LUMINOUS INTENSITY
* 8-STEP DIMMING CIRCUITRY
* WIDE VIEWING ANGLE
* SERIAL INTERFACE FOR CLOCK, DATA, INPUT, SYROBE PINS
* CMOS TECHNOLOGY

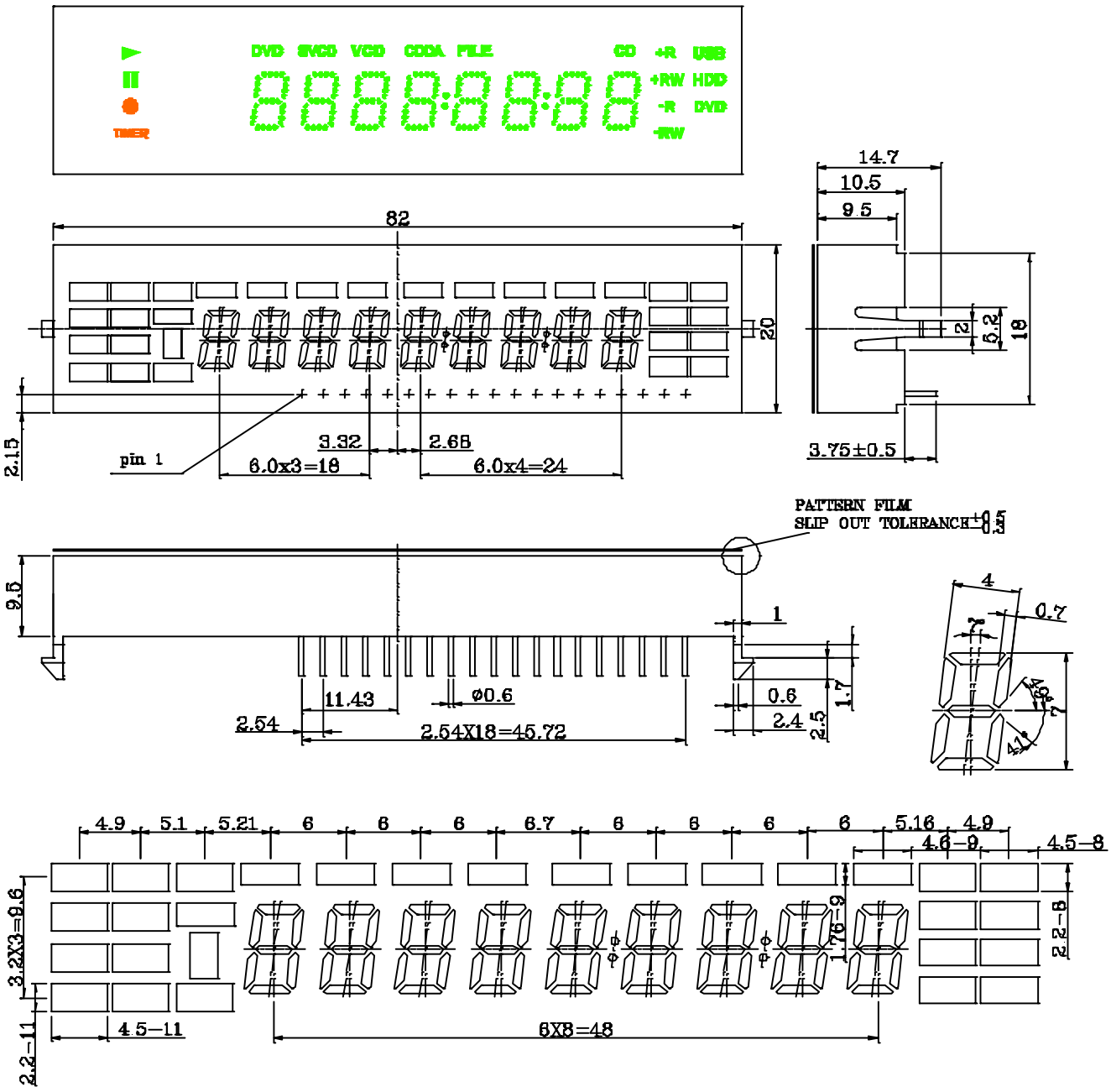
DESCRIPTION

The LTM-0340EM-02 is a 0.4 inch (10.5 mm) digit display. It has a built-in PT6961 MOS IC. The MOS IC produced with N-channel silicon gate technology. It uses AlInGaP RED LED chips (AlInGaP epi on GaAs substrate), AlInGaP GREEN chips (AlInGaP epi on GaAs substrate) This device is covered with a black pattern film, and packaged with white epoxy.

DEVICE

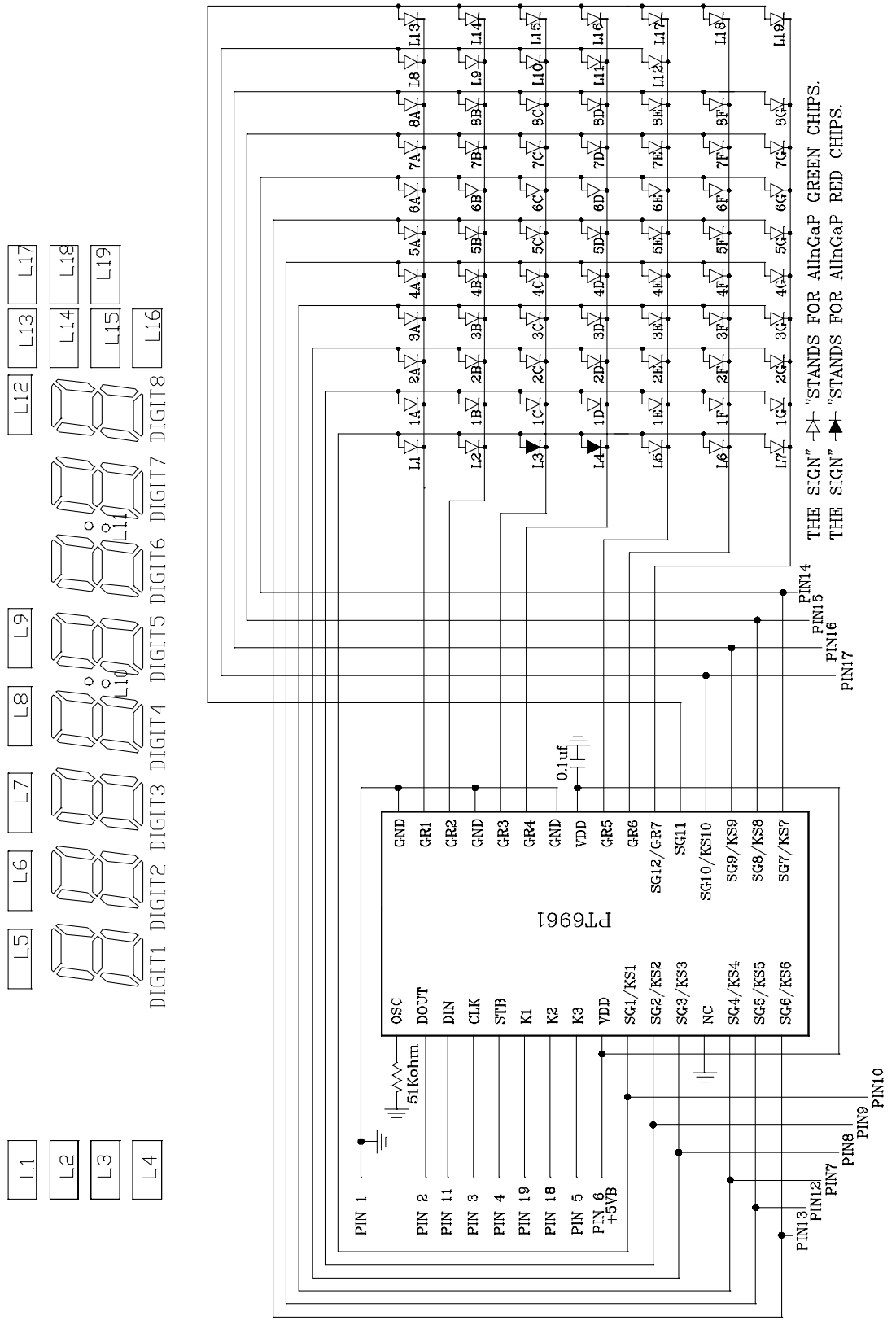
PART NO	DESCRIPTION
AlInGaP RED & AlInGaP GREEN	Multiplex with IC driver
LTM-0340EM-02	

PACKAGE DIMENSIONS



NOTES: All dimensions are in millimeters. Tolerances are 0.25mm(0.01“) unless otherwise

INTERNAL CIRCUIT DIAGRAM



PIN CONNECTION

NO.	CONNECTION
1	GND
2	DOUT
3	CLK
4	STB
5	K3
6	VDD
7	KS4
8	KS3
9	KS2
10	KS1
11	DIN
12	KS5
13	KS6
14	KS7
15	KS8
16	KS9
17	KS10
18	K2
19	K1

P-Gnd	Ground Pin
D_{OUT}	Data Output Pin (N-Channel, Open-Drain) This pin outputs serial data at the failing edge of the shift clock.
D_{IN}	Data Input Pin This pin inputs serial data at the rising edge of the shift clock (starting from the lower bot)
CLK	Clock Input Pin This pin reads serial data at rising edge and outputs data at the falling edge.
STB	Serial Interface Strobe Pin The data input after the STB has fallen is processed as a command. When this pin is “High”, CLK is ignored.
V_{DD}	Power Supply

ELECTRICAL OPTICAL CHARACTERISTICS

AlInGaP GREEN

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Average Luminous Intensity	Iv		4600		ucd	I_P = 25mA 1/8 DUTY
Peak Emission Wavelength	λ p		571		nm	I_F = 20mA
Spectral Line Half-Width	△ λ		15		nm	I_F = 20mA
Dominant Wavelength	λ d		572		nm	I_F = 20mA
Luminous Intensity Matching Ratio(Similar Light Area)	Iv-m			2:1		I_F = 20mA

AlInGaP RED

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Average Luminous Intensity	Iv		4600		ucd	I_P = 25mA 1/8 DUTY
Peak Emission Wavelength	λ p		632		nm	I_F = 20mA
Spectral Line Half-Width	△ λ		20		nm	I_F = 20mA
Dominant Wavelength	λ d		624		nm	I_F = 20mA
Luminous Intensity Matching Ratio(Similar Light Area)	Iv-m			2:1		I_F = 20mA

FUNCTIONAL DESCRIPTION

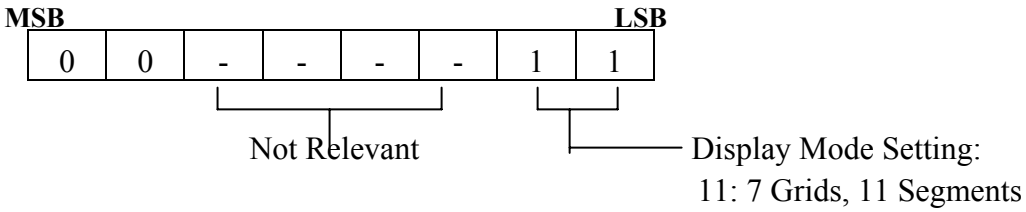
Commands

A command is the first byte (b0 to b7) inputted to PT 6961 via the D_{IN} Pin after STB Pin has changed from HIGH to LOW State. If for some reason the STB Pin is set to High while data or commands are being transmitted, the serial communication is initialized, and the data/commands being transmitted are considered invalid.

Commands 1: Display Mode Setting Commands

The Display Mode Setting Commands determine the number of segments and grids to be used (11 segments, 7 grids).

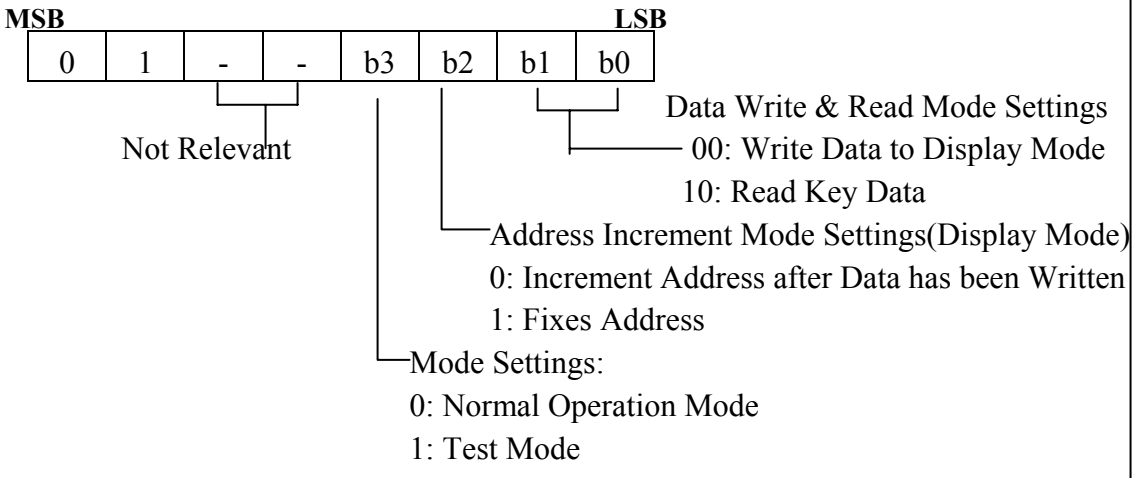
As stated earlier a command is the first one byte (b0 to b7) transmitted to PT6961 via the D_{IN} Pin when STB is LOW. However, for these commands, the bit 3 to bit 6 (b2 to b5) are ignored, bit 7 & bit 8 (b6 to b7) are given a value of 0.



Commands 2: Data Setting Commands

The Data Setting Commands executes the Data Write or Data Read Modes for PT6961. The data Setting Command, the bits 5 and 6(b4, b5) are ignored, bit 7(b6) is given the value of 1 while bit 8(b7) is given the value of 0. Please refer to the diagram below.

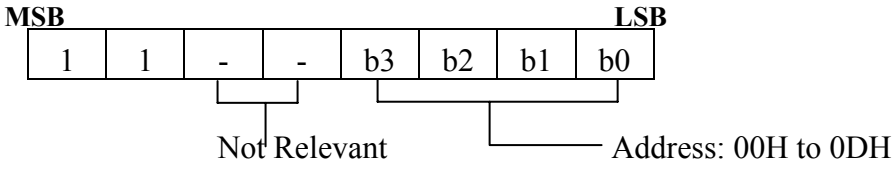
When power is turn ON, bit 4 to bit 1(b3 to b0) are given the value of 0.



Commands 3: Address Setting Commands

Address Setting Commands are used to set the address of the display memory. The address is considered valid if it has a value of 00H to 0DH. If the address is set to 0EH or higher, the data is ignored until a valid address is set. When power is turned ON, the address is set at 00H.

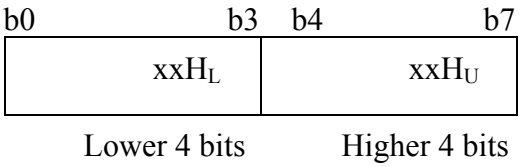
Please refer to the diagram below.



DISPLAY MODE AND RAM ADDRESS

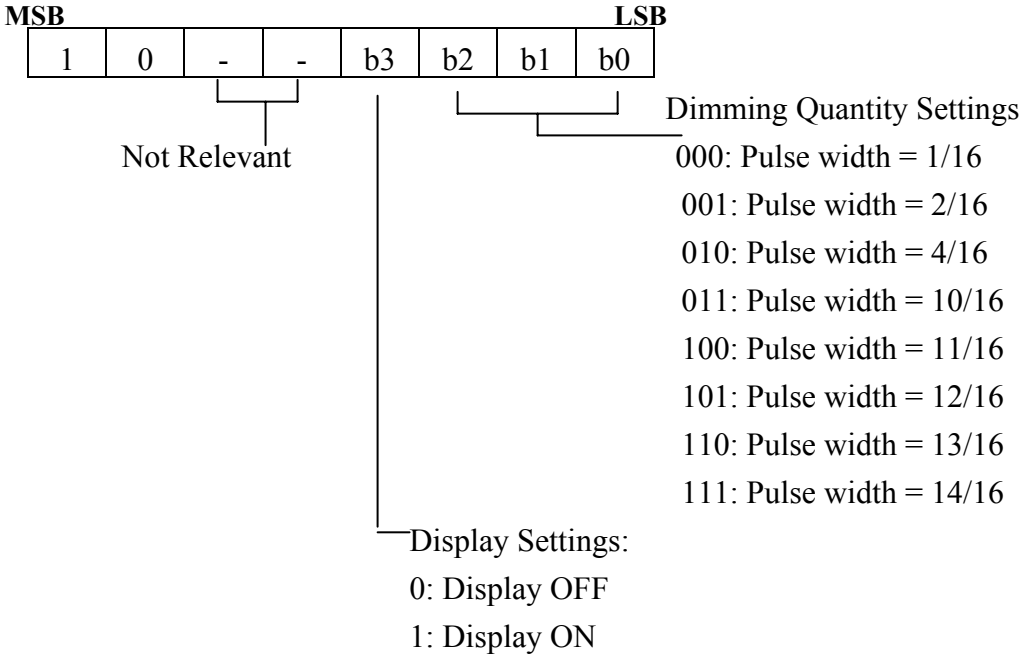
Data transmitted from an external device to PT6961 via the serial interface are stored in the Display RAM and are assigned address. The RAM addresses of PT6961 are given below in 8 bits unit.

SG1	SG4 SG5	SG8 SG9	SG12	
$00H_L$	$00H_U$	$01H_L$		**DIG1**
$02H_L$	$02H_U$	$03H_L$		**DIG2**
$04H_L$	$04H_U$	$05H_L$		**DIG3**
$06H_L$	$06H_U$	$07H_L$		**DIG4**
$08H_L$	$08H_U$	$09H_L$		**DIG5**
$0AH_L$	$0AH_U$	$0BH_L$		**DIG6**
$0CH_L$	$0CH_U$	$0DH_L$		**DIG7**



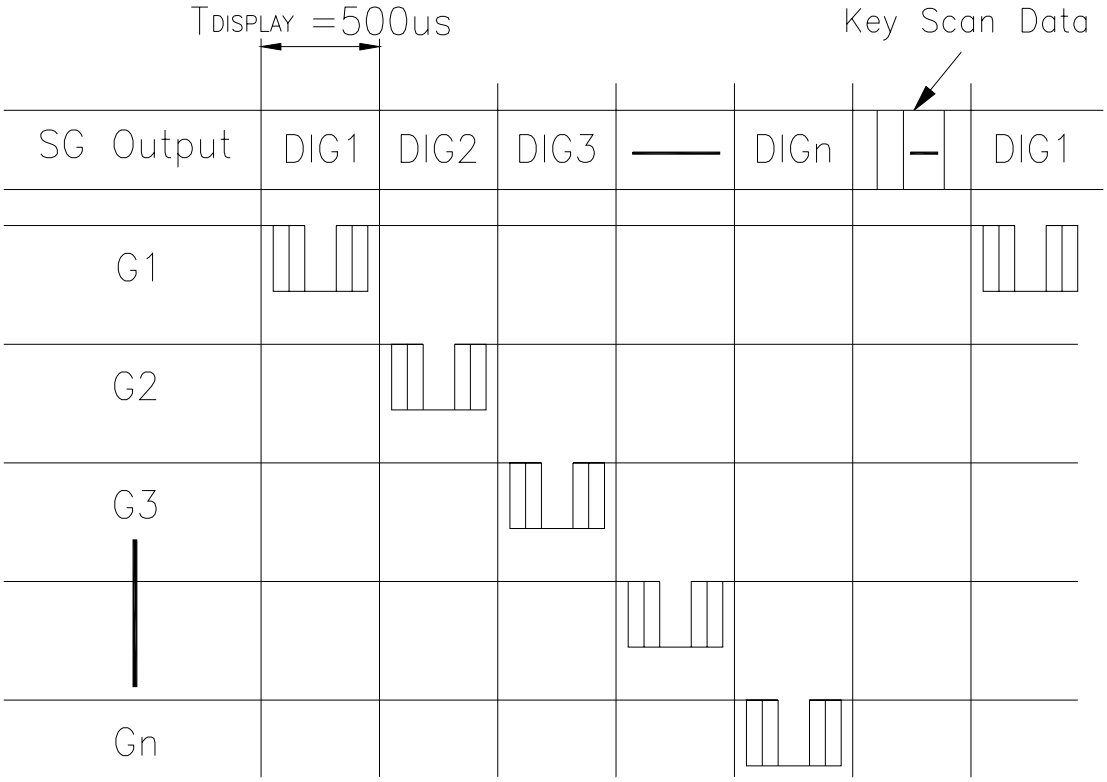
Commands 4: Display Control Commands

The Display Control Commands are used to turn ON or OFF a display. It also used to set the pulse width. Please refer to the diagram below. When the power is turned ON, a 1/16 pulse width is selected and the displayed is turned OFF(the key scanning is stopped).



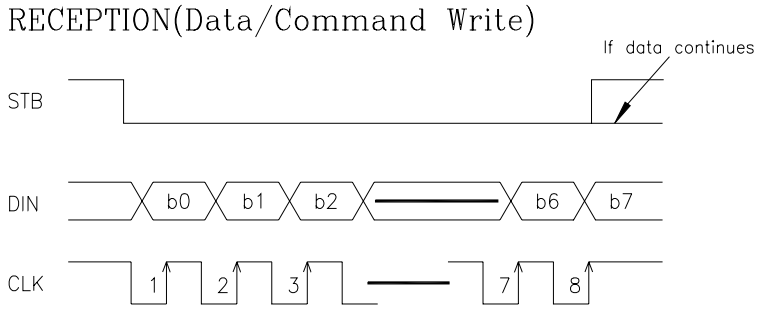
SCANNING AND DISPLAY TIMING

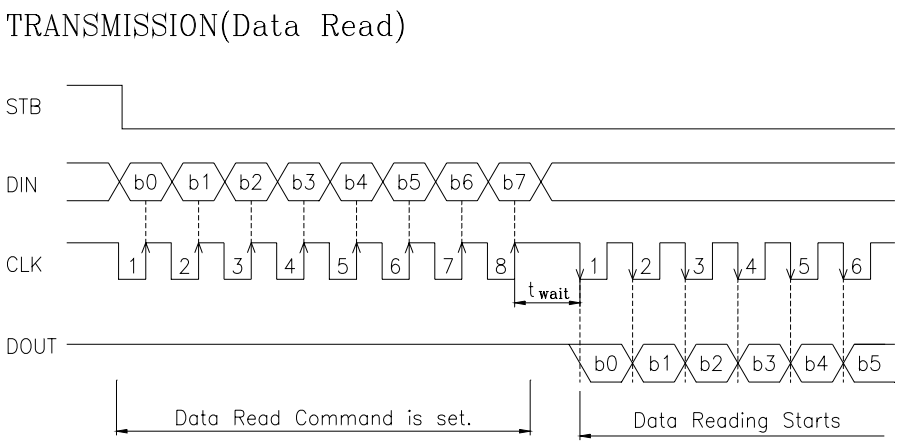
The Key Scanning and Display Timing diagram is given below. One cycle of key scanning consists of 2 frames. The data of the time are 10x3 matrix is stored in the RAM.



SCANNING AND DISPLAY TIMING

The following diagram shows the PT6961 serial communication format. The D_{OUT} Pin is an N-channel, open drain output pin, therefore, it is highly recommended that an external pull-up resistor(1KOhms to 10KOhms) must be connected to $D_{OUT.}$



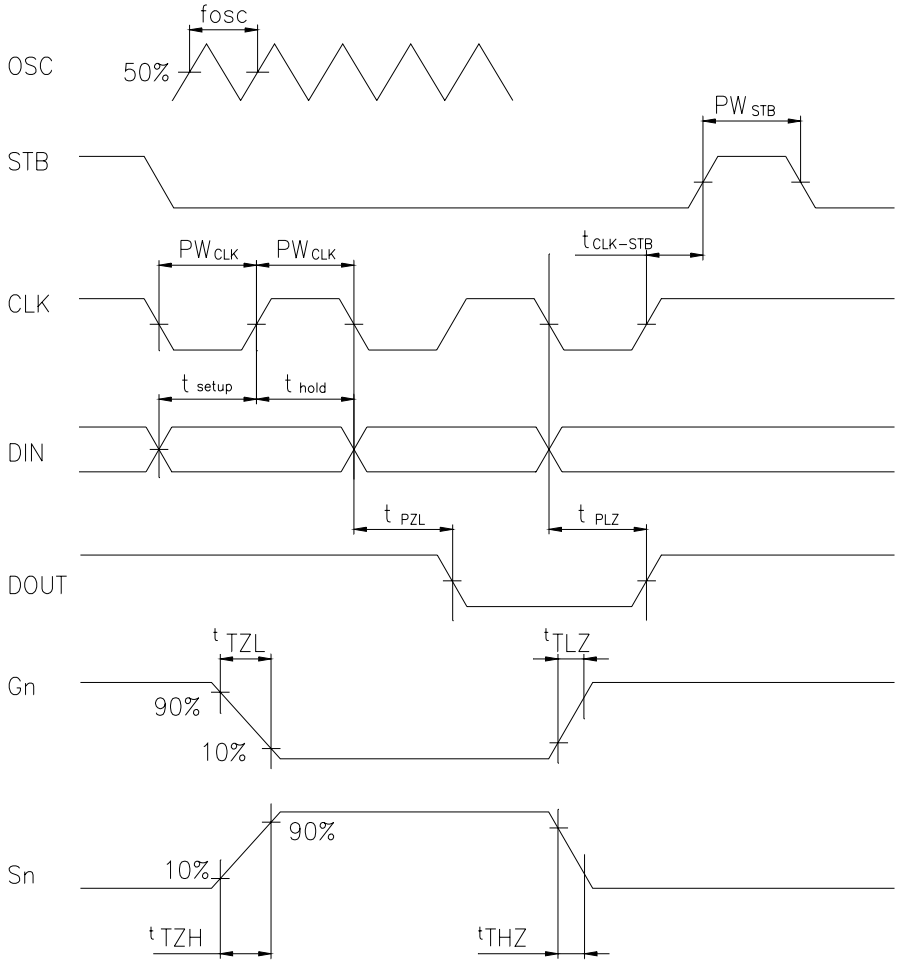


where: twait(waiting time) ≥ 1us

It must be noted that when the data is read, the waiting time(t_{wait}) between the rising of the eighth clock that has set the command and the falling of the first clock that has read the data is greater or equal to 1us.

SWITCHING CHARACTERISTIC WAVEFORM

PT6961 Switching Characteristics Waveform is given below.



where: PW_{CLK} (Clock Pulse Width) ≥ 400ns PW_{STB} (Strobe Pulse Width) ≥ 1us

t_{setup} (Data Setup Time) ≥ 100ns t_{hold} (Data Hold Time) ≥100ns

$t_{CLK-STB}$ (Clock-Strobe Time) ≥ 1uns t_{THZ} (Fall Time) ≤10us

t_{TZH} (Rise Time) ≤ 1us t_{PZL} (Propagation Delay Time) ≤100ns

f_{osc} = Oscillation Frequency t_{PLZ} (Propagation Delay Time) ≤300ns

t_{TZL} < 1us t_{TLZ} < 10us

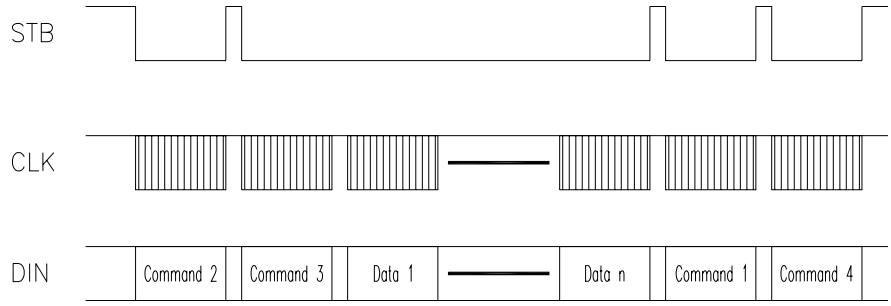
Note: Test condition under

t_{THZ} (Pull low resistor = 10k ohms, Loading capacitor = 300 pf)

t_{TLZ} (Pull low resistor = 10k ohms, Loading capacitor = 300 pf)

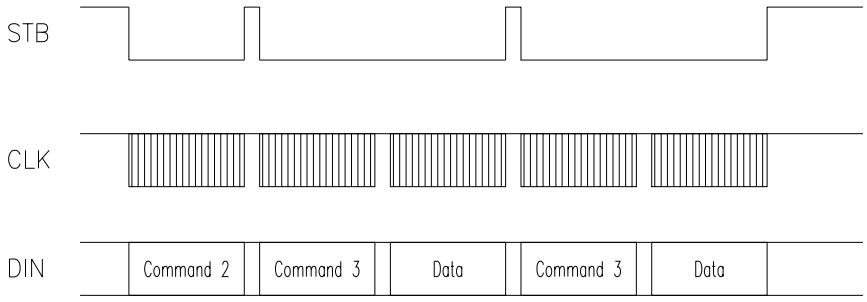
APPLICATIONS

Display memory is updated by incrementing address. Please refer to the following diagrams.



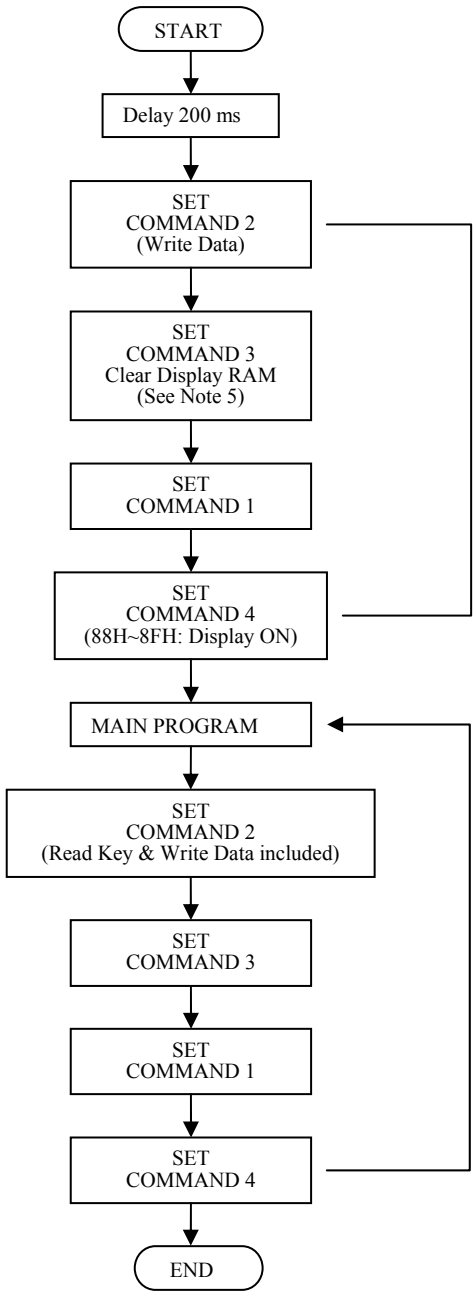
where: Command1: Display Mode Setting Command
Command2: Data Setting Command
Command3: Address Setting Command
Data 1 to n: Transfer Display Data(14 Bytes max.)
Command4: Display Control Command

The following diagram shows the waveforms when updating specific address.



where: Command2: Data Setting Command
Command3: Address Setting Command
Data: Display Data

RECOMMENDED SOFTWARE PROGRAMMING FLOWCHART



NOTE: 1. Command1: Display Mode Commands
2. Command2: Data Setting Commands
3. Command3: Address Setting Commands
4. Command4: Display Control Comamnds
5. When IC power is applied for the first time, the contents of the Display RAM is not defined; thus, it is strongly suggested that the contents of the Display RAM mist be cleared during the initial setting.

ABSOLUTE MAXIMUM RATINGS

(Unless otherwise stated, Ta = 25°C, GND = 0 V)

Parameter	Symbol	Ratings	Unit
Supply Voltage	V_{DD}	-0.5 to +7	V
Logic Input Voltage	V_I	-0.5 to V_{DD}+0.5	V
Driver Output Current	I_{OLGR}	+250	mA
	I_{OHSG}	-50	mA
Maximum Driver Output Current/Total	I_{TOTAL}	400	mA

RECOMMANDED OPERATING RANGE

(Unless otherwise stated, Ta = -20 to 70°C, GND = 0 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Logic Supply Voltage	V_{DD}	4.5	5	5.5	V
Dynamic Current(see Note)	I_{DDdyn}	-	-	5	mA
High-Level Input Voltage	V_{IH}	0.8V_{DD}	-	V_{DD}	V
Low-Level Input Voltage	V_{IL}	0	-	0.3 V_{DD}	V

Note: Test Condition: Set Display Control Commands = 80H

RECOMMANDED OPERATING RANGE

(Unless otherwise stated, Ta = -20 to 70°C, GND = 0 V)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
High-Level Output Current	I_{OHSG1}	V_O=V_{DD}-2V SG1 to SG12	-20	-25	-40	mA
	I_{OHSG2}	V_O=V_{DD}-3V SG1 to SG12	-25	-30	-50	mA
Low-Level Output Current	I_{LGR}	V_O=0.3V GR1 to GR7	100	140		mA
Low-Level Output Current	I_{OLDout}	$V_{O=}$0.4V	4			mA
Segment High-Level Output Current Tolerance	I_{ToLSG1}	V_O=V_{DD}-3V SG1 to SG12			±5	%
High-Level Input Voltage	V_{IH}	-	0.8 V_{DD}	-	5	V
Low-Level Input Voltage	V_{IL}	-	0	-	0.3 V_{DD}	V
Oscillation Frequency	f_{osc}	R=51Kohms	350	500	650	kHz