

FOD050L, FOD250L: Single Channel FOD053L: Dual Channel LVTTTL/LVCMOS 3.3V High Speed Transistor Optocouplers

Features

- Low power consumption
- High speed
- Available in single channel 8-pin DIP (FOD250L), 8-pin SOIC (FOD050L) or dual channel 8-pin SOIC (FOD053L)
- Superior CMR – $CM_H = 50kV/\mu s$ (typical) and $CM_L = 35kV/\mu s$ (typical)
- Guaranteed performance over temperature: 0°C to 70°C
- U.L. recognized (File # E90700)
- VDE pending

Applications

- Line receivers
- Pulse transformer replacement
- High speed logic ground isolation: LVTTTL/LVCMOS
- Wide bandwidth analog coupling

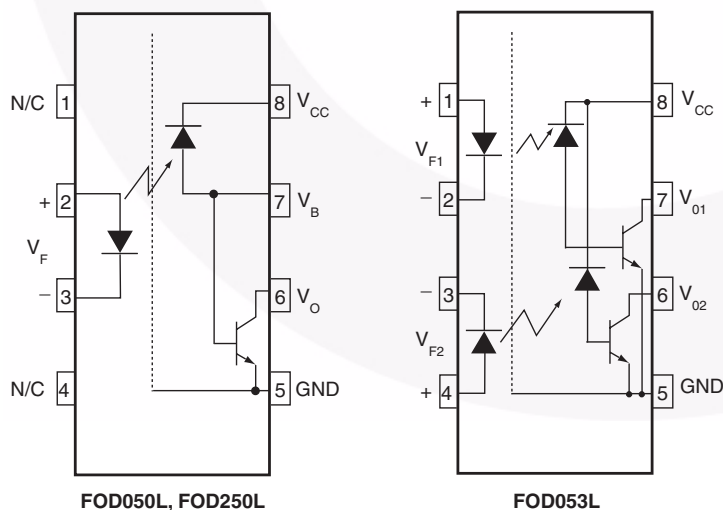
Description

The FOD250L, FOD050L and FOD053L optocouplers consist of an AlGaAs LED optically coupled to a high speed photodetector transistor. These devices are specified for operation at a 3.3V supply voltage.

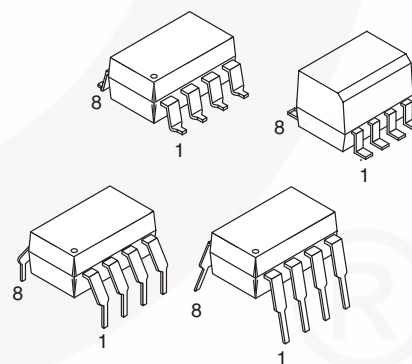
A separate connection for the bias of the photodiode improves the speed by several orders of magnitude over conventional phototransistor optocouplers by reducing the base-collector capacitance of the input transistor.

An internal noise shield provides superior common mode rejection of $CM_H = 50kV/ms$ (typical) and $CM_L = 35kV/ms$ (typical).

Schematics



Package Outlines



Truth Table

LED	V _O
On	LOW
Off	HIGH

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise specified.)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Value	Units
T _{STG}	Storage Temperature		-40 to +125	°C
T _{OPR}	Operating Temperature		-40 to +85	°C
T _{SOL}	Lead Solder Temperature (Wave solder only)		260 for 10 sec	°C
EMITTER				
I _F (avg)	DC/Average Forward Input Current	Each Channel	25	mA
I _F (pk)	Peak Forward Input Current (50% duty cycle, 1ms P.W.)	Each Channel	50	mA
I _F (trans)	Peak Transient Input Current (≤1 μs P.W., 300pps)	Each Channel	1.0	A
V _R	Reverse Input Voltage	Each Channel	5	V
P _D	Input Power Dissipation (No derating required up to 85°C)	Each Channel	45	mW
DETECTOR				
I _O (avg)	Average Output Current	Each Channel	8	mA
I _O (pk)	Peak Output Current	Each Channel	16	mA
V _{EBR}	Emitter-Base Reverse Voltage	FOD050L, FOD250L only	5	V
V _{CC}	Supply Voltage		-0.5 to 7	V
V _O	Output Voltage		-0.5 to 7	V
I _B	Base Current	FOD050L, FOD250L only	5	mA
P _D	Output Power Dissipation (No derating required up to 85°C)	Each Channel	100	mW

Electrical Characteristics ($T_A = 0$ to 70°C unless otherwise specified.)**Individual Component Characteristics**

Symbol	Parameter	Test Conditions	Device	Min.	Typ.*	Max.	Unit
EMITTER							
V_F	Input Forward Voltage	$I_F = 16\text{mA}$, $T_A = 25^\circ\text{C}$	All		1.45	1.7	V
		$I_F = 16\text{mA}$				1.8	
B_{VR}	Input Reverse Breakdown Voltage	$I_R = 10\mu\text{A}$	All	5.0			V
DETECTOR							
I_{OH}	Logic High Output Current	$I_F = 0\text{mA}$, $V_O = V_{CC} = 3.3\text{V}$, $T_A = 25^\circ\text{C}$	All		0.001	1	μA
I_{CCL}	Logic Low Supply Current	$I_F = 16\text{mA}$, $V_O = \text{Open}$, $V_{CC} = 3.3\text{V}$	FOD050L FOD250L			200	μA
		$I_{F1} = I_{F2} = 16\text{mA}$, $V_O = \text{Open}$, $V_{CC} = 3.3\text{V}$	FOD053L			400	
I_{CCH}	Logic High Supply Current	$I_F = 0\text{mA}$, $V_O = \text{Open}$, $V_{CC} = 3.3\text{V}$, $T_A = 25^\circ\text{C}$	FOD050L FOD250L			0.3	μA
		$I_F = 0\text{mA}$, $V_O = \text{Open}$, $V_{CC} = 3.3\text{V}$	FOD053L			10	

All Typicals at $T_A = 25^\circ\text{C}$ **Transfer Characteristics

Symbol	Parameter	Test Conditions	Device	Min.	Typ.**	Max.	Unit
COUPLED							
CTR	Current Transfer Ratio ⁽¹⁾	$I_F = 16\text{mA}$, $V_O = 0.4\text{V}$, $V_{CC} = 3.3\text{V}$, $T_A = 25^\circ\text{C}$	All	15		50	%
V_{OL}	Logic Low Output Voltage Output Voltage	$I_F = 16\text{mA}$, $I_O = 3\text{mA}$, $V_{CC} = 3.3\text{V}$, $T_A = 25^\circ\text{C}$	All			0.3	V

*All Typicals at $T_A = 25^\circ\text{C}$ **Note:**

1. Current Transfer Ratio is defined as a ratio of output collector current, I_O , to the forward LED input current, I_F , times 100%.

Electrical Characteristics (Continued) ($T_A = 0$ to 70°C unless otherwise specified.)**Switching Characteristics** ($V_{CC} = 3.3\text{V}$)

Symbol	Parameter	Test Conditions	Device	Min.	Typ.**	Max.	Unit
T_{PHL}	Propagation Delay Time to Logic LOW	$R_L = 1.9\text{k}\Omega$, $I_F = 16\text{mA}^{(2)}$ (Fig. 10) 25°C	All			1.0 2.0	μs
T_{PLH}	Propagation Delay Time to Logic HIGH	$R_L = 1.9\text{k}\Omega$, $I_F = 16\text{mA}^{(2)}$ (Fig. 10) 25°C	All			1.0 2.0	μs
ICM_{HI}	Common Mode Transient Immunity at Logic HIGH	$I_F = 0\text{mA}$, $V_{CM} = 1,000\text{V}_{P-P}$, $R_L = 4.1\text{k}\Omega$, $T_A = 25^\circ\text{C}^{(3,4)}$ (Fig. 11)	All	5,000	50,000		$\text{V}/\mu\text{s}$
		$I_F = 0\text{mA}$, $V_{CM} = 1,000\text{V}_{P-P}$, $T_A = 25^\circ\text{C}$, $R_L = 1.9\text{k}\Omega^{(2,4)}$ (Fig. 11)		5,000	50,000		$\text{V}/\mu\text{s}$
ICM_{LI}	Common Mode Transient Immunity at Logic LOW	$I_F = 16\text{mA}$, $V_{CM} = 1,000\text{V}_{P-P}$, $R_L = 4.1\text{k}\Omega$, $T_A = 25^\circ\text{C}^{(3,4)}$ (Fig. 11)	All	5,000	35,000		$\text{V}/\mu\text{s}$
		$I_F = 16\text{mA}$, $V_{CM} = 1,000\text{V}_{P-P}$, $R_L = 1.9\text{k}\Omega^{(2,4)}$ (Fig. 11)		5,000	35,000		$\text{V}/\mu\text{s}$

Isolation Characteristics

Symbol	Characteristics	Test Conditions	Device	Min.	Typ.**	Max.	Unit
I_{I-O}	Input-Output Insulation Leakage Current	Relative humidity = 45%, $T_A = 25^\circ\text{C}$, $t = 5\text{s}$, $V_{I-O} = 3000\text{VDC}^{(5)}$	All			1.0	μA
V_{ISO}	Withstand Insulation Test Voltage	$f = 60\text{Hz}$, $T_A = 25^\circ\text{C}$, $t = 1\text{ min.}^{(5)}$	FOD050L FOD053L	2500			V_{RMS}
			FOD250L	5000			
R_{I-O}	Resistance (input to output)	$V_{I-O} = 500\text{VDC}^{(5)}$	All	10^{11}	10^{12}		Ω
C_{I-O}	Capacitance (input to output)	$f = 1\text{MHz}^{(5)}$	All		0.2		pF

*All Typical at $T_A = 25^\circ\text{C}$ **Notes:**

- The $1.9\text{k}\Omega$ load represents 1 TTL unit load of 1.6mA and $5.6\text{k}\Omega$ pull-up resistor.
- The $4.1\text{k}\Omega$ load represents 1 LSTTL unit load of 0.36mA and $6.1\text{k}\Omega$ pull-up resistor.
- Common mode transient immunity in logic high level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse signal V_{CM} , to assure that the output will remain in a logic high state (i.e., $V_O > 2.0\text{V}$). Common mode transient immunity in logic low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM} , to assure that the output will remain in a logic low state (i.e., $V_O < 0.8\text{V}$).
- Device is considered a two terminal device: Pins 1, 2, 3 and 4 are shorted together and Pins 5, 6, 7 and 8 are shorted together.

Typical Performance Curves

Fig. 1 LED Forward Current vs. Forward Voltage

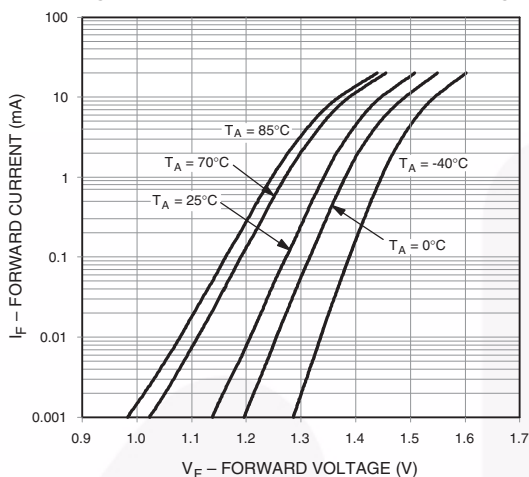


Fig. 2 Current Transfer Ratio vs. Forward Current (FOD050L, FOD053L)

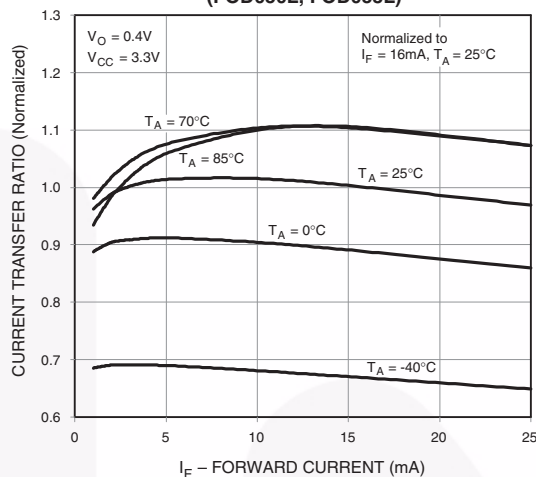


Fig. 3 Current Transfer Ratio vs. Input Forward Current (FOD250L)

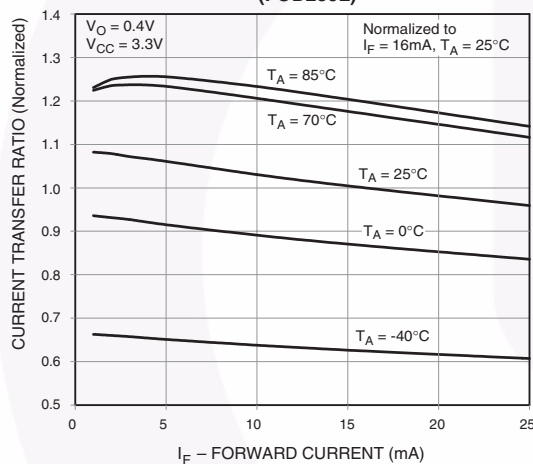


Fig. 4 Current Transfer Ratio vs. Ambient Temperature

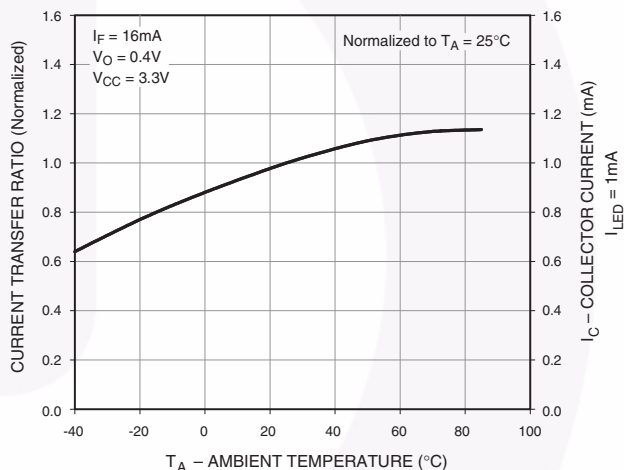


Fig. 5 Output Current vs. Output Voltage

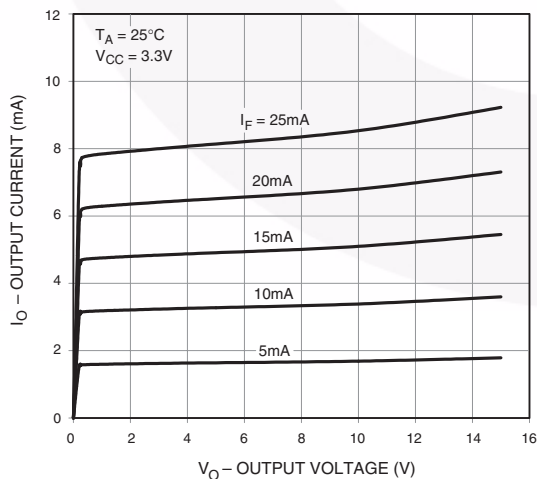
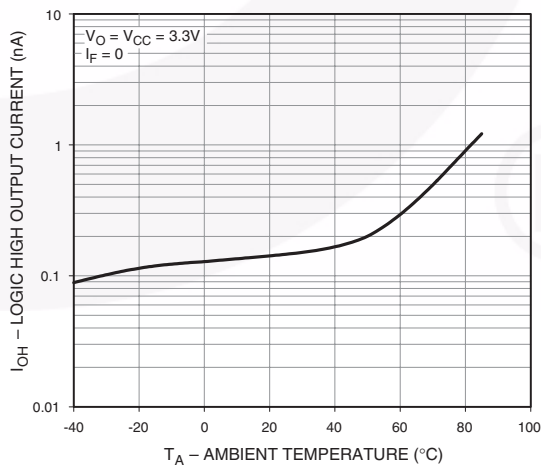


Fig. 6 Logic High Output Current vs. Ambient Temperature



Typical Performance Curves (Continued)

Fig. 7 Supply Current vs. Input Forward Current

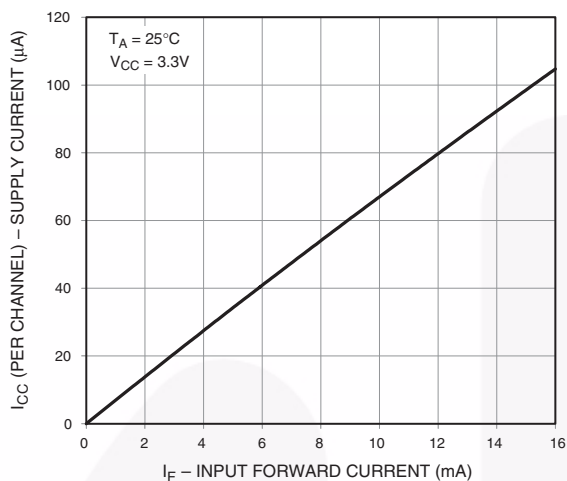


Fig. 8 Propagation Delay vs. Ambient Temperature

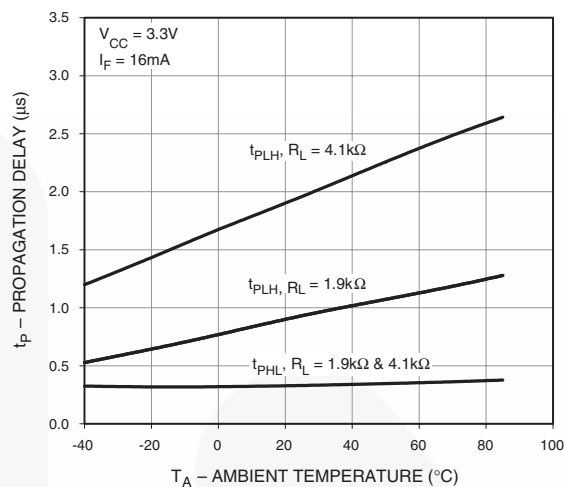
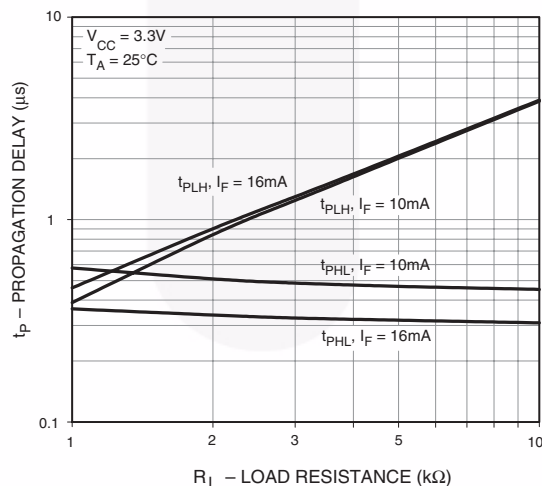


Fig. 9 Propagation Delay vs. Load Resistance



The figure contains two circuit diagrams. The left diagram is for the 74VHC00 (NAND gate). It shows a pulse generator with $t_r = 5\text{ ns}$, $Z_0 = 50\ \Omega$, 10% D.C., and $I_f < 100\ \mu\text{s}$ connected to pin 1. Pin 2 is connected to pin 3 through a resistor R_m and a monitor I_f monitor. Pin 4 is connected to GND. Pin 8 is connected to $V_{CC} = +3.3\text{ V}$. Pin 7 is connected to V_B . Pin 6 is connected to V_O . Pin 5 is connected to GND. A load resistor R_L is connected between V_{CC} and V_O . A capacitor $C_L = 1.5\text{ pF}$ is connected between V_O and GND. A noise shield is placed over the gate. The right diagram is for the 74VHC04 (inverter). It shows a pulse generator with $t_r = 5\text{ ns}$, $Z_0 = 50\ \Omega$, 10% DUTY CYCLE, and $I_f < 100\ \mu\text{s}$ connected to pin 1. Pin 2 is connected to pin 3 through a resistor R_m and a monitor I_f monitor. Pin 4 is connected to GND. Pin 8 is connected to $V_{CC} = +3.3\text{ V}$. Pin 7 is connected to V_{O1} . Pin 6 is connected to V_{O2} . Pin 5 is connected to GND. A load resistor R_L is connected between V_{CC} and V_{O1} . A capacitor $C_L = 1.5\text{ pF}$ is connected between V_{O1} and GND. A noise shield is placed over the gate.

Test Circuit for FOD053L

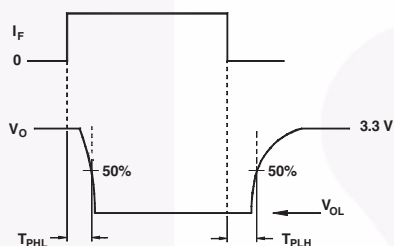
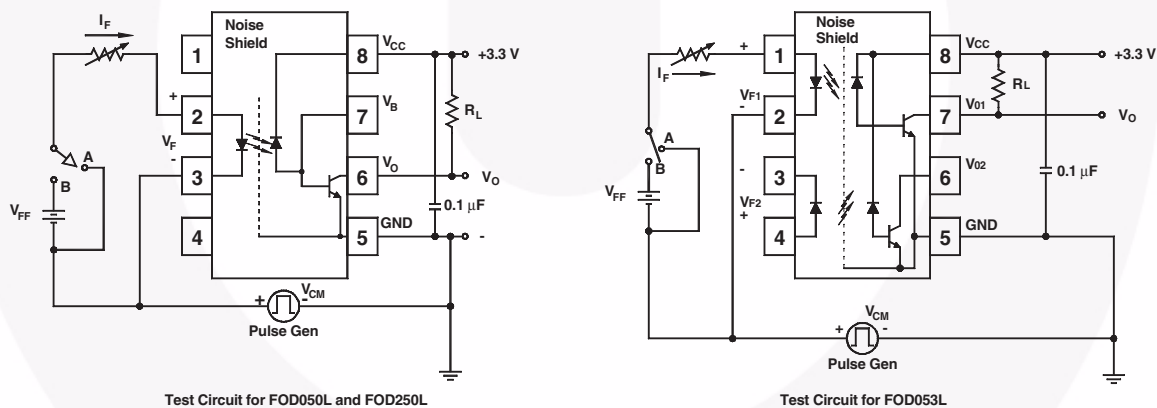


Fig. 10 Switching Time Test Circuit



Test Circuit for FOD053L

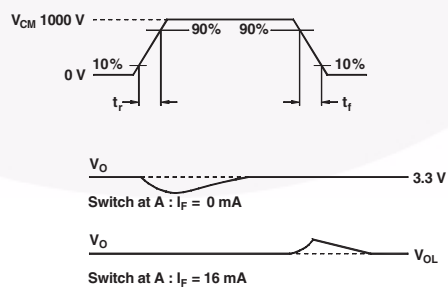
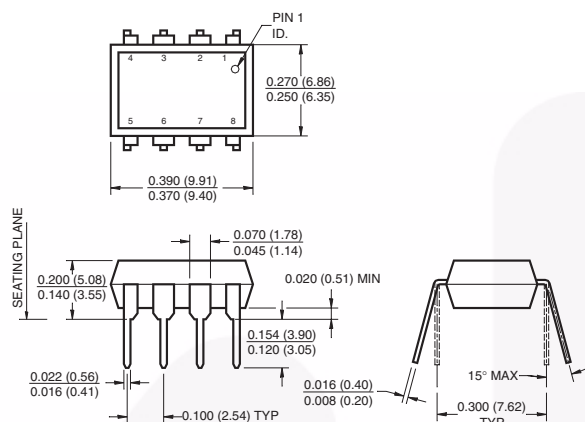


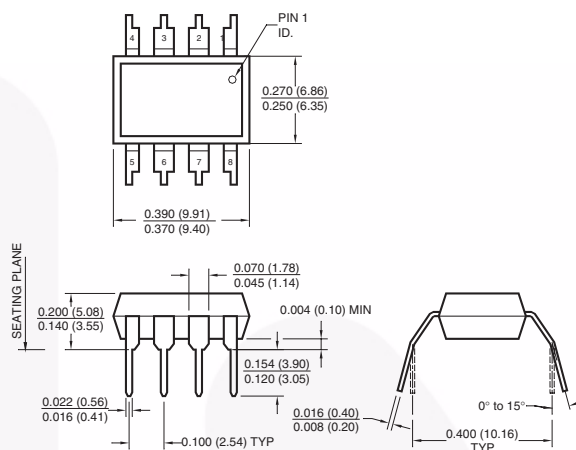
Fig. 11 Common Mode Immunity Test Circuit

Package Dimensions

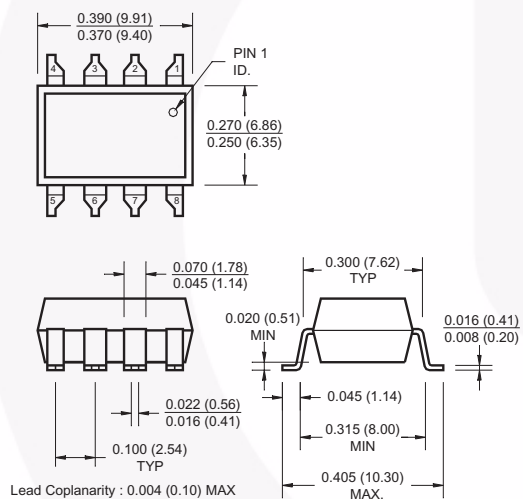
Through Hole



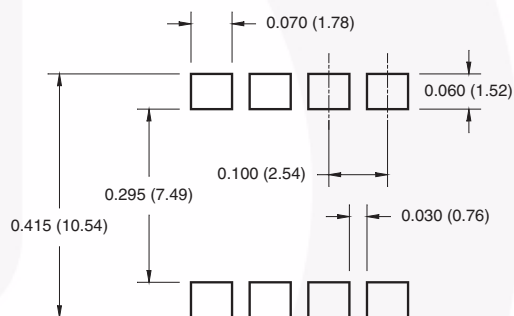
0.4" Lead Spacing



Surface Mount



8-Pin DIP – Land Pattern

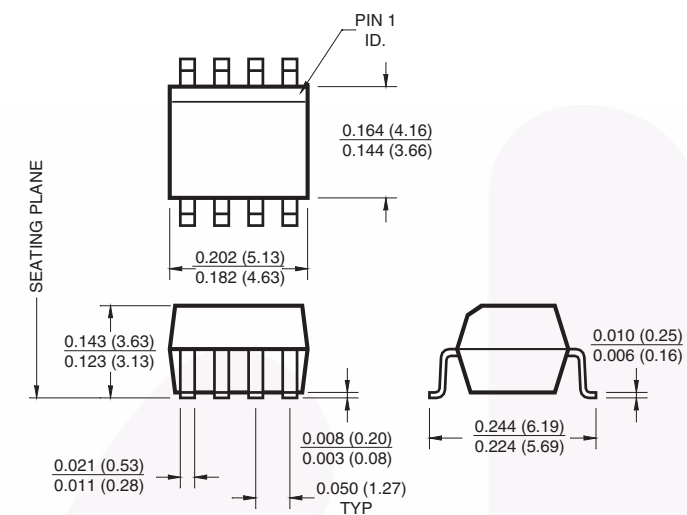


Note:

All dimensions are in inches (millimeters)

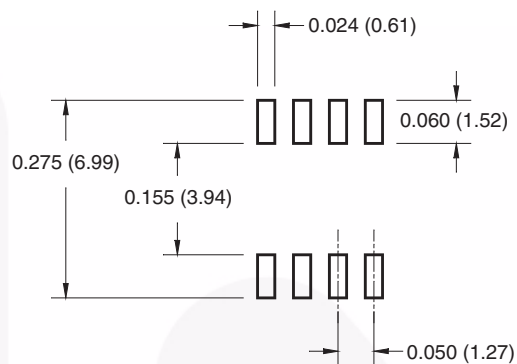
Package Dimensions (Continued) (8-Pin SOIC)

Surface Mount



Lead Coplanarity : 0.004 (0.10) MAX

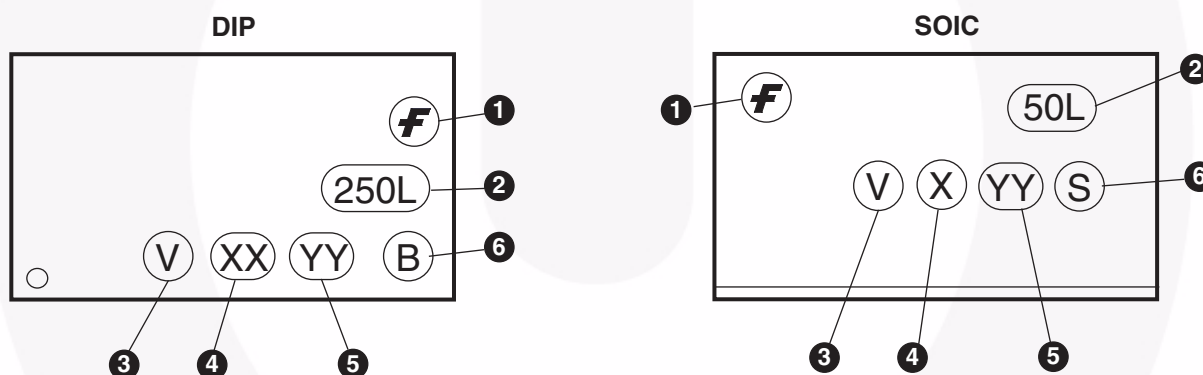
8-Pin Small Outline



Ordering Information

Option	Order Entry Identifier	Description
No Suffix	FOD250L	Through Hole (DIP package only)
	FOD050L	Surface Mount Lead Form (SOIC-8 package only)
S	FOD250LS	Surface Mount Lead Bend (DIP package only)
SD	FOD250LSD	Surface Mount; Tape and reel (DIP package only)
SV	Pending Approval	Surface Mount; VDE0884 (DIP package only)
SDV	Pending Approval	Surface Mount; Tape and reel, VDE0884 (1000 units per reel) (DIP package only)
T	FOD250LT	0.4" Lead Spacing (DIP package only)
TV	Pending Approval	0.4" Lead Spacing, VDE0884 (DIP package only)
R1	FOD050LR1	Tape and Reel (500 units per reel) (SOIC-8 package only)
R1V	Pending Approval	VDE, Tape and Reel (500 units per reel) (SOIC-8 package only)
R2	FOD050LR2	Tape and Reel (2500 units per reel) (SOIC-8 package only)
R2V	Pending Approval	VDE, Tape and Reel (2500 units per reel) (SOIC-8 package only)
V	Pending Approval	VDE (SOIC-8 package only)

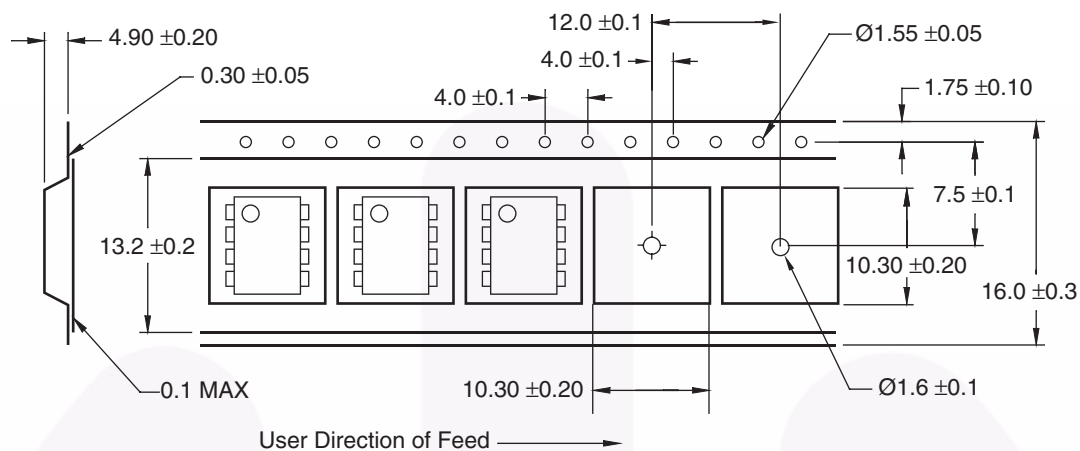
Marking Information



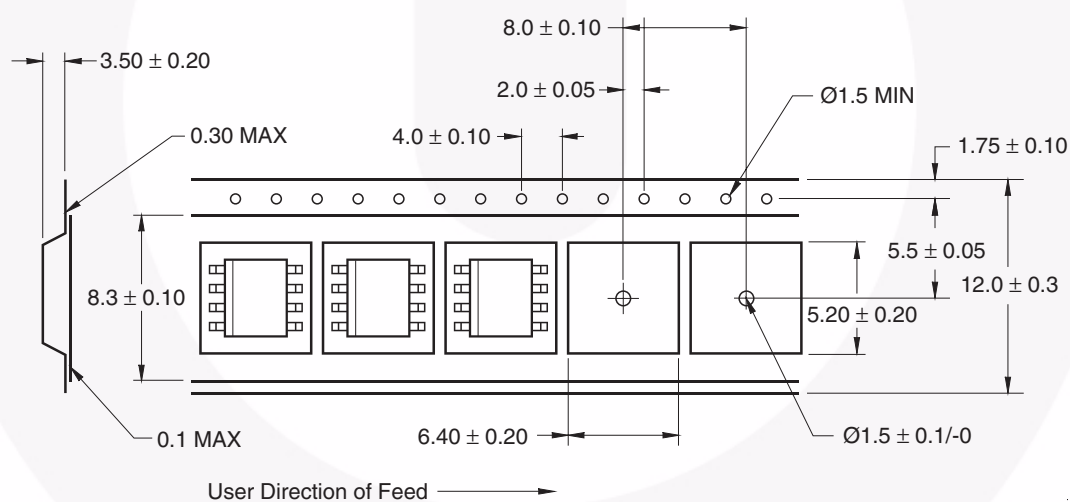
Definitions

1	Fairchild logo
2	Device number
3	VDE mark (Note: Only appears on parts ordered with VDE option – See order entry table)
4 (DIP)	Two digit year code, e.g., '03'
4 (SOIC)	One digit year code, e.g., '3'
5	Two digit work week ranging from '01' to '53'
6	Assembly package code

8-Pin DIP (FOD250L)



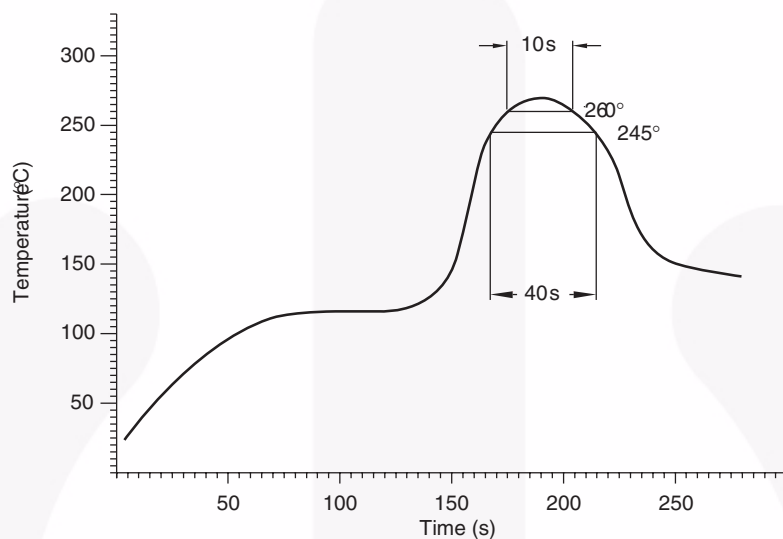
8-Pin SOIC (FOD050L, FOD053L)



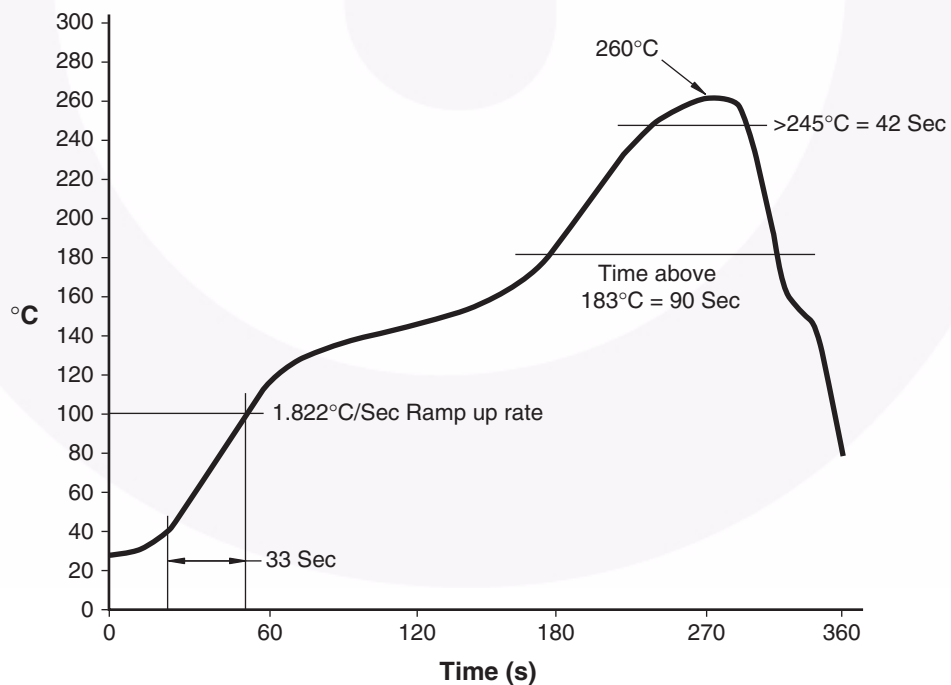
Reflow Profile

8-Pin DIP (FOD250L)

- Peak reflow temperature 260°C (package surface temperature)
- Time of temperature higher than 245°C 40 seconds or less
- Number of reflows Three



8-Pin SOIC (FOD050L, FOD053L)





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Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I40

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