Low Dropout, Low IQ, 500mA CMOS Linear Regulator

Check for Samples: LP8345

FEATURES

- **±1.5% Typical V_{OUT} Tolerance**
- **210mV Typical Dropout @ 500mA (V_O = 5V)**
- **Wide Operating Range 2.7V to 10V**
- **Internal 500mA PMOS Output Transistor**
- **19µA Typical Quiescent Current**
- **Thermal Overload Limiting**
- **Foldback Current Limiting**
- **Zener Trimmed Bandgap Reference**
- **Space Saving WSON package**
- **Temperature Range**
  - **LP8345C 0°C to 125°C**
  - **LP8345I −40°C to 125°C**

APPLICATIONS

- **Hard Disk Drives**
- **Notebook Computers**
- **Battery Powered Electronics**
- **Portable Instrumentation**

DESCRIPTION

The LP8345 low-dropout CMOS linear regulator are available in 5V, 3.3V, 2.5V, 1.8V or adjustable output versions. Packaged in our 6ld WSON package and 3ld DPAK they can deliver up to 500mA output current.

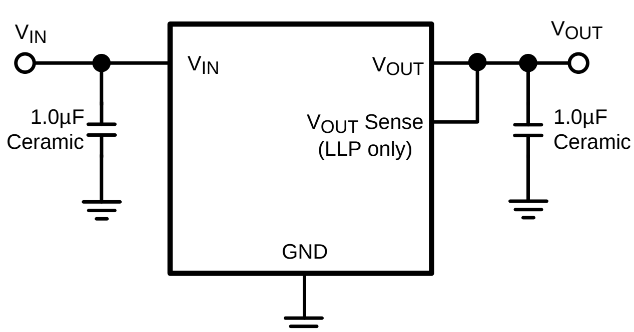
Typical dropout voltage @ 500mA is 210mV for the 5.0V version, 270mV for the 3.3V version and 335mV for the 2.5V version.

The devices include a zener trimmed bandgap voltage reference, foldback current limiting and thermal overload limiting.

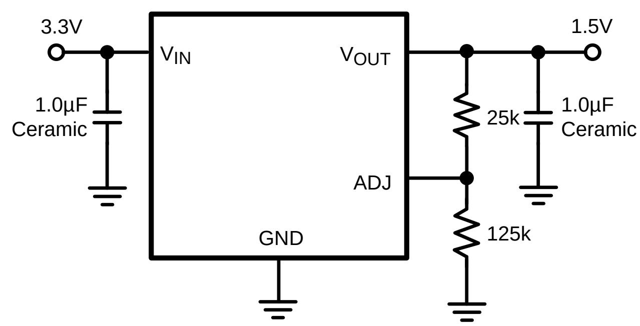
The LP8345 features a PMOS output transistor which unlike PNP type low dropout regulators requires no base drive current. This allows the device ground current to remain less than 50µA over operating temperature, supply voltage and irrespective of the load current.

TYPICAL APPLICATIONS

Fixed V_{OUT}



Adjustable V_{OUT}



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

CONNECTION DIAGRAMS

6-Pin WSON
FIXED OUTPUT VOLTAGE

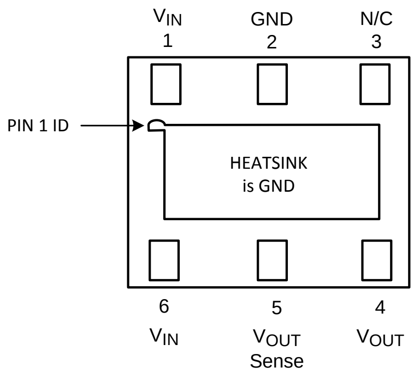


Figure 1. Bottom View

6-Pin WSON
ADJUSTABLE OUTPUT VOLTAGE

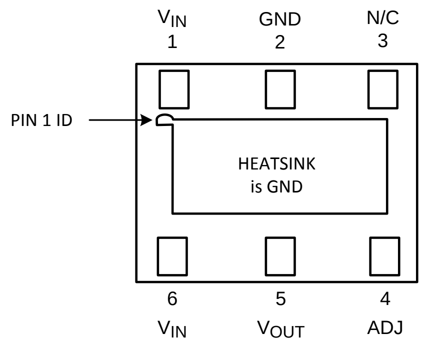


Figure 2. Bottom View

NOTE

V_{IN} Pins (Pin 1 & 6) must be connected together externally for full 500mA operation (250mA max per pin).

V_{OUT} Sense (Pin 5) must be connected to V_{OUT} (Pin 4).

PFM

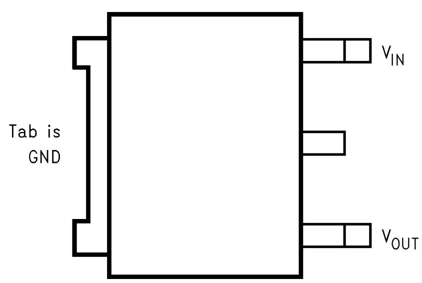


Figure 3. Top View

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1) (2)(3)

V_{IN}, V_{OUT}, V_{OUT} Sense, ADJ		−0.3V to 12V
Storage Temperature Range		−65°C to 160°C
Junction Temperature (T_J)		150°C
Power Dissipation		(4)
ESD Rating	Human Body Model (5)	2kV
	Machine Model	200V

(1) Absolute Maximum ratings indicate limits beyond which damage may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.
(2) All voltages are with respect to the potential at the ground pin.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) Maximum Power dissipation for the device is calculated using the following equations: $P_D = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$ where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. The value of the θ_{JA} for the WSON package is specifically dependant on the PCB trace area, trace material, and the number of layers and thermal vias. For improved thermal resistance and power dissipation for the WSON package, refer to Application Note AN-1187 (literature number SNOA401).
(5) Human body model 1.5kΩ in series with 100pF.

OPERATING RATINGS (1) (2)

Supply Voltage		2.7 to 10V
Temperature Range	LP8345C	0°C to 125°C
	LP8345I	−40°C to 125°C

(1) Absolute Maximum ratings indicate limits beyond which damage may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.
(2) All voltages are with respect to the potential at the ground pin.

LP8345C ELECTRICAL CHARACTERISTICS

Unless otherwise specified all limits specified for $V_{IN} = V_O + 1V$, $C_{IN} = C_{OUT} = 10µF$, $T_J = 25°C$. **Boldface** limits apply over the full operating temperature range of $T_J = 0°C$ to 125°C

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{IN}	Input Voltage	LP8345-ADJ,1.8, 2.5 LP8345-3.3, 5.0	**2.7**		**10** **10**	V
V_{OUT}	Output Voltage	LP8345-ADJ, ADJ = OUT I_{OUT} = 10mA, V_{IN} = 2.7V, T_J = 25°C 100µA ≤I_{OUT}≤ 500mA, 2.7V ≤V_{IN}≤V_{OUT} +4V	1.231 **1.213**	1.250	1.269 **1.288**	V
		LP8345-1.8 I_{OUT} = 10mA, V_{IN} = 2.8V, T_J = 25°C 100µA ≤I_{OUT} ≤500mA, 2.8V ≤V_{IN}≤6V	1.773 **1.746**	1.800	1.827 **1.854**	V
		LP8345-2.5 I_{OUT} = 10mA, V_{IN} = 3.5V, T_J = 25°C 100µA ≤I_{OUT} ≤500mA, 3.5V ≤V_{IN} ≤6.5V	2.463 **2.425**	2.500	2.538 **2.575**	V
		LP8345-3.3 I_{OUT} = 10mA, V_{IN} = 4.3V T_J = 25°C 100µA ≤I_{OUT} ≤500mA, 4.3V ≤V_{IN} ≤7.5V	3.250 **3.201**	3.300	3.350 **3.399**	V
		LP8345-5.0 I_{OUT} = 10mA, V_{IN} = 6V, T_J = 25°C 100µA ≤I_{OUT} ≤500mA, 6V ≤V_{IN} ≤9V	4.925 **4.850**	5.000	5.075 **5.150**	V

(1) All limits are specified by testing or statistical analysis.
(2) Typical Values represent the most likely parametric norm.

LP8345C ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified all limits specified for $V_{IN} = V_O + 1V$, $C_{IN} = C_{OUT} = 10\mu F$, $T_J = 25°C$. **Boldface** limits apply over the full operating temperature range of T_J = 0°C to 125°C

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
ΔV_O	Load Regulation	LP8345-ADJ, ADJ=OUT I_{OUT} = 1mA to 500mA, V_{IN} = 2.7V		6	**20**	mV
		LP8345-1.8 I_{OUT} = 1mA to 500mA, V_{IN} = 2.8V		7	**20**	
		LP8345-2.5 I_{OUT} = 1mA to 500mA, V_{IN} = 3.5V		9	**30**	
		LP8345-3.3 I_{OUT} = 1mA to 500mA, V_{IN} = 4.3V		12	**35**	
		LP8345-5.0 I_{OUT} = 1mA to 500mA, V_{IN} = 6V		14	**40**	
ΔV_O	Line Regulation	V_{OUT} + 0.5V ≤V_{IN} ≤10V, I_{OUT} = 25mA (3)		4	**15**	mV
$V_{IN} - V_O$	Dropout Voltage (3) (4)	LP8345-2.5 I_{OUT} = 500mA		335	**650**	mV
		LP8345-3.3 LP8345-ADJ, V_{OUT} = 3.3V, I_{OUT} = 500mA		270	**500**	
		LP8345-5.0 I_{OUT} = 500mA		210	**400**	
I_Q	Quiescent Current	V_{IN} ≤10V		19	**50**	µA
	Minimum Load Current	$V_{IN} - V_{OUT}$ ≤4V			**100**	µA
I_{LIMIT}	Foldback Current Limit	$V_{IN} - V_{OUT}$ >5V		450		mA
		$V_{IN} - V_{OUT}$ <4V		1200		
	Ripple Rejection Ratio	V_{IN} (dc) = V_{OUT} + 2V V_{IN} (ac) = $1V_{P-P}$ @ 120Hz	**48**	55		dB
T_{SD}	Thermal Shutdown Temp. Thermal Shutdown Hyst.			160 10		°C
	ADJ Input Leakage Current	V_{ADJ} = 1.5V or 0V		±0.01	±100	nA
	V_{OUT} Leakage Current	LP8345-ADJ ADJ = OUT, V_{OUT} = 2V, V_{IN} = 10V			10	µA
		LP8345-1.8, V_{OUT} = 2.5V, V_{IN} = 10V			10	
		LP8345-2.5, V_{OUT} = 3.5V, V_{IN} = 10V			10	
		LP8345-3.3, V_{OUT} = 4V, V_{IN} = 10V			10	
		LP8345-5.0, V_{OUT} = 6V, V_{IN} = 10V			10	
e_n	Output Noise	10Hz to 10kHz, R_L = 1kΩ, C_{OUT} = 10µF		250		µVrms

(3) Condition does not apply to input voltages below 2.7V since this is the minimum input operating voltage.
(4) Dropout voltage is measured by reducing V_{IN} until V_O drops 100mV from its normal value.

LP8345I ELECTRICAL CHARACTERISTICS

Unless otherwise specified all limits specified for $V_{IN} = V_O + 1V$, $C_{IN} = C_{OUT} = 10\mu F$, $T_J = 25°C$. **Boldface** limits apply over the full operating temperature range of T_J = −40°C to 125°C

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{IN}	Input Voltage	LP8345-ADJ,1.8, 2.5 LP8345-3.3, 5.0	**2.7**		**10** **10**	V

(1) All limits are specified by testing or statistical analysis.
(2) Typical Values represent the most likely parametric norm.

LP8345I ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified all limits specified for $V_{IN} = V_O + 1V$, $C_{IN} = C_{OUT} = 10µF$, $T_J = 25°C$. **Boldface** limits apply over the full operating temperature range of $T_J = -40°C$ to 125°C

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{OUT}	Output Voltage	LP8345-ADJ, ADJ = OUT I_{OUT} = 10mA, V_{IN} = 2.7V, T_J = 25°C 100µA ≤I_{OUT}≤ 500mA, 2.7V ≤V_{IN}≤V_{OUT} +4V	1.231 **1.213**	1.250	1.269 **1.288**	V
		LP8345-1.8 I_{OUT} = 10mA, V_{IN} = 2.8V, T_J = 25°C 100µA ≤I_{OUT} ≤500mA, 2.8V ≤V_{IN}≤6V	1.773 **1.746**	1.800	1.827 **1.854**	V
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		LP8345-3.3 I_{OUT} = 10mA, V_{IN} = 4.3V T_J = 25°C 100µA ≤I_{OUT} ≤500mA, 4.3V ≤V_{IN} ≤7.5V	3.250 **3.201**	3.300	3.350 **3.399**	V
		LP8345-5.0 I_{OUT} = 10mA, V_{IN} = 6V, T_J = 25°C 100µA ≤I_{OUT} ≤500mA, 6V ≤V_{IN} ≤9V	4.925 **4.850**	5.000	5.075 **5.150**	V
ΔV_O	Load Regulation	LP8345-ADJ, ADJ=OUT I_{OUT} = 1mA to 500mA, V_{IN} = 2.7V		6	**20**	mV
		LP8345-1.8 I_{OUT} = 1mA to 500mA, V_{IN} = 2.8V		7	**20**	
		LP8345-2.5 I_{OUT} = 1mA to 500mA, V_{IN} = 3.5V		9	**30**	
		LP8345-3.3 I_{OUT} = 1mA to 500mA, V_{IN} = 4.3V		12	**35**	
		LP8345-5.0 I_{OUT} = 1mA to 500mA, V_{IN} = 6V		14	**40**	
ΔV_O	Line Regulation	V_{OUT} + 0.5V ≤V_{IN} ≤10V, I_{OUT} = 25mA (3)		4	**15**	mV
$V_{IN} - V_O$	Dropout Voltage (3) (4)	LP8345-2.5 I_{OUT} = 500mA		335	**650**	mV
		LP8345-3.3 LP8345-ADJ, V_{OUT} = 3.3V, I_{OUT} = 500mA		270	**500**	
		LP8345-5.0 I_{OUT} = 500mA		210	**400**	
I_Q	Quiescent Current	V_{IN} ≤10V		19	**50**	µA
	Minimum Load Current	$V_{IN} - V_{OUT}$ ≤4V			**100**	µA
I_{LIMIT}	Foldback Current Limit	$V_{IN} - V_{OUT}$ >5V		450		mA
		$V_{IN} - V_{OUT}$ <4V		1200		
	Ripple Rejection Ratio	V_{IN} (dc) = V_{OUT} + 2V V_{IN} (ac) = 1V_{P-P} @ 120Hz	**48**	55		dB
T_{SD}	Thermal Shutdown Temp. Thermal Shutdown Hyst.			160 10		°C
	ADJ Input Leakage Current	V_{ADJ} = 1.5V or 0V		±0.01	±100	nA
	V_{OUT} Leakage Current	LP8345-ADJ ADJ = OUT, V_{OUT} = 2V, V_{IN} = 10V			10	µA
		LP8345-1.8, V_{OUT} = 2.5V, V_{IN} = 10V			10	
		LP8345-2.5, V_{OUT} = 3.5V, V_{IN} = 10V			10	
		LP8345-3.3, V_{OUT} = 4V, V_{IN} = 10V			10	
		LP8345-5.0, V_{OUT} = 6V, V_{IN} = 10V			10	
e_n	Output Noise	10Hz to 10kHz, R_L = 1kΩ, C_{OUT} = 10µF		250		µVrms

(3) Condition does not apply to input voltages below 2.7V since this is the minimum input operating voltage.
(4) Dropout voltage is measured by reducing V_{IN} until V_O drops 100mV from its normal value.

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified, $V_{IN} = V_O + 1.5V$, $C_{IN} = C_{OUT} = 10\mu F$ X7R ceramic, $T_J = 25°C$

Output Voltage Change vs. Temperature

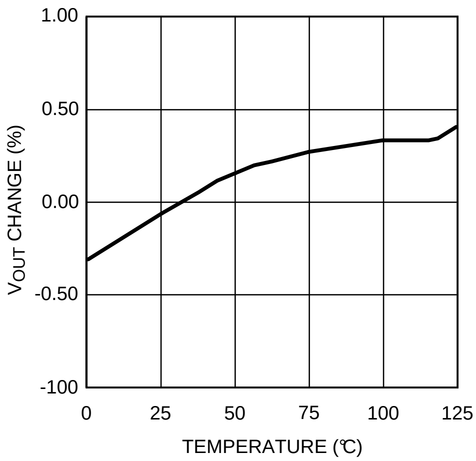

Figure 4.

Dropout Voltage vs. Load Current

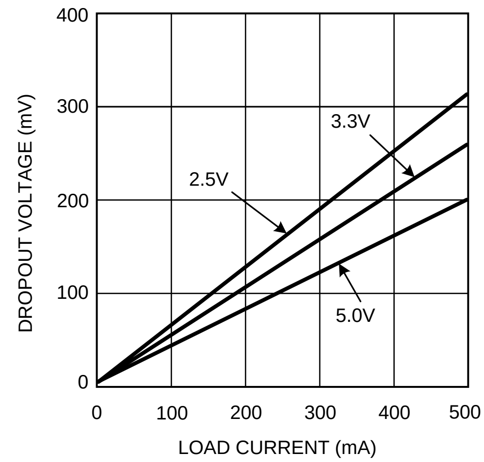

Figure 5.

Ground Current vs. Temperature (I_{LOAD} = 500mA)

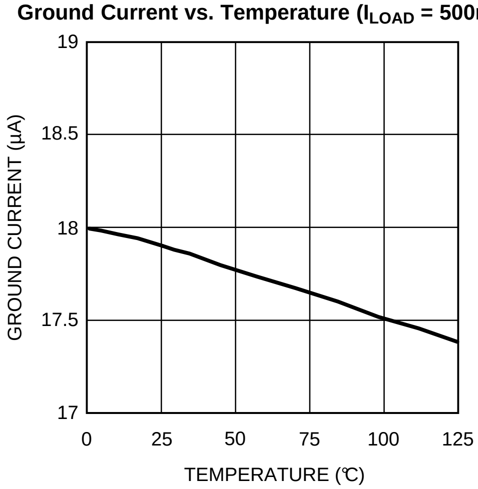

Figure 6.

Ground Current vs. Load Current

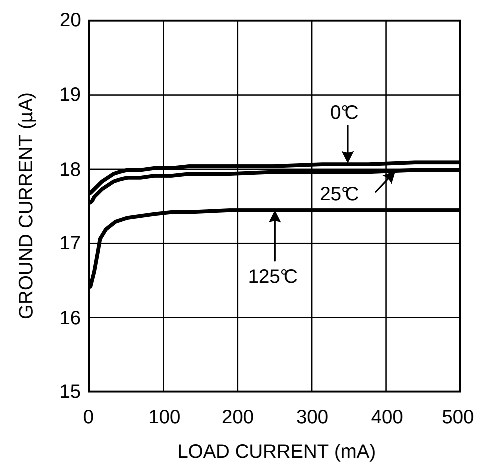

Figure 7.

Ground Current vs. Input Voltage

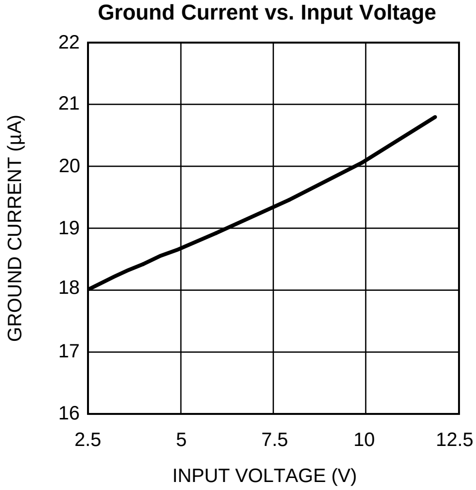

Figure 8.

Ripple Rejection Ratio vs. Frequency

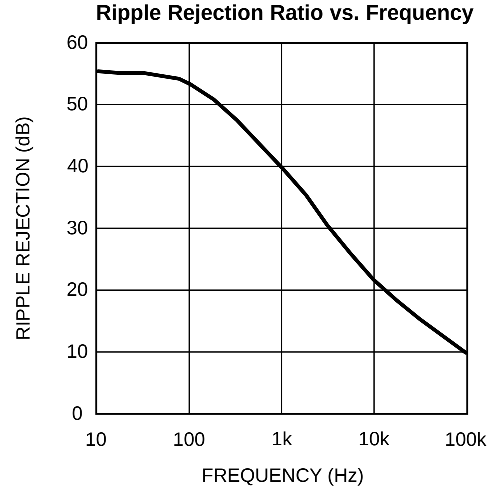

Figure 9.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, $V_{IN} = V_O + 1.5V$, $C_{IN} = C_{OUT} = 10\mu F$ X7R ceramic, $T_J = 25°C$

Load Transient Response

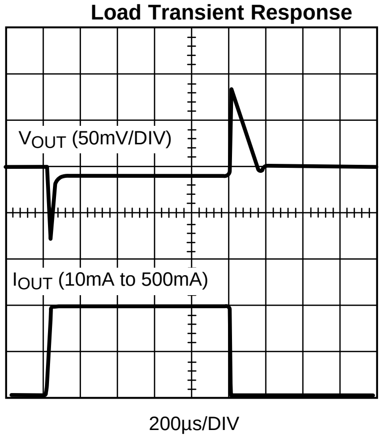

Figure 10.

Line Transient Response

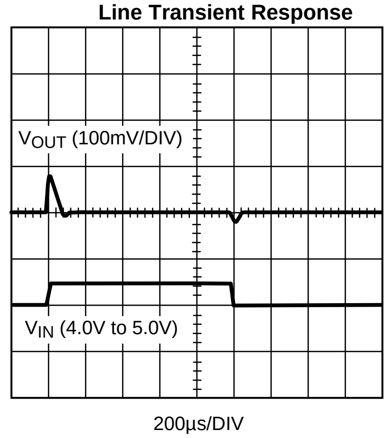

Figure 11.

Start-up Response

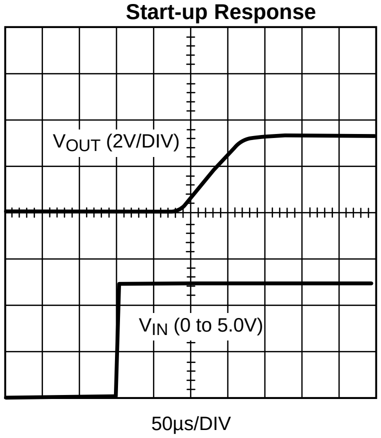

Figure 12.

Minimum Input Voltage Rise Time

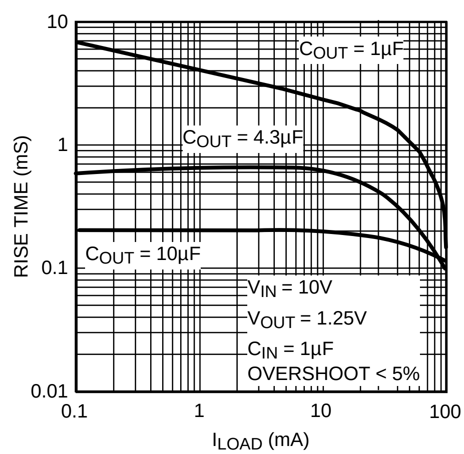

Figure 13.

Minimum Input Voltage Rise Time

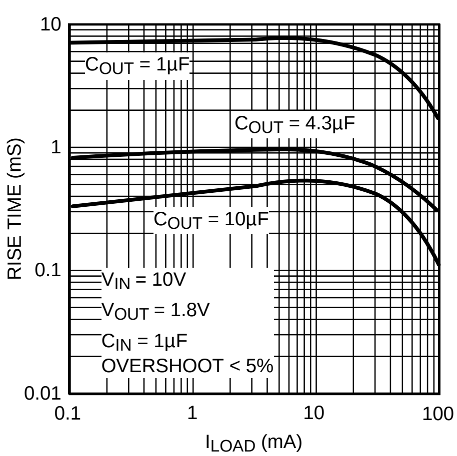

Figure 14.

Minimum Input Voltage Rise Time

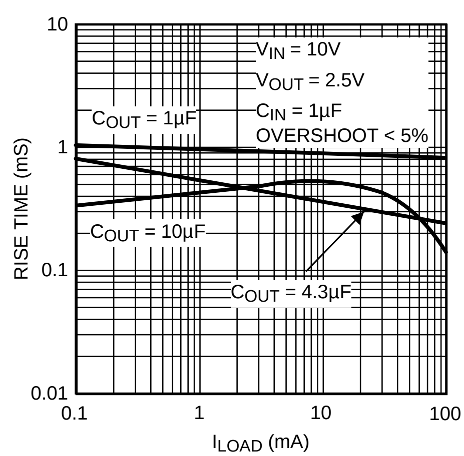

Figure 15.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, $V_{IN} = V_O + 1.5V$, $C_{IN} = C_{OUT} = 10\mu F$ X7R ceramic, $T_J = 25°C$

Minimum Input Voltage Rise Time

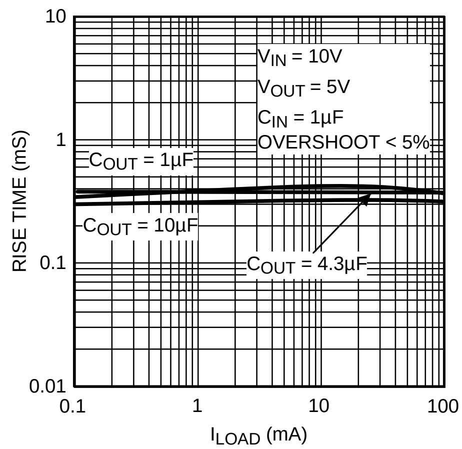

Figure 16.

Minimum Input Voltage Rise Time

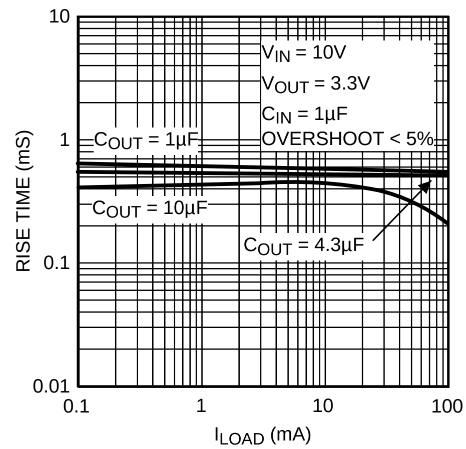

Figure 17.

APPLICATIONS SECTION

GENERAL INFORMATION

The LP8345 is a low-dropout, low quiescent current linear regulator. As shown in Figure 18 it consists of a 1.25V reference, error amplifier, MOSFET driver, PMOS pass transistor and for the fixed output versions, an internal feedback network (R_1/R_2). In addition, the device is protected from overload by a thermal shutdown circuit and a foldback current limit circuit.

The 1.25V reference is connected to the inverting input of the error amplifier. Regulation of the output voltage is achieved by means of negative feedback to the non-inverting input of the error amplifier. Feedback resistors R_1 and R_2 are either internal or external to the device, depending on whether it is a fixed voltage version or the adjustable version. The negative feedback and high open loop gain of the error amplifier cause the two inputs of the error amp to be virtually equal in voltage. If the output voltage changes due to load changes, the error amplifier and MOSFET driver provide the appropriate drive to the pass transistor to maintain the error amplifier's inputs as virtually equal.

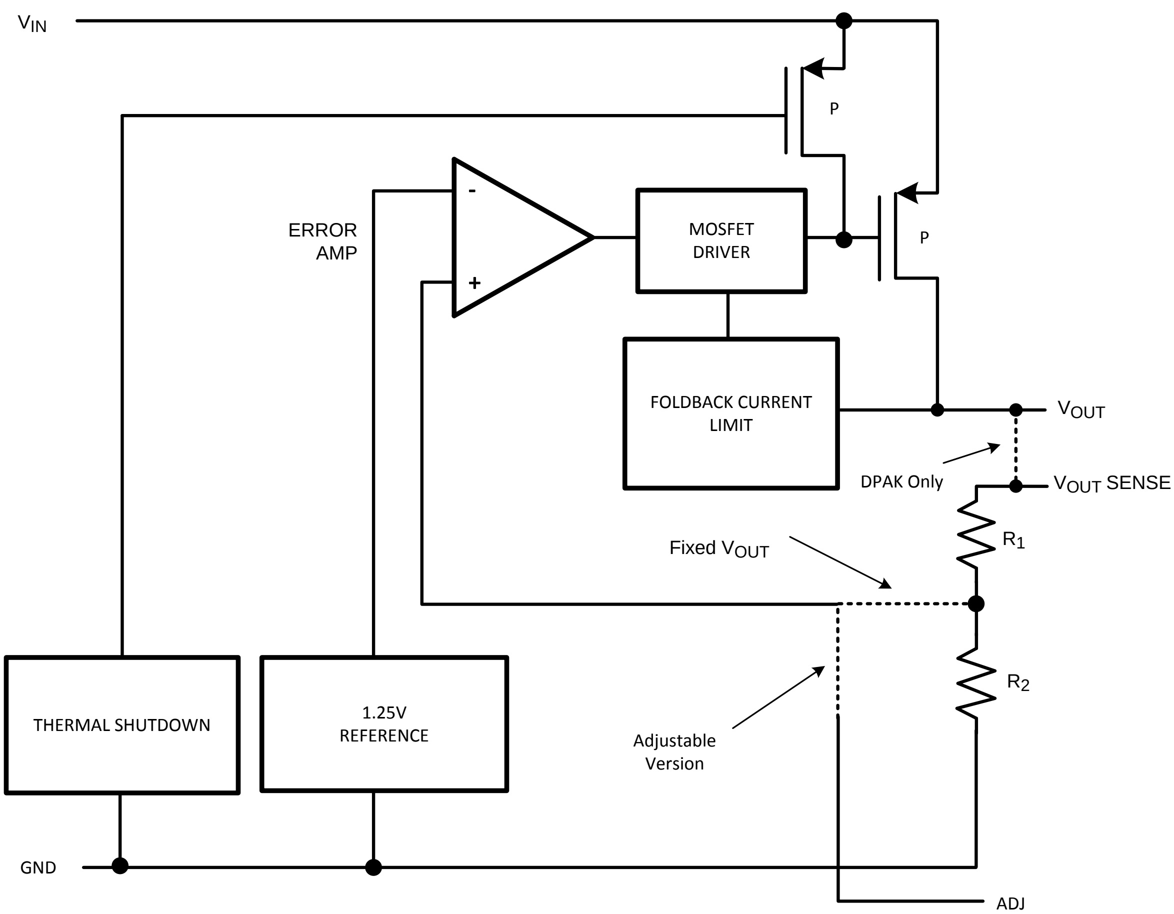

Figure 18. LP8345 Functional Block Diagram

EXTERNAL CAPACITOR

An Input capacitor of 1µF or greater is required between the LP8345 V_{IN} pin and ground. While 1µF will provide adequate bypassing of the V_{IN} supply larger values of input capacitor (i.e. 10µF) can provide improved bypassing of power supply noise.

Stable operation can be achieved with an output capacitor of 1µF or greater, either ceramic X7R dielectric or aluminum/tantalum electrolytic. While the minimum capacitor value is 1µF, the typical output capacitor values selected range from 1µF to 10µF. The larger values provide improved load-transient response, power supply rejection and stability.

OUTPUT VOLTAGE SETTING (ADJ VERSION ONLY)

The output voltage is set according to the amount of negative feedback (Note that the pass transistor inverts the feedback signal). This feedback is determined by R_1 and R_2 with the resulting output voltage represented by the following equation:

$$V_O = V_{REF}\left[\frac{R_1}{R_2} + 1\right] \quad (1)$$

Use the following equation to determine the values of R_1 and R_2 for a desired V_{OUT} (R_2 = 100kΩ is recommended).

$$R_1 = R_2\left[\frac{V_O}{1.25\,V} - 1\right] \quad (2)$$

MINIMUM LOAD CURRENT

A minimum load of 100µA is required for regulation and stability over the entire operating temperature range. If actual load current fall below 100µA it is recommended that a resistor of value $R_L = V_O$/100µA be placed between V_O and ground.

START UP CONSIDERATIONS

Under certain operating conditions, overshoot of V_{OUT} at start-up can occur. The observed overshoot is a function of rise time of V_{IN} waveform, C_{OUT}, start-up load current, and V_{IN}−V_{OUT} differential. The relationship between these conditions is shown in the Typical Performance Characteristics curves (Minimum Input Voltage Rise Time). V_{IN} rise times above the curve result in <5% overshoot.

Customers are encouraged to check the suitability of LP8345 in their specific application.

REVISION HISTORY

Changes from Revision E (April 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	10