



CYPRESS

PRELIMINARY

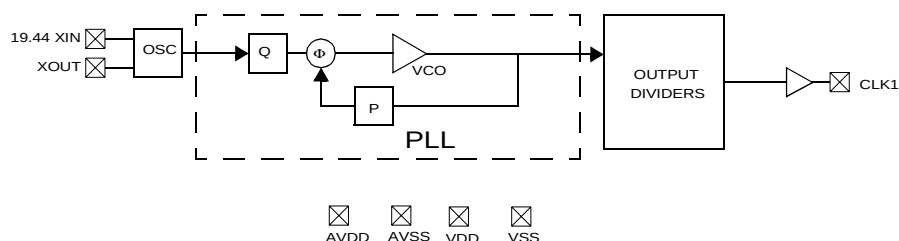
CY26200

T1/E1 Clock Generator

Features	Benefits
• Integrated phase-locked loop (PLL)	High-performance PLL tailored for T1/E1 clock generation
• Low-jitter, high-accuracy outputs	Meets critical timing requirements in complex system designs
• 3.3V operation	Enables application compatibility

Part Number	Outputs	Input Frequency Range	Output Frequencies
CY26200	1	19.44 MHz	1.544 MHz/2.048 MHz (selectable)

Logic Block Diagram



Pin Configuration

**CY26200
8-pin SOIC**

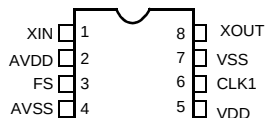


Table 1: CY26200 Frequency Select Option

Frequency Select	CLK1	Unit
0	1.544	MHz
1	2.048	MHz

Pin Summary

Pin Name	Pin Number	Pin Description
XIN	1	19.44-MHz Reference Input
AVDD	2	Analog Voltage Supply
FS	3	Frequency Select – see <i>Table 1</i>
AVSS	4	Analog Ground
VDD	5	Voltage Supply
CLK1	6	1.544-MHz/2.048-MHz Clock Output
VSS	7	Ground
XOUT ^[1]	8	Reference Output

Absolute Maximum Conditions

Parameter	Description	Min.	Max.	Unit
V _{DD}	Supply Voltage	–0.5	7.0	V
T _S	Storage Temperature ^[2]	–65	125	°C
T _J	Junction Temperature		125	°C
	Digital Inputs	V _{SS} – 0.3	V _{DD} + 0.3	V
	Digital Outputs Referred to V _{DD}	V _{SS} – 0.3	V _{DD} + 0.3	V
	Electrostatic Discharge	2000		V

Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
V _{DD} /AV _{DD}	Operating Voltage	3.135	3.3	3.465	V
T _A	Ambient Temperature (Commercial)	0		70	°C
T _A	Ambient Temperature (Industrial)	–40		+85	°C
C _{LOAD}	Max. Load Capacitance			15	pF
f _{REF}	Reference Frequency		19.44		MHz

DC Electrical Characteristics (Commercial)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
I _{OH}	Output High Current	V _{OH} = V _{DD} – 0.5, V _{DD} = 3.3V	12	24		mA
I _{OL}	Output Low Current	V _{OL} = 0.5, V _{DD} = 3.3V	12	24		mA
C _{IN}	Input Capacitance				7	pF
I _{Iz}	Input Leakage Current			5		μA
I _{DD}	Supply Current	Sum of Core and Output Current			20	mA

DC Electrical Characteristics (Industrial)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
I _{OH}	Output High Current	V _{OH} = V _{DD} – 0.5, V _{DD} = 3.3V	11	24		mA
I _{OL}	Output Low Current	V _{OL} = 0.5, V _{DD} = 3.3V	11	24		mA
C _{IN}	Input Capacitance				7	pF
I _{Iz}	Input Leakage Current			5		μA
I _{DD}	Supply Current	Sum of Core and Output Current			25	mA

AC Electrical Characteristics (V_{DD} = 3.3V, Commercial)

Parameter ^[3]	Description	Conditions	Min.	Typ.	Max.	Unit
DC	Output Duty Cycle	Duty Cycle is defined in <i>Figure 1</i> , 50% of V _{DD}	45	50	55	%
t ₃	Rising Edge Slew Rate	Output Clock Rise Time, 20% - 80% of V _{DD}	0.8	1.4		V/ns

Notes:

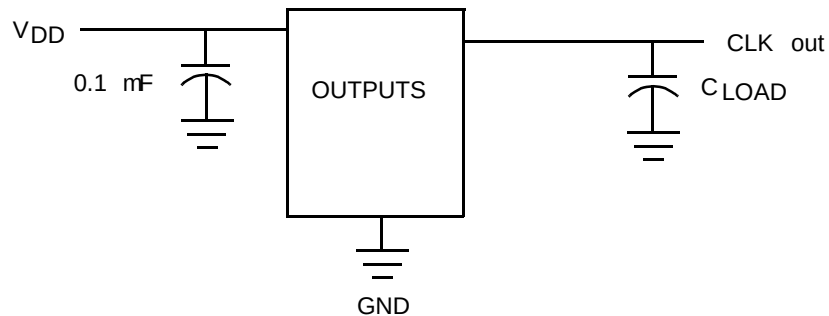
1. Float XOUT if XIN is externally driven
2. Rated for 10 years
3. Not 100% tested

AC Electrical Characteristics ($V_{DD} = 3.3V$, Commercial) (continued)

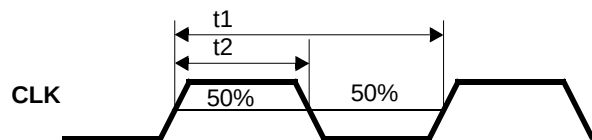
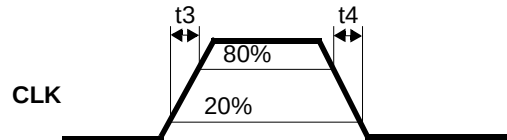
Parameter ^[3]	Description	Conditions	Min.	Typ.	Max.	Unit
t_4	Falling Edge Slew Rate	Output Clock Fall Time, 80% - 20% of V_{DD}	0.8	1.4		V/ns
t_9	Clock Jitter	Peak to Peak period jitter		200		ps
t_{10}	PLL Lock Time				3	ms

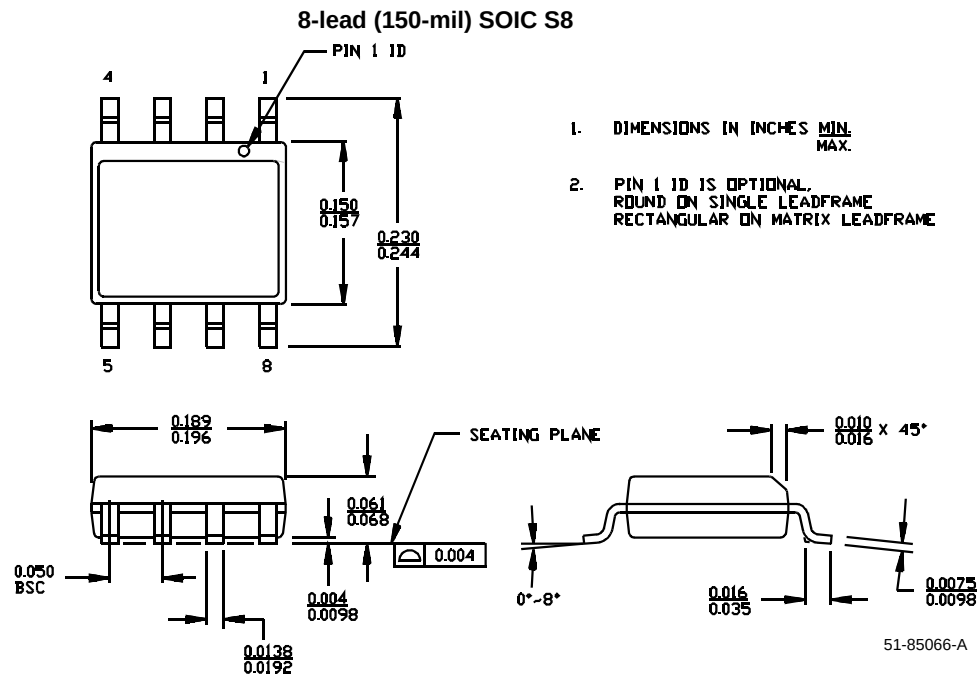
AC Electrical Characteristics ($V_{DD} = 3.3V$, Industrial)

Parameter ^[3]	Name	Description	Min.	Typ.	Max.	Unit
DC	Output Duty Cycle	Duty Cycle is defined in <i>Figure 1</i> , 50% of V_{DD}	45	50	55	%
t_3	Rising Edge Slew Rate	Output Clock Rise Time, 20% – 80% of V_{DD}	0.8	1.4		V/ns
t_4	Falling Edge Slew Rate	Output Clock Fall Time, 80% – 20% of V_{DD}	0.8	1.4		V/ns
t_9	Clock Jitter	Peak to Peak period jitter		200		ps
t_{10}	PLL Lock Time				3	ms

Test Circuit

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range	Operating Voltage
CY26200SC	S8	8-lead SOIC	Commercial	3.3V
CY26200SI	S8	8-lead SOIC	Industrial	3.3V


Figure 1. Duty Cycle Definition; $DC = t_2/t_1$

Figure 2. Rise and Fall Time Definitions

Package Diagram


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REV.	ECN No.	Issue Date	Orig. of Change	Description of Change
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