

E Series Power MOSFET

PRODUCT SUMMARY	
V_{DS} (V) at T_J max.	700
$R_{DS(on)}$ max. at 25 °C (Ω)	$V_{GS} = 10$ V 0.38
Q_g max. (nC)	70
Q_{gs} (nC)	9
Q_{gd} (nC)	16
Configuration	Single

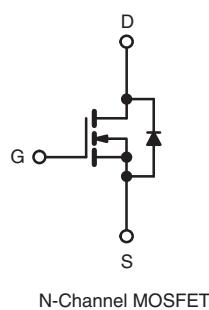
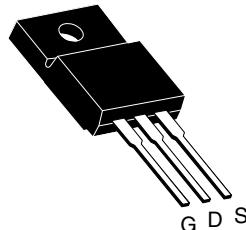
FEATURES

- Low Figure-of-Merit (FOM) $R_{on} \times Q_g$
- Low Input Capacitance (C_{iss})
- Reduced Switching and Conduction Losses
- Ultra Low Gate Charge (Q_g)
- Avalanche Energy Rated (UIS)
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

TO-220 FULLPAK



APPLICATIONS

- Server and Telecom Power Supplies
- Switch Mode Power Supplies (SMPS)
- Power Factor Correction Power Supplies (PFC)
- Lighting
 - High-Intensity Discharge (HID)
 - Fluorescent Ballast Lighting
- Industrial
 - Welding
 - Induction Heating
 - Motor Drives
 - Battery Chargers
 - Renewable Energy
 - Solar (PV Inverters)

ORDERING INFORMATION

Package	TO-220 FULLPAK
Lead (Pb)-free and Halogen-free	SiHF12N65E-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	650	V
Gate-Source Voltage		± 20	
Gate-Source Voltage AC ($f > 1$ Hz)		30	
Continuous Drain Current ($T_J = 150$ °C) ^e	I_D	12	A
		8	
		28	
Pulsed Drain Current ^a	I_{DM}	28	
Linear Derating Factor		0.26	W/°C
Single Pulse Avalanche Energy ^b	E_{AS}	226	mJ
Maximum Power Dissipation	P_D	33	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	°C
Drain-Source Voltage Slope	dV/dt	37	V/ns
Reverse Diode dV/dt ^d		28	
Soldering Recommendations (Peak Temperature) ^c	for 10 s	300	°C

Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω, $I_{AS} = 4$ A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$, $dI/dt = 100$ A/μs, starting $T_J = 25$ °C.
- Limited by maximum junction temperature.

THERMAL RESISTANCE RATINGS

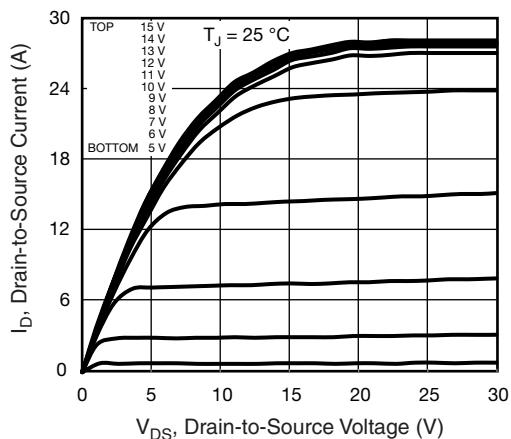
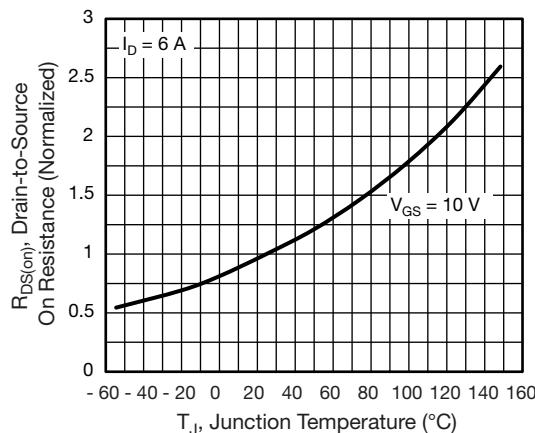
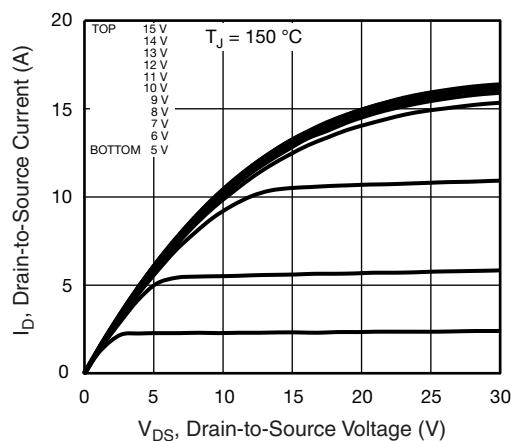
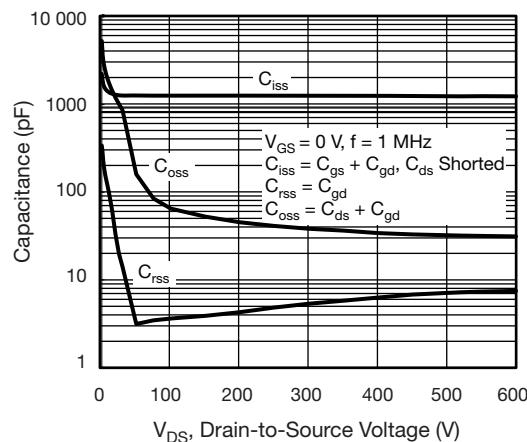
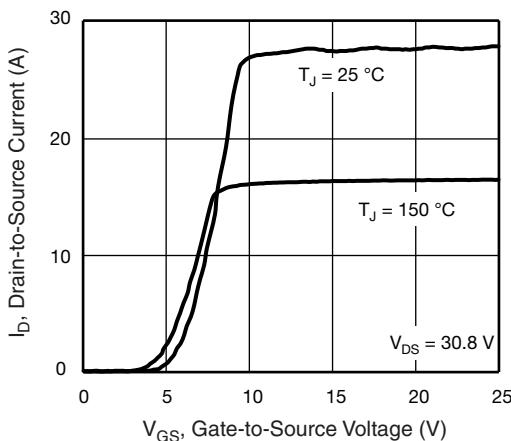
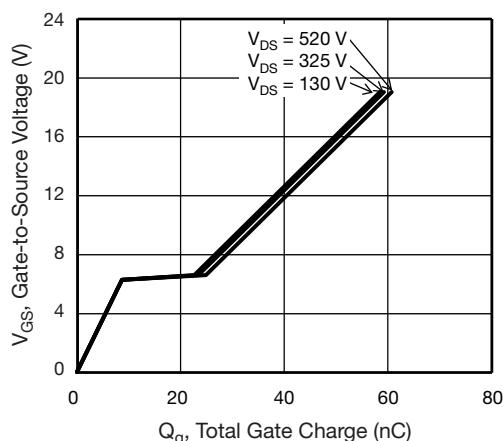
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	65	$^{\circ}\text{C}/\text{W}$
Maximum Junction-to-Case (Drain)	R_{thJC}	-	3.8	

SPECIFICATIONS ($T_J = 25^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$		650	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25°C , $I_D = 1 \text{ mA}$		-	0.78	-	$^{\circ}\text{C}/\text{V}$
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$		2	-	4	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 650 \text{ V}$, $V_{GS} = 0 \text{ V}$		-	-	1	μA
		$V_{DS} = 520 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 125^{\circ}\text{C}$		-	-	10	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$	$I_D = 6 \text{ A}$	-	0.33	0.38	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 30 \text{ V}$, $I_D = 6 \text{ A}$		-	3.5	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0 \text{ V}$, $V_{DS} = 100 \text{ V}$, $f = 1 \text{ MHz}$		-	1224	-	pF
Output Capacitance	C_{oss}			-	65	-	
Reverse Transfer Capacitance	C_{rss}			-	4	-	
Effective Output Capacitance, Energy Related ^a	$C_{o(er)}$	$V_{DS} = 0 \text{ V}$ to 520 V , $V_{GS} = 0 \text{ V}$		-	50	-	pF
Effective Output Capacitance, Time Related ^b	$C_{o(tr)}$			-	160	-	
Total Gate Charge	Q_g	$V_{GS} = 10 \text{ V}$	$I_D = 6 \text{ A}$, $V_{DS} = 520 \text{ V}$	-	35	70	nC
Gate-Source Charge	Q_{gs}			-	9	-	
Gate-Drain Charge	Q_{gd}			-	16	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 520 \text{ V}$, $I_D = 6 \text{ A}$, $V_{GS} = 10 \text{ V}$, $R_g = 9.1 \Omega$		-	16	32	ns
Rise Time	t_r		-	19	38		
Turn-Off Delay Time	$t_{d(off)}$		-	35	70		
Fall Time	t_f		-	18	36		
Gate Input Resistance	R_g	$f = 1 \text{ MHz}$, open drain		-	0.81	-	Ω
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	12	A
Pulsed Diode Forward Current	I_{SM}			-	-	28	
Diode Forward Voltage	V_{SD}	$T_J = 25^{\circ}\text{C}$, $I_S = 6 \text{ A}$, $V_{GS} = 0 \text{ V}$		-	1.0	1.2	V
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}\text{C}$, $I_F = I_S = 6 \text{ A}$, $dI/dt = 100 \text{ A}/\mu\text{s}$, $V_R = 25 \text{ V}$		-	309	618	ns
Reverse Recovery Charge	Q_{rr}			-	3.8	7.6	μC
Reverse Recovery Current	I_{RRM}			-	21	-	A

Notes

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .
b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics

Fig. 4 - Normalized On-Resistance vs. Temperature

Fig. 2 - Typical Output Characteristics

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 3 - Typical Transfer Characteristics

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

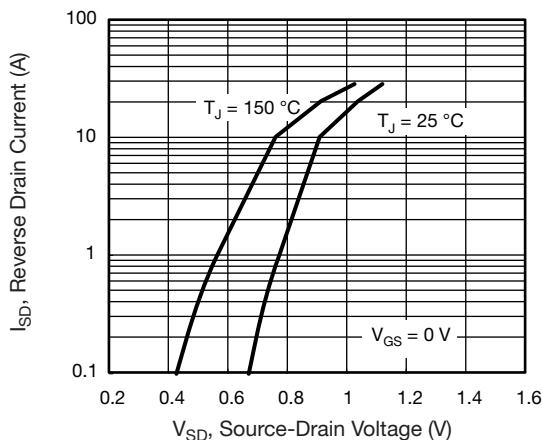


Fig. 7 - Typical Source-Drain Diode Forward Voltage

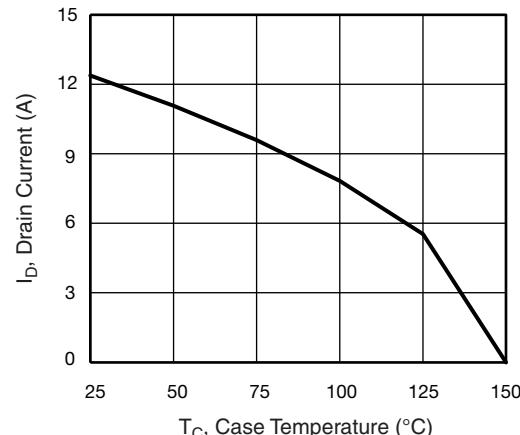


Fig. 9 - Maximum Drain Current vs. Case Temperature

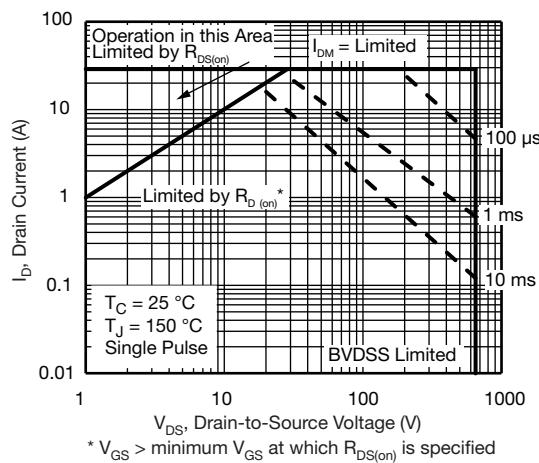


Fig. 8 - Maximum Safe Operating Area

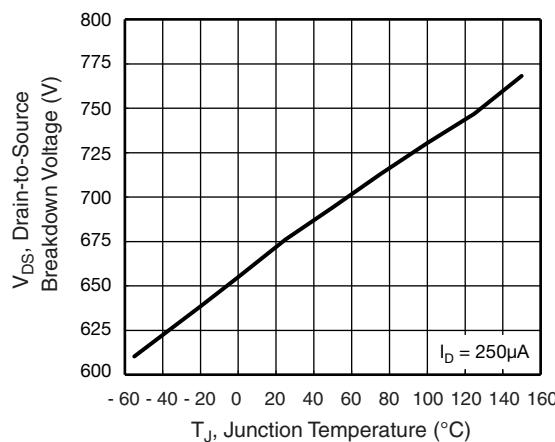


Fig. 10 - Temperature vs. Drain-to-Source Voltage

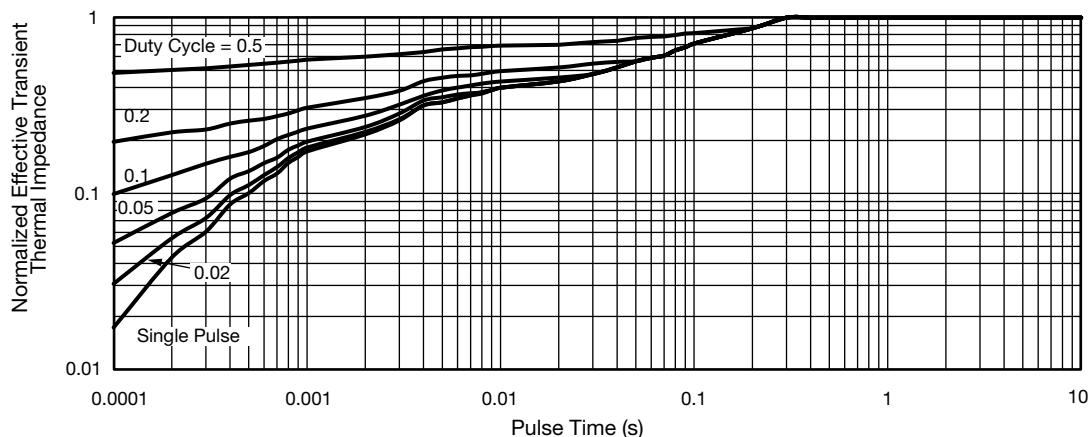


Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case

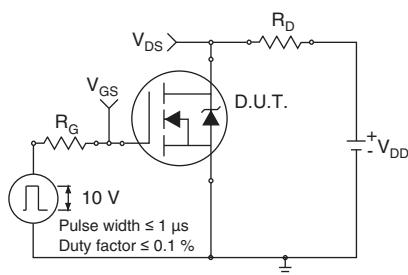


Fig. 12 - Switching Time Test Circuit

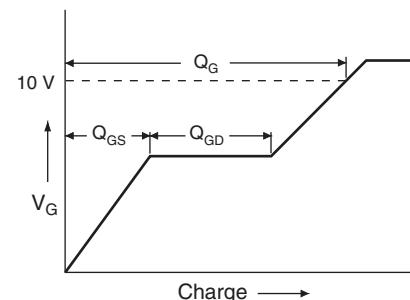


Fig. 16 - Basic Gate Charge Waveform

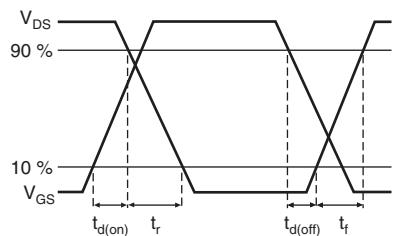


Fig. 13 - Switching Time Waveforms

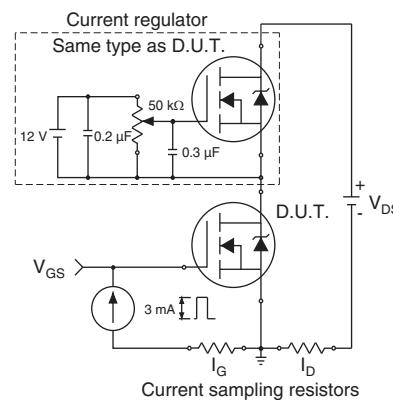


Fig. 17 - Gate Charge Test Circuit

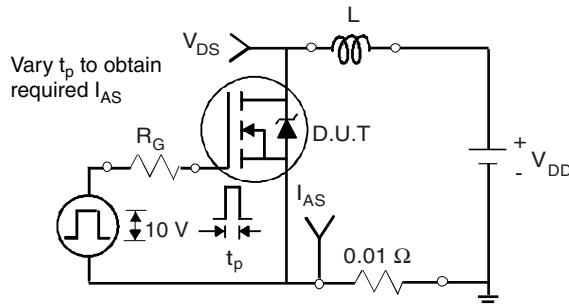


Fig. 14 - Unclamped Inductive Test Circuit

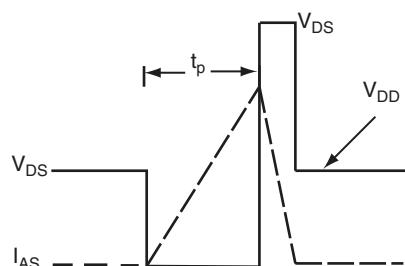


Fig. 15 - Unclamped Inductive Waveforms

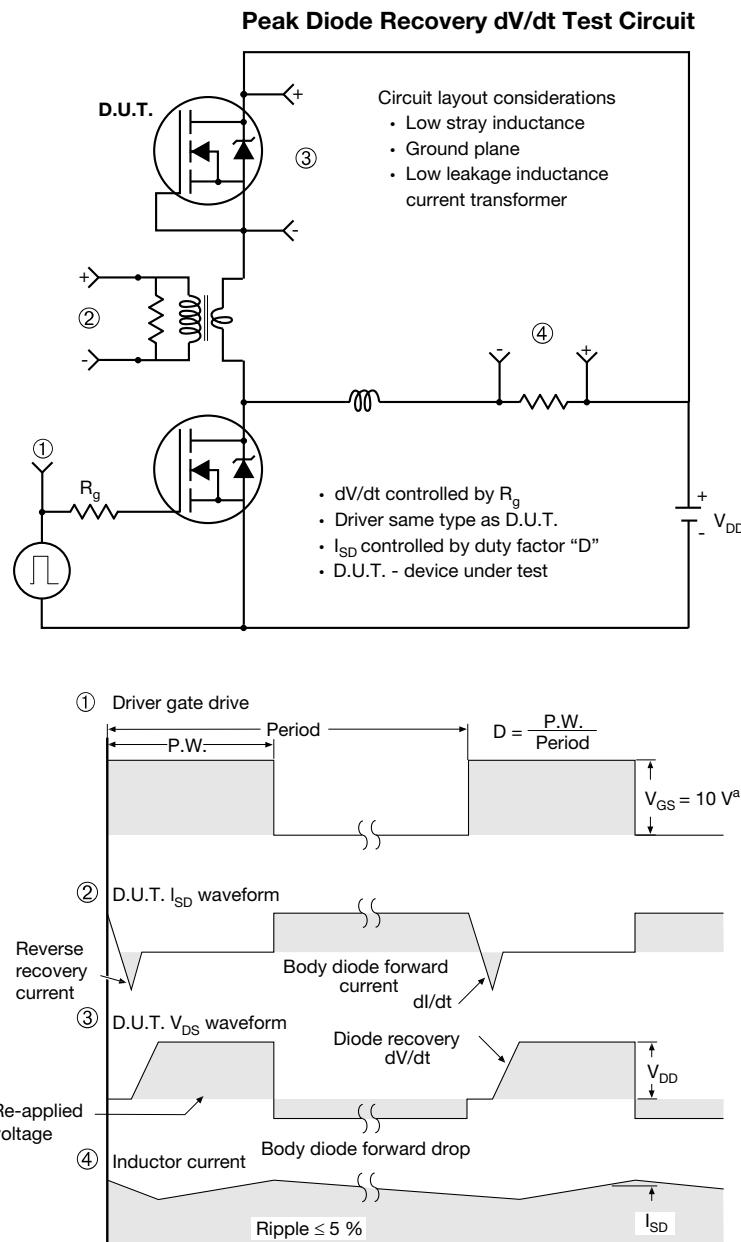


Fig. 18 - For N-Channel

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