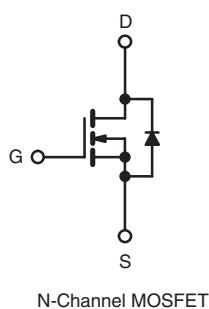
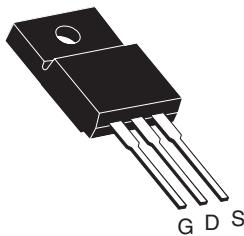


## Power MOSFET

PRODUCT SUMMARY	
$V_{DS}$ (V)	800
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10$ V 3.0
$Q_g$ (Max.) (nC)	78
$Q_{gs}$ (nC)	9.6
$Q_{gd}$ (nC)	45
Configuration	Single

**TO-220 FULLPAK**


### ORDERING INFORMATION

Package	TO-220 FULLPAK
Lead (Pb)-free	IRFIBE30GPbF SiHFIGE30G-E3
SnPb	IRFIBE30G SiHFIGE30G

### ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	800	
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$V_{GS}$ at 10 V	2.1	A
		1.4	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	8.4	
Linear Derating Factor		0.28	W/°C
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	240	mJ
Avalanche Current <sup>a</sup>	$I_{AR}$	2.1	A
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	3.5	mJ
Maximum Power Dissipation	$P_D$	35	W
Peak Diode Recovery dV/dt <sup>c</sup>	dV/dt	2.0	V/ns
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s	300 <sup>d</sup>	
Mounting Torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

#### Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b.  $V_{DD} = 50$  V, starting  $T_J = 25$  °C,  $L = 102$  mH,  $R_G = 25$  Ω,  $I_{AS} = 2.1$  A (see fig. 12).

c.  $I_{SD} \leq 4.1$  A,  $dI/dt \leq 100$  A/μs,  $V_{DD} \leq 600$  V,  $T_J \leq 150$  °C.

d. 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply



### FEATURES

- Isolated Package
- High Voltage Isolation = 2.5 kV<sub>RMS</sub> ( $t = 60$  s;  $f = 60$  Hz)
- Sink to Lead Creepage Distance = 4.8 mm
- Dynamic dV/dt Rating
- Low Thermal Resistance
- Lead (Pb)-free Available

### DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 FULLPAK eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. The isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The FULLPAK is mounted to a heatsink using a single clip or by a single screw fixing.

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	65	$^{\circ}\text{C}/\text{W}$
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	3.6	

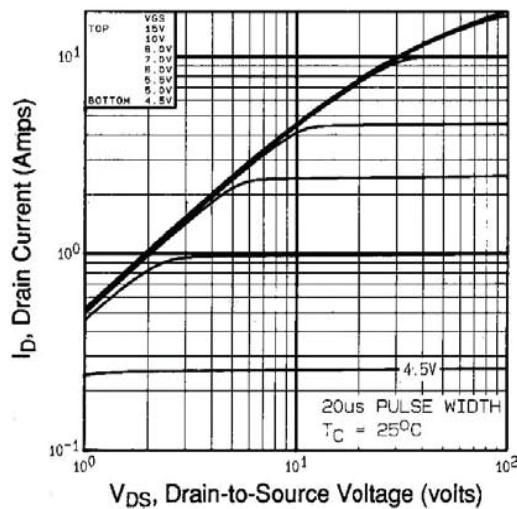
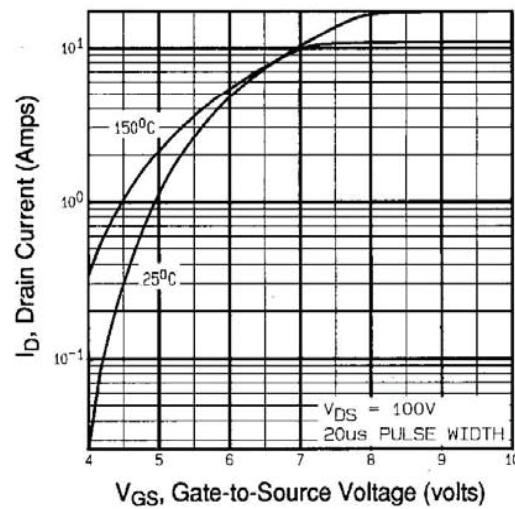
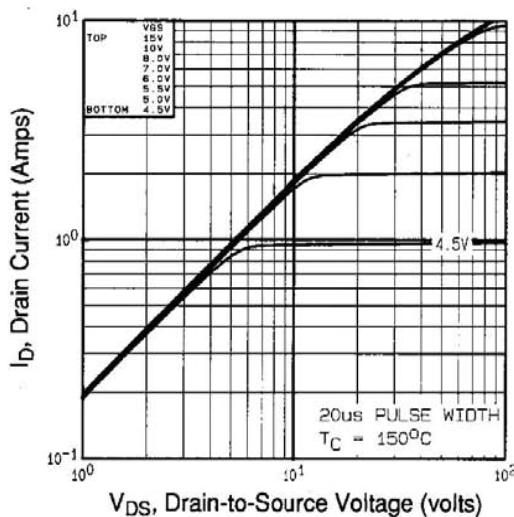
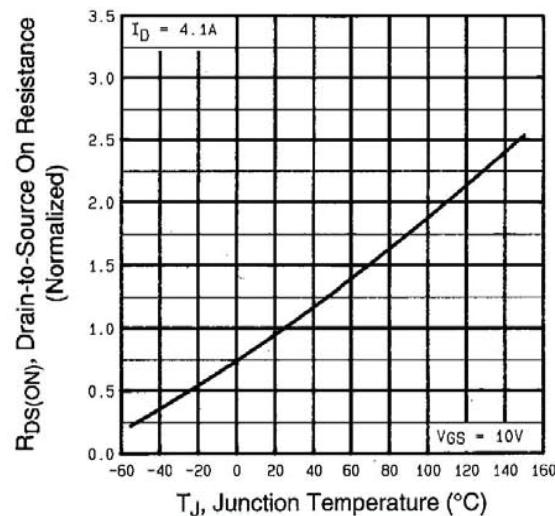
 **SPECIFICATIONS  $T_J = 25^{\circ}\text{C}$ , unless otherwise noted**

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}$ , $I_D = 250 \mu\text{A}$		800	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25^{\circ}\text{C}$ , $I_D = 1 \text{ mA}$		-	0.90	-	$^{\circ}\text{C}/\text{C}$
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250 \mu\text{A}$		2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20 \text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 800 \text{ V}$ , $V_{GS} = 0 \text{ V}$		-	-	100	$\mu\text{A}$
		$V_{DS} = 640 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $T_J = 125^{\circ}\text{C}$		-	-	500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$	$I_D = 1.3 \text{ A}^b$	-	-	3.0	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 50 \text{ V}$ , $I_D = 1.3 \text{ A}^b$		1.7	-	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0 \text{ V}$ , $V_{DS} = 25 \text{ V}$ , $f = 1.0 \text{ MHz}$ , see fig. 5		-	1300	-	pF
Output Capacitance	$C_{oss}$			-	310	-	
Reverse Transfer Capacitance	$C_{rss}$			-	190	-	
Drain to Sink Capacitance	C	$f = 1.0 \text{ MHz}$		-	12	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10 \text{ V}$	$I_D = 4.1 \text{ A}$ , $V_{DS} = 400 \text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	78	nC
Gate-Source Charge	$Q_{gs}$			-	-	9.6	
Gate-Drain Charge	$Q_{gd}$			-	-	45	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 400 \text{ V}$ , $I_D = 4.1 \text{ A}$ , $R_G = 12 \Omega$ , $R_D = 95 \Omega$ , see fig. 10 <sup>b</sup>		-	12	-	ns
Rise Time	$t_r$		-	33	-		
Turn-Off Delay Time	$t_{d(off)}$		-	82	-		
Fall Time	$t_f$		-	30	-		
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal Source Inductance	$L_S$			-	7.5	-	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode		-	-	2.1	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	8.4	
Body Diode Voltage	$V_{SD}$	$T_J = 25^{\circ}\text{C}$ , $I_S = 2.1 \text{ A}$ , $V_{GS} = 0 \text{ V}^b$		-	-	1.8	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25^{\circ}\text{C}$ , $I_F = 4.1 \text{ A}$ , $dI/dt = 100 \text{ A}/\mu\text{s}^b$		-	480	720	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	1.8	2.7	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width  $\leq 300 \mu\text{s}$ ; duty cycle  $\leq 2\%$ .

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

**Fig. 1 - Typical Output Characteristics,  $T_C = 25^\circ\text{C}$** 

**Fig. 3 - Typical Transfer Characteristics**

**Fig. 2 - Typical Output Characteristics,  $T_C = 150^\circ\text{C}$** 

**Fig. 4 - Normalized On-Resistance vs. Temperature**

# IRFIBE30G, SiHFIBE30G

Vishay Siliconix

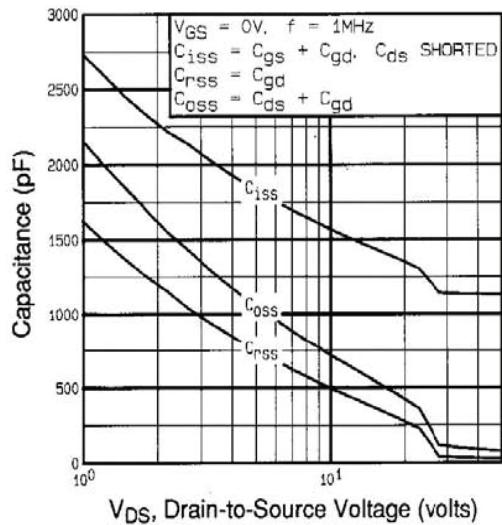


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

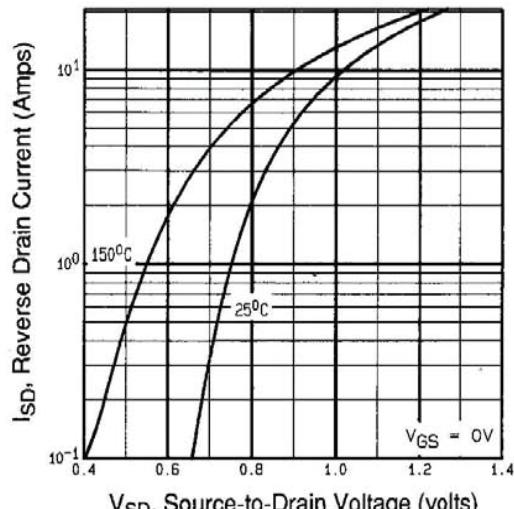


Fig. 7 - Typical Source-Drain Diode Forward Voltage

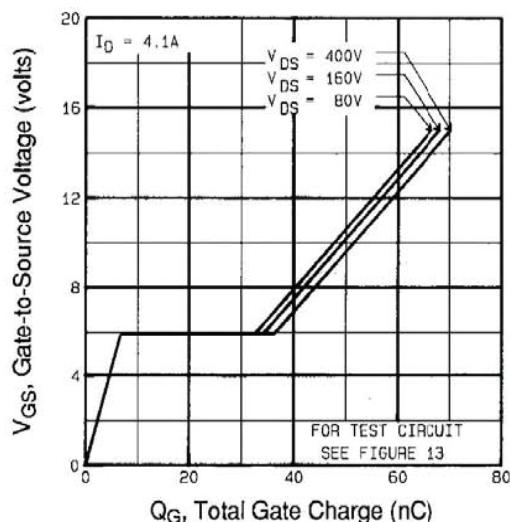


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

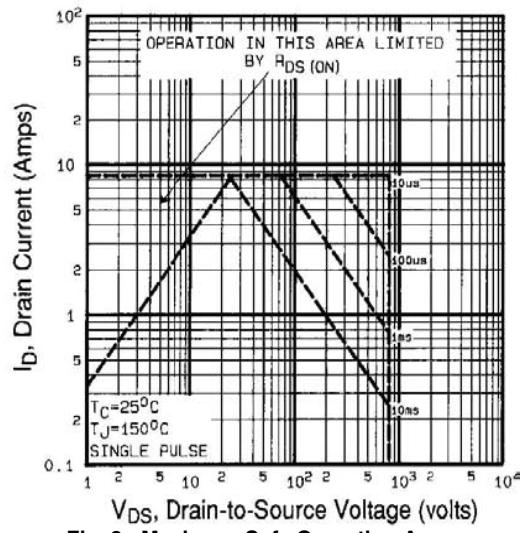


Fig. 8 - Maximum Safe Operating Area

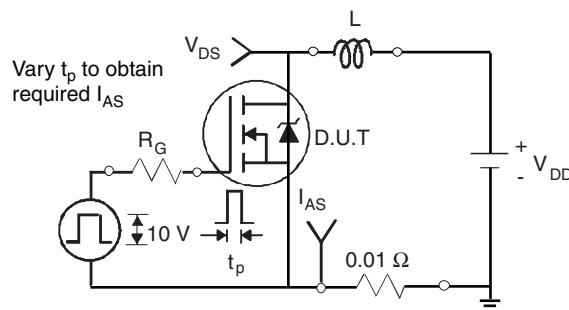


Fig. 9a - Unclamped Inductive Test Circuit

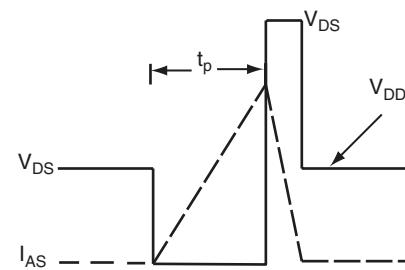


Fig. 9b - Unclamped Inductive Waveforms

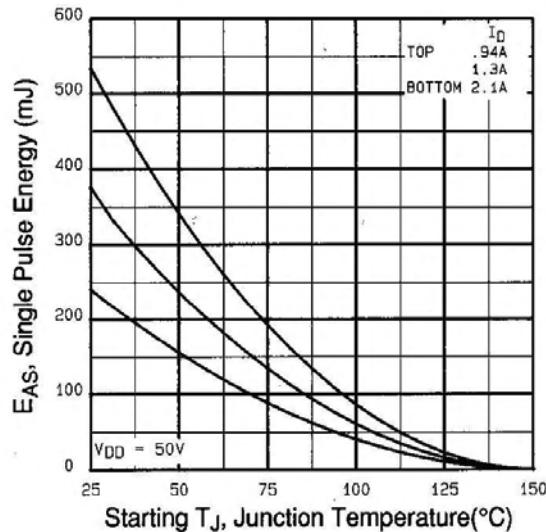


Fig. 9c - Maximum Avalanche Energy vs. Drain Current

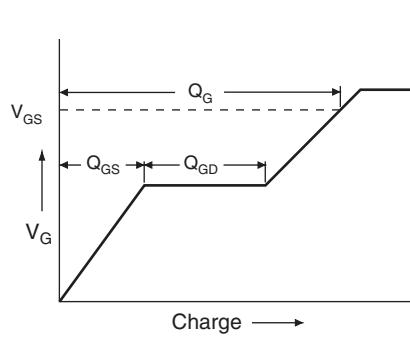


Fig. 10a - Basic Gate Charge Waveform

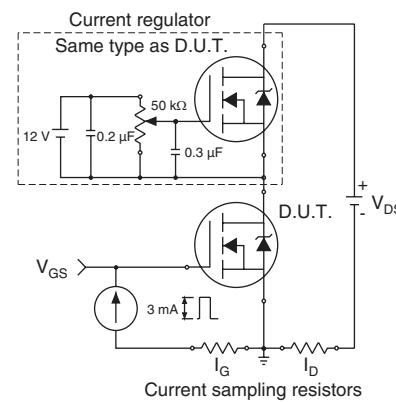
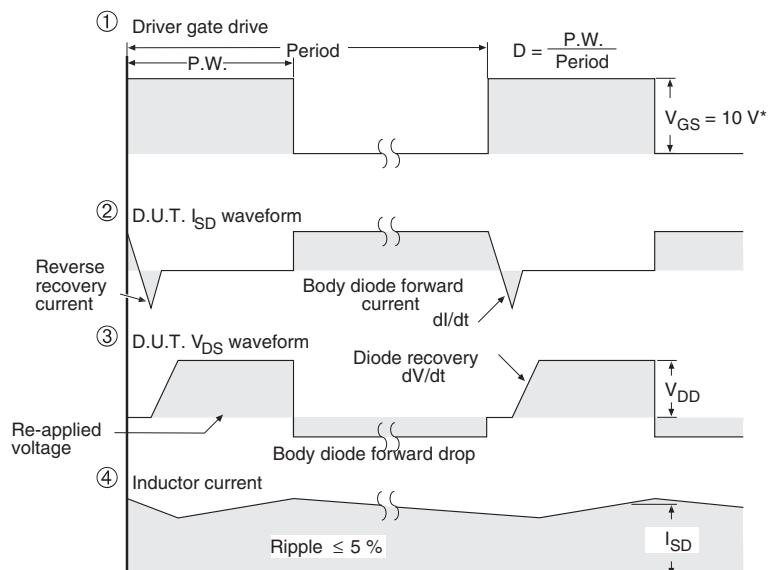
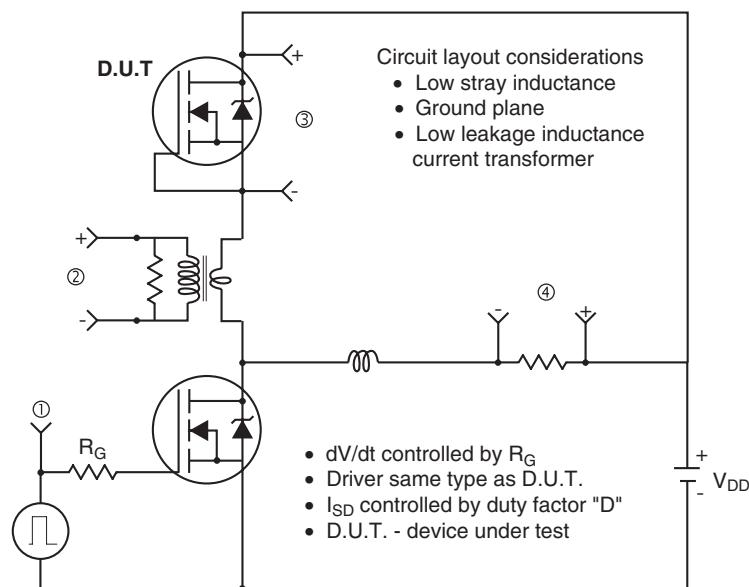


Fig. 10b - Gate Charge Test Circuit

### Peak Diode Recovery $dV/dt$ Test Circuit



\*  $V_{GS} = 5 \text{ V}$  for logic level devices

Fig. 11 - For N-Channel

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