

1.5-GHz Low-Phase Noise Clock Evaluation Board

This user's guide discusses the general operation and configuration of the Texas Instruments CDCE72010 evaluation board.

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1 Features

- Easy-to-use evaluation board to generate low-phase noise clocks up to 1.5 GHz
- Easy device programming via host-powered USB port
- Fast configuration through provided graphical user interface (GUI) software interface
- Total board power provided either through USB port or separate 3.3 V and ground connections.
- Single-ended or differential input reference clock
- Crystal filter on output readily available for clocking high-speed analog-to-digital converters, if needed.

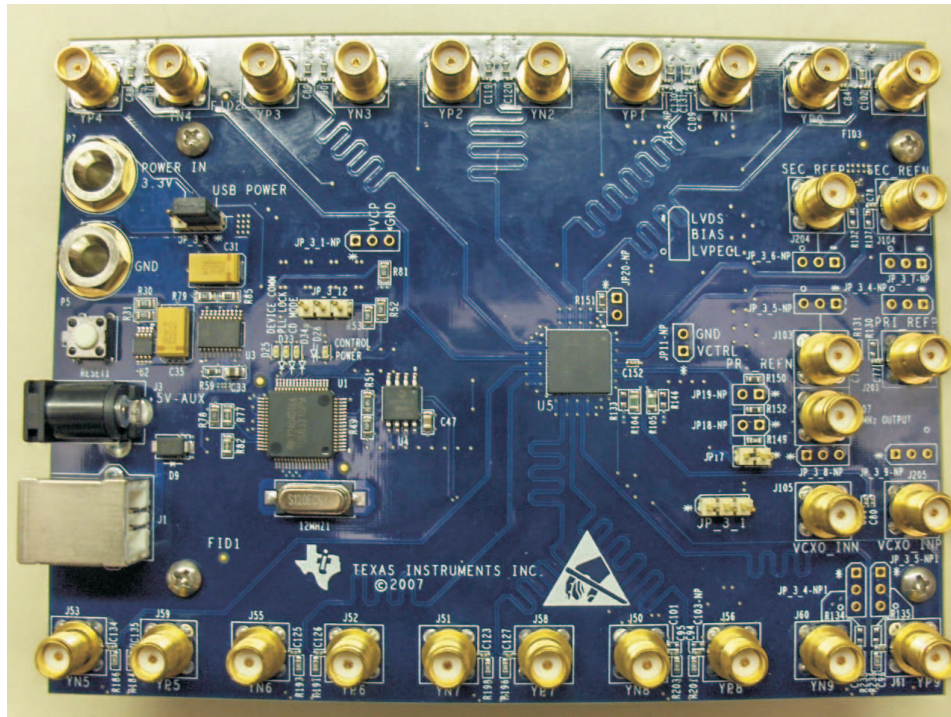


Figure 1. CDCE72010EVM Board

2 General Description

The CDCE72010 is a high-performance, low-phase noise clock synchronizer and jitter cleaner. It has one main universal VCO/VCXO input buffer and an auxiliary universal input buffer. Either Input can drive the outputs and/or the feedback path to the PFD. The maximum VCXO/VCO input frequency is 1.5 GHz. It provides support for two redundant input references and using its on-chip PLL architecture can provide up to ten differential or 20 single-ended low jitter outputs.

The CDCE72010 supports two reference inputs, which can be differential or single-ended. It also provides two VCXO inputs, which can drive up to ten outputs.

The CDCE72010 then can be programmed through the SPI interface using the evaluation module (EVM) programming GUI.

The evaluation module (EVM) is designed to demonstrate the electrical performance of the device.

This fully assembled and factory-tested evaluation board allows complete validation of all device functions.

For optimum performance, the board is equipped with 50-Ω SMA connectors and well-controlled 50-Ω impedance microstrip transmission lines.

3 Signal Path and Control Circuitry

The CDCE72010 provides support for selectable tri-inputs, and two of the inputs (PRI REF and SEC REF) can accept a 8-kHz to 500-MHz frequency input from a differential signal source or a 8-kHz to 200-MHz frequency input from a single-ended signal source.

The CDCE72010 provides support for up to ten differential (LVDS or LVPECL) or 20 single-ended (LVCMOS) or any combination of outputs up to 1.5 GHz. On the CDCE72010EVM, output 1 and output 8 have a footprint option for installing crystal filters that can drive the phase noise floor down by 10 dB or 15 dB. This filtered signal is intended to be used for clocking high-performance, high-speed analog-to-digital converters (ADC).

The CDCE72010 requires an external loop filter. The loop filter selection determines the PLL loop stability and also affects the phase noise of the output. The EVM provides four sets of filters optimized for a 30.72-MHz reference and 491.52-MHz VCXO. For any output of the CDCE72010, the frequency is determined by the selection of the VCO/VCXO and the setting of the output divider. The output jitter performance is determined by the PLL settings (including the PFD frequency, charge pump current, and the loop filter). See the CDCE72010 data sheet for more details and configuration settings.

Each of the ten outputs of the CDCE72010 can be selected through the software interface as LVPECL, LVDS, or LVCMOS. The CDCE72010EVM provides software selectable 150- Ω current-setting resistors.

The LVCMOS outputs work for frequencies up to 250 MHz; the LVDS outputs run up to 800 MHz; and LVPECL outputs function up to 1.175 MHz (these are all minimum frequencies).

4 Software Selectable Options

The provided GUI software allows users to easily send commands to the CDCE72010 through the host-powered USB interface. The EVM includes a slave USB controller that transmits the commands to the SPI programming interface included on the CDCE72010. The DC power for the USB controller can either be derived from the 5-V power pin in the USB cable or by using an external 5-V DC adapter into the slot available on the EVM. If the device is accessible for programming by the SPI programming interface through the USB controller, the onboard LED D25 is illuminated on power up.

In addition to writing commands to the CDCE72010 RAM while the board is powered, commands also can be stored in CDCE72010 EEPROM. This allows users to start the EVM in the desired state without needing programming at power up.

Note that the CDCE72010 has a permanent EEPROM lock mode. After this mode is selected, the EEPROM within the CDCE72010 cannot be changed. This is useful when setting final configurations.

The CDCE72010EVM software also provides support for the device GUI configurations to be saved into a configuration file, which can be opened at a later time with this GUI.

5 Installing the GUI Interface and USB Driver

To start installation, run the *CDCE72010 Control GUI v1.X.X.msi* file.

Make note of the installation folder because you may need to refer to it when the USB cable is connected and asks for the location of a driver file.

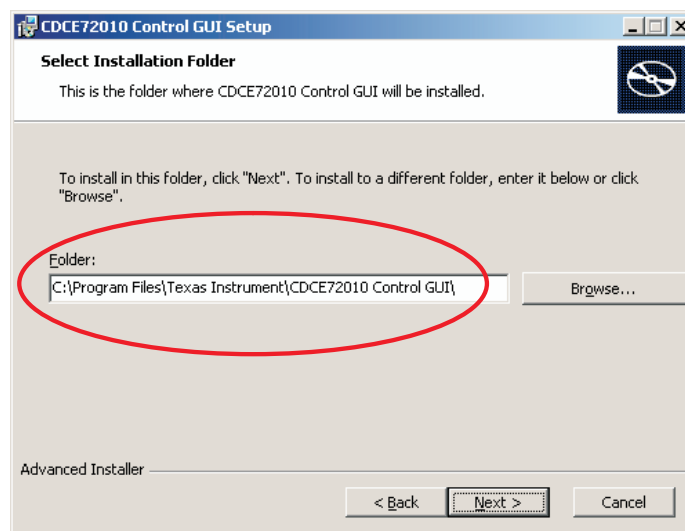
After the setup wizard has completed, start the GUI interface from the start menu (Start → CDCE72010 Control GUI).



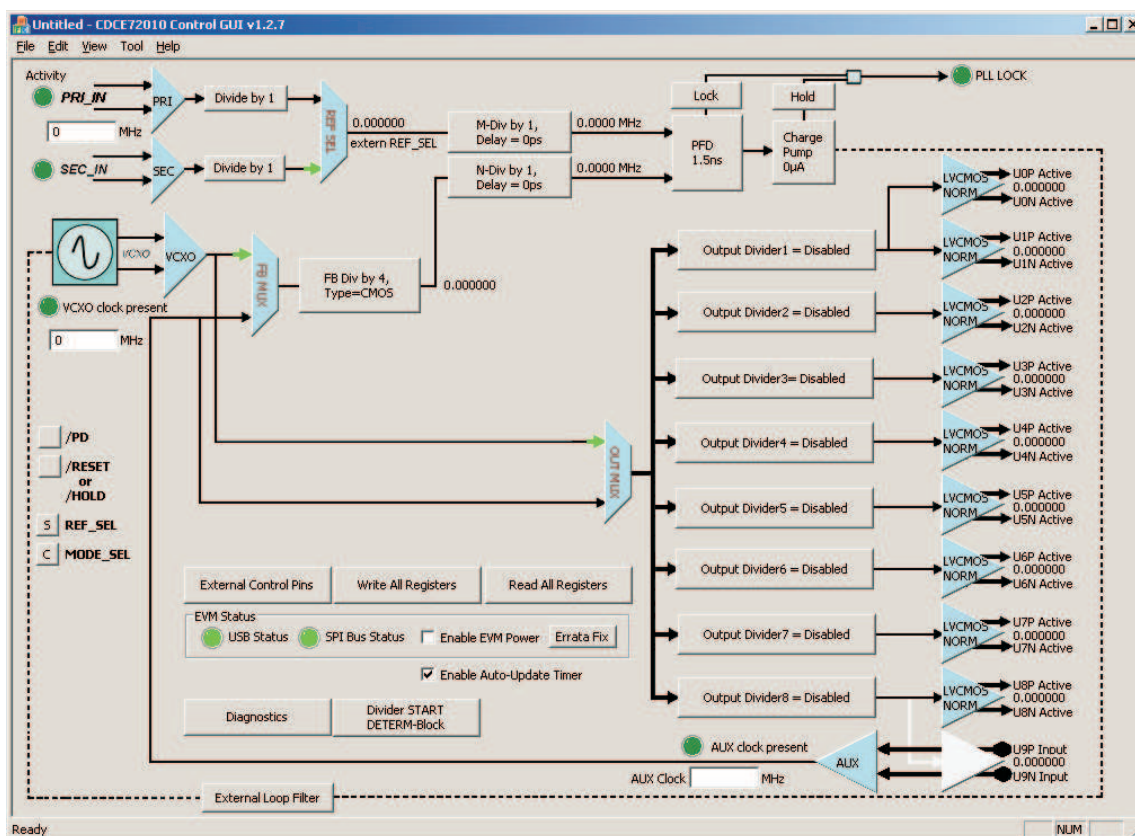
Connect the USB cable to the EVM. If The Windows™ operating system asks for an appropriate driver, do not use the automatic search option. Select a manual installation, and when prompted for the driver location, browse to the CDCE72010 GUI file folder that was used during installation. If the Windows operating system does not ask for a driver, no action is required.

After the USB driver installation, the GUI software must connect properly and be ready for use. A green light in the USB Status and SPI Bus Status boxes indicates good USB connection, and a red light indicates faulty USB connection or faulty SPI bus.

Note program file location as the USB controller driver is in the same location!



6 CDCE72010 Control GUI Interface



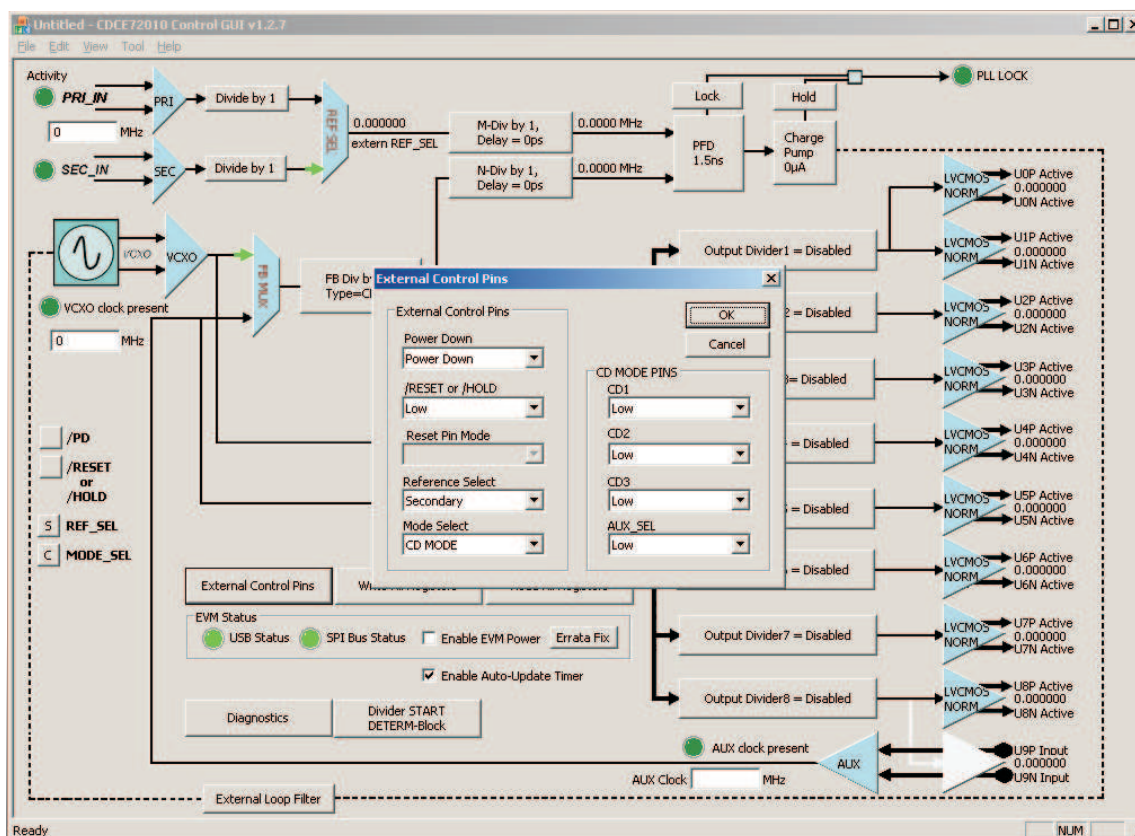
7 TI CDCE72010 Control GUI Interface

7.1 Using Software-Enabled PLL Selection

The illustration in the software shows the block diagram of the CDCE72010. In this illustration, the user can change the Input Frequency, Input Divider, Input type, Input selection, PFD Charge Pump, Output Divider, and Output type. The rest are selected by the software with user-selectable options as described in the steps below. If the power to the CDCE72010 is derived from the USB, the *Enable EVM Power* button needs to be checked. If the power to the CDCE72010 is derived from an external source, the *Enable EVM Power* button needs to be unchecked.

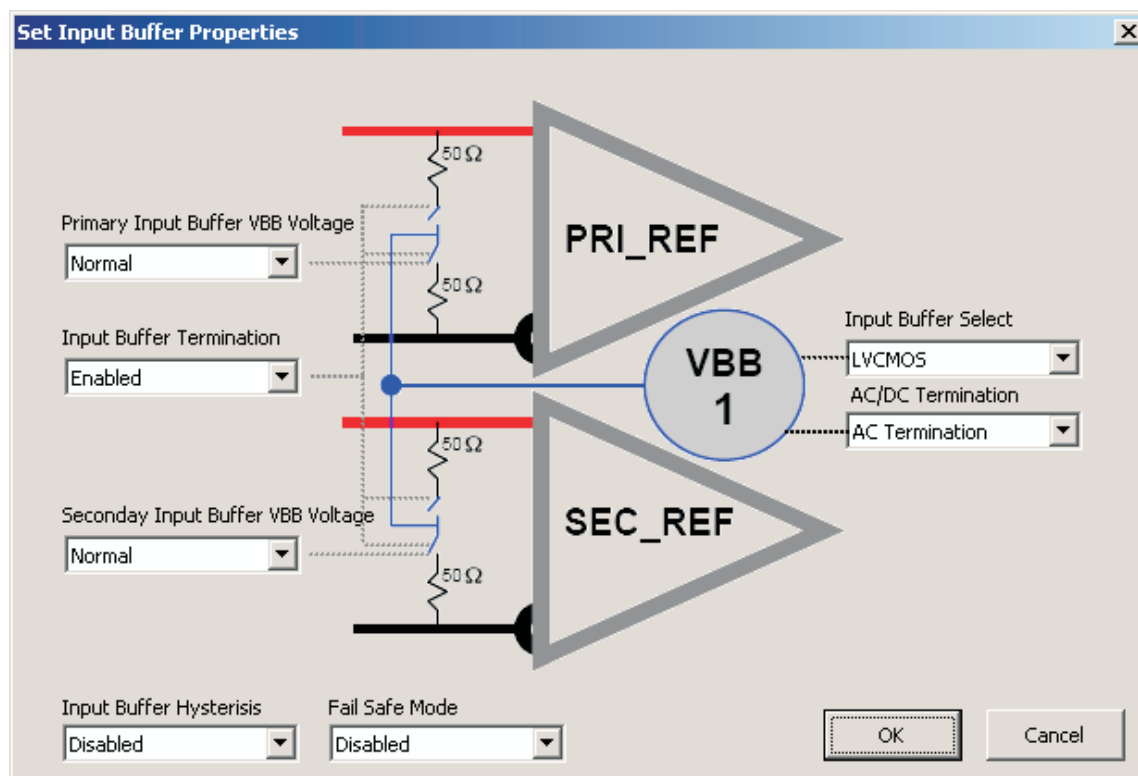
Step 1: External Control Pins Selection

Before programming the PLL, select the External Control Pins button in the *EVM Status* section of the GUI. The selections on this popup window, as shown in the following illustration, must be selected according to the desired working configuration of the CDCE72010.



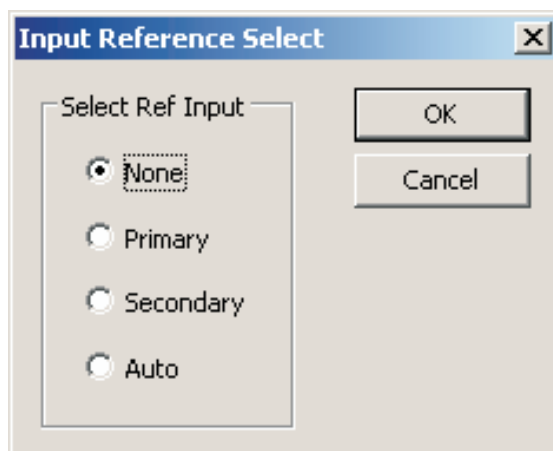
Step 2: Primary/Secondary Reference Input Selection

The primary or the secondary reference input buffer section on the GUI can be clicked for a popup window that opens up, as shown in the following illustration. This illustration shows selections on the external input signal type (differential or single ended), the external signal connection to the CDCE72010 primary/secondary inputs (AC or DC termination), input buffer internal termination (enabled or disabled), input buffer VBB voltage polarity (normal or inverted), input buffer hysteresis, and fail-safe mode (enabled or disabled).



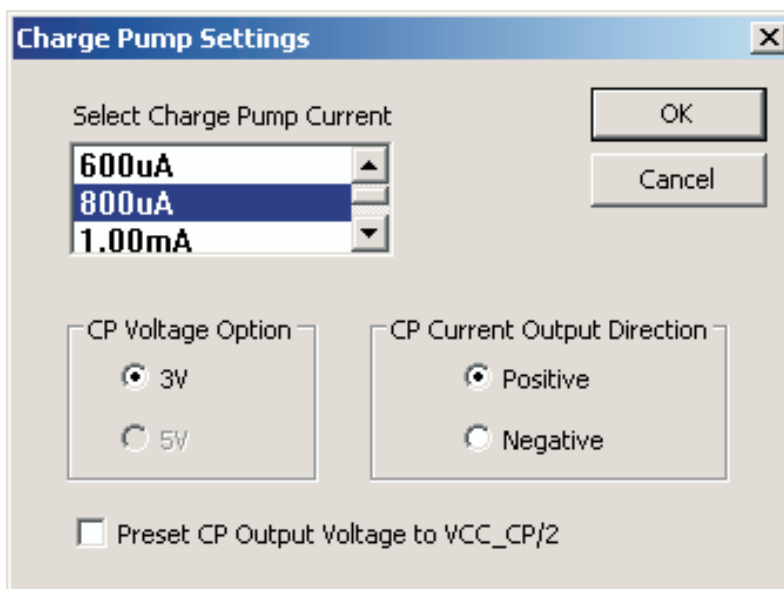
Step 3: Reference Input Selection through Smart MUX

The Smart MUX section of the GUI can be clicked for a popup window that opens up as displayed in the following illustration, showing selections of Primary, Secondary, Auto (with Primary preference), and None.



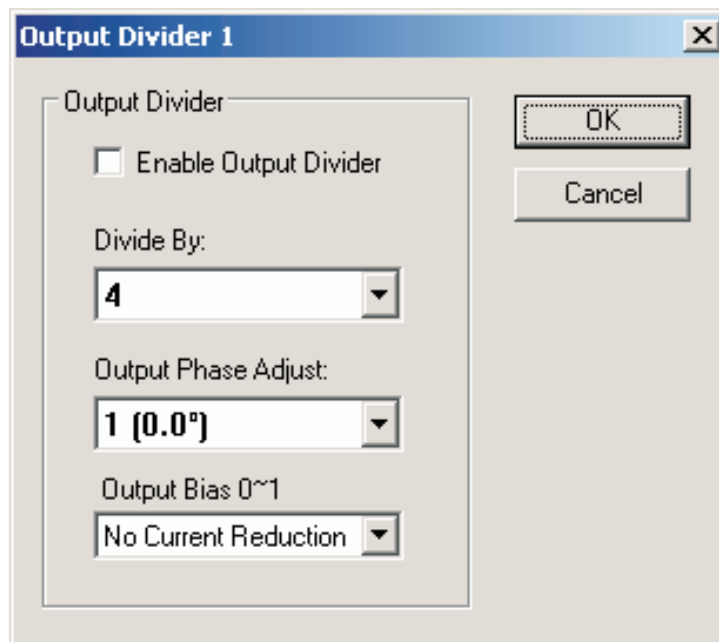
Step 4: PFD and Charge Pump Selection

The PFD and Charge Pump section of the GUI can be clicked for a popup window that opens up. The following illustration shows selections on the charge pump current and charge pump pulse width.



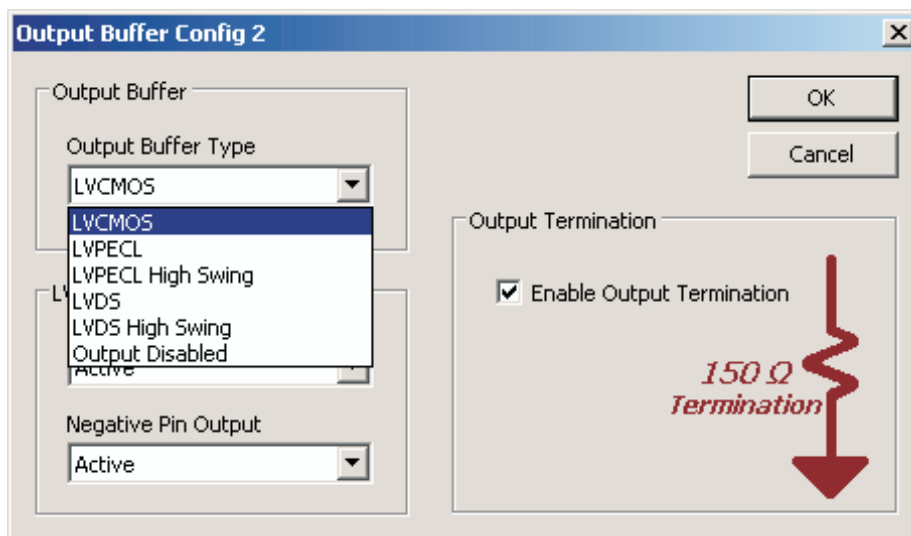
Step 5: Output Divider

The CDCE72010 has 10 outputs and 8 Output Dividers. Outputs 0 and 1 share the same divider, and outputs 8 and 9 share the same divider. The Output Divider and the Output Phase Adjust are accessed by clicking on the divider needed.



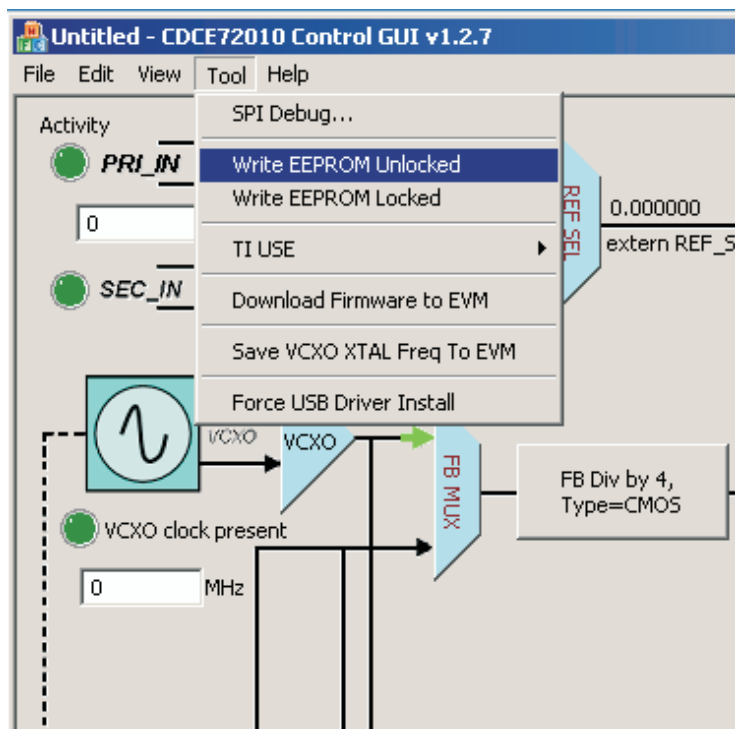
Step 6: Output Type Selection

The Output Buffer section of the GUI for each of the five outputs can be clicked for a popup window that opens up, as displayed in the following illustration. For each output clock source, the user can select LVPECL, LVPECL High Swing (in which cases the output 150-Ω termination is automatically enabled), LVDS, LVDS High Swing, or LVCMOS. In CMOS mode, the P and N outputs become separate CMOS outputs running at the same frequency. Either CMOS output can be active, inverting, tri-state or low. Each output can be independently disabled.



Step 7: Write to CDCE72010 EEPROM

To write any particular setting to the EEPROM (locked or unlocked), the menu item at the top of the GUI entitled *Tool* must be clicked which reveals the items *Write EEPROM Unlocked* and *Write EEPROM Locked* as part of a drop-down menu. Choosing the appropriate one after setting the desired PLL configurations results in writing to the EEPROM in the selected mode.



8 Configuring the Board

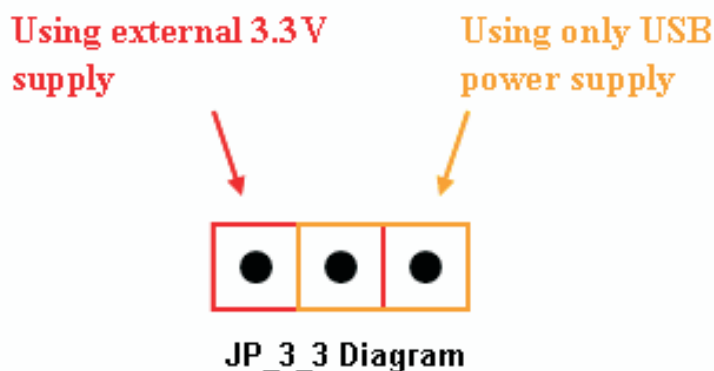
The CDCE72010EVM can be powered from the USB power supply or from an external source. The CDCE72010EVM only needs a USB cable attached for programming purposes. However, for test measurements, it is recommended to also use an external 3.3-V power supply. Test measurements also can be taken with only the USB-supplied power. However, due to USB port power limitations, results may degrade. It is also possible to program the CDCE72010 and then disconnect the USB cable (may require minor board configuration changes).

8.1 Default Configuration for Programming and Testing With USB Cable Attached

The CDCE72010EVM is configured by default to operate with the USB cable attached and a 3.3-V power supply added to EXT VDD and GND. In this configuration, the USB microcontroller is powered by the USB port's 5-V supply whereas the CDCE72010 is powered by the 3.3-V external supply. This setup is optimal for programming the CDCE72010 while also taking measurements. This configuration removes the power variation found in USB power supplies by isolating the CDCE72010 from the USB supply.

8.2 Configuration for Programming With USB Cable Attached

The CDCE72010EVM can use power supplied through the USB cable as its sole power source. However, due to power supply variances in the USB supply, this configuration is not recommended for measurements. This setup is for saving configuration settings to the CDCE72010 and later powering the device from its internal memory (useful if a USB port is unavailable in a laboratory or test chamber). In this configuration, JP_3_3 must be moved from its default position to the new position shown in the following illustration. Also, the Enable EVM Power box must be checked on the EVM GUI interface software.

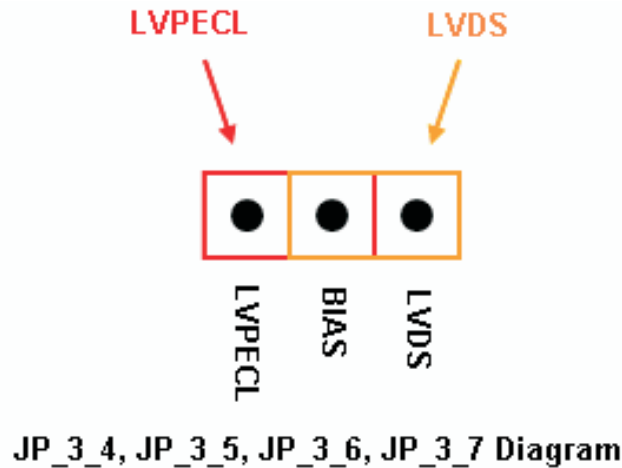


8.3 Configuration for Testing From a Saved Configuration With USB Cable Removed After Programming

When operating the CDCE72010 without the USB programming cable (useful in laboratory settings in which a PC is unavailable at the laboratory station), the CDCE72010 needs to be configured and saved in the EEPROM in one of the preceding configurations and then reconfigured for external power supply usage.

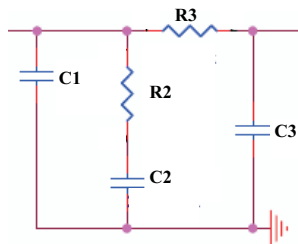
Prior to making these board modifications, the CDCE72010 settings must be saved with one of the USB cable attached configurations. The *Write EEPROM Unlocked* or *Write EEPROM Locked* software button must be used to save the CDCE72010 to its internal EEPROM. After the settings are saved to EEPROM, the USB cable can be removed. Once the cable has been disconnected, JP_3_3 must be in the *Using External 3.3V Supply* position (as seen in the preceding diagram). The EVM now is ready for use without the USB cable connected. The CDCE72010 always starts from its saved configuration state in this mode.

Configuration for Onboard Reference Input Biasing. If the on-chip biasing is not used in the CDCE72010 for AC-coupled reference input signals for PRI_REF or SEC_REF, the CDCE72010EVM alternately can be set up to provide onboard biasing for LVPECL or LVDS inputs. These bias voltages of 1.2 V for LVDS and 1.9 V for LVPECL are derived from the onboard voltage divider. The bias points are available for every leg of the differential signals at both PRI_REF and SEC_REF and can be enabled by using the jumpers on the CDCE72010EVM, JP_3_4 and JP_3_5 for PRI_REF and JP_3_6 and JP_3_7 for SEC_REF. Each of these jumpers can be configured as shown in the following diagram for either LVPECL or LVDS bias.



8.4 Configuration for Onboard External Loop Filter

If the CDCE72010 is chosen to be operated as a jitter cleaner, it requires use of the partially external loop filter which is located at the back side of the CDCE72010EVM. The EVM provides four external loop filter options. The external loop filter topology is shown in the following diagram. The device can handle more complex filter topologies, including active loop filters, but the EVM is only designed to illustrate second-order filter topology. Remember that the loop filter is calculated for and operates with a particular PFD frequency, charge pump current, and PLL gain (determined by the feedback divider settings).



The external loop filter can be chosen by selecting one from the four available options on the CDCE72010EVM using the dip switches, SW9 and SW10, located at the back side of the EVM as shown in the following illustration. The four options are Filter1 = 1 kHz, Filter2 = 520 Hz, Filter3 = 120 Hz, and Filter4 = 15 Hz.

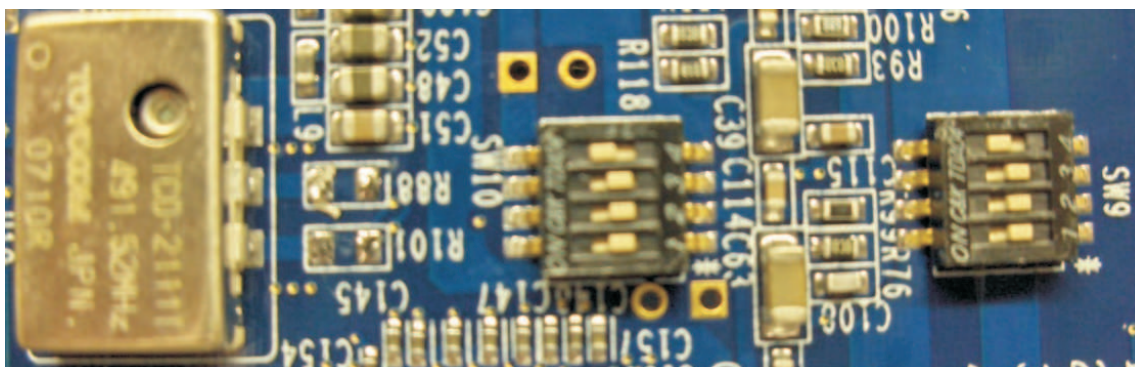
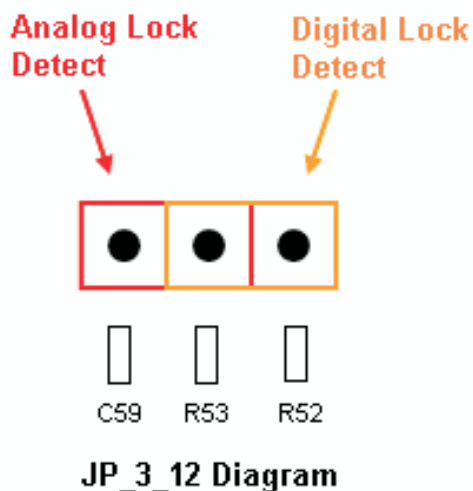


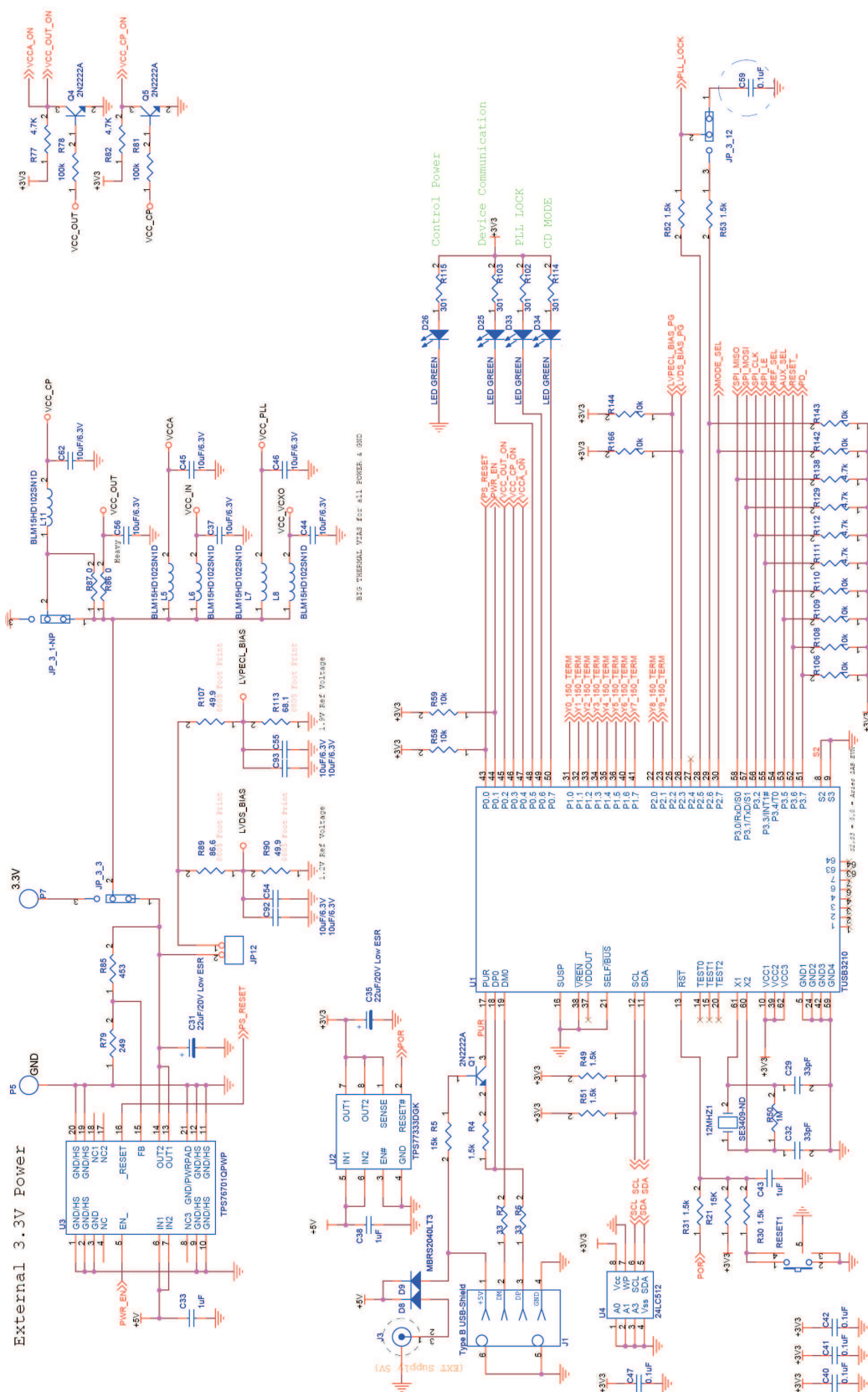
Figure 2. CDCE72010EVM External Loop Filter Topology

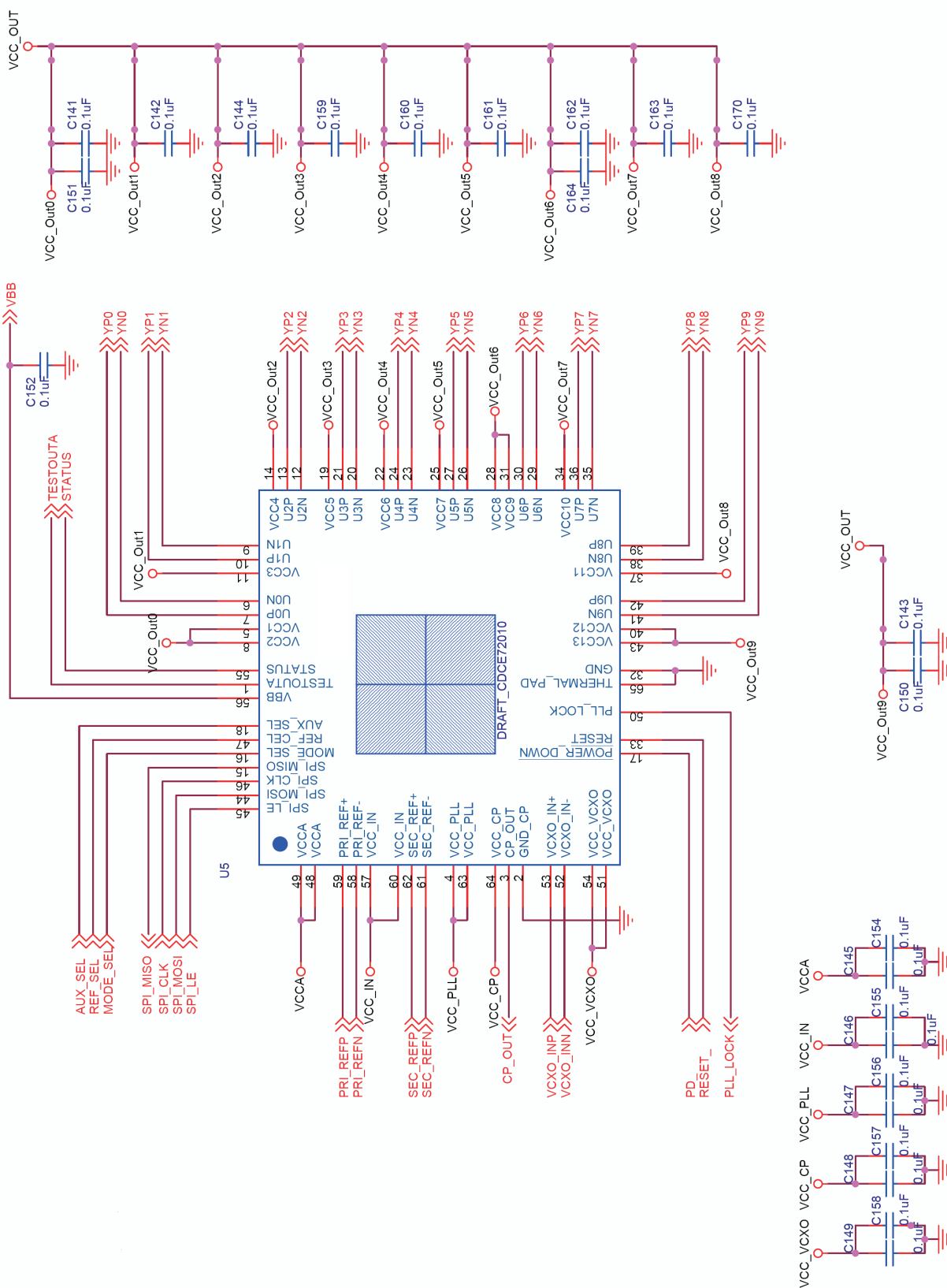
8.5 Configuration for PLL Lock Detect

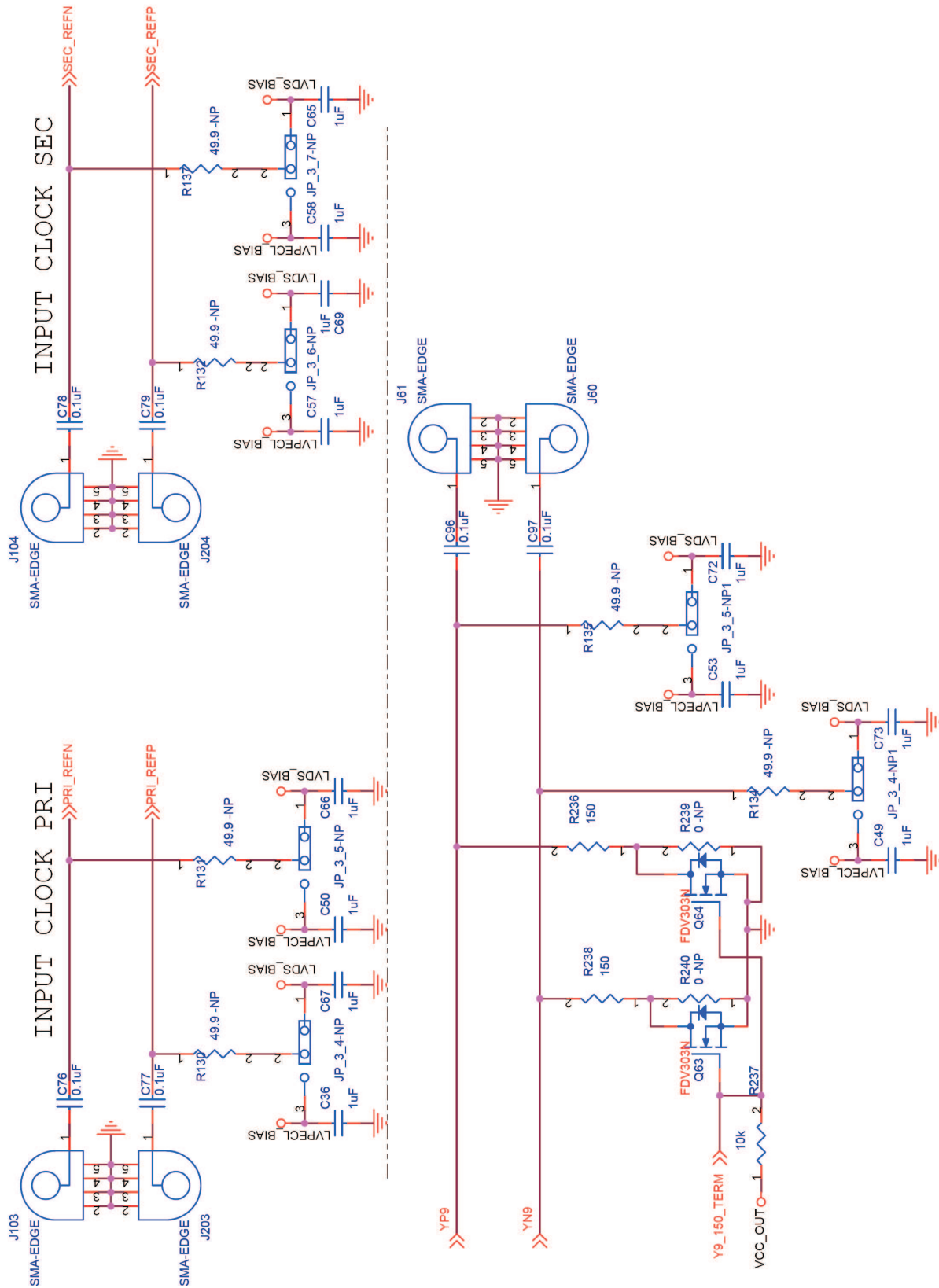
The CDCE72010 PLL lock detect can be chosen on the CDCE72010EVM as either an analog lock detect or a digital lock detect using the jumper, JP_3_12, located at the back side of the CDCE72010EVM. This jumper can be configured as shown in the following diagram for either analog or digital lock detect.

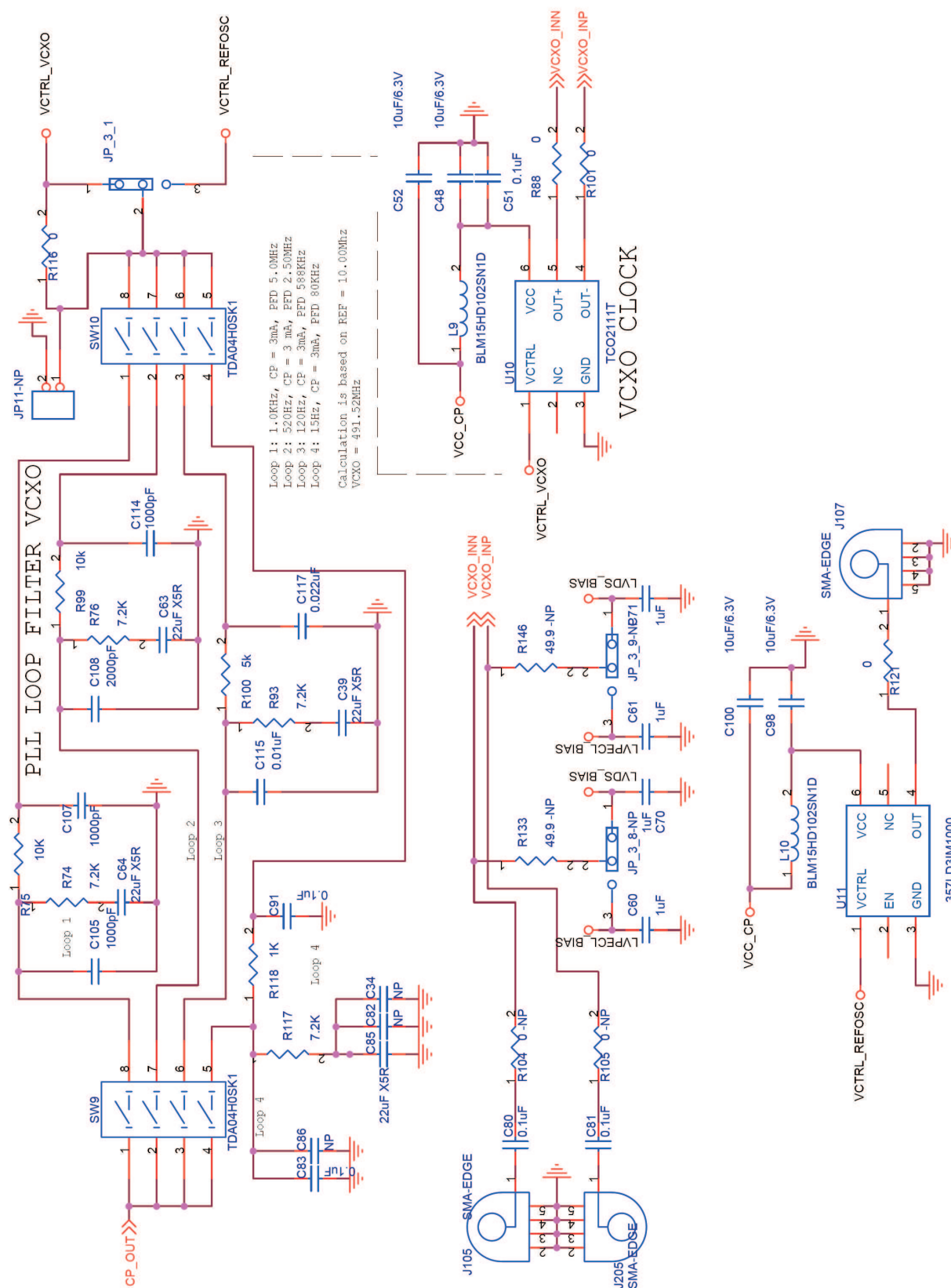


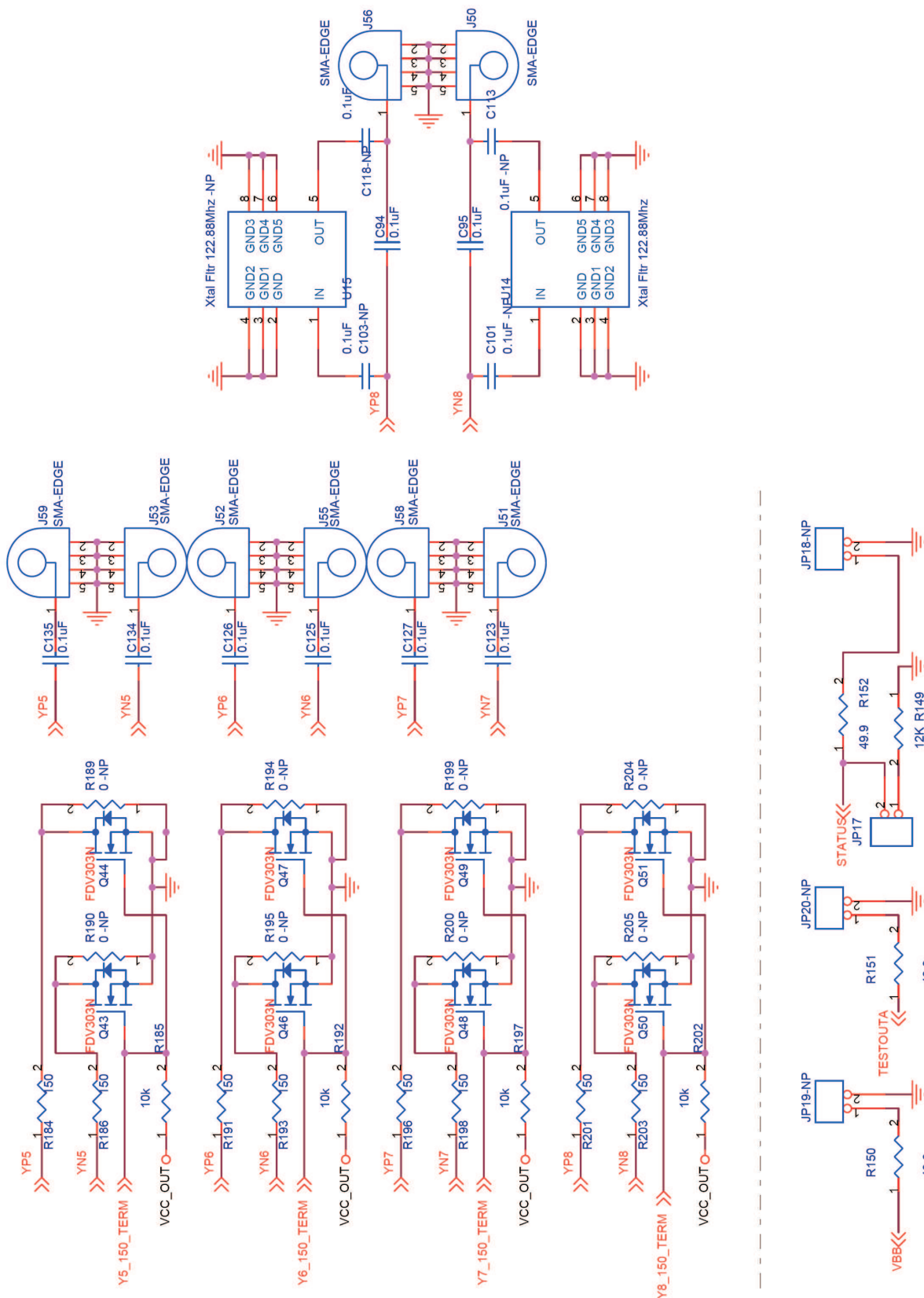
9 CDCE72010EVM Board Schematic Diagram











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It is important to operate this EVM within the input voltage range of 3 V to 3.6 V and the output voltage range of 0 V to 3.6 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

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During normal operation, some circuit components may have case temperatures greater than 120°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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