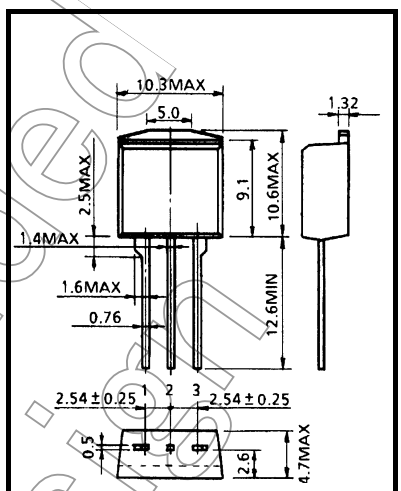
TOSHIBA Thyristor Silicon Planar Type

S6992

Condenser Discharge Control Applications

- Critical rate of rise of ON-state current: di/dt = 750 A/μs
- Repetitive surge ON-state current: I_{TRM} = 500 A (t_w = 2 μs)
- Repetitive peak OFF-state voltage: V_{DRM} = 800 V
- Gate trigger current: I_{GT} = 20 mA max.

Unit: mm



1. CATHODE
2. ANODE
3. GATE

JEDEC	—
JEITA	—
TOSHIBA	13-10J1B

Weight: 1.5 g (typ.)

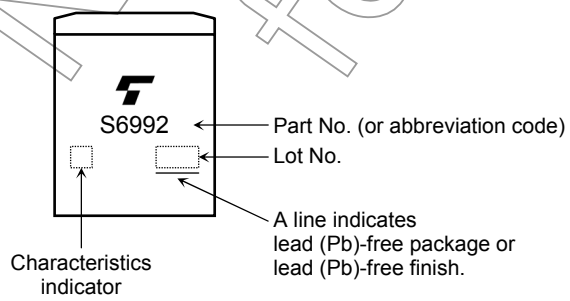
Absolute Maximum Ratings

Characteristics	Symbol	Rating	Unit
Repetitive peak OFF-state voltage	V_{DRM}	800	V
Repetitive peak surge ON-state current (Note 1)	I_{TRM}	500	A
Critical rate of rise of ON-state current (Note 1)	di/dt	750	A/μs
Peak gate power dissipation	P_{GM}	5	W
Average gate power dissipation	$P_{G\ (AV)}$	0.5	W
Peak forward gate voltage	V_{FGM}	10	V
Peak reverse gate voltage	V_{RGM}	−5	V
Peak forward gate current	I_{GM}	2	A
Junction temperature	T_j	−40~125	°C
Storage temperature range	T_{stg}	−40~150	°C

Note 1: $V_D \leqq 0.8 \times$ rated, Tc = 85°C, $i_{gp} \geqq 40$ mA, $t_{gw} \geqq 10$ μs, $t_{gr} \leqq 150$ ns

Note 2: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

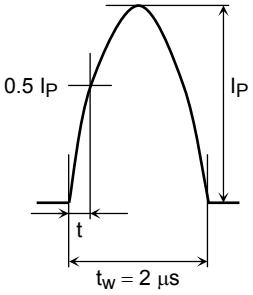
Marking



*: There is no reverse-blocking (reverse voltage) ability.

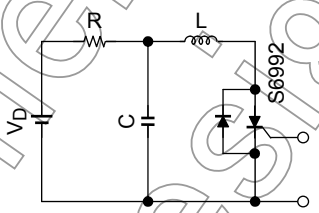
Electrical Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Repetitive peak OFF-state current	I_{DRM}	V_{DRM} = rated	—	—	10	μA
Peak ON-state voltage	V_{TM}	I_{TM} = 25 A	—	—	1.5	V
Gate trigger voltage	V_{GT}	V_D = 6 V, R_L = 10 Ω	—	—	1.0	V
Gate trigger current	I_{GT}		—	—	20	mA
Gate non-trigger voltage	V_{GD}	V_D = rated, Tc = 125°C	0.2	—	—	V
Critical rate of rise of OFF-state voltage	dv/dt	V_{DRM} = rated, Tc = 125°C Exponential rise	—	50	—	V/μs
Holding current	I_H	V_D = 6 V, I_{TM} = 1 A	—	—	40	mA
Thermal resistance	$R_{th\ (j-a)}$	Junction to ambient	—	—	70	°C/W



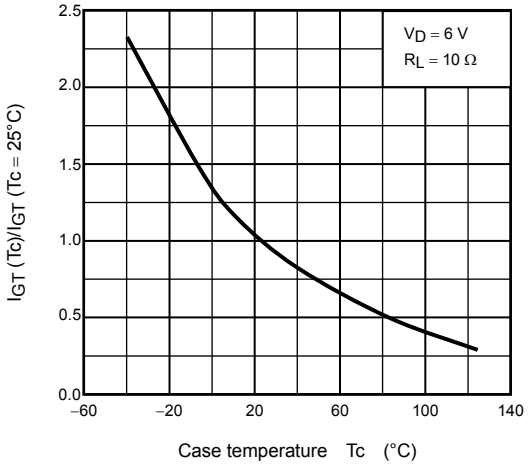
$$di/dt = \frac{0.5\ I_P}{t}$$

Test Circuit Examples

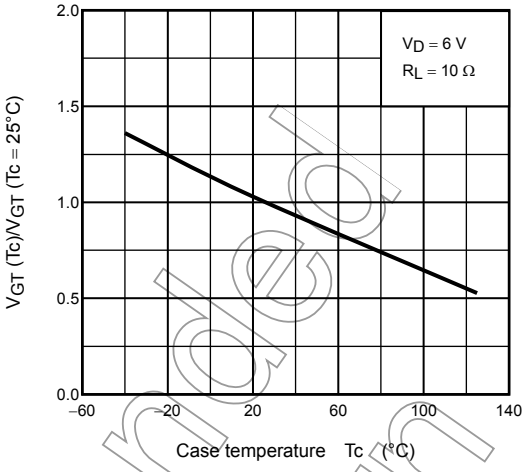


$$t_w \simeq \pi\sqrt{LC}\ ,\ I_P \simeq \frac{V_D}{\sqrt{L/C}}$$

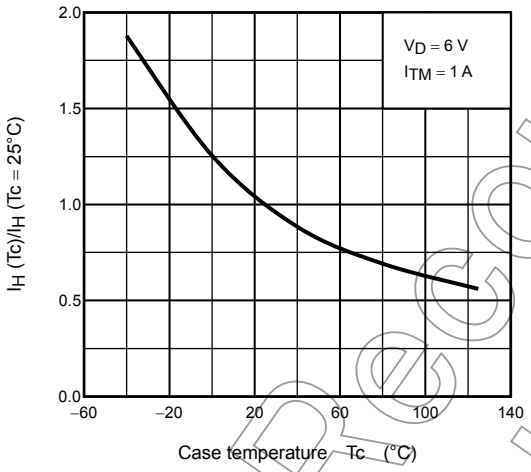
I_{GT} (Tc)/I_{GT} (Tc = 25°C) – Tc (typical)



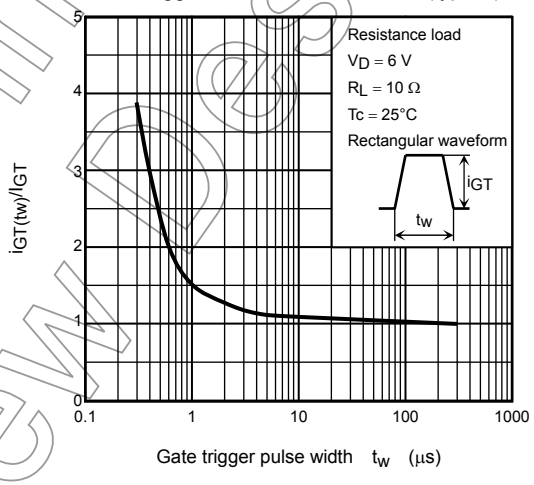
V_{GT} (Tc)/V_{GT} (Tc = 25°C) – Tc (typical)



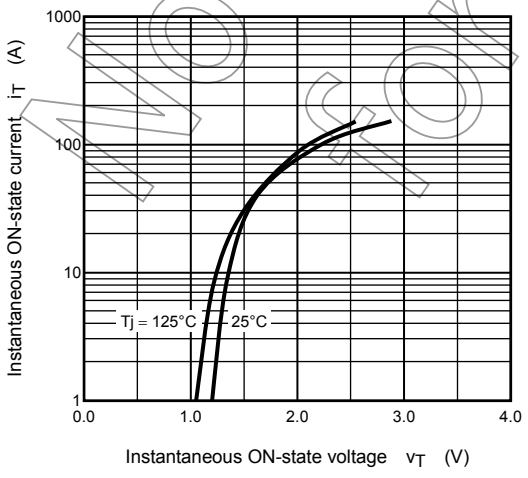
I_H (Tc)/I_H (Tc = 25°C) – Tc (typical)



Pulse trigger characteristics (typical)



i_T – v_T



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