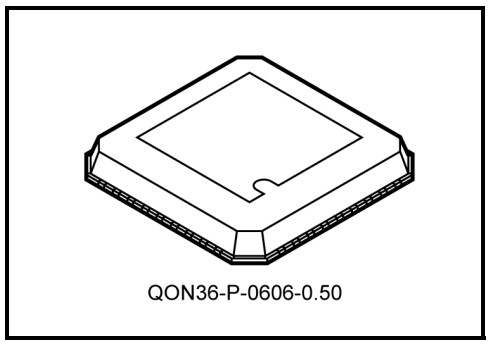
TOSHIBA BiCD Integrated Circuit Silicon Monolithic

TB6557FLG

DC Motor Driver

The TB6557FLG is a driver IC for driving DC motors. Its employs LDMOS devices with low ON resistance for output drive transistors. The TB6557FLG incorporates two constant current-controlled H-bridge drivers and four voltage-controlled H-bridge drivers, making it ideal for controlling Zoom/AF/IRIS lens motors in digital still cameras and camcorders. It supports three-wire serial data to control motors, thus reducing the number of lines for interfacing the control IC.



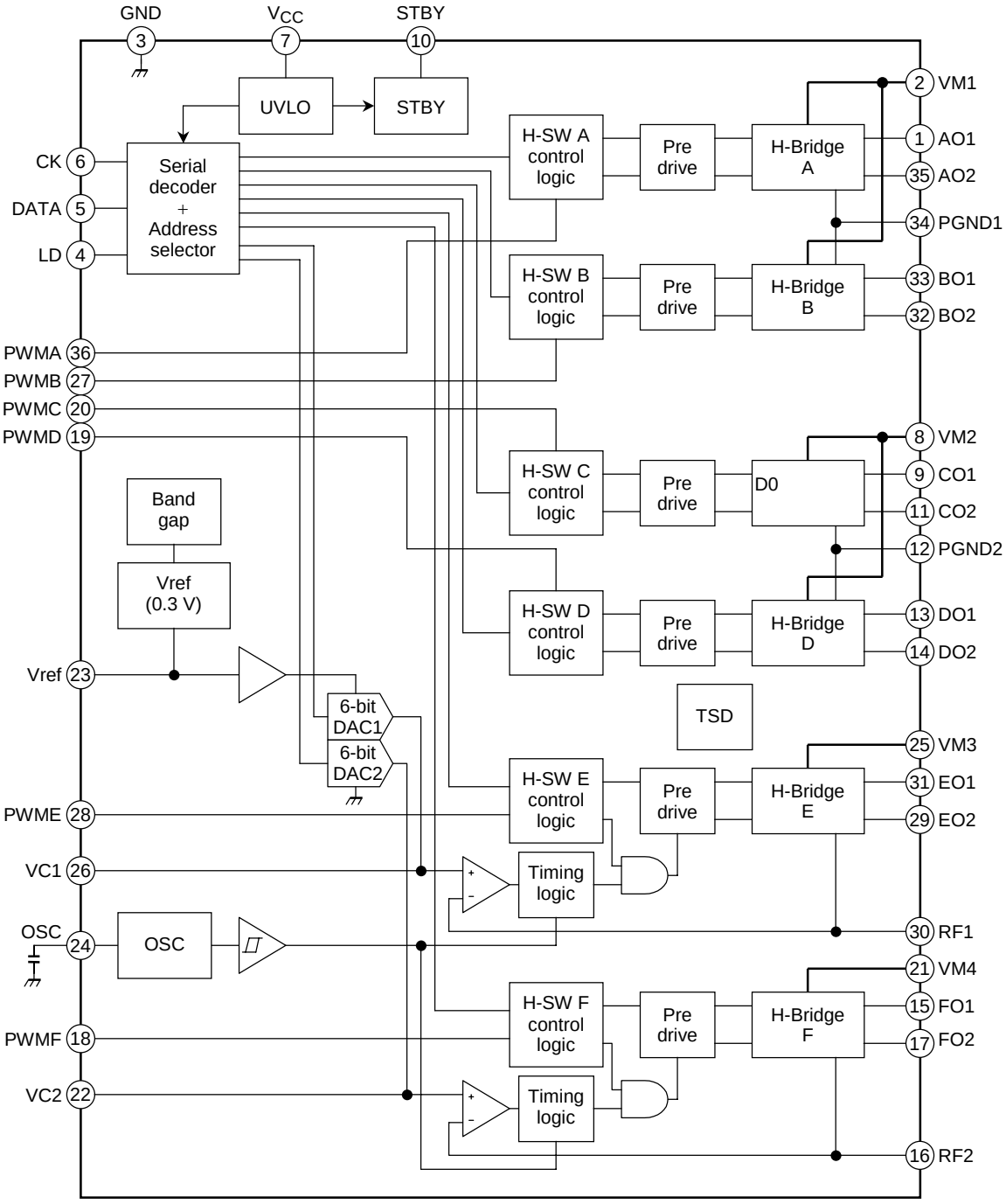
Weight: 0.08 g (typ.)

Features

- Motor power supply voltage: $V_M \leq 15$ V (max)
- Control power supply voltage: V_{CC} = 2.7 to 6 V
- Output current: $I_{out} \leq 0.8$ A (max)
- P-/N-ch LDMOS complementary output transistors
- Output ON resistance: Ron (upper + lower) = 1.5 Ω (typ.)
- High-speed PWM chopping control at 100 kHz or higher (constant-current H-SW)
- Independent standby (Power save) feature
- Two 6-bit DACs for setting current value for constant-current H-SW
- Thermal shutdown (TSD) protective circuit
- Circuit for preventing malfunction at low voltage (shuts down internal circuits at UVLO: $V_{CC} \leq 2.2$ V (typ.)).
- Small QON-36 package (0.5-mm lead pitch)
- Supports Pb-free reflow mounting

Note: This product has a MOS structure and is sensitive to electrostatic discharge. When handling this product, ensure that the environment is protected against electrostatic discharge by using an earth strap, a conductive mat and an ionizer. Ensure also that the ambient temperature and relative humidity are maintained at reasonable levels.

Block Diagram



Maximum Ratings (Ta = 25°C)

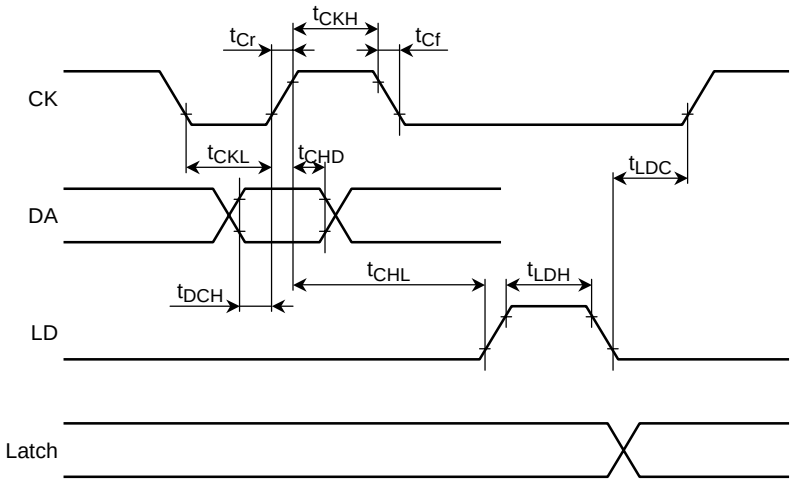
Characteristics	Symbol	Rating	Unit	Remarks
Supply voltage	V_{CC}	6	V	V_{CC}
Motor supply voltage	V_M	15	V	V_M
Output pin voltage	V_{OUT}	15	V	
Output current	I_{OUT}	0.8	A	
Input voltage	V_{IN}	−0.2 to 6	V	Each control input pin
Power dissipation	P_D	0.6	W	IC only
Operating temperature	T_{opr}	−20 to 85	°C	
Storage temperature	T_{stg}	−55 to 150	°C	

Recommended Operating Conditions (Ta = –20 to 85°C)

Characteristics	Symbol	Rating			Unit
		Min	Typ.	Max	
Small signal supply voltage	V_{CC}	2.7	3	5.5	V
Motor supply voltage	V_M	2.5	5	13.5	V
Output current	I_{OUT}	—	—	600	mA
PWM frequency	f_{PWM}	—	—	100	kHz
OSC oscillation frequency	f_{OSC}	—	—	1	MHz

Recommended Operating Conditions 2: Serial Data Controller (Ta = −20 to 85°C)

Characteristics	Symbol	Rating		Unit
		Min	Max	
Low-level clock pulse width	t_{CKL}	200	—	ns
High-level clock pulse width	t_{CKH}	200	—	ns
Clock rise time	t_{Cr}	—	50	ns
Clock fall time	t_{Cf}	—	50	ns
Data setup time	t_{DCH}	30	—	ns
Data hold time	t_{CHD}	60	—	ns
Load setup time	t_{CHL}	200	—	ns
Load hold time	t_{LDC}	100	—	ns
High-level load pulse width	t_{LDH}	100	—	ns
Latch output settling time	t_{LDD}	—	100	μs
CK (clock pulse) frequency	f_{CLK}	—	2.5	MHz
LD (load pulse) frequency	f_{LD}	—	1.5	MHz

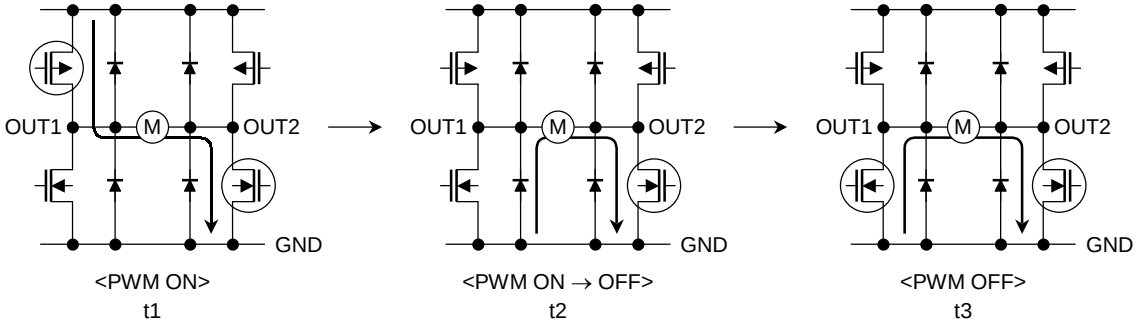


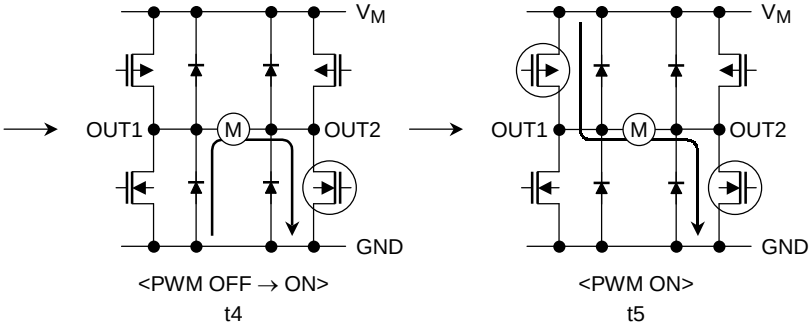
Specifications and Operation of Each Circuit Block:

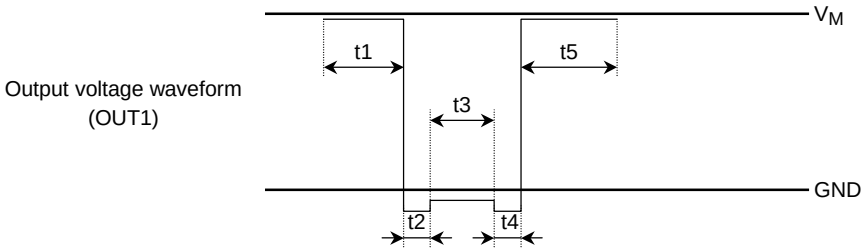
- Bridge output block:

PWM control feature

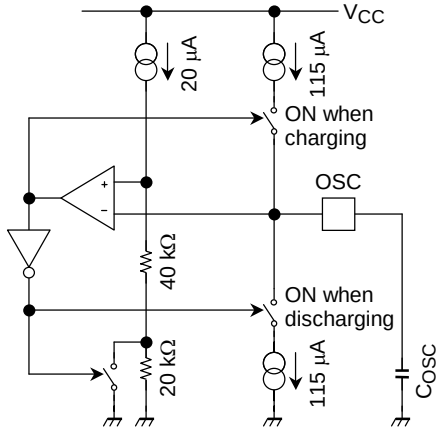
While PWM control is applied, normal operation t1, t5, and short brake t3 are repeated.
(Dead time t2 and t4 are inserted to prevent pass-through current.)



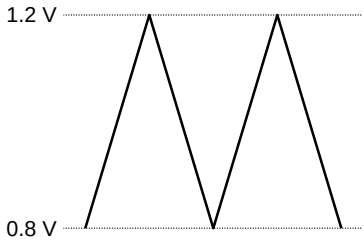




Operation of OSC oscillator: Charging and discharging external capacitor C_{OSC} cause OSC oscillation.



OSC block



V_{OSC} waveform

In the above circuit configuration, the voltage inclination, V_{OSC}, for charging (or discharging) external capacitor C_{OSC} is represented as follows:

$$V_{OSC} = \frac{1}{C_{OSC}} \int i \, dt$$

The following equations show relationships among t1 (time when V_{OSC} = 0.8 V), t2 (time when V_{OSC} = 1.2 V), and ΔV_{OSC} (variation in the V_{OSC} inclination):

$$\Delta V_{OSC} = I \times (t1 - t2)/C_{OSC}$$

$$\frac{1}{t1 - t2} = \frac{I}{\Delta V_{OSC} \cdot C_{OSC}}$$

The triangular oscillation frequency, f_{OSC}, represents a single period consisting of a pair of rising V_{OSC} inclination and falling inclination, so that the period is double the time between t1 and t2.

$\therefore$ Therefore, the relationship between C_{OSC} and f_{OSC} is shown by the following formula:

$$f_{OSC} = \frac{1}{2\,(t1 - t2)} = \frac{I}{2 \cdot \Delta V_{OSC} \cdot C_{OSC}}$$

With the above OSC block and V_{OSC} waveform, V_{OSC} = | 1.2 V – 0.8 V | = 0.4 V, so that the value of f_{OSC} is determined from the following formula:

$$f_{OSC} = \frac{1}{2 \times 0.4/115\ \mu A \times C_{OSC}} = \frac{1}{6.957 \times 10^3 \times C_{OSC}}$$

Example: The calculation shows f_{OSC} = 532 kHz when C_{OSC} = 270 pF and
f_{OSC} = 256 kHz when C_{OSC} = 560 pF.

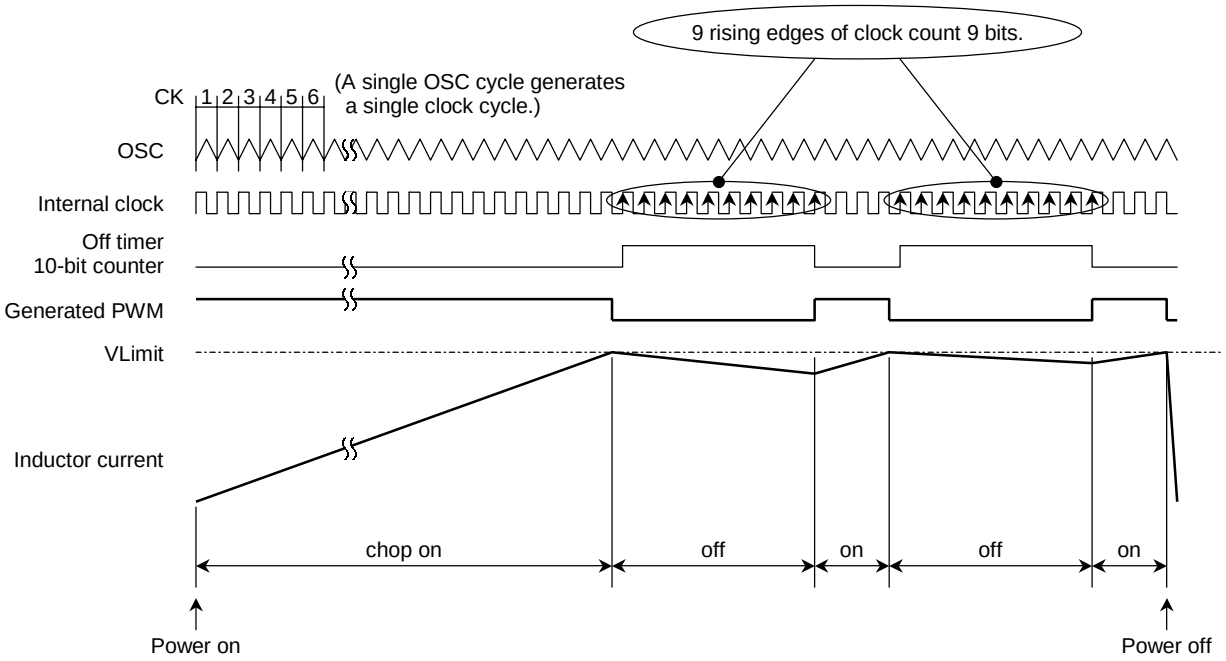
In an actual application, however, the required capacitance may slightly differ from the theoretical value due to board pin capacitance and other factors. It is, therefore, recommended to determine the value of C_{OSC} experimentally.

- Constant-current bridge block (H-SW E, F): Description of PWM constant-current chopping

  Turning on the power (Chop on) causes current to flow into the load inductor. Once the voltage (VRF) generated with the external current detection resistor reaches the comparator reference voltage, Vlimit (current limit), the comparator starts operating (Chop off). After the output Hi-side transistor is turned off, counting for the chop-off time starts at the next rising edge of the internal clock, producing a chop-off time of clock cycles for nine bits (reset at the rising edge for the 10th bit).

  This chop-off time control creates a PWM signal to turn the output transistor on and off.

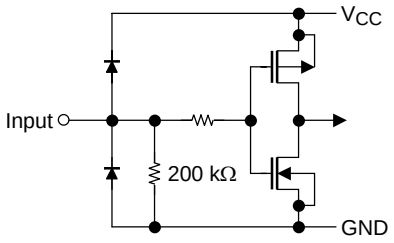
Conceptual diagram for PWM chopping operation



(The inductor current (I_O peak) is limited by the value obtained from the expression I_O = Vlimt/RNF.)

- Others

  Each input pin (CK, DA, LD, PWM-A, B, C, D, E, F, and STBY) has a built-in pull-down resistor (approx. 200 kΩ)



Serial Data Specifications:

Register modes

D8	D7	D6	D5	D4	D3	D2	D1	D0	Register	Remarks
0	0	0	mod2	mod1	p2a	p2b	p1a	p1b	0	ChA, ChB setting
0	0	1	mod4	mod3	p4a	p4b	p3a	p3b	1	ChC, ChD setting
0	1	0	mod6	mod5	p6a	p6b	p5a	p5b	2	ChE, ChF setting
0	1	1	pwm6	pwm5	pwm4	pwm3	pwm2	pwm1	3	PWM mode setting
1	0	0	DA5	DA4	DA3	DA2	DA1	DA0	4	DAC1 setting
1	0	1	DA5	DA4	DA3	DA2	DA1	DA0	5	DAC2 setting
1	1	1	0	0	0	0	0	0	—	Reset

Driver function table

modX = 0 pwmx = 0

pxa	pxb	PWMx	OUTxA	OUTxB	Operating Mode
L	L	X	Z	Z	STOP
L	H	L	L	L	Short brake
L	H	H	L	H	CCW
H	L	L	L	L	Short brake
H	L	H	H	L	CW
H	H	X	L	L	Short brake

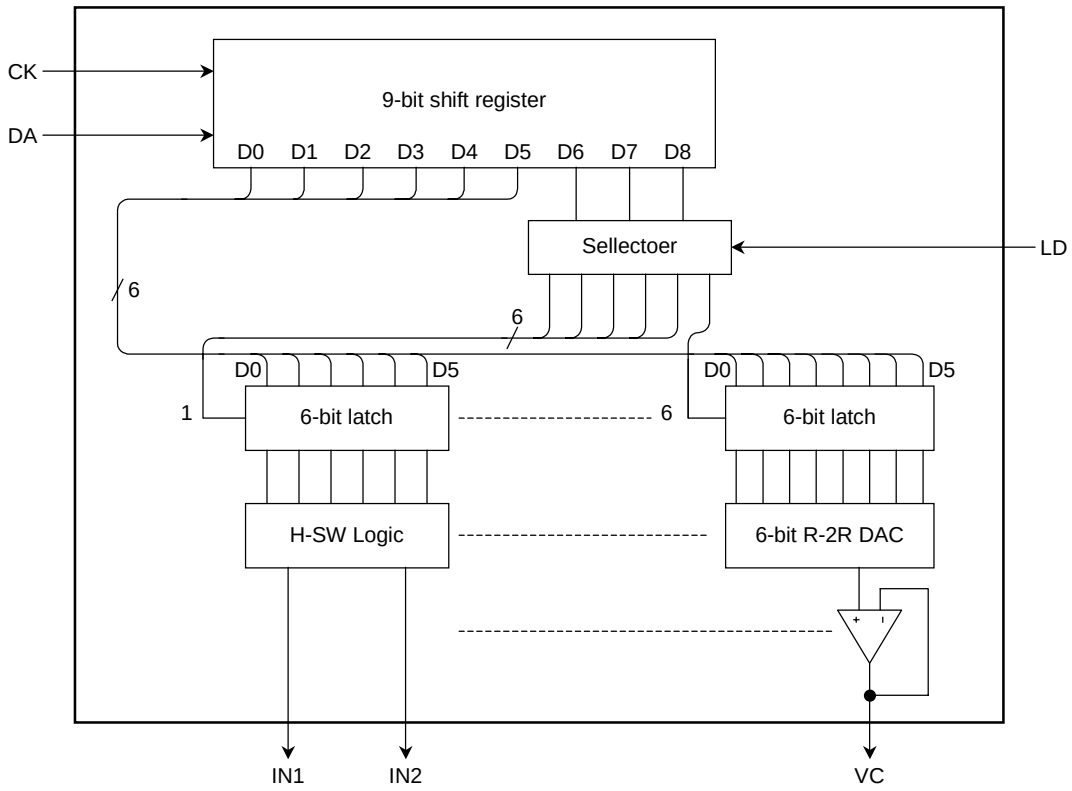
modX = 0 pwmx = 1

pxa	pxb	PWMx	OUTxA	OUTxB	Operating Mode
L	L	X	Z	Z	STOP
L	H	L	L	H	CCW
L	H	H	L	L	Short brake
H	L	L	H	L	CW
H	L	H	L	L	Short brake
H	H	X	L	L	Short brake

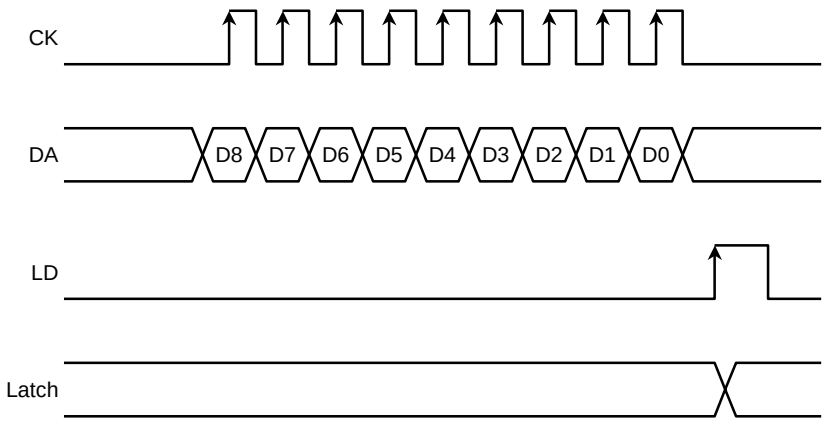
modX = 1 pwmx = X

pxa	pxb	PWMx	OUTxA	OUTxB	Operating Mode
L	X	X	Z	Z	STOP
H	L	L	H	L	CW
H	L	H	L	H	CCW
H	H	X	L	L	Short brake

Serial Decoder Block Diagram



Example Timing Chart



The 9-bit serial data, input to the DA pin, is detected on the rising edge of CK, and then serially stored into the 9-bit register.

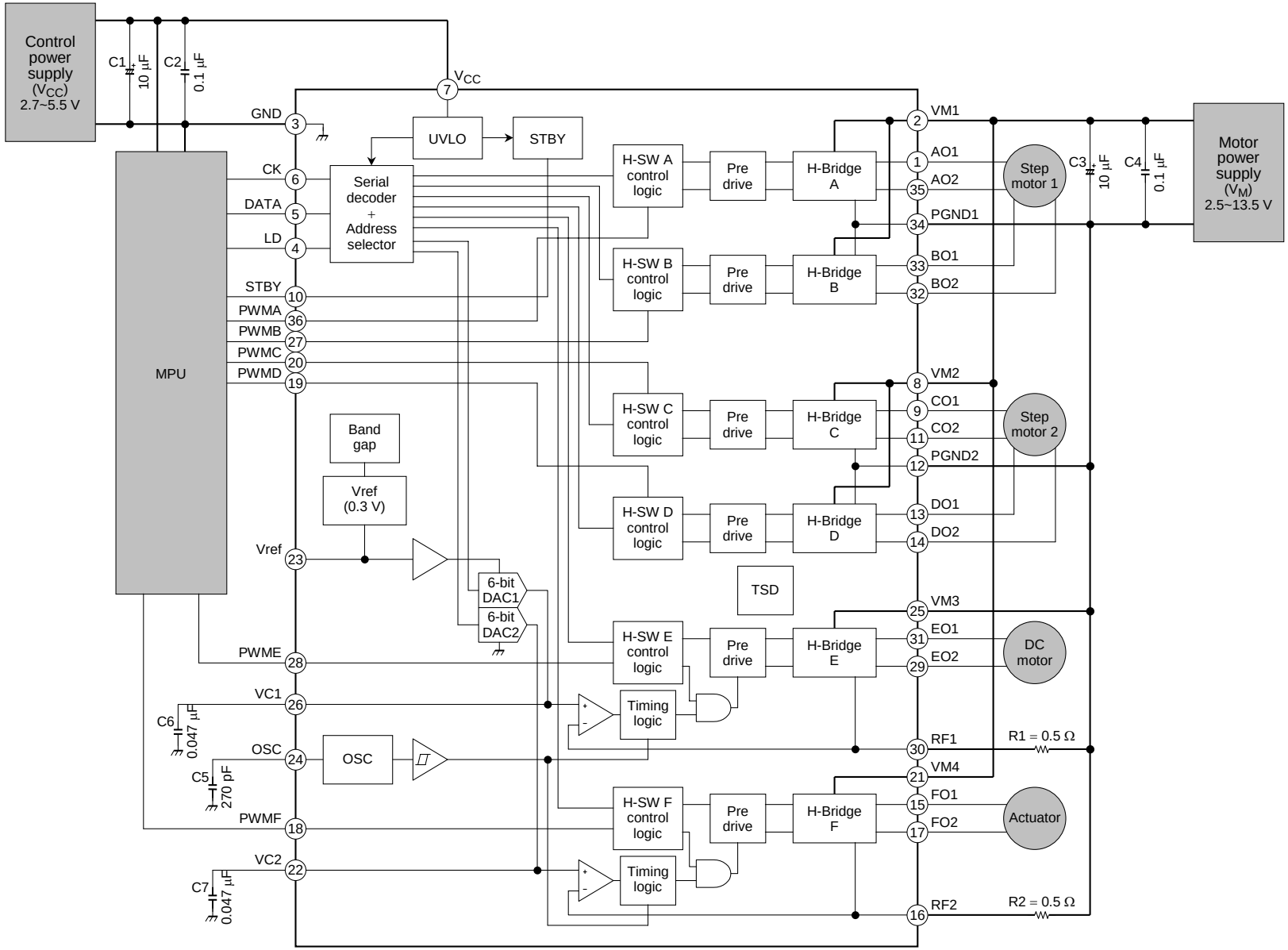
(1) The three bits in D8 to D6 select the register.
(2) The six bits in D5 to D0 specify the H-SW control mode or DAC output value.
(3) Data is output from the latch on the rising edge of the signal input to the LD pin.

Note: Driving the standby pin (pin 10) low resets the internal register.
The internal register is also reset in the default status upon power-on.

Electrical Characteristics (V_{CC} = 3 V, V_M = 5 V, and Ta = 25°C unless otherwise specified)

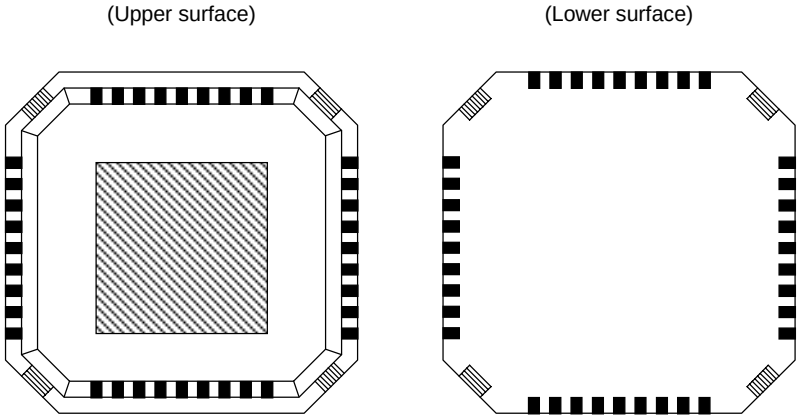
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Supply current		I_{CC}	All 6 channels in CW mode	—	3	5	mA
		$I_{CC\ (STB)}$	Standby mode	—	—	10	μA
		$I_{M\ (STB)}$		—	—	1	
Serial/standby input	Input voltage	V_{INH}		V_{CC} × 1/2	—	V_{CC} + 0.2	V
		V_{INL}		−0.2	—	0.4	
	Input current	I_{INH}	V_{IH} = 3 V	10	15	20	μA
		I_{INL}	V_{IL} = 0 V	—	—	1	
PWM input	Input voltage	V_{INSH}		2	—	V_{CC} + 0.2	V
		$V_{IN\ (HYS)}$	(Design value)	—	0.2	—	
		V_{INSL}		−0.2	—	0.8	
	Input current	I_{INSH}	V_{IH} = 3 V	10	15	20	μA
		I_{INSL}	V_{IL} = 0 V	—	—	1	
Output saturation voltage		$V_{sat\ (U + L)}$	I_O = 0.2 A	—	0.3		V
			I_O = 0.6 A	—	0.9		
Output leakage current		$I_{L\ (U)}$	V_M = 15 V	—	—	1	μA
		$I_{L\ (L)}$		—	—	1	
Output diode forward voltage		$V_{F\ (U)}$	I_F = 0.6 A (Design value)	—	1	—	V
		$V_{F\ (L)}$		—	1	—	
Internal reference voltage		V_{ref}		0.28	0.3	0.32	V
Offset voltage for constant-current detection comparator		Comp ofs	RRF = 1 Ω, V_C = 0.1 V (Design value)	−5	—	5	mV
Reference oscillation frequency		f_{OSC}	Cosc = 220 pF	430	530	630	kHZ
DAC	Nonlinearity error	LB		−3	—	3	LSB
	Differential linearity error	DLB		−2	—	2	
	Output voltage range	DR		0	—	2.7	V
Thermal shutdown circuit operating temperature		TSD	(Design value)	—	170	—	°C
Hysteresis temperature width for recovery from thermal shutdown		ΔTSD		—	20	—	

Example Application Circuit



Requests Concerning Use of QON

Outline Drawing of Package



When using QON, please take into account the following items.

Caution

(1) Do not carry out soldering on the island section in the four corners of the package (the section shown on the lower surface drawing with diagonal lines) with the aim of increasing mechanical strength.

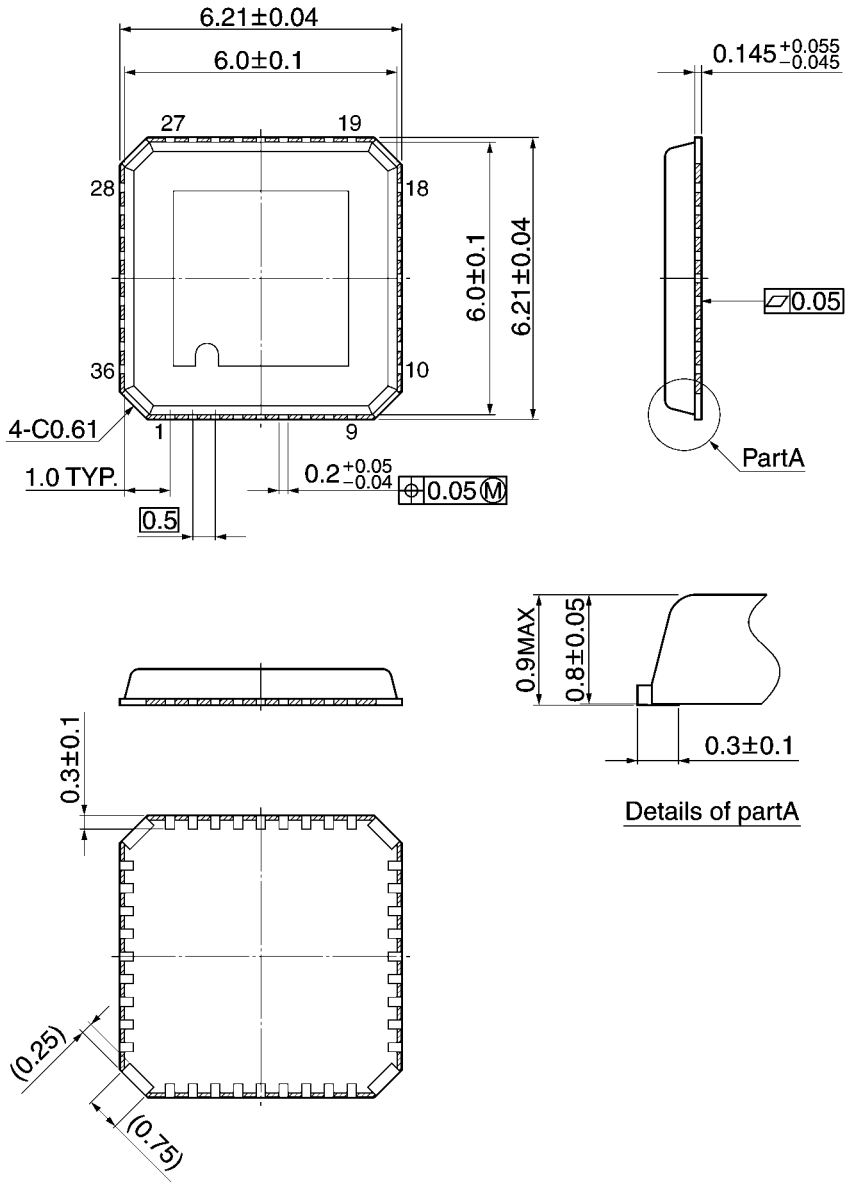
(2) The island section exposed on the package surface (the section shown on the upper surface drawing with diagonal lines) must be used as (Note) below while electrically insulated from outside.

Note: Ensure that the island section (the section shown on the lower surface drawing with diagonal lines) does not come into contact with solder from through-holes on the board layout.

- When mounting or soldering, take care to ensure that neither static electricity nor electrical overstress is applied to the IC (measures to prevent anti-static, leaks, etc.).
- When incorporating into a set, adopt a set design that does not apply voltage directly to the island section.

Package Dimensions

QON36-P-0606-0.50 Unit: mm



Note 1) The solder plating portion in four corners of tne package shall not be treated as an external terminal.

Note 2) Don`t carry out soldering to four corners of the package.

Note 3) area : Resin surface

Weight: 0.08 g (typ.)

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