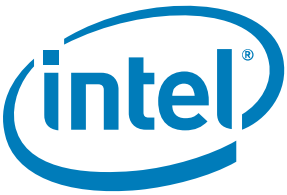
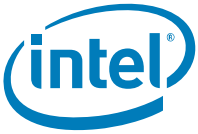


Intel® 631xESB/632xESB I/O Controller Hub

Datasheet

May 2006

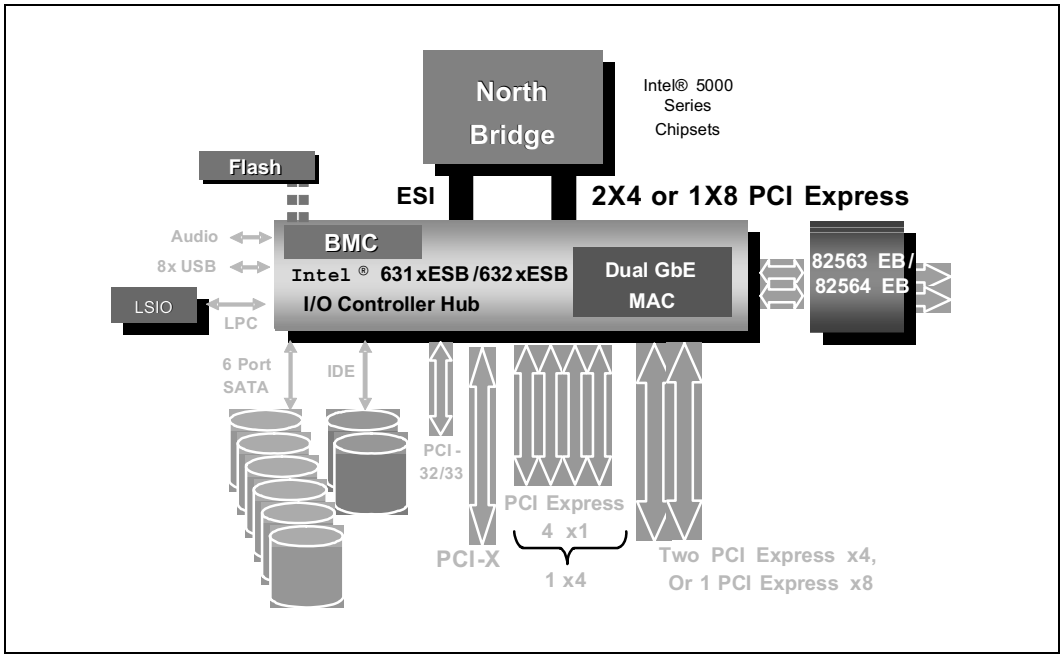
Document Number: 313082-001



Intel® 631xESB/632xESB I/O Controller Hub Features

- Interfaces to Memory Controller Hub
  - Enterprise South Bridge Interface: 1 GB/s each direction, full duplex, transparent to software
  - x4/x8 PCI Express* interface
- PCI Express Root Port
  - 4 PCI Express root ports
  - Fully PCI Express 1.0a compliant
  - Can be statically configured as 4x1, or 1x4
  - Support for full 2.5 Gb/s bandwidth in each direction
  - Module-based Hot-Plug supported
- PCI Express Downstream Ports
  - Two x4 or one x8 PCI Express 1.0a compliant ports
  - Hot-Plug support for Evolutionary (card-edge) form factor
- PCI Bus Interface
  - Supports PCI Rev 2.3 Specification at 33 MHz
  - Seven available PCI REQ/GNT pairs
  - Support for 64-bit addressing on PCI using DAC protocol
- PCI/PCI-X* Bus Interface
  - Configurable as 33- or 66- MHz PCI, 66-, 100-, or 133-MHz PCI-X
  - Supports Standard Hot-Plug Controller 1.0 Specification
- Integrated Serial ATA Host Controller
  - Independent DMA operation on six ports
  - Data transfer rates up to 3.0 Gb/s (300 MB/s)
  - Tri-state modes to enable swap bay
- Integrated IDE Controller
  - Independent timing of up to two drives
  - Ultra ATA/100/66/33, BMIDE and PIO modes
- USB 2.0
  - Includes four UHCI Host Controllers, increasing the number of external ports to eight
  - Includes one EHCI Host Controller that supports all eight ports
  - Includes one USB 2.0 High-speed Debug Port
  - Supports wake-up from sleeping states S1-S5
  - Supports legacy Keyboard/Mouse software
- High Definition Audio Interface
  - Independent Bus Master logic for eight general purpose streams: four input and four output
  - Support three external Codecs
  - Supports variable length stream slots
  - Supports 8 channel, 24-bit samples, 192 kHz sample rate output
  - Supports an array of up to six microphone inputs
  - Supports memory-based command/response transport
  - Provides cadence for non-48 kHz sampling output
- AC-Link for Audio and Telephony CODECs
  - Support for three AC '97 2.3 codecs.
  - Independent Bus Master logic for 8 channels (PCM In/Out, PCM 2 In, Mic 1 Input, Mic 2 Input, Modem In/Out, S/PDIF Out)
  - Support for up to six channels of PCM audio output (full AC3 decode)
- Timers Based on 82C54
  - System timer, Refresh request, speaker tone output
- Power Management Logic
  - ACPI 2.0 compliant
  - ACPI-defined power states
  - ACPI Power Management Timer
  - PME# support
  - SMI# generation
  - All registers readable/restorable for proper resume from 0 V suspend states
- External Glue Integration
  - Integrated pull-up, pull-down and series termination resistors on IDE, processor interface
  - Integrated pull-down and series resistors on USB
- Enhanced DMA Controller
  - Two cascaded 8237 DMA controllers
  - Supports LPC DMA
- Integrated dual-gigabit Media Access Controller
  - Compliant with the 1000 Mb/sec Ethernet/802.3z specification
  - Multi-speed operation: 10/100/1000Mb/s
  - Serial FLASH interface and SPI EEPROM interface. No support for uWire EEPROM.
  - SERDES interface for System interconnect
- Kumeran interface to external Gigabit Ethernet PHY
  - Dual Kumeran interface to two external 1000BASE-T PHYs
  - 4 pin per port interface (dual port)
  - In band MDIO for faster accesses
  - Remote PHY debug and diagnostics
- Integrated Board Management Controller
  - Full BMC implementation, meaning a standalone microcontroller with independent I/Os and memory
  - Expansion bus for use with external FLASH device, SRAM and SDRAM
  - 256 Kbytes of internal SRAM
  - Support for RMCP+
  - Cryptographic module, supporting AES and RC4 encryption algorithms and SHA1 and MD5 authentication algorithms
- External Board Management Controller Support
  - Pass Through and Super Pass Through capable via a TCO port
  - TCO port supports SMBus, Fast Management Link (FML), and I^2C commands for passing traffic
  - Manageability Fail-Over
  - IDE re-direction
  - Serial over LAN (SoL)
  - RMCP+ support

Intel® 631xESB/632xESB I/O Controller Hub Diagram



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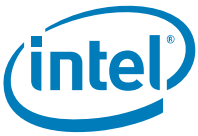
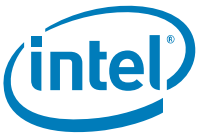
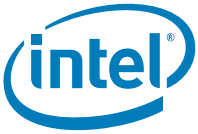
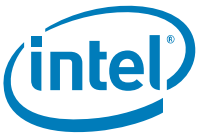


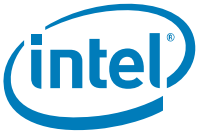


Figures

Tables







Revision History

Document Number	Revision Number	Description	Date
313082	-001	• Initial release of the document.	May 2006

§§

1 Introduction

1.1 About This Document

This specification is intended for Original Equipment Manufacturers designing and building Intel® 631xESB/632xESB I/O Controller Hub-based products. This manual assumes a working knowledge of the vocabulary and principles of PCI Express*, USB, IDE, AHCI, SATA, SMBus, PCI, PCI-X*, ACPI, ESI, JTAG, and LPC. Although some details of these features are described within this specification, refer to the individual industry specifications listed in Table 1-1 for complete details.

Table 1-1. Industry Specifications and Related Documents (Sheet 1 of 2)

Document	Location
Advanced Configuration and Power Interface, Version 2.0 (ACPI)	http://www.acpi.info/spec.htm
AES CBC-mode Cipher Algorithm, RFC 2451	http://www.ietf.org/rfc/rfc2451.txt?number=2451
Alert Standard Format Specification, Version 2.0	http://www.dmtf.org/standards/standard_alert.php
AT Attachment - 6 with Packet Interface (ATA/ATAPI - 6)	http://T13.org (T13 1410D)
Audio Codec '97 Component Specification, Version 2.3 (AC'97)	http://www.intel.com/labs/media/audio/index.htm
Enhanced Host Controller Interface Specification for Universal Serial Bus, Revision 1.0 (EHCI)	http://developer.intel.com/technology/usb/ehcispec.htm
HMAC Key-Hashing for Message Authentication, RFC 2104	http://www.ietf.org/rfc/rfc2104.txt?number=2104
IA-PC HPET (High Precision Event Timers) Specification, Revision 0.98a	http://www.intel.com/labs/platcomp/hpet/hpetspec.htm
IEEE 802.3 Fast Ethernet	http://standards.ieee.org
IEEE Standard Test Access Port and Boundary Scan Architecture 1149.1 Specifications	http://standards.ieee.org/reading/ieee/std_public/description/testtech/1149.1-1990_desc.html
Intel® 631xESB/632xESB I/O Controller Hub EDS Specification Update	http://developer.intel.com
IPMI v1.5 Specification	http://www.intel.com/design/servers/ipmi/spec.htm
Low Pin Count Interface Specification, Revision 1.1 (LPC)	http://developer.intel.com/design/chipsets/industry/lpc.htm
MD5 Message Digest algorithm, RFC 1321	http://www.ietf.org/rfc/rfc1321.txt?number=1321
PCI Express* Base Specification, Revision 1.0a	http://www.pcisig.com/specifications
PCI Local Bus Specification, Revision 2.3 (PCI)	http://www.pcisig.com/specifications
PCI Power Management Specification, Revision 1.1	http://www.pcisig.com/specifications
PCI Standard Hot-Plug Controller Specification Rev 1.0	http://www.pcisig.com/specifications
PCI-X Electrical and Mechanical Addendum to the PCI Base Specification, Revision 2.0a	http://www.pcisig.com/specifications
PCI-X Protocol Addendum to the PCI Base Specification, Revision 2.0a	http://www.pcisig.com/specifications
PCI-X Protocol Addendum to the PCI Local Bus Specification Revision 2.0	http://www.pcisig.com/specifications

Table 1-1. Industry Specifications and Related Documents (Sheet 2 of 2)

Document	Location
PCI-X* Protocol Addendum to the PCI Local Bus Specification, Revision 2.0a	http://www.pcisig.com/specifications
Serial ATA Advanced Host Controller Interface (AHCI) Specification, Revision 1.0	http://www.serialata.org
Serial ATA 1.0a Specification	http://www.serialata.org
Serial ATA II: Extensions to Serial ATA 1.0, Revision 1.0	http://www.serialata.org
SHA1 Secure Hash Algorithm RFC 3174	http://www.ietf.org/mail-archive/ietf-announce/Current/msg14881.html
System Management Bus Specification, Version 2.0 (SMBus)	http://www.smbus.org/specs/
Universal Serial Bus Revision 2.0 Specification (USB)	http://www.usb.org
Universal Host Controller Interface, Revision 1.1 (UHCI)	http://developer.intel.com/design/USB/UHCI11D.htm
Wired for Management Baseline Version 2.0 (WfM)	http://www.intel.com/labs/manage/wfm/wfmspecs.htm

The following is a chapter-by-chapter description of the information in this document.

Chapter 1, “Introduction”
Introduces the Intel® 631xESB/632xESB I/O Controller Hub, provides information on manual organization, and gives a general overview of the component.

Chapter 2, “Signal Descriptions”
Provides a block diagram of the Intel® 631xESB/632xESB I/O Controller Hub and a detailed description of each signal. Signals are arranged according to interface and details are provided as to the drive characteristics (Input/Output, Open Drain, and so on) of all signals.

Chapter 3, “Intel® 631xESB/632xESB I/O Controller Hub and System Clock Domains”
Provides a list of each clock domain associated with the Intel® 631xESB/632xESB I/O Controller Hub in an Intel® 631xESB/632xESB I/O Controller Hub-based system.

Chapter 4, “Intel® 631xESB/632xESB I/O Controller Hub Pin States”
Provides a complete list of signals, their associated power well, their logic level in each suspend state, and their logic level before and after reset.

Chapter 5, “Functional Description”
Provides a detailed description of the functions in the Intel® 631xESB/632xESB I/O Controller Hub. All PCI buses, devices and functions in this manual are abbreviated using the following nomenclature; Bus:Device:Function. This manual abbreviates buses as B0 and B1, devices as D8, D27, D28, D29, D30 and D31 and functions as F0, F1, F2, F3, F4, F5, F6 and F7. For example Device 31 Function 0 is abbreviated as D31:F0, Bus n Device 0Function 0 is abbreviated as Bn:D0:F0.

Chapter 6, “Electrical Characteristics”
Provides all AC and DC characteristics including detailed timing diagrams.

Chapter 7, “Component Ballout”
Provides tables with each signal and its ball assignment in the 641-mBGA package, as well as diagrams of the ballout grid.

Chapter 8, “Signal Lists”
Provides drawings of the physical dimensions and characteristics of the 641-mBGA package.

Chapter 9, “Mechanical Specifications”
Provides drawings of the physical dimensions and characteristics of the 641-mBGA package.

Chapter 10, “Testability”
Provides detail about the implementation of test modes provided in the Intel® 631xESB/632xESB I/O Controller Hub, and is the final chapter of Volume 1.

Chapter 11, “Register and Memory Mapping”
Provides an overview of the registers, fixed I/O ranges, variable I/O ranges, and memory ranges decoded by the Intel® 631xESB/632xESB I/O Controller Hub.

Chapter 12, “Chipset Configuration Registers”
Provides a detailed description of all registers and base functionality related to chipset configuration and not a specific interface (such as LPC, PCI, or PCI Express). It contains the root complex register block, which describes the behavior of the upstream internal link.

Chapter 13, “PCI Express* Bridge, Switch, and Endpoints Registers (Bm:D0:F0/F1/F3, Bp:D0:F0, Bp:D1:F0, Bp:D2:F0)”
Provides a detailed description of all registers that reside in the PCI Express-to-PCI-X bridge controller. This controller resides at Device 0, Function 0 (D0:F0). This includes the IOxAPIC (D0:F1), PCI Express upstream port (D0:F3), and 3 x4 PCI Express downstream ports (BP:D0/D1/D2:F0).

Chapter 14, “Intel® High Definition Audio Controller Registers (D27:F0)”
Provides a detailed description of all registers that reside in the High Definition Audio controller. This controller resides at Device 27, Function 0 (D27:F0).

Chapter 15, “PCI Express* Configuration Registers”
Provides a detailed description of all registers that reside in the PCI Express controller. This controller resides at Device 28, Functions 0 to 3 (D30:F0/F1/F2/F3).

Chapter 16, “UHCI Controllers Registers”
Provides a detailed description of all registers that reside in the four UHCI host controllers. These controllers reside at Device 29, Functions 0, 1, 2, and 3 (D29:F0/F1/F2/F3).

Chapter 17, “EHCI Controller Registers (D29:F7)”
Provides a detailed description of all registers that reside in the EHCI host controller. This controller resides at Device 29, Function 7 (D29:F7).

Chapter 18, “PCI-to-PCI Bridge Registers (D30:F0)”
Provides a detailed description of all registers that reside in the PCI-to-PCI bridge. This bridge resides at Device 30, Function 0 (D30:F0).

Chapter 19, “AC’97 Audio Controller Registers (D30:F2)”
Provides a detailed description of all registers that reside in the audio controller. This controller resides at Device 30, Function 2 (D30:F2). Note that this section of the EDS does not include the native audio mixer registers. Accesses to the mixer registers are forwarded over the AC-link to the codec where the registers reside.

Chapter 20, “AC’97 Modem Controller Registers (D30:F3)”
Provides a detailed description of all registers that reside in the modem controller. This controller resides at Device 30, Function 3 (D30:F3). Note that this section of the EDS does not include the modem mixer registers. Accesses to the mixer registers are forwarded over the AC-link to the codec where the registers reside.

Chapter 21, “LPC Interface Bridge Registers (D31:F0)”
Provides a detailed description of all registers that reside in the LPC bridge. This bridge resides at Device 31, Function 0 (D31:F0). This function contains registers for many different units within the Intel® 631xESB/632xESB I/O Controller Hub including DMA, Timers, Interrupts, Processor Interface, GPIO, Power Management, System Management, and RTC.

Chapter 22, “IDE Controller Registers (D31:F1)”
Provides a detailed description of all registers that reside in the IDE controller. This controller resides at Device 31, Function 1 (D31:F1).

Chapter 23, “SATA Controller Registers (D31:F2)”
Provides a detailed description of all registers that reside in the SATA controller. This controller resides at Device 31, Function 2 (D31:F2).

Chapter 24, “SMBus Controller Registers (D31:F3)”
Provides a detailed description of all registers that reside in the SMBus controller. This controller resides at Device 31, Function 3 (D31:F3).

Chapter 25, “LAN Controller and BMC Registers (Bn:F0/F1/F2/F3/F4/F5/F7)”
Provides a detailed description of all registers that reside in the Intel® 631xESB/632xESB I/O Controller Hub’s integrated LAN controller. The integrated LAN controller resides on the Intel® 631xESB/632xESB I/O Controller Hub’s external PCI bus (typically Bus 1) at Device 0, Function 0 (Bn:D0:F0).

Chapter 26, “High-Precision Event Timer Registers”
Provides a detailed description of all registers that reside in the multimedia timer memory mapped register space.

1.2 Overview

The Intel® 631xESB/632xESB I/O Controller Hub component integrates bridge functionality for PCI Express, PCI-X, conventional PCI, LPC, USB, SATA, IDE and SMBus, and dual-Gigabit ethernet MAC components as well as numerous board management functions. It provides for all system I/O, allowing for simpler system board architectures and smaller board areas than if discrete components were used.

Thus, the Intel® 631xESB/632xESB I/O Controller Hub provides extensive I/O support. Functions and capabilities include:

- Enterprise South Bridge Interface (ESI) and PCI Express X8 upstream ports to Memory Controller Hub (MCH)
- *PCI Express* Specification, Revision 1.0a*-compliant
- *PCI Protocol Addendum* and *PCI Electrical and Mechanical Addendum to the PCI Local Bus Specification, Revision 2.0a*-compliant
- *PCI Local Bus Specification, Revision 2.3*-compliant with support for 33 MHz PCI operations (supports up to seven Req/Gnt pairs)
- ACPI power management logic support
- Enhanced DMA controller, interrupt controller, and timer functions
- Integrated serial ATA host controller with independent DMA operation on six ports and AHCI support
- Integrated IDE controller supports Ultra ATA100/66/33
- USB host interface with support for eight USB ports; four UHCI host controllers; one EHCI high-speed USB 2.0 Host controller

- Dual Gigabit MAC with Kumeran interface to dual-PHY component
- PICMG-compliant Serdes backplane Gigabit Ethernet support
- Integrated Board Management Controller with basic ROM firmware, expandability through external flash and RAM memories
- *System Management Bus (SMBus) Specification, Version 2.0*-compliant with additional support for I^2C* devices
- Audio interface (AC'97 and Intel® High Definition Audio)
- Low Pin Count (LPC) interface
- Firmware Hub (FWH) interface support

The Intel® 631xESB/632xESB I/O Controller Hub incorporates a variety of PCI functions that are divided into several logical devices (Bm:D0, B0:D28, B0:D29, B0:D30, B0:D31, Bn:D0, Bp:D0, Bp:D1 and Bp:D3). Bm:D0 is the PCI Express upstream port-to-PCI-X bridge, D28 contains the PCI Express root ports, D30 is the ESI-to-PCI bridge, D31 contains the PCI-to-LPC bridge, IDE controller, SATA controller, SMBus controller and the AC '97 Audio and Modem controller functions, and D29 contains the four USB UHCI controllers and one USB EHCI controller. Bn:D0 is the integrated LAN controller and MACs. Bp:D0, Bp:D1 and Bp:D3 are PECI express downstream ports.

Table 1-2. PCI Devices and Functions (Sheet 1 of 2)

Bus:Device:Function	Function Description
Bus M:Device 0:Function 0	PCI Express* upstream port
Bus M:Device 0:Function 1	I/OxAPIC controller
Bus M:Device 0:Function 3	PCI Express-to-PCI-X* Bridge
Bus P:Device 0:Function 0	PCI Express downstream port 1
Bus P:Device 1:Function 0	PCI Express downstream port 2
Bus P:Device 2:Function 0	PCI Express downstream port 3
Bus 0:Device 30:Function 0	PCI-to-PCI Bridge
Bus 0:Device 30:Function 2	AC '97 Audio Controller
Bus 0:Device 30:Function 3	AC '97 Modem Controller
Bus 0:Device 31:Function 0	LPC Controller[1]
Bus 0:Device 31:Function 1	IDE Controller
Bus 0:Device 31:Function 2	SATA Controller
Bus 0:Device 31:Function 3	SMBus Controller
Bus 0:Device 29:Function 0	USB UHCI Controller #1
Bus 0:Device 29:Function 1	USB UHCI Controller #2
Bus 0:Device 29:Function 2	USB UHCI Controller #3
Bus 0:Device 29:Function 3	USB UHCI Controller #4
Bus 0:Device 29:Function 7	USB 2.0 EHCI Controller
Bus 0:Device 28:Function 0	PCI Express Port 1
Bus 0:Device 28:Function 1	PCI Express Port 2
Bus 0:Device 28:Function 2	PCI Express Port 3
Bus 0:Device 28:Function 3	PCI Express Port 4
Bus 0:Device 27:Function 0	High Definition Audio Controller

Table 1-2. PCI Devices and Functions (Sheet 2 of 2)

Bus:Device:Function	Function Description
Bus n:Device 0:Function 0	LAN 0/LAN 1 Controller
Bus n:Device 0:Function 1	LAN 0/LAN 1 Controller
Bus n:Device 0:Function 2	IDE Redirection Controller
Bus n:Device 0:Function 3	Serial Port Redirection Controller
Bus n:Device 0:Function 4	IPMI/KCS0
Bus n:Device 0:Function 5	UHCI Redirection Controller
Bus n:Device 0:Function 7	BT Controller

Note: The PCI-to-LPC bridge contains registers that control LPC, Power Management, System Management, GPIO, Processor Interface, RTC, Interrupts, Timers, and DMA.

The following sub-sections provide an overview of the Intel® 631xESB/632xESB I/O Controller Hub's capabilities.

Enterprise South Bridge Interface (ESI)

Enterprise South Bridge Interface (ESI) is the chip-to-chip connection between the Memory Controller Hub (MCH) and I/O Controller Hub functions of the Intel® 631xESB/632xESB I/O Controller Hub. Maximum realized bandwidth on this interface is 1 GB/s in each direction simultaneously, for an aggregate of 2 GB/s. Base functionality is completely software-transparent, permitting current and legacy software to operate normally.

PCI Express* Interfaces

The Intel® 631xESB/632xESB I/O Controller Hub provides 4 PCI Express Root Ports which are compliant to the *PCI Express* Base Specification Revision 1.0a*. The PCI Express Root Ports can be statically configured as four x1 ports or ganged together to form one x4 port. Each Root Port supports 250 MB/s bandwidth in each direction (500 MB/s concurrent).

An additional PCI Express interface is provided for connection to the Memory Controller Hub (MCH). Maximum realized bandwidth on this interface is 2 GB/s in each direction simultaneously, for an aggregate of 4 GB/s. This PCI Express interface is also compliant with the *PCI Express* Base Specification Revision 1.0a*, and supports x4 and x8 widths.

Intel® 631xESB/632xESB I/O Controller Hub also implement two x4 PCI Express Downstream Ports, maximum realized bandwidth on this interface is 1 GB/s in each direction simultaneously, for an aggregate of 2 GB/s. These two ports can also be configured as one x8 PCI Express port. This PCI Express interface is also compliant with the *PCI Express* Base Specification Revision 1.0a*.

PCI-X* Bus Interface

The Intel® 631xESB/632xESB I/O Controller Hub provides a PCI-X* Bus interface which can be independently configured as either a PCI Bus or a PCI-X Bus. This interface supports conventional PCI and PCI-X Mode 1. PCI Bus extensions are also supported; these include 64-bit addressing outbound with the capability to assert DAC, and full 64-bit addressing inbound. The inbound packet size is based on cache line size of the platform.

The PCI-X interface on the Intel® 631xESB/632xESB I/O Controller Hub is compliant with the *PCI-X Addendum to the PCI Local Bus Specification Revision 1.*0b as well as the *PCI-X Electrical and Mechanical Addendum to the PCI Local Bus Specification Revision 2.0a* and the *PCI-X Protocol Addendum to the PCI Local Bus Specification Revision 2.0a*.

For conventional PCI Mode, the Intel® 631xESB/632xESB I/O Controller Hub supports PCI bus frequencies of 33 MHz and 66 MHz. For PCI-X Mode 1, the Intel® 631xESB/632xESB I/O Controller Hub supports PCI bus frequencies of 66 MHz, 100 MHz, and 133 MHz. For this interface, four PCI-X bus slots are supported at 66 MHz, two slots are supported at 100 MHz, and one slot is supported at 133 MHZ.

PCI Bus Interface

The Intel® 631xESB/632xESB I/O Controller Hub PCI Local Bus interface provides a 33 MHz, Revision 2.3 implementation. All PCI signals are 5 V tolerant, except PCICLK PME#. The Intel® 631xESB/632xESB I/O Controller Hub integrates a PCI arbiter that supports up to seven external PCI Bus Masters in addition to the internal Intel® 631xESB/632xESB I/O Controller Hub requests. This allows for combinations of up to seven PCI down devices and PCI slots on this interface.

PCI Standard Hot-Plug Controller

The Intel® 631xESB/632xESB I/O Controller Hub Hot-Plug controller is compliant with *PCI Standard-Hot-Plug Controller and Subsystem Specification, Revision 1.0* and allows PCI card removal, replacement, and addition without powering down the system. The Intel® 631xESB/632xESB I/O Controller Hub Hot-Plug controller supports three to six PCI slots through an input/output serial interface when operating in Serial Mode, and one to two slots through an input/output parallel interface when operating in Parallel Mode. The Intel® 631xESB/632xESB I/O Controller Hub can also operate in “one-slot-no-glue” Hot-Plug mode, which does not require and on-board logic for enabling and disabling the bus and clocks signals to the PCI/PCI-X Hot-Plug slots. The input serial interface is polling and is in continuous operation. The output serial interface is “demand” and acts only when requested. These serial interfaces run at about 8.25 MHz regardless of the speed of the PCI bus. In parallel mode, the Intel® 631xESB/632xESB I/O Controller Hub performs the serial to parallel conversion internally, so the serial interface cannot be observed. However, internally the Hot-Plug controller always operates in a serial mode.

Serial ATA (SATA) Controller

The Intel® 631xESB/632xESB I/O Controller Hub has an integrated SATA host controller that supports independent DMA operation on six ports and supports data transfer rates of up to 3.0 Gb/s (300 MB/s). The SATA controller contains two modes of operation – a legacy mode using I/O space, and an AHCI mode using memory space.

SATA and PATA can also be used in a combined function mode (where the SATA function is used with PATA). In this combined function mode, AHCI mode is not used. Software that uses legacy mode will not have AHCI capabilities.

IDE Interface (Bus Master Capability and Synchronous DMA Mode)

The IDE interface supports up to two IDE devices providing an interface for IDE hard disks and ATAPI devices. Each IDE device can have independent timings. The IDE interface supports PIO IDE transfers up to 16 MBytes/sec and Ultra DMA transfer rates of up to 133 MB/sec on reads and 88 MB/sec on write. It does not consume any ISA DMA resources. The IDE interface integrates 16x32-bit buffers for optimal transfers.

The Intel® 631xESB/632xESB I/O Controller Hub's IDE system contains a single, independent IDE signal channel that can be electrically isolated. There are integrated series resistors on the data and control lines (see Section 5.17 for details).

Low Pin Count (LPC) Interface

The Intel® 631xESB/632xESB I/O Controller Hub implements an LPC Interface as described in the LPC 1.1 specification. The Low Pin Count (LPC) bridge function of the Intel® 631xESB/632xESB I/O Controller Hub resides in PCI Device 31:Function 0. In addition to the LPC bridge interface function, D31:F0 contains other functional units including DMA, interrupt controllers, timers, power management, system management, GPIO, and RTC.

Note that in the current chipset platform, the Super I/O (SIO) component has migrated to the Low Pin Count (LPC) interface. Migration to the LPC interface allows for lower cost Super I/O designs.

Compatibility Modules (DMA Controller, Timer/Counters, Interrupt Controller)

The DMA controller incorporates the logic of two 82C37 DMA controllers, with seven independently programmable channels. Channels 0–3 are hardwired to 8-bit, count-by-byte transfers, and channels 5–7 are hardwired to 16-bit, count-by-word transfers. Any two of the seven DMA channels can be programmed to support fast Type-F transfers.

The Intel® 631xESB/632xESB I/O Controller Hub supports LPC DMA, which is similar to ISA DMA, through the Intel® 631xESB/632xESB I/O Controller Hub's DMA controller. LPC DMA is handled through the use of the LDRQ# lines from peripherals and special encoding on LAD[3:0] from the host. Single, Demand, Verify, and Increment modes are supported on the LPC interface. Channels 0–3 are 8-bit channels. Channels 5–7 are 16-bit channels. Channel 4 is reserved as a generic Bus Master request.

The timer/counter block contains three counters that are equivalent in function to those found in one 82C54 programmable interval timer. These three counters are combined to provide the system timer function, and speaker tone. The 14.31818 MHz oscillator input provides the clock source for these three counters.

The Intel® 631xESB/632xESB I/O Controller Hub provides an ISA-Compatible Programmable Interrupt Controller (PIC) that incorporates the functionality of two, 82C59 interrupt controllers. The two interrupt controllers are cascaded so that 14 external and two internal interrupts are possible. In addition, the Intel® 631xESB/632xESB I/O Controller Hub supports a serial interrupt scheme.

All of the registers in these modules can be read and restored. This is required to save and restore system state after power has been removed and restored to the platform.

Advanced Programmable Interrupt Controller (APIC)

In addition to the standard ISA compatible Programmable Interrupt controller (PIC) described in the previous section, the Intel® 631xESB/632xESB I/O Controller Hub incorporates two Advanced Programmable Interrupt Controllers (APICs).

Universal Serial Bus (USB) Controller

The Intel® 631xESB/632xESB I/O Controller Hub contains an Enhanced Host Controller Interface (EHCI) compliant host controller that supports USB high-speed signaling. High-speed USB 2.0 allows data transfers up to 480 Mb/s which is 40 times faster than full-speed USB. The Intel® 631xESB/632xESB I/O Controller Hub also contains four Universal Host Controller Interface (UHCI) controllers that support USB full-speed and low-speed signaling.

The Intel® 631xESB/632xESB I/O Controller Hub supports eight USB 2.0 ports. All eight ports are high-speed, full-speed, and low-speed capable. The Intel® 631xESB/632xESB I/O Controller Hub's port-routing logic determines whether a USB port is controlled by one of the UHCI controllers or by the EHCI controller. See Section 5.20 and Section 5.21 for details.

RTC

The Intel® 631xESB/632xESB I/O Controller Hub contains a Motorola MC146818A*-compatible real-time clock with 256 bytes of battery-backed RAM. The real-time clock performs two key functions: keeping track of the time of day and storing system data, even when the system is powered down. The RTC operates on a 32.768 KHz crystal and a separate 3 V lithium battery that provides up to seven years of protection.

The RTC also supports two lockable memory ranges. By setting bits in the configuration space, two 8-byte ranges can be locked to read and write accesses. This prevents unauthorized reading of passwords or other system security information.

The RTC also supports a date alarm that allows for scheduling a wake up event up to 30 days in advance, rather than just 24 hours in advance.

GPIO

Various general purpose inputs and outputs are provided for custom system design.

Enhanced Power Management

The Intel® 631xESB/632xESB I/O Controller Hub's power management functions include enhanced clock control, local and global monitoring support for 14 individual devices, and various low-power (suspend) states. A hardware-based thermal management circuit permits software-independent entrance to low-power states. The Intel® 631xESB/632xESB I/O Controller Hub contains full support for the *Advanced Configuration and Power Interface, Version 2.0*.

System Management Bus (SMBus 2.0)

The Intel® 631xESB/632xESB I/O Controller Hub contains several SMBus host interfaces that allow the processor to communicate with SMBus Slaves. These interfaces are compatible with most I^2C devices. Special I^2C commands are implemented.

The Intel® 631xESB/632xESB I/O Controller Hub's SMBus host controllers provide a mechanism for the processor to initiate communications with SMBus peripherals (Slaves). Also, the Intel® 631xESB/632xESB I/O Controller Hub supports Slave functionality, including the Host Notify protocol. Hence, the host controller supports eight command protocols of the SMBus interface (see System Management Bus (SMBus) Specification, Version 2.0): Quick Command, Send Byte, Receive Byte, Write Byte/Word, Read Byte/Word, Process Call, Block Read/Write, and Host Notify.

The Intel® 631xESB/632xESB I/O Controller Hub's SMBus also implements hardware-based Packet Error Checking for data robustness and the Address Resolution Protocol (ARP) to dynamically provide addresses to all SMBus devices.

Manageability

The Intel® 631xESB/632xESB I/O Controller Hub integrates several functions designed to manage the system and lower the total cost of ownership (TCO) of the system. These system management functions are designed to report errors, diagnose the system, and recover from system lockups without the aid of an external microcontroller.

- **TCO Timer.** The Intel® 631xESB/632xESB I/O Controller Hub's integrated programmable TCO timer is used to detect system locks. The first expiration of the timer generates an SMI# that the system can use to recover from a software lock. The second expiration of the timer causes a system reset to recover from a hardware lock.
- **Processor Present Indicator.** The Intel® 631xESB/632xESB I/O Controller Hub looks for the processor to fetch the first instruction after reset. If the processor does not fetch the first instruction, the Intel® 631xESB/632xESB I/O Controller Hub will reboot the system.
- **ECC Error Reporting.** When detecting an ECC error, the host controller has the ability to send one of several messages to the Intel® 631xESB/632xESB I/O Controller Hub. The host controller can instruct the Intel® 631xESB/632xESB I/O Controller Hub to generate either an SMI#, NMI, SERR#, or TCO interrupt.
- **Function Disable.** The Intel® 631xESB/632xESB I/O Controller Hub provides the ability to disable the following integrated functions: AC '97 Modem, AC '97 Audio, IDE, LAN, USB, LPC, High Definition Audio, SATA, or SMBus. Once disabled, these functions no longer decode I/O, memory, or PCI configuration space. Also, no interrupts or power management events are generated from the disable functions.
- **Intruder Detect.** The Intel® 631xESB/632xESB I/O Controller Hub provides an input signal (INTRUDER#) that can be attached to a switch that is activated by the system case being opened. The Intel® 631xESB/632xESB I/O Controller Hub can be programmed to generate an SMI# or TCO interrupt due to an active INTRUDER# signal.
- **SMBus 2.0.** The Intel® 631xESB/632xESB I/O Controller Hub integrates SMBus controllers that provide interfaces to manage peripherals (for example, serial presence detection (SPD), thermal sensors, and so on) with host notify capabilities.
- **BMC.** The Intel® 631xESB/632xESB I/O Controller Hub implements an ARC4 microcontroller and its memory subsystem for all manageability operations. The Baseboard Management Controller (BMC) system includes interfaces to most modules and main nodes in the Intel® 631xESB/632xESB I/O Controller Hub LAN. The BMC system is operated by firmware (embedded software) and is a flexible infrastructure for server management implementation.
  - — *Note*: External BMC support. Refer to the 82571/82572/ESB2 LAN System Management Bus Interface Application Note (AP-497) for more information.

AC'97 2.3 Controller

The Intel® 631xESB/632xESB I/O Controller Hub integrates an *Audio Codec '97 Component Specification, Version 2.3* controller that can be used to attach an audio codec (AC), a modem codec (MC), an audio/modem codec (AMC) or a combination of ACs and a single MC. The Intel® 631xESB/632xESB I/O Controller Hub supports up to six channels of PCM audio output (full AC3 decode). For a complete surround-sound experience, six-channel audio consists of: front left, front right, back left, back right, center, and subwoofer. Intel® 631xESB/632xESB I/O Controller Hub has expanded support for up to three audio codecs on the AC-link.

In addition, an AC '97 soft modem can be implemented with the use of a modem codec. Several system options exist when implementing AC '97. The Intel® 631xESB/632xESB I/O Controller Hub-integrated AC '97 controller allows up to three external codecs to be connected to the Intel® 631xESB/632xESB I/O Controller Hub. The system designer can provide AC '97 modem with a modem codec, or both audio and modem with up to two audio codecs with a modem codec.

Intel® High Definition Audio Controller

The High Definition Audio specification defines a digital interface that can be used to attach audio codecs (AC), The High Definition Audio specification defines the interface between the system logic and the audio codec, known as the High Definition Audio Digital Link. The High Definition Audio Digital Link and the AC-link share signal lines. Concurrent operation of AC '97 and High Definition Audio audio is not supported.

By using an audio codec, the High Definition Audio digital link allows for cost-effective, high-quality (24-bit output, 16-bit input), integrated audio on Intel's chipset-based platform. The Intel® 631xESB/632xESB I/O Controller Hub-integrated digital link allows three external codecs to be connected to the Intel® 631xESB/632xESB I/O Controller Hub.

The Intel® 631xESB/632xESB I/O Controller Hub expands the audio capability with support for up to six channels of PCM audio output (full AC3 decode). Six-channel audio consists of Front Left, Front Right, Back Left, Back Right, Center, and Subwoofer, for a complete surround-sound effect. On the input side the Intel® 631xESB/632xESB I/O Controller Hub adds support for an array of up to six microphones.

The Intel® 631xESB/632xESB I/O Controller Hub's High Definition Audio controller has an integrated PCI Express controller which provides support for three virtual channels that can be used to provide glitch-free audio to the system.

Dual-Gigabit Ethernet

The Intel® 631xESB/632xESB I/O Controller Hub contains two fully integrated Gigabit Ethernet Media Access Control (MAC). This provides a standard IEEE 802.3 Ethernet interface for 1000BASE-T, 1000BASE-X, 100BASE-TX, and 10BASE-T applications (802.3, 802.3z, 802.3u, and 802.3ab). Each port contains a Kumeran interface for connecting the Intel® 631xESB/632xESB I/O Controller Hub to the 82563EB/82564EB Dual/Single-PHY device. This interface supports 4 pins per port, incorporating the MII management interface into the data packets pins in order to ease routing requirements and device pin count. Intel® 631xESB/632xESB I/O Controller Hub also incorporates dual SerDes interfaces for direct connection to switch fabrics and fiber modules. Intel® 631xESB/632xESB I/O Controller Hub LAN supports the I/OAT Technology.

I/OAT is a platform feature that provides TCP acceleration using chipset and LAN HW offload features and optimized IA software to provide high-performance, low CPU utilization networking.

JTAG

The Intel® 631xESB/632xESB I/O Controller Hub has a JTAG (TAP) port compliant with the *IEEE Standard Test Access Port and Boundary Scan Architecture 1149.1 Specifications.* The TAP controller is accessed serially through five dedicated pins. This can be used for test and debug purposes. System board interconnects can be DC tested using the boundary scan logic in pads. See Chapter 10 for more on Intel® 631xESB/632xESB I/O Controller Hub testability.

1.3 Intel® 631xESB/632xESB I/O Controller Hub SKU Definition

Table 1-3. Intel® 631xESB/632xESB I/O Controller Hub SKUs

Note: Intel® 631xESB/632xESB I/O Controller Hub can be upgraded to full IAMT solution

Intel® 631xESB/632xESB I/O Controller Hub SKUs	Intel® 6321ESB I/O Controller Hub[1] (Enterprise)	Intel® 6311ESB I/O Controller Hub[1]
1st x4 PCI Express*	YES	YES
2nd x4 PCI Express	YES	YES
2 x1 PCI Express (1st pair)	YES	YES
2 x1 PCI Express (2nd pair)	YES	YES
PCI-X*	YES	YES
6 SATA	YES	YES
Dual GbE	YES	NO
Intel® I/O Acceleration Technology	YES	NO
SERDES	YES	NO

Notes:
1. Contact your local Intel Field Sales Representative for currently available Intel® 631xESB/632xESB I/O Controller Hub SKUs.
2. "Intel® I/O Acceleration Technology" replaces prior "Diamond Peak Technology" codename.
3. Intel® Active Server Manager includes the following features: IPMI2.0 compliance, Intel® Active Client Manager, FW SDK, and SMWG based interface.

§

2 Signal Descriptions

This chapter provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface.

The "#" symbol at the end of the signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at the high voltage level.

The following notations are used to describe the signal type:

I	**Input Pin**
O	**Output Pin**
OD	**Open Drain Output Pin**
I/O	**Bi-directional Input/Output Pin**
I/OD	**Bi-directional, open drain input/output signal.**
OC	**Open Collector Output Pin**
A-in	**Analog Input Pin**
A-out	**Analog Output Pin**
T/s	**Tri-State is a bi-directional, tri-state input/output pin.**

Figure 2-1. Intel® 631xESB/632xESB I/O Controller Hub Interface Signals Block Diagram (Sheet 1 of 3)

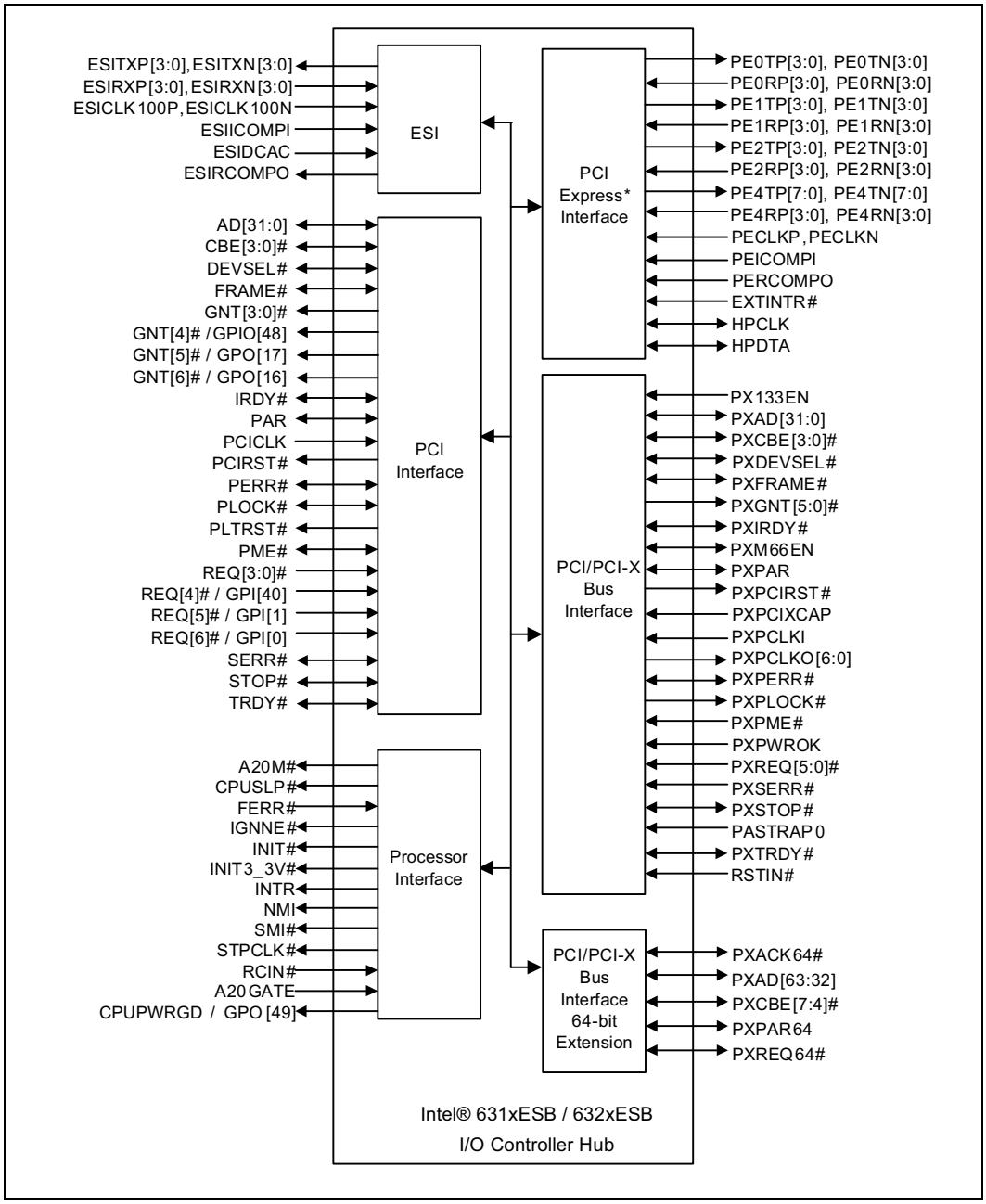


Figure 2-1. Intel® 631xESB/632xESB I/O Controller Hub Interface Signals Block Diagram (Sheet 2 of 3)

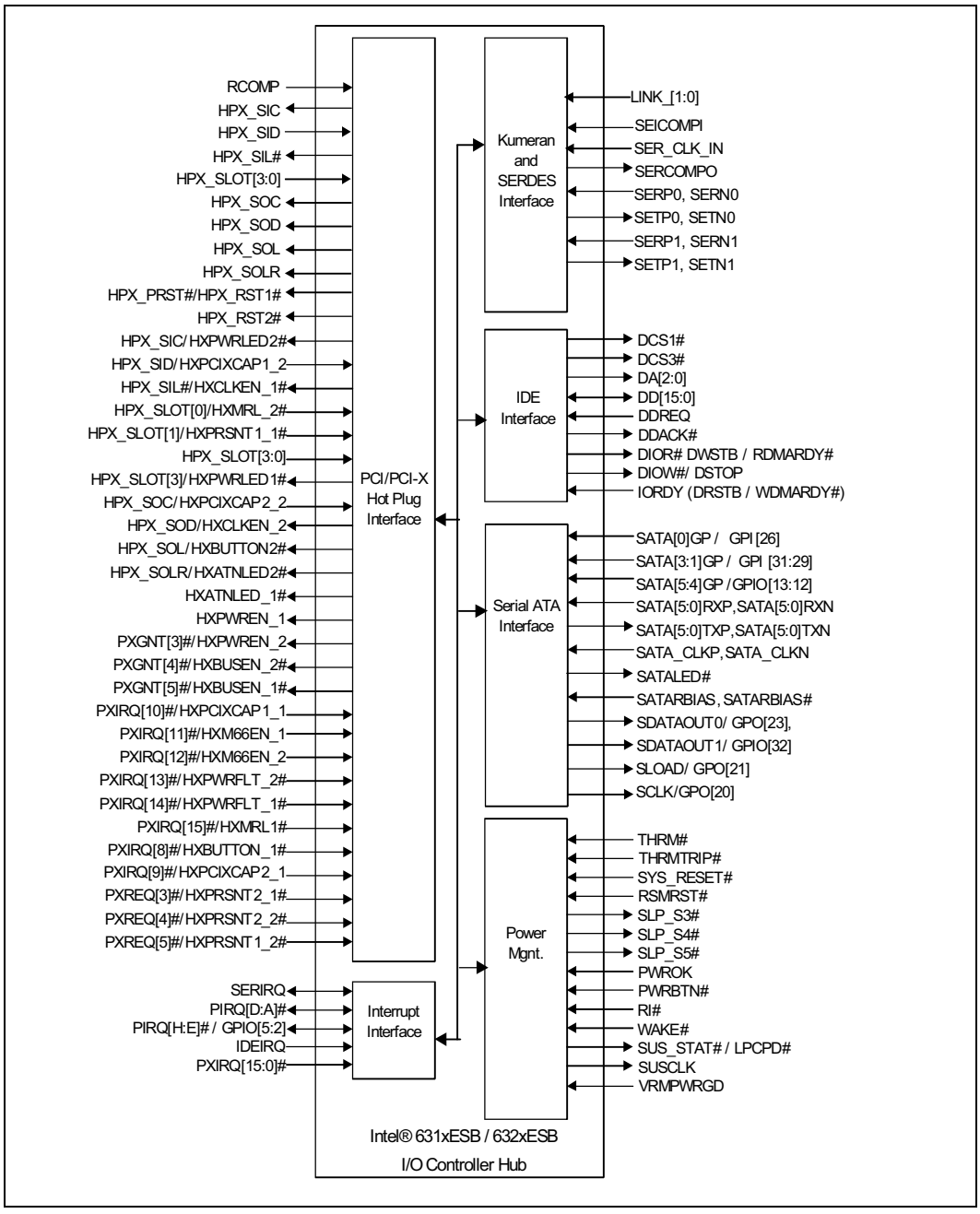
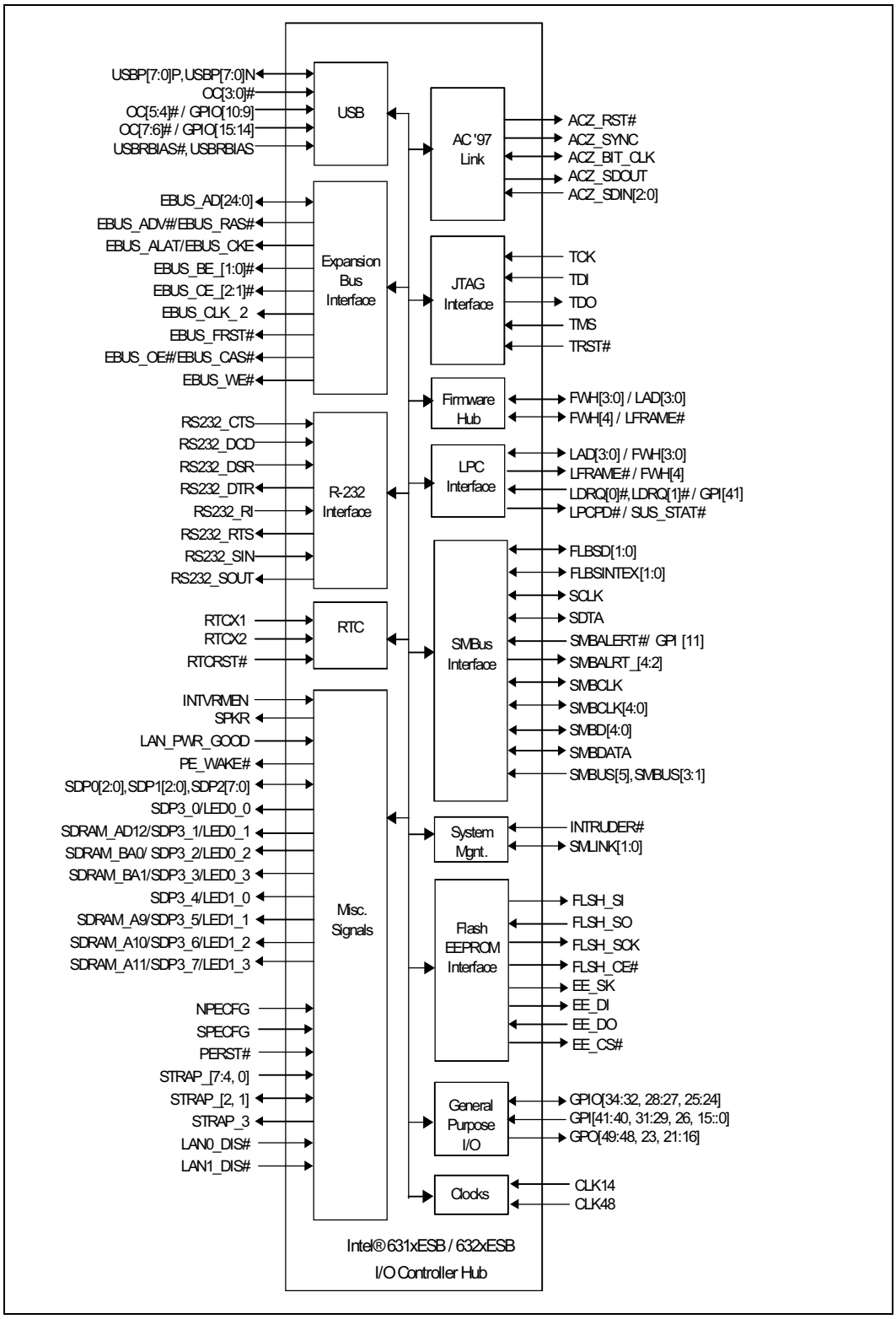


Figure 2-1. Intel® 631xESB/632xESB I/O Controller Hub Interface Signals Block Diagram (Sheet 3 of 3)



2.1 Enterprise South Bridge Interface (ESI) to Host Controller

Table 2-1. Enterprise South Bridge Interface Signals

Name	Type	Description
ESITXP[3:0], ESITXN[3:0]	O	**Enterprise South Bridge Interface Differential Transmit Pairs**
ESIRXP[3:0], ESIRXN[3:0]	I	**Enterprise South Bridge Interface Differential Receive Pair**
ESICLK100P, ESICLK100N	I	**100 MHz Differential Clock:** These signals are used to run the Enterprise South Bridge Interface. Runs at 100 MHz.
ESIICOMPI	I	**Enterprise South Bridge Interface Current Compensation Input**: Used to determine the bias current. Tied with ESIRCOMPO and pulled up to Vcc1_5 through a resistor on the system board.
ESIRCOMPO	O	**Enterprise South Bridge Interface Impedance Compensation Output:** Used to determine the impedance. Tied with ESIICOMPI and pulled up to Vcc1_5 through a resistor on the system board.
ESIDCAC	I	**ESI DA CAC Mode:** This signal is used to enable ESI interface to standard PCI Express signaling level (AC) or in half voltage (DC) mode. ESIDCAC = 1 (pulled up to Vcc1_5) ==> AC MODE (Default) ESIDCAC = 0 (pulled down to Vss) ==> DC MODE

2.2 PCI Express* Interface

Table 2-2. PCI Express* Root Port Signals

Name	Type	Description
PE0TP[3:0], PE0TN[3:0]	O	PCI Express Root Port Differential Transmit Pairs.
PE0RP[3:0], PE0RN[3:0]	I	PCI Express Root Port Differential Receive Pairs.

Table 2-3. PCI Express* Downstream Signals

Name	Type	Description
PE1TP[3:0], PE1TN[3:0]	O	PCI Express Downstream Port 1 Differential Transmit Pairs.
PE1RP[3:0], PE1RN[3:0]	I	PCI Express Downstream Port 1 Differential Receive Pairs.
PE2TP[3:0], PE2TN[3:0]	O	PCI Express Downstream Port 2 Differential Transmit Pairs.
PE2RP[3:0], PE2RN[3:0]	I	PCI Express Downstream Port 2 Differential Receive Pairs.
EXTINTR#	I	**Hot-Plug Controller interrupt pin.**
HPCLK	I/OD	**Hot-Plug Bus Clock:** SM Bus compatible Clock Pin. External pull-up required.
HPDTA	I/OD	**Hot-Plug Bus Data:** SM Bus compatible Data Pin. External pull-up required.

Table 2-4. PCI Express* Upstream Signals

Name	Type	Description
PE4TP[7:0], PE4TN[7:0]	O	**PCI Express Upstream Port Differential Transmit Pairs.**
PE4RP[7:0], PE4RN[7:0]	I	**PCI Express Upstream Port Differential Receive Pairs.**
PECLKP, PECLKN	I	**PCI Express Upstream Port Clock In**: A 100 MHz clock input used as the reference clock for this interface.
PEICOMPI	I	**PCI Express Upstream Port Current Compensation Input**: Tied with PEROCMPO and pulled up to Vcc1_5 through a resistor on the system board.
PERCOMPO	I	**PCI Express Upstream Port Impedance Compensation Output:** Used for current compensation and RX termination compensation. Tied with PEICOMPI and pulled up to Vcc1_5 through a resistor on the system board.

2.3 PCI Interface

Note: For all the PCI signals, they are 5v tolerant except PCICLK and PME#.

Table 2-5. PCI Interface Signals (Sheet 1 of 3)

Name	Type	Description
AD[31:0]	I/O	**PCI Address/Data**: AD[31:0] is a multiplexed address and data bus. During the first clock of a transaction, AD[31:0] contain a physical address (32 bits). During subsequent clocks, AD[31:0] contain data. The Intel® 631xESB/632xESB I/O Controller Hub will drive all 0s on AD[31:0] during the address phase of all PCI Special Cycles.
CBE#[3:0]	I/O	**Bus Command and Byte Enables**: The command and byte enable signals are multiplexed on the same PCI pins. During the address phase of a transaction, CBE[3:0]# define the bus command. During the data phase CBE[3:0]# define the Byte Enables. CBE[3:0]#Command Type 0 0 0 0Interrupt Acknowledge 0 0 0 1Special Cycle 0 0 1 0I/O Read 0 0 1 1I/O Write 0 1 1 0Memory Read 0 1 1 1Memory Write 1 0 1 0Configuration Read 1 0 1 1Configuration Write 1 1 0 0Memory Read Multiple 1 1 1 0Memory Read Line 1 1 1 1Memory Write and Invalidate All command encodings not shown are reserved. The Intel® 631xESB/632xESB I/O Controller Hub does not decode reserved values, and therefore will not respond if a PCI Master generates a cycle using one of the reserved values.
DEVSEL#	I/O	**Device Select**: The Intel® 631xESB/632xESB I/O Controller Hub asserts DEVSEL# to claim a PCI transaction. As an output, the Intel® 631xESB/632xESB I/O Controller Hub asserts DEVSEL# when a PCI Master peripheral attempts an access to an internal Intel® 631xESB/632xESB I/O Controller Hub address or an address destined ESI (main memory). As an input, DEVSEL# indicates the response to an Intel® 631xESB/632xESB I/O Controller Hub-initiated transaction on the PCI bus. DEVSEL# is tri-stated from the leading edge of PCIRST#. DEVSEL# remains tri-stated by the Intel® 631xESB/632xESB I/O Controller Hub until driven by a target device.

Table 2-5. PCI Interface Signals (Sheet 2 of 3)

Name	Type	Description
FRAME#	I/O	**Cycle Frame:** The current initiator drives FRAME# to indicate the beginning and duration of a PCI transaction. While the initiator asserts FRAME#, data transfers continue. When the initiator negates FRAME#, the transaction is in the final data phase. FRAME# is an input to the Intel® 631xESB/632xESB I/O Controller Hub when the Intel® 631xESB/632xESB I/O Controller Hub is the target, and FRAME# is an output from the Intel® 631xESB/632xESB I/O Controller Hub when the Intel® 631xESB/632xESB I/O Controller Hub is the initiator. FRAME# remains tri-stated by the Intel® 631xESB/632xESB I/O Controller Hub until driven by an initiator.
GNT[3:0]# GNT[4]# / GPIO[48] GNT[5]# / GPO[17]# **GNT[6]# /** GPO[16]#	O	**PCI Grants**: The Intel® 631xESB/632xESB I/O Controller Hub supports up to 7 Masters on the PCI bus. The GNT[4]# pin can instead be used as a GPIO. ***Note:*** GNT[6] is sampled at the rising edge of PWROK as a functional strap. See Section 2.28 for more details.
IRDY#	I/O	**Initiator Ready**: IRDY# indicates the Intel® 631xESB/632xESB I/O Controller Hub's ability, as an initiator, to complete the current data phase of the transaction. It is used in conjunction with TRDY#. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates the Intel® 631xESB/632xESB I/O Controller Hub has valid data present on AD[31:0]. During a read, it indicates the Intel® 631xESB/632xESB I/O Controller Hub is prepared to latch data. IRDY# is an input to the Intel® 631xESB/632xESB I/O Controller Hub when the Intel® 631xESB/632xESB I/O Controller Hub is the target and an output from the Intel® 631xESB/632xESB I/O Controller Hub when the Intel® 631xESB/632xESB I/O Controller Hub is an initiator. IRDY# remains tri-stated by the Intel® 631xESB/632xESB I/O Controller Hub until driven by an initiator.
PAR	I/O	**Calculated/Checked Parity:** PAR uses "even" parity calculated on 36 bits, AD[31:0] plus C/BE[3:0]#. "Even" parity means that the Intel® 631xESB/632xESB I/O Controller Hub counts the number of ones within the 36 bits plus PAR and the sum is always even. The Intel® 631xESB/632xESB I/O Controller Hub always calculates PAR on 36 bits regardless of the valid byte enables. The Intel® 631xESB/632xESB I/O Controller Hub generates PAR for address and data phases and only guarantees PAR to be valid one PCI clock after the corresponding address or data phase. The Intel® 631xESB/632xESB I/O Controller Hub drives and tri-states PAR identically to the AD[31:0] lines except that the Intel® 631xESB/632xESB I/O Controller Hub delays PAR by exactly one PCI clock. PAR is an output during the address phase (delayed one clock) for all Intel® 631xESB/632xESB I/O Controller Hub initiated transactions. PAR is an output during the data phase (delayed one clock) when the Intel® 631xESB/632xESB I/O Controller Hub is the initiator of a PCI write transaction, and when it is the target of a read transaction. Intel® 631xESB/632xESB I/O Controller Hub checks parity when it is the target of a PCI write transaction. If a parity error is detected, the Intel® 631xESB/632xESB I/O Controller Hub will set the appropriate internal status bits, and has the option to generate an NMI# or SMI#.
PCICLK	I	**PCI Clock**: This 33 MHz clock provides timing for all transactions on the PCI Bus.
PCIRST#	O	**PCI Reset:** This is a PCI bus reset signal. It is a logical OR of the primary interface PLTRST# signal and the state of the Secondary Bus Reset bit of the Bridge Control register (D30:F0:3Eh, bit 6). **NOTE:** PCIRST# is in the resume well.
PERR#	I/O	**Parity Error**: An external PCI device drives PERR# when it receives data that has a parity error. The Intel® 631xESB/632xESB I/O Controller Hub drives PERR# when it detects a parity error. The Intel® 631xESB/632xESB I/O Controller Hub can either generate an NMI# or SMI# upon detecting a parity error (either detected internally or reported via the PERR# signal).
PLOCK#	I/O	**PCI Lock**: This signal indicates an exclusive bus operation that may require multiple transactions to complete. The Intel® 631xESB/632xESB I/O Controller Hub asserts PLOCK# when it performs non-exclusive transactions on the PCI bus. PLOCK# is ignored when PCI Masters are granted the bus.

Table 2-5. PCI Interface Signals (Sheet 3 of 3)

Name	Type	Description
PLTRST#	O	**Platform Reset:** The Intel® 631xESB/632xESB I/O Controller Hub asserts PLTRST# to reset devices that reside on the PCI bus. The Intel® 631xESB/632xESB I/O Controller Hub asserts PLTRST# during power-up and when software initiates a hard reset sequence through the Reset Control register (I/O Register CF9h). The Intel® 631xESB/632xESB I/O Controller Hub drives PLTRST# inactive a minimum of 1 ms after both PWROK and VRMPWRGD are driven high. The Intel® 631xESB/632xESB I/O Controller Hub drives PLTRST# active a minimum of 1 ms when initiated through the Reset Control register (I/O Register CF9h). **NOTE:** PLTRST# is in the resume power plane.
PME#	I/OD	**PCI Power Management Event**: PCI peripherals drive PME# to wake the system from low-power states S1, S3, S4 and S5. PME# assertion can also be enabled to generate an SCI from the S0 state. **NOTE:** In some cases the Intel® 631xESB/632xESB I/O Controller Hub may drive PME# active due to an internal wake event. **NOTE:** PME# is in the resume power plane and it has internal pull-up.
REQ[3:0]# REQ[4]# / GPI[40] REQ[5]# / GPI[1] **REQ[6]# /** GPI[0]	I	**PCI Requests**: The Intel® 631xESB/632xESB I/O Controller Hub supports up to 7 Masters on the PCI bus. The REQ[4]#, REQ[5]#, and REQ[6]# pins can instead be used as a GPI.
SERR#	I/OD	**System Error**: SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the Intel® 631xESB/632xESB I/O Controller Hub has the ability to generate an NMI, SMI#, or interrupt.
STOP#	I/O	**Stop**: STOP# indicates that the Intel® 631xESB/632xESB I/O Controller Hub, as a target, is requesting the initiator to stop the current transaction. STOP# causes the Intel® 631xESB/632xESB I/O Controller Hub, as an initiator, to stop the current transaction. STOP# is an output when the Intel® 631xESB/632xESB I/O Controller Hub is a target and an input when the Intel® 631xESB/632xESB I/O Controller Hub is an initiator.
TRDY#	I/O	**Target Ready**: TRDY# indicates the Intel® 631xESB/632xESB I/O Controller Hub's ability as a target to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed when both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that the Intel® 631xESB/632xESB I/O Controller Hub, as a target, has placed valid data on AD[31:0]. During a write, TRDY# indicates the Intel® 631xESB/632xESB I/O Controller Hub, as a target, is prepared to latch data. TRDY# is an input to the Intel® 631xESB/632xESB I/O Controller Hub when the Intel® 631xESB/632xESB I/O Controller Hub is the initiator and an output from the Intel® 631xESB/632xESB I/O Controller Hub when the Intel® 631xESB/632xESB I/O Controller Hub is a target. TRDY# is tri-stated from the leading edge of PCIRST#. TRDY# remains tri-stated by the Intel® 631xESB/632xESB I/O Controller Hub until driven by a target.

2.4 PCI/PCI-X* Bus Interface

Table 2-6. PCI/PCI-X* Bus Interface Signals (Sheet 1 of 2)

Signal	Type	Description
PX133EN	I	Only relevant when Intel® 631xESB/632xESB I/O Controller Hub samples PxPCIXCAP at a level indicating 133 MHz PCI-X* capability. **PCI-X 133 MHz Enable**: Sets the maximum frequency capability of a PCI-X bus to either 100 MHz or 133 MHz. This pin, when high, allows the PCI-X segment to run at a maximum 133 MHz when in PCI-X mode. When low, the PCI-X segment is limited to a maximum frequency of 100 MHz when in PCI-X mode.
PXAD[31:0]	I/O	**PCI Address/Data:** These signals are a multiplexed address and data bus. During the address phase or phases of a transaction, the initiator drives a physical address on PXAD[31:0]. During the data phases of a transaction, the initiator drives write data, or the target drives read data.
PXCBE[3:0]#	I/O	**Bus Command and Byte Enables:** These signals are a multiplexed command field and byte enable field. During the address phase or phases of a transaction, the initiator drives the transaction type on PXCBE[3:0]#. For both read and write transactions, the initiator drives byte enables on PXCBE[3:0]# during the data phases.
PXDEVSEL#	I/O	**Device Select:** Intel® 631xESB/632xESB I/O Controller Hub asserts PXDEVSEL# to claim a PCI transaction. As a target, Intel® 631xESB/632xESB I/O Controller Hub asserts PXDEVSEL# when a PCI Master peripheral attempts an access to an internal address or an address destined for the PCI Express interface. As an initiator, PXDEVSEL# indicates the response to a PCI Express-to-PCI-X bridge-initiated transaction on the PCI bus. PXDEVSEL# is tri-stated from the leading edge of PXPCIRST#. PXDEVSEL# remains tri-stated by Intel® 631xESB/632xESB I/O Controller Hub until driven as a target.
PXFRAME#	I/O	**Frame:** PXFRAME# is driven by the Initiator to indicate the beginning and duration of an access. While PXFRAME# is asserted, data transfers continue. When PXFRAME# is negated, the transaction is in the final data phase.
PXGNT[5:0]#	O	**PCI Grants:** Bus grant output corresponding to request inputs 5 through 0 from Intel® 631xESB/632xESB I/O Controller Hub arbiter. This signal indicates that an initiator can start a transaction on the PCI bus.
PXIRDY#	I/O	**Initiator Ready:** PXIRDY# indicates the ability of the initiator to complete the current data phase of the transaction. A data phase is completed when both PXIRDY# and PXTRDY# are sampled asserted.
PXM66EN	I/O	Only relevant when Hot-Plug Mode is disabled (HPx_SLOT[3] = 0) or when in one-slot-no-glue Hot-Plug mode (HPx_SLOT[3:0] = 1111). **66 MHz Enable:** This input signal from the PCI Bus indicates the speed of the PCI Bus. If it is high, the bus speed is 66 MHz; if it is low, the bus speed is 33 MHz. This signal will be used to generate the appropriate clock (33 MHz or 66 MHz) on the PCI Bus. **Hot-Plug Mode Enabled:** Not used. The PCI bus will power up as 33 MHz PCI and Intel® 631xESB/632xESB I/O Controller Hub will drive this pin low. Also, if software ever writes 00 to the PFREQ Register, Intel® 631xESB/632xESB I/O Controller Hub will drive this pin low. **Hot-Plug Mode Disabled:** Controls max frequency (33 MHz or 66 MHz) of the PCI segment when running in conventional PCI mode: 0 = 33 MHz PCI 1 = 66 MHz PCI
PXPAR	I/O	**Parity:** Even parity calculated on 36 bits (PXAD[31:0] plus PXCBE[3:0]#). It is calculated on all 36 bits, regardless of the valid byte enables. It is driven identically to the PXAD[31:0] lines, except it is delayed by exactly one PCI clock.
PXPCIRST#	O	**PCI Reset:** Intel® 631xESB/632xESB I/O Controller Hub asserts PXPCIRST# to reset devices that reside on the secondary PCI bus. Intel® 631xESB/632xESB I/O Controller Hub asserts PXPCIRST# due to one of the following events: • RSTIN# is asserted. • PWROK is asserted. • The PCI Reset (bit 6) in the Bridge Control Register is set. Connect to the RST# pin of the PCI slot(s) in non-Hot-Plug mode.

Table 2-6. PCI/PCI-X* Bus Interface Signals (Sheet 2 of 2)

Signal	Type	Description
PXPCIXCAP	I	Only relevant when Hot-Plug Mode is disabled (HPX_SLOT[3] = 0) or when in one-slot-no-glue Hot-Plug mode (HPX_SLOT[3:0] = 1111). **PCI-X Capable:** This signal indicates whether all devices on the PCI bus are PCI-X devices, so that Intel® 631xESB/632xESB I/O Controller Hub can switch into PCI-X mode. Hot-Plug Mode Disabled or one-slot-no-glue Hot-Plug mode: Connect directly to the PCIXCAP pin on the PCI slot. Refer to the latest PCI-X specification. Hot-Plug Mode Enabled: Not used, except for one-slot-no glue Hot-Plug mode. If in one-slot-no glue Hot-Plug mode, connect to PCI slot PCIXCAP pin.
PXPCLKI	I	**PCI Clock In:** This signal is connected to the PXPCLKO[6] output.
PXPCLKO[6:0]	O	**PCI Clock Output:** These signals provide 33/66/100/133 MHz clock for a PCI/PCI-X device. PXPCLKO[0] goes to slot or device #1, PXPCLKO[1] goes to slot or device #2, and so forth, PXPCLKO[6] is connected to the PXPCLKI input. Unused PCI Clock outputs should be turned off by BIOS and left as no connects on the system board.
PXPERR#	I/O	**Parity Error:** PXPERR# is driven by an external PCI device when it receives data that has a parity error. Driven by Intel® 631xESB/632xESB I/O Controller Hub when, as an initiator it detects a parity error during a read transaction and as a target during write transactions.
PXPLOCK#	O	**PCI Lock:** This signal indicates an exclusive bus operation and may require multiple transactions to complete. Intel® 631xESB/632xESB I/O Controller Hub asserts PXPLOCK# when it is doing exclusive transactions on the PCI bus. PXPLOCK# is ignored when PCI Masters are granted the bus. Intel® 631xESB/632xESB I/O Controller Hub does not propagate locked transactions upstream.
PXPME#	I	**PCI Power Management Event:** PCI bus power management event signal. This is a shared open drain signal from all the PCI cards on the corresponding PCI bus segment. This is a level sensitive signal that will be converted to a PME event on the PCI Express bus.
PXPWROK	I	**Power Supply OK**: When high indicates that the system power supply has stabilized. When low, asynchronously resets the PCI Express Bridge/Switch. Some of the strap pins on the Intel® 631xESB/632xESB I/O Controller Hub are sampled on the rising edge of this signal. This signal can be used to gate the starting of the PCI Express clocks, since it is required that all voltages supplied to the Intel® 631xESB/632xESB I/O Controller Hub be valid and stable prior to starting the PCI Express clocks.
PXREQ[5:0]#	I	**PCI Request:** Request input into Intel® 631xESB/632xESB I/O Controller Hub arbiter.
PXSERR#	I	**System Error:** PXSERR# can be pulsed active by any PCI device that detects a system error condition except Intel® 631xESB/632xESB I/O Controller Hub. Intel® 631xESB/632xESB I/O Controller Hub samples PXSERR# as an input and conditionally forwards it to the PCI Express interface.
PXSTOP#	I/O	**Stop:** PXSTOP# indicates that the target is requesting an initiator to stop the current transaction.
PASTRAP0	I	**Strap:** Intel test mode signals: 1 = Reserved 0 = Normal operation
PXTRDY#	I/O	**Target Ready:** PXTRDY# indicates the ability of the target to complete the current data phase of the transaction. A data phase is completed when both PXTRDY# and PXIRDY# are sampled asserted. PXTRDY# is tri-stated from the leading edge of PXPCIRST#. PXTRDY# remains tri-stated by Intel® 631xESB/632xESB I/O Controller Hub until driven as a target.
RSTIN#	I	**Reset In**: When asserted, this signal asynchronously resets the Intel® 631xESB/632xESB I/O Controller Hub logic and asserts PXPCIRST# active output. This signal is typically connected to the PLTRST# output of the Intel® 631xESB/632xESB I/O Controller Hub.
RCOMP	I	**PCI RCOMP**: Analog compensation pin for PCI. Connect to a pull-down resistor to ground. Nominally 0.75VRCOMP

2.5 PCI/PCI-X* Bus Interface 64-bit Extension

Table 2-7. PCI Bus Interface 64-bit Extension Interface Signals

Signal	Type	Description
PXACK64#	I/O	**PCI Interface Acknowledge 64-bit Transfer:** This signal is asserted by the target only when PXREQ64# is asserted by the initiator. It indicates the target's ability to transfer data using 64 bits. It has the same timing as PXDEVSEL#.
PXAD[63:32]	I/O	**PCI Address/Data:** These signals are a multiplexed address and data bus. This bus provides an additional 32 bits to the PCI bus. During the data phases of a transaction, the initiator drives the upper 32 bits of 64-bit write data, or the target drives the upper 32 bits of 64-bit read data, when PXREQ64# and PXACK64# are both asserted.
PXCBE[7:4]#	I/O	**Bus Command and Byte Enables (Upper 4 bits):** These signals are a multiplexed command field and byte enable field. For both read and write transactions, the initiator will drive byte enables for the PXAD[63:32] data bits on PXCBE[7:4]# during the data phases when PXREQ64# and PXACK64# are both asserted.
PXPAR64	I/O	**PCI Interface Upper 32-bits Parity:** This signal carries the even parity of the 36 bits of PXAD[63:32] and PXCBE[7:4]# for both address and data phases.
PXREQ64#	I/O	**PCI interface Request 64-bit Transfer:** This signal is asserted by the initiator to indicate that the initiator is requesting a 64-bit data transfer. It has the same timing as PXFRAME#. When the Intel® 631xESB/632xESB I/O Controller Hub is the initiator, this signal is an output. When the Intel® 631xESB/632xESB I/O Controller Hub is the target, this signal is an input.

2.6 PCI/PCI-X Hot-Plug Interface

Table 2-8. General Hot-Plug Interface Signals – All Hot-Plug Modes

Signal	Type	Description
HPX_SLOT[3]	I	**Enable/Disable PCI Hot-Plug Mode**: 1 = Hot-Plug Mode Enabled 0 = Hot-Plug Mode Disabled
HPX_SLOT[2:0]	I	**Hot-Plug Mode / # of PCI Slots**: Used in conjunction with HPX_SLOT[3] signal to determine PCI Hot-Plug Mode and number of PCI slots on a bus segment. HPX_SLOT[3:0] = Hot-Plug Mode Enable/Disable, # of PCI slots 0000 = Hot-Plug disabled, 1 slot (optional). 0001 = Hot-Plug disabled, 2 slots (optional). 0010 = Hot-Plug disabled, 3 slots (optional). 0011 = Hot-Plug disabled, 4 slots (optional). 0100 = Hot-Plug disabled, 5 slots (optional). 0101 = Hot-Plug disabled, 6 slots (optional). 0110 = Hot-Plug disabled, 7 slots (optional). 0111 = Hot-Plug disabled, 8 slots (optional). 1000 = Reserved. 1001 = Hot-Plug enabled, 1 slot (parallel mode). 1010 = Hot-Plug enabled, 2 slots (parallel mode). 1011 = Hot-Plug enabled, 3 slots (serial mode). 1100 = Hot-Plug enabled, 4 slots (serial mode). 1101 = Hot-Plug enabled, 5 slots (serial mode). 1110 = Hot-Plug enabled, 6 slots (serial mode). 1111 = Hot-Plug enabled, 1-slot-no-glue (parallel mode).

Table 2-9. Serial Mode Hot-Plug Signals – 3 to 6 Slots

Signal	Type	Description
HPX_PRST#/ HPX_RST1#	O	**Primary Bus Reset Out (HPX_PRST#):** This is asserted whenever the upstream PCI Express ports of the Intel® 631xESB/632xESB I/O Controller Hub go through a reset, even if hot-plug is disabled. Resets the slot interface logic in Hot-Plug serial mode.
HPX_SIC	O	**Serial Input Clock:** This signal is normally high. It pulses low to shift external serial input shift register data one bit position. (The shift registers should be similar to standard “74x165” series.)
HPX_SID	I	**Serial Input Data:** Data shifted in from external logic on HPX_SIC.
HPX_SIL#	O	**Serial Input Load:** This signal is normally high. It pulses low to synchronously parallel load external serial input shift registers on the next rising edge of HPX_SIC.
HPX_SLOT[3:0]	I	**Hot-Plug Mode Enable / # of PCI Slots:** Used to enable/disable Hot-Plug mode and to determine number of Hot-Plug slots. HPX_SLOT[3:0]: 1011 = Hot-Plug enabled, 3 slots (serial mode). 1100 = Hot-Plug enabled, 4 slots (serial mode). 1101 = Hot-Plug enabled, 5 slots (serial mode). 1110 = Hot-Plug enabled, 6 slots (serial mode).
HPX_SOC	O	**Serial Output Clock:** This signal is normally high. It pulses low to shift internal serial output shift register data one bit position. (The shift registers should be similar to standard “74x164” series).
HPX_SOD	O	**Serial Output Data:** Data is shifted out to external logic on HPX_SOC.
HPX_SOL	O	**Serial Output Non-Reset Latch Load:** This signal is normally high. It pulses low to clock external latches (power-enable, clock-enable, slot bus-enable, and LED latches). The high edge acts as the clock.
HPX_SOLR	O	**Serial Output Reset Latch Load:** This signal is normally high. It pulses high to clock external latches (Reset latches) reading the serial output shift registers. The high edge acts as the clock.

Table 2-10. PCI-X* Parallel Mode Hot-Plug Signals – 1 to 2 Slots (Sheet 1 of 4)

Signal	Type	Description
HPX_PRST#/ HPX_RST1#	O	**Slot 1 Reset:** This is the slot 1 reset in the parallel Hot-Plug mode. Connected to the RST# pin of the first PCI Hot-Plug slot. Used when in 1-slot-no-glue, single-slot or dual-slot parallel Hot-Plug mode (HPX_SLOT[3:0] = 1111, 1001 or 1010).
HPX_RST2#	O	**Slot 2 Reset**: This is the slot 2 reset in the parallel Hot-Plug mode. Connected to the RST# pin of the second PCI Hot-Plug slot. Only used when in dual-slot parallel Hot-Plug mode (HPX_SLOT[3:0] = 1010).
HPX_SIC/ HXPWRLED2#	O	**Slot 2 Power LED**: Output signal connected to the power LED corresponding to the second Hot-Plug slot, which is green in color. Only used when in dual-slot parallel Hot-Plug mode (HPX_SLOT[3:0] = 1010).
HPX_SID/ HXPCIXCAP1_2	I	**Slot 2 PCIXCAP1**: Determines if the first Hot-Plug slot is PCI-X* capable, and if so, whether it can operate at 133 MHz. PCIXCAP1 and PCIXCAP2 represent a decoded version of the three-state PCIXCAP pin present on each slot. PCIXCAP2 represents whether the PCIXCAP pin was ground or not ground (that is, PCI-X capable), and PCIXCAP1 represents whether the PCIXCAP pin was “low” (66 MHz only) or high (133 MHz capable). The system initially powers up at 33 MHz PCI, and all Hot-Plug slots are scanned by firmware. If the system is capable, the bus is reset to run in the appropriate PCI-X mode. These pins are used only in dual-slot parallel Hot-Plug mode (HPX_SLOT[3:0] = 1010).

Table 2-10. PCI-X* Parallel Mode Hot-Plug Signals – 1 to 2 Slots (Sheet 2 of 4)

Signal	Type	Description
HPX_SIL#/ HXCLKEN_1#	O	**Slot 1 Clock Enable:** Clock enable signals that connect the PCI clock signals of the first PCI slot to the system bus PCI bus via FET isolation switches. Only used when in single-slot or dual-slot parallel Hot-Plug mode (HPX_SLOT[3:0] = 1001 or 1010).
HPX_SLOT[0]/ HXMRL_2#	I	**Slot 2 Manual Retention Latch:** Optional. Manually operated retention latch sensor input. A logic low input that is connected directly to the MRL sensor on the second Hot-Plug slot. When asserted it indicates that the MRL latch is closed. If a platform does not support MRL sensors, this must be wired to a low logic level (MRL closed). Only used when in dual-slot parallel Hot-Plug mode (HPX_SLOT[3:0] = 1010).
HPX_SLOT[1]/ HXPRSNT1_1#	I	**Slot 1 PRESENT1#:** Input signal (optional). Used in conjunction with HXPRSNT2_1# to indicate to the Intel® 631xESB/632xESB I/O Controller Hub whether an add-on card is installed in the first Hot-Plug slot and its power requirements. This signal is directly connected to the present bits on the PCI/PCI-X add-on card. Only used when in one slot no glue mode, single-slot or dual-slot parallel Hot-Plug mode (HPX_SLOT[3:0] = 1111, 1001 or 1010).
HPX_SLOT[3:0]	I	**Hot-Plug Mode Enable / # of PCI Slots:** Used to enable/disable Hot-Plug mode and to determine number of Hot-Plug slots. HPX_SLOT[3:0]: 1111 = Hot-Plug enabled, one-slot-no-glue Hot-Plug mode. 1001 = Hot-Plug enabled, 1 slot (parallel mode) 1010 = Hot-Plug enabled, 2 slots (parallel mode)
HPX_SLOT[3]/ HXPWRLED1#	O	**Slot 1 Power LED:** Output signal connected to the green power LED corresponding to the first Hot-Plug slot. Only used when in one-slot-no-glue, single-slot parallel, or dual-slot parallel Hot-Plug mode (HPX_SLOT[3:0] = 1111, 1001, or 1010).
HPX_SOC/ HXPCIXCAP2_2	I	**Slot 2 PCIXCAP2**: Determines if the second Hot-Plug slot is PCI-X capable, and if so, whether it can operate at 133 MHz. PCIXCAP1 and PCIXCAP2 represent a decoded version of the three-state PCIXCAP pin present on each slot. PCIXCAP2 represents whether the PCIXCAP pin was ground or not ground (that is, PCI-X capable), and PCIXCAP1 represents whether the PCIXCAP pin was “low” (66 MHz only) or high (133 MHz capable). The system initially powers up at 33 MHz PCI, and all Hot-Plug slots are scanned by firmware. If the system is capable, the bus is reset to run in the appropriate PCI-X mode. These pins are used only in the dual-slot parallel Hot-Plug mode (HPX_SLOT[3:0] = 1010).
HPX_SOD/ HXCLKEN_2	O	**Slot 2 Clock Enable**: Clock enable signals that connect the PCI clock signals of the second PCI slot to the system bus PCI bus via FET isolation switches. Only used when in dual-slot parallel Hot-Plug mode (HPX_SLOT[3:0] = 1010).
HPX_SOL/ HXBUTTON2#	O	**Slot 2 Attention Button**: Optional. Attention button input signal connected to the second Hot-Plug slot’s attention button. When low, indicates that the operator has requested attention. If attention button is not implemented, then this input must be wired to a high logic level. Only used when in dual-slot parallel Hot-Plug mode (HPX_SLOT[3:0] = 1010).
HPX_SOLR/ HXATNLED2#	O	**Slot 2 Attention LED**: Control for attention LED of the second Hot-Plug slot, which is yellow or amber in color. Only used when in dual-slot parallel Hot-Plug mode (HPX_SLOT[3:0] = 1010).
HXATNLED_1#	O	**Slot 1 Attention LED:** Control for attention LED of the first Hot-Plug slot, which is yellow or amber in color. Only used when in one-slot-no-glue, single-slot parallel, or dual-slot parallel Hot-Plug mode (HPX_SLOT[3:0] = 1111, 1001, or 1010).
HXPWREN_1	O	**Slot 1 Power Enable:** Connected to slot 1 on-board power controller to regulate current and voltage flow of the PCI slot. Only used when in one-slot-no-glue, single-slot parallel, or dual-slot parallel Hot-Plug mode (HPX_SLOT[3:0] = 1111, 1001, or 1010).
PXGNT[3]#/ HXPWREN_2	O	**Slot 2 Power Enable:** Connected to slot 2 on-board power controller to regulate current and voltage flow of the PCI slot. Only used when in dual-slot parallel Hot-Plug mode (HPX_SLOT[3:0] = 1010).

Table 2-10. PCI-X* Parallel Mode Hot-Plug Signals – 1 to 2 Slots (Sheet 3 of 4)

Signal	Type	Description
PXGNT[4]#/ HXBUSEN_2#	O	**Slot 2 Bus Enable:** Bus enable signals that connect the PCI bus signals of the second PCI slot to the system bus PCI bus via FET isolation switches. Only used when in dual-slot parallel Hot-Plug mode (HPX_SLOT[3:0] = 1010).
PXGNT[5]#/ HXBUSEN_1#	O	**Slot 1 Bus Enable:** Bus enable signals that connect the PCI bus signals of the first PCI slot to the system bus PCI bus via FET isolation switches. Only used when in single-slot or dual-slot parallel Hot-Plug mode (HPX_SLOT[3:0] = 1001 or 1010).
PXIRQ[10]#/ HXPCIXCAP1_1	I	**Slot 1 PCIXCAP1:** Determines if the first Hot-Plug slot is PCI-X capable, and if so, whether it can operate at 133 MHz. PCIXCAP1 and PCIXCAP2 represent a decoded version of the three-state PCIXCAP pin present on each slot. PCIXCAP2 represents whether the PCIXCAP pin was ground or not ground (that is, PCI-X capable), and PCIXCAP1 represents whether the PCIXCAP pin was “low” (66 MHz only) or high (133 MHz capable). The system initially powers up at 33 MHz PCI, and all Hot-Plug slots are scanned by firmware. If the system is capable, the bus is reset to run in the appropriate PCI-X mode. These pins are used only in the single-slot and dual-slot parallel Hot-Plug mode.
PXIRQ[11]#/ HXM66EN_1	I	**Slot 1 M66EN:** Determines if an add-in card is capable of running at 66 MHz in conventional PCI mode for the first Hot-Plug slot. Only used when in one-slot-no-glue, single-slot parallel, or dual-slot parallel Hot-Plug mode (HPX_SLOT[3:0] = 1111, 1001, or 1010).
PXIRQ[12]#/ HXM66EN_2	I	**Slot 2 M66EN:** Determines if an add-in card is capable of running at 66 MHz in conventional PCI mode for the second Hot-Plug slot. Only used when in dual-slot parallel Hot-Plug mode (HPX_SLOT[3:0] = 1010).
PXIRQ[13]#/ HXPWRFLT_2#	I	**Hot-Plug Parallel Mode only - (HXPWRFLT_2#):** Power controller fault indication for over-current / under-voltage condition for the second Hot-Plug slot. When asserted, Intel® 631xESB/632xESB I/O Controller Hub, if enabled, immediately asserts reset to the slot and disconnects the slot from the bus. Only used when in dual-slot parallel Hot-Plug mode (HPX_SLOT[3:0] = 1010).
PXIRQ[14]#/ HXPWRFLT_1#	I	**Slot 1 Power Fault:** Power controller fault indication for over-current / under-voltage condition for the first Hot-Plug slot. When asserted, Intel® 631xESB/632xESB I/O Controller Hub, if enabled, immediately asserts reset to the slot and disconnects the PCI slot from the bus. Only used when in one-slot-no-glue, single-slot parallel, or dual-slot parallel Hot-Plug mode (HPX_SLOT[3:0] = 1111, 1001, or 1010).
PXIRQ[15]#/ HXMRL1#	I	**Slot 1 Manual Retention Latch:** Optional. Manually operated retention latch sensor input. A logic low input that is connected directly to the MRL sensor on the first Hot-Plug slot. When asserted it indicates that the MRL latch is closed. If a platform does not support MRL sensors, this must be wired to a low logic level (MRL closed). Only used when in one-slot-no-glue, single-slot parallel, or dual-slot parallel Hot-Plug mode (HPX_SLOT[3:0] = 1111, 1001, or 1010).
PXIRQ[8]#/ HXBUTTON_1#	I	**Slot 1 Attention Button:** Optional. Attention button input signal connected to the first Hot-Plug slot’s attention button. When low, indicates that the operator has requested attention. If attention button is not implemented, then this input must be wired to a high logic level. Only used when in single-slot or dual-slot parallel Hot-Plug mode (HPX_SLOT[3:0] = 1001 or 1010).
PXIRQ[9]#/ HXPCIXCAP2_1	I	**Slot 1 PCIXCAP2**: Determines if the first Hot-Plug slot is PCI-X capable, and if so, whether it can operate at 133 MHz. PCIXCAP1 and PCIXCAP2 represent a decoded version of the three-state PCIXCAP pin present on each slot. PCIXCAP2 represents whether the PCIXCAP pin was ground or not ground (that is, PCI-X capable), and PCIXCAP1 represents whether the PCIXCAP pin was “low” (66 MHz only) or high (133 MHz capable). The system initially powers up at 33 MHz PCI, and all Hot-Plug slots are scanned by firmware. If the system is capable, the bus is reset to run in the appropriate PCI-X mode. These pins are used only in the single-slot and dual-slot parallel Hot-Plug mode.

Table 2-10. PCI-X* Parallel Mode Hot-Plug Signals – 1 to 2 Slots (Sheet 4 of 4)

Signal	Type	Description
PXREQ[3]#/ HXPRSNT2_1#	I	**Slot 1 PRESENT2#**: Input signal (optional). Used in conjunction with HXPRSNT1_1# to indicate to Intel® 631xESB/632xESB I/O Controller Hub whether an add-on card is installed in the first Hot-Plug slot and its power requirements. This signal is directly connected to the present bits on the PCI/PCI-X add-on card. Only used when in single-slot or dual-slot parallel Hot-Plug mode (HPX_SLOT[3:0] = 1001 or 1010).
PXREQ[4]#/ HXPRSNT2_2#	I	**Slot 2 PRESENT2#**: Input signal (optional). Used in conjunction with HXPRSNT1_2# to indicate to Intel® 631xESB/632xESB I/O Controller Hub whether an add-on card is installed in the second Hot-Plug slot and its power requirements. This signal is directly connected to the present bits on the PCI/PCI-X add-on card. Only used when in dual-slot parallel Hot-Plug mode (HPX_SLOT[3:0] = 1010).
PXREQ[5]#/ HXPRSNT1_2#	I	**Slot 2 PRESENT1#**: Input signal (optional). Used in conjunction with HXPRSNT2_2# to indicate to Intel® 631xESB/632xESB I/O Controller Hub whether an add-on card is installed in the second Hot-Plug slot and its power requirements. This signal is directly connected to the present bits on the PCI/PCI-X add-on card. Only used when in dual-slot parallel Hot-Plug mode (HPX_SLOT[3:0] = 1010).

2.7 Interrupt Interface

Table 2-11. Interrupt Signals

Name	Type	Description
IDEIRQ	I	**IDE Interrupt Request:** This interrupt input is connected to the IDE drive.
PIRQ[D:A]#	I/OD	**PCI Interrupt Requests:** In non-APIC mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in Section 5.10.6. Each PIRQx# line has a separate Route Control register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQA# is connected to IRQ16, PIRQB# to IRQ17, PIRQC# to IRQ18, and PIRQD# to IRQ19. This frees the legacy interrupts.
PIRQ[H:E]# / GPIO[5:2]	I/OD	**PCI Interrupt Requests:** In non-APIC mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in Section 5.10.6. Each PIRQx# line has a separate Route Control register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQE# is connected to IRQ20, PIRQF# to IRQ21, PIRQG# to IRQ22, and PIRQH# to IRQ23. This frees the legacy interrupts. If not needed for interrupts, these signals can be used as GPIO inputs.
SERIRQ	I/O	**Serial Interrupt Request:** This pin implements the serial interrupt protocol.
PXIRQ[15:0]#	I	**PCI-X* Interrupt Requests:** The PXIRQ# lines from PCI interrupts PIRQ[A:D] can be routed to these interrupt lines.

Note: PIRQ and IDEIRQ are 5v tolerant and SERIRQ is 3.3v tolerant.

2.8 Kumeran and SERDES Interface

Table 2-12. Kumeran Interface Signals

Name	Type	Description
SERP0, SERN0	A-in	**SERDES and Kumeran Receive**: Port 0 receive.
SETP0, SETN0	A-out	**SERDES and Kumeran Transmit**: Port 0 transmit.
SERP1, SERN1	A-in	**SERDES and Kumeran Receive**: Port 1receive.
SETP1, SETN1	A-out	**SERDES and Kumeran Transmit**: Port 1transmit.
SER_CLK_IN	A-in	**Reference Clock in**: This pin is driven by an external 62.5 or 25 MHz clock source. When Intel® 631xESB/632xESB I/O Controller Hub is connected to external Single or Dual PHY, the 62.5 or 25 MHz clock may be generated and provided by the PHY back to Intel® 631xESB/632xESB I/O Controller Hub. Otherwise, a standalone oscillator should be used. Frequency is selected by strapping at STRAP_2: when '1', 25 MHz; when '0': 62.5 MHz.
SEICOMPI	A-in	**Impedance Compensation**: Used to control impedance compensation for MAC interface. Tied with SERCOMPO and connect to VCCSE through a common resistor.
SERCOMPO	A-out	**Impedance Compensation**: Used to control the impedance compensation for the MAC interface. Tied with SEICOMPI and connect to VCCSE through a common resistor.
LINK_[1:0]	I	LINK_[1:0] act as SIG_DET[1:0] that connect to the optical PHY's respective signal detect pins.

2.9 Serial ATA Interface

Table 2-13. Serial ATA Interface Signals (Sheet 1 of 2)

Name	Type	Description
SATA[0]GP / GPI[26] SATA[3:1]GP / GPIO[31:29] SATA[5:4]GP / GPIO[13:12]	I	**Serial ATA General Purpose:** These are input pins which can be configured as interlock switches corresponding to SATA Ports 5-0. If interlock switches are not required, these pin can be configured as the listed GPIO pins instead.
SATA[5:0]RXP SATA[5:0]RXN	I	**Serial ATA Differential Receive Pairs:** These are inbound high-speed differential signals from Ports 5-0.
SATA[5:0]TXP SATA[5:0]TXN	O	Serial ATA Differential Transmit Pairs: These are outbound high-speed differential signals to Ports 5-0.
SATA_CLKP SATA_CLKN	I	**100 MHz Differential Clock:** These signals are used to run the SATA controller. Runs at 100 MHz. This clock is permitted to stop during S3 (or lower) states.
SATALED#	OC	**Serial ATA LED:** This is an open-collector output pin driven during SATA command activity. It is to be connected to external circuitry that can provide the current to drive a platform LED. When active, the LED is on. When tri-stated, the LED is off.
SATARBIAS SATARBIAS#	I	**Serial ATA Resistor Bias:** These are analog connection points for an external resistor to ground.
SDATAOUT0/ GPO[23]	O	The SDATAOUT0 signal carries output bits associated with disk drives in the target backplane. It is intended to control LEDs (for example, activity, fault, and locate LEDS). There are 3 output data bits for each driver. This pin repeatedly drives data in the following sequencing: drive 0, drive 1, drive 2, and drive 3. This pin may be optionally used as GPO[23]

Table 2-13. Serial ATA Interface Signals (Sheet 2 of 2)

Name	Type	Description
SDATAOUT1/ GPIO[32]	O	The SDATAOUT1 signal carries output bits associated with disk drives in the target backplane. It is intended to control LEDs (for example, activity, fault, and locate LEDS). There are 3 output data bits for each driver. This pin repeatedly drives data in the following sequencing: drive 4, drive 5 followed by six 0's. This pin may be optionally used as GPIO[32]
SLOAD / GPO[21]	O	The SLOAD signal indicates when the bit stream is ending and being restarted. SLOAD is asserted on the last clock of a bit stream. After SLOAD is set to 1, the next four bit positions on SLOAD contain a vendor-specific pattern. Following that, the initiator shall set SLOAD to 0 until it wants to restart the bit stream. The vendor-specific bits are intended to communicate drive-independent information to the target. The vendor- specific bits may change on each bit stream. After power on, the initiator may set SLOAD to 1 with the first rising edge of SCLK. If SCLK was already high and vendor-specific bit 0 is also set to 1, the target is not synchronized with the initiator during the first bit stream. The initiator should not set vendor-specific bit 0 to 1 during the first bit stream. The initiator should only set SLOAD to 1 to restart a bit stream during the third bit position for a drive. The initiator can not restart a bit stream until the first bit of the second drive, because of the vendor specific bit positions on SLOAD. This pin may be optionally used as GPO[21]
SCLK / GPO[20]	O	The SCLK is repeatedly toggled at 32kHZ, the rising edge of SCLK is used to transmit changes in SLOAD, SDATAOUT0 and SDATAOUT1. The falling edge of SCLK is used to latch SLOAD, SDATAOUT0 and SDATAOUT1. When not using the SGPIO bus (for example, during a reset and when power is off). The initiator shall tristate SCLK. This pin may be optionally used as GPO[20]

2.10 IDE Interface

Table 2-14. IDE Interface Signals (Sheet 1 of 2)

Name	Type	Description
DA[2:0]	O	**IDE Device Address:** These output signals are connected to the corresponding signals on the IDE connector. They are used to indicate which byte in either the ATA command block or control block is being addressed.
DCS1#	O	**IDE Device Chip Selects for 100 Range:** For ATA command register block. This output signal is connected to the corresponding signal on the IDE connector.
DCS3#	O	**IDE Device Chip Select for 300 Range:** For ATA control register block. This output signal is connected to the corresponding signal on the IDE connector.
DD[15:0]	I/O	**IDE Device Data:** These signals directly drive the corresponding signals on the IDE connector. There is a weak internal pull-down resistor on DD7.
DDACK#	O	**IDE Device DMA Acknowledge:** This signal directly drives the DAK# signal on the IDE connector. DDACK# is asserted by the Intel® 631xESB/632xESB I/O Controller Hub to indicate to IDE DMA Slave devices that a given data transfer cycle (assertion of DIOR# or DIOW#) is a DMA data transfer cycle. This signal is used in conjunction with the PCI Bus Master IDE function and are not associated with any AT-compatible DMA channel.
DDREQ	I	**IDE Device DMA Request:** This input signal is directly driven from the DRQ signal on the IDE connector. It is asserted by the IDE device to request a data transfer, and used in conjunction with the PCI Bus Master IDE function and are not associated with any AT compatible DMA channel.

Table 2-14. IDE Interface Signals (Sheet 2 of 2)

Name	Type	Description
DIOR# / DWSTB / RDMARDY#	O	**Disk I/O Read (PIO and Non-Ultra DMA)**: This is the command to the IDE device that it may drive data onto the DD lines. Data is latched by the Intel® 631xESB/632xESB I/O Controller Hub on the deassertion edge of DIOR#. The IDE device is selected either by the ATA register file chip selects (DCS1# or DCS3#) and the DA lines, or the IDE DMA acknowledge (DDAK#). Disk Write Strobe (Ultra DMA Writes to Disk): This is the data write strobe for writes to disk. When writing to disk, Intel® 631xESB/632xESB I/O Controller Hub drives valid data on rising and falling edges of DWSTB. Disk DMA Ready (Ultra DMA Reads from Disk): This is the DMA ready for reads from disk. When reading from disk, Intel® 631xESB/632xESB I/O Controller Hub deasserts RDMARDY# to pause burst data transfers.
DIOW# / DSTOP	O	**Disk I/O Write (PIO and Non-Ultra DMA)**: This is the command to the IDE device that it may latch data from the DD lines. Data is latched by the IDE device on the deassertion edge of DIOW#. The IDE device is selected either by the ATA register file chip selects (DCS1# or DCS3#) and the DA lines, or the IDE DMA acknowledge (DDAK#). Disk Stop (Ultra DMA): Intel® 631xESB/632xESB I/O Controller Hub asserts this signal to terminate a burst.
IORDY / (DRSTB / WDMARDY#)	I	**I/O Channel Ready (PIO)**: This signal will keep the strobe active (DIOR# on reads, DIOW# on writes) longer than the minimum width. It adds wait-states to PIO transfers. Disk Read Strobe (Ultra DMA Reads from Disk): When reading from disk, Intel® 631xESB/632xESB I/O Controller Hub latches data on rising and falling edges of this signal from the disk. Disk DMA Ready (Ultra DMA Writes to Disk): When writing to disk, this is de-asserted by the disk to pause burst data transfers.

2.11 Firmware Hub Interface

Table 2-15. Firmware Hub Interface Signals

Name	Type	Description
FWH[3:0] / LAD[3:0]	I/O	**Firmware Hub Signals.** These signals are multiplexed with the LPC address signals.
FWH4 / LFRAME#	I/O	**Firmware Hub Signals.** This signal is multiplexed with the LPC LFRAME# signal.

2.12 LPC Interface

Table 2-16. LPC Interface Signals

Name	Type	Description
LAD[3:0] / FWH[3:0]	I/O	**LPC Multiplexed Command, Address, Data.**
LDRQ[0]# LDRQ[1]# / GPI[41]	I	**LPC Serial DMA/Master Request Inputs:** LDRQ[1:0]# are used to request DMA or Bus Master access. These signals are typically connected to external Super I/O device. An internal pull-up resistor is provided on these signals. LDRQ[1]# may optionally be used as GPI.
LFRAME# / FWH[4]	O	**LPC Frame:** LFRAME# indicates the start of an LPC cycle, or an abort.
LPCPD# / SUS_STAT#	O	**Suspend Status**: Indicates that the system will be entering a low power state soon.

2.13 USB Interface

Table 2-17. USB Interface Signals

Name	Type	Description
OC[3:0]# OC[5:4]# / GPIO[10:9] OC[7:6]# / GPIO[15:14]	I	**Overcurrent Indicators**: These signals set corresponding bits in the USB controllers to indicate that an overcurrent condition has occurred. OC[7:4]# may optionally be used as GPIs. OC[7:0]# are not 5 V tolerant.
USBP[0]P, USBP[0]N, USBP[1]P, USBP[1]N	I/O	**Universal Serial Bus Port [1:0] Differential**: These differential pairs are used to transmit Data/Address/Command signals for ports 0 and 1. These ports can be routed to UHCI controller #1 or the EHCI controller.
USBP[2]P, USBP[2]N, USBP[3]P, USBP[3]N	I/O	**Universal Serial Bus Port [3:2] Differential**: These differential pairs are used to transmit data/address/command signals for ports 2 and 3. These ports can be routed to UHCI controller #2 or the EHCI controller.
USBP[4]P, USBP[4]N, USBP[5]P, USBP[5]N	I/O	**Universal Serial Bus Port [5:4] Differential**: These differential pairs are used to transmit Data/Address/Command signals for ports 4 and 5. These ports can be routed to UHCI controller #3 or the EHCI controller.
USBP[6]P, USBP[6]N, USBP[7]P, USBP[7]N	I/O	**Universal Serial Bus Port [7:6] Differential**: These differential pairs are used to transmit Data/Address/Command signals for ports 6 and 7. These ports can be routed to UHCI controller #4 or the EHCI controller.
USBRBIAS, USBRBIAS#	I	**USB Resistor Bias:** Analog connection point for an external resistor. Used to set transmit currents and internal load resistors.

2.14 AC '97 Link

Table 2-18. AC '97 Link Signals

Name	Type	Description
ACZ_RST#	O	**AC '97 / High Definition Audio Reset:** Master hardware reset to external codec(s).
ACZ_SYNC	O	**AC '97 / High Definition Audio Sync:** 48 kHz fixed rate sample sync to the codec(s). Also used to encode the stream number.
ACZ_BIT_CLK	I/O	**AC'97 Bit Clock Input:** 12.288 MHz serial data clock generated by the external codec(s). This signal has an integrated pull-down resistor (see Note 1). **High Definition Audio Bit Clock Output:** 24.000 MHz serial data clock generated by the High Definition Audio controller. This signal has an integrated pull-down resistor so that ACZ_BIT_CLK doesn't float when an High Definition Audio coded (or no codec) is connected, but the signals are temporarily configured as AC'97.
ACZ_SDOUT	O	**AC '97 / High Definition Audio Serial Data Out:** Serial TDM data output to the codec(s). This serial output is double-pumped for a bit rate of 48Mb/s for High Definition Audio ***Note:*** ACZ_SDOUT is sampled at the rising edge of PWROK as a functional strap. See Section 2.28 for more details.
ACZ_SDIN[2:0]	I	**AC '97 / High Definition Audio** Serial Data In [2:0]: Serial TDM data inputs from the three codecs. The serial input is single-pumped for a bit rate of 24 Mb/s for High Definition Audio.

Note: High Definition Audio mode is selected through D27:F0:40h, bit 0: AZ/AC97#. This bit selects the mode of the shared High Definition Audio/AC '97 signals. When set to 0 AC '97 mode is selected. When set to 1 High Definition Audio mode is selected. The bit defaults to 0 (AC '97 mode).

2.15 Processor Interface

Table 2-19. Processor Interface Signals (Sheet 1 of 2)

Name	Type	Description
A20GATE	I	**A20 Gate:** A20GATE is from the keyboard controller. The signal acts as an alternative method to force the A20M# signal active. It saves the external OR gate needed with various other chipsets.
A20M#	O	**Mask A20:** A20M# will go active based on either setting the appropriate bit in the Port 92h register, or based on the A20GATE input being active.
CPUPWRGD / GPO[49]	OD	**CPU Power Good:** This signal should be connected to the processor's PWRGOOD input. This is an open-drain output signal (external pull-up resistor required) that represents a logical AND of the Intel® 631xESB/632xESB I/O Controller Hub's PWROK and VRMPWRGD signals. This signal may optionally be configured as a GPIO.
CPUSLP#	O	**CPU Sleep:** This signal puts the processor into a state that saves substantial power compared to Stop-Grant state. However, during that time, no snoops occur. The Intel Intel® 631xESB/632xESB I/O Controller Hub can optionally assert the CPUSLP# signal when going to the S1 state.
FERR#	I	**Numeric Coprocessor Error:** This signal is tied to the coprocessor error signal on the processor. FERR# is only used if the Intel® 631xESB/632xESB I/O Controller Hub coprocessor error reporting function is enabled in the OIC.CEN register (Chipset Config Registers:Offset 31FFh: bit 1). If FERR# is asserted, the Intel® 631xESB/632xESB I/O Controller Hub generates an internal IRQ13 to its interrupt controller unit. It is also used to gate the IGNNE# signal to ensure that IGNNE# is not asserted to the processor unless FERR# is active. FERR# requires an external weak pull-up to ensure a high level when the coprocessor error function is disabled. ***Note:*** FERR# can be used in some states for notification by the processor of pending interrupt events. This functionality is independent of the OIC register bit setting.

Table 2-19. Processor Interface Signals (Sheet 2 of 2)

Name	Type	Description
IGNNE#	O	**Ignore Numeric Error:** This signal is connected to the ignore error pin on the processor. IGNNE# is only used if the Intel® 631xESB/632xESB I/O Controller Hub coprocessor error reporting function is enabled in the OIC.CEN register (Chipset Config Registers:Offset 31FFh: bit 1). If FERR# is active, indicating a coprocessor error, a write to the Coprocessor Error register (I/O register F0h) causes the IGNNE# to be asserted. IGNNE# remains asserted until FERR# is negated. If FERR# is not asserted when the Coprocessor Error register is written, the IGNNE# signal is not asserted.
INIT#	O	**Initialization:** INIT# is asserted by the Intel® 631xESB/632xESB I/O Controller Hub for 16 PCI clocks to reset the processor. Intel® 631xESB/632xESB I/O Controller Hub can be configured to support processor Built In Self Test (BIST).
INIT3_3V#	O	**Initialization 3.3 V:** This is the identical 3.3 V copy of INIT# intended for Firmware Hub.
INTR	O	**CPU Interrupt:** INTR is asserted by the Intel® 631xESB/632xESB I/O Controller Hub to signal the processor that an interrupt request is pending and needs to be serviced. It is an asynchronous output and normally driven low.
NMI	O	**Non-Maskable Interrupt:** NMI is used to force a non-Maskable interrupt to the processor. The Intel® 631xESB/632xESB I/O Controller Hub can generate an NMI when either SERR# is asserted or IOCHK# goes active via the SERIRQ# stream. The processor detects an NMI when it detects a rising edge on NMI. NMI is reset by setting the corresponding NMI source enable/disable bit in the NMI Status and Control register (I/O Register 61h).
RCIN#	I	**Keyboard Controller Reset CPU:** The keyboard controller can generate INIT# to the processor. This saves the external OR gate with the Intel® 631xESB/632xESB I/O Controller Hub's other sources of INIT#. When the Intel® 631xESB/632xESB I/O Controller Hub detects the assertion of this signal, INIT# is generated for 16 PCI clocks.
SMI#	O	**System Management Interrupt:** SMI# is an active low output synchronous to PCICLK. It is asserted by the Intel® 631xESB/632xESB I/O Controller Hub in response to one of many enabled hardware or software events.
STPCLK#	O	**Stop Clock Request:** STPCLK# is an active low output synchronous to PCICLK, asserted by the Intel® 631xESB/632xESB I/O Controller Hub in response to some hardware or software events. When the processor samples STPCLK# asserted, it responds by stopping its internal clock.

2.16 SMBus Interface

Table 2-20. SMBus Interface Signals

Name	Type	Description
SMBCLK	I/OD	**SMBus Clock.** External pull-up required.
SMBDATA	I/OD	**SMBus Data.** External pull-up required.
SMBALERT#/ GPI[11]	I	**SMBus Alert**: This signal is used to wake the system or generate SMI#. If not used for SMBALERT#, it can be used as a GPI.
SCLK	I/OD	**SM Bus Clock Pin:** External pull-up required. This SMBUS is used only for internal PCI-X bridge and works only as a Slave device.
SDTA	I/OD	**SM Bus Data Pin:** External pull-up required. This SMBUS is used only for internal PCI-X bridge and works only as a Slave device.
SMBUS[5], SMBUS[3:1]	I	**SMBus Address Straps**. Internal PCI-X bridge SMBUS address strap.
FLBSD[1:0]	I/O	BMC FastLink Slave Data: Data driven by the FML Slave device. In FML Slave, this is the data driven by the Intel® 631xESB/632xESB I/O Controller Hub. In FML Master, it is the data sampled by Intel® 631xESB/632xESB I/O Controller Hub as a Master device.
FLBSINTEX[1:0]	I/O	BMC FastLink Read Alert/Extend Clock Low: This pin is driven by the FML Slave device and has two functions: (1) Alert the Master device to read from Slave. (2) Clock extension - when set zero it indicates to the Master to extend its low period of the clock. When used as SMB, this pin can be used also as SMBUS Alert for SMBus1/0.
SMBCLK[4:0]	I/O/ OD	BMC SMB Clock: This pin is the CLK driven by the Bus Master One clock pulse is generated for each data bit transferred. In FML Master, this pin is output, in FML Slave, this pin is input. In SMB, this pin is open drain.
SMBD[4:0]	I/O/ OD	BMC SMB Data: Stable during the high period of the clock (unless it is a start or stop condition). In FML, this pin is the data driven by the Bus Master Data line is not changed while the FLBMCK is high (unless it is a start or stop condition). In FML Master, this pin is output, in FML Slave, this pin is input. In SMB, this pin is open drain.
SMBALRT_[4:2]	I/OD	BMC SMBus Alert: SMB Alert status can be polled by FW to indicate whether there is an alert event.

2.17 Power Management Interface

Table 2-21. Power Management Interface Signals (Sheet 1 of 2)

Name	Type	Description
PWRBTN#	I	**Power Button:** The Power Button will cause SMI# or SCI to indicate a system request to go to a sleep state. If the system is already in a sleep state, this signal will cause a wake event. If PWRBTN# is pressed for more than 4 seconds, this will cause an unconditional transition (power button override) to the S5 state. Override will occur even if the system is in the S1-S4 states.
PWROK	I	**Power OK:** When asserted, PWROK is an indication to the Intel® 631xESB/ 632xESB I/O Controller Hub that core power and PCICLK have been stable for at least 99 ms. PWROK can be driven asynchronously. When PWROK is negated, the Intel® 631xESB/632xESB I/O Controller Hub asserts PCIRST# and PLTRST#. ***Note:*** PWROK must deassert for a minimum of three RTC clock periods in order for the Intel® 631xESB/632xESB I/O Controller Hub to fully reset the power and properly generate the PCIRST# and PLTRST# outputs.
RI#	I	**Ring Indicate:** This signal is an input from a modem. It can be enabled as a wake event, and this is preserved across power failures.
RSMRST#	I	**Resume Well Reset:** This signal is used for resetting the resume power plane logic.

Table 2-21. Power Management Interface Signals (Sheet 2 of 2)

Name	Type	Description
SLP_S3#	O	**S3 Sleep Control:** SLP_S3# is for power plane control. This signal shuts off power to all non-critical systems when in S3 (Suspend To RAM), S4 (Suspend to Disk), or S5 (Soft Off) states.
SLP_S4#	O	**S4 Sleep Control:** SLP_S4# is for power plane control. This signal shuts power to all non-critical systems when in the S4 (Suspend to Disk) or S5 (Soft Off) state. ***Note:*** This pin must be used to control the DRAM power in order to use the Intel® 631xESB/632xESB I/O Controller Hub's DRAM power-cycling feature.
SLP_S5#	O	**S5 Sleep Control:** SLP_S5# is for power plane control. This signal is used to shut power off to all non-critical systems when in the S5 (Soft Off) states.
SUS_STAT# / LPCPD#	O	**Suspend Status:** This signal is asserted by the Intel® 631xESB/632xESB I/O Controller Hub to indicate that the system will be entering a low power state soon. This can be monitored by devices with memory that need to switch from normal refresh to suspend refresh mode. It can also be used by other peripherals as an indication that they should isolate their outputs that may be going to powered-off planes. This signal is called LPCPD# on the LPC interface.
SUSCLK	O	**Suspend Clock:** This clock is an output of the RTC generator circuit to use by other chips for refresh clock.
SYS_RESET#	I	**System Reset:** This pin forces an internal reset after being debounced. The Intel® 631xESB/632xESB I/O Controller Hub will reset immediately if the SMBus is idle; otherwise, it will wait up to 25 ms ± 2 ms for the SMBus to idle before forcing a reset on the system.
THRM#	I	**Thermal Alarm:** This is an active low signal generated by external hardware to start the Hardware clock throttling mode. Can also generate an SMI# or an SCI.
THRMTRIP#	I	**Thermal Trip:** When low, this signal indicates that a thermal trip from the processor occurred, and the Intel® 631xESB/632xESB I/O Controller Hub will immediately transition to a S5 state. The Intel® 631xESB/632xESB I/O Controller Hub will not wait for the processor stop grant cycle since the processor has overheated.
VRMPWRGD	I	**VRM Power Good:** This should be connected to be the processor's VRM Power Good signifying the VRM is stable.
WAKE#	I	**PCI Express Wake Event**

2.18 System Management Interface

Table 2-22. System Management Interface Signals

Name	Type	Description
INTRUDER#	I	**Intruder Detect:** This signal can be set to disable the system if it is detected that the system chassis is opened. This signal's status is readable, so it can be used like a GPI if the Intruder Detection is not needed.
SMLINK[1:0]	I/OD	**System Management Link:** SMBus link to optional external system management ASIC or LAN controller. External pull-ups are required. Note that SMLINK0 corresponds to an SMBus Clock signal, and SMLINK1 corresponds to an SMBus Data signal.

2.19 Flash and EEPROM Interface

Table 2-23. Flash and EEPROM Interface Signals

Name	Type	Description
FLSH_SI	O	**Flash Serial Data Output**: Input to the flash.
FLSH_SO	I	**Flash Serial Data**: Output from the flash.
FLSH_SCK	O	**Flash Serial Clock**: Operates at ~20 MHz.
FLSH_CE#	O	**Flash Chip Select Output**.
EE_SK	O	**EEPROM Shift Clock**: Serial clock output to the EEPROM, Operates at ~1 MHz.
EE_DI	O	**EEPROM Data In**: data output to EEPROM.
EE_DO	I	**EEPROM Data Out**: data input from EEPROM.
EE_CS#	O	**EEPROM Chip Select**: Chip select signal to the EEPROM.

2.20 Expansion Bus Interface

Table 2-24. Expansion Bus Interface

Name	Type	Description
EBUS_AD[24:9]	I/O	**Expansion Bus High Address Bits**: Multiplexed with data. Address data bus for parallel flash and SRAM. Data bus for SDRAM
EBUS_AD[8:0]	I/O	**Expansion Bus Address Bits**: Low address bits for parallel flash, SRAM and SDRAM
EBUS_ADV#/ EBUS_RAS#	O	**PFLASH Address Valid**/SDRAM RAS. Address valid for parallel flash. Row Address strobe for SDRAM.
EBUS_ALAT/ EBUS_CKE	O	Expansion Bus Address Latch: Used to latch Flash/SRAM address. Clock enable for SDRAM.
EBUS_BE_[1:0]#	O	**Expansion Bus Data** Byte **Enable**: byte enable for write operation EBUS_BE_0 = least significant bits, EBUS_BE_1 = most significant bits
EBUS_CE_[2:1]#	O	**Expansion Bus Chip Enable**: Chip enable 1 is flash chip enable. Chip enable 2 is SRAM or SDRAM memory chip enable.
EBUS_CLK_2	O	**Expansion Bus Clock Output:** 125 MHz clock output for SDRAM
EBUS_FRST#	O	**External Flash Reset.**
EBUS_OE#/ EBUS_CAS#	O	Output Enable for parallel flash and SRAM, column address strobe for SDRAM
EBUS_WE#	O	Expansion Bus Write Enable for parallel flash, SRAM and SDRAM.

2.21 RS-232 Interface

Table 2-25. RS-232 Interface

Name	Type	Description
RS232_CTS	I	**Clear to Send.**
RS232_DCD	I	**Data Carrier Detected.**
RS232_DSR	I	**Data Set Ready.**
RS232_DTR	O	**Data Terminal Ready.**
RS232_RI	I	**Ring Indicator.**
RS232_RTS	O	**Request to Send.**
RS232_SIN	I	**Serial Input.**
RS232_SOUT	O	**Serial Output.**

2.22 Real Time Clock Interface

Table 2-26. Real Time Clock Interface

Name	Type	Description
RTCX1	Special	**Crystal Input 1:** This signal is connected to the 32.768 kHz crystal. If no external crystal is used, then RTCX1 can be driven with the desired clock rate.
RTCX2	Special	**Crystal Input 2:** This signal is connected to the 32.768 kHz crystal. If no external crystal is used, then RTCX2 should be left floating.
RTCRST#	I	**RTC Reset:** When asserted, this signal resets register bits in the RTC well. ***Notes:*** 1. Unless CMOS is being cleared (only to be done in the G3 power state), the RTCRST# input must always be high when all other RTC power planes are on. 2. In the case where the RTC battery is dead or missing on the platform, the RTEST# pin must rise before the RTCRST# pin.

2.23 JTAG Interface

Table 2-27. JTAG Interface Signals

Signal	Type	Description
TCK	I	**TAP Clock In:** This is the input clock to the JTAG TAP controller active rising edge, which runs from 0-16 MHz.
TDI	I	**Test Data In:** This is the serial data input to the JTAG BSCAN shift register chain and to the BSCAN control logic. This is latched in on the rising edge of TCK.
TDO	O	**Test Data Output:** This is the serial data output from the BSCAN logic.
TMS	I	**Test Mode Select:** This signal controls the TAP controller state machine to move to different states and is sampled on the rising edge of TCK.
TRST#	I	**Test Reset In:** This signal is used to asynchronously reset the JTAG BSCAN logic.

2.24 Other Clocks

Table 2-28. Other Clocks

Name	Type	Description
CLK14	I	**Oscillator Clock:** Used for 8254 timers. Runs at 14.31818 MHz. This clock is permitted to stop during S3 (or lower) states.
CLK48	I	**48 MHz Clock:** Used to run the USB controller. Runs at 48 MHz. This clock is permitted to stop during S3 (or lower) states.

2.25 General Purpose I/O

Table 2-29. General Purpose I/O Signals (Sheet 1 of 2)

Name	Type	Tolerance	Power Well	Description
GPO[49]	OD	3.3 V	V_CPU_IO	Fixed as Output only. Can instead be used as CPUPWRGD.
GPIO[48]	O	3.3 V	Vcc33	Fixed as Output only. Can instead be used as GNT4#.
GPIO[47:42]	N/A	N/A	N/A	Not implemented.
GPI[41]	I	3.3 V	Vcc33	Fixed as Input only. Can be used instead as LDRQ1#.
GPI[40]	I	5 V	V5REF	Fixed as Input only. Can be used instead as REQ4#.
GPIO[39:35]	N/A	N/A	N/A	Not implemented.
GPIO[34:33]	I/O	3.3 V	Vcc33	Can be input or output. Unmuxed
GPIO[32]	I/O	3.3V	Vcc33	Can be input or output. Can be used instead as SDATAOUT1
GPI[31]	I	3.3 V	Vcc33	Fixed as input. Can instead be used for SATA[3]GP.
GPI[30]	I	3.3 V	Vcc33	Fixed as input. Can instead be used for SATA[2]GP.
GPI[29]	I	3.3 V	Vcc33	Fixed as input. Can instead be used for SATA[1]GP.
GPIO[28:27]	I/O	3.3 V	VCCPSUS	Can be input or output. Unmuxed. ***Note:*** GPIO[28:27] may be programmed to blink (controllable by GPIO_BLINK (D31:F0:Offset GPIOBASE+18h:bit 28:27)).
GPI[26]	I	3.3 V	Vcc33	Fixed as input. Can instead be used for SATA[0]GP.

Table 2-29. General Purpose I/O Signals (Sheet 2 of 2)

Name	Type	Tolerance	Power Well	Description
GPIO[25]	I/O	3.3 V	VCCPSUS	Can be input or output. Unmuxed. Strap for internal Vcc2_5 regulator. See Section 2.28. ***Note:*** GPIO[25] may be programmed to blink (controllable by GPIO_BLINK (D31:F0:Offset GPIOBASE+18h:bit 25)).
GPIO[24]	I/O	3.3 V	VCCPSUS	Can be input or output. Unmuxed.
GPO[23]	O	3.3 V	Vcc33	Fixed as output only. Can be used instead as SDATAOUT0
GPIO[22]	N/A	N/A	N/A	Not Implemented
GPO[21]	O	3.3 V	Vcc33	Fixed as output only. Can be used instead as SLOAD
GPO[20]	O	3.3 V	Vcc33	Fixed as output only. Can be used instead as SCLK
GPO[19]	O	3.3 V	Vcc33	Fixed as output only. Unmuxed. ***Note:*** GPO[19] may be programmed to blink (controllable by GPIO_BLINK (D31:F0:Offset GPIOBASE+18h:bit 19)).
GPO[18]	O	3.3 V	Vcc33	Fixed as output only. Unmuxed. ***Note:*** GPO[18] will blink by default immediately after reset (controllable by GPIO_BLINK (D31:F0:Offset GPIOBASE+18h:bit 18)).
GPO[17]	O	3.3 V	Vcc33	Fixed as Output only. Can be used instead as PCI GNT[5]#.
GPO[16]	O	3.3 V	Vcc33	Fixed as Output only. Can be used instead as PCI GNT[6]#.
GPI[15:14]	I	3.3 V	VCCPSUS	Fixed as Input only. Can be used instead as OC[7:6]#
GPI[13]	I	3.3V	Vcc33	Fixed as Input only. Can instead be used for SATA[5]GP.
GPI[12]	I	3.3V	Vcc33	Fixed as input. Can instead be used for SATA[4]GP.
GPI[11]	I	3.3 V	VCCPSUS	Fixed as Input only. Can be used instead as SMBALERT#.
GPI[10:9]	I	3.3 V	VCCPSUS	Fixed as Input only. Can be used instead as OC[5:4]#.
GPI[8]	I	3.3 V	VCCPSUS	Fixed as Input only. Unmuxed.
GPI[7]	I	3.3 V	Vcc33	Fixed as Input only. Unmuxed.
GPI[6]	I	3.3 V	Vcc33	Fixed as Input only. Unmuxed.
GPI[5:2]	I	5 V	V5REF	Fixed as Input only. Can be used instead as PIRQ[H:E]#.
GPI[1,0]	I	5 V	V5REF	Fixed as Input only. Can be used instead as PCI REQ[5,6]#.

Notes:
1. GPI[15:0] can be configured to cause a SMI# or SCI. Note that a GPI can be routed to either an SMI# or an SCI, but not both.
2. All inputs are sticky. The status bit remains set as long as the input was asserted for two clocks. GPIO inputs are sampled on PCI clocks in S0/S1. GPIO inputs are sampled on RTC clocks in S3/S4/S5.
3. Some GPIOs exist in the VCCPSUS power plane. Care must be taken to make sure GPIO signals are not driven high into powered-down planes. Some Intel® 631xESB/632xESB I/O Controller Hub GPIOs may be connected to pins on devices that exist in the core well. If these GPIOs are outputs, there is a danger that a loss of core power (PWROK low) or a Power Button Override event will result in the Intel® 631xESB/632xESB I/O Controller Hub driving a pin to a logic 1 to another device that is powered down.

2.26 Miscellaneous Signals

Table 2-30. Miscellaneous Signals (Sheet 1 of 2)

Name	Type	Description
INTVRMEN	I	**Internal Voltage Regulator Enable**: This signal enables the internal 1.5 V Suspend regulator when connected to VccRTC. When connected to Vss, the internal regulator is disabled
SPKR	O	**Speaker**: The SPKR signal is the output of counter 2 and is internally "ANDed" with Port 61h bit 1 to provide Speaker Data Enable. This signal drives an external speaker driver device, which in turn drives the system speaker. Upon PLTRST#, its output state is 0. ***Note:*** SPKR is sampled at the rising edge of PWROK as a functional strap. See Section 2.28 for more details. There is a weak integrated pull-down resistor on SPKR pin.
TP[0]	I	**Test Point 0:** Strap pin for XOR test mode. Route this pin to a test point.
ESB2_TEST0	O	Should be left unconnected.
ESB2_TEST1	I/O	Should be left unconnected.
ESB2_TEST2	I	Should be left unconnected.
LAN_PWR_GOOD	I	**LAN Power Enable**: This pin indicates that the aux power is stable. At a low level this pins disable any functionality of the LAN & management part of Intel® 631xESB/632xESB I/O Controller Hub. Low to Hi transition initialize the LAN & management part of Intel® 631xESB/632xESB I/O Controller Hub. This pin must rise at least 300ms before the rising edge of the PERST# signal.
PERST#	I	**LAN Core Power and Clock Good Indication:** The assertion of PERST# indicates that both the power and the PCI Express clock sources are stable.
PE_WAKE#	OD	**PME WAKE**: Intel® 631xESB/632xESB I/O Controller Hub will drive this signal to 0 when wakeup event occurs and wake is enabled.
LAN0_DIS#	I	**LAN 0 Disable:** Used as strapping pins to disable or enable LAN port 0. Should have an external pull-up that is connected to Vaux to avoid disabling of the LAN if the internal pull-up is released.
LAN1_DIS#	I	**LAN 1 Disable:** Used as strapping pins to disable or enable LAN port 1. Should have an external pull-up that is connected to Vaux to avoid disabling of the LAN if the internal pull-up is released.
SDP0[2:0]	I/O	**Software-Defined Pins for LAN port 0**:These pins are shared with LAN port 0, these pins are software programmable with write/read input/output capability. These pins are input pins by default, but can be reset to their EEPROM defaults at AC power on, LAN PCI Express reset or LAN port state change from D3 ~ D0. Input function is always available, but if it's used as output, the output function will be locked for up to 1 second until EEPROM defaults are updated, so these pins are not recommended to be used as output. If LAN port is disabled by LAN_DIS_0/1# pin, these pins are not functional.
SDP1[2:0]	I/O	**Software-Defined Pins for LAN port 1**:These pins are shared with LAN port 1, these pins are software programmable with write/read input/output capability. These pins are input pins by default, but can be reset to their EEPROM defaults at AC power on, LAN PCI Express reset or LAN port state change from D3 ~ D0. Input function is always available, but if it's used as output, the output function will be locked for up to 1 second until EEPROM defaults are updated, so these pins are not recommended to be used as output. If LAN port is disabled by LAN_DIS_0/1# pin, these pins are not functional.
SDP2[7:0]	I/O	**BMC GPIO**. Dedicated to MMS. Can be used either as regular GPIO or as tachometers or PWM generators. The direction and the value (when configured as an output) are EEPROM configurable during power-on reset. These pins are not affected by SW or system reset.
SDP3_0/LED0_0	O	Used either as BMC generic GPIO, or as LAN 0 -activity LED Driver Output by default.
SDRAM_AD12/ SPD3_1/LED0_1	O	Used as A12 if the port is used in external SDRAM mode, or as BMC generic GPIO, or as LAN 0 - 10M LED Driver Output by default if SDRAM mode is not enabled.

Table 2-30. Miscellaneous Signals (Sheet 2 of 2)

Name	Type	Description
SDRAM_BA0/ SDP3_2/LED0_2	O	Used as BA0 if the port is used in external SDRAM mode, or as BMC generic GPIO, or as LAN 0 - 100M LED Driver Output by default if SDRAM mode is not enabled.
SDRAM_BA1/ SDP3_3/LED0_3	O	Used as BA1 if the port is used in external SDRAM mode, or as BMC generic GPIO, or as LAN 0 - 1000M LED Driver Output by default if SDRAM mode is not enabled.
SDP3_4/LED1_0	O	Used either as BMC generic GPIO, or as LAN 1-activity LED Driver Output by default.
SDRAM_A9/ SDP3_5/LED1_1	O	Used as A9 if the port is used in external SDRAM mode, or as BMC generic GPIO, or MAC 1 - 10M LED Driver Output by default if SDRAM mode is not enabled.
SDRAM_A10/ SDP3_6/LED1_2	O	Used as A10 if the port is used in external SDRAM mode, or as BMC generic GPIO, or as LAN 1- 100M LED Driver Output by default if SDRAM mode is not enabled.
SDRAM_A11/ SDP3_7/LED1_3	O	Used as A11 if the port is used in external SDRAM mode, or as BMC generic GPIO, or as LAN 1- 1000M LED Driver Output by default if SDRAM mode is not enabled.
NPECFG	I	**North PCI Express connections. For details, please see** "Pin Straps"**.**
SPECFG	I	**South PCI Express connections. For details, please see "Pin Straps"**
STRAP_[0:8]	I/O	**Strap pins. For details, please see** "Pin Straps"

2.27 Power and Ground

Table 2-31. Power and Ground Signals (Sheet 1 of 2)

Name	Description
V5REFSUS	**Reference for 5V STB Tolerance**: Used on resume well inputs (1 pin). This power is not expected to be shut off unless the system is unplugged.
VCC5REF	**Reference for 5V Tolerance**: Used on core well inputs (2 pins). This power is shut off in S3, S4 and S5 states.
VCCAESI	**ESI PLL Analog Power**: 1.5V, This power is shut off in S3, S4 and S5 states.
VCCBGESI	**Analog Power for ESI AFE Reference Circuitry**: 3.3V, this power is supplied with the core well.
VSSBGESI	**Analog GND for ESI AFE Reference Circuitry**
VCCAPLL	**SATA PLL Analog Power**: 1.5V, this power is supplied with the core well.
VCCARX	**SATA Rx Analog Power**: 1.5V, this power is supplied with the core well.
VCCATX	**SATA Tx Analog Power**: 1.5V, this power is supplied with the core well.
Vccasatabg	**Analog Power for SATA AFE Reference Circuitry**: 3.3V. This power is supplied with the core well
Vssasatabg	**Analog Ground for SATA AFE Reference Circuitry**
Vcc	**Power for Core**: 1.5V, This power is shut off in S3, S4 and S5 states.
Vss	**Ground**
VCCPCPU	**Power for CPU I/F Signals**: 1.0V to 1.55V. The power will be shut in S3, S4, and S5 states.
VCCPIDE	**Power for IDE Periphery**: 3.3V. This power will be shut in S3, S4, and S5 states.
VCCPPCI	**Power for PCI Periphery**: 3.3V. This power will be shut in S3, S4, and S5 states.

Table 2-31. Power and Ground Signals (Sheet 2 of 2)

Name	Description
VCCPRTC	**Supply for RTC Well** (1 pin). 3.3 V (can drop to 2.0 V min. in G3 state). This power is not expected to be shut off unless the RTC battery is removed or completely drained. Note: Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low. Clearing CMOS in an Intel® 631xESB/632xESB I/O Controller Hub-based platform can be done by using a jumper on RTCRST# or GPIO.
VCCPSUS	**Suspend Well IO Supply**: 3.3 V supply for resume well I/O buffers. This power is not expected to be shut off unless the system is unplugged.
VCCSUS[2:1]	**Suspend Well Core Supply**: 1.5V Standby. This must only be connected to an external 1.5V power supply when the Integrated VRM is disabled. This power is not expected to be shut unless the system is in a G3 state (unplugged in desktop).
VccUSB	**Power for USB AFE Logic:** 1.5V. This must only be connected to an external 1.5V power supply when the Integrated VRM is disabled. This power is supplied with the suspend well.
VccUSBCore	**Power for USB AFE Logic**: 1.5V. This power is supplied with core well.
VccpUSB	**Power for USB Output Drivers:** 3.3V. This power is supplied with the suspend well.
Vccaupll	**Analog Power for USB AFE PLL:** 1.5V. This power is supplied with the core well.
Vccaubg	**Analog Power for USB AFE Reference Circuitry:** 3.3V. This power is supplied with the suspend well.
Vssaubg	**Analog Ground for USB AFE Reference Circuitry**
Vccp25pci	**Power for PCI Periphery:** 2.5V. This supply will be shut in S3_Cold, S4 and S5 states. This power may be supplied by either an external regulator or by an internal regulator. This selection is determined by a strap that determines the source for both the 2.5V PCI and 2.5V IDE power planes together. The Intel® 631xESB/632xESB I/O Controller Hub consumes additional power on the Vccpide and Vccppci power planes (<30 mW) when the internal regulators are enabled. When disabled, the internal regulators draw negligible power (<1 mW)
Vccp25ide	**Power for IDE Periphery**: 2.5 V. This supply will be shut in S3_Cold, S4 and S5 states. This power may be supplied by either an external regulator or by an internal regulator. This selection is determined by a strap that determines the source for both the 2.5V PCI and 2.5V IDE power planes together. The Intel® 631xESB/632xESB I/O Controller Hub consumes additional power on the Vccpide and Vccppci power planes (<30 mW) when the internal regulators are enabled. When disabled, the internal regulators draw negligible power (<1mW)
VCC15	**1.5V PCI-X* IO supply**
VCC33	**3.3V PCI-X IO supply**
VCCAP1	**LBW PLL Analog Power**: supplied with1.5V core voltage
VCCAP3	**PCI-X PLL Analog Power**: supplied with1.5V core voltage
VCCAPE	**PCI Express PLL Analog Power**, supplied with1.5V core voltage
VREFPCI	**PCI VREF**: VREF reference voltage to the PCI pads
VCCBGPE	**PCI Express Bandgap Power**, supplied by 2.5V core voltage
VCCPE	**Power ESI/PCI Express Transmitter and Receiver:** 1.5 V supply for PCI Express and ESI logic. This power may be shut off in S3, S4 and S5 states.
VSSAPE	**PCI Express PLL Analog Ground**
VSSBGPE	**PCI Express Bandgap Ground**
VCCA3_3	**Serdes Bandgap Power: 3.3V AUX power**
VCCAPLL1_5	**Serdes PLL Analog Power: 1.5V AUX power**
VCCAUX1_5	**AUX Well: 1.5V AUX power**
VSS2	**Ground**
VCCAUX3_3	**BMC IO supply**: 3.3V AUX power
VCCSE	**Serdes IO Supply**: 1.5V AUX power
VSSA3_3	**Serdes Bandgap Ground**
VSSAPLL1_5	**Serdes PLL Analog Ground**

2.28 Pin Straps

The following signals are used for static configuration. They are sampled at the rising edge of PWROK to select configurations (except as noted), and then revert later to their normal usage. To invoke the associated mode, the signal should be driven at least four PCI clocks prior to the time it is sampled.

Table 2-32. Functional Strap Definitions (Sheet 1 of 3)

Signal	Usage	When Sampled	Comment
ACZ_SDOUT	1, XOR Chain Entrance 2, PCI Express Port Config Bit 1	Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP[0] pulled low at rising edge of PWROK. See Section 10 for XOR Chain functionality information. When TP[0] not pulled low at rising edge of PWROK, sets bit 1 of RPC.PC (Chipset Config Registers:Offset 224h). See Section 12.1.51 for details. This signal has a weak internal pull-down.
ACZ_SYNC	PCI Express Port Config Bit 0	Rising Edge of PWROK	Sets bit 0 of RPC.PC (Chipset Config Registers:Offset 224h). See Section 12.1.51 for details. This signal has a weak internal pull-down.
GNT[5]#/ GPO[17]#	Boot BIOS Destination Selection	Rising Edge of PWROK	Signal has a weak internal pull-up. Allows for select memory ranges to be forwarded out the PCI Interface as opposed to the Firmware Hub. When sampled high, destination is LPC. Also controllable via Boot BIOS Destination bit (Chipset Configuration Registers:Offset 3410h:bit 3)
GNT[6]#/ GPO[16]	Top-Block Swap Override	Rising Edge of PWROK	The signal has a weak internal pull-up. If the signal is sampled low, this indicates that the system is strapped to the “top-block swap” mode (Intel® 631xESB/632xESB I/O Controller Hub inverts A16 for all cycles targeting FWH BIOS space). The status of this strap is readable via the Top Swap bit (Chipset Configuration Registers:Offset 3414h:bit 0). Note that software will not be able to clear the Top-Swap bit until the system is rebooted without GNT6# being pulled down.
GPIO[25]	Integrated Vcc2_5 VRM Enable/Disable	Rising Edge of RSMRST#	Integrated VRMs are enabled when sampled low. Weak internal Pull-up during the RSMRST#. This pull-up is disabled within 100 ms after RSMRST# deasserts.
SPKR	No Reboot	Rising Edge of PWROK	The signal has a weak internal pull-down. If the signal is sampled high, this indicates that the system is strapped to the “No Reboot” mode (Intel® 631xESB/632xESB I/O Controller Hub will disable the TCO Timer system reboot feature). The status of this strap is readable via the NO REBOOT bit (Chipset Config Registers:Offset 3410h:bit 5).
HPX_SIC	Test Mode	Rising Edge of PXPWROK	1 = Normal operation 0 = Reserved
HPX_SID/ HXPCIXCAP1_2	Test Mode	Rising Edge of PXPWROK	1 = Reserved 0 = Normal operation

Table 2-32. Functional Strap Definitions (Sheet 2 of 3)

Signal	Usage	When Sampled	Comment
HPX_SLOT[2] HPX_SLOT[1]/ HXPRSNT1_1# HPX_SLOT[0]/ HXMRL_2#	Hot-Plug Mode / # of PCI Slots	Rising Edge of PXPWROK	Used in conjunction with HPX_SLOT[3] signal to determine PCI Hot-Plug Mode and number of PCI slots on a bus segment. HPX_SLOT[3:0] = Hot-Plug Mode Enable/Disable, # of PCI slots 0000 = Hot-Plug disabled, 1 slot (optional) 0001 = Hot-Plug disabled, 2 slots (optional) 0010 = Hot-Plug disabled, 3 slots (optional) 0011 = Hot-Plug disabled, 4 slots (optional) 0100 = Hot-Plug disabled, 5 slots (optional) 0101 = Hot-Plug disabled, 6 slots (optional) 0110 = Hot-Plug disabled, 7 slots (optional) 0111 = Hot-Plug disabled, 8 slots (optional) 1000 = Reserved 1001 = Hot-Plug enabled, 1 slot (parallel mode) 1010 = Hot-Plug enabled, 2 slots (parallel mode) 1011 = Hot-Plug enabled, 3 slots (serial mode) 1100 = Hot-Plug enabled, 4 slots (serial mode) 1101 = Hot-Plug enabled, 5 slots (serial mode) 1110 = Hot-Plug enabled, 6 slots (serial mode) 1111 = Hot-Plug enabled, 1 slot-no-glue (parallel mode)
HPX_SLOT[3]/ HXPWRLED1#	PCI/PCI-X* Hot-Plug Mode Enable/Disable	Rising Edge of PXPWROK	1 = Hot-Plug Mode Enabled 0 = Hot-Plug Mode Disabled
INTVRMEN	Integrated VccSus1_5 VRM Enable/Disable	Always	Enables integrated VccSus1_5 VRM when sampled high.
PX133EN	133 MHz PCI-X Enable / Disable	Rising Edge of PXPWROK	Only relevant when Hot-Plug Mode is disabled (HPX_SLOT[3] = 0) OR when in one-slot-no-glue Hot-Plug mode (HPX_SLOT[3:0] = 1111), AND when in PCI-X Mode (PxPCIXCAP = 1). Determines the maximum frequency (100 MHz or 133 MHz) of the PCI bus segment when in PCI-X Mode: 1 = 133 MHz PCI-X capable. 0 = 100 MHz PCI-X max bus frequency.
PXM66EN	PCI 66 MHz Enable / Disable	Rising Edge of PXPWROK	Only relevant when Hot-Plug Mode is disabled (HPX_SLOT[3] = 0) OR when in one-slot-no-glue Hot-Plug mode (HPX_SLOT[3:0] = 1111) AND when in conventional PCI mode (PXPCIXCAP = 0). Determines the maximum frequency (33 MHz or 66 MHz) of the PCI bus segment when in conventional PCI mode: 1 = 66 MHz capable when in conventional PCI mode. 0 = 33 MHz max frequency when in conventional PCI mode.
PASTRAP0	Test Mode	Rising Edge of PXPWROK	1 = Reserved 0 = Normal operation
SMBUS[5] SMBUS[3:1]	SMBus Addressing Straps	Rising Edge of PXPWROK	Sets the SMBus address. SMBus Addressing: Bit 7----------'1' Bit 6----------'1' Bit 5----------SMBUS[5] Bit 4----------'0' Bit 3---------- SMBUS[3] Bit 2---------- SMBUS[2] Bit 1---------- SMBUS[1]

Table 2-32. Functional Strap Definitions (Sheet 3 of 3)

Signal	Usage	When Sampled	Comment
NPECFG	North PCI Express connections	Rising Edge of PXPWROK	Selects north PCI Express port connectivity 0 = Configured as single x8 port or single x4 1 = Configured as two x4 ports -- Lanes 3:0 no change. -- Lanes 7:4 become new x4 port.
SPECFG	South PCI Express connections	Rising Edge of PXPWROK	Selects external south PCI Express port connectivity: 0 = Configured as one x8 port 1 = Configured as two x4 ports When the Intel® 631xESB/632xESB I/O Controller Hub south ports are put in x8 mode, PE1 lanes 3:0 stay the same, and PE2 lanes 3:0 become PE1 lanes 7:4.
SDP2[0],SDP2[1] (Note: for A0 silicon only)	JTAG function strapping	Rising Edge of PERST	SDP2[0] with default being high. When low, it allows only LAN JTAG to be tested. When high with SDP2[1] being high, LAN JTAG is allowed to be tested. When high with SDP2[1] being low, it doesn't allow LAN JTAG to be tested.
FLSH_SI, EE_DI (Note: for A1 and later silicon)	JTAG function strapping	Rising Edge of PERST	FLSH_SI. When low, it allows only LAN JTAG to be tested. When high with EE_DI being high, LAN JTAG is allowed to be tested. When high with EE_DI being low, it doesn't allow LAN JTAG to be tested.
STRAP_0	Test Mode	PERST#	**Strap Pin.** Need external pull-down in normal operation.
STRAP_1	Test Mode	PERST#	**Strap Pin.** Need external pull-up to Vaux in normal operation.
STRAP_2	Reference Clock	LAN_PWR_GOOD	**Strap Pin.** • Connect to GND via 1k ohm resistor for 62.5 MHz SER_CLK_IN (default) • Connect to VCCAUX3_3 via 10k ohm resistor for 25 MHz SER_CLK_IN
STRAP_3	Test Mode	LAN_PWR_GOOD	**Strap Pin.** Need external pull-down in normal operation.
STRAP_4	Reserved	N/A	**Strap Pin.** Pulled up to P1V5_ESB.
STRAP_5	Reserved	N/A	**Strap Pin.** Pulled up to P1V5_ESB.
STRAP_6	Reserved	N/A	**Strap Pin.** Pulled up to P1V5_AUX.
STRAP_7	Reserved	N/A	**Strap Pin.** Need external pull-up.
STRAP_8	Reserved	N/A	**Strap Pin.** Connected to ground, 0 Ohm resistor.

2.29 Intel® 631xESB/632xESB I/O Controller Hub Revision and Device ID Table

Table 2-33. Intel® 631xESB/632xESB I/O Controller Hub Revision and Device ID Table (Sheet 1 of 2)

Device Function	Function Description	Intel® 631xESB/632xESB I/O Controller Hub Dev ID	Intel® 631xESB/632xESB I/O Controller Hub A0 Rev ID	Intel® 631xESB/632xESB I/O Controller Hub A1 Rev ID	Comments
B0:D30:F0	PCI to PCI bridge	244Eh	D8h	D9h	
B0:D30:F2	AC'97 Audio	2698h	08h	09h	
B0:D30:F3	AC'97 modem	2699h	08h	09h	
B0:D31:F0	LPC interface	267xh	08h	09h	2670h-267Fh3
B0:D31:F1	PATA controller	269Eh	08h	09h	
B0:D31:F2	SATA controller as IDE	2680h	08h	09h	D31F2 can be one of four types of HBA depending on device ID
B0:D31:F2	SATA controller as SATA	2681h	08h	09h	
B0:D31:F2	SATA controller as RAID 0/1/5	2682h	08h	09h	
B0:D31:F2	SATA controller as RAID 0/1	2683h	08h	09h	
B0:D31:F3	SMBus controller	269Bh	08h	09h	
B0:D27:F0	High Definition Audio Controller	269Ah	08h	09h	
B0:D28:F0	PCI Express port 1	269xh	08h	09h	FDPCI Express1 = 0, 2690h; FDPCI Express1 = 1, 2691h
B0:D28:F1	PCI Express port 2	269xh	08h	09h	FDPCI Express1 = 0, 2692h; FDPCI Express1 = 1, 2693h
B0:D28:F2	PCI Express port 3	269xh	08h	09h	FDPCI Express1 = 0, 2694h; FDPCI Express1 = 1, 2695h
B0:D28:F3	PCI Express port 4	269xh	08h	09h	FDPCI Express1 = 0, 2696h; FDPCI Express1 = 1, 2697h
B0:D29:F0	USB 1.1 port 0,1	2688h	08h	09h	
B0:D29:F1	USB 1.1 port 2,3	2689h	08h	09h	
B0:D29:F2	USB 1.1 port 4,5	268Ah	08h	09h	
B0:D29:F3	USB 1.1 port 6,7	268Bh	08h	09h	
B0:D29:F7	USB2 host controller	268xh	08h	09h	268Ch-268Fh2
Bm:D0:F0	PCI Express upstream port	See comments	00h	01h	3500h - 3503h[4]
Bm:D0:F1	I/OxAPIC controller	See comments	00h	01h	3504h - 3507h[4]
Bm:D0:F3	PCI Express-to-PCI-X Bridge	See comments	00h	01h	350Ch - 350Fh[4]

Table 2-33. Intel® 631xESB/632xESB I/O Controller Hub Revision and Device ID Table (Sheet 2 of 2)

Device Function	Function Description	Intel® 631xESB/632xESB I/O Controller Hub Dev ID	Intel® 631xESB/632xESB I/O Controller Hub A0 Rev ID	Intel® 631xESB/632xESB I/O Controller Hub A1 Rev ID	Comments
Bp:D0:F0	PCI Express downstream port E1	See comments	00h	01h	3510h - 3513h[4]
Bp:D1:F0	PCI Express downstream port E2	See comments	00h	01h	3514h - 3517h[4]
Bp:D2:F0	PCI Express downstream port E3	See comments	00h	01h	3518h -351Bh[4]
Bn:D0:F0	LAN 0/LAN 1 Controller	See comments	00h	01h	See Section 25 for LAN Controller configuration information.
Bn:D0:F1	LAN 0/LAN 1 Controller	See comments	00h	01h	
Bn:D0:F2	IDE Redirection Controller	See comments	00h	01h	
Bn:D0:F3	Serial Port Redirection Controller	See comments	00h	01h	
Bn:D0:F4	IPMI/KCS0	See comments	00h	01h	
Bn:D0:F5	UHCI Redirection Controller	See comments	00h	01h	
Bn:D0:F7	BT Controller	See comments	00h	01h	

Note:
1. PCI Express Device ID: This bit is mapped directly to bit [0] of the PCI Express ports Device ID register (ID.DID), located at Device 28, Functions 0 - 3.
2. USB2 Device ID: These bits are mapped directly to bits [1:0] of the USB2 host controller Device ID register (ID.DID), located at Device 29, Function 7.
3. LPC Device ID: These bits are mapped directly to bits [3:0] of LPC Device ID registers (ID.DID), located at Device 31, Function 0 (LPC bridge).
4. See Section 13 for PCI Express Bridge/Switch configuration information.

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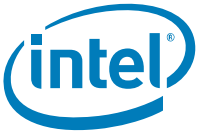


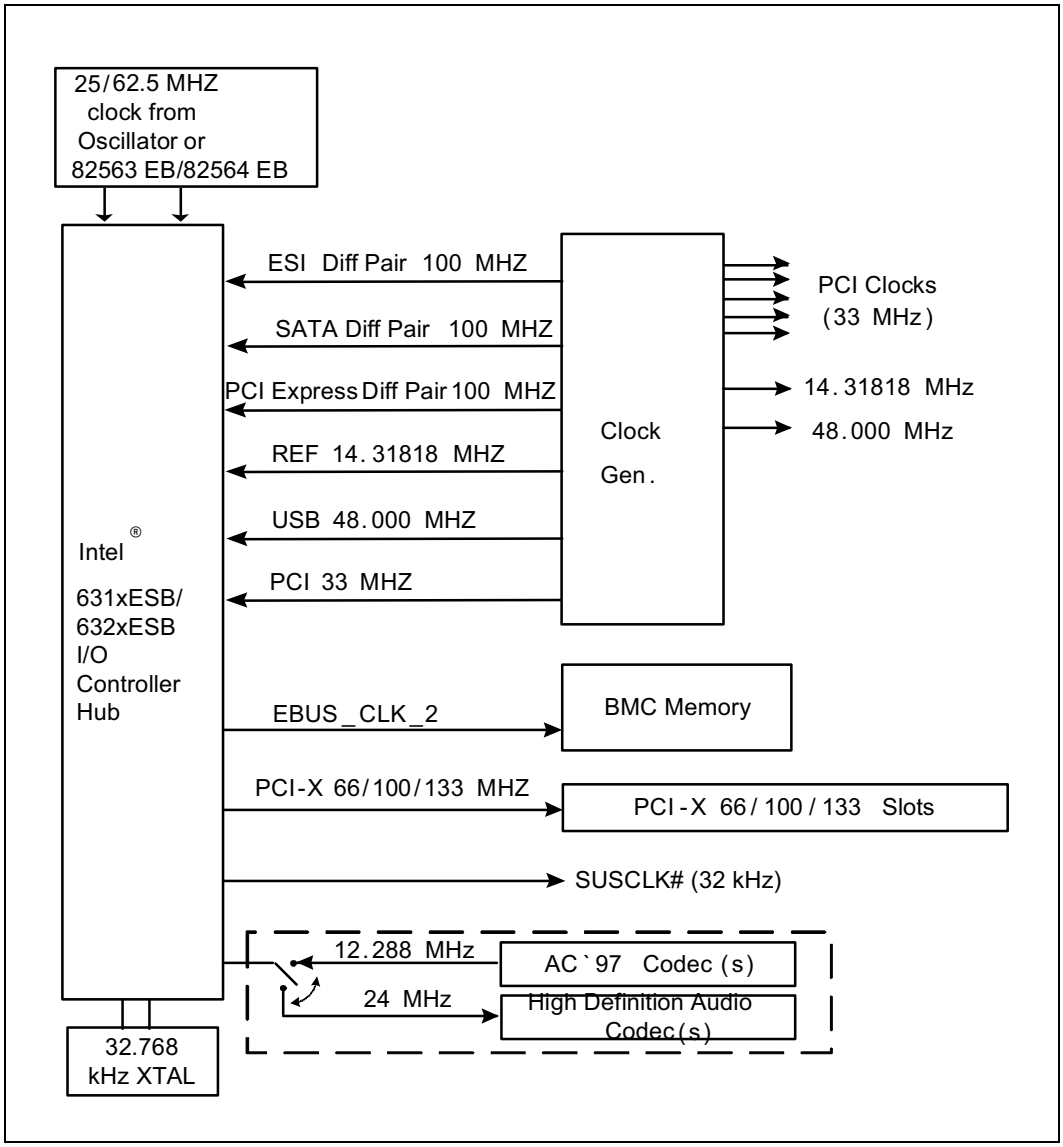
3 Intel® 631xESB/632xESB I/O Controller Hub and System Clock Domains

Table 3-1 shows the system clock domains. For complete details of the system clocking solution, refer to the system's clock generator component specification.

Table 3-1. Intel® 631xESB/632xESB I/O Controller Hub and System Clock Domains

Clock Domain	Frequency	Source	Usage
ESB2 ACZ_BIT_CLK	12.288 MHz	AC'97 Codec	AC-link. Generated by AC'97 Codec. Can be shut by codec in D3. Expected to be shut off during S3 or below. ***Note:*** For use only in AC '97 mode.
ESB2 CLK14	14.31818 MHz	Main Clock Generator	Used for ACPI timer and Multimedia Timers. Expected to be shut off during S3 or below.
ESB2 CLK48	48.000 MHz	Main Clock Generator	Super I/O, USB controllers. Expected to be shut off during S3 or below.
ESB2 ESI_CLKP, ESI_CLKN	100 MHz	Main Clock Generator	Differential clock pair used for ESI.
ESB2 PCICLK	33 MHz	Main Clock Generator	Free-running PCI Clock to Intel® 631xESB/632xESB I/O Controller Hub. This clock remains on during S0 and S1 state, and is expected to be shut off during S3 or below.
ESB2 PECLKP PECLKN	100 MHz	Main Clock Generator	PCI Express Upstream Port Clock.
ESB2 PXPCLKO[6:0] PXPCLKI	33/66/100/ 133 MHz	Intel® 631xESB /632xESB I/O Controller Hub	PCI/PCI-X Interface Clocks.
ESB2 SATA_CLKP, SATA_CLKN	100 MHz	Main Clock Generator	Differential clock pair used for SATA.
ESB2 SER_CLK_IN	25/62.5 MHz	PHY or external Oscillator	Kumeran/SERDES Interface. The LAN and MMS are clocked with clocks that are generated from this clock
System PCI	33 MHz	Main Clock Generator	PCI Bus, LPC I/F. These only go to external PCI and LPC devices.
ESB2 EBUS_CLK_2	125 MHZ	Intel® 631xESB /632xESB I/O Controller Hub	125 MHz clock output for SDRAM

Figure 3-1. Conceptual System Clock Diagram



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4 Intel® 631xESB/632xESB I/O Controller Hub Pin States

4.1 Integrated Pull-Ups and Pull-Downs

Table 4-1. Integrated Pull-Up and Pull-Down Resistors (Sheet 1 of 4)

Signal	Resistor Type	Nominal Value (Ohm)	Notes
DD[7]	Pull-down	11.5K	1
DDREQ	Pull-down	11.5K	1
GNT[3:0]#	Pull-up	20K	2, 3
GNT[4]# / GPIO[48]	Pull-up	20K	2, 3
GNT[5]# / GPO[17]	Pull-up	20K	2
GNT[6]# / GPO[16]	Pull-up	20K	2
PME#	Pull-up	20K	2
FWH[3:0]/LAD[3:0]	Pull-up	20K	2
LDRQ[0]#	Pull-up	20K	2
LDRQ[1]#/GPI[41]	Pull-up	20K	2
ACZ_BIT_CLK, AC '97	Pull-down	20K	5, 6, 8
ACZ_RST#, AC '97	Pull-down	20K	4, 6, 8
ACZ_SDIN[2:0], AC '97	Pull-down	20K	4, 8
ACZ_SDOUT, AC '97	Pull-down	20K	4, 7, 8
ACZ_SYNC, AC '97	Pull-down	20K	4, 7, 8
ACZ_BIT_CLK, High Definition Audio	Pull-down	20K	5, 8, 9
ACZ_RST#, High Definition Audio	None	N/A	8
ACZ_SDIN[2:0], High Definition Audio	Pull-down	20K	4, 8
ACZ_SDOUT, High Definition Audio	Pull-down	20K	8
ACZ_SYNC, High Definition Audio	Pull-down	20K	4, 8
PWRBTN#	Pull-up	20K	2
SPKR	Pull-down	20K	4
TP[0]	Pull-up	20K	10
GPIO[25]	Pull-up	20K	2, 11
USBP[7:0][P,N]	Pull-down	15K	12
HPX_PRST#/HPX_RST1#	Pull-up	8.33K	13
HPX_RST2#	Pull-up	8.33K	13
HPX_SIL#	Pull-up	8.33K	13
HPX_SOD	Pull-up	8.33K	13
HPX_SOL	Pull-up	8.33K	13

Table 4-1. Integrated Pull-Up and Pull-Down Resistors (Sheet 2 of 4)

Signal	Resistor Type	Nominal Value (Ohm)	Notes
HPX_SOLR	Pull-up	8.33K	13
HXATNLED_1#	Pull-up	8.33K	13
HXPWREN_1	Pull-up	8.33K	13
PXGNT[0]#	Pull-up	8.33K	13
PXGNT[1]#	Pull-up	8.33K	13
PXGNT[2]#	Pull-up	8.33K	13
PXGNT[3]#/HXPWREN_2	Pull-up	8.33K	13
PXGNT[4]#/HXBUSEN_2#	Pull-up	8.33K	13
PXGNT[5]#/HXBUSEN_1#	Pull-up	8.33K	13
PXIRDY#	Pull-up	8.33K	13
PXIRQ[0]#	Pull-up	8.33K	13
PXIRQ[1]#	Pull-up	8.33K	13
PXIRQ[10]#	Pull-up	8.33K	13
PXIRQ[11]#	Pull-up	8.33K	13
PXIRQ[12]#	Pull-up	8.33K	13
PXIRQ[13]#	Pull-up	8.33K	13
PXIRQ[14]#	Pull-up	8.33K	13
PXIRQ[15]#	Pull-up	8.33K	13
PXIRQ[2]#	Pull-up	8.33K	13
PXIRQ[3]#	Pull-up	8.33K	13
PXIRQ[4]#	Pull-up	8.33K	13
PXIRQ[5]#	Pull-up	8.33K	13
PXIRQ[6]#	Pull-up	8.33K	13
PXIRQ[7]#	Pull-up	8.33K	13
PXIRQ[8]#	Pull-up	8.33K	13
PXIRQ[9]#	Pull-up	8.33K	13
PXPAR	Pull-up	8.33K	13
PXPAR64	Pull-up	8.33K	13
PXPERR#	Pull-up	8.33K	13
PXPLOCK#	Pull-up	8.33K	13
PXREQ[0]#	Pull-up	8.33K	13
PXREQ[1]#	Pull-up	8.33K	13
PXREQ[2]#	Pull-up	8.33K	13
PXREQ[3]#	Pull-up	8.33K	13
PXREQ[4]#/HXPRSNT2_2#	Pull-up	8.33K	13
PXREQ[5]#/HXPRSNT1_2#	Pull-up	8.33K	13
PXREQ64#	Pull-up	8.33K	13
PXSERR#	Pull-up	8.33K	13
PXSTOP#	Pull-up	8.33K	13
PXTRDY#	Pull-up	8.33K	13
EXTINTR#	Pull-up	8.33K	13
TDI	Pull-up	20K	16

Table 4-1. Integrated Pull-Up and Pull-Down Resistors (Sheet 3 of 4)

Signal	Resistor Type	Nominal Value (Ohm)	Notes
TRST#	Pull-up	20K	16
TMS	Pull-up	20K	16
SMBD0	Pull-up	20K	17
SMBCLK0	Pull-up	20K	17
FLBSD0	Pull-up	20K	17
FLBSINTEX0	Pull-up	20K	17
SMBD1	Pull-up	20K	14
SMBCLK1	Pull-up	20K	14
FLBSD1	Pull-up	20K	14
FLBSINTEX1	Pull-up	20K	14
SMBD2	Pull-up	20K	15, 16
SMBCLK2	Pull-up	20K	15, 16
SMBALRT_2	Pull-up	20K	15, 16
SMBD3	Pull-up	20K	15, 16
SMBCLK3	Pull-up	20K	15, 16
SMBALRT_3	Pull-up	20K	15, 16
SMBD4	Pull-up	20K	15, 16
SMBCLK4	Pull-up	20K	15, 16
SMBALRT_4	Pull-up	20K	15, 16
RS232_CTS	Pull-up	20K	15, 16
RS232_DCD	Pull-up	20K	15, 16
RS232_DSR	Pull-up	20K	15, 16
RS232_DTR	Pull-up	20K	15, 16
RS232_RI	Pull-up	20K	15, 16
RS232_RTS	Pull-up	20K	15, 16
RS232_SIN	Pull-up	20K	15, 16
RS232_SOUT	Pull-up	20K	15, 16
EBUS_AD[24:16]	Pull-up	20K	15, 16
EBUS_AD[15:0]	Pull-up	20K	15, 16
EBUS_ADV#/EBUS_RAS#	Pull-up	20K	15, 16
EBUS_ALAT/EBUS_CKE	Pull-up	20K	15, 16
EBUS_BE_[1:0]#	Pull-up	20K	15, 16
EBUS_CE_[2:1]#	Pull-up	20K	15, 16
EBUS_FRST#	Pull-up	20K	15, 16
EBUS_OE#/EBUS_CAS#	Pull-up	20K	15, 16
EBUS_WE#	Pull-up	20K	15, 16
SDP0[2:0]	Pull-up	20K	15, 16
SDP1[2:0]	Pull-up	20K	15, 16
SDP2[7:0]	Pull-up	20K	15, 16
LAN0_DIS#	Pull-up	20K	15, 16
LAN1_DIS#	Pull-up	20K	15, 16
SDP3_0/LED0_0	Pull-up	20K	15, 16

Table 4-1. Integrated Pull-Up and Pull-Down Resistors (Sheet 4 of 4)

Signal	Resistor Type	Nominal Value (Οηµ)	Notes
SDRAM_AD12/SPD3_1/ LED0_1	Pull-up	20K	15, 16
SDRAM_BA0/SDP3_2/LED0_2	Pull-up	20K	15, 16
SDRAM_BA1/SDP3_3/LED0_3	Pull-up	20K	15, 16
SDP3_4/LED1_0	Pull-up	20K	15, 16
SDRAM_A9/SDP3_5/LED1_1	Pull-up	20K	15, 16
SDRAM_A10/SDP3_6/LED1_2	Pull-up	20K	15, 16
SDRAM_A11/SDP3_7/LED1_3	Pull-up	20K	15, 16
STRAP_2	Pull-up	20K	15, 16
ESB2_TEST2	Pull-up	20K	15, 16
PXCBE[7:0]	Pull-up	8.33K	13

Notes:
1. Simulation data shows that these resistor values can range from 5.7k Ohm to 28.3k Ohm.
2. Simulation data shows that these resistor values can range from 15k Ohm to 35k Ohm.
3. The internal pull-up is enabled only when the PCIRST# pin is driven low and the PWROK indication is high.
4. Simulation data shows that these resistor values can range from 9k Ohm to 50k Ohm.
5. Simulation data shows that these resistor values can range from 10k Ohm to 40k Ohm.
6. The pull-down resistors on ACZ_BIT_CLK (AC '97) and ACZ_RST# are enabled when either:
   - The LSO bit (bit 3) in the AC'97 Global Control Register (D30:F2:2C) is set to 1, or
   - Both Function 2 and Function 3 of Device 30 are disabled.

   Otherwise, the integrated Pull-down resistor is disabled.
7. The pull-down resistors on ACZ_SYNC (AC '97) and ACZ_SDOUT (AC '97) are enabled during reset and also enabled when either:
   - The LSO bit (bit 3) in the AC'97 Global Control Register (D30:F2:2C) is set to 1, or
   - Both Function 2 and Function 3 of Device 30 are disabled.

   Otherwise, the integrated Pull-down resistor is disabled.
8. The AC '97/High Definition Audio Link signals may either all be configured to be an AC-Link or an High Definition Audio Link.
9. The pull-down on this signal (in Intel High Definition Audio mode) is only enabled when in S3Cold.
10. Simulation data shows that these resistor values can range from 10k Ohm to 30k Ohm.
11. GPIO[25] transitions from pulled high internally to actively driven to '1' following the deassertion of the RSMRST# pin. This transition must be glitch-free.
12. Simulation data shows that these resistor values can range from 14.25k Ohm to 24.8k Ohm
13. ±40%.
14. These pull-up registers are controlled by the FML1PUEN field in the GSCR register of the MMS auxiliary space (0x0F00:23).
15. Note that the pullup is active only when the signal is in input mode. In output mode, the pullup resistor is disconnected inside Intel® 631xESB/632xESB I/O Controller Hub. These signal do not need motherboard pullups
16. Simulation data shows that these resistor values can range from 15.3k Ohm to 29.7k Ohm.
17. These pull-up registers are controlled by the FML0PUEN field in the GSCR register of the MMS auxiliary space (0x0F00:22).

4.2 IDE Integrated Series Termination Resistors

Table 4-2 shows the Intel® 631xESB/632xESB I/O Controller Hub IDE signals that have integrated series termination resistors.

Table 4-2. IDE Series Termination Resistors

Signal	Integrated Series Termination Resistor Value
DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	Approximately 33Ω (See Note)

Note: Simulation data indicates that the integrated series termination resistors are nominally 33Ω but can range from 21Ω to 75Ω.

4.3 Output and I/O Signals Planes and States

Table 4-3 shows the power plane associated with the output and I/O signals, as well as the state at various times. Within the table, the following terms are used:

"High-Z" Tri-state. Intel® 631xESB/632xESB I/O Controller Hub not driving the signal high or low.

"High" Intel® 631xESB/632xESB I/O Controller Hub is driving the signal to a logic 1

"Low" Intel® 631xESB/632xESB I/O Controller Hub is driving the signal to a logic 0

"Defined" Driven to a level that is defined by the function (will be high or low)

"Undefined" Intel® 631xESB/632xESB I/O Controller Hub is driving the signal, but the value is indeterminate.

"Running" Clock is toggling or signal is transitioning because function not stopping

"Off" The power plane is off, so Intel® 631xESB/632xESB I/O Controller Hub is not driving

Note that the signal levels are the same in S4 and S5, except as noted.

Table 4-3. Power Plane and States for Output and I/O Signals for Intel® 631xESB/632xESB I/O Controller Hub (Sheet 1 of 6)

Signal Name	Power Plane	During PLTRST#[4] / RSMRST#[5]	Immediately after PLTRST#[4] / RSMRST#[5]	S1	S3	S4/S5
PCI Express*						
PE0TP[3:0] PE0TN[3:0]	Vcc1_5	High	High10	Defined	Off	Off
PE1TP[3:0] PE1TN[3:0]	Vcc1_5	High	High10	Defined	Off	Off
PE2TP[3:0] PE2TN[3:0]	Vcc1_5	High	High10	Defined	Off	Off
PCI Bus						
AD[31:0]	Vcc33	Low	Undefined	Defined	Off	Off
C/BE[3:0]#	Vcc33	Low	Undefined	Defined	Off	Off
DEVSEL#	Vcc33	High-Z	High-Z	High-Z	Off	Off

Table 4-3. Power Plane and States for Output and I/O Signals for Intel® 631xESB/632xESB I/O Controller Hub (Sheet 2 of 6)

Signal Name	Power Plane	During PLTRST#[4] / RSMRST#[5]	Immediately after PLTRST#[4] / RSMRST#[5]	S1	S3	S4/S5
FRAME#	Vcc33	High-Z	High-Z	High-Z	Off	Off
GNT[4:0]#	Vcc33	High with Internal Pull-ups	High	High	Off	Off
GNT[5]#/GPO[17]	Vcc33	High-Z with Internal Pull-up	High	High	Off	Off
GNT[6]#/GPO[16]	Vcc33	High-Z with Internal Pull-up	High	High	Off	Off
IRDY#, TRDY#	Vcc33	High-Z	High-Z	High-Z	Off	Off
PAR	Vcc33	Low	Undefined	Defined	Off	Off
PCIRST#	VCCPSUS	Low	High	High	Low	Low
PERR#	Vcc33	High-Z	High-Z	High-Z	Off	Off
PLOCK#	Vcc33	High-Z	High-Z	High-Z	Off	Off
STOP#	Vcc33	High-Z	High-Z	High-Z	Off	Off
PCI-X* Bus						
HxATNLED_1#	3.3V	High-Z	Pulled High	Pulled High	Off	Off
HxPWREN_1	3.3V	High-Z	Pulled High	Pulled High	Off	Off
HPX_PRST#/ HPX_RST1#	3.3V	High	High	High	Off	Off
HPx_RST2#	3.3V	High-Z	High	High	Off	Off
HPxSOC	3.3V	High-Z	Pulled High	Pulled High	Off	Off
HPxSOD	3.3V	High-Z	Pulled High	Pulled High	Off	Off
HPxSOL	3.3V	High-Z	Pulled High	Pulled High	Off	Off
HPxSOLR	3.3V	Undefined	Pulled High	Pulled High	Off	Off
PxACK64#	3.3V/1.5V	High-Z	Pulled High	Pulled High	Off	Off
PxAD[63:0]	3.3V/1.5V	High-Z	Pulled High	Pulled High	Off	Off
PxCBE_[7]#	3.3V/1.5V	High-Z	Pulled High	Pulled High	Off	Off
PxCBE_[6]#	3.3V/1.5V	High-Z	Pulled High	Pulled High	Off	Off
PxCBE_[5]#	3.3V/1.5V	High-Z	Pulled High	Pulled High	Off	Off
PxCBE_[4]#	3.3V/1.5V	High-Z	Pulled High	Pulled High	Off	Off
PxCBE_[3]#	3.3V/1.5V	High-Z	Pulled High	Pulled High	Off	Off
PxCBE_[2]#	3.3V/1.5V	High-Z	Pulled High	Pulled High	Off	Off
PxCBE_[1]#	3.3V/1.5V	High-Z	Pulled High	Pulled High	Off	Off
PxCBE_[0]#	3.3V/1.5V	High-Z	Pulled High	Pulled High	Off	Off
PxDEVSEL#	3.3V	High-Z	Pulled High	Pulled High	Off	Off
PxFRAME#	3.3V	High-Z	Pulled High	Pulled High	Off	Off
PxGNT_[5]#	3.3V	High	Pulled High	Pulled High	Off	Off
PxGNT_[4]#	3.3V/1.5V	High	Pulled High	Pulled High	Off	Off
PxGNT_[3]#	3.3V/1.5V	High	Pulled High	Pulled High	Off	Off
PxGNT_[2]#	3.3V/1.5V	High	Pulled High	Pulled High	Off	Off
PxGNT_[1]#	3.3V	High	Pulled High	Pulled High	Off	Off

Table 4-3. Power Plane and States for Output and I/O Signals for Intel® 631xESB/632xESB I/O Controller Hub (Sheet 3 of 6)

Signal Name	Power Plane	During PLTRST#[4] / RSMRST#[5]	Immediately after PLTRST#[4] / RSMRST#[5]	S1	S3	S4/S5
PxGNT_[0]#	3.3V	High	Pulled High	Pulled High	Off	Off
PxIRDY#	3.3V	High-Z	Pulled High	Pulled High	Off	Off
PxM66EN	3.3V	High-Z	Undefined	Undefined	Off	Off
PxPAR	3.3V/1.5V	High-Z	Pulled High	Pulled High	Off	Off
PxPAR64	3.3V/1.5V	High-Z	Pulled High	Pulled High	Off	Off
PxPERR#	3.3V	High-Z	Pulled High	Pulled High	Off	Off
PxPLOCK#	3.3V	High-Z	Pulled High	Pulled High	Off	Off
PxREQ_[5]#	3.3V/1.5V	High-Z	Pulled High	Pulled High	Off	Off
PxREQ64#	3.3V/1.5V	High-Z	Pulled High	Pulled High	Off	Off
PxSTOP#	3.3V	High-Z	Pulled High	Pulled High	Off	Off
PxTRDY#	3.3V	High-Z	Pulled High	Pulled High	Off	Off
SDTA	3.3V	High-Z	High-Z	High-Z	Off	Off
LPC Interface						
LAD[3:0] / FWH[3:0]	Vcc33	High	High	High	Off	Off
LFRAME# / FWH[4]	Vcc33	High	High	High	Off	Off
IDE Interface						
DA[2:0]	Vcc33	Undefined	Undefined	Undefined	Off	Off
DCS1#, DCS3#	Vcc33	High	High	High	Off	Off
DD[15:8], DD[6:0]	Vcc33	High-Z	High-Z	High-Z	Off	Off
DD[7]	Vcc33	Low	Low	Low	Off	Off
DDACK#	Vcc33	High	High	High	Off	Off
DIOR#, DIOW#	Vcc33	High	High	High	Off	Off
SATA Interface						
SATA[5:0]TXP SATA[5:0]TXN	Vcc33	High-Z	High-Z	Defined	Off	Off
SATALED#	Vcc33	High-Z	High-Z	Defined	Off	Off
SATARBIAS	Vcc33	High-Z	High-Z	High-Z	Off	Off
Interrupts						
PIRQ[A:H]#	Vcc33	High-Z	High-Z	High-Z	Off	Off
SERIRQ	Vcc33	High-Z	High-Z	High-Z	Off	Off
USB Interface						
USBP[7:0][P,N]	VCCPSUS	Low	Low	Low	Low	Low
USBRBIAS	VCCPSUS	High-Z	High-Z	Defined	Defined	Defined
Power Management						
PLTRST#	VCCPSUS	Low	High	High	Low	Low
SLP_S3#	VCCPSUS	Low	High	High	Low	Low
SLP_S4#	VCCPSUS	Low	High	High	High	Low

Table 4-3. Power Plane and States for Output and I/O Signals for Intel® 631xESB/632xESB I/O Controller Hub (Sheet 4 of 6)

Signal Name	Power Plane	During PLTRST#[4] / RSMRST#[5]	Immediately after PLTRST#[4] / RSMRST#[5]	S1	S3	S4/S5
SLP_S5#	VCCPSUS	Low	High	High	High	Low[8]
SUS_STAT#	VCCPSUS	Low	High	High	Low	Low
SUSCLK	VCCPSUS	Low	Running			
Processor Interface						
A20M#	V_CPU_IO	See Note 1	See Note 1	High	Off	Off
CPUPWRGD	V_CPU_IO	See Note 3	High-Z	High-Z	Off	Off
CPUSLP#	V_CPU_IO	High	High	Defined	Off	Off
IGNNE#	V_CPU_IO	See Note 1	See Note 1	High	Off	Off
INIT#	V_CPU_IO	High	High	High	Off	Off
INIT3_3V#	Vcc33	High	High	High	Off	Off
INTR	V_CPU_IO	See Note 6	See Note 6	Low	Off	Off
NMI	V_CPU_IO	See Note 6	See Note 6	Low	Off	Off
SMI#	V_CPU_IO	High	High	High	Off	Off
STPCLK#	V_CPU_IO	High	High	Low	Off	Off
SMBus Interface						
SMBCLK, SMBDATA	VCCPSUS	High-Z	High-Z	Defined	Defined	Defined
SCLK, SDTA	Vcc33	High-Z	High-Z	Defined	Defined	Defined
FLBSD[1:0] FLBSINTEX[1:0]	VCCAUX3_3	High-Z	High-Z	Defined	Defined	Defined
SMBCLK[4:0] SMBD[4:0]	VCCAUX3_3	High-Z	High-Z	Defined	Defined	Defined
System Management Interface						
SMLINK[1:0]	VCCPSUS	High-Z	High-Z	Defined	Defined	Defined
LINKALERT#	VCCPSUS	High-Z	High-Z	Defined	Defined	Defined
Flash and EEPROM Interface[12]						
FLSH_SI	VccAUX3_3	Defined	Defined	Defined	Defined	Defined
FLSH_SCK	VccAUX3_3	Defined	Defined	Defined	Defined	Defined
FLSH_CE#	VccAUX3_3	Defined	Defined	Defined	Defined	Defined
EE_SK	VccAUX3_3	Defined	Defined	Defined	Defined	Defined
EE_DI	VccAUX3_3	Defined	Defined	Defined	Defined	Defined
EE_CS#	VccAUX3_3	Defined	Defined	Defined	Defined	Defined
Kumeran Interface Signals						
SETP0	VccAUX3_3	Defined	Defined	Defined	Defined	Defined
SETN0	VccAUX3_3	Defined	Defined	Defined	Defined	Defined
SETP1	VccAUX3_3	Defined	Defined	Defined	Defined	Defined
SETN1	VccAUX3_3	Defined	Defined	Defined	Defined	Defined
SERCOMPO	VccAUX3_3	Defined	Defined	Defined	Defined	Defined

Table 4-3. Power Plane and States for Output and I/O Signals for Intel® 631xESB/632xESB I/O Controller Hub (Sheet 5 of 6)

Signal Name	Power Plane	During PLTRST#[4] / RSMRST#[5]	Immediately after PLTRST#[4] / RSMRST#[5]	S1	S3	S4/S5
Expansion Bus Interface[12]						
EBUS_AD[8:0]	VccAUX3_3	Defined	Defined	Defined	Defined	Defined
EBUS_AD[24:9]	VccAUX3_3	Defined	Defined	Defined	Defined	Defined
EBUS_WE#	VccAUX3_3	Defined	Defined	Defined	Defined	Defined
EBUS_OE#/ EBUS_CAS#	VccAUX3_3	Defined	Defined	Defined	Defined	Defined
EBUS_CE1#	VccAUX3_3	Defined	Defined	Defined	Defined	Defined
EBUS_CE2#	VccAUX3_3	Defined	Defined	Defined	Defined	Defined
EBUS_BE0#	VccAUX3_3	Defined	Defined	Defined	Defined	Defined
EBUS_BE1#	VccAUX3_3	Defined	Defined	Defined	Defined	Defined
EBUS_CLK2	VccAUX3_3	Defined	Defined	Defined	Defined	Defined
EBUS_ADV#/ EBUS_RAS#	VccAUX3_3	Defined	Defined	Defined	Defined	Defined
EBUS_FRST#	VccAUX3_3	Defined	Defined	Defined	Defined	Defined
EBUS_ALAT/ EBUS_CKE	VccAUX3_3	Defined	Defined	Defined	Defined	Defined
R-232 Interface Signals						
RS232_DTR	VccAUX3_3	Defined	Defined	Defined	Defined	Defined
RS232_SOUT	VccAUX3_3	Defined	Defined	Defined	Defined	Defined
Miscellaneous Signals						
SPKR	Vcc33	High-Z with Internal Pull-down	Low	Defined	Off	Off
SDP0[2:0]	VccAUX3_3	Defined	Defined	Defined	Defined	Defined
SDP1[2:0]	VccAUX3_3	Defined	Defined	Defined	Defined	Defined
SDP2[7:0]	VccAUX3_3	Defined	Defined	Defined	Defined	Defined
SDP3_0/LED0_0	VccAUX3_3	Defined	Defined	Defined	Defined	Defined
SDRAM_AD12/ SPD3_1/LED0_1	VccAUX3_3	Defined	Defined	Defined	Defined	Defined
SDRAM_BA0/ SDP3_2/LED0_2	VccAUX3_3	Defined	Defined	Defined	Defined	Defined
SDRAM_BA1/ SDP3_3/LED0_3	VccAUX3_3	Defined	Defined	Defined	Defined	Defined
SDP3_4/LED1_0	VccAUX3_3	Defined	Defined	Defined	Defined	Defined
SDRAM_A9/ SDP3_5/LED1_1	VccAUX3_3	Defined	Defined	Defined	Defined	Defined
SDRAM_A10/ SDP3_6/LED1_2	VccAUX3_3	Defined	Defined	Defined	Defined	Defined
SDRAM_A11/ SDP3_7/LED1_3	VccAUX3_3	Defined	Defined	Defined	Defined	Defined
AC'97 Interface						
ACZ_RST#	VCCPSUS	Low	Low	Cold Reset Bit (High)	Low	Low
ACZ_SDOUT	Vcc33	Low	Running	Low	Off	Off

Table 4-3. Power Plane and States for Output and I/O Signals for Intel® 631xESB/632xESB I/O Controller Hub (Sheet 6 of 6)

Signal Name	Power Plane	During PLTRST#[4] / RSMRST#[5]	Immediately after PLTRST#[4] / RSMRST#[5]	S1	S3	S4/S5
ACZ_SYNC	Vcc33	Low	Running	Low	Off	Off
Intel® High Definition Audio Interface						
ACZ_RST#	VCCPSUS	Low	Low[9]	High	Low	Low
ACZ_SDOUT	Vcc33	High-Z with Internal Pull-down	Running	Low	Off	Off
ACZ_SYNC	Vcc33	High-Z with Internal Pull-down	Running	Low	Off	Off
ACZ_BIT_CLK	Vcc33	High-Z with Internal Pull-down	Low9	Low	Off	Off
Unmuxed GPIO Signals						
GPO[18]	Vcc33	High	See Note 1	Defined	Off	Off
GPO[19]	Vcc33	High	High	Defined	Off	Off
SCLK/GPO[20]11	Vcc33	Undefined	Toggling	Defined	Off	Off
SLOAD/GPO[21]11	Vcc33	Undefined	Low	Defined	Off	Off
SDATAOUT0/ GPO[23]11	Vcc33	Undefined	Low	Defined	Off	Off
GPIO[24]	VCCPSUS	High	High	Defined	Defined	Defined
GPIO[25]	VCCPSUS	High	High2	Defined	Defined	Defined
GPIO[28:27]	VCCPSUS	High	High	Defined	Defined	Defined
SDATAOUT1/ GPIO[32]11	Vcc33	Undefined	Low	Defined	Off	Off
GPIO[34:33]	Vcc33	High	High	Defined	Off	Off

Notes:

1. Intel® 631xESB/632xESB I/O Controller Hub drives these signals Low before PWROK rising and High after the CPU Reset.
2. GPO[18] will toggle at a frequency of approximately 1 Hz when the Intel® 631xESB/632xESB I/O Controller Hub comes out of reset.
3. CPUPWRGD is an open-drain output that represents a logical AND of the Intel® 631xESB/632xESB I/O Controller Hub's VRMPWRGD and PWROK signals, and thus will be driven low by Intel® 631xESB/632xESB I/O Controller Hub when either VRMPWRGD or PWROK are inactive. During boot, or during a hard reset with power cycling, CPUPWRGD will be expected to transition from low to High-Z.
4. The states of Vcc33 signals are taken at the times During PLTRST# and Immediately after PLTRST#.
5. The states of VCCPSUS signals are taken at the times During RSMRST# and Immediately after RSMRST#.
6. Intel® 631xESB/632xESB I/O Controller Hub drives these signals Low before PWROK rising and Low after the CPU Reset.
7. GPIO[25] transitions from pulled high internally to actively driven following the deassertion of the RSMRST# pin.
8. SLP_S5# signals will be high in the S4 state.
9. Low until Intel High Definition Audio Controller Reset bit set (D27:F0:Offset HDBAR+08h:bit 0), at which time ACZ_RST# will be High and ACZ_BIT_CLK will be Running.
10. PETp/n[4:1] high until port is enabled by software.
11. SDATAOUT0/GPO[23], SDATAOUT1/GPIO[32], SLOAD/GPO[21SCLK/GPO[20], requires 2K Ohm external pull-up.
12. Since all the BMC related interfaces (Flash, EEPROM and Expansion Bus) resident on the standby power rail, they are expected to be active at all states and thus have no default values at any of the states listed in the table. All signal's status is driven by BIOS or software.

4.4 Power Planes for Input Signals

Table 4-4 shows the power plane associated with each input signal, as well as what device drives the signal at various times. Valid states include:

- High
- Low
- Static: Will be high or low, but will not change
- Driven: Will be high or low, and is allowed to change
- Running: For input clocks

Table 4-4. Power Plane for Input Signals for Intel® 631xESB/632xESB I/O Controller Hub (Sheet 1 of 3)

Signal Name	Power Well	Driver During Reset	S1	S3	S4/S5
A20GATE	Vcc33	External Microcontroller	Static	Low	Low
ACZ_BIT_CLK (AC '97 Mode)	Vcc33	AC'97 Codec	Low	Low	Low
ACZ_SDIN[2:0] (AC '97 Mode)	VCCPSUS	AC'97 Codec	Low	Low	Low
ACZ_SDIN[2:0] (Intel High Definition Audio Mode)	VCCPSUS	Intel High Definition Audio Codec	Low	Low	Low
CLK14	Vcc33	Clock Generator	Running	Low	Low
CLK48	Vcc33	Clock Generator	Running	Low	Low
DDREQ	Vcc33	IDE Device	Static	Low	Low
ESICLK100P, ESICLK100N	Vcc33	Clock Generator	Running	Low	Low
FERR#	V_CPU_IO	Processor	Static	Low	Low
GPI[6]	Vcc33	External Device or External Pull-up/Pull-down	Driven	Off	Off
GPI[7]	Vcc33	External Device or External Pull-up/Pull-down	Driven	Off	Off
GPI[8]	VCCPSUS	External Device or External Pull-up/Pull-down	Driven	Driven	Driven
PE0RP[3:0], PE0RN[3:0]	Vcc1_5	PCI Express Device	Driven	Driven	Driven
PE1RP[3:0], PE1RN[3:0]	Vcc1_5	PCI Express Device	Driven	Driven	Driven
PE2RP[3:0], PE2RN[3:0]	Vcc1_5	PCI Express Device	Driven	Driven	Driven
IDEIRQ	Vcc33	IDE	Static	Low	Low
INTRUDER#	VccRTC	External Switch	Driven	Driven	Driven
INTVRMEN	VccRTC	External Pull-up or Pull-down	Driven	Driven	Driven
IORDY	Vcc33	IDE Device	Static	Low	Low
SER_CLK_IN	VccAUX3_3	External Phy or XTAL	Running	Running	Running
LAN_PWR_GOOD	VccAUX3_3	External Logic	High	High	High
FLSH_SO	VccAUX3_3	External serial flash	Driven	Driven	Driven
EE_DO	VccAUX3_3	External EEPROM	Driven	Driven	Driven

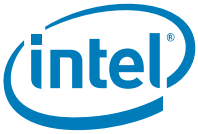
Table 4-4. Power Plane for Input Signals for Intel® 631xESB/632xESB I/O Controller Hub (Sheet 2 of 3)

Signal Name	Power Well	Driver During Reset	S1	S3	S4/S5
SERP0	VccAUX3_3	82563EB/82564EB Dual/ Single-PHY device	Driven	Driven	Driven
SERN0	VccAUX3_3	82563EB/82564EB Dual/ Single-PHY device	Driven	Driven	Driven
SERP1	VccAUX3_3	82563EB/82564EB Dual/ Single-PHY device	Driven	Driven	Driven
SERN1	VccAUX3_3	82563EB/82564EB Dual/ Single-PHY device	Driven	Driven	Driven
LINK_0	VccAUX3_3	Fiber transceiver	Driven	Driven	Driven
LINK_1	VccAUX3_3	Fiber transceiver	Driven	Driven	Driven
SEICOMPI	VccAUX3_3	Circuit on board (Internal Pull-up)	Driven	Driven	Driven
RS232_CTS	VccAUX3_3	External RS232 device	Driven	Driven	Driven
RS232_DCD	VccAUX3_3	External RS232 device	Driven	Driven	Driven
RS232_DSR	VccAUX3_3	External RS232 device	Driven	Driven	Driven
RS232_RI	VccAUX3_3	External RS232 device	Driven	Driven	Driven
RS232_SIN	VccAUX3_3	External RS232 device	Driven	Driven	Driven
LDRQ[0]#	Vcc33	LPC Devices	High	Low	Low
LDRQ[1]#	Vcc33	LPC Devices	High	Low	Low
OC[7:0]#	VCCPSUS	External Pull-ups	Driven	Driven	Driven
PCICLK	Vcc33	Clock Generator	Running	Low	Low
PME#	VCCPSUS	Internal Pull-up	Driven	Driven	Driven
PWRBTN#	VCCPSUS	Internal Pull-up	Driven	Driven	Driven
PWROK	VccRTC	System Power Supply	Driven	Low	Low
RCIN#	Vcc33	External Microcontroller	High	Low	Low
REQ[6:0]#	Vcc33	PCI Master	Driven	Low	Low
RI#	VCCPSUS	Serial Port Buffer	Driven	Driven	Driven
RSMRST#	VccRTC	External RC Circuit	High	High	High
RTCRST#	VccRTC	External RC Circuit	High	High	High
SATA_CLKP, SATA_CLKN	Vcc33	Clock Generator	Running	Low	Low
SATA[5:0]RXP SATA[5:0]RXN	Vcc33	SATA Drive	Driven	Driven	Driven
SATARBIAS#	Vcc33	External Pull-down	Driven	Driven	Driven
SATA[5:0]GP/ GPI[13, 12, 31:29, 26]	Vcc33	External Device or External Pull-up/Pull-down	Driven	Driven	Driven
SERR#	Vcc33	PCI Bus Peripherals	High	Low	Low
SMBALERT#	VCCPSUS	External Pull-up	Driven	Driven	Driven
SYS_RESET#	VCCPSUS	External Circuit	Driven	Driven	Driven
THRM#	Vcc33	Thermal Sensor	Driven	Low	Low
THRMTRIP#	V_CPU_IO	Thermal Sensor	Driven	Low	Low
TP[0]	VCCPSUS	External Pull-up	High	High	High
USBRBIAS#	VCCPSUS	External Pull-down	Driven	Driven	Driven
VRMPWRGD	Vcc33	Processor Voltage Regulator	High	Low	Low

Table 4-4. Power Plane for Input Signals for Intel® 631xESB/632xESB I/O Controller Hub (Sheet 3 of 3)

Signal Name	Power Well	Driver During Reset	S1	S3	S4/S5
WAKE#	VCCPSUS	External Pull-up	Driven	Driven	Driven
HPx_SIC	3.3V	High-Z	Undefined	Low	Low
HPx_SID	3.3V	High-Z	Undefined	Low	Low
HPx_SIL#	3.3V	High-Z	Pulled High	Low	Low
HPxSLOT[3]	3.3V	High-Z	Undefined	Low	Low
HPxSLOT[2]	3.3V	High-Z	Undefined	Low	Low
HPxSLOT[1]	3.3V	High-Z	Undefined	Low	Low
HPxSLOT[0]	3.3V	High-Z	Undefined	Low	Low
Px133EN	3.3V	High-Z	Undefined	Low	Low
PxIRQ_[15]#	3.3V	High-Z	Pulled High	Low	Low
PxIRQ_[14]#	3.3V	High-Z	Pulled High	Low	Low
PxIRQ_[13]#	3.3V	High-Z	Pulled High	Low	Low
PxIRQ_[12]#	3.3V	High-Z	Undefined	Low	Low
PxIRQ_[11]#	3.3V	High-Z	Undefined	Low	Low
PxIRQ_[10]#	3.3V	High-Z	Pulled High	Low	Low
PxIRQ_[9]#	3.3V	High-Z	Pulled High	Low	Low
PxIRQ_[8]#	3.3V	High-Z	Pulled High	Low	Low
PxIRQ_[7]#	3.3V	High-Z	Pulled High	Low	Low
PxIRQ_[6]#	3.3V	High-Z	Pulled High	Low	Low
PxIRQ_[5]#	3.3V	High-Z	Pulled High	Low	Low
PxIRQ_[4]#	3.3V	High-Z	Pulled High	Low	Low
PxIRQ_[3]#	3.3V	High-Z	Pulled High	Low	Low
PxIRQ_[2]#	3.3V	High-Z	Pulled High	Low	Low
PxIRQ_[1]#	3.3V	High-Z	Pulled High	Low	Low
PxIRQ_[0]#	3.3V	High-Z	Pulled High	Low	Low
PxPCIXCAP	3.3V	High-Z	Pulled High	Low	Low
PxPME#	3.3V	High-Z	Undefined	Low	Low
PxREQ_[4]#	3.3V	High-Z	Pulled High	Low	Low
PxREQ_[3]#	3.3V	High-Z	Pulled High	Low	Low
PxREQ_[2]#	3.3V	High-Z	Pulled High	Low	Low
PxREQ_[1]#	3.3V	High-Z	Pulled High	Low	Low
PxREQ_[0]#	3.3V	High-Z	Pulled High	Low	Low
PxSERR#	3.3V	High-Z	Pulled High	Low	Low
PxSTRAP0	3.3V	High-Z	Pulled Low	Low	Low
SCLK	3.3V	High-Z	High-Z	Low	Low
SMBUS[5]	3.3V	High-Z	Undefined	Low	Low
SMBUS[3]	3.3V	High-Z	Undefined	Low	Low
SMBUS[2]	3.3V	High-Z	Undefined	Low	Low
SMBUS[1]	3.3V	High-Z	Undefined	Low	Low

§§



5 Functional Description

This chapter describes the functions and interfaces of the Intel® 631xESB/632xESB I/O Controller Hub.

Intel® 631xESB/632xESB I/O Controller Hub support configurations are one x8 Balanced configuration and two x4 connection as LAN Centric configuration (as Figure 5-1and Figure 5-2 show).

Figure 5-1. Intel® 631xESB/632xESB I/O Controller Hub Device Diagram – Balanced

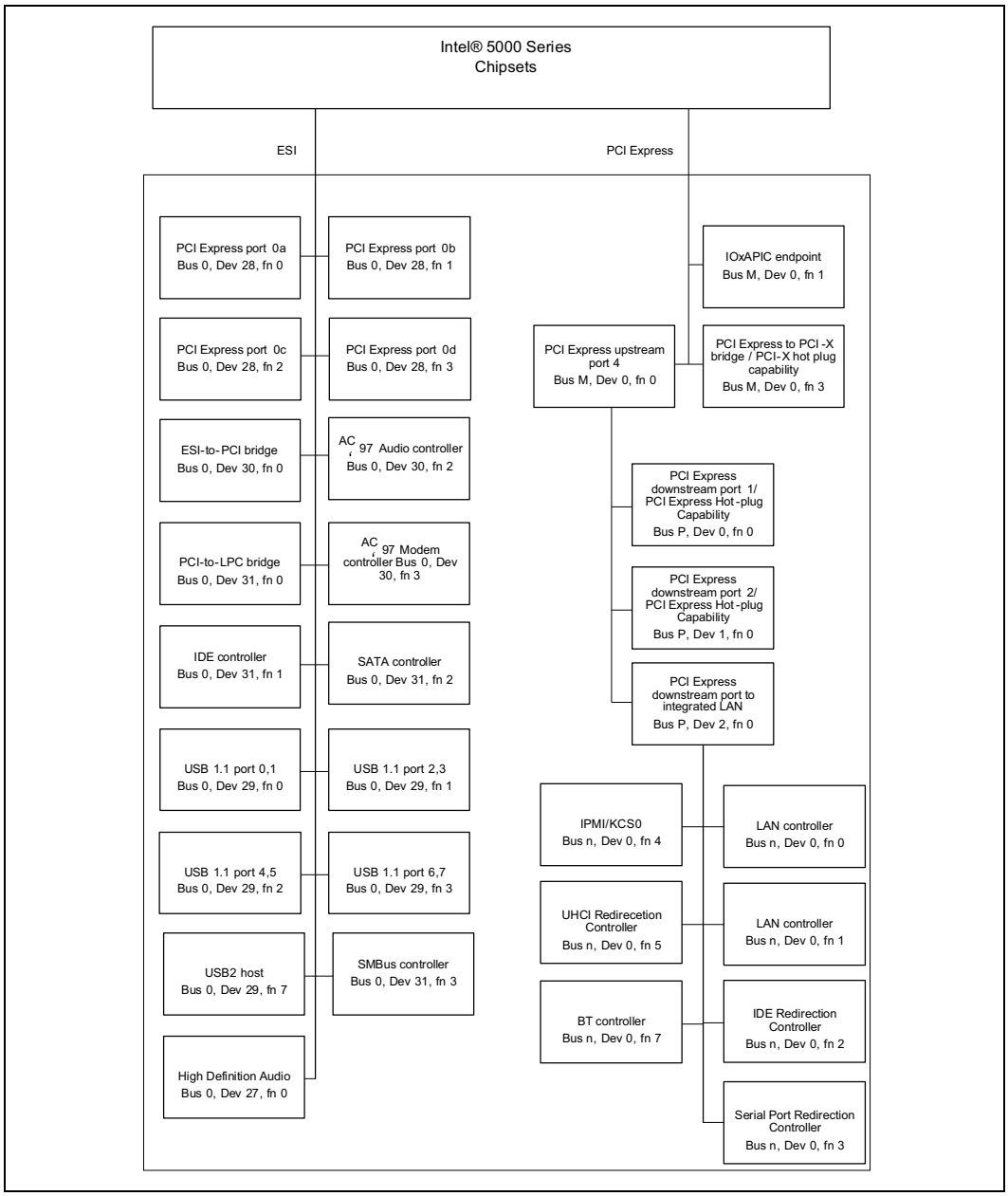
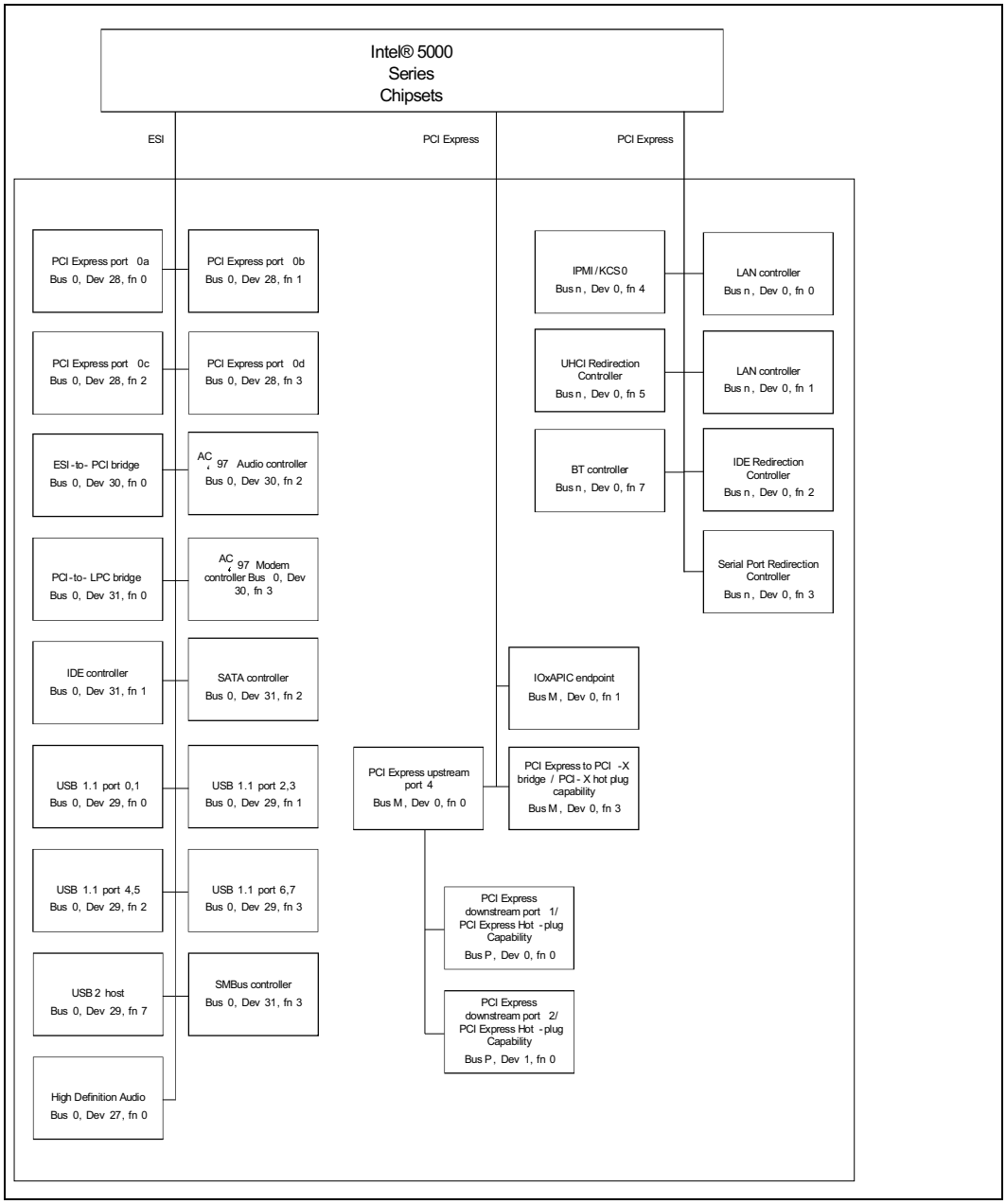


Figure 5-2. Intel® 631xESB/632xESB I/O Controller Hub Device Diagram – LAN Centric



As shown below, Intel® 631xESB/632xESB I/O Controller Hub configurations are determined with power-on strapping.

Table 5-1. Strap Values for Each Configuration

Configuration	NPECFG
LAN BW Centric Configuration	1
Balanced Configuration	0

5.1 PCI Express* Bridge, Switch, and Endpoints

As Figure 5-1 and Figure 5-2 show, Intel® 631xESB/632xESB I/O Controller Hub couples on its 'south' interfaces to three individual x4 PCI Express links (one is the internal link for Intel® 631xESB/632xESB I/O Controller Hub LAN controller, the other two external links may be combined into a single x8 link by using a strapping pin during reset. Refer to Section 2.28) and to one 64-bit PCI/PCI-X secondary bus interface.

Intel® 631xESB/632xESB I/O Controller Hub 'north' PCI Express interface is the logical primary bus, the physical PCI-X bus segment becomes a separate secondary bus with a PCI Express to PCI-X bridge corresponding to Function 3. The upstream PCI Express port provides the link to another secondary PCI bus with a PCI Express switch model. The Standard Hot -Plug Controller (SHPC) associated with the PCI-X bus segment appears as a capability of the PCI Express to PCI-X Bridge. The I/OxAPIC controller resides as a separate PCI Express function.

- **PCI Express Upstream port (Bm:D0:F0)**. Intel® 631xESB/632xESB I/O Controller Hub implements a upstream PCI Express port that provides the link to another secondary PCI bus with a PCI Express switch model.
- **PCI Express Downstream ports (Bp:D0:F0, Bp:D1:F0, Bp:D2:F0)**. Intel® 631xESB/632xESB I/O Controller Hub implements a downstream PCI Express port that provides the link to another secondary PCI bus with a PCI Express switch model. Intel® 631xESB/632xESB I/O Controller Hub integrates three individual x4 PCI Express links on this secondary PCI bus (Bp:D2:F0 are internally link for Intel® 631xESB/632xESB I/O Controller Hub LAN controllers and BMC functions, Bp:D0:F0, Bp:D1:F0 are for external links)
- **I/OxAPIC Devices (Bm:D0:F1)**. Intel® 631xESB/632xESB I/O Controller Hub implements a variation of the APIC known as the I/OxAPIC. It resides on the primary bus.
- **Standard Hot-Plug Controller (Bm:D0:F3)**. Intel® 631xESB/632xESB I/O Controller Hub supports a single SHPC controller. This Standard Hot-Plug Controller appears as a capability of its associated PCI Express to PCI-X Bridge.
- **PCI Express to PCI-X Bridge (Bm:D0:F3)**. Intel® 631xESB/632xESB I/O Controller Hub implements the buffering and control logic between the PCI Express and the PCI-X buses. The PCI bus arbitration is handled by these PCI devices. The PCI decoder in this device must decode the ranges for PCI Express to the MCH. This register set also provides support for Reliability, Availability, and Serviceability (RAS).

5.1.1 PCI Express* Upstream Ports

5.1.1.1 Features

The following list summarizes some of the features of the Intel® 631xESB/632xESB I/O Controller Hub PCI Express Upstream ports:

- Full interoperability with Intel® 5000 Series Chipsets
- Raw bit-rate on the data pins of 2.5 Gbit/s, resulting in a raw bandwidth per pin of 250 MB/s
- x8, x4 modes of operation
- Maximum realized bandwidth (in x8 mode) on PCI Express interface is 2 GB/s in each direction simultaneously, for an aggregate of 4 GB/s
- Pleisochronous operation with automatic clock extraction and phase correction

- Hierarchical PCI configuration mechanism for downstream devices
- Full 64-bit inbound addressing supported as defined by PCI Express specifications
- 64-bit outbound addressing support (that is, capability to generate DAC transactions on PCI)
- Forwarding of relaxed ordering PCI-X transaction attribute by way of PCI Express Relaxed Ordering Type 1 ordering attribute feature
- Forwarding of non-snooped PCI-X transaction attribute by way of a non-snooped PCI Express attribute
- Full-speed self-test and diagnostic (IBIST) functionality
- Automatic link initialization, configuration and re-training out of reset
- Runtime detection and recovery for loss of link synchronization
- 32-bit CRC (cyclic redundancy checking) covering all transmitted data packets
- 16 bit CRC on all link message information
- Hardware link-level retry to recover from transient errors without system failure (software transparent)
- Support for non-addressable electrical repeater devices in-line on any link to increase routing distances
- Support of in-band power management event, RAS error, boot interrupt, and component reset signaling
- Support of MSI and SAPIC interrupt messaging over PCI Express
- VC#0 only support. No ISOC support
- No support for beacon

5.1.2 PCI Express* to PCI-X* Bridge (Bm:D0:F3)

Intel® 631xESB/632xESB I/O Controller Hub implements the buffering and control logic between the PCI Express and the PCI-X buses. The PCI bus arbitration is handled by these PCI devices. The PCI decoder in this device must decode the ranges for PCI Express to the MCH. This register set also provides support for Reliability, Availability, and Serviceability (RAS).

The north PCI Express interface is the logical primary bus. The physical PCI-X bus segment becomes a separate secondary bus with a PCI Express to PCI-X Bridge.

5.1.2.1 Features of PCI-X* Interface

- PCI Spec rev 2.3 compliant
- PCI-X 1.0b spec compliant
- 64-bit 66 MHz, 3.3 V NOT 5 V tolerant
- 2-level programmable round-robin internal arbiter with MTT
- Six external REQ/GNT pairs for internal arbiter, but only three pairs are available when operating SHPC in parallel mode
- PCI clock-feed support from an external source for asynchronous primary and secondary domain operation
- Programmable bus parking on either the last agent or always on Intel® 631xESB/632xESB I/O Controller Hub

- On-die termination of 8.33 K ohms @ 40%
- 64-bit addressing, inbound and outbound and support for DAC command
- Outbound LOCK# support
- No inbound LOCK# support
- PCI fast Back-to-Back capable as target
- Up to 4 active and 4 pending inbound PCI-X memory read transactions and up to 2 outbound delayed (memory read, I/O read and write and Configuration read and write) transaction
- Tunable inbound read prefetch algorithm for PCI MRM/MRL commands
- NO Device ID Messaging (DIM) support
- NO Interface low power state support
- NO ECC Support

5.1.2.2 Features of Hot-Plug Interface

- *PCI Standard Hot-Plug Controller Specification Rev 1.0* compliant
- Dedicated controller for PCI(X) bus segment
- Support for 6 slots maximum
- Parallel mode operation for 1 and 2 slot systems. Slot interface logic not needed.
- Serial mode operation for other systems with Hot-Plug slots from 3 to 6. Slot interface logic needed to serialize and de-serialize information from Intel® 631xESB/632xESB I/O Controller Hub.
- 1-slot-no-glue parallel mode operation when the number of slots controlled is one and there are no other devices on the PCI bus. No on-board Q-Switches are needed for bus isolation in this mode
- In-box and out-of-box PCI Express system solution support with firmware initialization of the Hot-Plug controller. There is NO PROM/Pin-Strap support in Intel® 631xESB/632xESB I/O Controller Hub for PCI Express slot/cabled-out-of-box applications.
- ACPI support for Intel® 631xESB/632xESB I/O Controller Hub-SHPC with in-band PCI Express messaging

5.1.2.3 Initialization

When Hot-Plug is enabled (HPX_SLOT[3]=1) for a PCI segment in this mode, Intel® 631xESB/632xESB I/O Controller Hub always powers up in the 33 MHz PCI mode regardless of the capabilities of the cards and the bus segment. BIOS would then initialize the bus to the proper mode and frequency at POST. When Hot-Plug is disabled (HPX_SLOT[3]=0) for a PCI segment, Intel® 631xESB/632xESB I/O Controller Hub samples the M66EN, PCIXCAP, MODE2, M266EN and the PX133EN pins, to determine the mode and frequency of operation. Intel® 631xESB/632xESB I/O Controller Hub uses the encoding table (Table 5-2) for the M66EN, PCIXCAP and PX133EN pins, to set the mode and frequency of operation. ‘DC’ in the table below refers to a don’t care function and VCC refers to 3.3 V.

Table 5-2. M66EN, PCIXCAP, And PX133EN Pin Encoding Table

M66EN	PCIXCAP	PX133EN	PCI Bus Mode	PCI Bus Frequency
Hot-Plug Enabled				
DC	DC	DC	PCI	33 MHz
Hot-Plug Disabled				
GND	< 0.11VCC	DC	PCI	33 MHz
VCC	< 0.11VCC	DC	PCI	66 MHz
DC	< 0.89VCC & > 0.11VCC	DC	PCI-X*	66 MHz
DC	> 0.89VCC	GND	PCI-X	100 MHz
DC	> 0.89VCC	VCC	PCI-X	133 MHz

Once Intel® 631xESB/632xESB I/O Controller Hub identifies the capabilities of the PCI bus devices, it drives the initialization pattern on DEVSEL#, STOP#, TRDY#, FRAME# and IRDY# pins per Table 5-3 to initialize the PCI bus devices to the proper mode and frequency. The patterns shown in the table below are guaranteed to be stable on the rising edge of PCIRST# pin. Refer to the PCI specifications for details of the timing of these patterns with respect to the PCIRST# pin.

Table 5-3. PCI-X* Initialization Pattern Driven by Intel® 631xESB/632xESB I/O Controller Hub

DEVSEL#	STOP#	TRDY#	Mode	Clock Period (ns)		Clock Freq (MHz)	
				Max	Min	Min	Max
Deasserted	Deasserted	Deasserted	PCI		30	0	33
			PCI	30	15	33	66
Deasserted	Deasserted	Asserted	PCI-X* Mode1	20	15	50	66
Deasserted	Asserted	Deasserted	PCI-X Mode1	15	10	66	100
Deasserted	Asserted	Asserted	PCI-X Mode1	10	7.5	100	133

Note: Intel® 631xESB/632xESB I/O Controller Hub never drives these patterns on the rising edge of PCIRST# signal. These patterns could though appear before the signals settle to a steady value at the rising edge of PCIRST#.

5.1.2.4 Transactions Supported

5.1.2.4.1 PCI Mode

The table below lists all the transactions supported by Intel® 631xESB/632xESB I/O Controller Hub on the PCI bus. Note that PCI command encodings that do not correspond to the transactions listed below are ignored by Intel® 631xESB/632xESB I/O Controller Hub. Intel® 631xESB/632xESB I/O Controller Hub supports full 64-bit addressing inbound and outbound. This implies that Intel® 631xESB/632xESB I/O Controller Hub as a target can accept dual address cycles and as a Master can generate dual address cycles.

Table 5-4. PCI Transactions Supported

Transaction	C/BE[3:0]# Encoding	Master	Target
Interrupt acknowledge	0000	No	No
Special cycle (PCI Express Type1-to-Special Cycle)	0001	Yes	No
I/O read	0010	Yes	No
I/O write	0011	Yes	No
Memory read	0110	Yes	Yes
Memory write	0111	Yes	Yes
Configuration Read	1010	Yes	No
Configuration Write	1011	Yes	No
Memory Read Multiple	1100	No	Yes
Dual Address Cycle	1101	Yes	Yes
Memory Read Line	1110	No	Yes
Memory Write and Invalidate	1111	No	Yes
LOCK Transaction	-	Yes	No

5.1.2.4.2 PCI-X* Mode

The table below lists the transactions that Intel® 631xESB/632xESB I/O Controller Hub supports when the PCI interface is in the PCI-X mode. PCI-X commands that are not any of the commands listed in the table are ignored by Intel® 631xESB/632xESB I/O Controller Hub. Intel® 631xESB/632xESB I/O Controller Hub supports the PCI-X memory block write command in support of DMA writes from PCI Express. This is new in Intel® 631xESB/632xESB I/O Controller Hub.

Table 5-5. PCI-X* Transactions Supported (Sheet 1 of 2)

Transaction	Encoding	Master	Target	Length (Bytes Max)	
				Master	Target
Interrupt acknowledge	0000	No	No	N/A	N/A
Special cycle (PCI Express Type1-to-Special Cycle)	0001	Yes	No	4[1]	N/A
I/O read	0010	Yes	No	41	41
I/O write	0011	Yes	No	41	41
DeviceID Message	0101	No	No	N/A	N/A
Memory Read DWORD	0110	Yes	Yes	4	4
Memory Write	0111	Yes	Yes	128	4K
Alias to Memory Read Block	1000	No	Yes	N/A	4K
Alias to Memory Write Block	1001	No	Yes	N/A	4K
Configuration Read	1010	Yes	No	41	42
Configuration Write	1011	Yes	No	41	42
Split Completion	1100	Yes	Yes	4K	1283
Dual Address Cycle	1101	Yes	Yes	-	-

Table 5-5. PCI-X* Transactions Supported (Sheet 2 of 2)

Transaction	Encoding	Master	Target	Length (Bytes Max)	
				Master	Target
Memory Read Block	1110	Yes	Yes	128[3]	4K
Memory Write Block	1111	Yes	Yes	128[3]	4K
LOCK Transaction	-	Yes	No	-	-

Notes:
1. Naturally aligned DWORD lengths.
2. Naturally aligned DWORD lengths.
3. Naturally aligned to 128 byte address boundaries.

5.1.2.5 PCI-X* Hot-Plug Controller

The following list summarizes some of the features of the Intel® 631xESB/632xESB I/O Controller Hub PCI Express Upstream interface:

- *PCI Standard Hot-Plug Controller Specification Rev 1.0* compliant
- Support for 6 slots maximum
- Parallel mode operation for 1 and 2 slot systems. Slot interface logic not needed.
- Serial mode operation for other systems with Hot-Plug slots from 3 to 6. Slot interface logic needed to serialize and de-serialize information from Intel® 631xESB/632xESB I/O Controller Hub
- 1-slot-no-glue parallel mode operation when the number of slots controlled is one and there are no other devices on the PCI bus. No on-board Q-Switches are needed for bus isolation in this mode
- In-box and out-of-box PCI Express system solution support with firmware initialization of the Hot-Plug controller. There is NO PROM/Pin-Strap support in Intel® 631xESB/632xESB I/O Controller Hub for PCI Express slot/cabled-out-of-box applications
- ACPI support for Intel® 631xESB/632xESB I/O Controller Hub-SHPC with in-band PCI Express messaging

5.1.2.5.1 Introduction

Intel® 631xESB/632xESB I/O Controller Hub integrates a standard Hot-Plug controller for the PCI-X port that is compliant with the *PCI Standard Hot-Plug Controller Specification Revision 1.0.* This standard applies to both PCI and PCI-X modes of operation. The new standard is motivated by the concept that standardization of more features of the PCI Hot-Plug specification will reduce both the cost of hardware and software development time. Differences between the PCI Hot-Plug model and the standard Hot-Plug model include standardization of the following features:

- Power and attention indicators
- Manually-operated Retention Latch (MRL)
- MRL Sensor
- S/W Programming model
- Slot Numbering
- Attention button

A new register set is defined for the SHPC Capabilities List and the SHPC Working Register Set. The new registers are defined as a PCI-PCI bridge capability in the PCI-X configuration registers and not as a separate PCI controller device. The new specification also fixes the architectural proximity of the SHPC function to the PCI slots it controls. Per the new specification, the Intel® 631xESB/632xESB I/O Controller Hub may control slots only on its secondary bus and there must be a separate SHPC capability associated with the logical PCI-PCI bridge configuration space, the standard Hot-Plug controller being a capability of the PCI-PCI bridge. For details on the operation of the standard Hot-Plug controller, refer to the *PCI Standard Hot-Plug Controller Specification Revision 1.0*.

5.1.2.5.2 System Architecture

The PCI/ PCI-X Standard Hot-Plug Controller in Intel® 631xESB/632xESB I/O Controller Hub can control a maximum of 6 slots in the system. The interface between Intel® 631xESB/632xESB I/O Controller Hub and the Hot-Plug system board logic could be either serial or parallel. In the serial mode of operation, external glue logic is needed to interface Intel® 631xESB/632xESB I/O Controller Hub to the Hot-Plug slot side interface. In parallel mode, there is no glue logic needed and Intel® 631xESB/632xESB I/O Controller Hub directly controls and receives status from the slot control interface, one set of signals per slot. Intel® 631xESB/632xESB I/O Controller Hub supports parallel mode only when the number of Hot-Plug slots is either one or two.

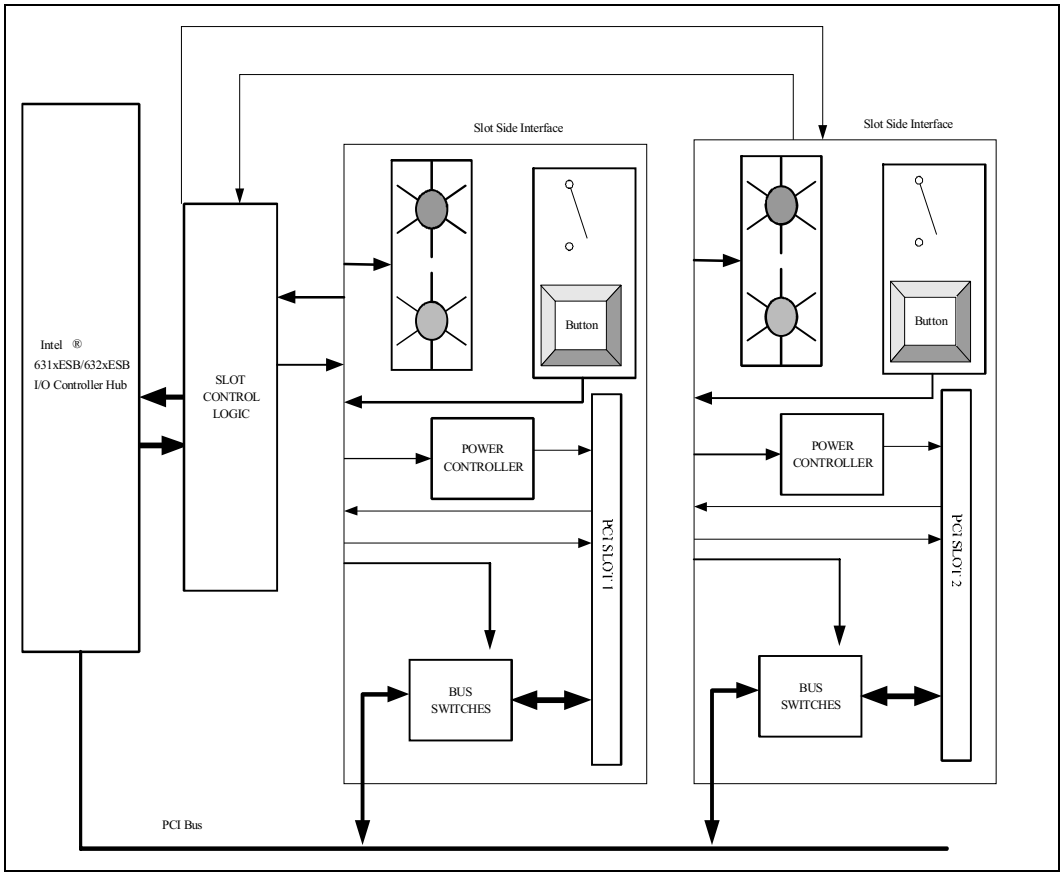
If the number of Hot-Plug slots is greater than two, then Intel® 631xESB/632xESB I/O Controller Hub's standard Hot-Plug controller switches to the serial mode. Intel® 631xESB/632xESB I/O Controller Hub does not support parallel operation when the number of Hot-Plug slots is greater than two nor does it support serial operation when the number of Hot-Plug slots is less than three. In the parallel mode, when the number of Hot-Plug slots being controlled is one and the only one in the system, and there is only one PCI device on the segment in that Hog-Plug slot, then Intel® 631xESB/632xESB I/O Controller Hub provides the 1-slot-no-glue mode where the on-board FET switches (otherwise needed to isolate the Intel® 631xESB/632xESB I/O Controller Hub's PCI buffers from the slot) are no longer needed. Here is a summary of the three different modes in which the Intel® 631xESB/632xESB I/O Controller Hub's standard Hot-Plug controller can function.

Table 5-6. Standard Hot-Plug Controller Modes

Hot-Plug Mode	Glue Logic	FET Isolation
Serial	Yes	Yes
Parallel	No	Yes
Parallel 1-slot-no-glue	No	No

Figure 5-3 below illustrates the general standard Hot-Plug system architecture with two PCI slots. The slot control logic here refers to the board glue logic consisting of a pair of serializer and de-serializer needed to convert between serial and parallel data from to/ from Intel® 631xESB/632xESB I/O Controller Hub. This slot control logic is required only in the serial mode of operation (number of slots greater than 2). When in parallel mode, Intel® 631xESB/632xESB I/O Controller Hub has direct access to the power controller, LEDs, bus switches and the attention button. The slot control logic is not needed anymore in this mode. The bus switches shown in the picture could be removed when Intel® 631xESB/632xESB I/O Controller Hub's standard Hot-Plug controller is programmed for the 1-slot-no-glue mode.

Figure 5-3. Standard Hot-Plug System Architecture for PCI-X*



Mode Determination

The standard Hot-Plug controller is enabled and mode selected through pin strappings and these strappings are sampled on the rising edge of PWROK signal. The table below shows the information. When the standard Hot-Plug controller is disabled (HXSLOT[3] = “0”), the standard Hot-Plug capability registers and the working register set are hidden from software and the standard Hot-Plug controller is essentially disabled. The number of standard Hot-Plug slots the controller handles is logged into the slot configuration register at offset 0Ch in the SHPC working register set. This register is read-only register and cannot be written to by BIOS to change the mode of operation of the controller in Intel® 631xESB/632xESB I/O Controller Hub (between serial and parallel).

Table 5-7. Standard Hot-Plug Controller Mode Determination (Sheet 1 of 2)

HXSLOT[3:0]	# Slots (Intel® 631xESB/632xESB I/O Controller Hub SHPC Mode)
Hot-Plug Disabled	
0000	1 Slot
0001	2 Slots
0010	3 Slots
0011	4 Slots

Table 5-7. Standard Hot-Plug Controller Mode Determination (Sheet 2 of 2)

HXSLOT[3:0]	# Slots (Intel® 631xESB/632xESB I/O Controller Hub SHPC Mode)
0100	5 Slots
0101	6 Slots
0110	7 Slots
0111	8 Slots
Hot-Plug Enabled	
1000	Reserved[1]
1001	1-slot (parallel)
1010	2-slot (parallel)
1011	3-slot (serial)
1100	4-slot (serial)
1101	5-slot (serial)
1110	6-slot (serial)
1111	1-slot-no-glue (parallel)

Note: Using a reserved encoding could cause undefined behavior

Slot Control Signals

This section discusses the signals needed to control the slot side interface. This is a brief discussion of the their operation. For a more detailed discussion, refer to the standard Hot-Plug specification. These signals are direct inputs and outputs from Intel® 631xESB/632xESB I/O Controller Hub in the parallel mode. In the serial mode, these signals are sent or received serially to or from the slot side interface.

Output Control

These seven signals are output from Intel® 631xESB/632xESB I/O Controller Hub (serial or parallel) and control the slot side interface to do various functions from connecting the slot to the bus to turning on/off the LEDs.

- **HXPWREN**: Power enable signal connected to on-board slot-specific power controller to regulate current and voltage of the slot.
- **HXCLKEN#, HXBUSEN#**: Clock and bus enable signals that connect the PCI bus and clock signal of the slot to the system bus PCI bus by way of FET isolation switches.
- **HPX_RST#**: Connected to the PCIRST# pin of the slot.
- **HXATNLED#**: Connected to attention LED which is yellow or amber in color.
- **HXPWRLED#:** Connected to the power LED which is green in color.

Input Control

These eight signals are used to poll the status of the Hot-Plug slots for such things are MRL switch closure and power fault in the slot power controller.

- **HXPWRFLT#:** Power controller fault indication for over-current / under-volt indication. When asserted, the Intel® 631xESB/632xESB I/O Controller Hub, if enabled, immediately asserts reset to the slot and disconnects the slot from the bus.

- **HXPRSNT1#, HXPRSNT2#:** These signals are used to indicate to Intel® 631xESB/632xESB I/O Controller Hub whether a card is installed in the slot or not and its power requirements. These signals are directly connected to the present bits on the PCI card

PRSNT1#	PRSNT2#	Meaning
1	1	No expansion board present
0	1	Expansion board present, 25 W maximum
1	0	Expansion board present, 15 W maximum
0	0	Expansion board present, 7.5 W maximum

- **HXM66EN:** Determines if a card is capable of running at 66 MHz in the conventional PCI mode.
- **HXPCIXCAP1 and HXPCIXCAP2**: Determines if a slot is PCI-X capable, and if so, whether it can operate at 133 MHz. PCIXCAP1 and 2 represent a decoded version of the three-state PCIXCAP pin present on each slot. PCIXCAP2 represents whether the PCIXCAP pin was ground or not ground (that is, PCI-X capable), and PCIXCAP1 represents whether the PCIXCAP pin was “low” (66 MHz only) or “high” (133 MHz capable). The system initially powers up at 33 MHz PCI, and all Hot-Plug slots are scanned by firmware. If the system is capable, the bus is reset to run in the appropriate PCI-X mode.

PCIXCAP1	PCIXCAP2	Meaning
1	1	133MHz PCI-X* Mode
0	1	66MHz PCI-X Mode
1	0	Reserved
0	0	PCI Mode

- **HXMRL#:** Manually operated retention latch sensor input. A logic low input that is connected directly to the MRL sensor. When asserted it indicates that the MRL latch is closed. If a platform does not support MRL sensors, this must to be wired to a low logic level (MRL closed).
- **HXBUTTON#:** Attention button input signal connected to the slot’s attention button. When low, indicates that the operator has requested attention. If attention button is not implemented, then this input must be wired to a high logic level.

Parallel Mode Operation

In the parallel mode, Intel® 631xESB/632xESB I/O Controller Hub provides 6 slot control outputs and 8 slot control inputs for each of the two slots it can control. Intel® 631xESB/632xESB I/O Controller Hub operates in this mode, if the number of Hot-Plug slots implemented is 1 or 2. If the number of slots is 1, then Intel® 631xESB/632xESB I/O Controller Hub ignores the second port. Platform must tie this port to its benign value.

One-Slot-No-Glue Parallel Mode Operation

When only 1 slot is implemented, the bus isolation switches are not required as there are no other devices on the PCI bus other than that one slot. There is no reason to isolate the card from Intel® 631xESB/632xESB I/O Controller Hub’s I/O buffers.

Intel® 631xESB/632xESB I/O Controller Hub enters this mode if HXSLOT[3:0] is a "1111." There are special requirements for how the PCI bus signals are handled in this mode.

Driving Bus To Ground When PCI Card is Disconnected

When in single-slot-no-glue mode, all PCI signals are to be driven to ground whenever PCI card is disconnected. The signals that must be driven to ground are the following:

- AD[63:0], C/BE[7:0]#, PAR, PAR64, REQ64#, ACK64#
- FRAME#, IRDY#, TRDY#, STOP#, DEVSEL#, LOCK#, IDSEL
- PCIRST#
- GNT[4:0]#, REQ[5:4]#, REQ[1:0]#
- PERR#, SERR#
- PCLKOUT[4:0]
- IRQ[7:0], PME#

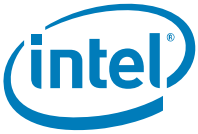
These signals will be driven back to their normal PCI levels at various times in the clock connection process. When a card is reconnected to the bus, it follows the following algorithm:

- Power is applied to the card. This does not affect any of the PCI signals which are now being driven to ground.
- After a fixed (refer to SHPC spec) period of time, the clock is connected to the card. When this occurs, PCLKOUT[4:0] will no longer be driven to ground, but will toggle normally (assuming that SW has not disabled that particular PCLKOUT pin). In Hot-Plug terms, this is the equivalent of the "CLKEN#" signal.
- After another fixed (refer to SHPC spec) period of time, the bus is connected to the card. When this occurs, The remaining signals listed above which were driven to ground will be driven to their default values, except for reset, which will continue to be driven to ground. The new signal values are listed below:
  - AD[63:0], C/BE[7:0]#, PAR, PAR64, REQ64#, ACK64# – driven
  - FRAME#, IRDY#, TRDY#, STOP#, DEVSEL#, LOCK#, IDSEL – driven to VCC for one clock, then tri-stated
  - GNT#, REQ# – driven to VCC for one clock, then tri-stated
  - PERR#, SERR# – driven to VCC for one clock, then tri-stated
  - IRQ[7:0] tri-states, PME# tristates

  In Hot-Plug terms, this is the equivalent of the "BUSEN#" signal.
- After a final fixed period of time, the card is taken out of reset. When this occurs, the PCIRST# pin will be continuously driven to VCC.

Aborting Outbound PCI Cycles When Card is Disconnected

When a PCI card is not present in a multi-slot system, it has been isolated. This means that all cycles destined for that particular card (peer traffic or other CPU based traffic) will Master abort on the PCI bus because no DEVSEL# will be driven. To be consistent in a single-slot system, the Intel® 631xESB/632xESB I/O Controller Hub must Master abort cycles that are destined for that PCI bus when the card is disconnected. Therefore, the buffer interface will have to internally Master abort all outbound transactions destined for that PCI bus until a card is connected again.



Serial Mode Operation

During the Serial mode of operation, the Intel® 631xESB/632xESB I/O Controller Hub sends and receives information serially from the slot control logic. The slot control logic is required to deserialize the output information to the bus switches and slot. The Slot control logic is also required to convert parallel input information from the slots into serial data to Intel® 631xESB/632xESB I/O Controller Hub. The serial interface will run at 16.5 MHz. In this mode, Intel® 631xESB/632xESB I/O Controller Hub constantly polls the slot inputs serially looking for an event at any of the Hot-Plug slots. The output serial stream from Intel® 631xESB/632xESB I/O Controller Hub is on demand and is sent out only when Intel® 631xESB/632xESB I/O Controller Hub needs to schedule an event at a slot.

Switch Debounce

For the switch inputs, Intel® 631xESB/632xESB I/O Controller Hub provides a 8 ms debounce timer internally (board does not have to provide one). This is true in both the serial and parallel modes. A change on any of the switch inputs initiates an 8 ms glitch filter timer. If a change is detected on any slot switch input, the switch input is at an 8 ms time interval. If the switches remain stable, then a change is state is confirmed. If any switch is still changing state, the glitch filter counter is cleared and the sequence restarts.

Secondary Bus Initialization and SHPC Role

With the in-box solution it is assumed that Intel® 631xESB/632xESB I/O Controller Hub would be an embedded part of the system board and the system BIOS has complete knowledge of the PCI buses below the Intel® 631xESB/632xESB I/O Controller Hub, like the loading characteristics of the bus, the slot numbering scheme on the bus and so forth. In such an architecture, whenever the SHPC in Intel® 631xESB/632xESB I/O Controller Hub is initialized (power-on or a PCI Express bus reset) the system BIOS/firmware would be invoked to initialize the SHPC working register set with board-specific information (HWInit Registers) and also initialize the PCI bus beneath Intel® 631xESB/632xESB I/O Controller Hub to the proper mode and frequency. Whenever the standard Hot-Plug controller is reset, the slot interface outputs are reset to the following:

- RST# is asserted.
- BUSEN# is de-asserted (disconnected from the bus).
- CLKEN# is de-asserted (PCI clock disconnected from the bus).
- PWREN is de-asserted (slot power is removed).
- All PWRLED# and ATNLED# outputs are set to OFF.

When HXSLOT[3] for a PCI interface is “1” (Hot-Plug is enabled), then whenever the SHPC is initialized, the PCI bus will power up operating at 33 MHz PCI and all Hot-Plug slots isolated from the bus. The platform BIOS/firmware could later determine the capabilities of the non-Hot-Plug PCI cards (reading the PCI-X and 66 MHz capability bits in the PCI register space of the cards) and also the capabilities of the inserted Hot-Plug cards, for PCI-X capability, or PCI capability at 66 MHz, and then could reset the PCI bus to operate in the new mode. The software could execute a set bus frequency/mode command to achieve the mode.

M66EN Pin Handling

The Intel® 631xESB/632xESB I/O Controller Hub can drive the PxM66EN pin on each PCI bus to GND in Serial Mode, 1-slot-parallel and in 2-Slot parallel mode (1-slot-no-glue mode is excluded here). There are three possible cases where Intel® 631xESB/632xESB I/O Controller Hub will drive the M66EN pin:

- The PFREQ and PMODE registers are reprogrammed for 33MHz PCI mode and a secondary bus reset is completed
- The Intel® 631xESB/632xESB I/O Controller Hub is powered on with any Hot-Plug mode enabled by strapping the HXSLOT[3] pin to '1' at PWROK
- A change frequency/mode command is executed by the standard Hot-Plug controller with the frequency set at 33 MHz

In each of these cases, the Intel® 631xESB/632xESB I/O Controller Hub will drive the PXM66EN pin to GND for the affected PCI bus. However, it should be noted that when the Intel® 631xESB/632xESB I/O Controller Hub is in a 1-Slot mode and the slot is disconnected, it will never drive the PxM66EN pin. This is to allow the Hot-Plug controller the ability to correctly sample the M66EN pin on the slot when the PCI bus is grounded (not connected) but the PCI card is powered on. In this mode, it is recommended that the M66EN pin be pulled up to PCI slot's 3.3 V power rail which is controlled by the Hot-Plug controller.

5.1.2.5.3 Assumptions and Intel® 631xESB/632xESB I/O Controller Hub Requirements

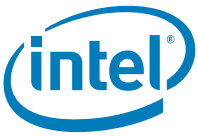
MRL Opening During the Sequence

While executing a enable or disable sequence, if the MRL of one of the cards is opened then the Intel® 631xESB/632xESB I/O Controller Hub performs the auto power down for that slot after executing the current enable/disable operation. As the maximum time required to enable is disable is 319 ms, the maximum delay between MRL open and auto-power down would be less than 320 ms.

Power Fault

The power controller/slot control logic is responsible for removing power from the slot when a power fault happens, regardless of the Hot-Plug mode in Intel® 631xESB/632xESB I/O Controller Hub. Also, the slot control logic is responsible for asserting reset and isolating the card in the event of a power fault, in serial mode. In parallel mode, Intel® 631xESB/632xESB I/O Controller Hub will perform the above-mentioned actions. In 2-slot, 1-slot-no-glue and 1-slot parallel mode, Intel® 631xESB/632xESB I/O Controller Hub will assert reset to the slot, disable bus/clock from the slot (by way of deasserting the BUSEN and CLKEN signals) asynchronously when the power fault happens. In the 1-slot-no-glue mode, Intel® 631xESB/632xESB I/O Controller Hub will assert reset and ground the bus when the power fault happens. The PWREN signal from Intel® 631xESB/632xESB I/O Controller Hub is not asynchronously deasserted on a slot power fault and deasserted only under software control.

Intel® 631xESB/632xESB I/O Controller Hub would keep the slot that has the powerfault isolated from the bus, till the bits 17 and 20 in the slot event latch field are cleared and the software issues an enable slot command. Note that an enable command from software will not take affect if the slot that incurred the power fault is currently not in a disabled state. The disable could be because of a previous disable command from software or could be because of an MRL open event at the slot.



5.1.3 PCI Express* Downstream Ports (Bp:D0:F0; Bp:D1:F0)

PCI Express downstream ports have two x4 PCI Express ports, and these two ports can also be configured as one x8 PCI Express port. These ports reside on Device 0: Function 0 and Device 1:Function 0.

- Raw bit-rate on the data pins of 2.5 Gbit/s, resulting in a raw bandwidth per pin of 250 MB/s
- x4 or x8 modes of operation
- Maximum realized bandwidth (in x8 mode) on PCI Express interface is 2 GB/s in each direction simultaneously, for an aggregate of 4 GB/s
- Maximum realized bandwidth (in x4 mode) on PCI Express interface is 1 GB/s in each direction simultaneously, for an aggregate of 2 GB/s
- Pleisochronous operation with automatic clock extraction and phase correction
- Hierarchical PCI configuration mechanism for downstream devices
- Full 64-bit inbound addressing supported as defined by PCI Express specifications
- 64-bit outbound addressing support (that is, capability to generate DAC transactions on PCI)
- Forwarding of relaxed ordering attribute
- Forwarding of non-snooped/snooped attribute
- Full-speed self-test and diagnostic (IBIST) functionality
- Automatic link initialization, configuration and re-training out of reset
- Runtime detection and recovery for loss of link synchronization
- 32-bit CRC (cyclic redundancy checking) covering all transmitted data packets
- 16-bit CRC on all link message information
- Hardware link-level retry to recover from transient errors without system failure (software transparent)
- Support of in-band power management event, RAS error, boot interrupt, and component reset signaling
- Support of MSI and SAPIC interrupt messaging over PCI Express
- Support of Assert_INTx message interrupt messaging over PCI Express
- Supports PCI Express native Hot-Plug and hot removal
- VC#0 only support. No ISOC support.
- No support for transaction layer CRC (ECRC)

5.1.3.1 PCI Express* Hot-Plug Support

Intel® 631xESB/632xESB I/O Controller Hub supports Hot-Plug of PCI Express cards installed in slots attached to these 2 x4 PCI Express ports

5.1.3.1.1 Introduction

The Intel® 631xESB/632xESB I/O Controller Hub PCI Express Hot-Plug design accommodates two PCI Express Hot-Pluggable devices simultaneously and uses an SMBus interface to communicate with a serial I/O expander device (for example the Phillips 9555) to provide connectivity to the external Hot-Plug signals.

5.1.3.1.2 Overview

PCI Express native Hot-Plug allows for higher availability and serviceability of a server. It gives the user the capability of adding, removing, or swapping out a PCI Express slot device without taking down the system. The user and system communicate through a combination of software and hardware utilizing notification through mechanical means and indicator lights. The signals involved with be briefly discussed here. One should refer to the PCI Express specification itself for complete details.

The following table provides a matrix of the registers requirements for a PCI Express switch implementing Hot-Plug. The form factor referred in the table as PCI Express-C is a traditional card-edge connector slot, which is the form factor that Intel® 631xESB/632xESB I/O Controller Hub supports. Also, there are 2 categories under PCI Express-C that are designated as optional. Only the first of these two optional items are supported; namely the attention indicators. The register bit definitions can be found in the configuration register description chapter.

Table 5-8. PCI Express* Register Requirements

Register Group	PCI Express*-C
Attention Button Registers	Required
Attention Indicator Registers	Optional
Power Indicator Registers	Required
Presence Detect Registers	Required
MRL Registers	Optional
Power Controller Registers	Required

Of particular interest to this discussion is what signals are necessary to support PCI Express Hot-Plug. The Attention Button Registers will require an input from an external attention button. The Attention Indicator Registers will utilize an output to drive an external indicator light. The Power Indicator Registers will utilize an output to drive an external power indicator light. The Presence Detect Registers will require an input pin to detect the presence of an add-in card. The Power Controller Register requires an output to control the power supplied to the add-in card. It also requires an input to indicate a power fault when it occurs. The total of all these signals comes to 4 inputs (attention pushbutton, presence detect, power fault, and mechanical latch) and 4 outputs (attention indicator, power indicator, power enable/control, and spare) for a total of 8 pins. Normally these 8 pins would come directly off of the integrated Hot-Plug controller, but with the requirement to support more than one Hot-Plug slot, and with the lack of spare signals on Intel® 631xESB/632xESB I/O Controller Hub, this has prompted a different approach, described in the following section.

5.1.3.1.3 Hardware Interface Overview

Intel® 631xESB/632xESB I/O Controller Hub has decided to utilize an external I/O expander device, which interfaces to the I^2C/SMBus. Intel® 631xESB/632xESB I/O Controller Hub will modify its existing SMB target, to become both a Master and a Target. This will allow Intel® 631xESB/632xESB I/O Controller Hub to control this external device. The only pin that need be added to support Hot-Plug is an interrupt pin from the external device, which indicates that one of its input pins has changed. The cost of an external device plus one package signal has been traded off against the cost of supplying 12 additional package signals to support 2 PCI Express Hot-Plug slots.

In the overview figure below, we have two separate PCI Express units (PCI Expressx and PCI Expressy) that communicate to their respective slots by way of two separate paths. Note that x and y refer to the south x4 PCI Express ports. The non-Hot-Plug or

traditional interface signals have a direct path to the slots. The Hot-Plug signals, from both units, communicate to a common Hot-Plug controller. This controller then interfaces to the SMBus, which connects to the external I/O expander. It is the external expander, which interfaces directly with the Hot-Plug signals of the slot. Note that the "slot" reference is a generic one, since not all Hot-Plug signals will actually go to the card, but to logic that supports the slot. In fact, only the presence detect signal will come directly from the actual card slot. The power controller, pushbutton, and indicator lights associated with each slot will not be on the actual add-in card.

The diagram separates the Intel® 631xESB/632xESB I/O Controller Hub from external components. The external features include the slots themselves, the I/O expander device, a pull-up resistor on the external interrupt, debounce-circuitry for the attention buttons (designated as DB), and board loop back for unused pins for validation purposes.

5.1.3.1.4 I/O Expander Device

The recommended I/O Expander is a device compatible with the Philips PCA9554 component or the Philips PCA9555 component. Details of those components follow:

Figure 5-4 is a pictorial view of the pin assignments for the PCA9554 device.

Figure 5-4. Pin Assignments For PCA9554

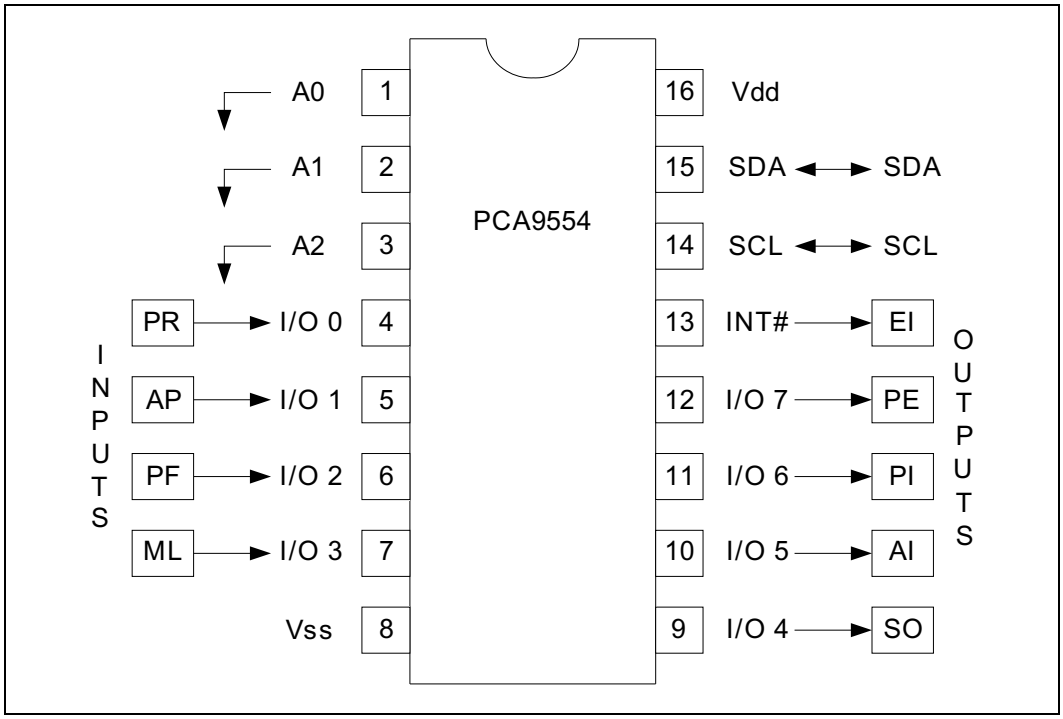


Figure 5-5 is a pictorial view of the pin assignments for the PCA9555 device.

Figure 5-5. Pin Assignments For PCA9555

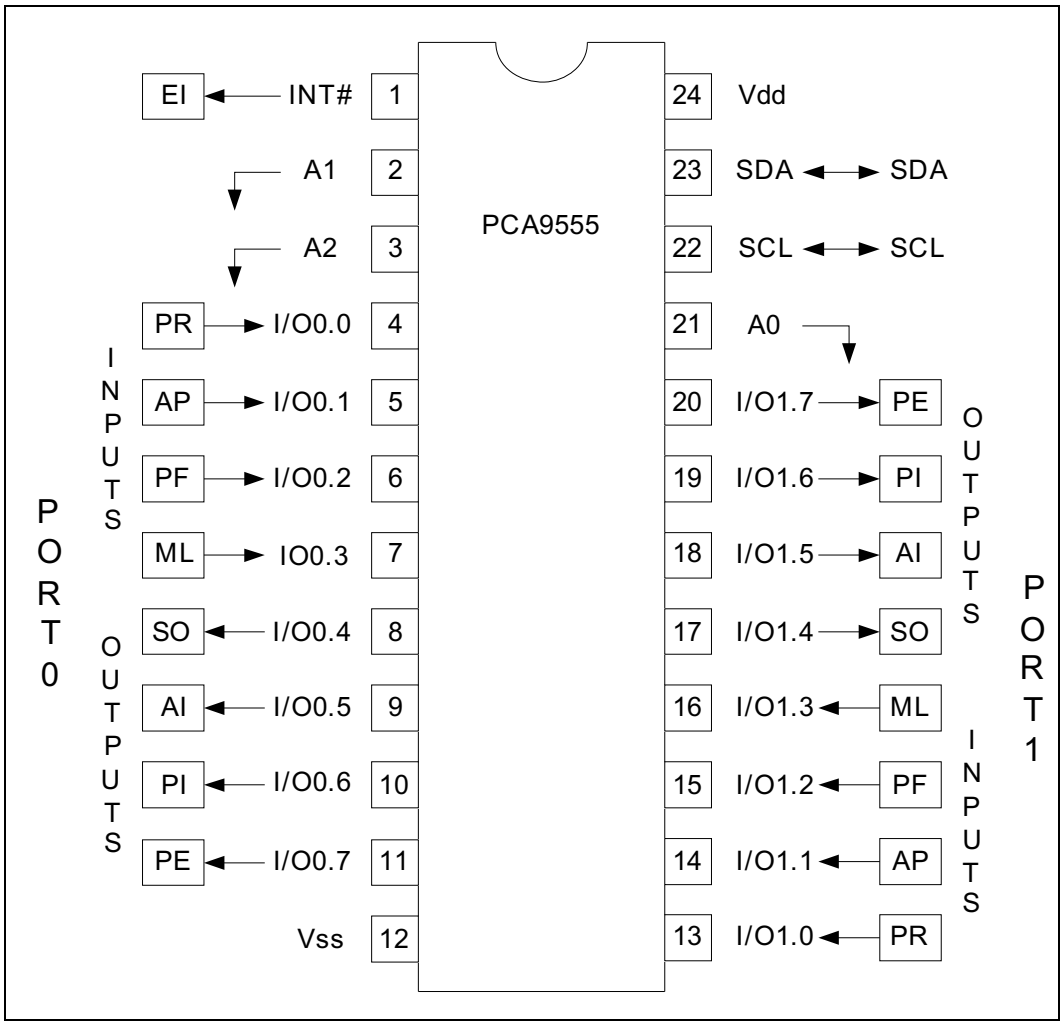


Table 5-9 shows the relationship between the hot plug signals and the I/O expander signals:

Table 5-9. HOT-PLUG SIGNAL TO BIT ASSIGNMENT

Bit	Signal Name	PCA955x	I/O	Active Meaning*	Inactive Meaning
0	Presence Detect	PR	Input	Card Present in Slot	Slot is Empty
1	Attention Pushbutton	AP	Input	Button Pressed	Button Not Pressed
2	Power Fault	PF	Input	Power Fault	No Power Fault
3	Mechanical Latch	ML	Input	Latch is Open (card can be removed)	Latch is Closed (card cannot be removed)
4	Spare Output	SO	Output	User Defined	User Defined
5	Attention Indicator	AI	Output	Indicator On	Indicator Off
6	Power Indicator	PI	Output	Indicator On	Indicator Off
7	Power Enable/Control	PE	Output	Power Enabled	Power Disabled

5.1.3.1.5 I/O Expander Address

One point of confusion is sometimes the SMB address. The I/O Expander Address is adjustable at the upper bits through the HPCCTL register, but in order to access the PCA9554 and PCA9555 devices the upper nibble (A6:A3) needs to be set to 0100b. If for some reason, a PCA9554A device is used, these same bits must be set to 0111b. From a bit position perspective, it would appear the address of the PCA9555 device of 0100000b is 20h, but because of the lsb R/W bit for addressing, this is referred to as 40h. This convention is standard to the SMB specification.

Refer to *RS-Enterprise South Bridge 2 BIOS Specification* for how to program the SMBus address for the I/O expander.

Table 5-10. I/O Expander Address Matrix

Upper Address Nibble	Mode	Port	SMB Address
A6 A5 A4 A3	Dual Byte	0	A6 A5 A4 A3 0 0 0
A6 A5 A4 A3	Dual Byte	1	A6 A5 A4 A3 0 0 0
A6 A5 A4 A3	Single Byte Low	0	A6 A5 A4 A3 0 0 0
A6 A5 A4 A3	Single Byte High	1	A6 A5 A4 A3 0 0 1

5.1.3.1.6 Software Interface Overview

Not all concepts from the Standard PCI Hot-Plug definition apply directly to PCI Express interfaces. The specification still calls for an identical software interface in order to facilitate adoption with minimal development overhead on this aspect of the implementation.

The largest variance from the old PCI Hot-Plug model is in control of the interface itself. PCI required arbitration support for idling already connected components, and “quick switches” to isolate the bus interface pins of a Hot-Plug slot. PCI Express is a point-to-point interface, making Hot-Plug a subset of the old model that doesn’t require such arbiter support. Furthermore, the PCI Express interface is inherently tolerant of hot connect or disconnect, and does not have explicit clock or reset pins defined as a part of the bus (although they are standard pieces of some defined PCI Express connector form factors). As a result of these differences, some of the inherited Hot-Plug command and status codes are misleading when applied to PCI Express.

5.1.3.1.7 PCI Express* Hot-Plug Register Descriptions

The Hot-Plug function is advertised in the PCI Express capability for its associated downstream port within the Intel® 631xESB/632xESB I/O Controller Hub. Hot-Plug is supported for downstream ports attached to slots.

For specific information on the Hot-Plug register set, refer to the PCI Express Device Capability register, Slot Capability register, Slot Status register, and Slot Control register in the associated downstream port.

5.1.4 I/OxAPIC Devices (Bm:D0:F1).

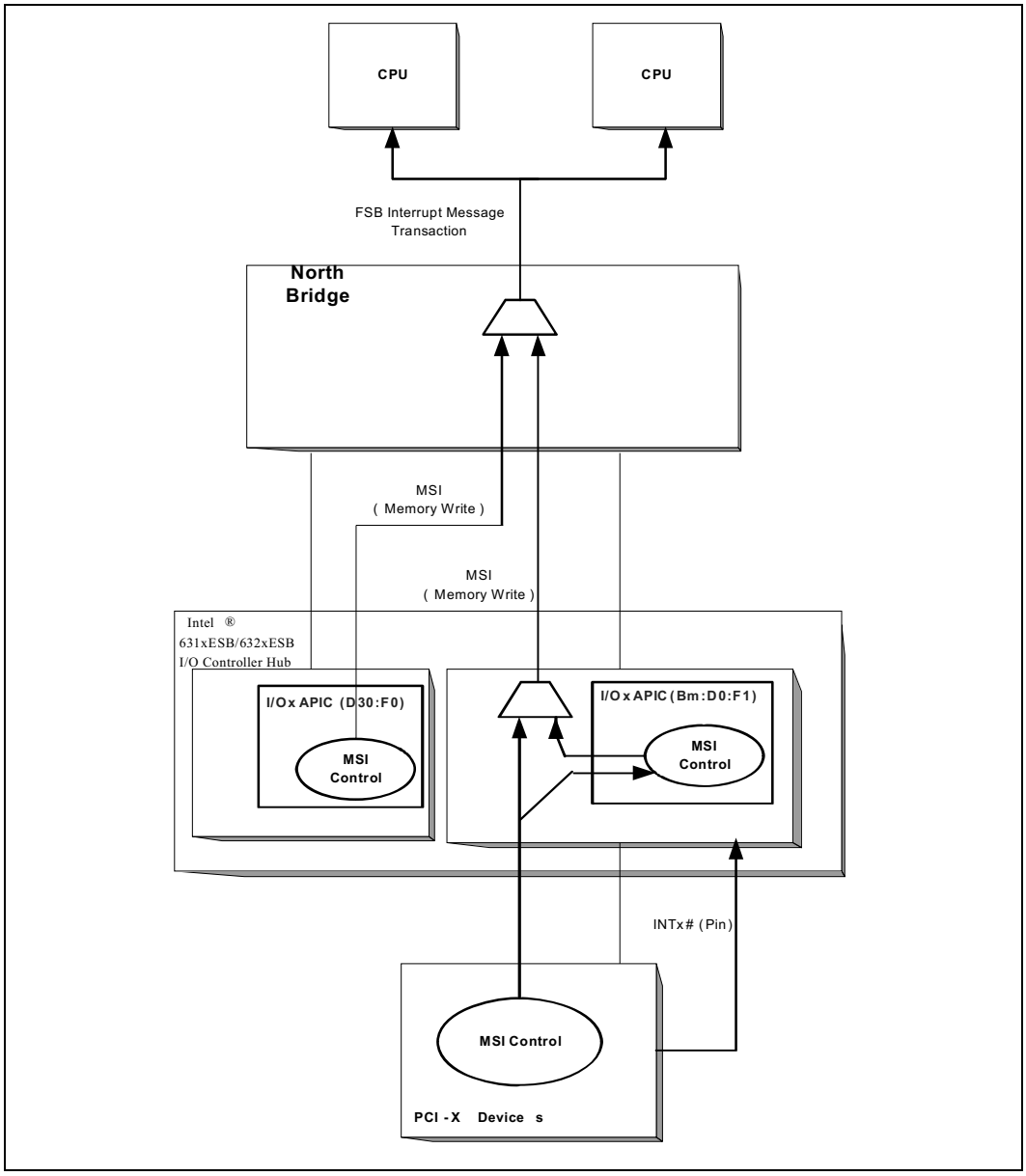
As shown in Figure 5-6, Intel® 631xESB/632xESB I/O Controller Hub implements two I/OxAPIC controllers. For information about I/OxAPIC (D31:F0), refer to Section 5.11.

This I/OxAPIC (D0:F1) resides on the primary bus. The intended use of this controller is to have the interrupts from the PCI-X bus connected to this interrupt controller on Device 0: Function 1.

The following list summarizes some of the features of the Intel® 631xESB/632xESB I/O Controller Hub I/OxAPIC controller (D0:F1):

- One I/OxAPIC controller, support for 24 interrupts
- 16 physical PCI interrupt pins per PCI bus in the server mode
- PCI virtual wire interrupt support by way of writing to Pin Assertion Register in the I/OxAPIC
- Support for both IA-32 and Itanium® processor front side bus messages
- No support for serial bus delivery
- No support for EOI special cycle propagation to PCI

Figure 5-6. System Interrupt Architecture



5.1.4.1 PCI IRQ# Interrupts

The I/O APIC (D0:F1) within the Intel® 631xESB/632xESB I/O Controller Hub can handle up to 16 pin interrupts. Interrupts delivered by a pin can be either in level or edge mode, and may be either active high or active low. Since this I/OxAPIC is connected to a PCI bus, its most likely configuration will be as active low level, which will match the PCI pin polarity and functionality. Each pin is collected by Intel® 631xESB/632xESB I/O Controller Hub, synchronized into the PCI clock domain, and scheduled for delivery if it is unmasked.

Intel® 631xESB/632xESB I/O Controller Hub has only 16 interrupt pins on the PCI-X segment. These pins are connected to I/OxAPIC redirection table entries 15 – 0 (of 24 entries). The standard Hot-Plug controller is hardwired to redirection table entry 23 of the I/OxAPIC. All other interrupts are addressable only through the PCI virtual wire mechanism. The unused pins must be connected to VCC.

5.1.4.2 PCI Message Signaled Interrupts (MSI)

These interrupts which appear on the PCI bus as inbound memory writes are decoded by Intel® 631xESB/632xESB I/O Controller Hub in the PCI bridge inverse decode window and passed upstream without any modifications. BIOS would setup the PCI bridge decode register such that 0xFEEx_xxxx falls in the inverse decode window of Intel® 631xESB/632xESB I/O Controller Hub.

5.1.4.3 PCI Virtual Wire Interrupts

PCI devices could directly write to the PAR (Pin Assertion Register, See Section 13.5.2.4) in the corresponding bridge I/OxAPIC device to cause an upstream interrupt message. All the 24 interrupt entries are addressable through this mechanism. Values above 23 are invalid in the pin assertion register and are ignored by the Intel® 631xESB/632xESB I/O Controller Hub.

Intel® 631xESB/632xESB I/O Controller Hub decodes the memory write transactions to the pin assertion register in the P2P bridge inverse decode window, just as any other upstream transaction.

5.1.4.4 PCI Express* Legacy INTx Support and Boot Interrupt

The Intel® 631xESB/632xESB I/O Controller Hub has the capability to generate an in-band interrupt request on the PCI Express bus when the I/O APIC (D0:F1) is disabled. This in-band interrupt mechanism is necessary for systems that do not support the I/O APIC (D0:F1) and for boot. The PCI Express protocol describes an inband legacy wire-interrupt INTx mechanism for I/O devices to signal PCI-style level interrupts. The Intel® 631xESB/632xESB I/O Controller Hub generates a PCI Express INTx message as follows: each interrupt pin input (16 interrupt pins) and INT[23]# is compared with its mask (bit 16 in the redirection table low, RDL register). If the interrupt is masked in the I/O APIC (D0:F1), that interrupt needs to cause an INTx message over the PCI Express bus whenever asserted. If the interrupt is not masked, then that interrupt is being used by the I/O APIC (D0:F1) and should not cause an INTx message on the PCI Express bus.

In PCI Express, the legacy interrupts are virtualized using a pair of ASSERT and DEASSERT messages. This then gives a way to preserve the level-sensitive semantics of the PCI interrupts on PCI Express. PCI Express defines four virtual wire interrupts - INTA:INTD -corresponding to the four interrupt wires defined in PCI spec.
Intel® 631xESB/632xESB I/O Controller Hub routes its PCI interrupt pins and the internal interrupts, to PCI Express INTx interrupts according to the following table

Table 5-11. Intel® 631xESB/632xESB I/O Controller Hub INTX Routing Table

PCI Interrupt Pins	Internal Interrupts	PCI Express* INTx Message
0, 4, 8, 12	SHPC (IRQ[23])	INTA
1, 5, 9, 13	-	INTB
2, 6, 10, 14	-	INTC
3, 7, 11, 15	-	INTD

5.1.4.5 Buffer Flushing

Intel® 631xESB/632xESB I/O Controller Hub does not implement any buffer flushing feature that is,. when Intel® 631xESB/632xESB I/O Controller Hub receives an interrupt on its interrupt pin, it does not flush its posted write buffers in the inbound direction in the PCI interface. This is not required from Intel® 631xESB/632xESB I/O Controller Hub because PCI device drivers ultimately have to guarantee that all posted writes from the device to the memory are all flushed before executing the interrupt service routine. It could do this by doing a dummy read to the device that originated the interrupt. Or the originating device could solve this problem if it did a read of the memory to guarantee that the write before it went through and then signal an interrupt.

5.1.4.6 EOI Special Cycles

Intel® 631xESB/632xESB I/O Controller Hub could get EOI special cycles over PCI Express in the IA32 FSB mode. This is the result of MCH broadcasting the IA32 FSB EOI cycle. The I/OxAPIC (D0:F1) in Intel® 631xESB/632xESB I/O Controller Hub would compare the vector number in the EOI data field with the vector field for each entry in the I/O Redirection Table. When a match is found, the Remote_IRR bit for that I/O Redirection Entry in the I/OxAPIC will be cleared.

Note that if multiple I/O Redirection entries, for any reason, assign the same vector for more than one interrupt input, each of those entries will have the Remote_IRR bit reset to ‘0’.

5.1.4.7 Upstream Interrupt Message Format

When an interrupt message needs to be sent over PCI Express, that is, when the IRR bit is set for an interrupt, the Intel® 631xESB/632xESB I/O Controller Hub will perform a memory write on PCI Express. The message format is the same as in Table 5-24 and Table 5-25.

5.1.5 Flow Control

The PCI Express mechanism for flow control is credit based and only applies to TLPs. DLLP packets do not consume any credits. Through initial hardware negotiation and subsequent updates, a PCI Express transmitter is aware of the credit capabilities of the interfacing device. A PCI Express requester will never issue a transaction when there are not enough advertised credits in the other component to support that transaction. If there are not enough credits, the requester will hold off that transaction until enough credits free up to support the transaction. If the ordering rules and available credits allow other subsequent transactions to proceed, the Intel® 631xESB/632xESB I/O Controller Hub will allow those transactions.

Note: Flow control is orthogonal with packet ACKs.

The PCI Express flow control credit types are described in Table 5-12. The *PCI Express Base Specification*, Revision 1.0a defines which TLPs are covered by each flow control type.

Table 5-12. PCI Express Credit Mapping Table

Direction	Flow Control Type	Limit
Inbound	Posted Request Header Credits (IPRH)	4
	Posted Request Data Credits (IPRD)	32x16 bytes
	Non-Posted Request Header Credits (INPRH)	4
	Non-Posted Request Data Credits (INPRD)	4x4 bytes
	Completion Header Credits (CPH)	4
	Completion Data Credits (CPD)	32x16 bytes*
Outbound	Posted Request Header Credits (OPRH)	16
	Posted Request Data Credits (OPRD)	128x16 bytes
	Non-Posted Request Header Credits (ONPRH)	1
	Non-Posted Request Data Credits (ONPRD)	1x4 bytes
	Completion Header Credits (CPLH)	16
	Completion Data Credits (CPLD)	128x16 bytes*

Note: * denotes initial credits for downstream E1 or E2 ports upon power-up; once running, these may be reduced and change dynamically

5.2 PCI Express* Root Ports (D28:F0,F1,F2,F3)

There are four PCI Express root ports in the Intel® 631xESB/632xESB I/O Controller Hub. These all reside in device 28, and take function 0 – 3. Port 1 is function 0, port 2 is function 1, port 3 is function 2, and port 4 is function 3.

5.2.1 Interrupt Generation

The root ports generate interrupts on behalf of Hot-Plug and power management events, when enabled. These interrupts can either be pin based, or can be MSIs, when enabled.

When an interrupt is generated by way of the legacy pin, the pin is internally routed to the Intel® 631xESB/632xESB I/O Controller Hub interrupt controllers. The pin that is driven is based upon the setting of the chipset configuration registers. Specifically, the chipset configuration registers used are the D28IP (Base address + 310Ch) and D28IR (Base address + 3146h) registers.

Table 5-13 summarizes interrupt behavior for MSI and wire-modes. In the table “bits” refers to the Hot-Plug and PME interrupt bits.

Table 5-13. MSI vs. PCI IRQ Actions

Interrupt Register	Wire-Mode Action	MSI Action
All bits 0	Wire inactive	No action
One or more bits set to 1	Wire active	Send message
One or more bits set to 1, new bit gets set to 1	Wire active	Send message
One or more bits set to 1, software clears some (but not all) bits	Wire active	Send message
One or more bits set to 1, software clears all bits	Wire inactive	No action
Software clears one or more bits, and one or more bits are set on the same clock	Wire active	Send message

5.2.2 Power Management

5.2.2.1 S3/S4/S5 Support

Software initiates the transition to S3/S4/S5 by performing an I/O write to the Power Management Control register in the Intel® 631xESB/632xESB I/O Controller Hub. After the I/O write completion has been returned to the CPU the Power Management Controller will signal each root port to send a PME_Turn_Off message on its downstream link. The device attached to the link will eventually respond with a PME_TO_Ack followed by sending a PM_Enter_L23 DLLP request to enter L23. The Intel® 631xESB/632xESB I/O Controller Hub root ports and Power Management Controller take no action upon receiving a PME_TO_Ack. When all the Intel® 631xESB/632xESB I/O Controller Hub and MCH root ports links are in state L23, the Intel® 631xESB/632xESB I/O Controller Hub Power Management Controller will proceed with the entry into S3/S3/S5. See Chapter 16 for additional details for the S3/S4/S5 entry sequence.

Prior to entering S3, software is required to put each device into $\mathbf{D3_{HOT}}$. When a device is put into $\mathbf{D3_{HOT}}$ it will initiate entry into a L1 link state by sending a PM_Enter_L1 DLLP. Thus under normal operating conditions when the root port sends the PME_Turn_Off message the link will be in state L1. However, when the root port is instructed to send the PME_Turn_Off message, it will send it whether or not the link was in L1. Endpoints attached to Intel® 631xESB/632xESB I/O Controller Hub can make no assumptions about the state of the link prior to receiving a PME_Turn_Off message.

5.2.2.2 Resuming from Suspended State

The root port contains enough circuitry in the resume well to detect a wake event through the WAKE# signal and to wake the system. When WAKE# is detected asserted, an internal signal is sent to the power management controller of the Intel® 631xESB/632xESB I/O Controller Hub to cause the system to wake up. This internal message is not logged in any register, nor is an interrupt/GPE generated due to it.

5.2.2.3 Device Initiated PM_PME Message

When the system has returned to a working state from a previous low power state, a device requesting service will send a PM_PME message continuously, until acknowledge by the root port. The root port will take different actions depending upon whether this is the first PM_PME has been received, or whether a previous message has been received but not yet serviced by the operating system.

If this is the first message received (RSTS.PS - D28:F0/F1/F2/F3:Offset 60h:bit 16 is cleared), the root port will set RSTS.PS, and log the PME Requester ID into RSTS.RID (D28:F0/F1/F2/F3:Offset 60h:bits 15:0). If an interrupt is enabled by way of RCTL.PIE (D28:F0/F1/F2/F3:Offset 5Ch:bit 3), an interrupt will be generated. This interrupt can be either a pin or an MSI if MSI is enabled by way of MC.MSIE (D28:F0/F1/F2/F3:Offset 82h:bit 0). See section Section 5.2.2.4 for SMI/SCI generation.

If this is a subsequent message received (RSTS.PS is already set), the root port will set RSTS.PP (D28:F0/F1/F2/F3:Offset 60h:bit 17) and log the PME Requester ID from the message in a hidden register. No other action will be taken.

When the first PME event is cleared by software clearing RSTS.PS, the root port will set RSTS.PS, clear RSTS.PP, and move the requester ID from the hidden register into RSTS.RID.

If RCTL.PIE is set, generate an interrupt. If RCTL.PIE is not set, send over to the power management controller so that a GPE can be set. If messages have been logged (RSTS.PS is set), and RCTL.PIE is later written from a 0 to a 1, and interrupt must be generated. This last condition handles the case where the message was received prior to the operating system re-enabling interrupts after resuming from a low power state.

5.2.2.4 SMI/SCI Generation

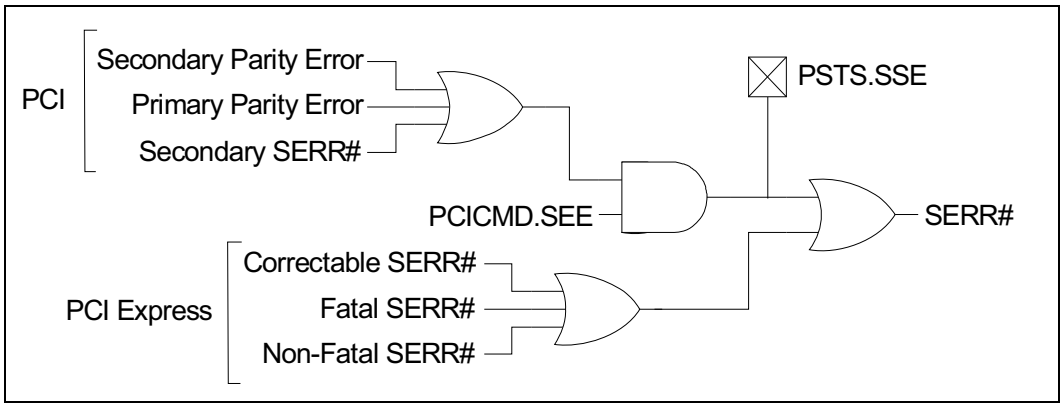
Interrupts for power management events are not supported on legacy operating systems. To support power management on non PCI Express aware operating systems, PM events can be routed to generate SCI. To generate SCI, MPC.PMCE must be set. When set, a power management event will cause SMSCS.PMCS (D28:F0/F1/F2/F3:Offset DCh:bit 31) to be set.

Additionally, BIOS workarounds for power management can be supported by setting MPC.PMME (D28:F0/F1/F2/F3:Offset D8h:bit 0). When this bit is set, power management events will set SMSCS.PMMS (D28:F0/F1/F2/F3:Offset DCh:bit 0), and SMI # will be generated. This bit will be set regardless of whether interrupts or SCI is enabled. The SMI# may occur concurrently with an interrupt or SCI.

5.2.3 SERR# Generation

SERR# may be generated by way of two paths – through PCI mechanisms involving bits in the PCI header, or through PCI Express mechanisms involving bits in the PCI Express capability structure.

Figure 5-7. Generation of SERR# to Platform



5.2.4 Hot-Plug

Each root port implements a Hot-Plug controller which performs the following:

- Messages to turn on / off / blink LEDs
- Presence and attention button detection
- Interrupt generation

The root port allows only Hot-Plug with modules (for example, ExpressCard*). Edge-connector based hot-plug is not supported.

5.2.4.1 Presence Detection

When a module is plugged in and power is supplied, the physical layer will detect the presence of the device, and the root port sets SLSTS.PDS (D28:F0/F1/F2/F3:Offset 5Ah:bit 6) and SLSTS.PDC (D28:F0/F1/F2/F3:Offset 6h:bit 3). If SLCTL.PDE (D28:F0/F1/F2/F3:Offset 58h:bit 3) and SLCTL.HPE (D28:F0/F1/F2/F3:Offset 58h:bit 5) are both set, the root port will also generate an interrupt.

When a module is removed (by way of the physical layer detection), the root port clears SLSTS.PDS and sets SLSTS.PDC. If SLCTL.PDE and SLCTL.HPE are both set, the root port will also generate an interrupt.

5.2.4.2 Message Generation

When system software writes to SLCTL.AIC (D28:F0/F1/F2/F3:Offset 58h:bits 7:6) or SLCTL.PIC (D28:F0/F1/F2/F3:Offset 58h:bits 9:8), the root port will send a message down the link to change the state of LEDs on the module.

Writes to these fields are non-postable cycles, and the resulting message is a postable cycle. When receiving one of these writes, the root port performs the following:

- Changes the state in the register.
- Generates a completion into the upstream queue
- Formulates a message for the downstream port if the field is written to regardless of if the field changed.
- Generates the message on the downstream port
- When the last message of a command is transmitted, sets SLSTS.CCE (D28:F0/F1/F2/F3:Offset 58h:bit 4) to indicate the command has completed. If SLCTL.CCE and SLCTL.HPE (D28:F0/F1/F2/F3:Offset 58h:bit 5) are set, the root port generates an interrupt.

The command completed register (SLSTS.CC) applies only to commands issued by software to control the Attention Indicator (SLCTL.AIC), Power Indicator (SKLCTL.PIC), or Power Controller (SLCTL.PCC). However, writes to other parts of the Slot Control Register would invariably end up writing to the indicators and power controller fields. Hence, any write to the Slot Control Register is considered a command and if enabled, will result in a command complete interrupt. the only exception to this rule is a write to disable the command complete interrupt which will not result in a command complete interrupt.

A single write to the Slot Control Register is considered to be a single command, and hence receives a single command complete, even if the write affects more than one field in the Slot Control Register.

5.2.4.3 Attention Button Detection

When an attached device is ejected, an attention button could be pressed by the user. This attention button press will result in a the PCI Express message “Attention_Button_Pressed” from the device. Upon receiving this message, the root port will set SLSTS.ABP (D28:F0/F1/F2/F3:Offset 5Ah:bit 0).

If SLCTL.ABE (D28:F0/F1/F2/F3:Offset 58h:bit 0) and SLCTL.HPE (D28:F0/F1/F2/F3:Offset 58h:bit 5) are set, the Hot-Plug controller will also generate an interrupt. The interrupt is generated on an edge-event. For example, if SLSTS.ABP is already set, a new interrupt will not be generated.

5.2.4.4 SMI/SCI Generation

Interrupts for Hot-Plug events are not supported on legacy operating systems. To support Hot-Plug on non-PCI Express aware operating systems, Hot-Plug events can be routed to generate SCI. To generate SCI, MPC.HPCE (D28:F0/F1/F2/F3:Offset D8h:bit 30) must be set. When set, enabled Hot-Plug events will cause SMSCS.HPCS (D28:F0/F1/F2/F3:Offset DCh:bit 30) to be set.

Additionally, BIOS workarounds for Hot-Plug can be supported by setting MPC.HPME (D28:F0/F1/F2/F3:Offset D8h:bit 1). When this bit is set, Hot-Plug events can cause SMI status bits in SMSCS to be set. Supported Hot-Plug events and their corresponding SMSCS bit are:

- Command Completed = SMSCS.HPCCM (D28:F0/F1/F2/F3:Offset DCh:bit 3)
- Presence Detect Changed = SMSCS.HPPDM (D28:F0/F1/F2/F3:Offset DCh:bit 1)
- Attention Button Pressed = SMSCS.HPABM (D28:F0/F1/F2/F3:Offset DCh:bit 2)

When any of these bits are set, SMI # will be generated. These bits are set regardless of whether interrupts or SCI is enabled for Hot-Plug events. The SMI# may occur concurrently with an interrupt or SCI.

5.3 PCI-to-PCI Bridge (D30:F0)

The PCI-to-PCI bridge resides in PCI Device 30, Function 0 on bus #0. This portion of the Intel® 631xESB/632xESB I/O Controller Hub implements the buffering and control logic between PCI and the ESI. The arbitration for the PCI bus is handled by this PCI device. The PCI decoder in this device must decode the ranges for the ESI. All register contents are lost when core well power is removed.

Enterprise South Bridge Interface (ESI) is the chip-to-chip connection between the Memory Controller Hub (MCH) and Intel® 631xESB/632xESB I/O Controller Hub. This high-speed interface integrates advanced priority-based servicing allowing for concurrent traffic and true isochronous transfer capabilities. Base functionality is completely software transparent permitting current and legacy software to operate normally.

Configuration registers for ESI and ESI active state power management (ASPM) are in the RCRB space in the Chipset Config Registers (Section 12).

5.3.1 PCI Bus Interface

The Intel® 631xESB/632xESB I/O Controller Hub PCI interface provides a 33 MHz, *PCI Local Bus Specification, Revision 2.3*-compliant implementation. All PCI signals are 5 V tolerant (except PME#). The Intel® 631xESB/632xESB I/O Controller Hub integrates a PCI arbiter that supports up to five external PCI Bus Masters in addition to the internal Intel® 631xESB/632xESB I/O Controller Hub requests.

5.3.2 PCI Bridge as an Initiator

The bridge initiates cycles on the PCI bus when granted by the PCI arbiter. The bridge generates the following cycle types:

Table 5-14. PCI Bridge Initiator Cycle Types

Command	C/BE#	Notes
I/O Read/Write	2h/3h	Non-posted
Memory Read/Write	6h/7h	Writes are posted
Configuration Read/Write	Ah/Bh	Non-posted
Special Cycles	1h	Posted

5.3.2.1 Memory Reads and Writes

The bridge bursts memory writes on PCI that are received as a single packet from ESI.

5.3.2.2 I/O Reads and Writes

The bridge generates single DW I/O read and write cycles. When the cycle completes on PCI bus, the bridge generates a corresponding completion on ESI. If the cycle is retried, the cycle is kept in the downbound queue and may be passed by a postable cycle.

5.3.2.3 Configuration Reads and Writes

The bridge generates single DW configuration read and write cycles. When the cycle completes on PCI bus, the bridge generates a corresponding completion. If the cycle is retried, the cycle is kept in the downbound queue and may be passed by a postable cycle.

5.3.2.4 Locked Cycles

The bridge propagates locks from ESI per the PCI specification. The PCI bridge implements bus lock, which means the arbiter will not grant to any agent except ESI while locked.

If a locked read results in a Target or Master abort, the lock is not established (as per the PCI specification). Agents north of the Intel® 631xESB/632xESB I/O Controller Hub must not forward a subsequent locked read to the bridge if they see the first one finish with a failed completion.

5.3.2.5 Target/Master Aborts

When a cycle initiated by the bridge is Master/Target aborted, the bridge will not re-attempt the same cycle. For multiple DW cycles, the bridge increments the address and attempts the next DW of the transaction. For all non-postable cycles, a Target abort response packet is returned for each DW that was Master or Target aborted on PCI. The bridge drops posted writes that abort.

5.3.2.6 Secondary Master Latency Timer

The bridge implements a Master Latency Timer by way of the SLT register which, upon expiration, causes the de-assertion of FRAME# at the next legal clock edge when there is another active request to use the PCI bus.

5.3.2.7 Dual Address Cycle (DAC)

The bridge will issue full 64-bit dual address cycles for device memory-mapped registers above 4 GB.

5.3.2.8 Memory and I/O Decode to PCI

The PCI bridge in the Intel® 631xESB/632xESB I/O Controller Hub is a **subtractive decode agent**, which follows the following rules when forwarding a cycle from ESI to the PCI interface:

- The PCI bridge will **positively decode** any memory I/O address within its window registers, assuming PCICMD.MSE (D30:F0:Offset 04h:bit 1) is set for memory windows and PCICMD.IOSE (D30:F0:Offset 04h:bit 0) is set for I/O windows.
- The PCI bridge will **subtractively decode** any 64-bit memory address not claimed by another agent, assuming PCICMD.MSE (D30:F0:Offset 04h:bit 1) is set.
- The PCI bridge will **subtractively decode** any 16-bit I/O address not claimed by another agent assuming PCICMD.IOSE (D30:F0:Offset 04h:bit 0) set
- If BCTRL.IE (D30:F0:Offset 3Eh:bit 2) is set, the PCI bridge **will not positively forward** from primary to secondary called out ranges in the I/O window per PCI specification (I/O transactions addressing the last 768 bytes in each, 1-KB block: offsets 100 h to 3 FFh). The PCI bridge will still take them subtractively assuming the above rules.
- If BCTRL.VGAE (D30:F0:Offset 3Eh:bit 3) is set, the PCI bridge will positively forward from primary to secondary I/O and memory ranges as called out in the PCI bridge specification, assuming the above rules are met.

5.3.3 Parity Error Detection and Generation

PCI parity errors can be detected and reported. The following behavioral rules apply:

- When a parity error is detected on PCI, the bridge sets the SECSTS.DPE (D30:F0:Offset 1Eh:bit 15).
- If the bridge is a Master and BCTRL.PERE (D30:F0:Offset 3Eh:bit 0) and one of the parity errors defined below is detected on PCI, then the bridge will set SECSTS.DPD (D30:F0:Offset 1Eh:bit 8) and will also generate an internal SERR#.
  - — During a write cycle, the PERR# signal is active, or
  - — A data parity error is detected while performing a read cycle
- If an address or command parity error is detected on PCI and PCICMD.SEE (D30:F0:Offset 04h:bit 8), BCTRL.PERE, and BCTRL.SEE (D30:F0:Offset 3Eh:bit 1) are all set, the bridge will set the PSTS.SSE (D30:F0:Offset 06h:bit 14) and generate an internal SERR#.
- If the PSTS.SSE is set because of an address parity error and the PCICMD.SEE is set, the bridge will generate an internal SERR#
- When bad parity is detected from ESI, bad parity will be driven on all data the bridge.
- When an address parity error is detected on PCI, the PCI bridge will never claim the cycle. This is a slight deviation from the PCI bridge spec, which says that a cycle should be claimed if BCTRL.PERE is not set. However, ESI does not have a concept of address parity error, so claiming the cycle could result in the rest of the system seeing a bad transaction as a good transaction.

5.3.4 PCIRST#

PCIRST# is generated under two conditions:

- PLTRST# active
- BCTRL.SBR (D30:F0:Offset 3Eh:bit 6) set to 1

The PCIRST# pin is in the resume well. PCIRST# should be tied to PCI bus agents, but not other agents in the system.

5.3.5 PCI-to-PCI Bridge Model

From a software perspective, the Intel® 631xESB/632xESB I/O Controller Hub contains a PCI-to-PCI bridge. This bridge connects ESI to the PCI bus. By using the PCI-to-PCI bridge software model, the Intel® 631xESB/632xESB I/O Controller Hub can have its decode ranges programmed by existing plug-and-play software such that PCI ranges do not conflict with graphics aperture ranges in the Host controller.

Note: All downstream should be disabled before reconfiguring the PCI Bridge. Failure to do so may cause undefined results.

5.3.6 IDSEL to Device Number Mapping

When addressing devices on the external PCI bus (with the PCI slots), the Intel® 631xESB/632xESB I/O Controller Hub asserts one address signal as an IDSEL. When accessing device 0, the Intel® 631xESB/632xESB I/O Controller Hub asserts AD16. When accessing Device 1, the Intel® 631xESB/632xESB I/O Controller Hub asserts AD17. This mapping continues all the way up to device 15 where the Intel® 631xESB/632xESB I/O Controller Hub asserts AD31. Note that the Intel® 631xESB/632xESB I/O Controller Hub's internal functions (AC'97, Intel High Definition Audio, IDE, USB, SATA and PCI Bridge) are enumerated like they are off of a separate PCI bus (ESI) from the external PCI bus.

5.3.7 Standard PCI Bus Configuration Mechanism

The PCI Bus defines a slot based "configuration space" that allows each device to contain up to eight functions with each function containing up to 256, 8-bit configuration registers. The *PCI Local Bus Specification, Revision 2.3* defines two bus cycles to access the PCI configuration space: Configuration Read and Configuration Write. Memory and I/O spaces are supported directly by the processor. Configuration space is supported by a mapping mechanism implemented within the Intel® 631xESB/632xESB I/O Controller Hub. The *PCI Local Bus Specification, Revision 2.3* defines two mechanisms to access configuration space, Mechanism 1 and Mechanism 2. The Intel® 631xESB/632xESB I/O Controller Hub supports only Mechanism 1.

Warning: Configuration writes to internal devices, when the devices are disabled, are illegal and may cause undefined results.

5.4 Integrated LAN Controller and SERDES/Kumeran Interface

The Intel® 631xESB/632xESB I/O Controller Hub integrated LAN controller employs a 4 wire per port interface for use in connecting to an external PHY. This interface, called Kumeran, was reduced to 4 wires per port by incorporating the MII management interface into the packet data pins, thus reducing pin count and easing board layout constraints.

5.4.1 Integrated LAN Controller

The Intel® 631xESB/632xESB I/O Controller Hub integrated LAN Controller provides 4 lanes of PCI Express bus interface working at 2.5 GHz each, providing sufficient bandwidth to support sustained dual-port 1000 Mb/s transfer rates. A configurable 48 Kbytes of on-chip buffer mitigates instantaneous receive bandwidth demands and eliminates transmit under–runs by buffer the entire outgoing packet prior to transmission.

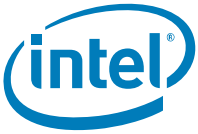
Numerous features have been incorporated to allow greater throughput with less direct CPU intervention. The LAN controller implements TCP segmentation offload. The controller also has the ability to split the Ethernet header information from the payload of the packet, allowing the OS protocol stack to access the packets header in a cacheable memory while the packets payload remain in non cacheable memory improving headers access time by eliminating cache misses, thus saving CPU cycles and improve overall performance. It also supports fragmented UDP checksum offload for packet reassembly. Dual transmit and receive queues for Receive Side Scaling (RSS), QoS, and other programmable usage models are also supported.

The device also supports programmable host memory receive buffers from 1 Kbytes to 16 Kbytes in 1-Kbyte increments, allowing for the most flexible usage model across a large array of packet sizes, including Jumbo Frames of up to 9014 bytes in size.

The Intel® 631xESB/632xESB I/O Controller Hub integrated LAN Controller provides a serial FLASH interface, along with a SPI EEPROM interface. The EEPROM contains power on initialization for the hardware and software configuration parameters, along with some configuration information used in the external PHY.

The following list summarizes some of the features of the Intel® 631xESB/632xESB I/O Controller Hub Integrated LAN Controller:

- PCI Express host interface with 4 lanes support
- Intel® I/O Acceleration Technology support
- Dual Kumeran interface to two external 1000BASE-T PHYs (specifications in a separate document)
- Multi-speed operation: 10/100/1000 Mbyte/s
- Half duplex and full duplex operation at all supported speeds (except for half-duplex mode, not supported in gigabit speed)
- 64-bit address support for systems using more than 4 Gbytes of physical memory
- Programmable flexible host memory receive buffers (1KB to 16KB) in 1KB increments.
- Support Jumbo frames of up to 9014 bytes long
- Descriptor ring management hardware for transmit and receive
- SERDES Auto-Negotiation



- Flow Control Support: send/receive PAUSE frames and receive FIFO thresholds
- ACPI register set and power down functionality supporting D0 and D3 states
- Software-controlled global reset bit (resets everything except the configuration registers)
- 802.1q VLAN support
- TCP Segmentation capability compatible with NT 5.x “Large Send” offloading features
- Message Signaled Interrupts support
- Wakeup the system through PE_WAKE pin upon various network wakeup packets and events
- Pass through-compatible SMB-based management packet transmit/receive support
- Support for Ipv6 including:
  - Ipv6 support for IP/TCP and IP/UDP receive checksum offload
  - Ipv6 wake-up filters
- Intelligent interrupt generation features to enhance driver performance:
- Packet interrupt coalescing timers (packet timers) and absolute-delay interrupt timers for both transmit and receive operation
  - Transmit Descriptor-Ring “Low” Description
  - Interrupt Throttling control to limit maximum interrupt rate and improve CPU utilization
- Configurable LED operation for software or OEM customization of LED displays
- Configurable 48-Kbyte receive and transmit data FIFO
- Serial FLASH interface
- SPI EEPROM interface
- Protected EEPROM space for private configuration
- Programmable cache line size of 64 bytes or128 bytes
- ACK-packet detection delayed interrupt for improved response time to TCP acknowledges
- Additional statistics to enhance new interrupt features
- Programmable flexible host memory receive buffers (1 Kbyte to 16 Kbytes) in 1-Kbyte increments
- SERDES interface for external PHY connection or System interconnect
- Dual Transmit and Receive queues for Receive Side Scaling (RSS), QoS and other programmable usage models
- Fragmented UDP checksum offload for packet reassembly
- Default configuration by EEPROM for all LEDs for pre-driver functionality
- 8 VLAN tag Flex Filters
- Updated RSS engine to support Microsoft Toeplitz RSS hash algorithm

5.4.2 Packet Reception and Transmission

In the general case, packet reception consists of recognizing the presence of a packet on the wire, performing address filtering, storing the packet in the receive data FIFO, transferring the data to one of the two receive queues in host memory, and updating the state of a receive descriptor.

Output packets are made up of pointer-length pairs constituting a descriptor chain. Software forms transmit packets by assembling the list of pointer-length pairs, storing this information in the transmit descriptor, and then updating the on-chip transmit tail pointer to the descriptor. The transmit descriptor and buffers are stored in host memory. Hardware typically transmits the packet only after it has completely fetched all packet data from host memory and deposited it into the on-chip transmit FIFO. This permits TCP or UDP checksum computation, and avoids under-runs due to PCI Expressx latency.

5.4.3 Buffer and Descriptor Structure

Software allocates transmit and receive buffers and forms descriptors that contain pointers to, and status of, those buffers. A conceptual ownership boundary exists between the driver software and the hardware for buffers and descriptors.

Software gives hardware ownership of a queue of buffers for receive. These buffers store data that software acquires ownership of once valid packets arrive.

For transmit, software maintains a queue of buffers. The driver "owns" a buffer until it is ready to transmit. Software commits the buffer to the hardware at which time the hardware "owns" the buffer until data is transmitted or loaded in the transmit FIFO.

Descriptors store information about the buffers. They contain the physical address, length, and status information about the referenced buffer. An end-of-packet field indicates the last buffer for a packet.

The descriptors also contain packet specific information indicating type of packet and specific operations to perform in the context of transmitting a packet such as those for VLAN or checksum offload support.

5.4.4 LAN Controller PCI Express* Bus Interface

As a Gigabit Ethernet controller, the role of the Intel® 631xESB/632xESB I/O Controller Hub integrated LAN controller is to fetch data for transmission and transmit on the network and receive data from the network and deposit into host memory. The LAN controller, as a Bus Master device, initiates memory cycles by way of the PCI Express bus to fetch or deposit the required data. To perform these actions, the LAN controller is controlled and examined by the processor by way of its control and status structures and registers. Some of these control and status structures reside in the LAN controller and some reside in system memory. For access to the LAN controller's Control/Status Registers (CSR), the LAN controller acts as a Slave (in other words, a target device). The LAN controller serves as a Slave also while the processor accesses the EEPROM or Flash devices.

5.4.4.1 Functionality

The PCI Express capability register states the device/port type. In the Intel® 631xESB/632xESB I/O Controller Hub integrated LAN controller, all functions besides the IDE and UHCI are defined as Native devices. In the Intel® 631xESB/632xESB I/O Controller Hub integrated LAN controller, IDE definition as a PCI Express native or legacy endpoint

is determined by the *Legacy Endpoint* bit in the *PCI Express init configuration 2 word* (word 19h). The UHCI definition is set by UHCI Device Type bit in the *Functions Control 2 word* (word 2Eh). The control bits are loaded from EEPROM.

The Intel® 631xESB/632xESB I/O Controller Hub integrated LAN controller is native device by default. The device does not support locked requests as Target or Master.

5.4.4.1.1 Transaction Layer

The upper layer of the PCI Express architecture is the Transaction Layer. The Transaction layer connects to the device core using an implementation specific protocol. Through this core-to-Transaction-layer protocol, the application-specific parts of the device interact with the PCI Express subsystem and transmit and receive Requests to or from the remote PCI Express Agent, respectively.

5.4.4.1.2 Transaction Initiated by Intel® 631xESB/632xESB I/O Controller Hub as Master

The Intel® 631xESB/632xESB I/O Controller Hub supports the following subset transaction types as a Master:

Table 5-15 depicts the PCI Express packet types supported as Master.

Table 5-15. Packet Type Initiated as Master

Request	Packet Type	Payload Size	Comments
Memory Read	MRd	None	Request is limited to 512 bytes. Both 32- and 64-bit addresses.
Posted Memory Write	MWr	≤ MAX_PAYLOAD_SIZE (see Note)	Both 32- and 64-bit addresses.
Target Read Completions	CplD	DWord	Data to be returned in a single completion packet.
Target I/O Read Completion	Cpl	None	32-bit addressing only.
Target I/O Write Completion	CplD	DWord	32-bit addressing only.
Configuration Read Completion	Cpl	DWord	32-bit addressing only.
Configuration Write Completion	Cpl	None	32-bit addressing only
System Messages	Msg MsgD	Message specific	For various standard messages, some with Data, and some requiring Completion
Unsuccessful Reception	Cpl	None	Unsuccessful completion

Note: MAX_PAYLOAD_SIZE is loaded from EEPROM (either 128 or 256 bytes).

Table 5-16 lists the standard messages generated by the Intel® 631xESB/632xESB I/O Controller Hub as Master.

Table 5-16. Standard Messages Initiated by the Intel® 631xESB/632xESB I/O Controller Hub

Message	Description/Comments
ERR_COR	Signal detection of a correctable error
ERR_UNC	Signal detection of an uncorrectable error
ERR_FATAL	Signal detection of a fatal error
PM_Enter_L2	Request to transition the link to L2
PM_PME	PME message conveying the ID of the PME originator
PME_TO_Ack	Acknowledge turn-off of Link clock and power
Assert_INTA	Assert INTA virtual signal
Deassert_INTA	Deassert INTA virtual signal
Assert_INTB	Assert INTB virtual signal
Deassert_INTB	Deassert INTB virtual signal

5.4.4.1.3 Alignment

Requests must never specify an Address/Length combination that causes a Memory Space access to cross a 4-Kbyte boundary. It is the hardware's responsibility to break requests into 4-Kbyte-aligned requests (if needed). This does not pose any requirement on the software. However, if the software allocates a buffer across a 4-Kbyte boundary, hardware will issue multiple requests for the buffer. Software should consider aligning buffers to 4-Kbyte boundaries in cases where it improves performance.

It is also recommended that requests be multiples of 64 bytes and aligned to make better use of memory controller resources.

5.4.4.1.4 Transactions Supported by the Intel® 631xESB/632xESB I/O Controller Hub as the Target

The Intel® 631xESB/632xESB I/O Controller Hub supports the following subset transaction types as target:

Table 5-17 depicts the PCI Express packet types supported as target.

Table 5-17. Packet Types Supported as Target (Sheet 1 of 2)

Request	Packet Type	Payload Size	Comments
Target Read	MRd	None	The Intel® 631xESB/632xESB I/O Controller Hub supports target read requests of up to 64-bits. Longer requests will be accepted and dropped internally[1]. Both 32-bit and 64-bit addresses.
Target Posted Write	MWr	DWord	The Intel® 631xESB/632xESB I/O Controller Hub supports target writes of up to 64-bits. Longer writes will be accepted and dropped internally[2]. Both 32-bit and 64-bit addresses
Target I/O Read	IORd	None	32-bit addressing only.
Target I/O Write	IOWr	Dword	32-bit addressing only.
Master Read Completion	CplD	≤ MAX_PAYLOAD_SIZE	In-order completions of read request.
Configuration Read	CfgRd0	None	Both PCI compatible and PCI Express Enhanced configurations.

Table 5-17. Packet Types Supported as Target (Sheet 2 of 2)

Request	Packet Type	Payload Size	Comments
Configuration Write	CfgWr0	DWord	Both PCI compatible and PCI Express Enhanced configurations.
System Messages	Msg MsgD	Message specific	For various standard messages, some with Data, and some requiring Completion.
Completion with unsuccessful status	Cpl	None	See Table 5-22.

Notes:
1. Read requests larger than 8 Bytes (2 DWords) are acknowledged with a "UR" completion status.
2. In case of a write request larger than 8 Bytes (2 DWords), an internal error bit is set in the error reporting registers and a message error is reported according to the error reporting status.

Table 5-18 lists the standard messages accepted by the Intel® 631xESB/632xESB I/O Controller Hub as target:

Table 5-18. Standard Messages accepted by the Intel® 631xESB/632xESB I/O Controller Hub as Target

Message	Description/Comment
PM_Active_State_NAK	Rejection of request to enter a low power state.
PME_Turn_Off	Notification of pending turn-off of Link clock and power.

5.4.4.1.5 Host I/F

PCI Express Device numbers identify logical devices within the physical device (Intel® 631xESB/632xESB I/O Controller Hub LAN core is a physical device). Intel® 631xESB/632xESB I/O Controller Hub LAN core implements a single logical device with seven separate PCI Functions: LAN 0 and LAN 1. The device number is captured from each Type 0 configuration write transaction.

Each of the PCI Express functions interfaces with the unit through one or more clients. A client ID identifies the client and is included in the Tag field of the packet header. Completions always carry the tag value included in the request to allow routing of the completion to the appropriate client.

Client Ids are assigned as shown in Table 5-19.

Table 5-19. Assignment of Client IDs (Sheet 1 of 2)

Tag	Module	Client
00h	DMA Rx	Write data from Ethernet to main memory
01h	DMA Rx	Read descriptor to core
02h	DMA Rx	Write back descriptor from core to memory
04h	DMA Tx	Read descriptor to core
05h	DMA Tx	Write back descriptor from core to memory
06h	DMA Tx	Read descriptor to core second queue
07h	DMA Tx	Write back descriptor from core to memory second queue
08h	DMA TX	Read data 0 from main memory to Ethernet
09h	DMA TX	Read data 1 from main memory to Ethernet
0Ah	DMA TX	Read data 2 from main memory to Ethernet

Table 5-19. Assignment of Client IDs (Sheet 2 of 2)

Tag	Module	Client
0Bh	DMA TX	Read data 3 from main memory to Ethernet
0Ch	DMA RX	Write descriptor to core second queue
0Eh	DMA RX	Write back descriptor from core to memorysecond Queue
10h	MNG	Read data
11h	MNG	Write data
1Eh	PCI Express	MSI
1Fh	PCI Express	Message Unit
Others	Reserved	

5.4.4.1.6 PCI Power Management

Enhanced support for the power management standard, *PCI Local Bus Specification, Revision 2.3*, and PCI Express specification is provided in the Intel® 631xESB/632xESB I/O Controller Hub integrated LAN controller. The LAN controller supports a large set of wake-up packets and the capability to wake the system from a low power state on a link status change. The LAN controller enables the host system to be in a sleep state and remain virtually connected to the network. After a power management event or link status change is detected, the LAN controller wakes the host system. The sections below describe these events, the LAN controller power states, and estimated power consumption at each power state.(The estimated power consumption refers to Chapeter6)

The LAN controller contains power management registers for PCI, and implements two power states, D0 and D3, which vary from maximum power consumption at D0 to the minimum-power consumption at D3. PCI transactions are allowed in only the D0 state, except for host accesses to the LAN controller's PCI configuration registers. D0 is divided into two sub-states: D0u and D0a. Additionally, the controller supports a Dr state that is entered when PERST# is de-asserted (including the $D3_{cold}$ state).In the D3 cold state, the LAN controller can provide wake-up capabilities. Wake-up indications from the LAN controller are provided by either the PE_WAKE# signal or a power management message according to the link state of the PCI Express.

The amount of power required for the function is advertised in the Power Management Data Register, which is loaded from the EEPROM.

If D3cold is supported, the PME_En and PME_Status bits of the Power Management Control/Status Register (PMCSR), as well as their shadow bits in the Wake Up Control Register (WUC) will be reset only by the power up reset (detection of power rising).

5.4.4.2 Reset Operation

The Intel® 631xESB/632xESB I/O Controller Hub integrated LAN controller's reset sources are described below:

- **LAN_PWR_GOOD** – This reset acts as a Master reset of the entire LAN controller. It is level sensitive, and while it is 0 will hold all of the LAN controller's registers in reset. LAN_PWR_GOOD is interpreted to be an indication that device power supplies are all stable. LAN_PWR_GOOD changes state during system power-up.
- **PERST# –** The assertion of PERST# indicates that both the power and the PCI Express clock sources are stable. This pin will assert an internal reset also after a D3cold exit. Most units are reset on the rising edge of PERST#. The only exception is the GIO unit, which is kept in reset while PERST# is de-asserted (level).

- **In-Band PCI Express Reset** – The Intel® 631xESB/632xESB I/O Controller Hub's integrated LAN controller will generate an internal reset in response to a Physical layer message from a PCI Express bus or when the PCI Express link goes down (entry to Polling or Detect state). This reset is equivalent to PCI reset in previous (PCI) gigabit LAN controllers.
- **$D3_{hot}$ to D0 transition –** This is also known as ACPI Reset. The Intel® 631xESB/632xESB I/O Controller Hub's integrated LAN controller generates an internal reset on the transition from $D3_{hot}$ power state to D0 (caused after configuration writes from D3 to D0 power state). Note that this reset is per function and resets only the function that transitioned from $D3_{hot}$ to D0.
- **Software Reset** – Software can reset the Intel® 631xESB/632xESB I/O Controller Hub integrated LAN controller by writing the Device Reset bit of the Device Control Register (CTRL.RST). The Intel® 631xESB/632xESB I/O Controller Hub's integrated LAN controller re-reads the per-function EEPROM fields after a software reset. Bits that are normally read from the EEPROM will be reset to their default hardware values. Note that this reset is per function and resets only the function that received the software reset. PCI Configuration space (configuration and mapping) of the device is unaffected.
- **Force TCO** – This reset is generated when manageability logic is enabled. It will be generated only if the Reset on Force TCO bit of the EEPROM's Management Control word is 1. In pass through mode it is generated when receiving a ForceTCO SMB command with bit 1 or bit 7 set.
- **Firmware (FW) Reset** – This reset is activated by writing a 1 to the FWR bit in the HOST Interface Control Register (HICR) in CSR address 0x8F00.
- **SERDES Link Reset** – When the Link Reset bit of the Device Control Register (CTRL.LRST) is written as a logic 1, the device is forced into a link reset state. In this state SERDES auto-negotiation is disabled. The transmitter will send /C/ ordered sets when Link Reset is 1. Auto-negotiation is initiated/restarted when LRST is transitions to 0. A link reset is relevant in only SERDES mode.
- **EEPROM Reset** – Writing a 1 to the EEPROM Reset bit of the Extended Device Control Register (CTRL_EXT.EE_RST) will cause the LAN controller to re-read the per-function configuration from the EEPROM, setting the appropriate bits in the registers loaded by the EEPROM.
- P**HY Reset** – Software can write a 1 to the PHY Reset bit of the Device Control Register (CTRL.PHY_RST) to reset the 82563 EB/82564 EB, through Kumeran interface. Intel® 631xESB/632xESB I/O Controller Hub MMS (Management Microcontroller System) unit must configure the PHY following a PHY Reset.

5.4.5 Wake-Up

The Intel® 631xESB/632xESB I/O Controller Hub's integrated LAN controller supports following wakeup mechanism:

- PCI Express Power Management Wakeup

The PCI Express Power Management Wakeup uses the PE_WAKE# pin to wake the system up.

5.4.5.1 PCI Express* Power Management Wakeup

The Intel® 631xESB/632xESB I/O Controller Hub's integrated LAN controller supports PCI Express Power Management based Wakeups. It can generate system wake-up events from three sources:

- Reception of a “Magic Packet”.
- Reception of a Network Wakeup Packet.
- Detection of a link change of state.

Activating PCI Express Power Management Wakeup requires the following steps:

- The driver programs the Wake Up Filter Control Register (WUFC) to indicate the packets it wishes to wake up and supplies the necessary data to the IPv4/v6 Address Table (IP4AT, IP6AT) and the Flexible Filter Mask Table (FFMT), Flexible Filter Length Table (FFLT), and the Flexible Filter Value Table (FFVT). It can also set the Link Status Change Wake Up Enable (LNKC) bit in the Wake Up Filter Control Register (WUFC) to cause wakeup when the link changes state.
- The OS (at configuration time) writes a 1 to the Pme_En bit of the Power Management Control / Status Register (PMCSR.8).

Normally, after enabling wakeup, the OS will write 11b to the lower two bits of the PMCSR to put the Intel® 631xESB/632xESB I/O Controller Hub’s integrated LAN controller into low-power mode.

Once Wakeup is enabled, the Intel® 631xESB/632xESB I/O Controller Hub’s integrated LAN controller monitors incoming packets, first filtering them according to its standard address filtering method, then filtering them with all of the enabled wakeup filters. If a packet passes both the standard address filtering and at least one of the enabled wakeup filters, the Intel® 631xESB/632xESB I/O Controller Hub’s integrated LAN controller will:

- Set the PME_Status bit in the Power Management Control / Status Register (PMCSR)
- If the PME_En bit in the Power Management Control / Status Register (PMCSR) is set, assert PE_WAKE# or send an inband PME message.
- Store the first 128 bytes of the packet in the Wakeup Packet Memory.
- Set one or more of the “Received” bits in the Wake Up Status Register (WUS). (The Intel® 631xESB/632xESB I/O Controller Hub will set more than one bit if a packet matches more than one filter.)
- Set the packet length in the Wake Up Packet Length Register (WUPL).

If enabled, a link state change wakeup will cause similar results, setting PME_Status, asserting PE_WAKE# or send an inband PME message and setting the Link Status Changed (LNKC) bit in the Wake Up Status Register (WUS) when the link goes up or down.

PE_WAKE# will remain asserted until the OS either writes a 1 to the PME_Status bit of the PMCSR register or writes a 0 to the Pme_En bit.

After receiving a wakeup packet, the Intel® 631xESB/632xESB I/O Controller Hub’s integrated LAN controller will ignore any subsequent wakeup packets until the driver clears all of the “Received” bits in the Wake Up Status Register (WUS). It will also ignore link change events until the driver clears the Link Status Changed (LNKC) bit in the Wake Up Status Register (WUS).

5.4.5.2 Wakeup Packets

In PCI Express power management mode, the Intel® 631xESB/632xESB I/O Controller Hub’s integrated LAN controller supports various wakeup packets using two types of filters:

- Pre-defined Filters
- Flexible Filters

Each of these filters will be enabled if the corresponding bit in the Wake Up Filter Control Register (WUFC) is set to 1.

5.4.5.2.1 Pre-defined Filters

The following packets are supported by Intel® 631xESB/632xESB I/O Controller Hub LAN core's Pre-defined Filters:

- Directed Packet (including exact, multicast indexed, and broadcast)
- Magic Packet
- ARP/IPv4 Request Packet
- Directed IPv4 Packet
- Directed IPv6 Packet

Each of these filters will be enabled if the corresponding bit in the Wakeup Filter Control Register (WUFC) is set to 1.

The explanation of each filter includes a table showing which bytes at which offsets are compared to determine if the packet passes the filter. Both VLAN frames and LLC/Snap can increase the given offsets if they are present.

5.4.5.2.2 Directed Exact Packet

The Intel® 631xESB/632xESB I/O Controller Hub's integrated LAN controller will generate a wakeup event upon reception of any packet whose destination address matches one of the 16 valid programmed Receive Addresses if the Directed Exact Wake Up Enable bit is set in the Wake Up Filter Control Register (WUFC.EX).

Offset	# of Bytes	Field	Value	Action	Comment
0	6	Destination Address		Compare	Match any pre-programmed address

5.4.5.2.3 Directed Multicast Packet

For multicast packets, the upper bits of the incoming packet's destination address index a bit vector, the Multicast Table Array that indicates whether to accept the packet. If the Directed Multicast Wake Up Enable bit set in the Wake Up Filter Control Register (WUFC.MC) and the indexed bit in the vector is one then Intel® 631xESB/632xESB I/O Controller Hub will generate a wakeup event. The exact bits used in the comparison are programmed by software in the Multicast Offset field of the Receive Control Register (RCTL.MO).

Offset	# of Bytes	Field	Value	Action	Comment
0	6	Destination Address		Compare	See above paragraph

5.4.5.2.4 Broadcast

If the Broadcast Wake Up Enable bit in the Wake Up Filter Control Register (WUFC.BC) is set the Intel® 631xESB/632xESB I/O Controller Hub's integrated LAN controller will generate a wake up event when it receives a broadcast packet.

Offset	# of Bytes	Field	Value	Action	Comment
0	6	Destination Address	FF*6h	Compare	

5.4.5.2.5 Magic Packet

Magic packets are defined as follows:

Magic Packet Technology Details

Once the LAN controller has been put into the Magic Packet mode, it scans all incoming frames addressed to the node for a specific data sequence, which indicates to the controller that this is a Magic Packet frame. A Magic Packet frame must also meet the basic requirements for the LAN technology chosen, such as SOURCE ADDRESS, DESTINATION ADDRESS (which may be the receiving station's IEEE address or a MULTICAST address which includes the BROADCAST address), and CRC. The specific data sequence consists of 16 duplications of the IEEE address of this node, with no breaks or interruptions. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream. The synchronization stream allows the scanning state machine to be much simpler. The synchronization stream is defined as 6 bytes of FFh.

The Intel® 631xESB/632xESB I/O Controller Hub's integrated LAN controller will expect the destination address to either:

1. Be the broadcast address (FF.FF.FF.FF.FF.FF)
2. Match the value in Receive Address Register 0 (RAH0, RAL0). This is initially loaded from the EEPROM but may be changed by the driver.
3. Match any other address filtering enabled by the driver.

The Intel® 631xESB/632xESB I/O Controller Hub's integrated LAN controller will search for the contents of *Receive Address Register 0* (RAH0, RAL0) as the embedded IEEE address. It will consider any non-FFh byte after a series of at least 6 FFs to be the start of the IEEE address for comparison purposes. (that is,. It will catch the case of 7 FFs followed by the IEEE address). As soon as one of the first 96 bytes after a string of FFs doesn't match, it will continue to search for anther set of at least 6 FFs followed by the 16 copies of the IEEE address later in the packet. Note that this definition precludes the first byte of the destination address from being FF.

A Magic Packet's destination address must match the address filtering enabled in the configuration registers with the exception that broadcast packets will be considered to match even if the *Broadcast Accept* bit of the *Receive Control Register* (RCTL.BAM) is 0.

5.4.5.2.6 ARP/IPv4 Request Packet

The Intel® 631xESB/632xESB I/O Controller Hub's integrated LAN controller will support reception of ARP Request packets for wake up if the ARP bit is set in the Wake Up Filter Control Register (WUFC). Four IPv4 addresses are supported which are programmed in the IPv4 Address Table (IP4AT). A successfully matched packet must contain a broadcast MAC address, a Protocol Type of 0x0806, an ARP OPCODE of 0x01, and one of the four programmed IPv4 addresses. The Intel® 631xESB/632xESB I/O Controller Hub's integrated LAN controller also handles ARP Request packets that have VLAN tagging on both Ethernet II and Ethernet SNAP types.

5.4.5.2.7 Directed IPv4 Packet

The Intel® 631xESB/632xESB I/O Controller Hub's integrated LAN controller will support reception of Directed IPv4 packets for wake up if the IPV4 bit is set in the Wake Up Filter Control Register (WUFC). Four IPv4 addresses are supported which are programmed in the IPv4 Address Table (IP4AT). A successfully matched packet must contain the station's MAC address, a Protocol Type of 0x0800, and one of the four programmed IPv4 addresses. The Intel® 631xESB/632xESB I/O Controller Hub's integrated LAN controller also handles Directed IPv4 packets that have VLAN tagging on both Ethernet II and Ethernet SNAP types.

5.4.5.2.8 Directed IPv6 Packet

The Intel® 631xESB/632xESB I/O Controller Hub's integrated LAN controller will support reception of Directed IPv6 packets for wake up if the IPV6 bit is set in the Wake Up Filter Control Register (WUFC). One IPv6 address is supported and it is programmed in the IPv6 Address Table (IP6AT). A successfully matched packet must contain the station's MAC address, a Protocol Type of 0x0800, and the programmed IPv6 address. The Intel® 631xESB/632xESB I/O Controller Hub's integrated LAN controller also handles Directed IPv6 packets that have VLAN tagging on both Ethernet II and Ethernet SNAP types.

5.4.5.2.9 Flexible Filter

Intel® 631xESB/632xESB I/O Controller Hub LAN supports a total of four flexible filters. Each filter can be configured to recognize any arbitrary pattern within the first 128 byte of the packet. To configure the flexible filter, the software programs the mask values, the required values and the minimum packet length. Once enabled, the flexible filters will scan incoming packets for a match. If the filter encounters any byte in the packet where the mask bit is one and the byte doesn't match the byte that was programmed by software, then the filter will fail that packet. If the filter reaches the required length without failing the packet, it passes the packet and generates a wake up event. It will ignore any mask bits set to one beyond the required length. The minimum length of the pattern that is supported is 2 bytes.

5.4.6 CSMA/CD Unit

The Intel® 631xESB/632xESB I/O Controller Hub's integrated LAN controller MAC provides a complete CSMA/CD function supporting IEEE 802.3 (10Mb/s), 802.3u (100Mb/s), 802.3z and 802.3ab (1000Mb/s) implementations. The device performs all of the functions required for transmission, reception and collision handling called out in the standards.

5.4.6.1 Speed and Duplex

The Intel® 631xESB/632xESB I/O Controller Hub LAN controller can operate in 10Mb/s, 100Mb/s and 1Gb/s. It supports both half duplex and full duplex when working in 10/100Mb/s and full duplex in only 1Gb/s.

When operating in full-duplex mode, the LAN controller can transmit and receive frames simultaneously. Transmission starts regardless of the state of the internal receive path. When operating in half duplex, it can either receive or transmit at any given time. In this mode, transmission will start only when there is no carrier sense on the line, according to the 802.3 standard. Reception starts when the external PHY detects a valid frame on its receive differential pair. For proper operation, both the LAN controller CSMA/CD module and the external PHY must operate in the same speed and duplex mode. Following reset, the external PHY negotiates the speed and duplex with

its link partner according o the 802.3 standard and selects the highest speed and duplex supported by both sides. The speed can also be forced by the LAN driver, in which case, only half duplex is supported. The Intel® 631xESB/632xESB I/O Controller Hub LAN controller receives status indications about the external PHY's speed and duplex over the Kumeran interface and sets its speed and duplex accordingly

5.4.6.2 Flow Control

The LAN controller supports IEEE 802.3x frame-based flow control frames in only full duplex switched environment. The LAN controller flow control feature is not intended to be used in shared media environments.

Flow control is optional in full-duplex mode and is selected through software configuration. When flow control is enabled, the Intel® 631xESB/632xESB I/O Controller Hub LAN controller tracks its receive buffer free space and sends pause packets to the link partner to prevent the receive FIFO from overflow. Upon reception of a flow control packet, the Intel® 631xESB/632xESB I/O Controller Hub LAN ceases transmission as a mean of protecting the link partner's receive buffer.

5.4.7 802.1q VLAN Support

The Intel® 631xESB/632xESB I/O Controller Hub's integrated LAN controller provides several specific mechanisms to support 802.1q VLANs:

- Optional adding (for transmits) and stripping (for receives) of IEEE 802.1q VLAN tags.
- Optional ability to filter packets belonging to certain 802.1q VLANs.

5.4.7.1 Transmitting and Receiving 802.1q packets

Since the 802.1q tag is only four bytes, adding and stripping of tags could be done completely in software. (In other words, for transmits, software inserts the tag into packet data before it builds the transmit descriptor list, and for receives, software strips the 4 byte tag from the packet data before delivering the packet to upper layer software.)

However, because adding and stripping of tags in software results in more over-head for the host, the Intel® 631xESB/632xESB I/O Controller Hub's integrated LAN controller has additional capabilities to add and strip tags in hardware.

5.4.7.1.1 Adding 802.1q tags on transmits

Software may command the Intel® 631xESB/632xESB I/O Controller Hub's integrated LAN controller to insert an 802.1q VLAN tag on a per packet basis. If CTRL.VME is set to 1, and the VLE bit in the transmit descriptor is set to 1, then the Intel® 631xESB/ 632xESB I/O Controller Hub's integrated LAN controller will insert a VLAN tag into the packet that it transmits over the wire.

5.4.7.1.2 Stripping 802.1q tags on receives

Software may instruct the Intel® 631xESB/632xESB I/O Controller Hub's integrated LAN controller to strip 802.1 q VLAN tags from received packets. The Intel® 631xESB/ 632xESB I/O Controller Hub's integrated LAN controller will indicate by way of the descriptor that the packet had a VLAN tag that was stripped.

5.4.8 EEPROM Interface

5.4.8.1 General Overview

Intel® 631xESB/632xESB I/O Controller Hub uses an EEPROM device for storing product configuration information. The EEPROM is divided into three general regions:

- Hardware accessed – loaded by Intel® 631xESB/632xESB I/O Controller Hub after power-up, PCI Reset de-assertion, D3 --> D0 transition, or software commanded EEPROM read (CTRL_EXT.EE_RST).
- Software accessed – used by software only.
- Firmware accessed – used by BMC firmware.

5.4.8.2 EEPROM Device

The EEPROM interface supports an SPI interface mode 0. It expects the EEPROM to be capable of 2MHz operation.

Intel® 631xESB/632xESB I/O Controller Hub is compatible with many sizes of 4-wire serial EEPROM devices. If flexibility mode functionality is desired, up to 256 Kbit serial SPI compatible EEPROM may be used. If no manageability or only pass-through mode is desired a 4 Kbit serial SPI compatible EEPROM may be used. All EEPROMs are accessed in 16-bit words (to be compatible with older designs) although the EEPROM is designed to accept also an 8-bit data accesses.

Intel® 631xESB/632xESB I/O Controller Hub will automatically determine the address size to be used with the SPI EEPROM it is connected to and set the EEPROM Size field of the EEPROM/FLASH Control and Data Register (EEC.EE_ADDR_SIZE) field appropriate. Software can use this size to determine how to access the EEPROM. The exact size of the EEPROM will be determined within one of the EEPROM words.

Note: The different EEPROM sizes have two differing numbers of address bits (8 bits or 16 bits), and therefore must be accessed with a slightly different serial protocol. Software must be aware of this if it accesses the EEPROM using direct access.

5.4.8.3 Software Accesses

Intel® 631xESB/632xESB I/O Controller Hub provides two different methods for software access to the EEPROM. It can either use the built-in controller to read the EEPROM, or access the EEPROM directly using the EEPROM's 4-wire interface. Please refer to the Intel® 631xESB/632xESB I/O Controller Hub LAN EEPROM Map and Programming Information document for more information about software access to the EEPROM.

5.4.9 Serial Flash Interface

Intel® 631xESB/632xESB I/O Controller Hub provides an external serial interface to a Flash, or Boot ROM, device such as the Atmel AT25F1024 or AT25FB512. All accesses to this device are controlled by Intel® 631xESB/632xESB I/O Controller Hub and are accessible to software as normal PCI reads or writes to the Flash memory mapping range. Intel® 631xESB/632xESB I/O Controller Hub supports serial FLASH devices with up to 64 Mb (8 MB) of memory. The size of the Flash implemented with Intel® 631xESB/632xESB I/O Controller Hub may be encoded into bits in the EEPROM. The Flash and Expansion ROM BARs are reconfigured based on these EEPROM settings.

Flash interface type is SPI mode 0.

5.4.9.1 Flash Interface Operation

Intel® 631xESB/632xESB I/O Controller Hub provides two different methods for software access to the Flash. The flash can either be accessed by direct memory mapping, or software can directly control the 4-wire interface. By default the flash can only be read. To allow write operations, software has to enable write to the flash in the flash control and data register.

Using the legacy Flash transactions the Flash is read from, or written to, whenever the host CPU performs a read or a write operation to a memory location that is within the FLASH address mapping or upon boot by way of accesses in the space indicated by the Expansion ROM Base Address Register. All accesses to the Flash require the appropriate command sequence for the device used. Refer to the specific Flash data sheet for more details on reading from or writing to Flash. Accesses to the Flash are based on a direct decode of CPU accesses to a memory window defined in either:

1. Intel® 631xESB/632xESB I/O Controller Hub's Flash Base Address Register (PCI Express Control Register at offset 14h).
2. A certain address range of the IOADDR register defined by the IO Base Address Register (PCI Express Configuration Register at offset 18 h).
3. The Expansion ROM Base Address Register (PCI Express Control Register at offset 30 h).

Intel® 631xESB/632xESB I/O Controller Hub controls accesses to the Flash when it decodes a valid access.

Another way for SW to access the Flash is directly using the Flash's 4-wire interface through the Flash Access Register. It can use this for reads, writes, or other Flash operations (accessing the Flash status register, erase).

5.4.9.2 Flash Write Control

The Flash is write controlled by the 2 bits in the EEPROM/FLASH Control and Data Register (EEC.FWE). Note that attempts to write to the Flash device should not be attempted when writes are disabled(FWE=01). Behavior after such an operation is undefined, and may result in component and/or system hangs.

After sending one byte write to the flash, SW can check if it can send the next byte to write (check if the write process in the Flash had finished) by reading the Flash Access Register, If bit (FLA.FL_BUSY) in this register is set the current write did not finished, If bit (FLA.FL_BUSY) is clear then the SW can continue and write the next byte to the Flash.

Note: Writing to the Serial Flash should be done, taking in account the limitations of the page boundaries, specifically to the flash memory type.

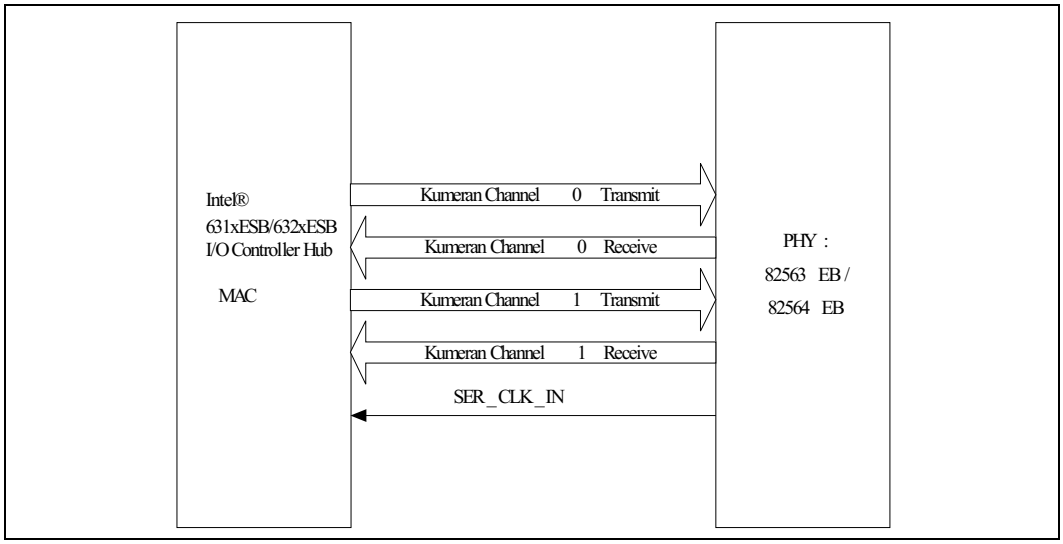
5.4.10 Intel® 631xESB/632xESB I/O Controller Hub MAC-PHY Interconnection

This section summarizes the modes of connection between MAC and PHY.

5.4.10.1 Intel® 631xESB/632xESB I/O Controller Hub – PHY Kumeran Connection

This is the default connection between the Intel® 631xESB/632xESB I/O Controller Hub and Intel Dual/Single 1Gb PHY - 82563EB/82564EB. The interface is based on the Kumeran which is Intel proprietary reduced pin count MAC-PHY interface. Information about the Kumeran signals and electrical specifications can be found in the separated Kumeran Specification.

Figure 5-8. Intel® 631xESB/632xESB I/O Controller Hub – 82563EB/82564EB Kumeran Connection



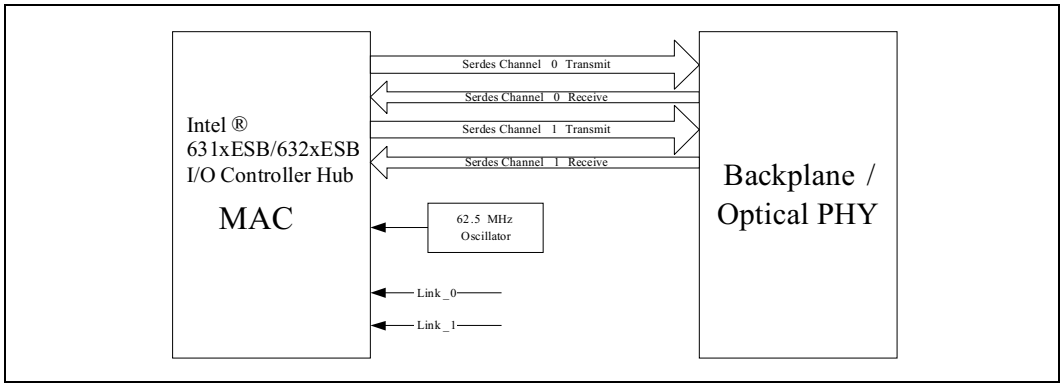
The signal that is optionally connected is:

- SER_CLK_IN. This 62.5 MHz/25 MHz clock is supplied by the 82563 EB/82564 EB (PHY) to the Kumeran block of the Intel® 631xESB/632xESB I/O Controller Hub. Intel® 631xESB/632xESB I/O Controller Hub can also use a local 62.5 MHz// 25 MHz Clock oscillator instead of the clock signal from the 82563EB/82564EB.

5.4.10.2 Intel® 631xESB/632xESB I/O Controller Hub – SerDes Backplane Connection

This mode implements 802.3 z protocol, including auto-negotiation. In this mode, the Intel® 631xESB/632xESB I/O Controller Hub LAN controller is directly connected to the network without the need of an external PHY.

Figure 5-9. SerDes Backplane Connection



Intel® 631xESB/632xESB I/O Controller Hub has SerDes port that conforms with PICMG3.1 standard and is used for connecting the Intel® 631xESB/632xESB I/O Controller Hub LAN to copper backplanes in blade servers.

This SerDes port can also work with Fiber 1G transceiver. LINK_0 and LINK_1 pins are used as SIG_DET (signal detect) signals.

The characteristics of SIG_DET signal are described in IEEE 802.3 standard, clause 38.2.

When high, SIG_DET indicates that a signal is detected; when low, it indicates that no signal is detected.

For non-optical connection in backplane applications, SIG_DET signals will be shortened to '1' (3.3V).

5.4.11 LAN Disabling

The LAN0_DIS# and LAN1_DIS# pins are used as strapping pins to disable or enable each LAN function. This allows changing dynamically the LAN status at boot time, in order to either enabling or disabling it, upon user or system aESInistrator request.

When a port is disabled, its PCI Express register set disappear and the MAC is not functional and can not receive and transmit packets. The status of the pin is sampled at PCI Express reset time.

The flow to disable or enable a port is described below:

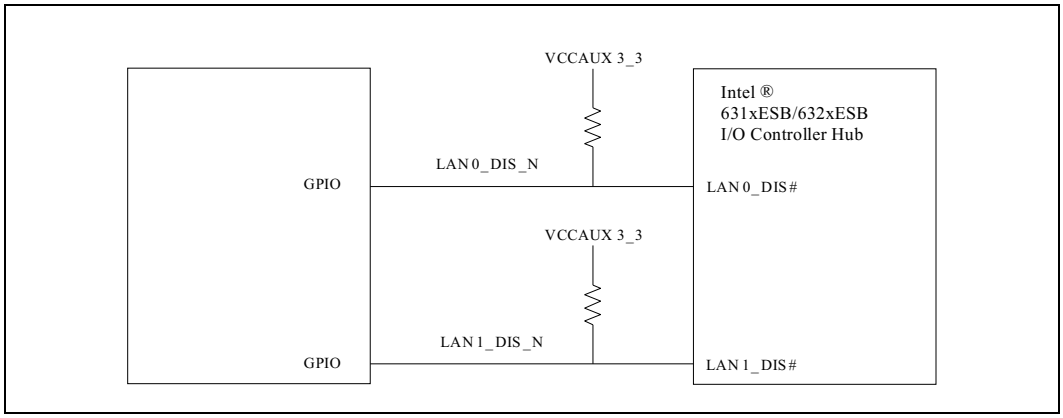
1. Assume that following power up sequence LANx_DIS# signals are driven hi (by internal or external pullup)
2. The PCI Express is established following the PERST# de-assertion
3. BIOS recognize that a LAN function in Intel® 631xESB/632xESB I/O Controller Hub should be disabled
4. The BIOS drive the LANx_DIS# signal to the low level.
5. The BIOS issue an In-Band Reset (warm reset) to Intel® 631xESB/632xESB I/O Controller Hub on the PCI Express
6. As a result, Intel® 631xESB/632xESB I/O Controller Hub samples the LANx_DIS# signals and disables the LAN function
7. BIOS may start with the Device enumeration procedure (the disabled LAN function is invisible)
8. Proceed with Nominal operation

Re-enable could be done by driving high the LANx_DIS_N signal, issue an In-Band PCI Express Reset and then request the user to issue a warm boot that generate bus enumeration.

5.4.11.1 Board Connection Requirements

The following figure shows the external board connection to control the port enabling / disabling.

Figure 5-10. LAN Port Disable



If this feature is to be implemented in a specific board the following changes should be made:

1. The LANx_DIS# signal should be connected to BIOS controlled GPIOs
2. These GPIOs should be either input, pull up, or active high by default (at reset) to avoid disabling the LAN for the management. They should be unchanged by reset (“sticky”).
3. The LAN0_DIS# and LAN1_DIS# pins may have internal pull-ups that are driven by Aux power, so the driving GPIOs should be either powered by AUX power or capable to withstand the power driven by the internal pull up even when not powered. Alternatively, the GPIOs can be isolated from Intel® 631xESB/632xESB I/O Controller Hub using a pass-gate enabled by core power.

In any configuration, both LAN0_DIS# and LAN1_DIS# pins should have an external pull-up that is connected to Vaux to avoid disabling of the LAN if the internal pull-up is released.

5.5 Board Management Controller (BMC)

5.5.1 Management Microcontroller System Theory of Operation

The Intel® 631xESB/632xESB I/O Controller Hub implements an ARC4 microcontroller and its memory subsystem for all manageability operations. The MMS (Management Microcontroller System) includes interfaces to most modules and main nodes in the Intel® 631xESB/632xESB I/O Controller Hub LAN. The Intel® 631xESB/632xESB I/O Controller Hub MMS (Management Microcontroller System) is operated by firmware (embedded software) and is a flexible infrastructure for server management implementation. This firmware can be loaded from external memory as the parallel FLASH.

The Intel® 631xESB/632xESB2 I/O Controller Hub has two BMC support options. External BMC's are supported in what is referred to as "Pass-Thru" mode. Pass-Thru configuration is beyond the scope of this document. Please refer to 82571/82572/ESB2 LAN System Manageability Application Note (AP-497). The second option is to use the BMC that is integrated into the Intel® 631xESB/632xESB I/O Controller Hub. The resident BMC requires optional firmware to function. Please contact your Intel support representative to determine what SKU supports this feature.

A basic firmware is pre-programmed in the MMS (Management Microcontroller System) ROM, which can be configured by the EEPROM/Strapping options for one of the following modes:

1. Load firmware from external memory, either by serial or parallel flash.(Can be implemented as IPMI BMC or another server management implementation)
2. TCO port / Pass Through mode – in this mode the Intel® 631xESB/632xESB I/O Controller Hub is used as a pipe between the external management controller (that is, Pass Through Mode. an external BMC) and Ethernet networking hardware. For more details on this mode of operation please refer to the 82571/82572/ESB2 LAN System Manageability Application Note (AP-497).

5.5.2 Feature List

The features of the Intel® 631xESB/632xESB I/O Controller Hub's internal BMC include:

- ARC4 processor working at 62.5 MHz speed
- 16Kbyte I-Cache and 16Kbyte D-Cache support for expansion bus accesses
- 256 Kbytes of internal SRAM with dual port (one for code accesses and one for all other accesses) – zero wait states.
- 192 Kbytes ROM including, pass through, ASF, IDE redirection and COM redirection code – zero wait states.
- Interface to both LAN ports of Intel® 631xESB/632xESB I/O Controller Hub allowing direct connection to the net and access to all LAN registers.
- An expansion bus, allowing connection to:
  - External Flash PROM. Up to 16 Mbytes as code memory over the Expansion Bus.

  - External SRAM up to 32 Mbytes over the Expansion Bus.
  - External SDRAM 16Mbyte or 32 Mbytes (256 Mbits) over the Expansion Bus.
- Support for PLD in expansion bus that implements a Flash I/F.
- Cryptographic module, supporting AES and RC4 encryption algorithms and SHA1 and MD5 authentication algorithms.
- 3 KCS functions, two of can be controlled by the BIOS, and residing on LPC bus, the 3rd implemented over PCI Express function (KCS is an interface between host software and BMC for more details see the IPMI specification).
- BT (Block transfer) function over PCI Express (BT is an interface between software and BMC in IPMI specification, see the IPMI specification).
- IDE function over PCI Express for IDE redirection.
- USB Rev1.1 function over PCI Express for USB re-direction implementing UHCI interface.
- RS232 UART
- Eight General Propose input/output pins (GPIO).
- Fan controller pins (tradeoff with GPIO) support for Fan control and tachometer.
- Host memory DMA access – can be used for IDE redirection, USB redirection or any other purpose.
- Three SMBus and two FML/SMBus ports.
- Connection of the COM redirection to LPC also
- ARC debugging interface by way of JTAG.
- Flexible filters for LAN. 8 VLAN filters.
- SOL function either trough PCI_E or LPC (mutually exclusive).
- Generation of NMI/SMI by way of SERIRQ.
- Timers for periodic interrupts, real time clock and watchdog mechanisms
- IPMI/KCS interface (SMS)
- KTFC redirect
- Full BMC implementation, meaning a standalone microcontroller with independent I/Os and memory (detail descriptions in Section 5.5)
- Secured mechanism for loadable Regulated FW
- 3 KCS ports, one in PCI space, 2 in LPC bus
- KT function made accessible from LPC bus
- USB redirection module, implemented with UHCI standard, residing on PCI Express as device 5
- BT module, residing on PCI Express as device 7

5.5.3 Memory Sub-System

Intel® 631xESB/632xESB I/O Controller Hub MMS memory subsystem includes a large internal Code / Data RAM in addition to Code ROM. The memory system includes the following components:

- Internal ROM – 192 Kbytes
- Internal SRAM – 256 Kbytes

- External Parallel flash – up to 16 Mbytes.
- External RAM – either SRAM or SDRAM – up to 32 Mbytes.

The internal SRAM is mapped to the code address space and to the data address space, which gives full flexibility in using it. The FW can access the Code area (ROM and RAM) by using ARC load/store commands.

The internal RAM is used also as buffer for receiving packets from the Rx/Tx filter and for transmitting packets, SMB data buffer and more.

The Intel® 631xESB/632xESB I/O Controller Hub BMC SDRAM controller only supports 16 or 32 bytes, 125MHz SDRAM, we don't support 8M bytes or less SDRAM device. For example:

Density	Micron Part Number
16M bytes	MT48LC8M16A2
32M bytes	MT48LC16M16A2

The external parallel flash and external RAM can be accessed either by fetch (code) or load/store (data) accesses. These accesses are cached by an I-cache and a D-Cache.

Table 5-20 describes the mapping of the different components in the memory sub-system

Table 5-20. ARC Memory System Table in Intel® 631xESB/632xESB I/O Controller Hub MMS

	Width	Size in Kbytes	Address space	Comments
Internal ROM	32 bit	192K	0x0000000 – 0x002FFFF	0WS
Internal RAM	128 bit	256K	0x0080000 – 0x00BFFFF	0WS
PLD	16 bit	128 Bytes	0x00C00000 – 0x00C0007F	External PLD access
External parallel flash	16 bit	Up to 16M	0x1000000 – 0x1FFFFFF	Programmable WS. Cached accesses.
External RAM	16 bit	Up to 32M	x2000000 – 0x3FFFFFF	Cached accesses.

5.5.4 Instruction Cache and Data Cache

The I-cache is needed due to slow access time of p-flash and external RAM, to optimize code fetch from p-flash. The instruction cache (I-Cache) size is 16 Kbytes and works with external instruction memory. To work with external SDRAM data memory Intel® 631xESB/632xESB I/O Controller Hub MMS (Management Microcontroller System) includes a data cache (D-Cache).

5.5.5 External Interfaces

5.5.5.1 PCI Express* Functions

The Intel® 631xESB/632xESB I/O Controller Hub MMS (Management Microcontroller System) implements the following PCI Express functions over the PCI Express bus:

- Function 4 – SMS function. This function is used for the implementation of the System Management Software Interface of the IPMI specification. This function can implement KCS interface (see the IPMI specification).
- Function 3 – KT interface function. This function is used to implement the COM port interface for the keyboard and text redirect/serial over LAN (see Serial Over LAN white paper).
- Function 2 – IDE function. This function is used to implement the IDE interface for the Floppy/Disk redirection.
- Function 5 – The USB 1.1 function for USB redirection implementing UHCI.
- Function 7 – BT function. This function is used for the implementation of the System Management Software Interface of the IPMI specification. This function can implement BT interface (see the IPMI specification).

5.5.5.1.1 PCI Express* Function 2 – IDE Interface

To control remotely the machine it is useful to redirect the machine's IDE controller to a remote control machine that has IDE CD-ROM device and IDE floppy device attached (usually attached to the management terminal window on a remote control station) or to have on the management console files that have a full copy of a CD-ROM or a Floppy (ISO files). Using such a feature will enable control of such a machine through the network without the need to physically be near that machine.

Intel® 631xESB/632xESB I/O Controller Hub MMS (Management Microcontroller System) includes a standard native PCI IDE function with a single IDE cable with CD-ROM and Floppy devices attached to it. The devices will be emulated by software on the management console. To achieve this functionality, Intel® 631xESB/632xESB I/O Controller Hub MMS Hardware contains an IDE port functionality, while the Firmware should implement autonomously a minimal subset of the ATA commands. The complementary set of ATA and ATAPI commands are redirected to the management console which interpret them by a dedicated SW. The management console SW will access locally either files that contain Floppy or CD images, or real Floppy and CD devices to service the MMS initiated requests.

ATA/ATAPI Command Block Registers

Intel® 631xESB/632xESB I/O Controller Hub MMS (Management Microcontroller System) emulates two removable media devices: LS120 Floppy and CD-ROM drives. These two devices comply to the ATAPI specification. Such devices must response to some basic ATA commands as well as ATAPI specific commands. ATA and ATAPI devices are supported by a set of registers which have a meaning that is command dependant (ATA or ATAPI). Hence the IDE set of registers is interpreted as ATA or ATAPI registers – depends on the command issued.

Software Usage

There are several stages in the lifetime of the PC where interactive local control is needed. These stages will be identified and remote control support will be considered.

BIOS and EFI Usage at Boot Time

At boot time, IA-32 PC compatible machines run their BIOS firmware. EFI behaves similarly; that SW performs plug and play on existing PCI devices and allocates resources. OS boot is done on existing attached bootable devices. One of them is IDE CD, or IDE Floppy (LS120).

BIOS and EFI can boot off this IDE controller like it has CD and Floppy drives attached locally. The BIOS or EFI has to support a native PCI IDE controller (that use plug and play I/O addresses and interrupts rather than legacy I/O addresses and legacy interrupts). The BIOS and EFI need also to support the IDE Floppy device (LS120 compatible).

Windows*, Linux*, and CD Install Usage

All type of OS and SW can access the Intel® 631xESB/632xESB I/O Controller Hub MMS (Management Microcontroller System) IDE function and find there a remote CD-ROM or floppy, depends on the attached device at the remote console. Intel® 631xESB/632xESB I/O Controller Hub MMS FW could encapsulate the written IDE commands and send them over to the management console. Results will return in a similar way.

For more details of the IDE function implementation please refer to the Intel® 631xESB/632xESB I/O Controller Hub Software Design Guidelines.

5.5.5.1.2 PCI Express* Function 3 – KT (Keyboard/Text) Interface

Intel® 631xESB/632xESB I/O Controller Hub MMS (Management Microcontroller System) exposes a standard COM port that can be used by the host software (BIOS, EFI, OS) to redirect its text output or keyboard input through it. To control remotely the managed machine Intel® 631xESB/632xESB I/O Controller Hub MMS supports redirect of the on-screen text and keyboard to a remote control screen (usually a terminal window on a remote control station). The Keyboard and Text redirection enables the control of such a machine through the network without the need to be physically near that machine.

COM Port Registers

Intel® 631xESB/632xESB I/O Controller Hub MMS (Management Microcontroller System) implements a set of registers which are mapped into I/O space and to memory space. This set of registers are similar/compatible to those of the 16550 device. Dual mapping is needed for two different applications. Typically in IA-32 machines, BIOS and OS drivers access the COM ports using I/O mapped registers. In the Itanium processor family, system firmware typically accesses devices through memory access. The two methods access the same registers on the device. There are 8 registers implemented in the device. The I/O BAR reflects this size exactly, while the memory BAR cannot expose fewer than 16 registers by PCI definition. PCI specification encourages implementations to expose not fewer than 4k registers through memory BARs. MMS decodes 4-Kbyte space, while the first 8 bytes are mapped to the those registers and the rest are hard coded in “read” to a value of 0.

BIOS Text and Keyboard at Boot Time

At boot time, IA-32 PC compatible machines run their BIOS code. The BIOS writes its messages and draws its menus on the attached VGA screen in text mode. User is prompted to intervene in the flow of the boot process through the keyboard. There are some BIOS that already support screen text and keyboard redirection to one of the machine’s COM ports. Other BIOS do not have such a capability. In order to support screen text redirection to another output device, the BIOS has to be changed and provide SW access to the screen written data. Well behaved SW, including BIOS and DOS write to the screen through a standard INT10 API. By intercepting INT10 calls, the BIOS can copy the calling parameters and interpret the write data commands by sending them over the COM port. MMS (Management Microcontroller System) can redirect the data from the COM port to the management console by way of the LAN.

There are utilities (such as SCSI cards' BIOS boot ROMs) which write directly to the screen memory buffer. These writes can not be intercepted as described above. A more general method that can cover direct access to the screen memory is a code that is chained to the BIOS timer interrupt and every timer tick reads the screen text buffer and looks for new updates in it.

Keyboard input for the BIOS User Interface can be read from the COM port and be placed in the keyboard input buffer. BIOS software can either poll the COM port triggered by timer interrupt or by COM port interrupt (generated by the chip upon receive data available in the COM port buffer.

EFI Text and Keyboard at Boot Time

EFI is designed to support text and keyboard redirection over COM port. No specific additions are needed in EFI to be supported.

Linux Text and Keyboard at OS Start and While OS is Running

Linux is natively equipped with text and keyboard redirection to COM port. No special software is needed in order to redirect if we implement COM port function.

Windows Text and Keyboard While OS is Running

Windows.NET has a new EMS (Emergency Management Services) facility. This specification allows text messages and keyboard control to be sent through a standard COM port as out of band control. OS boot options selection, OS Upgrade, OS installation, networking setup, applications setup and control and blue screen messages are routed to the selected COM port interface. For more details, see http://www.microsoft.com/hwdev/platform/server/headless.

5.5.5.1.3 PCI Express* Function 4 – System Management Software (SMS) Interface

The SMS interface implements the IPMI KCS interface. This interface is connected to the system manageability SW through PCI Express Function 4. For each KCS cluster, there are four 8-bit registers that are used for communication between software and Intel® 631xESB/632xESB I/O Controller Hub MMS (Management Microcontroller System).

Control register.

1. Status register – Read only by the device driver.
2. Data in – Read only by firmware.
3. Data Out – Read only by the device driver.

The SMS block will generate an interrupt to the ARC (upon configuration) whenever the control register is being written by the device driver. Intel® 631xESB/632xESB I/O Controller Hub MMS can work with the device driver on an interrupt or polling basis.

5.5.5.1.4 PCI Express* Function 5 – UHCI Interface

UHCI is a standard interface used to interface between a USB driver and the USB 1.1 controller. In Intel® 631xESB/632xESB I/O Controller Hub/BMC, it is used to emulate a USB controller and provide USB redirection capabilities.The implementation of the UHCI functionality, other than the register set and interrupts generation, is the responsibility of the FW.

5.5.5.1.5 PCI Express* Function 7 - BT Interface

The BT Interface is so named because an entire block of message data is buffered before the management controller is notified of available data. This is different from the SMIC and KCS interfaces, which are byte-transfer oriented. A BT Interface Capabilities command provides supplementary information about extended buffer sizes and other elements of the interface.

5.5.5.2 SMBus and Fast Management Link Bus Interfaces

In Intel® 631xESB/632xESB I/O Controller Hub BMC there are 5 SMB interfaces. SMB Interfaces are Master/Slave interface. Two interfaces can be used as either Fast Management Link (FML) interfaces or as standard SMBus and the rest are conventional SMBus. Though the register sets are identical, only SMB0 and SMB1 may be used as FML.

Table 5-21. Intel® 631xESB/632xESB I/O Controller Hub BMC SMBus Interface Usage Summary

Interface	Usage	Master/Slave	Ports Pads
SMB0	SMBus or FML	Master/Slave	SMBD0 SMBCLK0 FLBSD0 FLBSINTEX0
SMB1	SMBus	Master/Slave	SMBD1 SMBCLK1 FLBSD1 FLBSINTEX1
SMB2	SMBus	Master/Slave	SMBD2 SMBCLK2 SMBALRT_2
SMB3	SMBus	Master/Slave	SMBD3 SMBCLK3 SMBALRT_3
SMB4	SMBus	Master/Slave	SMBD4 SMBCLK4 SMBALRT_4

Notes:
1. Port number 0 and number 1 can be either FML or SMBus ports.
2. Slave and Master interfaces are independent one each other to allow the Slave and the Master working together. In order to enhance the performance, DMAs were added to the Master machine.
3. Intel recommends using SMBus 3 for passing traffic between the TCO port and an external BMC.

5.5.5.2.1 FML Description

Overview

The Fast Management Link Bus (FML) is a point-to-point wire interface. The FML Bus is based on the principles of the SMBus and can work up to 8Mhz.

The FML is a single Master and single Slave bus.

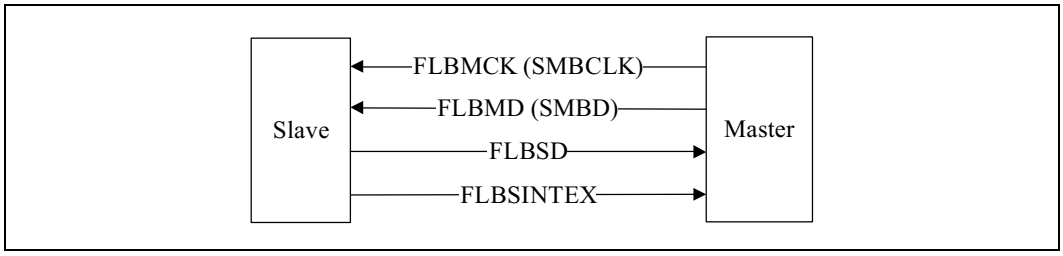
General Characteristics

The FML Bus is point-to-point wire interface. The main differences between the SMBus and the FML is that the FML is point-to-point (one Master, one Slave) and it is not an open-drain bus. Each wire in the interface is driven by a single source (Master or Slave).

In the FML there is only one Master and one Slave. These two devices cannot change their role: One of them is always the Master while the other is always the Slave.

The following figure shows how the FML is connected between the two devices and the relevant SMBus pad used.

Figure 5-11. FML Topology



The FLBMCK is the clock of the BUS, which is always driven by the Master. The FLBMD is the data line driven by the Master while FLBSD is the data line driven by the Slave. Both Slave and Master data lines are not changed while the FLBMCK is high (unless it is a start or stop condition).

The FLBSINTEX that is driven by the Slave device is used for two purposes:

1. Alert the Master device to read from Slave. When the interrupt is asserted, it will be asserted until the next start.
2. Clock extension – when set zero it indicates the Master to extend its current clock state (if the Master clock is high it should remain high until the FLBSINTEX is high again). This is way the Slave can hold the transaction when it is not ready yet.

The FLBSINTEX functions as an alert signal while the bus is idle (between stop to start) and it functions as an extension indication from the Slave device during the transaction itself.

The behavior of the bus and the transactions on the bus are the same as in SMBus (Start, Stop, repeated start, and so forth).

5.5.5.3 General Purpose I/O Pins

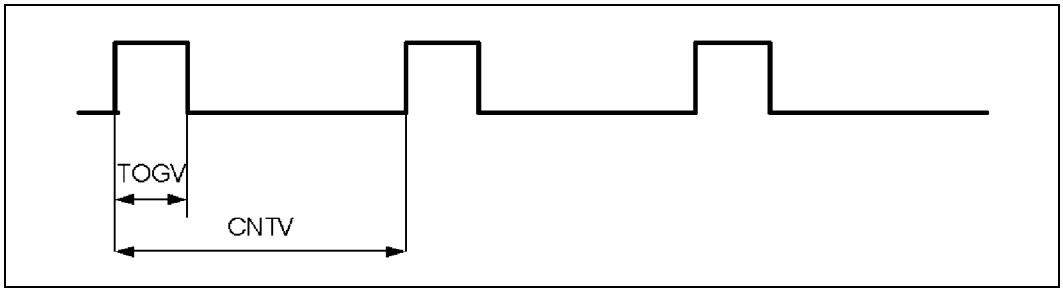
The BMC has an 8 bit GPIO port. The GPIO can be used in the following modes:

- Output
- Input
- Output PWM
- Input FAN Tachometer mode

5.5.5.3.1 PWM Mode

PWM mode is used to control devices on the board according to the duty cycle of pin as an output.

Figure 5-12. PWM Mode Duty Cycle



In Figure 5-12, the two periods TOGV and CNTV are fields of GPIO control register. In PWM mode the 8-bit counter starts counting from 0 until CNTV.

- In value 0 the pin is set.
- In value TOGV the pin is reset
- In value CNTV the counter is reset.
- The polarity is controlled by a different field.
- Any write to the control register will restart the counter.

5.5.5.3.2 Fan Tachometer Mode

The Fan Tachometer mode is used to sense the states of devices on the board according to time between pulses. It measures the amount of time it took for a programmable number of pulses on the input pin. In this mode the pin is an input, and two counters are used: the time counter and the pulse counter.

After setting Fan Tachometer mode by writing to the control register, the 8 bit time counter is reset, and the pulse counter is loaded with the CNTV value.

The pulse counter decrements each rising or falling edge (the polarity is programmable) of the input pin. When the counter reaches 0, it is disabled.

The time counter starts counting on the first edge of the pin and stops after the pulse counter reaches 0.

5.5.5.4 UART Interface

The UART performs serial-to-parallel conversion on data originating from modems or other serial devices, and performs parallel-to-serial conversion on data from the ARC to these devices. The UART registers are compatible with the 16550 device.

The ARC can read the complete status of the UART at any time during the functional operation. Status information reported includes the type and condition of the transfer operations being performed by the UART, as well as any error conditions (parity, overrun, framing, or break interrupt).

The ARC can program the following serial-interface characteristics:

- 5, 6, 7 or 8 bit characters
- Even, odd, or no-parity bit generation and detection
- 1, 1.5 or 2 stop bit generation
- BAUD generation

The UART includes the MODEM control functions. The UART also has a loop-back mode control for communications link fault isolation as well as break, parity, overrun, and framing error simulation.

5.5.5.5 EEPROM Write/Read Interface

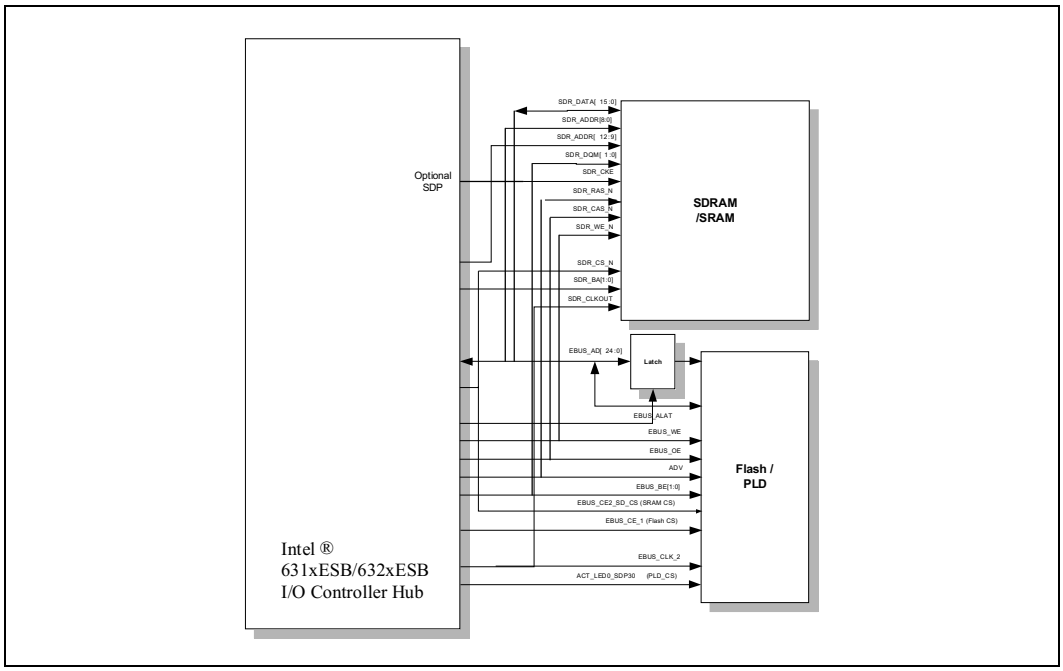
This interface is not part of Intel® 631xESB/632xESB I/O Controller Hub MMS hardware. The ARC microcontroller can use the MAC CSR interface in order to access the EPROM unit of the LAN for read/write single byte.

5.5.5.6 Expansion Bus and External Memory Devices

Intel® 631xESB/632xESB I/O Controller Hub MMS (Management Microcontroller System) provides an interface to external memory devices. This interface includes multiplexed address/data bus and the control signals that are needed to control the memory devices.

Intel® 631xESB/632xESB I/O Controller Hub MMS can handle two different types of memory. The first one is a Flash memory, which will typically be used for code. The second type will be either an SRAM or an SDRAM memory. All the signals will be common to both types of memory except the chip-enable signal and the clock signal (available only for sync memories). There are two different sets of those parameters, each associated with one CE (chip enable) signal.

Figure 5-13. Expansion Bus Signal Block Diagram



5.5.6 Memory Host DMA

The Host Interface connects Intel® 631xESB/632xESB I/O Controller Hub MMS (Management Microcontroller System) to the Host memory as a Master for read/write transactions. The read/write transactions of the MMS HOST DMA are the lowest priority between all Intel® 631xESB/632xESB I/O Controller Hub DMA channels that use this HOST arbiter. The Memory DMA could be used for IDE redirection USB redirection, or other purposes.

The HOST interface is built from two different channels:

- **Write channel** – This channel allows the MMS to write data from the internal data memory of the MMS into the HOST main memory. This channel has no restriction on the memory alignment of the location of the data in the HOST memory. Write channels request are limited to the size of 128 bytes.
- **Read channel** – This channel allows the MMS to read data from the HOST memory into the data memory of the MMS. Data should be 128 bit aligned in the BMC memory. Read request are limited to 128 bytes.

These two channels do not work simultaneously, which means that the MMS can only do a write transaction or a read transaction at any given time.

5.5.7 Cryptography Module

Intel® 631xESB/632xESB I/O Controller Hub MMS (Management Microcontroller System) provides a hardware accelerator for encryption and authentication algorithms which can be used to offload cryptographic and authentication tasks from the ARC and to improve the performance in the overall server management solution.

The cryptography module performs the following functions:

- Encryption/decryption based on RC4 and AES algorithms
- Authentication based on SHA1/MD5 algorithms.

In addition, the cryptography module includes a DMA engine, allowing transferring of data within the BMC memory space. This DMA can be used even without applying a cryptographic algorithm.

5.5.7.1 RC4* Hardware Accelerator

RC4* is a stream cipher symmetric key algorithm from RSA. RC4 uses a variable length key from 1 to 256 bytes to initialize a 256-byte state table. The state table is used for subsequent generation of pseudo-random bytes and then to generate a pseudo-random stream, which is XORed with the plaintext to give the ciphertext. Each element in the state table is swapped at least once. The implementation of the algorithm contains two init phases that will randomize an init table. During run time one of the 256 bytes will be chosen through a random method and this byte will be XORed with the incoming data, resulting in cipher text (encryption) or plain text (decryption).

5.5.7.2 AES Hardware Accelerator

This standard specifies the **Rijndael** algorithm, a symmetric block cipher that can process data blocks of 128 bits, using cipher keys with lengths of 128, 192,and 256 bits. Rijndael was designed to handle additional block sizes and key lengths. However, only 128 bits are implemented in the Intel® 631xESB/632xESB I/O Controller Hub.

AES is used as recommended by IETF documents, in ESP (CBC mode).

5.5.7.3 HMAC-SHA1/MD5 Hardware Accelerator

HMAC consists of a mechanism for message authentication using cryptographic hash functions.HMAC can be used with any iterative cryptographic hash function, for example, MD5 or SHA-1, in combination with a secret shared key.

The SHA1 algorithm specifies a Secure Hash Algorithm, for computing a condensed representation of a message or a data file. When a message of any length < 2^{64} bits is input, the SHA-1 produces a 160-bit output called a message digest. The message digest can then, for example, be input to a signature algorithm, which generates or verifies the signature for the message.

The MD5 algorithm takes as input a message of arbitrary length and produces as output a 128-bit "fingerprint" or "message digest" of the input. It is conjectured that it is computationally infeasible to produce two messages having the same message digest, or to produce any message having a given pre-specified target message digest.

5.6 LPC Bridge (with System and Management Functions) (D31:F0)

The LPC bridge function of the Intel® 631xESB/632xESB I/O Controller Hub resides in PCI Device 31:Function 0. In addition to the LPC bridge function, D31:F0 contains other functional units including DMA, Interrupt controllers, Timers, Power Management, System Management, GPIO, and RTC. In this chapter, registers and functions associated with other functional units (power management, GPIO, USB, IDE, and so forth) are described in their respective sections.

5.6.1 LPC Interface

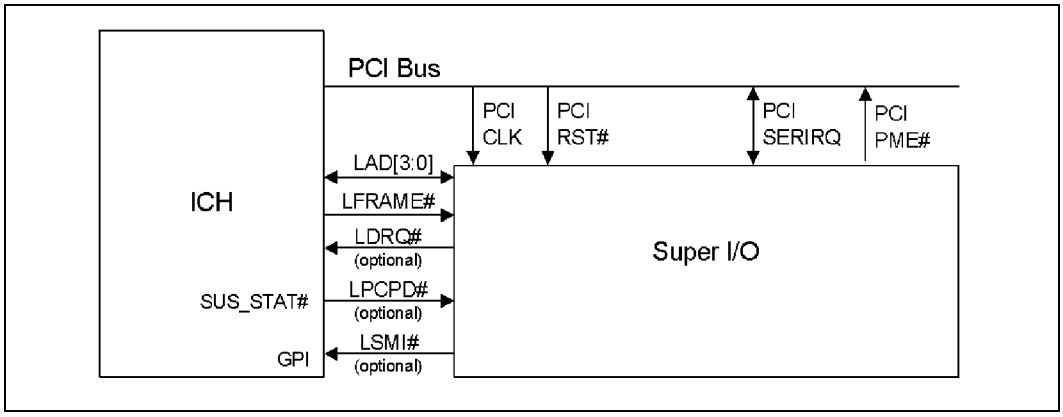
The Intel® 631xESB/632xESB I/O Controller Hub implements an LPC interface as described in the *Low Pin Count Interface Specification, Revision 1.1*. The LPC interface to the Intel® 631xESB/632xESB I/O Controller Hub is shown in Figure 5-14. The LPC Controller implements all of the signals that are shown as optional, but peripherals are not required to do so.

For Intel® 631xESB/632xESB I/O Controller Hub LPC controller:

- SLSMI# can be connected to any of the SMI capable GPIO signals.
- The Super I/O's PME# can be connected to the PCI PME# signal; however, this may cause software problems. A better choice is to connect it to one of the LPC Controller's SCI capable GPIO signals.
- The LPC Controller's SUS_STAT# signal is connected directly to the LPCPD# signal.

All the other signals have the same name on the LPC Controller and on the LPC I/F.

Figure 5-14. LPC Interface Diagram



5.6.1.1 LPC Cycle Types

The Intel® 631xESB/632xESB I/O Controller Hub implements all of the cycle types described in the *Low Pin Count Interface Specification, Revision 1.0*. Table 5-22 shows the cycle types supported by the Intel® 631xESB/632xESB I/O Controller Hub.

Table 5-22. LPC Cycle Types Supported

Cycle Type	Comment
Memory Read	Single: 1 byte only
Memory Write	Single: 1 byte only
I/O Read	1 byte only. Intel® 631xESB/632xESB I/O Controller Hub breaks up 16- and 32-bit processor cycles into multiple 8-bit transfers. See Note 1 below.
I/O Write	1 byte only. Intel® 631xESB/632xESB I/O Controller Hub breaks up 16- and 32-bit processor cycles into multiple 8-bit transfers. See Note 1 below.
DMA Read	Can be 1, or 2 bytes
DMA Write	Can be 1, or 2 bytes
Bus Master Read	Can be 1, 2, or 4 bytes. (See Note 2 below)
Bus Master Write	Can be 1, 2, or 4 bytes. (See Note 2 below)

Notes:
1. For memory cycles below 16 MB that do not target enabled firmware hub ranges, the Intel® 631xESB/632xESB I/O Controller Hub performs standard LPC memory cycles. It attempts only 8-bit transfers. If the cycle appears on PCI as a 16-bit transfer, it appears as two consecutive 8-bit transfers on LPC. Likewise, if the cycle appears as a 32-bit transfer on PCI, it appears as four consecutive 8-bit transfers on LPC. If the cycle is not claimed by any peripheral, it is subsequently aborted, and the Intel® 631xESB/632xESB I/O Controller Hub returns a value of all 1s to the processor. This is done to maintain compatibility with ISA memory cycles where pull-up resistors would keep the bus high if no device responds.
2. Bus Master Read or Write cycles must be naturally aligned. For example, a 1-byte transfer can be to any address. However, the 2-byte transfer must be word aligned (that is, with an address where A0=0). A DWord transfer must be DWord aligned (that is, with an address where A1 and A0 are both 0).

5.6.1.2 Start Field Definition

Table 5-23. Start Field Bit Definitions

Bits[3:0] Encoding	Definition
0000	Start of cycle for a generic target
0010	Grant for Bus Master 0
0011	Grant for Bus Master 1
1111	Stop/Abort: End of a cycle for a target.

Note: All other encodings are RESERVED.

5.6.1.3 Cycle Type / Direction (CYCTYPE + DIR)

The Intel® 631xESB/632xESB I/O Controller Hub always drives bit 0 of this field to 0. Peripherals running Bus Master cycles must also drive bit 0 to 0. Table 5-24 shows the valid bit encodings.

Table 5-24. Cycle Type Bit Definitions

Bits[3:2]	Bit1	Definition
00	0	I/O Read
00	1	I/O Write
01	0	Memory Read
01	1	Memory Write
10	0	DMA Read
10	1	DMA Write
11	x	Reserved. If a peripheral performing a Bus Master cycle generates this value, the Intel® 631xESB/632xESB I/O Controller Hub aborts the cycle.

5.6.1.4 SIZE

Bits[3:2] are reserved. The Intel® 631xESB/632xESB I/O Controller Hub always drives them to 00. Peripherals running Bus Master cycles are also supposed to drive 00 for bits 3:2; however, the Intel® 631xESB/632xESB I/O Controller Hub ignores those bits. Bits[1:0] are encoded as listed in Table 5-25.

Table 5-25. Transfer Size Bit Definition

Bits[1:0]	Size
00	8-bit transfer (1 byte)
01	16-bit transfer (2 bytes)
10	Reserved. The Intel® 631xESB/632xESB I/O Controller Hub never drives this combination. If a peripheral running a Bus Master cycle drives this combination, the Intel® 631xESB/ 632xESB I/O Controller Hub may abort the transfer.
11	32-bit transfer (4 bytes)

5.6.1.5 SYNC

Valid values for the SYNC field are shown in Table 5-26.

Table 5-26. SYNC Bit Definition

Bits[3:0]	Indication
0000	**Ready:** SYNC achieved with no error. For DMA transfers, this also indicates DMA request deassertion and no more transfers desired for that channel.
0101	**Short Wait:** Part indicating wait-states. For Bus Master cycles, the Intel® 631xESB/ 632xESB I/O Controller Hub does not use this encoding. Instead, the Intel® 631xESB/ 632xESB I/O Controller Hub uses the Long Wait encoding (see next encoding below).
0110	**Long Wait:** Part indicating wait-states, and many wait-states will be added. This encoding driven by the Intel® 631xESB/632xESB I/O Controller Hub for Bus Master cycles, rather than the Short Wait (0101).
1001	**Ready More (Used only by peripheral for DMA cycle):** SYNC achieved with no error and more DMA transfers desired to continue after this transfer. This value is valid on only DMA transfers and is not allowed for any other type of cycle.
1010	**Error:** Sync achieved with error. This is generally used to replace the SERR# or IOCHK# signal on the PCI/ISA bus. It indicates that the data is to be transferred, but there is a serious error in this transfer. For DMA transfers, this not only indicates an error, but also indicates DMA request deassertion and no more transfers desired for that channel.

Note: All other combinations are RESERVED.

5.6.1.6 SYNC Time-Out

There are several error cases that can occur on the LPC interface. The Intel® 631xESB/632xESB I/O Controller Hub responds as defined in section 4.2.1.9 of the *Low Pin Count Interface Specification, Revision 1.1* to the stimuli described therein. There may be other peripheral failure conditions; however, these are not handled by the Intel® 631xESB/632xESB I/O Controller Hub.

5.6.1.7 SYNC Error Indication

The Intel® 631xESB/632xESB I/O Controller Hub responds as defined in section 4.2.1.10 of the *Low Pin Count Interface Specification, Revision 1.1*.

Upon recognizing the SYNC field indicating an error, the Intel® 631xESB/632xESB I/O Controller Hub treats this as SERR by reporting this into the Device 31 Error Reporting Logic.

5.6.1.8 LFRAME# Usage

The Intel® 631xESB/632xESB I/O Controller Hub follows the usage of LFRAME# as defined in the *Low Pin Count Interface Specification*, *Revision 1.1*.

The Intel® 631xESB/632xESB I/O Controller Hub performs an abort for the following cases (possible failure cases):

- Intel® 631xESB/632xESB I/O Controller Hub starts a Memory, I/O, or DMA cycle, but no device drives a valid SYNC after four consecutive clocks.
- Intel® 631xESB/632xESB I/O Controller Hub starts a Memory, I/O, or DMA cycle, and the peripheral drives an invalid SYNC pattern.
- A peripheral drives an illegal address when performing Bus Master cycles.
- A peripheral drives an invalid value.

5.6.1.9 I/O Cycles

For I/O cycles targeting registers specified in the Intel® 631xESB/632xESB I/O Controller Hub's decode ranges, the Intel® 631xESB/632xESB I/O Controller Hub performs I/O cycles as defined in the *Low Pin Count Interface Specification, Revision 1.1*. These are 8-bit transfers. If the processor attempts a 16-bit or 32-bit transfer, the Intel® 631xESB/632xESB I/O Controller Hub breaks the cycle up into multiple 8-bit transfers to consecutive I/O addresses.

Note: If the cycle is not claimed by any peripheral (and subsequently aborted), the Intel® 631xESB/632xESB I/O Controller Hub returns a value of all 1s (FFh) to the processor. This is to maintain compatibility with ISA I/O cycles where pull-up resistors would keep the bus high if no device responds.

5.6.1.10 Bus Master Cycles

The Intel® 631xESB/632xESB I/O Controller Hub supports Bus Master cycles and requests (using LDRQ#) as defined in the *Low Pin Count Interface Specification, Revision 1.1*. The Intel® 631xESB/632xESB I/O Controller Hub has two LDRQ# inputs, and thus supports two separate Bus Master devices. It uses the associated START fields for Bus Master 0 (0010b) or Bus Master 1 (0011b).

Note: The Intel® 631xESB/632xESB I/O Controller Hub does not support LPC Bus Masters performing I/O cycles. LPC Bus Masters should only perform memory read or memory write cycles.

5.6.1.11 LPC Power Management

LPCPD# Protocol

Same timings as for SUS_STAT#. Upon driving SUS_STAT# low, LPC peripherals drive LDRQ# low or tri-state it. Intel® 631xESB/632xESB I/O Controller Hub shuts off the LDRQ# input buffers. After driving SUS_STAT# active, the Intel® 631xESB/632xESB I/O Controller Hub drives LFRAME# low, and tri-states (or drive low) LAD[3:0].

Note: The *Low Pin Count Interface Specification, Revision 1.1* defines the LPCPD# protocol where there is at least 30 µs from LPCPD# assertion to LRST# assertion. This specification explicitly states that this protocol applies only to entry/exit of low power states which does not include asynchronous reset events. The Intel® 631xESB/632xESB I/O Controller Hub asserts both SUS_STAT# (connects to LPCPD#) and PCIRST# (connects to LRST#) at the same time when the core logic is reset (by way of CF9h, PWROK, or SYS_RESET#, and so forth). This is not inconsistent with the LPC LPCPD# protocol.

5.6.1.12 Configuration and Intel® 631xESB/632xESB I/O Controller Hub Implications

LPC I/F Decoders

To allow I/O cycles and memory mapped cycles to go to the LPC interface, the Intel® 631xESB/632xESB I/O Controller Hub has several decoders. During configuration, the Intel® 631xESB/632xESB I/O Controller Hub must be programmed with the same decode ranges as the peripheral. The decoders are programmed by way of the Device 31:Function 0 configuration space.

Note: The Intel® 631xESB/632xESB I/O Controller Hub cannot accept PCI write cycles from PCI-to-PCI bridges or devices with similar characteristics (specifically those with a “Retry Read” feature which is enabled) to an LPC device if there is an outstanding LPC read cycle towards the same PCI device or bridge. These cycles are not part of normal system operation, but may be encountered as part of platform validation testing using custom test fixtures.

Bus Master Device Mapping and START Fields

Bus Masters must have a unique START field. In the case of the Intel® 631xESB/632xESB I/O Controller Hub that supports two LPC Bus Masters, it drives 0010 for the START field for grants to Bus Master #0 (requested by way of LDRQ0#) and 0011 for grants to Bus Master #1 (requested by way of LDRQ1#.). Thus, no registers are needed to configure the START fields for a particular Bus Master.

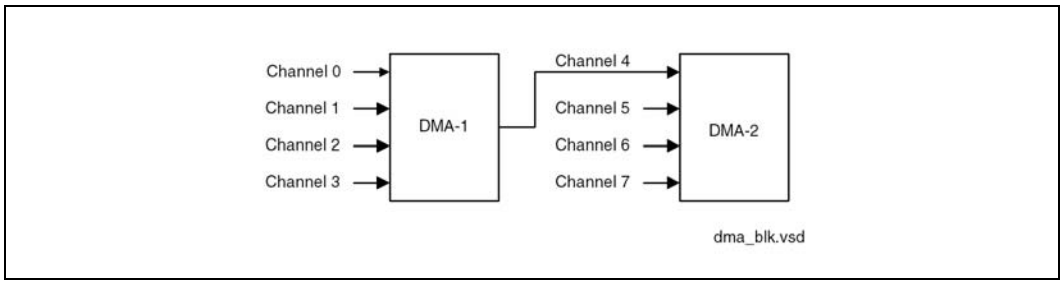
5.7 DMA Operation (D31:F0)

The Intel® 631xESB/632xESB I/O Controller Hub supports LPC DMA using a DMA controller. The DMA controller has registers that are fixed in the lower 64 KB of I/O space. The DMA controller is configured using registers in the PCI configuration space. These registers allow configuration of the channels for use by LPC DMA.

The DMA circuitry incorporates the functionality of two 82C37 DMA controllers with seven independently programmable channels (Figure 5-15). DMA controller 1 (DMA-1) corresponds to DMA channels 0–3 and DMA controller 2 (DMA-2) corresponds to channels 5–7. DMA channel 4 is used to cascade the two controllers and defaults to cascade mode in the DMA Channel Mode (DCM) Register. Channel 4 is not available for

any other purpose. In addition to accepting requests from DMA Slaves, the DMA controller also responds to requests that software initiates. Software may initiate a DMA service request by setting any bit in the DMA Channel Request Register to a 1.

Figure 5-15. Intel® 631xESB/632xESB I/O Controller Hub DMA Controller



Each DMA channel is hardwired to the compatible settings for DMA device size: channels [3:0] are hardwired to 8-bit, count-by-bytes transfers, and channels [7:5] are hardwired to 16-bit, count-by-words (address shifted) transfers.

Intel® 631xESB/632xESB I/O Controller Hub provides 24-bit addressing in compliance with the ISA-Compatible specification. Each channel includes a 16-bit ISA-Compatible Current Register which holds the 16 least-significant bits of the 24-bit address, an ISA-Compatible Page Register which contains the eight next most significant bits of address.

The DMA controller also features refresh address generation, and autoinitialization following a DMA termination.

5.7.1 Channel Priority

For priority resolution, the DMA consists of two logical channel groups: channels 0–3 and channels 4–7. The mode of operation for each controller is determined by the DMA Command Register (address 08h for channels 0-3, D0h for channels 4-7). Since channels 0-3 are cascaded onto channel 4, any request seen on channel 0 - 3 appears as a request on channel 4. The DMA controller stops rotating when an NMI is pending.

In fixed mode, the lowest numbered channel in a channel group receives highest priority. Therefore, channel 0 is the highest priority device of channels 0 - 3, and channel 4 is the highest priority device of channels 4 - 7. When both channels are programmed in fixed mode, channel 0 has highest priority, and channel 7 the lowest.

In rotating mode, the lowest numbered channel starts out with highest priority. When it is serviced, the next numbered channel receives highest priority, and the previous channel receives lowest priority. For example, if channel 0 has highest priority and is requesting, it will win arbitration, then will be the lowest priority channel until channel 1, 2, and 3 have been serviced.

Due to the nature of channel 0 - 3 being cascaded onto channel 4, rotating mode adds some peculiarities to the arbitration scheme. Table 5-27 lists arbitration winners, assuming all channels were requesting.

Table 5-27. DMA Channel Priority

Current	Both Fixed	Lower Fixed, Upper Rotating	Lower Rotating, Upper Fixed	Both Rotating
0	0, 1, 2, 3, 5, 6, 7	5, 6, 7, 0, 1, 2, 3	1, 2, 3, 0, 5, 6, 7	5, 6, 7, 1, 2, 3, 0
1	0, 1, 2, 3, 5, 6, 7	5, 6, 7, 0, 1, 2, 3	2, 3, 0, 1, 5, 6, 7	5, 6, 7, 2, 3, 0, 1
2	0, 1, 2, 3, 5, 6, 7	5, 6, 7, 0, 1, 2, 3	3, 0, 1, 2, 5, 6, 7	5, 6, 7, 3, 0, 1, 2
3	0, 1, 2, 3, 5, 6, 7	5, 6, 7, 0, 1, 2, 3	0, 1, 2, 3, 5, 6, 7	5, 6, 7, 0, 1, 2, 3
5	0, 1, 2, 3, 5, 6, 7	6, 7, 0, 1, 2, 3, 5	0, 1, 2, 3, 5, 6, 7	6, 7, 0, 1, 2, 3, 5
6	0, 1, 2, 3, 5, 6, 7	7, 0, 1, 2, 3, 5, 6	0, 1, 2, 3, 5, 6, 7	7, 0, 1, 2, 3, 5, 6
7	0, 1, 2, 3, 5, 6, 7	0, 1, 2, 3, 5, 6, 7	0, 1, 2, 3, 5, 6, 7	0, 1, 2, 3, 5, 6, 7

5.7.2 Address Compatibility Mode

When the DMA is operating, the addresses do not increment or decrement through the High and Low Page Registers. Therefore, if a 24-bit address is 01FFFFh and increments, the next address is 010000h, not 020000h. Similarly, if a 24-bit address is 020000h and decrements, the next address is 02FFFFh, not 01FFFFh.

However, when the DMA is operating in 16-bit mode, the addresses still do not increment or decrement through the High and Low Page Registers but the page boundary is now 128 K. Therefore, if a 24-bit address is 01FFFEh and increments, the next address is 000000h, not 0100000h. Similarly, if a 24-bit address is 020000h and decrements, the next address is 03FFFEh, not 02FFFEh. This is compatible with the 82C37 and Page Register implementation used in the PC-AT. This mode is set after CPURST is valid.

5.7.3 Summary of DMA Transfer Sizes

Table 5-28 lists each of the DMA device transfer sizes. The column labeled “Current Byte/Word Count Register” indicates that the register contents represents either the number of bytes to transfer or the number of 16-bit words to transfer. The column labeled “Current Address Increment/Decrement” indicates the number added to or taken from the Current Address register after each DMA transfer cycle. The DMA Channel Mode Register determines if the Current Address Register will be incremented or decremented.

Table 5-28. DMA Transfer Size

DMA Device Date Size And Word Count	Current Byte/Word Count Register	Current Address Increment/Decrement
8-Bit I/O, Count By Bytes	Bytes	1
16-Bit I/O, Count By Words (Address Shifted)	Words	1

5.7.3.1 Address Shifting When Programmed for 16-Bit I/O Count by Words

The Intel® 631xESB/632xESB I/O Controller Hub maintains compatibility with the implementation of the DMA in the PC AT that used the 82C37. The DMA shifts the addresses for transfers to/from a 16-bit device count-by-words.

Note: The least significant bit of the Low Page Register is dropped in 16-bit shifted mode. When programming the Current Address Register (when the DMA channel is in this mode), the Current Address must be programmed to an even address with the address value shifted right by one bit.

The address shifting is shown in Table 5-29.

Table 5-29. Address Shifting in 16-Bit I/O DMA Transfers

Output Address	8-Bit I/O Programmed Address (Ch 0–3)	16-Bit I/O Programmed Address (Ch 5–7) (Shifted)
A0 A[16:1] A[23:17]	A0 A[16:1] A[23:17]	0 A[15:0] A[23:17]

Note: The least significant bit of the Page Register is dropped in 16-bit shifted mode.

5.7.4 Autoinitialize

By programming a bit in the DMA Channel Mode Register, a channel may be set up as an autoinitialize channel. When a channel undergoes autoinitialization, the original values of the Current Page, Current Address and Current Byte/Word Count Registers are automatically restored from the Base Page, Address, and Byte/Word Count Registers of that channel following TC. The Base Registers are loaded simultaneously with the Current Registers by the microprocessor when the DMA channel is programmed and remain unchanged throughout the DMA service. The mask bit is not set when the channel is in autoinitialize. Following autoinitialize, the channel is ready to perform another DMA service, without processor intervention, as soon as a valid DREQ is detected.

5.7.5 Software Commands

There are three additional special software commands that the DMA controller can execute. The three software commands are:

- Clear Byte Pointer Flip-Flop
- Master Clear
- Clear Mask Register

They do not depend on any specific bit pattern on the data bus.

5.8 LPC DMA

DMA on LPC is handled through the use of the LDRQ# lines from peripherals and special encodings on LAD[3:0] from the host. Single, Demand, Verify, and Increment modes are supported on the LPC interface. Channels 0–3 are 8 bit channels. Channels 5–7 are 16-bit channels. Channel 4 is reserved as a generic Bus Master request.

5.8.1 Asserting DMA Requests

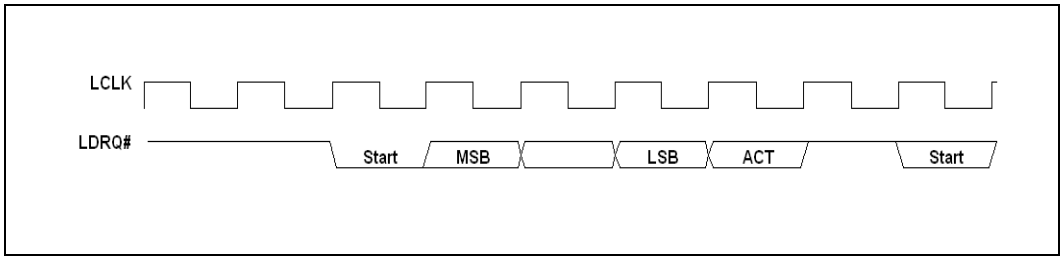
Peripherals that need DMA service encode their requested channel number on the LDRQ# signal. To simplify the protocol, each peripheral on the LPC I/F has its own dedicated LDRQ# signal (they may not be shared between two separate peripherals). The Intel® 631xESB/632xESB I/O Controller Hub has two LDRQ# inputs, allowing at least two devices to support DMA or Bus Mastering.

LDRQ# is synchronous with LCLK (PCI clock). As shown in Figure 5-16, the peripheral uses the following serial encoding sequence:

- Peripheral starts the sequence by asserting LDRQ# low (start bit). LDRQ# is high during idle conditions.
- The next three bits contain the encoded DMA channel number (MSB first).
- The next bit (ACT) indicates whether the request for the indicated DMA channel is active or inactive. The ACT bit is 1 (high) to indicate if it is active and 0 (low) if it is inactive. The case where ACT is low is rare, and is used only to indicate that a previous request for that channel is being abandoned.
- After the active/inactive indication, the LDRQ# signal must go high for at least 1 clock. After that one clock, LDRQ# signal can be brought low to the next encoding sequence.

If another DMA channel also needs to request a transfer, another sequence can be sent on LDRQ#. For example, if an encoded request is sent for channel 2, and then channel 3 needs a transfer before the cycle for channel 2 is run on the interface, the peripheral can send the encoded request for channel 3. This allows multiple DMA agents behind an I/O device to request use of the LPC interface, and the I/O device does not need to self-arbitrate before sending the message.

Figure 5-16. DMA Request Assertion through LDRQ#



5.8.2 Abandoning DMA Requests

DMA Requests can be deasserted in two fashions: on error conditions by sending an LDRQ# message with the ‘ACT’ bit set to 0, or normally through a SYNC field during the DMA transfer. This section describes boundary conditions where the DMA request needs to be removed prior to a data transfer.

There may be some special cases where the peripheral desires to abandon a DMA transfer. The most likely case of this occurring is due to a floppy disk controller which has overrun or underrun its FIFO, or software stopping a device prematurely.

In these cases, the peripheral wishes to stop further DMA activity. It may do so by sending an LDRQ# message with the ACT bit as 0. However, since the DMA request was seen by the Intel® 631xESB/632xESB I/O Controller Hub, there is no guarantee that the cycle has not been granted and will shortly run on LPC. Therefore, peripherals must take into account that a DMA cycle may still occur. The peripheral can choose not to respond to this cycle, in which case the host will abort it, or it can choose to complete the cycle normally with any random data.

This method of DMA deassertion should be prevented whenever possible, to limit boundary conditions both on the Intel® 631xESB/632xESB I/O Controller Hub and the peripheral.

5.8.3 General Flow of DMA Transfers

Arbitration for DMA channels is performed through the 8237 within the host. Once the host has won arbitration on behalf of a DMA channel assigned to LPC, it asserts LFRAME# on the LPC I/F and begins the DMA transfer. The general flow for a basic DMA transfer is as follows:

1. Intel® 631xESB/632xESB I/O Controller Hub starts transfer by asserting 0000b on LAD[3:0] with LFRAME# asserted.
2. Intel® 631xESB/632xESB I/O Controller Hub asserts ‘cycle type’ of DMA, direction based on DMA transfer direction.
3. Intel® 631xESB/632xESB I/O Controller Hub asserts channel number and, if applicable, terminal count.
4. Intel® 631xESB/632xESB I/O Controller Hub indicates the size of the transfer: 8 or 16 bits.
5. If a DMA read…
   - The Intel® 631xESB/632xESB I/O Controller Hub drives the first 8 bits of data and turns the bus around.
   - The peripheral acknowledges the data with a valid SYNC.
   - If a 16-bit transfer, the process is repeated for the next 8 bits.
6. If a DMA write…
   - The Intel® 631xESB/632xESB I/O Controller Hub turns the bus around and waits for data.
   - The peripheral indicates data ready through SYNC and transfers the first byte.
   - If a 16-bit transfer, the peripheral indicates data ready and transfers the next byte.
7. The peripheral turns around the bus.

5.8.4 Terminal Count

Terminal count is communicated through LAD[3] on the same clock that DMA channel is communicated on LAD[2:0]. This field is the CHANNEL field. Terminal count indicates the last byte of transfer, based upon the size of the transfer.

For example, on an 8-bit transfer size (SIZE field is 00b), if the TC bit is set, then this is the last byte. On a 16-bit transfer (SIZE field is 01b), if the TC bit is set, then the second byte is the last byte. The peripheral, therefore, must internalize the TC bit when the CHANNEL field is communicated, and signal TC only when the last byte of that transfer size has been transferred.

5.8.5 Verify Mode

Verify mode is supported on the LPC interface. A verify transfer to the peripheral is similar to a DMA write, where the peripheral is transferring data to main memory. The indication from the host is the same as a DMA write, so the peripheral will be driving data onto the LPC interface. However, the host will not transfer this data into main memory.

5.8.6 DMA Request De-Assertion

An end of transfer is communicated to the Intel® 631xESB/632xESB I/O Controller Hub through a special SYNC field sent by the peripheral. An LPC device must not attempt to signal the end of a transfer by deasserting LDREQ#. If a DMA transfer is several bytes (for example, a transfer from a demand mode device) the Intel® 631xESB/632xESB I/O Controller Hub needs to know when to deassert the DMA request based on the data currently being transferred.

The DMA agent uses a SYNC encoding on each byte of data being transferred, which indicates to the Intel® 631xESB/632xESB I/O Controller Hub whether this is the last byte of transfer or if more bytes are requested. To indicate the last byte of transfer, the peripheral uses a SYNC value of 0000b (ready with no error), or 1010b (ready with error). These encodings tell the Intel® 631xESB/632xESB I/O Controller Hub that this is the last piece of data transferred on a DMA read (Intel® 631xESB/632xESB I/O Controller Hub to peripheral), or the byte that follows is the last piece of data transferred on a DMA write (peripheral to Intel® 631xESB/632xESB I/O Controller Hub).

When the Intel® 631xESB/632xESB I/O Controller Hub sees one of these two encodings, it ends the DMA transfer after this byte and deasserts the DMA request to the 8237. Therefore, if the Intel® 631xESB/632xESB I/O Controller Hub indicated a 16-bit transfer, the peripheral can end the transfer after one byte by indicating a SYNC value of 0000b or 1010b. The Intel® 631xESB/632xESB I/O Controller Hub does not attempt to transfer the second byte, and deasserts the DMA request internally.

If the peripheral indicates a 0000b or 1010b SYNC pattern on the last byte of the indicated size, then the Intel® 631xESB/632xESB I/O Controller Hub only deasserts the DMA request to the 8237 since it does not need to end the transfer.

If the peripheral wishes to keep the DMA request active, then it uses a SYNC value of 1001b (ready plus more data). This tells the 8237 that more data bytes are requested after the current byte has been transferred, so the Intel® 631xESB/632xESB I/O Controller Hub keeps the DMA request active to the 8237. Therefore, on an 8-bit transfer size, if the peripheral indicates a SYNC value of 1001b to the Intel® 631xESB/632xESB I/O Controller Hub, the data will be transferred and the DMA request will remain active to the 8237. At a later time, the Intel® 631xESB/632xESB I/O Controller Hub will then come back with another START–CYCTYPE–CHANNEL–SIZE and so forth. combination to initiate another transfer to the peripheral.

The peripheral must not assume that the next START indication from the Intel® 631xESB/632xESB I/O Controller Hub is another grant to the peripheral if it had indicated a SYNC value of 1001b. On a single mode DMA device, the 8237 will re-

arbitrate after every transfer. Only demand mode DMA devices can be guaranteed that they will receive the next START indication from the Intel® 631xESB/632xESB I/O Controller Hub.

Note: Indicating a 0000b or 1010b encoding on the SYNC field of an odd byte of a 16-bit channel (first byte of a 16 bit transfer) is an error condition.

Note: The host stops the transfer on the LPC bus as indicated, fills the upper byte with random data on DMA writes (peripheral to memory), and indicates to the 8237 that the DMA transfer occurred, incrementing the 8237's address and decrementing its byte count.

5.8.7 SYNC Field / LDRQ# Rules

Since DMA transfers on LPC are requested through an LDRQ# assertion message, and are ended through a SYNC field during the DMA transfer, the peripheral must obey the following rule when initiating back-to-back transfers from a DMA channel.

The peripheral must not assert another message for eight LCLKs after a deassertion is indicated through the SYNC field. This is needed to allow the 8237, that typically runs off a much slower internal clock, to see a message deasserted before it is re-asserted so it can arbitrate to the next agent.

Under default operation, the host performs only 8-bit transfers on 8-bit channels and 16-bit transfers on 16-bit channels.

The method by which this communication between host and peripheral through system BIOS is performed is beyond the scope of this specification. Since the LPC host and LPC peripheral are motherboard devices, no "plug-n-play" registry is required.

The peripheral must not assume that the host is able to perform transfer sizes that are larger than the size allowed for the DMA channel, and be willing to accept a SIZE field that is smaller than what it may currently have buffered.

To that end, it is recommended that future devices that may appear on the LPC bus, that require higher bandwidth than 8-bit or 16-bit DMA allow, do so with a Bus Mastering interface and not rely on the 8237.

5.9 8254 Timers (D31:F0)

The Intel® 631xESB/632xESB I/O Controller Hub contains three counters that have fixed uses. All registers and functions associated with the 8254 timers are in the core well. The 8254 unit is clocked by a 14.31818 MHz clock.

Counter 0, System Timer

This counter functions as the system timer by controlling the state of IRQ0 and is typically programmed for Mode 3 operation. The counter produces a square wave with a period equal to the product of the counter period (838 ns) and the initial count value. The counter loads the initial count value 1 counter period after software writes the count value to the counter I/O address. The counter initially asserts IRQ0 and decrements the count value by two each counter period. The counter negates IRQ0 when the count value reaches 0. It then reloads the initial count value and again decrements the initial count value by two each counter period. The counter then asserts IRQ0 when the count value reaches 0, reloads the initial count value, and repeats the cycle, alternately asserting and negating IRQ0.

Counter 1, Refresh Request Signal

This counter provides the refresh request signal and is typically programmed for Mode 2 operation and impacts only the period of the REF_TOGGLE bit in Port 61. The initial count value is loaded one counter period after being written to the counter I/O address. The REF_TOGGLE bit will have a square wave behavior (alternate between 0 and 1) and will toggle at a rate based on the value in the counter. Programming the counter to anything other than Mode 2 will result in undefined behavior for the REF_TOGGLE bit.

Counter 2, Speaker Tone

This counter provides the speaker tone and is typically programmed for Mode 3 operation. The counter provides a speaker frequency equal to the counter clock frequency (1.193 MHz) divided by the initial count value. The speaker must be enabled by a write to port 061h.

5.9.1 Timer Programming

The counter/timers are programmed in the following fashion:

1. Write a control word to select a counter.
2. Write an initial count for that counter.
3. Load the least and/or most significant bytes (per Control Word bits 5:4) of the 16-bit counter.
4. Repeat with other counters.

Only two conventions need to be observed when programming the counters. First, for each counter, the control word must be written before the initial count is written. Second, the initial count must follow the count format specified in the control word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

A new initial count may be written to a counter at any time without affecting the counter's programmed mode. Counting is affected as described in the mode definitions. The new count must follow the programmed count format.

If a counter is programmed to read/write two-byte counts, a program must not transfer control between writing the first and second byte to another routine which also writes into that same counter. Otherwise, the counter will be loaded with an incorrect count.

The Control Word Register at port 43h controls the operation of all three counters. Several commands are available:

- **Control Word Command.** Specifies which counter to read or write, the operating mode, and the count format (binary or BCD).
- **Counter Latch Command.** Latches the current count so that it can be read by the system. The countdown process continues.
- **Read Back Command.** Reads the count value, programmed mode, the current state of the OUT pins, and the state of the Null Count Flag of the selected counter.

Table 5-30 lists the six operating modes for the interval counters.

Table 5-30. Counter Operating Modes

Mode	Function	Description
0	Out signal on end of count (=0)	Output is 0. When count goes to 0, output goes to 1 and stays at 1 until counter is reprogrammed.
1	Hardware retriggerable one-shot	Output is 0. When count goes to 0, output goes to 1 for one clock time.
2	Rate generator (divide by n counter)	Output is 1. Output goes to 0 for one clock time, then back to 1 and counter is reloaded.
3	Square wave output	Output is 1. Output goes to 0 when counter rolls over, and counter is reloaded. Output goes to 1 when counter rolls over, and counter is reloaded, and so forth.
4	Software triggered strobe	Output is 1. Output goes to 0 when count expires for one clock time.
5	Hardware triggered strobe	Output is 1. Output goes to 0 when count expires for one clock time.

5.9.2 Reading from the Interval Timer

It is often desirable to read the value of a counter without disturbing the count in progress. There are three methods for reading the counters: a simple read operation, counter Latch command, and the Read-Back command. Each is explained below.

With the simple read and counter latch command methods, the count must be read according to the programmed format; specifically, if the counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other. Read, write, or programming operations for other counters may be inserted between them.

5.9.2.1 Simple Read

The first method is to perform a simple read operation. The counter is selected through port 40h (counter 0), 41h (counter 1), or 42h (counter 2).

Note: Performing a direct read from the counter does not return a determinate value, because the counting process is asynchronous to read operations. However, in the case of counter 2, the count can be stopped by writing to the GATE bit in port 61h.

5.9.2.2 Counter Latch Command

The Counter Latch command, written to port 43h, latches the count of a specific counter at the time the command is received. This command is used to ensure that the count read from the counter is accurate, particularly when reading a two-byte count. The count value is then read from each counter's Count register as was programmed by the Control register.

The count is held in the latch until it is read or the counter is reprogrammed. The count is then unlatched. This allows reading the contents of the counters on the fly without affecting counting in progress. Multiple Counter Latch Commands may be used to latch more than one counter. Counter Latch commands do not affect the programmed mode of the counter in any way.

If a Counter is latched and then, some time later, latched again before the count is read, the second Counter Latch command is ignored. The count read is the count at the time the first Counter Latch command was issued.

5.9.2.3 Read Back Command

The Read Back command, written to port 43h, latches the count value, programmed mode, and current states of the OUT pin and Null Count flag of the selected counter or counters. The value of the counter and its status may then be read by I/O access to the counter address.

The Read Back command may be used to latch multiple counter outputs at one time. This single command is functionally equivalent to several counter latch commands, one for each counter latched. Each counter's latched count is held until it is read or reprogrammed. Once read, a counter is unlatched. The other counters remain latched until they are read. If multiple count Read Back commands are issued to the same counter without reading the count, all but the first are ignored.

The Read Back command may additionally be used to latch status information of selected counters. The status of a counter is accessed by a read from that counter's I/O port address. If multiple counter status latch operations are performed without reading status, all but the first are ignored.

Both count and status of the selected counters may be latched simultaneously. This is functionally the same as issuing two consecutive, separate Read Back commands. If multiple count and/or status Read Back commands are issued to the same counters without any intervening reads, all but the first are ignored.

If both count and status of a counter are latched, the first read operation from that counter returns the latched status, regardless of which was latched first. The next one or two reads, depending on whether the counter is programmed for one or two type counts, returns the latched count. Subsequent reads return unlatched count.

5.10 8259 Interrupt Controllers (PIC) (D31:F0)

The Intel® 631xESB/632xESB I/O Controller Hub incorporates the functionality of two 8259 interrupt controllers that provide system interrupts for the ISA compatible interrupts. These interrupts are: system timer, keyboard controller, serial ports, parallel ports, floppy disk, IDE, mouse, and DMA channels. In addition, this interrupt controller can support the PCI based interrupts, by mapping the PCI interrupt onto the compatible ISA interrupt line. Each 8259 core supports eight interrupts, numbered 0–7. Table 5-31 shows how the cores are connected.

Table 5-31. Interrupt Controller Core Connections (Sheet 1 of 2)

8259	8259 Input	Typical Interrupt Source	Connected Pin / Function
Master	0	Internal	Internal Timer / Counter 0 output / HPET #0
	1	Keyboard	IRQ1 via SERIRQ
	2	Internal	Slave controller INTR output
	3	Serial Port A	IRQ3 via SERIRQ, PIRQ#
	4	Serial Port B	IRQ4 via SERIRQ, PIRQ#
	5	Parallel Port / Generic	IRQ5 via SERIRQ, PIRQ#
	6	Floppy Disk	IRQ6 via SERIRQ, PIRQ#
	7	Parallel Port / Generic	IRQ7 via SERIRQ, PIRQ#

Table 5-31. Interrupt Controller Core Connections (Sheet 2 of 2)

8259	8259 Input	Typical Interrupt Source	Connected Pin / Function
Slave	0	Internal Real Time Clock	Internal RTC / HPET #1
	1	Generic	IRQ9 via SERIRQ, SCI, TCO, or PIRQ#
	2	Generic	IRQ10 via SERIRQ, SCI, TCO, or PIRQ#
	3	Generic	IRQ11 via SERIRQ, SCI, TCO, or PIRQ#
	4	PS/2 Mouse	IRQ12 via SERIRQ, SCI, TCO, or PIRQ#
	5	Internal	State Machine output based on processor FERR# assertion. May optionally be used for SCI or TCO interrupt if FERR# not needed.
	6	IDE cable, SATA	IDEIRQ (legacy mode), SATA Primary (legacy mode), or via SERIRQ or PIRQ#
	7	SATAReserved	SATA Secondary (legacy mode) or via SERIRQ or PIRQ#Reserved

The Intel® 631xESB/632xESB I/O Controller Hub cascades the Slave controller onto the Master controller through Master controller interrupt input 2. This means there are only 15 possible interrupts for the Intel® 631xESB/632xESB I/O Controller Hub PIC.

Interrupts can individually be programmed to be edge or level, except for IRQ0, IRQ2, IRQ8#, and IRQ13.

Note: Active-low interrupt sources (for example, the PIRQ#s) are inverted inside the Intel® 631xESB/632xESB I/O Controller Hub. In the following descriptions of the 8259s, the interrupt levels are in reference to the signals at the internal interface of the 8259s, after the required inversions have occurred. Therefore, the term “high” indicates “active,” which means “low” on an originating PIRQ#.

5.10.1 Interrupt Handling

5.10.1.1 Generating Interrupts

The PIC interrupt sequence involves three bits, from the IRR, ISR, and IMR, for each interrupt level. These bits are used to determine the interrupt vector returned, and status of any other pending interrupts. Table 5-32 defines the IRR, ISR, and IMR.

Table 5-32. Interrupt Status Registers

Bit	Description
IRR	**Interrupt Request Register.** This bit is set on a low to high transition of the interrupt line in edge mode, and by an active high level in level mode. This bit is set whether or not the interrupt is masked. However, a masked interrupt will not generate INTR.
ISR	**Interrupt Service Register.** This bit is set, and the corresponding IRR bit cleared, when an interrupt acknowledge cycle is seen, and the vector returned is for that interrupt.
IMR	**Interrupt Mask Register.** This bit determines whether an interrupt is masked. Masked interrupts will not generate INTR.

5.10.1.2 Acknowledging Interrupts

The processor generates an interrupt acknowledge cycle that is translated by the host bridge into a PCI Interrupt Acknowledge Cycle to the Intel® 631xESB/632xESB I/O Controller Hub. The PIC translates this command into two internal INTA# pulses expected by the 8259 cores. The PIC uses the first internal INTA# pulse to freeze the state of the interrupts for priority resolution. On the second INTA# pulse, the Master or

Slave sends the interrupt vector to the processor with the acknowledged interrupt code. This code is based upon bits [7:3] of the corresponding ICW2 register, combined with three bits representing the interrupt within that controller.

Table 5-33. Content of Interrupt Vector Byte

Master, Slave Interrupt	Bits [7:3]	Bits [2:0]
IRQ7,15	ICW2[7:3]	111
IRQ6,14		110
IRQ5,13		101
IRQ4,12		100
IRQ3,11		011
IRQ2,10		010
IRQ1,9		001
IRQ0,8		000

5.10.1.3 Hardware/Software Interrupt Sequence

1. One or more of the Interrupt Request lines (IRQ) are raised high in edge mode, or seen high in level mode, setting the corresponding IRR bit.
2. The PIC sends INTR active to the processor if an asserted interrupt is not masked.
3. The processor acknowledges the INTR and responds with an interrupt acknowledge cycle. The cycle is translated into a PCI interrupt acknowledge cycle by the host bridge. This command is broadcast over PCI by the Intel® 631xESB/632xESB I/O Controller Hub.
4. Upon observing its own interrupt acknowledge cycle on PCI, the Intel® 631xESB/632xESB I/O Controller Hub converts it into the two cycles that the internal 8259 pair can respond to. Each cycle appears as an interrupt acknowledge pulse on the internal INTA# pin of the cascaded interrupt controllers.
5. Upon receiving the first internally generated INTA# pulse, the highest priority ISR bit is set and the corresponding IRR bit is reset. On the trailing edge of the first pulse, a Slave identification code is broadcast by the Master to the Slave on a private, internal three bit wide bus. The Slave controller uses these bits to determine if it must respond with an interrupt vector during the second INTA# pulse.
6. Upon receiving the second internally generated INTA# pulse, the PIC returns the interrupt vector. If no interrupt request is present because the request was too short in duration, the PIC returns vector 7 from the Master controller.
7. This completes the interrupt cycle. In AEOI mode the ISR bit is reset at the end of the second INTA# pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.

5.10.2 Initialization Command Words (ICWx)

Before operation can begin, each 8259 must be initialized. In the Intel® 631xESB/632xESB I/O Controller Hub, this is a four byte sequence. The four initialization command words are referred to by their acronyms: ICW1, ICW2, ICW3, and ICW4.

The base address for each 8259 initialization command word is a fixed location in the I/O memory space: 20h for the Master controller, and A0h for the Slave controller.

5.10.2.1 ICW1

An I/O write to the Master or Slave controller base address with data bit 4 equal to 1 is interpreted as a write to ICW1. Upon sensing this write, the Intel® 631xESB/632xESB I/O Controller Hub PIC expects three more byte writes to 21h for the Master controller, or A1h for the Slave controller, to complete the ICW sequence.

A write to ICW1 starts the initialization sequence during which the following automatically occur:

1. Following initialization, an interrupt request (IRQ) input must make a low-to-high transition to generate an interrupt.
2. The Interrupt Mask Register is cleared.
3. IRQ7 input is assigned priority 7.
4. The Slave mode address is set to 7.
5. Special mask mode is cleared and Status Read is set to IRR.

5.10.2.2 ICW2

The second write in the sequence (ICW2) is programmed to provide bits [7:3] of the interrupt vector that will be released during an interrupt acknowledge. A different base is selected for each interrupt controller.

5.10.2.3 ICW3

The third write in the sequence (ICW3) has a different meaning for each controller.

- For the Master controller, ICW3 is used to indicate which IRQ input line is used to cascade the Slave controller. Within the Intel® 631xESB/632xESB I/O Controller Hub, IRQ2 is used. Therefore, bit 2 of ICW3 on the Master controller is set to a 1, and the other bits are set to 0s.
- For the Slave controller, ICW3 is the Slave identification code used during an interrupt acknowledge cycle. On interrupt acknowledge cycles, the Master controller broadcasts a code to the Slave controller if the cascaded interrupt won arbitration on the Master controller. The Slave controller compares this identification code to the value stored in its ICW3, and if it matches, the Slave controller assumes responsibility for broadcasting the interrupt vector.

5.10.2.4 ICW4

The final write in the sequence (ICW4) must be programmed for both controllers. At the very least, bit 0 must be set to a 1 to indicate that the controllers are operating in an Intel Architecture-based system.

5.10.3 Operation Command Words (OCW)

These command words reprogram the Interrupt controller to operate in various interrupt modes.

- OCW1 masks and unmasks interrupt lines.
- OCW2 controls the rotation of interrupt priorities when in rotating priority mode, and controls the EOI function.
- OCW3 is sets up ISR/IRR reads, enables/disables the special mask mode (SMM), and enables/disables polled interrupt mode.

5.10.4 Modes of Operation

5.10.4.1 Fully Nested Mode

In this mode, interrupt requests are ordered in priority from 0 through 7, with 0 being the highest. When an interrupt is acknowledged, the highest priority request is determined and its vector placed on the bus. Additionally, the ISR for the interrupt is set. This ISR bit remains set until: the processor issues an EOI command immediately before returning from the service routine; or if in AEOI mode, on the trailing edge of the second INTA#. While the ISR bit is set, all further interrupts of the same or lower priority are inhibited, while higher levels generate another interrupt. Interrupt priorities can be changed in the rotating priority mode.

5.10.4.2 Special Fully-Nested Mode

This mode is used in the case of a system where cascading is used, and the priority has to be conserved within each Slave. In this case, the special fully-nested mode is programmed to the Master controller. This mode is similar to the fully-nested mode with the following exceptions:

- When an interrupt request from a certain Slave is in service, this Slave is not locked out from the Master's priority logic and further interrupt requests from higher priority interrupts within the Slave are recognized by the Master and initiate interrupts to the processor. In the normal-nested mode, a Slave is masked out when its request is in service.
- When exiting the Interrupt Service routine, software has to check whether the interrupt serviced was the only one from that Slave. This is done by sending a Non-Specific EOI command to the Slave and then reading its ISR. If it is 0, a non-specific EOI can also be sent to the Master.

5.10.4.3 Automatic Rotation Mode (Equal Priority Devices)

In some applications, there are a number of interrupting devices of equal priority. Automatic rotation mode provides for a sequential 8-way rotation. In this mode, a device receives the lowest priority after being serviced. In the worst case, a device requesting an interrupt has to wait until each of seven other devices are serviced at most once.

There are two ways to accomplish automatic rotation using OCW2; the Rotation on Non-Specific EOI Command (R=1, SL=0, EOI=1) and the rotate in automatic EOI mode which is set by (R=1, SL=0, EOI=0).

5.10.4.4 Specific Rotation Mode (Specific Priority)

Software can change interrupt priorities by programming the bottom priority. For example, if IRQ5 is programmed as the bottom priority device, then IRQ6 is the highest priority device. The Set Priority Command is issued in OCW2 to accomplish this, where: R=1, SL=1, and LO–L2 is the binary priority level code of the bottom priority device.

In this mode, internal status is updated by software control during OCW2. However, it is independent of the EOI command. Priority changes can be executed during an EOI command by using the Rotate on Specific EOI Command in OCW2 (R=1, SL=1, EOI=1 and LO–L2=IRQ level to receive bottom priority.

5.10.4.5 Poll Mode

Poll mode can be used to conserve space in the interrupt vector table. Multiple interrupts that can be serviced by one interrupt service routine do not need separate vectors if the service routine uses the poll command. Poll mode can also be used to expand the number of interrupts. The polling interrupt service routine can call the appropriate service routine, instead of providing the interrupt vectors in the vector table. In this mode, the INTR output is not used and the microprocessor internal Interrupt Enable flip-flop is reset, disabling its interrupt input. Service to devices is achieved by software using a Poll command.

The Poll command is issued by setting P=1 in OCW3. The PIC treats its next I/O read as an interrupt acknowledge, sets the appropriate ISR bit if there is a request, and reads the priority level. Interrupts are frozen from the OCW3 write to the I/O read. The byte returned during the I/O read contains a 1 in bit 7 if there is an interrupt, and the binary code of the highest priority level in bits 2:0.

5.10.4.6 Cascade Mode

The PIC in Intel® 631xESB/632xESB I/O Controller Hub has one Master 8259 and one Slave 8259 cascaded onto the Master through IRQ2. This configuration can handle up to 15 separate priority levels. The Master controls the Slaves through a three bit internal bus. In the Intel® 631xESB/632xESB I/O Controller Hub, when the Master drives 010b on this bus, the Slave controller takes responsibility for returning the interrupt vector. An EOI command must be issued twice: once for the Master and once for the Slave.

5.10.4.7 Edge and Level Triggered Mode

In ISA systems this mode is programmed using bit 3 in ICW1, which sets level or edge for the entire controller. In the Intel® 631xESB/632xESB I/O Controller Hub, this bit is disabled and a new register for edge and level triggered mode selection, per interrupt input, is included. This is the Edge/Level control Registers ELCR1 and ELCR2.

If an ELCR bit is 0, an interrupt request will be recognized by a low-to-high transition on the corresponding IRQ input. The IRQ input can remain high without generating another interrupt. If an ELCR bit is 1, an interrupt request will be recognized by a high level on the corresponding IRQ input and there is no need for an edge detection. The interrupt request must be removed before the EOI command is issued to prevent a second interrupt from occurring.

In both the edge and level triggered modes, the IRQ inputs must remain active until after the falling edge of the first internal INTA#. If the IRQ input goes inactive before this time, a default IRQ7 vector is returned.

5.10.4.8 End of Interrupt (EOI) Operations

An EOI can occur in one of two fashions: by a command word write issued to the PIC before returning from a service routine, the EOI command; or automatically when AEOI bit in ICW4 is set to 1.

5.10.4.9 Normal End of Interrupt

In normal EOI, software writes an EOI command before leaving the interrupt service routine to mark the interrupt as completed. There are two forms of EOI commands: Specific and Non-Specific. When a Non-Specific EOI command is issued, the PIC clears the highest ISR bit of those that are set to 1. Non-Specific EOI is the normal mode of

operation of the PIC within the Intel® 631xESB/632xESB I/O Controller Hub, as the interrupt being serviced currently is the interrupt entered with the interrupt acknowledge. When the PIC is operated in modes that preserve the fully nested structure, software can determine which ISR bit to clear by issuing a Specific EOI. An ISR bit that is masked is not cleared by a Non-Specific EOI if the PIC is in the special mask mode. An EOI command must be issued for both the Master and Slave controller.

5.10.4.10 Automatic End of Interrupt Mode

In this mode, the PIC automatically performs a Non-Specific EOI operation at the trailing edge of the last interrupt acknowledge pulse. From a system standpoint, this mode should be used only when a nested multi-level interrupt structure is not required within a single PIC. The AEOI mode can be used only in the Master controller and not the Slave controller.

5.10.5 Masking Interrupts

5.10.5.1 Masking on an Individual Interrupt Request

Each interrupt request can be masked individually by the Interrupt Mask Register (IMR). This register is programmed through OCW1. Each bit in the IMR masks one interrupt channel. Masking IRQ2 on the Master controller masks all requests for service from the Slave controller.

5.10.5.2 Special Mask Mode

Some applications may require an interrupt service routine to dynamically alter the system priority structure during its execution under software control. For example, the routine may wish to inhibit lower priority requests for a portion of its execution but enable some of them for another portion.

The special mask mode enables all interrupts not masked by a bit set in the Mask register. Normally, when an interrupt service routine acknowledges an interrupt without issuing an EOI to clear the ISR bit, the interrupt controller inhibits all lower priority requests. In the special mask mode, any interrupts may be selectively enabled by loading the Mask Register with the appropriate pattern. The special mask mode is set by OCW3 where: SSMM=1, SMM=1, and cleared where SSMM=1, SMM=0.

5.10.6 Steering PCI Interrupts

The Intel® 631xESB/632xESB I/O Controller Hub can be programmed to allow PIRQA#-PIRQH# to be internally routed to interrupts
3–7, 9–12, 14 or 15. The assignment is programmable through the through the PIRQx Route Control registers, located at 60–63h and 68–6Bh in Device 31:Function 0. One or more PIRQx# lines can be routed to the same IRQx input. If interrupt steering is not required, the Route registers can be programmed to disable steering.

The PIRQx# lines are defined as active low, level sensitive to allow multiple interrupts on a PCI board to share a single line across the connector. When a PIRQx# is routed to specified IRQ line, software must change the IRQ's corresponding ELCR bit to level sensitive mode. The Intel® 631xESB/632xESB I/O Controller Hub internally inverts the PIRQx# line to send an active high level to the PIC. When a PCI interrupt is routed onto the PIC, the selected IRQ can no longer be used by an acting high device (through SERIRQ). However, active low interrupts can share their interrupt with PCI interrupts.

Internal sources of the PIRQs, including SCI and TCO interrupts, cause the external PIRQ to be asserted. The Intel® 631xESB/632xESB I/O Controller Hub receives the PIRQ input, like all of the other external sources, and routes it accordingly.

5.11 Advanced Programmable Interrupt Controller (APIC) (D31:F0)

In addition to the standard ISA-compatible PIC described in the previous chapter, the Intel® 631xESB/632xESB I/O Controller Hub incorporates two APICs (diagram shown in Figure 5-6), one I/OxAPIC (Bm:D0:F1) resides in Bus M, for information, refer to Section 5.1.4). While the standard interrupt controller is intended for use in a uniprocessor system, APIC can be used in either a uniprocessor or multiprocessor system.

5.11.1 Interrupt Handling

The I/O APIC handles interrupts very differently than the 8259. Briefly, these differences are:

- **Method of Interrupt Transmission.** The I/O APIC transmits interrupts through memory writes on the normal datapath to the processor, and interrupts are handled without the need for the processor to run an interrupt acknowledge cycle.
- **Interrupt Priority.** The priority of interrupts in the I/O APIC is independent of the interrupt number. For example, interrupt 10 can be given a higher priority than interrupt 3.
- **More Interrupts.** The I/O APIC in the Intel® 631xESB/632xESB I/O Controller Hub supports a total of 24 interrupts.
- **Multiple Interrupt Controllers.** The I/O APIC architecture allows for multiple I/O APIC devices in the system with their own interrupt vectors.

5.11.2 Interrupt Mapping

The I/O APIC within the Intel® 631xESB/632xESB I/O Controller Hub supports 24 APIC interrupts. Each interrupt has its own unique vector assigned by software. The interrupt vectors are mapped as follows, and match “Config 6” of the Multiprocessor Specification.

Table 5-34. APIC Interrupt Mapping (Sheet 1 of 2)

IRQ #	Via SERIRQ	Direct from Pin	Via PCI Message	Internal Modules
0	No	No	No	Cascade from 8259 #1
1	Yes	No	Yes	
2	No	No	No	8254 Counter 0, HPET #0 (legacy mode)
3	Yes	No	Yes	
4	Yes	No	Yes	
5	Yes	No	Yes	
6	Yes	No	Yes	
7	Yes	No	Yes	
8	No	No	No	RTC, HPET #1 (legacy mode)
9	Yes	No	Yes	Option for SCI, TCO

Table 5-34. APIC Interrupt Mapping (Sheet 2 of 2)

IRQ #	Via SERIRQ	Direct from Pin	Via PCI Message	Internal Modules
10	Yes	No	Yes	Option for SCI, TCO
11	Yes	No	Yes	HPET #2, Option for SCI, TCO
12	Yes	No	Yes	
13	No	No	No	FERR# logic
14	Yes	Yes[1]	Yes	IDEIRQ (legacy mode), SATA Primary (legacy mode)
15	Yes	Yes	Yes	SATA Secondary (legacy mode)
16	PIRQA#	PIRQA#	No[4]	USB UHCI Controller #1, USB UHCI Controller #4
17	PIRQB#	PIRQB#	No[4]	AC'97 Audio, Modem, option for SMBus
18	PIRQC#	PIRQC#	No[4]	USB UHCI Controller #3, Storage (IDE/SATA) Native mode
19	PIRQD#	PIRQD#	No[4]	USB UHCI Controller #2
20	N/A	PIRQE#	No[4]	LAN, option for SCI, TCO, HPET #0,1,2
21	N/A	PIRQF#	Yes	Option for SCI, TCO, HPET #0,1,2
22	N/A	PIRQG#	Yes	Option for SCI, TCO, HPET #0,1,2
23	N/A	PIRQH#	No[4]	USB EHCI Controller, option for SCI, TCO, HPET #0,1,2

Notes:
1. IDEIRQ can be driven directly from the pin only when in legacy IDE mode.
2. When programming the polarity of internal interrupt sources on the APIC, interrupts 0 through 15 receive active-high internal interrupt sources, while interrupts 16 through 23 receive active-low internal interrupt sources.
3. If IRQ 11 is used for HPET #2, software should ensure IRQ 11 is not shared with any other devices to guarantee the proper operation of HPET #2. Intel® 631xESB/632xESB I/O Controller Hub hardware does not prevent sharing of IRQ 11.
4. PCI Message interrupts are not prevented by hardware in these cases. However, the system must not program these interrupts as edge-triggered (as required for PCI message interrupts) because the internal and external PIRQs on these inputs must be programmed in level-triggered modes.

5.11.3 PCI/PCI Express* Message-Based Interrupts

When external devices connected by way of PCI/PCI Express wish to generate an interrupt, they will send the message defined in the PCI Express specification for generating INTA# - INTD#. These will be translated internal assertions/de-assertions of INTA# - INTD#.

5.11.4 System Bus Interrupt Delivery

For processors that support System Bus interrupt delivery, the Intel® 631xESB/632xESB I/O Controller Hub requires that the I/O APIC deliver interrupt messages to the processor in a parallel manner, rather than using the I/O APIC serial scheme.

This is done by the Intel® 631xESB/632xESB I/O Controller Hub writing (by way of ESI) to a memory location that is snooped by the processor(s). The processor(s) snoop the cycle to know which interrupt goes active.

The following sequence is used:

1. When the Intel® 631xESB/632xESB I/O Controller Hub detects an interrupt event (active edge for edge-triggered mode or a change for level-triggered mode), it sets or resets the internal IRR bit associated with that interrupt.

2. Internally, the Intel® 631xESB/632xESB I/O Controller Hub requests to use the bus in a way that automatically flushes upstream buffers. This can be internally implemented similar to a DMA device request.
3. The Intel® 631xESB/632xESB I/O Controller Hub then delivers the message by performing a write cycle to the appropriate address with the appropriate data. The address and data formats are described below in Section 5.11.4.4.

Note: System Bus Interrupt Delivery compatibility with processor clock control depends on the processor, not the Intel® 631xESB/632xESB I/O Controller Hub.

5.11.4.1 Edge-Triggered Operation

In this case, the “Assert Message” is sent when there is an inactive-to-active edge on the interrupt.

5.11.4.2 Level-Triggered Operation

In this case, the “Assert Message” is sent when there is an inactive-to-active edge on the interrupt. If after the EOI the interrupt is still active, then another “Assert Message” is sent to indicate that the interrupt is still active.

5.11.4.3 Registers Associated with System Bus Interrupt Delivery

Capabilities Indication: The capability to support System Bus interrupt delivery is indicated by way of ACPI configuration techniques. This involves the BIOS creating a data structure that gets reported to the ACPI configuration software.

5.11.4.4 Interrupt Message Format

The Intel® 631xESB/632xESB I/O Controller Hub writes the message to PCI (and to the Host controller) as a 32-bit memory write cycle. It uses the formats shown in Table 5-35 and Table 5-36 for the address and data.

The local APIC (in the processor) has a delivery mode option to interpret Front Side Bus messages as a SMI in which case the processor treats the incoming interrupt as a SMI instead of as an interrupt. This does not mean that the Intel® 631xESB/632xESB I/O Controller Hub has any way to have a SMI source from Intel® 631xESB/632xESB I/O Controller Hub power management logic cause the I/O APIC to send an SMI message (there is no way to do this). The Intel® 631xESB/632xESB I/O Controller Hub’s I/O APIC can send interrupts only, due to interrupts which do not include SMI, NMI or INIT. This means that in Itanium architecture-based systems, System Bus interrupt message format delivery modes 010 (SMI/PMI), 100 (NMI), and 101 (INIT) as indicated in this section, must not be used and is not supported. Only the hardware pin connection is supported by Intel® 631xESB/632xESB I/O Controller Hub.

Table 5-35. Interrupt Message Address Format (Sheet 1 of 2)

Bit	Description
31:20	Will always be FEEh.
19:12	**Destination ID:** This is the same as bits 63:56 of the I/O Redirection Table entry for the interrupt associated with this message.
11:4	**Extended Destination ID**: This is the same as bits 55:48 of the I/O Redirection Table entry for the interrupt associated with this message.

Table 5-35. Interrupt Message Address Format (Sheet 2 of 2)

Bit	Description
3	**Redirection Hint:** This bit is used by the processor host bridge to allow the interrupt message to be redirected. 0 = The message will be delivered to the agent (processor) listed in bits 19:12. 1 = The message will be delivered to an agent with a lower interrupt priority. This can be derived from bits 10:8 in the Data Field (see below). The Redirection Hint bit will be a 1 if bits 10:8 in the delivery mode field associated with corresponding interrupt are encoded as 001 (Lowest Priority). Otherwise, the Redirection Hint bit will be 0.
2	**Destination Mode:** This bit is used only when the Redirection Hint bit is set to 1. If the Redirection Hint bit and the Destination Mode bit are both set to 1, then the logical destination mode is used, and the redirection is limited to only those processors that are part of the logical group as based on the logical ID.
1:0	Will always be 00.

Table 5-36. Interrupt Message Data Format

Bit	Description
31:16	Will always be 0000h.
15	**Trigger Mode:** 1 = Level, 0 = Edge. Same as the corresponding bit in the I/O Redirection Table for that interrupt.
14	**Delivery Status:** 1 = Assert, 0 = Deassert. Only Assert message are sent, this bit is always 1.
13:12	Will always be 00
11	**Destination Mode:** 1 = Logical. 0 = Physical. Same as the corresponding bit in the I/O Redirection Table for that interrupt.
10:8	**Delivery Mode:** This is the same as the corresponding bits in the I/O Redirection Table for that interrupt. 000 = Fixed 100 = NMI 001 = Lowest Priority 101 = INIT 010 = SMI/PMI 110 = Reserved 011 = Reserved 111 = ExtINT
7:0	**Vector:** This is the same as the corresponding bits in the I/O Redirection Table for that interrupt.

5.12 Serial Interrupt (D31:F0)

The Intel® 631xESB/632xESB I/O Controller Hub supports a serial IRQ scheme. This allows a single signal to be used to report interrupt requests. The signal used to transmit this information is shared between the host, the Intel® 631xESB/632xESB I/O Controller Hub, and all peripherals that support serial interrupts. The signal line, SERIRQ, is synchronous to PCI clock, and follows the sustained tri-state protocol that is used by all PCI signals. This means that if a device has driven SERIRQ low, it will first drive it high synchronous to PCI clock and release it the following PCI clock. The serial IRQ protocol defines this sustained tri-state signaling in the following fashion:

- **S – Sample Phase.** Signal driven low
- **R – Recovery Phase.** Signal driven high
- **T – Turn-around Phase.** Signal released

The Intel® 631xESB/632xESB I/O Controller Hub supports a message for 21 serial interrupts. These represent the 15 ISA interrupts (IRQ0–1, 2–15), the four PCI interrupts, and the control signals SMI# and IOCHK#. The serial IRQ protocol does not support the additional APIC interrupts (20–23).

Note: When the IDE controller is enabled or the SATA controller is configured for legacy IDE mode, IRQ14 and IRQ15 are not accessible to the Interrupt controllers through the Serial Interrupt pin.

5.12.1 Start Frame

The serial IRQ protocol has two modes of operation which affect the start frame. These two modes are: Continuous, where the Intel® 631xESB/632xESB I/O Controller Hub is solely responsible for generating the start frame; and Quiet, where a serial IRQ peripheral is responsible for beginning the start frame.

The mode that must first be entered when enabling the serial IRQ protocol is continuous mode. In this mode, the Intel® 631xESB/632xESB I/O Controller Hub asserts the start frame. This start frame is 4, 6, or 8 PCI clocks wide based upon the Serial IRQ Control Register, bits 1:0 at 64h in Device 31:Function 0 configuration space. This is a polling mode.

When the serial IRQ stream enters quiet mode (signaled in the Stop Frame), the SERIRQ line remains inactive and pulled up between the Stop and Start Frame until a peripheral drives the SERIRQ signal low. The Intel® 631xESB/632xESB I/O Controller Hub senses the line low and continues to drive it low for the remainder of the Start Frame. Since the first PCI clock of the start frame was driven by the peripheral in this mode, the Intel® 631xESB/632xESB I/O Controller Hub drives the SERIRQ line low for 1 PCI clock less than in continuous mode. This mode of operation allows for a quiet, and therefore lower power, operation.

5.12.2 Data Frames

Once the Start frame has been initiated, all of the SERIRQ peripherals must start counting frames based on the rising edge of SERIRQ. Each of the IRQ/DATA frames has exactly 3 phases of 1 clock each:

- **Sample Phase.** During this phase, the SERIRQ device drives SERIRQ low if the corresponding interrupt signal is low. If the corresponding interrupt is high, then the SERIRQ devices tri-state the SERIRQ signal. The SERIRQ line remains high due to pull-up resistors (there is no internal pull-up resistor on this signal, an external pull-up resistor is required). A low level during the IRQ0–1 and IRQ2–15 frames

indicates that an active-high ISA interrupt is not being requested, but a low level during the PCI INT[A:D], SMI#, and IOCHK# frame indicates that an active-low interrupt is being requested.

- **Recovery Phase.** During this phase, the device drives the SERIRQ line high if in the Sample Phase it was driven low. If it was not driven in the sample phase, it is tri-stated in this phase.
- **Turn-around Phase.** The device tri-states the SERIRQ line.

5.12.3 Stop Frame

After all data frames, a Stop Frame is driven by the Intel® 631xESB/632xESB I/O Controller Hub. The SERIRQ signal is driven low by the Intel® 631xESB/632xESB I/O Controller Hub for 2 or 3 PCI clocks. The number of clocks is determined by the SERIRQ configuration register. The number of clocks determines the next mode:

Table 5-37. Stop Frame Explanation

Stop Frame Width	Next Mode
2 PCI clocks	**Quiet Mode.** Any SERIRQ device may initiate a Start Frame
3 PCI clocks	**Continuous Mode.** Only the host (Intel® 631xESB/632xESB I/O Controller Hub) may initiate a Start Frame

5.12.4 Specific Interrupts Not Supported by way of SERIRQ

There are three interrupts seen through the serial stream that are not supported by the Intel® 631xESB/632xESB I/O Controller Hub. These interrupts are generated internally, and are not sharable with other devices within the system. These interrupts are:

- IRQ0. Heartbeat interrupt generated off of the internal 8254 counter 0.
- IRQ8#. RTC interrupt can be generated only internally.
- IRQ13. Floating point error interrupt generated off of the processor assertion of FERR#.

The Intel® 631xESB/632xESB I/O Controller Hub ignores the state of these interrupts in the serial stream, and does not adjust their level based on the level seen in the serial stream.

5.12.5 Data Frame Format

Table 5-38 shows the format of the data frames. For the PCI interrupts (A–D), the output from the Intel® 631xESB/632xESB I/O Controller Hub is ANDed with the PCI input signal. This way, the interrupt can be signaled by way of both the PCI interrupt input signal and by way of the SERIRQ signal (they are shared).

Table 5-38. Data Frame Format (Sheet 1 of 2)

Data Frame #	Interrupt	Clocks Past Start Frame	Comment
1	IRQ0	2	Ignored. IRQ0 can be generated only by way of the internal 8524
2	IRQ1	5	
3	SMI#	8	Causes SMI# if low. Will set the SERIRQ_SMI_STS bit.
4	IRQ3	11	

Table 5-38. Data Frame Format (Sheet 2 of 2)

Data Frame #	Interrupt	Clocks Past Start Frame	Comment
5	IRQ4	14	
6	IRQ5	17	
7	IRQ6	20	
8	IRQ7	23	
9	IRQ8	26	Ignored. IRQ8# can be generated internally only.
10	IRQ9	29	
11	IRQ10	32	
12	IRQ11	35	
13	IRQ12	38	
14	IRQ13	41	Ignored. IRQ13 can be generated only from FERR#
15	IRQ14	44	Not attached to PATA or SATA logic
16	IRQ15	47	Not attached to PATA or SATA logic
17	IOCHCK#	50	Same as ISA IOCHCK# going active.
18	PCI INTA#	53	Drive PIRQA#
19	PCI INTB#	56	Drive PIRQB#
20	PCI INTC#	59	Drive PIRQC#
21	PCI INTD#	62	Drive PIRQD#

5.13 Real Time Clock (D31:F0)

The Real Time Clock (RTC) module provides a battery backed-up date and time keeping device with two banks of static RAM with 128 bytes each, although the first bank has 114 bytes for general purpose usage. Three interrupt features are available: time of day alarm with once a second to once a month range, periodic rates of 122 µs to 500 ms, and end of update cycle notification. Seconds, minutes, hours, days, day of week, month, and year are counted. Daylight savings compensation is available. The hour is represented in twelve or twenty-four hour format, and data can be represented in BCD or binary format. The design is functionally compatible with the Motorola MS146818B. The time keeping comes from a 32.768 kHz oscillating source, which is divided to achieve an update every second. The lower 14 bytes on the lower RAM block has very specific functions. The first ten are for time and date information. The next four (0Ah to 0Dh) are registers, which configure and report RTC functions.

The time and calendar data should match the data mode (BCD or binary) and hour mode (12 or 24 hour) as selected in register B. It is up to the programmer to make sure that data stored in these locations is within the reasonable values ranges and represents a possible date and time. The exception to these ranges is to store a value of C0–FFh in the Alarm bytes to indicate a don't care situation. All Alarm conditions must match to trigger an Alarm Flag, which could trigger an Alarm Interrupt if enabled. The SET bit must be 1 while programming these locations to avoid clashes with an update cycle. Access to time and date information is done through the RAM locations. If a RAM read from the ten time and date bytes is attempted during an update cycle, the value read do not necessarily represent the true contents of those locations. Any RAM writes under the same conditions are ignored.

Note: The leap year determination for adding a 29th day to February does not take into account the end-of-the-century exceptions. The logic simply assumes that all years divisible by 4 are leap years. According to the Royal Observatory Greenwich, years that

are divisible by 100 are typically not leap years. In every fourth century (years divisible by 400, like 2000), the 100-year-exception is over-ridden and a leap-year occurs. Note that the year 2100 will be the first time in which the current RTC implementation would incorrectly calculate the leap-year.

The Intel® 631xESB/632xESB I/O Controller Hub does not implement month/year alarms.

5.13.1 Update Cycles

An update cycle occurs once a second, if the SET bit of register B is not asserted and the divide chain is properly configured. During this procedure, the stored time and date are incremented, overflow is checked, a matching alarm condition is checked, and the time and date are rewritten to the RAM locations. The update cycle will start at least 488 µs after the UIP bit of register A is asserted, and the entire cycle does not take more than 1984 µs to complete. The time and date RAM locations (0–9) are disconnected from the external bus during this time.

To avoid update and data corruption conditions, external RAM access to these locations can safely occur at two times. When a updated-ended interrupt is detected, almost 999 ms is available to read and write the valid time and date data. If the UIP bit of Register A is detected to be low, there is at least 488 µs before the update cycle begins.

Warning: The overflow conditions for leap years and daylight savings adjustments are based on more than one date or time item. To ensure proper operation when adjusting the time, the new time and data values should be set at least two seconds before one of these conditions (leap year, daylight savings time adjustments) occurs.

5.13.2 Interrupts

The real-time clock interrupt is internally routed within the Intel® 631xESB/632xESB I/O Controller Hub both to the I/O APIC and the 8259. It is mapped to interrupt vector 8. This interrupt does not leave the Intel® 631xESB/632xESB I/O Controller Hub, nor is it shared with any other interrupt. IRQ8# from the SERIRQ stream is ignored. However, the High Performance Event Timers can also be mapped to IRQ8#; in this case, the RTC interrupt is blocked.

5.13.3 Lockable RAM Ranges

The RTC's battery-backed RAM supports two 8-byte ranges that can be locked by way of the configuration space. If the locking bits are set, the corresponding range in the RAM will not be readable or writable. A write cycle to those locations will have no effect. A read cycle to those locations will not return the location's actual value (resultant value is undefined).

Once a range is locked, the range can be unlocked only by a hard reset, which will invoke the BIOS and allow it to relock the RAM range.

5.13.4 Century Rollover

The Intel® 631xESB/632xESB I/O Controller Hub detects a rollover when the Year byte (RTC I/O space, index offset 09h) transitions form 99 to 00. Upon detecting the rollover, the Intel® 631xESB/632xESB I/O Controller Hub sets the NEWCENTURY_STS bit (TCOBASE + 04h, bit 7). If the system is in an S0 state, this causes an SMI#. The SMI# handler can update registers in the RTC RAM that are associated with century value. If the system is in a sleep state (S1–S5) when the century rollover occurs, the

Intel® 631xESB/632xESB I/O Controller Hub also sets the NEWCENTURY_STS bit, but no SMI# is generated. When the system resumes from the sleep state, BIOS should check the NEWCENTURY_STS bit and update the century value in the RTC RAM.

5.13.5 Clearing Battery-Backed RTC RAM

Clearing CMOS RAM in an Intel® 631xESB/632xESB I/O Controller Hub-based platform can be done by using a jumper on RTCRST# or GPI. Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low.

Using RTCRST# to clear CMOS

A jumper on RTCRST# can be used to clear CMOS values, as well as reset to default, the state of those configuration bits that reside in the RTC power well. When the RTCRST# is strapped to ground, the RTC_PWR_STS bit (D31:F0:A4h bit 2) will be set and those configuration bits in the RTC power well will be set to their default state. BIOS can monitor the state of this bit, and manually clear the RTC CMOS array once the system is booted. The normal position would cause RTCRST# to be pulled up through a weak pull-up resistor. Table 5-39 shows which bits are set to their default state when RTCRST# is asserted. This RTCRST# jumper technique allows the jumper to be moved and then replaced, all while the system is powered off. Then, once booted, the RTC_PWR_STS can be detected in the set state.

Table 5-39. Configuration Bits Reset by RTCRST# Assertion (Sheet 1 of 2)

Bit Name	Register	Location	Bit(s)	Default State
Alarm Interrupt Enable (AIE)	I/O space (RTC Index + 0Bh)	I/O space (RTC Index + 0Bh)	5	X
Alarm Flag (AF)	Register C (Flag Register): RTC_REGC	I/O space (RTC Index + 0Ch)	5	X
SWSMI_RATE_SEL	General PM Configuration 3 Register: GEN_PMCON_3	D31:F0:A4h	7:6	0
SLP_S4# Minimum Assertion Width	General PM Configuration 3 Register: GEN_PMCON_3	D31:F0:A4h	5:4	0
SLP_S4# Assertion Stretch Enable	General PM Configuration 3 Register: GEN_PMCON_3	D31:F0:A4h	3	0
RTC Power Status (RTC_PWR_STS)	General PM Configuration 3 Register: GEN_PMCON_3	D31:F0:A4h	2	0
Power Failure (PWR_FLR)	General PM Configuration 3 Register: (GEN_PMCON_3)	D31:F0:A4h	1	0
AFTERG3_EN	General PM Configuration 3 Register: GEN_PMCON_3	D31:F0:A4h	0	0
Power Button Override Status (PRBTNOR_STS)	Power Management 1Status Register: PM1_STS	PMBase + 00h	11	0
RTC Event Enable (RTC_EN)	Power Management 1Enable Register: PM1_EN	PMBase + 02h	10	
Sleep Type (SLP_TYP)	Power Management 1 Control: PM1_CNT	PMBase + 04h	12:10	0

Table 5-39. Configuration Bits Reset by RTCRST# Assertion (Sheet 2 of 2)

Bit Name	Register	Location	Bit(s)	Default State
PME_EN	General Purpose Event 0 Enables Register (GPE0_EN)	PMBase + 2Ch	11	0
BATLOW_EN	General Purpose Event 0 Enables Register (GPE0_EN)	PMBase + 2Ch	10	
RI_EN	General Purpose Event 0 Enables Register (GPE0_EN)	PMBase + 2Ch	8	0
NEW_CENTURY_STS	TCO1 Status Register (TCO1_STS)	TCOBase + 04h	7	0
INTRD_DET	TCO2 Status Register (TCO2_STS)	TCOBase + 06h	0	0
Top Swap (TS)	Backed Up Control Register (BUC)	Chipset Config Registers:Offset 3414h	0	X

Using a GPI to Clear CMOS

A jumper on a GPI can also be used to clear CMOS values. BIOS would detect the setting of this GPI on system boot-up, and manually clear the CMOS array.

Note: The GPI strap technique to clear CMOS requires multiple steps to implement. The system is booted with the jumper in new position, then powered back down. The jumper is replaced back to the normal position, then the system is rebooted again. The RTCRST# jumper technique allows the jumper to be moved and then replaced, all while the system is powered off. Then, once booted, the RTC_PWR_STS can be detected in the set state.

Warning: Clearing CMOS, using a jumper on VccRTC, must **not** be implemented.

5.14 Processor Interface (D31:F0)

The Intel® 631xESB/632xESB I/O Controller Hub interfaces to the processor with a variety of signals

- Standard Outputs to processor: A20M#, SMI#, NMI, INIT#, INTR, STPCLK#, IGNNE#, CPUSLP#, CPUPWRGD
- Standard Input from processor: FERR#

Most Intel® 631xESB/632xESB I/O Controller Hub outputs to the processor use CMOS open drain buffers. The Intel® 631xESB/632xESB I/O Controller Hub has separate V_{CPU_IO} signals that are pulled up at the system level to the processor voltage, and thus determines VOH for the outputs to the processor.

The Intel® 631xESB/632xESB I/O Controller Hub contains one input from the CPU, FERR#. The Vil threshold needs to be compatible with CPUs that might drive FERR# to no higher than 1.3 V± 5%.

5.14.1 Processor Interface Signals

This section describes each of the signals that interface between the Intel® 631xESB/632xESB I/O Controller Hub and the processor(s). Note that the behavior of some signals may vary during processor reset, as the signals are used for frequency strapping.

5.14.1.1 A20M# (Mask A20)

The A20M# signal is active (low) when both of the following conditions are true:

- The ALT_A20_GATE bit (Bit 1 of PORT92 register) is a 0.
- The A20GATE input signal is a 0.

The A20GATE input signal is expected to be generated by the external microcontroller (KBC).

5.14.1.2 INIT# (Initialization)

The INIT# signal is active (driven low) based on any one of several events described in Table 5-40. When any of these events occur, INIT# is driven low for 16 PCI clocks, then driven high.

Note: The 16-clock counter for INIT# assertion halts while STPCLK# is active. Therefore, if INIT# is supposed to go active while STPCLK# is asserted, it actually goes active after STPCLK# goes inactive.

This section refers to INIT#, but applies to two signals: INIT# and INIT3_3V#, as INIT3_3V# is functionally identical to INIT#, but signaling at 3.3V.

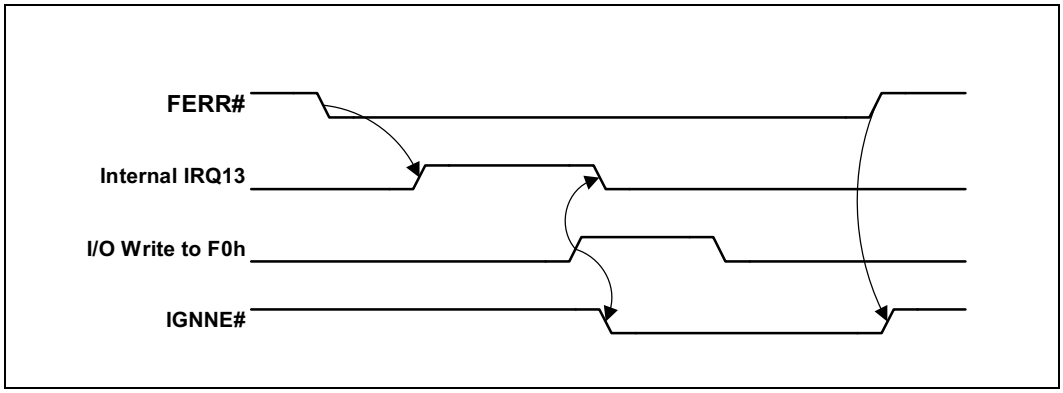
Table 5-40. INIT# Going Active

Cause of INIT# Going Active	Comment
Shutdown special cycle from processor.	
PORT92 write, where INIT_NOW (bit 0) transitions from a 0 to a 1.	
PORTCF9 write, where SYS_RST (bit 1) was a 0 and RST_CPU (bit 2) transitions from 0 to 1.	
RCIN# input signal goes low. RCIN# is expected to be driven by the external microcontroller (KBC).	0 to 1 transition on RCIN# must occur before the Intel® 631xESB/632xESB I/O Controller Hub will arm INIT# to be generated again. ***Note:*** RCIN# signal is expected to be high during $S3_{HOT}$ and low during $S3_{COLD}$, S4, and S5 states. Transition on the RCIN# signal in those states (or the transition to those states) may not necessarily cause the INIT# signal to be generated to the processor.
CPU BIST	To enter BIST, software sets CPU_BIST_EN bit and then does a full processor reset using the CF9 register.

5.14.1.3 FERR# / IGNNE# (Numeric Coprocessor Error / Ignore Numeric Error)

The Intel® 631xESB/632xESB I/O Controller Hub supports the coprocessor error function with the FERR#/IGNNE# pins. The function is enabled by way of the COPROC_ERR_EN bit (Chipset Config Registers:Offset 31FFh:bit 1). FERR# is tied directly to the Coprocessor Error signal of the processor. If FERR# is driven active by the processor, IRQ13 goes active (internally). When it detects a write to COPROC_ERR (I/O Register F0h), the Intel® 631xESB/632xESB I/O Controller Hub negates the internal IRQ13 and drives IGNNE# active. IGNNE# remains active until FERR# is driven inactive. IGNNE# is never driven active unless FERR# is active.

Figure 5-17. Coprocessor Error Timing Diagram



If COPROC_ERR_EN is not set, the assertion of FERR# will have not generate an internal IRQ13, nor will the write to F0h generate IGNNE#.

5.14.1.4 NMI (Non-Maskable Interrupt)

Non-Maskable Interrupts (NMIs) can be generated by several sources, as described in Table 5-41.

Table 5-41. NMI Sources

Cause of NMI	Comment
SERR# goes active (either internally, externally via SERR# signal, or via message from MCH)	Can instead be routed to generate an SCI, through the NMI2SCI_EN bit (Device 31:Function 0, TCO Base + 08h, bit 11).
IOCHK# goes active via SERIRQ# stream (ISA system Error)	Can instead be routed to generate an SCI, through the NMI2SCI_EN bit (Device 31:Function 0, TCO Base + 08h, bit 11).

5.14.1.5 Stop Clock Request and CPU Sleep (STPCLK# and CPUSLP#)

The Intel® 631xESB/632xESB I/O Controller Hub power management logic controls these active-low signals. Refer to Section 5.15 for more information on the functionality of these signals.

5.14.1.6 CPU Power Good (CPUPWRGD)

This signal is connected to the processor's PWRGOOD input. This is an open-drain output signal (external pull-up resistor required) that represents a logical AND of the Intel® 631xESB/632xESB I/O Controller Hub's PWROK and VRMPWRGD signals.

5.14.2 Dual-Processor Issues

5.14.2.1 Signal Differences

In dual-processor designs, some of the processor signals are unused or used differently than for uniprocessor designs.

Table 5-42. DP Signal Differences

Signal	Difference
A20M# / A20GATE	Generally not used, but still supported by the Intel® 631xESB/632xESB I/O Controller Hub.
STPCLK#	Used for S1 State as well as preparation for entry to S3–S5 Also allows for THERM# based throttling (not via ACPI control methods). Should be connected to both processors.
FERR# / IGNNE#	Generally not used, but still supported by Intel® 631xESB/632xESB I/O Controller Hub.

5.14.2.2 Power Management

For multiple-CPU (or multiple-core) configurations in which more than one Stop Grant cycle may be generated, the MCH is expected to count Stop Grant cycles and only pass the last one through to the Intel® 631xESB/632xESB I/O Controller Hub. This prevents the Intel® 631xESB/632xESB I/O Controller Hub from getting out of sync with the processor on multiple STPCLK# assertions.

Because the S1 state will have the STPCLK# signal active, the STPCLK# signal can be connected to both processors. However, for ACPI implementations, the BIOS must indicate that the Intel® 631xESB/632xESB I/O Controller Hub supports the C1 state for only dual-processor designs.

In going to the S1 state, multiple Stop-Grant cycles will be generated by the CPUs. The Intel® 631xESB/632xESB I/O Controller Hub also has the option to assert the CPU's SLP# signal (CPUSLP#). It is assumed that prior to setting the SLP_EN bit (which causes the transition to the S1 state), the CPUs will not be executing code that is likely to delay the Stop-Grant cycles.

In going to the S3, S4, or S5 states, the system will appear to pass through the S1 state; thus, STPCLK# and SLP# are also used. During the S3, S4, and S5 states, both processors will lose power. Upon exit from those states, the processors will have their power restored.

5.15 Power Management (D31:F0)

5.15.1 Features

- Support for *Advanced Configuration and Power Interface, Version 2.0* (ACPI) providing power and thermal management
  - — ACPI 24-Bit Timer
  - — Software initiated throttling of processor performance for Thermal and Power Reduction
  - — Hardware Override to throttle processor performance if system too hot
  - — SCI and SMI# Generation
- PCI PME# signal for Wake Up from Low-Power states

- PCI Express WAKE# signal for Wake from Low-Power states
- SYS_Reset# input to eliminate external glue logic
- System Sleep State Control
  - — ACPI S1 state: Stop Grant (using STPCLK# signal) halts processor's instruction stream (only STPCLK# active, and CPUSLP# optional)
  - — ACPI S3 state – Suspend to RAM (STR)
  - — ACPI S4 state – Suspend-to-Disk (STD)
  - — ACPI G2/S5 state – Soft Off (SOFF)
  - — Power Failure Detection and Recovery
- Support for Intel Itanium architecture processors

Note: For IA-32 desktop systems, and systems with Intel Itanium architecture processors, the Intel® 631xESB/632xESB I/O Controller Hub does not support the C2 states. ACPI throttling is not directly supported for any platform that has more than one logical processor. Software can be used to coordinate throttling requirements among several logical processors.

5.15.2 Intel® 631xESB/632xESB I/O Controller Hub and System Power States

Table 5-43 shows the power states defined for Intel® 631xESB/632xESB I/O Controller Hub-based platforms. The state names generally match the corresponding ACPI states.

Table 5-43. General Power States for Systems Using Intel® 631xESB/632xESB I/O Controller Hub (Sheet 1 of 2)

State/ Substates	Legacy Name / Description
G0/S0/C0	**Full On:** Processor operating. Individual devices may be shut down to save power. The different processor operating levels are defined by Cx states, as shown in Table 5-44. Within the C0 state, the Intel® 631xESB/632xESB I/O Controller Hub can throttle the processor using the STPCLK# signal to reduce power consumption. The throttling can be initiated by software or by the operating system or BIOS.
G0/S0/C1	**Auto-Halt:** Processor has executed an AutoHalt instruction and is not executing code. The processor snoops the bus and maintains cache coherency.
G0/S0/C2	**Stop-Grant:** The STPCLK# signal goes active to the processor. The processor performs a Stop-Grant cycle, halts its instruction stream, and remains in that state until the STPCLK# signal goes inactive. In the Stop-Grant state, the processor snoops the bus and maintains cache coherency. ***Note:*** This state is not supported for IA-64 processors. They should instead use C1.
G0/S0/C3	**Stop-Clock:** This is only for mobile systems. The STPCLK# signal goes active to the processor. The processor performs a Stop-Grant cycle, halts its instruction stream. then asserts SLP#, then DPSLP#, followed by STP_CPU#, which forces the clock generator to stop the processor clock. This is also used for Intel SpeedStep technology support. Accesses to memory (by AGP, PCI, or internal units) is not permitted while in a C3 state, except the new non-snoop cycles associated with PCI Express. It is assumed that the ARB_DIS bit is set by software prior to entering C3 state, even if the hardware ignores the ARB_DIS bit.
G0/S0/C4	**Stop-Clock with lower processor voltage.** This closely resembles the G0/S0/C3 state. However, after the has asserted STP_CPU#, it then lowers the voltage to the processor by asserting DPRSLPVR. This reduces processor leakage. Prior to exiting the C4 state, the deasserts DPRSLPVR, which increases the voltage to the processor. The Yonah processor enhances C4 (i.e., C4E), but requires the DPRSTP# pin.
G1/S1	**Stop-Grant:** Similar to G0/S0/C2 state. The Intel® 631xESB/632xESB I/O Controller Hub also has the option to assert the CPUSLP# signal to further reduce processor power consumption. ***Note:*** The behavior for this state is slightly different when supporting IA-64 processors. The platform will generally use 10s of Watts during this state. ***Note:*** May be too high for meeting Energy Star requirements for some platforms. ***Note:*** This was previously known as S1-D, but was renamed due to deletion of S1-M.

Table 5-43. General Power States for Systems Using Intel® 631xESB/632xESB I/O Controller Hub (Sheet 2 of 2)

State/ Substates	Legacy Name / Description
G1/S3	**Suspend-To-RAM (STR):** The system context is maintained in system DRAM, but power is shut off to non-critical circuits. Memory is retained, and refreshes continue. All clocks stop except RTC clock. ***Note:*** There are two flavors of S3: S3-Hot and S3-Cold. S3-Hot uses SLP_S4# to kill system power rather than SLP_S3#. It requires fewer FETs, has more power planes to be on during S3 and results in a less expensive platform. There are no differences from the Intel® 631xESB/632xESB I/O Controller Hub perspective.
G1/S4	**Suspend-To-Disk (STD):** The context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume.
G2/S5	**Soft Off (SOFF):** System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.
G3	**Mechanical OFF (MOFF):** System context not maintained. All power is shut off except for the RTC. No "Wake" events are possible, because the system does not have any power. This state occurs if the user turns off a mechanical switch or if the system power supply is at a level that is insufficient to power the "waking" logic. When system power returns, transition will depends on the state just prior to the entry to G3 and the AFTERG3 bit in the GEN_PMCON3 register (D31:F0, offset A4). Refer to Table 5-50 for more details.

Note: The above table is for informational purposes, and should not be used by designers or validators as part of the behavioral description.

Table 5-44 shows the transitions rules among the various states.

Note: Transitions among the various states may appear to temporarily transition through intermediate states. For example, in going from S0 to S1, it may appear to pass through the G0/S0/C2 states. These intermediate transitions and states are not listed in the table.

Table 5-44. State Transition Rules for Intel® 631xESB/632xESB I/O Controller Hub

Present State	Transition Trigger	Next State
G0/S0/C0	• Processor halt instruction • Level 2 Read • SLP_EN bit set • Power Button Override • Mechanical Off/Power Failure	• G0/S0/C1 • G0/S0/C2 • G1/Sx or G2/S5 state • G2/S5 • G3
G0/S0/C1	• Any Enabled Break Event • STPCLK# goes active • Power Button Override • Power Failure	• G0/S0/C0 • G0/S0 • G2/S5 • G3
G0/S0/C2	• Any Enabled Break Event • Power Button Override • Resume Well Power Failure	• G0/S0/C0 • G2/S5 • G3
G1/S1, G1/S3, or G1/S4	• Any Enabled Wake Event • Power Button Override • Power Failure	• G0/S0/C0 • G2/S5 • G3
G2/S5	• Any Enabled Wake Event • Power Failure	• G0/S0/C0 • G3
G3	• Power Returns	• Optional to go to S0/C0 (reboot) or G2/S5 (stay off until power button pressed or other wake event). (See Note 1)

Note: Some wake events can be preserved through power failure.

5.15.3 System Power Planes

The system has several independent power planes, as described in Table 5-45. Note that when a particular power plane is shut off, it should go to a 0 V level.

Table 5-45. System Power Plane

Plane	Controlled By	Description
CPU	SLP_S3# signal	The SLP_S3# signal can be used to cut the power to the processor completely.
MAIN	SLP_S3# or SLP_S4# signal	S3-Cold: When SLP_S3# goes active, power can be shut off to any circuit not required to wake the system from the S3 state. Since the S3 state requires that the memory context be preserved, power must be retained to the main memory. Devices on the PCI bus, LPC Interface, ESI and PCI Express will typically be shut off when the Main power plane is shut, although there may have small subsections powered. S3-Hot: SLP_S4# is used to cut the main power well, rather than using SLP_S3#. This impacts the board design, but there is no specific Intel® 631xESB/632xESB I/O Controller Hub bit or strap needed to indicate which option is selected.
DEVICES and MEMORY	SLP_S4# signal SLP_S5# signal	When the SLP_S4# goes active, power can be shut off to any circuit not required to wake the system from the S4. Since the memory context does not need to be preserved in the S4 state, the power to the memory can also be shut down. When SLP_S5# goes active, power can be shut to any circuit not required to wake the system from the S5 state. Since the memory context does not need to be preserved in the S5 state, the power to the memory can also be shut.
DEVICE[n]	GPIO	Individual subsystems may have their own power plane. For example, GPIO signals may be used to control the power to disk drives, audio amplifiers, or the display screen.

5.15.4 SMI#/SCI Generation

Upon any SMI# event taking place, Intel® 631xESB/632xESB I/O Controller Hub asserts SMI# to the processor, which causes it to enter SMM space. SMI# remains active until the EOS bit is set. When the EOS bit is set, SMI# goes inactive for a minimum of 4 PCICLK. If another SMI event occurs, SMI# is driven active again.

The SCI is a level-mode interrupt that is typically handled by an ACPI-aware operating system. In non-APIC systems (which is the default), the SCI IRQ is routed to one of the 8259 interrupts (IRQ 9, 10, or 11). The 8259 interrupt controller must be programmed to level mode for that interrupt.

In systems using the APIC, the SCI can be routed to interrupts 9, 10, 11, 20, 21, 22, or 23. The interrupt polarity changes depending on whether it is on an interrupt shareable with a PIRQ or not (see Section 21.1.13). The interrupt remains asserted until all SCI sources are removed.

Table 5-46 shows which events can cause an SMI# and SCI. Note that some events can be programmed to cause either an SMI# or SCI. The usage of the event for SCI (instead of SMI#) is typically associated with an ACPI-based system. Each SMI# or SCI source has a corresponding enable and status bit.

Table 5-46. Causes of SMI# and SCI (Sheet 1 of 2)

Cause	SCI	SMI	Additional Enables	Where Reported
PME#	Yes	Yes	PME_EN=1	PME_STS
PME_B0 (internal EHCI controller)	Yes	Yes	PME_B0_EN=1	PME_B0_STS
SATA SCI	Yes	No	SATA_SCI_EN = 1	SATA_SCI_STS bit
PCI Express PME Messages	Yes	Yes	PCI_EXP_EN=1 (Not enabled for SMI)	PCI_EXP_STS
PCI Express Hot-Plug Message	Yes	Yes	HOT_PLUG_EN=1 (Not enabled for SMI)	HOT_PLUG_STS
Power Button Press	Yes	Yes	PWRBTN_EN=1	PWRBTN_STS
RTC Alarm	Yes	Yes	RTC_EN=1	RTC_STS
Ring Indicate	Yes	Yes	RI_EN=1	RI_STS
AC'97 wakes	Yes	Yes	AC97_EN=1	AC97_STS
USB#1 wakes	Yes	Yes	USB1_EN=1	USB1_STS
USB#2 wakes	Yes	Yes	USB2_EN=1	USB2_STS
USB#3 wakes	Yes	Yes	USB3_EN=1	USB3_STS
USB#4 wakes	Yes	Yes	USB4_EN=1	USB4_STS
THRM# pin active	Yes	Yes	THRM_EN=1	THRM_STS
ACPI Timer overflow (2.34 sec.)	Yes	Yes	TMROF_EN=1	TMROF_STS
Any GPI	Yes	Yes	GPIO[x]_Route=10 (SCI) GPIO[x]_Route=01 (SMI) GPE0[x]_EN=1	GPIO[x]_STS GPE0_STS
TCO SCI Logic	Yes	No	TCOSCI_EN=1	TCOSCI_STS
TCO SCI message from MCH	Yes	No	none	MCHSCI_STS
TCO SMI Logic	No	Yes	TCO_EN=1	TCO_STS
TCO SMI – Year 2000 Rollover	No	Yes	none	NEWCENTURY_STS
TCO SMI – TCO TIMEROUT	No	Yes	none	TIMEOUT
TCO SMI – OS writes to TCO_DAT_IN register	No	Yes	none	OS_TCO_SMI
TCO SMI – Message from MCH	No	Yes	none	MCHSMI_STS
TCO SMI – NMI occurred (and NMIs mapped to SMI)	No	Yes	NMI2SMI_EN=1	NMI2SMI_STS
TCO SMI – INTRUDER# signal goes active	No	Yes	INTRD_SEL=10	INTRD_DET
TCO SMI – Change of the BIOSWP bit from 0 to 1	No	Yes	BLD=1	BIOSWR_STS
TCO SMI – Write attempted to BIOS	No	Yes	BIOSWP=1	BIOSWR_STS
BIOS_RLS written to	Yes	No	GBL_EN=1	GBL_STS
GBL_RLS written to	No	Yes	BIOS_EN=1	BIOS_STS
Periodic timer expires	No	Yes	PERIODIC_EN=1	PERIODIC_STS
64 ms timer expires	No	Yes	SWSMI_TMR_EN=1	SWSMI_TMR_STS
Enhanced USB Legacy Support Event	No	Yes	LEGACY_USB2_EN = 1	LEGACY_USB2_STS
Enhanced USB Intel Specific Event	No	Yes	INTEL_USB2_EN = 1	INTEL_USB2_STS
UHCI USB Legacy logic	No	Yes	LEGACY_USB_EN=1	LEGACY_USB_STS
Serial IRQ SMI reported	No	Yes	none	SERIRQ_SMI_STS

Table 5-46. Causes of SMI# and SCI (Sheet 2 of 2)

Cause	SCI	SMI	Additional Enables	Where Reported
Device monitors match address in its range	No	Yes	none	DEVMON_STS, DEVACT_STS
SMBus Host Controller	No	Yes	SMB_SMI_EN Host Controller Enabled	SMBus host status reg.
SMBus Slave SMI message	No	Yes	none	SMBUS_SMI_STS
SMBus SMBALERT# signal active	No	Yes	none	SMBUS_SMI_STS
SMBus Host Notify message received	No	Yes	HOST_NOTIFY_INTREN	SMBUS_SMI_STS HOST_NOTIFY_STS
Access microcontroller 62h/66h	No	Yes	MCSMI_EN	MCSMI_STS
SLP_EN bit written to 1	No	Yes	SMI_ON_SLP_EN=1	SMI_ON_SLP_EN_STS

Notes:
1. SCI_EN must be 1 to enable SCI. SCI_EN must be 0 to enable SMI.
2. SCI can be routed to cause interrupt 9:11 or 20:23 (20:23 available only in APIC mode).
3. GBL_SMI_EN must be 1 to enable SMI.
4. EOS must be written to 1 to re-enable SMI for the next 1.

5.15.4.1 SATA SCI

SATA can cause an SCI, but not an SMI or wake event. when SATA causes an SCI, the SATA_SCI_STS bit will be set.

5.15.4.2 PCI Express* SCI

The Intel® 631xESB/632xESB I/O Controller Hub's PCI Express Root and Downstream ports and the MCH (by way of ESI) have the ability to cause PME using messages. When a PME message is received, Intel® 631xESB/632xESB I/O Controller Hub will set the PCI_EXP_STS bit. If the PCI_EXP_EN bit is also set, the Intel® 631xESB/632xESB I/O Controller Hub can cause an SCI by way of the GPE1_STS register.

5.15.4.3 PCI Express* Hot-Plug

PCI Express has a Hot-Plug mechanism and is capable of generating a SCI by way of the GPE1 register. It is also capable of generating an SMI. However, it is not capable of generating a wake event.

5.15.5 Dynamic Processor Clock Control

The Intel® 631xESB/632xESB I/O Controller Hub has primary control for dynamically starting and stopping system clocks. The clock control is used for transitions among the various S0/Cx states, and processor throttling. Each dynamic clock control method is described in this section. The various sleep states may also perform types of non-dynamic clock control.

The Intel® 631xESB/632xESB I/O Controller Hub supports the ACPI C0 and C1 states.

The Dynamic Processor Clock control is handled using the following signals:

- STPCLK#: Used to halt processor instruction stream.

The C1 state is entered based on the processor performing an auto halt instruction.

A C1 state ends due to a Break event. Based on the break event, the Intel® 631xESB/632xESB I/O Controller Hub returns the system to C0 state.

5.15.5.1 Transition Rules among S0/Cx and Throttling States

The following priority rules and assumptions apply among the various S0/Cx and throttling states:

- Entry to any S0/Cx state is mutually exclusive with entry to any S1–S5 state. This is because the processor can perform only one register access at a time and Sleep states have higher priority than thermal throttling.
- When the SLP_EN bit is set (system going to a S1 - S5 sleep state), the THTL_EN and FORCE_THTL bits can be internally treated as being disabled (no throttling while entering sleep state).
- The Host controller must post Stop-Grant cycles in such a way that the processor gets an indication of the end of the special cycle prior to the Intel® 631xESB/ 632xESB I/O Controller Hub observing the Stop-Grant cycle. This ensures that the STPCLK# signals stays active for a sufficient period after the processor observes the response phase.

5.15.6 Sleep States

5.15.6.1 Sleep State Overview

The Intel® 631xESB/632xESB I/O Controller Hub directly supports different sleep states (S1–S5), which are entered by setting the SLP_EN bit, or due to a Power Button press. The entry to the Sleep states are based on several assumptions:

- Entry to a Cx state is mutually exclusive with entry to a Sleep state. This is because the processor can perform only one register access at a time. A request to Sleep always has higher priority than throttling.
- Prior to setting the SLP_EN bit, the software turns off processor-controlled throttling. Note that thermal throttling cannot be disabled, but setting the SLP_EN bit disables thermal throttling (since S1–S5 sleep state has higher priority).
- The G3 state cannot be entered by way of any software mechanism. The G3 state indicates complete power loss.

5.15.6.2 Initiating Sleep State

Sleep states (S1–S5) are initiated by:

- Masking interrupts, turning off all Bus Master enable bits, setting the desired type in the SLP_TYP field, and then setting the SLP_EN bit. The hardware then attempts to gracefully put the system into the corresponding Sleep state.
- Pressing the PWRBTN# Signal for more than 4 seconds to cause a Power Button Override event. In this case the transition to the S5 state is less graceful, since there are no dependencies on observing Stop-Grant cycles from the processor or on clocks other than the RTC clock.

Table 5-47. Sleep Types

Sleep Type	Comment
S1	Intel® 631xESB/632xESB I/O Controller Hub asserts the STPCLK# signal. It also has the option to assert CPUSLP# signal. This lowers the processor's power consumption. No snooping is possible in this state.
S3	Intel® 631xESB/632xESB I/O Controller Hub asserts SLP_S3#. The SLP_S3# signal controls the power to non-critical circuits. Power is retained only to devices needed to wake from this sleeping state, as well as to the memory.
S4	Intel® 631xESB/632xESB I/O Controller Hub asserts SLP_S3# and SLP_S4#. The SLP_S4# signal shuts off the power to the memory subsystem. Only devices needed to wake from this state should be powered.
S5	Same power state as S4. Intel® 631xESB/632xESB I/O Controller Hub asserts SLP_S3#, SLP_S4# and SLP_S5#.

5.15.6.3 Exiting Sleep States

Sleep states (S1–S5) are exited based on Wake events. The Wake events forces the system to a full on state (S0), although some non-critical subsystems might still be shut off and have to be brought back manually. For example, the hard disk may be shut off during a sleep state, and have to be enabled by way of a GPIO pin before it can be used.

Upon exit from the Intel® 631xESB/632xESB I/O Controller Hub-controlled Sleep states, the WAK_STS bit is set. The possible causes of Wake Events (and their restrictions) are shown in Table 5-48.

Table 5-48. Causes of Wake Events

Cause	States Can Wake From	How Enabled
RTC Alarm	S1—S5 (Note 1)	Set RTC_EN bit in PM1_EN register
Power Button	S1—S5	Always enabled as Wake event
GPIO[0:n]	S1–S5 (Note 1)	GPE0_EN register Note: GPIs that are in the core well are not capable of waking the system from sleep states where the core well is not powered.
Classic USB	S1–S5	Set USB1_EN, USB 2_EN, USB3_EN, and USB4_EN bits in GPE0_EN register
RI#	S1–S5 (Note 1)	Set RI_EN bit in GPE0_EN register
AC'97 / Intel High Definition Audio	S1–S5	Set AC97_EN bit in GPE0_EN register
Primary PME#	S1–S5 (Note 1)	PME_B0_EN bit in GPE0_EN register
Secondary PME#	S1–S5	Set PME_EN bit in GPE0_EN register.
PCI_EXP_WAKE#	S1–S5	PCI_EXP_WAKE bit
PCI_EXP PME Message	S1	Must use the PCI Express WAKE# pin rather than messages for wake from S3,S4, or S5.
SMBALERT#	S1—S5	Always enabled as Wake event
SMBus Slave Message	S1—S5	Wake/SMI# command always enabled as a Wake event. Note: SMBus Slave Message can wake the system from S1–S5, as well as from S5 due to Power Button Override.
SMBus Host Notify message received	S1—S5	HOST_NOTIFY_WKEN bit SMBus Slave Command register. Reported in the SMB_WAK_STS bit in the GPEO_STS register.

Notes:
1. This is a wake event from S5 only if the sleep state was entered by setting the SLP_EN and SLP_TYP bits by way of software, or if there is a power failure.
2. If in the S5 state due to a powerbutton override or THRMTRIP#, the possible wake events are due to Power Button, Hard Reset Without Cycling (See Command Type 3 in Table 5-71), and Hard Reset System (See Command Type 4 in Table 5-71).

It is important to understand that the various GPIs have different levels of functionality when used as wake events. The GPIs that reside in the core power well can generate wake events from sleep states only where the core well is powered. Also, only certain GPIs are “ACPI Compliant,” meaning that their Status and Enable bits reside in ACPI I/O space. Table 5-49 summarizes the use of GPIs as wake events.

Table 5-49. GPI Wake Events

GPI	Power Well	Wake From	Notes
GPIO[7:0]	Core	S1	
GPIO[15:14, 11:8]	Resume	S1–S5	ACPI Compliant

The latency to exit the various Sleep states varies greatly and is heavily dependent on power supply design, so much so that the exit latencies due to the Intel® 631xESB/632xESB I/O Controller Hub are insignificant.

5.15.6.4 PCI Express* WAKE# Signal and PME Event Message

PCI Express Root and Downstream ports can wake the platform from any sleep state (S1, S3, S4, or S5) using the WAKE# pin. WAKE# is treated as a wake event, but does not cause any bits to go active in the GPE_STS register.

PCI Express ports and the MCH (by way of ESI) have the ability to cause PME using messages. When a PME message is received, Intel® 631xESB/632xESB I/O Controller Hub will set the PCI_EXP_STS bits.

5.15.6.5 Sx-G3-Sx, Handling Power Failures

In server systems, power failures can occur if the AC power is cut (a real power failure) or if the system is unplugged. In either case, PWROK and RSMRST# are assumed to go low.

Depending on when the power failure occurs and how the system is designed, different transitions could occur due to a power failure.

The AFTER_G3 bit provides the ability to program whether or not the system should boot once power returns after a power loss event. If the policy is to not boot, the system remains in an S5 state (unless previously in S4). There are only three possible events that will wake the system after a power failure.

1. **PWRBTN#:** PWRBTN# is always enabled as a wake event. When RSMRST# is low (G3 state), the PWRBTN_STS bit is reset. When the Intel® 631xESB/632xESB I/O Controller Hub exits G3 after power returns (RSMRST# goes high), the PWRBTN# signal is already high (because V_{CC}-standby goes high before RSMRST# goes high) and the PWRBTN_STS bit is 0.
2. **RI#:** RI# does not have an internal pull-up. Therefore, if this signal is enabled as a wake event, it is important to keep this signal powered during the power loss event. If this signal goes low (active), when power returns the RI_STS bit is set and the system interprets that as a wake event.
3. **RTC Alarm:** The RTC_EN bit is in the RTC well and is preserved after a power loss. Like PWRBTN_STS the RTC_STS bit is cleared when RSMRST# goes low.

The Intel® 631xESB/632xESB I/O Controller Hub monitors both PWROK and RSMRST# to detect for power failures. If PWROK goes low, the PWROK_FLR bit is set. If RSMRST# goes low, PWR_FLR is set.

Note: Although PME_EN is in the RTC well, this signal cannot wake the system after a power loss. PME_EN is cleared by RTCRST#, and PME_STS is cleared by RSMRST#.

Table 5-50. Transitions Due to Power Failure

State at Power Failure	AFTERG3_EN bit	Transition When Power Returns
S0, S1, S3	1 0	S5 S0
S4	1 0	S4 S0
S5	1 0	S5 S0

5.15.7 Thermal Management

The Intel® 631xESB/632xESB I/O Controller Hub has several mechanisms to assist with managing thermal problems in the system.

Note: Thermal Management based on throttling is not supported when the Intel® 631xESB/632xESB I/O Controller Hub is used with Itanium architecture-based processors.

5.15.7.1 THRM# Signal

The THRM# signal is used as a status input for a thermal sensor. The sensor could be inside the processor or in a separate component near the processor. The Intel® 631xESB/632xESB I/O Controller Hub follows these behaviors with regard to the THRM# signal:

1. Based on the THRM# signal going active, the Intel® 631xESB/632xESB I/O Controller Hub generates an SMI# or SCI (depending on SCI_EN).
2. If the THRM_POL bit is set low, when the THRM# signal goes low, the THRM_STS bit will be set. This is an indicator that the thermal threshold has been exceeded. If the THRM_EN bit is set, then when THRM_STS goes active, either an SMI# or SCI will be generated (depending on the SCI_EN bit being set). The power management software (BIOS or ACPI) can then take measures to start reducing the temperature. Examples include shutting off unwanted subsystems, or halting the processor.
3. By setting the THRM_POL bit to high, another SMI# or SCI can optionally be generated when the THRM# signal goes back high. This allows the software (BIOS or ACPI) to turn off the cooling methods.

Note: THRM# assertion does not cause a TCO event message in S3 or S4. The level of the signal is not reported in the heartbeat message.

5.15.7.2 Processor Initiated Passive Cooling

This is a method to cool the system by throttling the processor. The mode is initiated by software setting the THTL_EN or THTL_DTY bits.

Behavioral Description:

1. Software sets the THTL_DTY bits to select throttle ratio and THTL_EN bit to enable the throttling.
2. Throttling results in STPCLK# active for a minimum time of 12.5% and a maximum of 87.5%. The period is 1024 PCI clocks. Thus, the STPCLK# signal can be active for as little as 128 PCI clocks or as much as 896 PCI clocks. The actual slowdown (and cooling) of the processor depends on the instruction stream, because the

processor is allowed to finish the current instruction. Furthermore, the Intel® 631xESB/632xESB I/O Controller Hub waits for the STOP-GRANT cycle before starting the count of the time the STPCLK# signal is active.

3. Intel® 631xESB/632xESB I/O Controller Hub will perform the Go-C2/Ack-C2 and Go-C0/Ack-C0 messages for throttling, just as if it were making transitions to/from a C2 state.

5.15.7.3 THRM# Override Software Bit

The FORCE_THTL bit allows the BIOS to force passive cooling, independent of the ACPI software (which uses the THTL_EN and THTL_DTY bits). If this bit is set, the Intel® 631xESB/632xESB I/O Controller Hub starts throttling using the ratio in the THRM_DTY field.

When this bit is cleared the Intel® 631xESB/632xESB I/O Controller Hub stops throttling, unless the THTL_EN bit is set (indicating that ACPI software is attempting throttling).

If both the THTL_EN and FORCE_THTL bits are set, then the Intel® 631xESB/632xESB I/O Controller Hub should use the duty cycle defined by the THRM_DTY field, not the THTL_DTY field.

5.15.7.4 Active Cooling

Active cooling involves fans. The GPIO signals from the Intel® 631xESB/632xESB I/O Controller Hub can be used to turn on/off a fan.

5.15.8 Event Input Signals and Their Usage

The Intel® 631xESB/632xESB I/O Controller Hub has various input signals that trigger specific events. This section describes those signals and how they should be used.

5.15.8.1 PWRBTN# (Power Button)

The Intel® 631xESB/632xESB I/O Controller Hub PWRBTN# signal operates as a “Fixed Power Button” as described in the *Advanced Configuration and Power Interface, Version 2.0b.* PWRBTN# signal has a 16 ms de-bounce on the input. The state transition descriptions are included in Table 5-51. Note that the transitions start as soon as the PWRBTN# is pressed (but after the debounce logic), and does not depend on when the Power Button is released.

Note: During the time that the SLP_S4# signal is stretched for the minimum assertion width (if enabled), the Power Button is not a wake event. Refer to Power Button Override Function section below for further detail.

Table 5-51. Transitions Due to Power Button

Present State	Event	Transition / Action	Comment
S0/Cx	PWRBTN# goes low.	SMI# or SCI generated (depending on SCI_EN).	Software typically initiates a Sleep state.
S1–S5	PWRBTN# goes low.	Wake Event. Transitions to S0 state.	Standard wakeup.
G3	PWRBTN# pressed.	None.	No effect since no power. Not latched nor detected.
S0–S4	PWRBTN# held low for at least 4 consecutive seconds.	Unconditional transition to S5 state.	No dependence on processor (for example, Stop-Grant cycles) or any other subsystem.

5.15.8.1.1 Power Button Override Function

If PWRBTN# is observed active for at least four consecutive seconds, the state machine should unconditionally transition to the G2/S5 state, regardless of present state (S0–S4), even if PWROK is not active. In this case, the transition to the G2/S5 state should not depend on any particular response from the processor (for example, a Stop-Grant cycle), nor any similar dependency from any other subsystem.

The PWRBTN# status is readable to check if the button is currently being pressed or has been released. The status is taken after the de-bounce, and is readable by way of the PWRBTN_LVL bit.

Note: The 4-second PWRBTN# assertion should only be used if a system lock-up has occurred. The 4-second timer starts counting when the Intel® 631xESB/632xESB I/O Controller Hub is in a S0 state. If the PWRBTN# signal is asserted and held active when the system is in a suspend state (S1–S5), the assertion causes a wake event. Once the system has resumed to the S0 state, the 4-second timer starts.

Note: During the time that the SLP_S4# signal is stretched for the minimum assertion width (if enabled by D31:F0:A4h bit 3), the Power Button is not a wake event. As a result, it is conceivable that the user will press and continue to hold the Power Button waiting for the system to awake. Since a 4-second press of the Power Button is already defined as an Unconditional Power down, the power button timer will be forced to inactive while the power-cycle timer is in progress. Once the power-cycle timer has expired, the Power Button awakes the system. Once the minimum SLP_S4# power cycle expires, the Power Button must be pressed for another 4 to 5 seconds to create the Override condition to S5.

5.15.8.1.2 Sleep Button

The *Advanced Configuration and Power Interface, Version 2.0b* defines an optional Sleep button. It differs from the power button in that it is only a request to go from S0 to S1–S4 (not S5). Also, in an S5 state, the Power Button can wake the system, but the Sleep Button cannot.

Although the Intel® 631xESB/632xESB I/O Controller Hub does not include a specific signal designated as a Sleep Button, one of the GPIO signals can be used to create a “Control Method” Sleep Button. See the *Advanced Configuration and Power Interface, Version 2.0b* for implementation details.

5.15.8.2 RI# (Ring Indicator)

The Ring Indicator can cause a wake event (if enabled) from the S1–S5 states. Table 5-52 shows when the wake event is generated or ignored in different states. If in the G0/S0/Cx states, the Intel® 631xESB/632xESB I/O Controller Hub generates an interrupt based on RI# active, and the interrupt will be set up as a Break event.

Table 5-52. Transitions Due to RI# Signal

Present State	Event	RI_EN	Event
S0	RI# Active	X	Ignored
S1–S5	RI# Active	0 1	Ignored Wake Event

Note: Filtering/Debounce on RI# will not be done in Intel® 631xESB/632xESB I/O Controller Hub. Can be in modem or external.

5.15.8.3 PME# (PCI Power Management Event)

The PME# signal comes from a PCI device to request that the system be restarted. The PME# signal can generate an SMI#, SCI, or optionally a Wake event. The event occurs when the PME# signal goes from high to low. No event is caused when it goes from low to high.

There is also an internal PME_B0 bit. This is separate from the external PME# signal and can cause the same effect.

5.15.8.4 SYS_RESET# Signal

When the SYS_RESET# pin is detected as active after the 16 ms debounce logic, the Intel® 631xESB/632xESB I/O Controller Hub attempts to perform a “graceful” reset, by waiting up to 25 ms for the SMBus to go idle. If the SMBus is idle when the pin is detected active, the reset occurs immediately; otherwise, the counter starts. If at any point during the count the SMBus goes idle the reset occurs. If, however, the counter expires and the SMBus is still active, a reset is forced upon the system even though activity is still occurring.

Once the reset is asserted, it remains asserted for ~1 ms regardless of whether the SYSRESET# input remains asserted or not. It cannot occur again until SYS_RESET# has been detected inactive after the debounce logic, and the system is back to a full S0 state with PLTRST# inactive.

5.15.8.5 THRMTRIP# Signal

If THRMTRIP# goes active, the processor is indicating an overheat condition, and the Intel® 631xESB/632xESB I/O Controller Hub immediately transitions to an S5 state. However, since the processor has overheated, it does not respond to the Intel® 631xESB/632xESB I/O Controller Hub’s STPCLK# pin with a stop grant special cycle. Therefore, the Intel® 631xESB/632xESB I/O Controller Hub does not wait for one. Immediately upon seeing THRMTRIP# low, the Intel® 631xESB/632xESB I/O Controller Hub initiates a transition to the S5 state, drive SLP_S3#, SLP_S4#, SLP_S5# low, and set the CTS bit. The transition looks like a power button override.

It is extremely important that when a THRMTRIP# event occurs, the Intel® 631xESB/632xESB I/O Controller Hub power down immediately without following the normal S0 -> S5 path. This path may be taken in parallel, but Intel® 631xESB/632xESB I/O Controller Hub must immediately enter a power down state. It does this by driving SLP_S3#, SLP_S4#, and SLP_S5# immediately after sampling THRMTRIP# active.

If the processor is running extremely hot and is heating up, it is possible (although very unlikely) that components around it, such as the Intel® 631xESB/632xESB I/O Controller Hub, are no longer executing cycles properly. Therefore, if THRMTRIP# goes active, and the Intel® 631xESB/632xESB I/O Controller Hub is relying on state machine logic to perform the power down, the state machine may not be working, and the system will not power down.

The Intel® 631xESB/632xESB I/O Controller Hub follows this flow for THRMTRIP#.

1. At boot (PLTRST# low), THRMTRIP# ignored.
2. After power-up (PLTRST# high), if THRMTRIP# sampled active, SLP_S3#, SLP_S4#, and SLP_S5# assert, and normal sequence of sleep machine starts.
3. Until sleep machine enters the S5 state, SLP_S3#, SLP_S4#, and SLP_S5# stay active, even if THRMTRIP# is now inactive. This is the equivalent of “latching” the thermal trip event.
4. If S5 state reached, go to step #1, otherwise stay here. If the Intel® 631xESB/632xESB I/O Controller Hub never reaches S5, the Intel® 631xESB/632xESB I/O Controller Hub does not reboot until power is cycled.

During boot, THRMTRIP# is ignored until SLP_S3#, PWROK, VRMPWRGD/VGATE, and PLTRST# are all ‘1’. During entry into a powered-down state (due to S3,S4, S5 entry, power cycle reset, and so forth.) THRMTRIP# is ignored until either SLP_S3# = 0, or PWROK = 0, or VRMPWRGD/ VGATE = 0.

Note: A thermal trip event will:

- Set the AFTERG3_EN bit.
- Clear the PWRBTN_STS bit.
- Clear all the GPE0_EN register bits.
- Clear the SMB_WAK_STS bit only if SMB_SAK_STS was set due to SMBus Slave receiving message and not set due to SMBAlert.

5.15.9 ALT Access Mode

Before entering a low power state, several registers from powered down parts may need to be saved. In the majority of cases, this is not an issue, as registers have read and write paths. However, several of the ISA compatible registers are either read only or write only. To get data out of write-only registers, and to restore data into read-only registers, the Intel® 631xESB/632xESB I/O Controller Hub implements an ALT access mode.

If the ALT access mode is entered and exited after reading the registers of the Intel® 631xESB/632xESB I/O Controller Hub timer (8254), the timer starts counting faster (13.5 ms). The following steps listed below can cause problems:

1. BIOS enters ALT access mode for reading the Intel® 631xESB/632xESB I/O Controller Hub timer related registers.
2. BIOS exits ALT access mode.

3. BIOS continues through the execution of other needed steps and passes control to the operating system.

After getting control in step #3, if the operating system does not reprogram the system timer again, the timer ticks may be happening faster than expected. For example DOS and its associated software assume that the system timer is running at 54.6 ms and as a result the time-outs in the software may be happening faster than expected.

Operating systems (for example, Microsoft Windows* 98, Windows* 2000, and Windows NT*) reprogram the system timer and therefore do not encounter this problem.

For some other loss (for example, Microsoft MS-DOS*) the BIOS should restore the timer back to 54.6 ms before passing control to the operating system. If the BIOS is entering ALT access mode before entering the suspend state it is not necessary to restore the timer contents after the exit from ALT access mode.

5.15.9.1 Write Only Registers with Read Paths in ALT Access Mode

The registers described in Table 5-53 have read paths in ALT access mode. The access number field in the table indicates which register will be returned per access to that port.

Table 5-53. Write Only Registers with Read Paths in ALT Access Mode (Sheet 1 of 2)

Restore Data				Restore Data			
I/O Addr	# of Rds	Access	Data	I/O Addr	# of Rds	Access	Data
00h	2	1	DMA Chan 0 base address low byte	40h	7	1	Timer Counter 0 status, bits [5:0]
		2	DMA Chan 0 base address high byte			2	Timer Counter 0 base count low byte
01h	2	1	DMA Chan 0 base count low byte			3	Timer Counter 0 base count high byte
		2	DMA Chan 0 base count high byte			4	Timer Counter 1 base count low byte
02h	2	1	DMA Chan 1 base address low byte			5	Timer Counter 1 base count high byte
		2	DMA Chan 1 base address high byte			6	Timer Counter 2 base count low byte
03h	2	1	DMA Chan 1 base count low byte			7	Timer Counter 2 base count high byte
		2	DMA Chan 1 base count high byte	41h	1		Timer Counter 1 status, bits [5:0]
04h	2	1	DMA Chan 2 base address low byte	42h	1		Timer Counter 2 status, bits [5:0]
		2	DMA Chan 2 base address high byte	70h	1		Bit 7 = NMI Enable, Bits [6:0] = RTC Address
05h	2	1	DMA Chan 2 base count low byte	C4h	2	1	DMA Chan 5 base address low byte
		2	DMA Chan 2 base count high byte			2	DMA Chan 5 base address high byte
06h	2	1	DMA Chan 3 base address low byte	C6h	2	1	DMA Chan 5 base count low byte
		2	DMA Chan 3 base address high byte			2	DMA Chan 5 base count high byte
07h	2	1	DMA Chan 3 base count low byte	C8h	2	1	DMA Chan 6 base address low byte
		2	DMA Chan 3 base count high byte			2	DMA Chan 6 base address high byte

Table 5-53. Write Only Registers with Read Paths in ALT Access Mode (Sheet 2 of 2)

Restore Data				Restore Data			
I/O Addr	# of Rds	Access	Data	I/O Addr	# of Rds	Access	Data
08h	6	1	DMA Chan 0–3 Command[2]	CAh	2	1	DMA Chan 6 base count low byte
		2	DMA Chan 0–3 Request			2	DMA Chan 6 base count high byte
		3	DMA Chan 0 Mode: Bits(1:0) = 00	CCh	2	1	DMA Chan 7 base address low byte
		4	DMA Chan 1 Mode: Bits(1:0) = 01			2	DMA Chan 7 base address high byte
		5	DMA Chan 2 Mode: Bits(1:0) = 10	CEh	2	1	DMA Chan 7 base count low byte
		6	DMA Chan 3 Mode: Bits(1:0) = 11.			2	DMA Chan 7 base count high byte
20h	12	1	PIC ICW2 of Master controller	D0h	6	1	DMA Chan 4–7 Command[2]
		2	PIC ICW3 of Master controller			2	DMA Chan 4–7 Request
		3	PIC ICW4 of Master controller			3	DMA Chan 4 Mode: Bits(1:0) = 00
		4	PIC OCW1 of Master controller[1]			4	DMA Chan 5 Mode: Bits(1:0) = 01
		5	PIC OCW2 of Master controller			5	DMA Chan 6 Mode: Bits(1:0) = 10
		6	PIC OCW3 of Master controller			6	DMA Chan 7 Mode: Bits(1:0) = 11.
		7	PIC ICW2 of Slave controller				
		8	PIC ICW3 of Slave controller				
		9	PIC ICW4 of Slave controller				
		10	PIC OCW1 of Slave controller[1]				
		11	PIC OCW2 of Slave controller				
		12	PIC OCW3 of Slave controller				

Notes:
1. The OCW1 register must be read before entering ALT access mode.
2. Bits 5, 3, 1, and 0 return 0.

5.15.9.2 PIC Reserved Bits

Many bits within the PIC are reserved, and must have certain values written in order for the PIC to operate properly. Therefore, there is no need to return these values in ALT access mode. When reading PIC registers from 20h and A0h, the reserved bits shall return the values listed in Table 5-54.

Table 5-54. PIC Reserved Bits Return Values

PIC Reserved Bits	Value Returned
ICW2(2:0)	000
ICW4(7:5)	000
ICW4(3:2)	00
ICW4(0)	0
OCW2(4:3)	00
OCW3(7)	0
OCW3(5)	Reflects bit 6
OCW3(4:3)	01

5.15.9.3 Read Only Registers with Write Paths in ALT Access Mode

The registers described in Table 5-55 have write paths to them in ALT access mode. Software restores these values after returning from a powered down state. These registers must be handled special by software. When in normal mode, writing to the base address/count register also writes to the current address/count register. Therefore, the base address/count must be written first, then the part is put into ALT access mode and the current address/count register is written.

Table 5-55. Register Write Accesses in ALT Access Mode

I/O Address	Register Write Value
08h	DMA Status Register for channels 0–3.
D0h	DMA Status Register for channels 4–7.

5.15.10 System Power Supplies, Planes, and Signals

5.15.10.1 Power Plane Control with SLP_S3#, SLP_S4#, and SLP_S5#

The usage of SLP_S3# and SLP_S4# depends on whether the platform is configured for S3-Hot and S3-Cold.

- S3-Hot: The SLP_S3# output signal is used to cut power only to the processor and to stop system clocks.
- S3-Cold: The SLP_S3# output signal can be used to cut power to the system core supply, since it goes active only for the STR state (typically mapped to ACPI S3). Power must be maintained to the Intel® 631xESB/632xESB I/O Controller Hub resume well, and to any other circuits that need to generate Wake signals from the STR state.

Cutting power to the core may be done by way of the power supply, or by external FETs to the motherboard.

The SLP_S4# or SLP_S5# output signal can be used to cut power to the system core supply, as well as power to the system memory, since the context of the system is saved on the disk. Cutting power to the memory may be done by way of the power supply, or by external FETs to the motherboard. In systems set up for S3-Hot, the SLP_S4# is also used to kill power to the subsystems that are powered during the S3-Hot state.

The SLP_S4# output signal is used to remove power to additional subsystems that are powered during SLP_S3#.

SLP_S5# output signal can be used to cut power to the system core supply, as well as power to the system memory, since the context of the system is saved on the disk. Cutting power to the memory may be done by way of the power supply, or by external FETs to the motherboard.

5.15.10.2 SLP_S4# and Suspend-To-RAM Sequencing

The system memory suspend voltage regulator is controlled by the Glue logic. The SLP_S4# signal should be used to remove power to system memory rather than the SLP_S5# signal. The SLP_S4# logic in the Intel® 631xESB/632xESB I/O Controller Hub provides a mechanism to fully cycle the power to the DRAM and/or detect if the power is not cycled for a minimum time.

Note: To utilize the minimum DRAM power-down feature that is enabled by the SLP_S4# Assertion Stretch Enable bit (D31:F0:A4h bit 3), the DRAM power must be controlled by the SLP_S4# signal.

5.15.10.3 PWROK Signal

The PWROK input should go active based on the core supply voltages becoming valid. PWROK must not go high until at least 99 ms after the power is guaranteed valid. This is required to meet the 100ms delay from valid power to PLTRST# deassertion in the PCI 2.3 Specification.

1. SYSRESET# is recommended for implementing the system reset button. This saves external logic that is needed if the PWROK input is used. Additionally, it allows for better handling of the SMBus and processor resets, and avoids improperly reporting power failures.
2. If a design has an active-low reset button electrically ANDed with the PWROK signal from the power supply and the processor's voltage regulator module the Intel® 631xESB/632xESB I/O Controller Hub PWROK_FLR bit will be set. The Intel® 631xESB/632xESB I/O Controller Hub treats this internally as if the RSMRST# signal had gone active. However, it is not treated as a full power failure. If PWROK goes inactive and then active (but RSMRST# stays high), then the Intel® 631xESB/632xESB I/O Controller Hub reboots (regardless of the state of the AFTERG3 bit). If the RSMRST# signal also goes low before PWROK goes high, then this is a full power failure, and the reboot policy is controlled by the AFTERG3 bit.
3. PWROK and RSMRST# are sampled using the RTC clock. Therefore, low times that are less than one RTC clock period may not be detected by the Intel® 631xESB/ 632xESB I/O Controller Hub.
4. In the case of true PWROK failure, PWROK goes low first before the VRMPWRGD.
5. If the PWROK input is used to implement the system reset button, the Intel® 631xESB/632xESB I/O Controller Hub does not provide any mechanism to limit the amount of time that the processor is held in reset. The platform must externally guarantee that maximum reset assertion specs are met.

5.15.10.4 CPUPWRGD Signal

This signal is connected to the processor's VRM by way of the VRMPWRGD signal and is internally ANDed with the PWROK signal that comes from the system power supply.

5.15.10.5 VRMPWRGD Signal

VRMPWRGD is an input from the regulator indicating that all of the outputs from the regulator are on and within specification. VRMPWRGD may go active before or after the PWROK from the main power supply. Intel® 631xESB/632xESB I/O Controller Hub has no dependency on the order in which these two signals go active or inactive.

5.15.10.6 Controlling Leakage and Power Consumption During Low-Power States

To control leakage in the system, various signals tri-state or go low during some low-power states.

General principles:

- All signals going to powered down planes (either internally or externally) must be either tri-stated or driven low.

- Signals with pull-up resistors should not be low during low-power states. This is to avoid the power consumed in the pull-up resistor.
- Buses should be halted (and held) in a known state to avoid a floating input (perhaps to some other device). Floating inputs can cause extra power consumption.

Based on the above principles, the following measures are taken:

- During S3 (STR), all signals attached to powered down planes are tri-stated or driven low.

5.15.11 Clock Generators

The clock generator is expected to provide the frequencies shown in Table 5-56.

Table 5-56. Intel® 631xESB/632xESB I/O Controller Hub Clock Inputs

Clock Domain	Frequency	Source	Usage
CLK100	100 MHz Differential	Main Clock Generator	Used by SATA controller. Stopped in S3 ~ S5 based on SLP_S3# assertion.
PCICLK	33 MHz	Main Clock Generator	Free-running PCI Clock to Intel® 631xESB/632xESB I/O Controller Hub. Stopped in S3 ~ S5 based on SLP_S3# assertion.
CLK48	48 MHz	Main Clock Generator	Used by USB controllers and Intel High Definition Audio controller. Stopped in S3 ~ S5 based on SLP_S3# assertion.
CLK14	14.318 MHz	Main Clock Generator	Used by ACPI timers. Stopped in S3 ~ S5 based on SLP_S3# assertion.
ACZ_BIT_CLK	12.288 MHz	AC'97 Codec	AC-link. Control policy is determined by the clock source. ***Note:*** Becomes clock output when Intel High Definition Audio is enabled.

5.15.12 Legacy Power Management Theory of Operation

Instead of relying on ACPI software, legacy power management uses BIOS and various hardware mechanisms. The scheme relies on the concept of detecting when individual subsystems are idle, detecting when the whole system is idle, and detecting when accesses are attempted to idle subsystems.

5.16 System Management (D31:F0)

The Intel® 631xESB/632xESB I/O Controller Hub provides various functions to make a system easier to manage and to lower the Total Cost of Ownership (TCO) of the system. Features and functions can be augmented by way of external A/D converters and GPIO, as well as an external microcontroller.

The following features and functions are supported by Intel® 631xESB/632xESB I/O Controller Hub:

- 1st Timer to Generate SMI# after Programmable Time
  - — 1st timeout causes SMI#. Allows for SMM-Based Recovery from OS lockup.
  - — OS-based software agent accesses Intel® 631xESB/632xESB I/O Controller Hub to periodically reload timer.
- Ability for OS to generate SMI#
  - — Call-back from OS to TCO code in SMM handler.

- 2nd Hard Coded Timeout to Generate Reboot
  - Used only after 1st timeout occurs
  - 2nd timeout allows for automatic system ‘reset and reboot’ if hardware error detected. Various system states are preserved by way of this special reset to allow for possible error detection and correction.
  - Reset associated with ‘reboot’ may attempt to preserve some registers for diagnostic purposes.
  - SMI# handler must reload the main timer within 2.4 seconds to prevent the 2nd timer from causing a ‘reboot’ (timeout during SMI is assumed as broken CPU or stuck hardware).
  - Option to prevent reset if 2nd timeout occurs.
- Ability to detect “Broken” CPU:
  - Detects if processor fails to restart after it has been reset.
  - If CPU failure detected, option to pulse a GPIO or send SMBus message. The SMBus message can be used to indicate to an External D110 LAN controller to send a distress message. The GPIO can control an LED with optional blink.
- Ability to Handle Various Errors (such as ECC Errors) Indicated by the MCH
  - Can generate SMI# or TCO interrupt.
- Intruder Detect input if the system cover is removed
  - Can generate TCO interrupt or SMI#
- Ability for TCO messages to coexist with standard SMBus devices
- Detection of bad FWH programming. Done by checking that data on the first read is not FFh
- Based on Cape Lookout ASF (CLASF) core

5.16.1 Theory of Operation

The System Management functions are designed to allow the system to diagnose failing subsystems. An industry term, ‘Functionally Replaceable Units’ (FRUs), will be used throughout this document, although the subsystem may not technically be a FRU. Each FRU, and the method to detect its failure, will be discussed below.

The intent of this logic is that some of the system management functionality be provided without the aid of an external microcontroller.

The Intel® 631xESB/632xESB I/O Controller Hub’s System Management logic allows for diagnostic and recovery software to be distributed between an SMI handler and OS-based code. The handling methods between the SMI handler and OS are also discussed.

5.16.1.1 Detecting a DOA CPU or System

A CPU may fail to reset if it has been inserted incorrectly, is somehow damaged (that is, due to vibrational stress), if the chipset itself is not working properly, or if the CPU is missing. After the chipset attempts to reset the CPU, the CPU is expected to fetch its first instruction.

If it fails to do so, the chipset will detect this because the TCO timer will timeout twice.

If TCO Reboots are not enabled, then Intel® 631xESB/632xESB I/O Controller Hubs will either:

a. The SMLink will send out the first 8 bits of the message. After the 8th bit, the logic will stall because there is no integrated LAN controller to send the ACK. The logic will then abort the transfer. External logic can monitor the toggling and use that to drive an LED.

b. If an External LAN controller is connected: send the appropriate message to the External LAN controller.

If TCO Reboots are enabled, then Intel® 631xESB/632xESB I/O Controller Hub attempts to asserts PCIRST# to reboot the system.

Note:

1. If the NO-REBOOT bit (D31:F0:Offset D4:bit 1) is set (no reboots are intended) and SECOND_TO_STS bit (TCO I/O Offset 06h, bit 1) is set and DOACPU_STS bit (TCO I/O Offset 06h, bit 2) is set, the Intel® 631xESB/632xESB I/O Controller Hub will indicate this in the TCO message by setting the CPU Missing bit in the message.
2. If the NO-REBOOT bit (D31:F0:Offset D4:bit 1) is not set (reboots intended and SECOND_TO_STS bit TCO I/O Offset 06h, bit 1) is set, then Intel® 631xESB/ 632xESB I/O Controller Hub will attempt to reboot. After the reboot, the SECOND_TO_STS bit will still be set. If the CPU fails to fetch the first instruction, the DOA_CPU_STS bit is set, and when the TCO timer times out (actually for the third time, the first two caused the SECOND_TO_STS bit to be set), then Intel® 631xESB/632xESB I/O Controller Hub sets the CPU MISSING EVENT bit for the TCO message.

5.16.1.2 Handling an OS Lockup

Under some conditions, the OS may lock up. To handle this, the TCO Timer is used with the following algorithm:

1. BIOS programs the TCO Timer, by way of the TCO_TMR register with an initial value.
2. An OS-based software agent periodically writes to the TCO_RLD register to reload the timer and keep it from generating the SMI#. The software agent can read the TCO_RLD register to see if it is close to timing out, and possibly determine if the time-out should be increased. The OS can also modify the values in the TCO_TMR register.3. If the timer reaches 0, an SMI# can be generated. This should occur only if the OS was not able to reload the timer. It is assumed that the OS will not be able to reload the timer if it has locked up.
3. Upon generating the SMI#, the TCO Timer automatically reloads with the default value of 04h and start counting down.
4. The SMI handler can then:
   a. Read the TIMEOUT bit in the TCO_STS register to check that the SMI# was caused by the TCO timer. And, the SMI handler should also clear the TIMEOUT bit.
   b. Write to the TCO_RLD register to reload the timer to make sure the TCO timer does not reach 0 again.
   c. Attempt to recover. May need to periodically reload the TCO timer.

The exact recovery algorithm will be system-specific.

Note: If the SMI handler was not able to clear the TIMEOUT bit and write to the TCO_RLD register, the timer will reach zero a second time approximately 2.4 seconds later. At that point, the hardware is assumed to be locked up, and the timer will read 0 a second

time, which causes the SECOND_TO_STS bit to be set. At that point the logic will reset the platform if the reboots are enabled.

5.16.1.3 Handling a CPU or Other Hardware Lockup

If after the TIMEOUT SMI is generated, and the TCO timer again reaches 0, and reboots are enabled, the System Management logic will reset (and reboot) the system. This would be in the case where the CPU or other system hardware is locked up. During every boot, BIOS should read the SECOND_TO_STS bit in the TCO_STS register to see if this is normal boot or a reboot due to the timeout. The BIOS may also check the OS_POLICY bits to see if it should try another boot or shutdown.

5.16.1.4 Handling an Intruder

The Intel® 631xESB/632xESB I/O Controller Hub has an input signal, INTRUDER#, that can be attached to a switch that is activated by the system's case being open. This input has a two RTC clock debounce. If INTRUDER# goes active (after the debouncer), this will set the INTRD_DET bit in the TCO_STS register. The INTRD_SEL bits in the TCO_CNT register can enable the Intel® 631xESB/632xESB I/O Controller Hub to cause an SMI# or interrupt. The BIOS or interrupt handler can then cause a transition to the S5 state by writing to the SLP_EN bit.

The software can also directly read the status of the INTRUDER# signal (high or low) by clearing and then reading the INTRD_DET bit. This allows the signal to be used as a GPI if the intruder function is not required.

If the INTRUDER# signal goes inactive some point after the INTRD_DET bit is written as a 1, then the INTRD_DET signal will go to a 0 when INTRUDER# input signal goes inactive. Note that this is slightly different than a classic sticky bit, since most sticky bits would remain active indefinitely when the signal goes active and would immediately go inactive when a 1 is written to the bit.

Note: The INTRD_DET bit resides in the Intel® 631xESB/632xESB I/O Controller Hub's RTC well, and is set and cleared synchronously with the RTC clock. Thus, when software attempts to clear INTRD_DET (by writing a 1 to the bit location) there may be as much as two RTC clocks (about 65 µs) delay before the bit is actually cleared. Also, the INTRUDER# signal should be asserted for a minimum of 1 ms to guarantee that the INTRD_DET bit will be set.

Note: If the INTRUDER# signal is still active when software attempts to clear the INTRD_DET bit, the bit remains set and the SMI is generated again immediately. The SMI handler can clear the INTRD_SEL bits to avoid further SMIs. However, if the INTRUDER# signal goes inactive and then active again, there will not be further SMIs, since the INTRD_SEL bits would select that no SMI# be generated.

5.16.1.5 Handling a Potentially Failing Power Supply

It may be possible to detect that a power supply may fail in the near future by monitoring its voltages for fluctuations. To support such an application, external A/Ds with programmable thresholds could be included by way of SMBus/I^2C. Upon receiving the SMBus/I^2C message, Intel® 631xESB/632xESB I/O Controller Hub can generate an SMI or interrupt. The SMI handler (or OS-based extension) could then attempt to send a message before the power completely fails.

Another option would be to build an A/D into the power supply itself. Another signal, other than PWROK, could report that the power supply might soon fail.

5.16.1.6 Detecting Improper Firmware Hub Programming

The Intel® 631xESB/632xESB I/O Controller Hub can detect the case where the Firmware Hub is not programmed. This results in the first instruction fetched to have a value of FFh. If this occurs, the Intel® 631xESB/632xESB I/O Controller Hub sets the BAD_BIOS bit, which can then be reported by way of the Heartbeat and Event reporting using an external, Alert on LAN* enabled LAN controller (See Section 5.16.2).

5.16.2 Heartbeat and Event Reporting by way of SMBUS

The Intel® 631xESB/632xESB I/O Controller Hub integrated LAN controller supports ASF heartbeat and event reporting functionality. This allows the integrated LAN controller to report messages to a network management console without the aid of the system processor. This is crucial in cases where the processor is malfunctioning or cannot function due to being in a low-power state.

All heartbeat and event messages are sent on the SMBus interface. This allows an external LAN controller to act upon these messages if the internal LAN controller is not used.

The basic scheme is for the Intel® 631xESB/632xESB I/O Controller Hub integrated LAN controller to send a prepared Ethernet message to a network management console. The prepared message is stored in the non-volatile EEPROM that is connected to the Intel® 631xESB/632xESB I/O Controller Hub.

Messages are sent by the LAN controller either because a specific event has occurred, or they are sent periodically (also known as a heartbeat). The event and heartbeat messages have the exact same format. The event messages are sent based on events occurring. The heartbeat messages are sent every 30 to 32 seconds. When an event occurs, the Intel® 631xESB/632xESB I/O Controller Hub sends a new message and increments the SEQ[3:0] field. For heartbeat messages, the sequence number does not increment.

The following rules/steps apply if the system is in a G0 state and the policy is for the Intel® 631xESB/632xESB I/O Controller Hub **to reboot** the system after a hardware lockup:

1. On detecting the lockup, the SECOND_TO_STS bit is set. The Intel® 631xESB/632xESB I/O Controller Hub may send up to 1 Event message to the LAN controller. The Intel® 631xESB/632xESB I/O Controller Hub then attempts to reboot the processor.
2. If the reboot at step 1 is successful then the BIOS should clear the SECOND_TO_STS bit. This prevents any further Heartbeats from being sent. The BIOS may then perform addition recovery/boot steps. (See note 2, below.)
3. If the reboot attempt in step 1 is not successful, the timer will timeout a third time. At this point the system has locked up and was unsuccessful in rebooting. The Intel® 631xESB/632xESB I/O Controller Hub does not attempt to automatically reboot again. The Intel® 631xESB/632xESB I/O Controller Hub starts sending a message every heartbeat period
(30–32 seconds). The heartbeats continue until some external intervention occurs (reset, power failure, and so forth.).
4. After step 3 (unsuccessful reboot after third timeout), if the user does a Power Button Override, the system goes to an S5 state. The Intel® 631xESB/632xESB I/O Controller Hub continues sending the messages every heartbeat period.

5. After step 4 (power button override after unsuccessful reboot) if the user presses the Power Button again, the system should wake to an S0 state and the processor should start executing the BIOS.
6. If step 5 (power button press) is successful in waking the system, the Intel® 631xESB/632xESB I/O Controller Hub continues sending messages every heartbeat period until the BIOS clears the SECOND_TO_STS bit. (See note 2)
7. If step 5 (power button press) is unsuccessful in waking the system, the Intel® 631xESB/632xESB I/O Controller Hub continues sending a message every heartbeat period. The Intel® 631xESB/632xESB I/O Controller Hub does not attempt to automatically reboot again. The Intel® 631xESB/632xESB I/O Controller Hub starts sending a message every heartbeat period (30–32 seconds). The heartbeats continue until some external intervention occurs (reset, power failure, and so forth.). (See note 3)
8. After step 3 (unsuccessful reboot after third timeout), if a reset is attempted (using a button that pulses PWROK low or by way of the message on the SMBus Slave I/F), the Intel® 631xESB/632xESB I/O Controller Hub attempts to reset the system.
9. After step 8 (reset attempt) if the reset is successful, the BIOS is run. The Intel® 631xESB/632xESB I/O Controller Hub continues sending a message every heartbeat period until the BIOS clears the SECOND_TO_STS bit. (See note 2)
10. After step 8 (reset attempt), if the reset is unsuccessful, the Intel® 631xESB/632xESB I/O Controller Hub continues sending a message every heartbeat period. The Intel® 631xESB/632xESB I/O Controller Hub does not attempt to reboot the system again without external intervention. (See note 3)

The following rules/steps apply if the system is in a G0 state and the policy is for the Intel® 631xESB/632xESB I/O Controller Hub to **not reboot** the system after a hardware lockup.

1. On detecting the lockup the SECOND_TO_STS bit is set. The Intel® 631xESB/632xESB I/O Controller Hub sends a message with the Watchdog (WD) Event status bit set (and any other bits that must also be set). This message is sent as soon as the lockup is detected, and is sent with the next (incremented) sequence number.
2. After step 1, the Intel® 631xESB/632xESB I/O Controller Hub sends a message every heartbeat period until some external intervention occurs.
3. Rules/steps 4–10 apply if no user intervention (resets, power button presses, SMBus reset messages) occur after a third timeout of the watchdog timer. If the intervention occurs before the third timeout, then jump to rule/step 11.
4. After step 3 (third timeout), if the user does a Power Button Override, the system goes to an S5 state. The Intel® 631xESB/632xESB I/O Controller Hub continues sending heartbeats at this point.
5. After step 4 (power button override), if the user presses the power button again, the system should wake to an S0 state and the processor should start executing the BIOS.
6. If step 5 (power button press) is successful in waking the system, the Intel® 631xESB/632xESB I/O Controller Hub continues sending heartbeats until the BIOS clears the SECOND_TO_STS bit. (See note 2)
7. If step 5 (power button press) is unsuccessful in waking the system, the Intel® 631xESB/632xESB I/O Controller Hub continues sending heartbeats. The Intel® 631xESB/632xESB I/O Controller Hub does not attempt to reboot the system again until some external intervention occurs (reset, power failure, and so forth.). (See note 3)

8. After step 3 (third timeout), if a reset is attempted (using a button that pulses PWROK low or by way of the message on the SMBus Slave I/F), the Intel® 631xESB/632xESB I/O Controller Hub attempts to reset the system.
9. If step 8 (reset attempt) is successful, the BIOS is run. The Intel® 631xESB/632xESB I/O Controller Hub continues sending heartbeats until the BIOS clears the SECOND_TO_STS bit. (See note 2)
10. If step 8 (reset attempt), is unsuccessful, the Intel® 631xESB/632xESB I/O Controller Hub continues sending heartbeats. The Intel® 631xESB/632xESB I/O Controller Hub does not attempt to reboot the system again without external intervention. **Note:** A system that has locked up and can not be restarted with power button press is probably broken (bad power supply, short circuit on some bus, and so forth.)
11. This and the following rules/steps apply if the user intervention (power button press, reset, SMBus message, and so forth.) occur prior to the third timeout of the watchdog timer.
12. After step 1 (second timeout), if the user does a Power Button Override, the system goes to an S5 state. The Intel® 631xESB/632xESB I/O Controller Hub continues sending heartbeats at this point.
13. After step 12 (power button override), if the user presses the power button again, the system should wake to an S0 state and the processor should start executing the BIOS.
14. If step 13 (power button press) is successful in waking the system, the Intel® 631xESB/632xESB I/O Controller Hub continues sending heartbeats until the BIOS clears the SECOND_TO_STS bit. (See note 2)
15. If step 13 (power button press) is unsuccessful in waking the system, the Intel® 631xESB/632xESB I/O Controller Hub continues sending heartbeats. The Intel® 631xESB/632xESB I/O Controller Hub does not attempt to reboot the system again until some external intervention occurs (reset, power failure, and so forth.). (See note 3)
16. After step 1 (second timeout), if a reset is attempted (using a button that pulses PWROK low or by way of the message on the SMBus Slave I/F), the Intel® 631xESB/632xESB I/O Controller Hub attempts to reset the system.
17. If step 16 (reset attempt) is successful, the BIOS is run. The Intel® 631xESB/632xESB I/O Controller Hub continues sending heartbeats until the BIOS clears the SECOND_TO_STS bit. (See note 2)
18. If step 16 (reset attempt), is unsuccessful, the Intel® 631xESB/632xESB I/O Controller Hub continues sending heartbeats. The Intel® 631xESB/632xESB I/O Controller Hub does not attempt to reboot the system again without external intervention. (See note 3)

If the system is in a G1 (S1–S4) state, the Intel® 631xESB/632xESB I/O Controller Hub sends a heartbeat message every 30–32 seconds. If an event occurs prior to the system being shutdown, the Intel® 631xESB/632xESB I/O Controller Hub immediately sends an event message with the next incremented sequence number. After the event message, the Intel® 631xESB/632xESB I/O Controller Hub resumes sending heartbeat messages.

Note: A system that has locked up and can not be restarted with power button press is assumed to have broken hardware (bad power supply, short circuit on some bus, and so forth.).

The following rules will apply if the system is in a G1 (S1-S4) state:

- Intel® 631xESB/632xESB I/O Controller Hub will send a Heartbeat message every Heartbeat Period (30-32 seconds).
  - If an event occurs prior to the system being shut down, the Intel® 631xESB/632xESB I/O Controller Hub will immediately send another Event message with the next (incremented) sequence number.
  - After the event, it will resume sending Heartbeat messages.

Note: Normally, the Intel® 631xESB/632xESB I/O Controller Hub does not send heartbeat messages while in the G0 state (except in the case of a lockup). However, if a hardware event (or heartbeat) occurs just as the system is transitioning into a G0 state, the hardware continues to send the message even though the system is in a G0 state (and the status bits may indicate this).

These messages are sent by way of the SMBus. The Intel® 631xESB/632xESB I/O Controller Hub abides by the SMBus rules associated with collision detection. It delays starting a message until the bus is idle, and detects collisions. If a collision is detected the Intel® 631xESB/632xESB I/O Controller Hub waits until the bus is idle, and tries again.

Warning: It is important the BIOS clears the SECOND_TO_STS bit, as the alerts interfere with the LAN device driver from working properly. The alerts reset part of the LAN controller and would prevent an operating system's device driver from sending or receiving some messages.

Note: A spurious alert could occur in the following sequence:

- The processor has initiated an alert using the SEND_NOW bit
- During the alert, the THRM#, INTRUDER# or GPI[11] changes state
- The system then goes to a non-S0 state.

Once the system transitions to the non-S0 state, it may send a single alert with an incremental SEQUENCE number.

Note: An inaccurate alert message can be generated in the following scenario

- The system successfully boots after a second watchdog Timeout occurs.
- PWROK goes low (typically due to a reset button press) or a power button override occurs (before the SECOND_TO_STS bit is cleared).
- An alert message indicating that the processor is missing or locked up is generated with a new sequence number.

Table 5-57 shows the data included in the Alert on LAN messages.

Table 5-57. Heartbeat Message Data (Sheet 1 of 2)

Field	Comment
Cover Tamper Status	1 = This bit is set if the intruder detect bit is set (INTRD_DET).
Temp Event Status	1 = This bit is set if the Intel® 631xESB/632xESB I/O Controller Hub THERM# input signal is asserted.
Processor Missing Event Status	1 = This bit is set if the processor failed to fetch its first instruction.
TCO Timer Event Status	1 = This bit is set when the TCO timer expires.
Software Event Status	1 = This bit is set when software writes a 1 to the SEND_NOW bit.
Unprogrammed Firmware Hub Event Status	1 = First BIOS fetch returned a value of FFh, indicating that the Firmware Hub has not yet been programmed (still erased).

Table 5-57. Heartbeat Message Data (Sheet 2 of 2)

Field	Comment
GPIO Status	1 = This bit is set when GPI[11] signal is high. 0 = This bit is cleared when GPI[11] signal is low. An event message is triggered on an transition of GPI[11].
SEQ[3:0]	This is a sequence number. It initially is 0, and increments each time the Intel® 631xESB/632xESB I/O Controller Hub sends a new message. Upon reaching 1111, the sequence number rolls over to 0000. MSB (SEQ3) sent first.
System Power State	00 = G0, 01 = G1, 10 = G2, 11 = Pre-Boot. MSB sent first
MESSAGE1	Will be the same as the MESSAGE1 Register. MSB sent first.
MESSAGE2	Will be the same as the MESSAGE2 Register. MSB sent first.
WDSTATUS	Will be the same as the WDSTATUS Register. MSB sent first.

5.17 IDE Controller (D31:F1)

The Intel® 631xESB/632xESB I/O Controller Hub IDE controller features one sets of interface signals (Primary channel) that can be enabled, tri-stated or driven low.

The IDE interfaces of the Intel® 631xESB/632xESB I/O Controller Hub can support several types of data transfers:

- **Programmed I/O (PIO):** Processor is in control of the data transfer.
- **8237 style DMA:** DMA protocol that resembles the DMA on the ISA bus, although it does not use the 8237 in the Intel® 631xESB/632xESB I/O Controller Hub. This protocol off loads the processor from moving data. This allows higher transfer rate of up to 16 MB/s.
- **Ultra ATA/33:** DMA protocol that redefines signals on the IDE cable to allow both host and target throttling of data and transfer rates of up to 33 MB/s.
- **Ultra ATA/66:** DMA protocol that redefines signals on the IDE cable to allow both host and target throttling of data and transfer rates of up to 66 MB/s.
- **Ultra ATA/100:** DMA protocol that redefines signals on the IDE cable to allow both host and target throttling of data and transfer rates of up to 100 MB/s.

5.17.1 PIO Transfers

The Intel® 631xESB/632xESB I/O Controller Hub IDE controller includes both compatible and fast timing modes. The fast timing modes can be enabled only for the IDE data ports. All other transactions to the IDE registers are run in single transaction mode with compatible timings.

Up to two IDE devices may be attached to the IDE connector (drive 0 and drive 1). The IDE_TIMP and IDE_TIMS Registers permit different timing modes to be programmed for drive 0 and drive 1 of the same connector.

The Ultra ATA/33/66/100 synchronous DMA timing modes can also be applied to each drive by programming the IDE I/O Configuration register and the Synchronous DMA Control and Timing registers. When a drive is enabled for synchronous DMA mode operation, the DMA transfers are executed with the synchronous DMA timings. The PIO transfers are executed using compatible timings or fast timings if also enabled.

5.17.1.1 PIO IDE Timing Modes

IDE data port transaction latency consists of startup latency, cycle latency, and shutdown latency. Startup latency is incurred when a PCI Master cycle targeting the IDE data port is decoded and the DA[2:0] and CSxx# lines are not set up. Startup latency provides the setup time for the DA[2:0] and CSxx# lines prior to assertion of the read and write strobes (DIOR# and DIOW#).

Cycle latency consists of the I/O command strobe assertion length and recovery time. Recovery time is provided so that transactions may occur back-to-back on the IDE interface (without incurring startup and shutdown latency) without violating minimum cycle periods for the IDE interface. The command strobe assertion width for the enhanced timing mode is selected by the IDE_TIM Register and may be set to 2, 3, 4, or 5 PCI clocks. The recovery time is selected by the IDE_TIM Register and may be set to 1, 2, 3, or 4 PCI clocks.

If IORDY is asserted when the initial sample point is reached, no wait-states are added to the command strobe assertion length. If IORDY is negated when the initial sample point is reached, additional wait-states are added. Since the rising edge of IORDY must be synchronized, at least two additional PCI clocks are added.

Shutdown latency is incurred after outstanding scheduled IDE data port transactions (either a
non-empty write post buffer or an outstanding read prefetch cycles) have completed and before other transactions can proceed. It provides hold time on the DA[2:0] and CSxx# lines with respect to the read and write strobes (DIOR# and DIOW#). Shutdown latency is two PCI clocks in duration.

The IDE timings for various transaction types are shown in Table 5-58.

Table 5-58. IDE Transaction Timings (PCI Clocks)

IDE Transaction Type	Startup Latency	IORDY Sample Point (ISP)	Recovery Time (RCT)	Shutdown Latency
Non-Data Port Compatible	4	11	22	2
Data Port Compatible	3	6	14	2
Fast Timing Mode	2	2–5	1–4	2

5.17.1.2 IORDY Masking

The IORDY signal can be ignored and assumed asserted at the first IORDY Sample Point (ISP) on a drive by drive basis by way of the IDETIM Register.

5.17.1.3 PIO 32-Bit IDE Data Port Accesses

A 32-bit PCI transaction run to the IDE data address (01F0h primary) results in two back to back 16-bit transactions to the IDE data port. The 32-bit data port feature is enabled for all timings, not just enhanced timing. For compatible timings, a shutdown and startup latency is incurred between the two, 16-bit halves of the IDE transaction. This guarantees that the chip selects are deasserted for at least two PCI clocks between the two cycles.

5.17.1.4 PIO IDE Data Port Prefetching and Posting

The Intel® 631xESB/632xESB I/O Controller Hub can be programmed by way of the IDETIM registers to allow data to be posted to and prefetched from the IDE data ports.

Data prefetching is initiated when a data port read occurs. The read prefetch eliminates latency to the IDE data ports and allows them to be performed back to back for the highest possible PIO data transfer rates. The first data port read of a sector is called the demand read. Subsequent data port reads from the sector are called prefetch reads. The demand read and all prefetch reads much be of the same size (16 or 32 bits).

Data posting is performed for writes to the IDE data ports. The transaction is completed on the PCI bus after the data is received by the Intel® 631xESB/632xESB I/O Controller Hub. The Intel® 631xESB/632xESB I/O Controller Hub then runs the IDE cycle to transfer the data to the drive. If the Intel® 631xESB/632xESB I/O Controller Hub write buffer is non-empty and an unrelated (non-data or opposite channel) IDE transaction occurs, that transaction will be stalled until all current data in the write buffer is transferred to the drive.

5.17.2 Bus Master Function

The Intel® 631xESB/632xESB I/O Controller Hub can act as a PCI Bus Master on behalf of an IDE device. One PCI Bus Master channel is provided for the IDE connector. By performing the IDE data transfer as a PCI Bus Master, the Intel® 631xESB/632xESB I/O Controller Hub off-loads the processor and improves system performance in multitasking environments. Both devices attached to the connector can be programmed for Bus Master transfers, but only one device can be active at a time.

5.17.2.1 Physical Region Descriptor Format

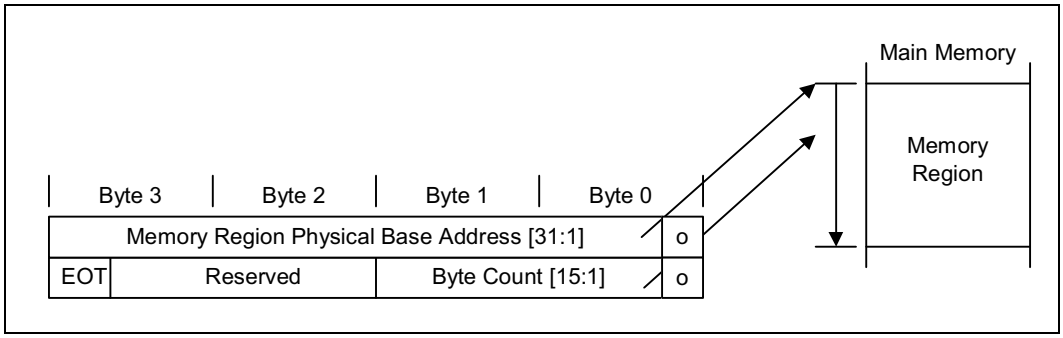
The physical memory region to be transferred is described by a Physical Region Descriptor (PRD). The PRDs are stored sequentially in a Descriptor Table in memory. The data transfer proceeds until all regions described by the PRDs in the table have been transferred.

Descriptor Tables must not cross a 64-KB boundary. Each PRD entry in the table is 8 bytes in length. The first 4 bytes specify the byte address of a physical memory region. This memory region must be DWord-aligned and must not cross a 64-KB boundary. The next two bytes specify the size or transfer count of the region in bytes (64-KB limit per region). A value of 0 in these two bytes indicates 64-KB (thus the minimum transfer count is 1). If bit 7 (EOT) of the last byte is a 1, it indicates that this is the final PRD in the Descriptor table. Bus Master operation terminates when the last descriptor has been retired.

When the Bus Master IDE controller is reading data from the memory regions, bit 1 of the Base Address is masked and byte enables are asserted for all read transfers. When writing data, bit 1 of the Base Address is not masked and if set, will cause the lower Word byte enables to be deasserted for the first DWord transfer. The write to PCI typically consists of a 32-byte cache line. If valid data ends prior to end of the cache line, the byte enables will be deasserted for invalid data.

The total sum of the byte counts in every PRD of the descriptor table must be equal to or greater than the size of the disk transfer request. If greater than the disk transfer request, the driver must terminate the Bus Master transaction (by setting bit 0 in the Bus Master IDE Command Register to 0) when the drive issues an interrupt to signal transfer completion.

Figure 5-18. Physical Region Descriptor Table Entry



5.17.2.2 Bus Master IDE Timings

The timing modes used for Bus Master IDE transfers are identical to those for PIO transfers. The DMA Timing Enable Only bits in IDE Timing register can be used to program fast timing mode for DMA transactions only. This is useful for IDE devices whose DMA transfer timings are faster than its PIO transfer timings. The IDE device DMA request signal is sampled on the same PCI clock that DIOR# or DIOW# is deasserted. If inactive, the DMA Acknowledge signal is deasserted on the next PCI clock and no more transfers take place until DMA request is asserted again.

5.17.2.3 Interrupts

The Intel® 631xESB/632xESB I/O Controller Hub can generate interrupts based upon a signal coming from the PATA device, or due to the completion of a PRD with the 'I' bit set.

The interrupt is edge triggered and active high. The PATA host controller generates IDEIRQ.

When the Intel® 631xESB/632xESB I/O Controller Hub IDE controller is operating independently from the SATA controller (D31:F2), IDEIRQ will generate IRQ14. When operating in conjunction with the SATA controller (combined mode), IDE interrupts will still generate IDEIRQ, but this may in turn generate either IRQ14 or IRQ15, depending upon the value of the MAP.MV (D31:F2:90h:bits 1:0) register. When in combined mode and the SATA controller is emulating the logical secondary channel (MAP.MV = 1h), the PATA channel will emulate the logical primary channel and IDEIRQ will generate IRQ14. Conversely, if the SATA controller in combined mode is emulating the logical primary channel (MAP.MV=2h), IDEIRQ will generate IRQ15.

Note: IDE interrupts cannot be communicated through PCI devices or the serial stream.

5.17.2.4 Bus Master IDE Operation

To initiate a Bus Master transfer between memory and an IDE device, the following steps are required:

1. Software prepares a PRD table in system memory. The PRD table must be DWord aligned and must not cross a 64-KB boundary.
2. Software provides the starting address of the PRD Table by loading the PRD Table Pointer Register. The direction of the data transfer is specified by setting the Read/Write Control bit. The interrupt bit and Error bit in the Status register are cleared.
3. Software issues the appropriate DMA transfer command to the disk device.

4. The Bus Master function is engaged by software writing a 1 to the Start bit in the Command Register. The first entry in the PRD table is fetched and loaded into two registers which are not visible by software, the Current Base and Current Count registers. These registers hold the current value of the address and byte count loaded from the PRD table. The value in these registers is valid only when there is an active command to an IDE device.
5. Once the PRD is loaded internally, the IDE device will receive a DMA acknowledge.
6. The controller transfers data to/from memory responding to DMA requests from the IDE device. The IDE device and the host controller may or may not throttle the transfer several times. When the last data transfer for a region has been completed on the IDE interface, the next descriptor is fetched from the table. The descriptor contents are loaded into the Current Base and Current Count registers.
7. At the end of the transfer, the IDE device signals an interrupt.
8. In response to the interrupt, software resets the Start/Stop bit in the command register. It then reads the controller status followed by the drive status to determine if the transfer completed successfully.

The last PRD in a table has the End of List (EOL) bit set. The PCI Bus Master data transfers terminate when the physical region described by the last PRD in the table has been completely transferred. The active bit in the Status Register is reset and the DDRQ signal is masked.

The buffer is flushed (when in the write state) or invalidated (when in the read state) when a terminal count condition exists; that is, the current region descriptor has the EOL bit set and that region has been exhausted. The buffer is also flushed (write state) or invalidated (read state) when the Interrupt bit in the Bus Master IDE Status register is set. Software that reads the status register and finds the Error bit reset, and either the Active bit reset or the Interrupt bit set, can be assured that all data destined for system memory has been transferred and that data is valid in system memory. Table 5-59 describes how to interpret the Interrupt and Active bits in the Status Register after a DMA transfer has started.

Table 5-59. Interrupt/Active Bit Interaction Definition

Interrupt	Active	Description
0	1	DMA transfer is in progress. No interrupt has been generated by the IDE device.
1	0	The IDE device generated an interrupt. The controller exhausted the Physical Region Descriptors. This is the normal completion case where the size of the physical memory regions was equal to the IDE device transfer size.
1	1	The IDE device generated an interrupt. The controller has not reached the end of the physical memory regions. This is a valid completion case where the size of the physical memory regions was larger than the IDE device transfer size.
0	0	This bit combination signals an error condition. If the Error bit in the status register is set, then the controller has some problem transferring data to/from memory. Specifics of the error have to be determined using bus-specific information. If the Error bit is not set, then the PRD's specified a smaller size than the IDE transfer size.

5.17.2.5 Error Conditions

IDE devices are sector based mass storage devices. The drivers handle errors on a sector basis; either a sector is transferred successfully or it is not. A sector is 512 bytes.

If the IDE device does not complete the transfer due to a hardware or software error, the command will eventually be stopped by the driver setting Command Start bit to 0 when the driver times out the disk transaction. Information in the IDE device registers help isolate the cause of the problem.

If the controller encounters an error while doing the Bus Master transfers it will stop the transfer (that is, reset the Active bit in the Command register) and set the Error bit in the Bus Master IDE Status register. The controller does not generate an interrupt when this happens. The device driver can use device specific information (PCI Configuration Space Status register and IDE Drive Register) to determine what caused the error.

Whenever a requested transfer does not complete properly, information in the IDE device registers (Sector Count) can be used to determine how much of the transfer was completed and to construct a new PRD table to complete the requested operation. In most cases the existing PRD table can be used to complete the operation.

5.17.3 Ultra ATA/100/66/33 Protocol

The Intel® 631xESB/632xESB I/O Controller Hub supports Ultra ATA/100/66/33 Bus Mastering protocol, providing support for a variety of transfer speeds with IDE devices. Ultra ATA/33 provides transfers up to 33 MB/s, Ultra ATA/66 provides transfers at up to 44 MB/s or 66 MB/s, and Ultra ATA/100 can achieve read transfer rates up to 100 MB/s and write transfer rates up to 88.9 MB/s.

The Ultra ATA/100/66/33 definition also incorporates a Cyclic Redundancy Checking (CRC-16) error checking protocol.

5.17.3.1 Operation

Initial setup programming consists of enabling and performing the proper configuration of the Intel® 631xESB/632xESB I/O Controller Hub and the IDE device for Ultra ATA/100/66/33 operation. For the Intel® 631xESB/632xESB I/O Controller Hub, this consists of enabling synchronous DMA mode and setting up appropriate Synchronous DMA timings.

When ready to transfer data to or from an IDE device, the Bus Master IDE programming model is followed. Once programmed, the drive and Intel® 631xESB/632xESB I/O Controller Hub control the transfer of data by way of the Ultra ATA/100/66/33 protocol. The actual data transfer consists of three phases, a start-up phase, a data transfer phase, and a burst termination phase.

The IDE device begins the start-up phase by asserting DMARQ signal. When ready to begin the transfer, the Intel® 631xESB/632xESB I/O Controller Hub asserts DMACK# signal. When DMACK# signal is asserted, the host controller drives CS0# and CS1# inactive, DA0–DA2 low. For write cycles, the Intel® 631xESB/632xESB I/O Controller Hub deasserts STOP, waits for the IDE device to assert DMARDY#, and then drives the first data word and STROBE signal. For read cycles, the Intel® 631xESB/632xESB I/O Controller Hub tri-states the DD lines, deasserts STOP, and asserts DMARDY#. The IDE device then sends the first data word and STROBE.

The data transfer phase continues the burst transfers with the data transmitter (Intel® 631xESB/632xESB I/O Controller Hub – writes, IDE device – reads) providing data and toggling STROBE. Data is transferred (latched by receiver) on each rising and falling edge of STROBE. The transmitter can pause the burst by holding STROBE high or low, resuming the burst by again toggling STROBE. The receiver can pause the burst by deasserting DMARDY# and resumes the transfers by asserting DMARDY#. The Intel® 631xESB/632xESB I/O Controller Hub pauses a burst transaction to prevent an

internal line buffer over or under flow condition, resuming once the condition has cleared. It may also pause a transaction if the current PRD byte count has expired, resuming once it has fetched the next PRD.

The current burst can be terminated by either the transmitter or receiver. A burst termination consists of a Stop Request, Stop Acknowledge and transfer of CRC data. The Intel® 631xESB/632xESB I/O Controller Hub can stop a burst by asserting STOP, with the IDE device acknowledging by deasserting DMARQ. The IDE device stops a burst by deasserting DMARQ and the Intel® 631xESB/632xESB I/O Controller Hub acknowledges by asserting STOP. The transmitter then drives the STROBE signal to a high level. The Intel® 631xESB/632xESB I/O Controller Hub then drives the CRC value onto the DD lines and deassert DMACK#. The IDE device latches the CRC value on rising edge of DMACK#. The Intel® 631xESB/632xESB I/O Controller Hub terminates a burst transfer if it needs to service the opposite IDE channel, if a Programmed I/O (PIO) cycle is executed to the IDE channel currently running the burst, or upon transferring the last data from the final PRD.

5.17.4 Ultra ATA/33/66/100 Timing

The timings for Ultra ATA/33/66/100 modes are programmed by way of the Synchronous DMA Timing register and the IDE Configuration register. Different timings can be programmed for each drive in the system. The Base Clock frequency for each drive is selected in the IDE Configuration register. The Cycle Time (CT) and Ready to Pause (RP) time (defined as multiples of the Base Clock) are programmed in the Synchronous DMA Timing Register. The Cycle Time represents the minimum pulse width of the data strobe (STROBE) signal. The Ready to Pause time represents the number of Base Clock periods that the Intel® 631xESB/632xESB I/O Controller Hub waits from deassertion of DMARDY# to the assertion of STOP when it desires to stop a burst read transaction.

Note: The internal Base Clock for Ultra ATA/100 (Mode 5) runs at 133 MHz, and the Cycle Time (CT) must be set for three Base Clocks. The Intel® 631xESB/632xESB I/O Controller Hub thus toggles the write strobe signal every 22.5 ns, transferring two bytes of data on each strobe edge. This means that the Intel® 631xESB/632xESB I/O Controller Hub performs Mode 5 write transfers at a maximum rate of 88.9 MB/s. For read transfers, the read strobe is driven by the ATA/100 device, and the Intel® 631xESB/632xESB I/O Controller Hub supports reads at the maximum rate of 100 MB/s.

5.17.5 IDE Swap Bay

To support a swap bay, the Intel® 631xESB/632xESB I/O Controller Hub allows the IDE output signals to be tri-stated and input buffers to be turned off. This should be done prior to the removal of the drive. The output signals can also be driven low. This can be used to remove charge built up on the signals. Configuration bits are included in the IDE I/O Configuration register, offset 54h in the IDE PCI configuration space.

In an IDE Hot Swap Operation, an IDE device is removed and a new one inserted while the IDE interface is powered down and the rest of the system is in a fully powered-on state (SO). During an IDE Hot Swap, if the operating system executes cycles to the IDE interface after it has been powered down it will cause the Intel® 631xESB/632xESB I/O Controller Hub to hang the system that is waiting for IORDY to be asserted from the drive.

To correct this issue, the following BIOS procedures are required for performing an IDE hot swap:

1. Program IDE SIG_MODE (Configuration register at offset 54h) to 10b (drive low mode).
2. Clear IORDY Sample Point Enable (bits 1 or 5 of IDE Timing reg.). This prevents the Intel® 631xESB/632xESB I/O Controller Hub from waiting for IORDY assertion when the operating system accesses the IDE device after the IDE drive powers down, and ensures that 0s are always be returned for read cycles that occur during hot swap operation.

Warning: Software should **not** attempt to control the outputs (either tri-state or driving low), while an IDE transfer is in progress. Unpredictable results could occur, including a system lockup.

5.17.6 SMI Trapping

Device 31:Function 1: Offset C0h (see Section 22.1.26) contain control for generating SMI# on accesses to the IDE I/O spaces. These bits map to the legacy ranges (1F0–1F7h and 3F6h). Accesses to one of these ranges with the appropriate bit set causes the cycle to not be forwarded to the IDE controller, and for an SMI# to be generated. If an access to the Bus-Master IDE registers occurs while trapping is enabled for the device being accessed, then the register is updated, an SMI# is generated, and the device activity status bits (Device 31:Function 1:Offset C4h) are updated indicating that a trap occurred.

5.18 SATA Host Controller (D31:F2)

The Intel® 631xESB/632xESB I/O Controller Hub has an integrated SATA host controller that supports independent DMA operation on six ports and supports data transfer rates of up to 3.0 Gb/s (300 MB/s). The SATA host controller contains two modes of operation – a legacy mode using I/O space, and an AHCI mode using memory space. The memory space bit GHC.AE, set by software, indicates to hardware that AHCI is being used. Software must not implement code which mixes the use of legacy mode and AHCI mode.

When in combined function mode, where the SATA function is used with PATA, AHCI mode is not used. Software that uses legacy mode will not have AHCI capabilities, and therefore will not set GHC.AE.

5.18.1 Legacy Operation

In this mode of operation, software is performing I/O operations to the controller and SATA devices. The SATA controller is using the shadow registers as described in the SATA specification, and performing Master/Slave operation on the ports. Additionally, this mode of operation is used during combined mode, where the SATA function is shared with PATA.

Software must program the DEV bit in the task file as its first operation before programming the rest of the transfer or setting the bus Master registers.

5.18.1.1 Standard ATA Emulation

The Intel® 631xESB/632xESB I/O Controller Hub contains a set of registers that shadow the contents of the legacy IDE registers. The behavior of the Command and Control Block registers, PIO, and DMA data transfers, resets, and interrupts are all emulated.

5.18.1.2 48-Bit LBA Operation

The SATA host controller supports 48-bit LBA through the host-to-device register FIS when accesses are performed by way of writes to the task file. The SATA host controller will ensure that the correct data is put into the correct byte of the host-to-device FIS.

There are special considerations when reading from the task file to support 48-bit LBA operation. Software may need to read all 16-bits. Since the registers are only 8 bits wide and act as a FIFO, a bit must be set in the device/control register, which is at offset 3F6h for primary and 376h for secondary (or their native counterparts).

If software clears bit 7 of the control register before performing a read, the last item written will be returned from the FIFO. If software sets bit 7 of the control register before performing a read, the first item written will be returned from the FIFO.

5.18.1.3 Hot-Plug Operation

Dynamic Hot-Plug (for example, surprise removal) is not supported by the SATA host controller. However, using the PCS register configuration bits and power management flows, a device can be powered down by software, and the port can then be powered off, allowing removal and insertion of a new device.

Note: This Hot-Plug operation requires board hardware (implementation specific), BIOS, and operating system support.

5.18.1.4 Intel® RAID Technology Configuration

The Intel® RAID Technology solution offers data striping for higher performance (RAID Level 0), alleviating disk bottlenecks by taking advantage of the independent DMA engines that each SATA port offers in the Intel® 631xESB/632xESB I/O Controller Hub. Intel RAID Technology also offers mirroring for data security (RAID Level 1). There is no loss of PCI resources (request/grant pair) or add-in card slot.

Intel RAID Technology functionality requires the following items:

- Intel® 631xESB/632xESB I/O Controller Hub
- Intel RAID Technology Option ROM must be on the platform
- Intel® Application Accelerator RAID Edition drivers, most recent revision.
- Two SATA hard disk drives.

Intel RAID Technology is not available in the following configurations:

- The SATA controller in compatible mode.

5.18.1.5 Intel® RAID Technology Option ROM

The Intel RAID Technology for SATA Option ROM provides a pre-operating system user interface for the Intel RAID Technology implementation and provides the ability for an Intel RAID Technology volume to be used as a boot disk as well as to detect any faults in the Intel RAID Technology volume(s) attached to the Intel RAID controller.

5.18.1.6 Power Management Operation

Power management of the Intel® 631xESB/632xESB I/O Controller Hub SATA controller and ports will cover operations of the host controller and the SATA wire.

5.18.1.6.1 Power State Mappings

SATA devices may also have multiple power states. From parallel ATA, three device states are supported through ACPI. They are:

- **D0** – Device is working and instantly available.
- **D1** – device enters when it receives a STANDBY IMMEDIATE command. Exit latency from this state is in seconds.
- **D3** – from the SATA device's perspective, no different than a D1 state, in that it is entered by way of the STANDBY IMMEDIATE command. However, an ACPI method is also called which will reset the device and then cut its power.

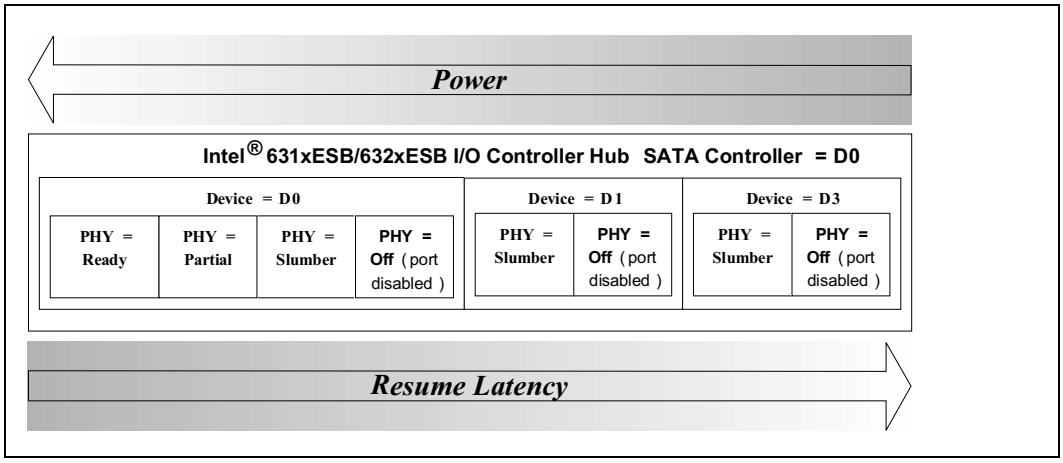
Each of these device states are subsets of the host controller's D0 state.

Finally, SATA defines three PHY layer power states, which have no equivalent mappings to parallel ATA. They are:

- **PHY READY** – PHY logic and PLL are both on and active.
- **Partial** – PHY logic is powered, but in a reduced state. Exit latency is no longer than 10 ns
- **Slumber** – PHY logic is powered, but in a reduced state. Exit latency can be up to 10 ms.

Since these states have much lower exit latency than the ACPI D1 and D3 states, the SATA controller defines these states as sub-states of the device D0 state.

Figure 5-19. SATA Power States



5.18.1.6.2 Power State Transitions

Partial and Slumber State Entry/Exit

The partial and slumber states save interface power when the interface is idle. The SATA controller defines PHY layer power management (as performed by way of primitives) as a driver operation from the host side, and a device proprietary mechanism on the device side. The SATA controller accepts device transition types, but does not issue any transitions as a host. All received requests from a SATA device will be ACKed.

When an operation is performed to the SATA controller such that it needs to use the SATA cable, the controller must check whether the link is in the Partial or Slumber states, and if so, must issue a COM_WAKE to bring the link back online. Similarly, the SATA device must perform the same action.

Device D1, D3 States

These states are entered after some period of time when software has determined that no commands will be sent to this device for some time. The mechanism for putting a device in these states does not involve any work on the host controller, other then sending commands over the interface to the device. The command most likely to be used in ATA/ATAPI is the “STANDBY IMMEDIATE” command.

5.18.1.7 SATA Interrupts

Table 5-60 summarizes interrupt behavior for MSI and wire-modes. In the table “bits” refers to the four possible interrupt bits in I/O space, which are: PSTS.PRDIS (offset 02h, bit 7), PSTS.I (offset 02h, bit 2), SSTS.PRDIS (offset 0Ah, bit 7), and SSTS.I (offset 0Ah, bit 2).

Table 5-60. SATA MSI vs. PCI IRQ Actions

Interrupt Register	Wire-Mode Action	MSI Action
All bits are 0	Wire Inactive	No Action
One or more bits set to 1	Wire Active	Send Message
One or more bits set to 1, new bit gets set to 1	Wire Active	Send Message
One or more bits set to 1, software clears some (but not all) bits	Wire Active	Send Message
One or more bits set to 1, software clears all bits	Wire Inactive	No Action
Software clears one or more bits, and one or more bits is set simultaneously	Wire Active	Send Message

5.18.1.8 SATA LED

The SATALED# output is driven whenever the BSY bit is set in any SATA port. The SATALED# is an active-low open-collector output. When SATALED# is low, the LED should be active. When SATALED# is tri-stated, the LED should be inactive.

5.18.2 AHCI Operation

The Intel® 631xESB/632xESB I/O Controller Hub provide hardware support for Advanced Host Controller Interface (AHCI), a new programming interface for SATA host controllers developed through a joint industry effort. AHCI defines transactions between the SATA controller and software and enables advanced performance and usability with SATA. Platforms supporting AHCI may take advantage of performance features such as no Master/Slave designation for SATA devices – each device is treated as a Master – and hardware assisted Native Command Queuing (NCQ). AHCI also provides usability enhancements such as Hot-Plug. AHCI requires appropriate software support (for example, an AHCI driver) and for some features, hardware support in the SATA device or additional platform hardware.

The Intel® 631xESB/632xESB I/O Controller Hub supports all of the mandatory features of the *Serial ATA Advanced Host Controller Interface (AHCI) Specification, Revision 1.0* and many optional features, such as hardware assisted Native Command

Queuing (NCQ), aggressive power management, LED indicator support, and Hot-Plug through the use of interlock switch support (additional platform hardware and software may be required depending upon the implementation).

Note: For reliable device removal notification while in AHCI operation without the use of interlock switches (surprise removal), interface power management should be disabled for the associated port. See section 7.3.1 of the AHCI Specification for more information.

5.18.2.1 Data Transfer Operation

Refer to Chapter 5 of the AHCI specification for details.

5.18.2.2 Error Reporting and Recovery

Refer to Chapter 6 of the AHCI specification for details.

5.18.2.3 Hot-Plug Operation

Refer to Chapter 7 of the AHCI specification for details.

Intel® 631xESB/632xESB I/O Controller Hub supports Hot-Plug Surprise Removal Notification. However Hot-Plug Surprise Removal Notification (without an interlock switch) is mutually exclusive with the PARTIAL and SLUMBER power management states. The following conceptual flows describe the different software initialization steps necessary to support Surprise Removal Notification or Power Management.

5.18.2.3.1 Per Port Software Initialization to Support Surprise Insertion and Removal Notification:

1. Set PxSCTL.IPM to 3h to disable both PARTIAL and SLUMBER transitions invoked by the drive.
2. Set PxCMD.ALPE to 0 to disable aggressive power management by the HBA.
3. Set PxIE.PCE to 1 to enable interrupts for Hot-Plug insertions.
4. The PxIS.PCS interrupt status bit indicates to software that a Hot-Plug insertion event occurred.
5. Write a 1 to the PxSERR.DIAG.X bit to clear it and the PxIS.PCS bit.

After a drive is detected on the port:

6. Set the newly defined PxIE.PRCE to 1 to enable interrupts for Hot-Plug removals.
7. Issue the Set Features command to the drive to disable interface power management.
8. The newly defined PxIS.PRCS interrupt status bit indicates to software that a Hot-Plug removal event occurred.
9. Set the PxIE.PRCE to 0 to disable interrupts so that only the PxIS.PCS bit will generate an insertion event interrupt. If this bit is left enabled two interrupts may be generated on the insertion event.

5.18.2.3.2 Per Port Software Initialization to Support PARTIAL and SLUMBER Power Management:

1. Set PxSCTL.IPM to 0h to enable PARTIAL and SLUMBER transitions for the HBA port.
2. Set PxCMD.ALPE and PxCMD.ASP appropriately based on aggressive power management policy.

3. Set PxIE.PRCE to 0 to disable interrupts when PhyRdy changes state due to PARTIAL and SLUMBER transitions.
4. During active operation PxSSTS.DET = 3h indicates to software that the link is operational.

5.18.2.4 Power Management Operation

Refer to Chapter 8 of the AHCI specification for details.

5.18.2.5 SATA LED Driving Capability

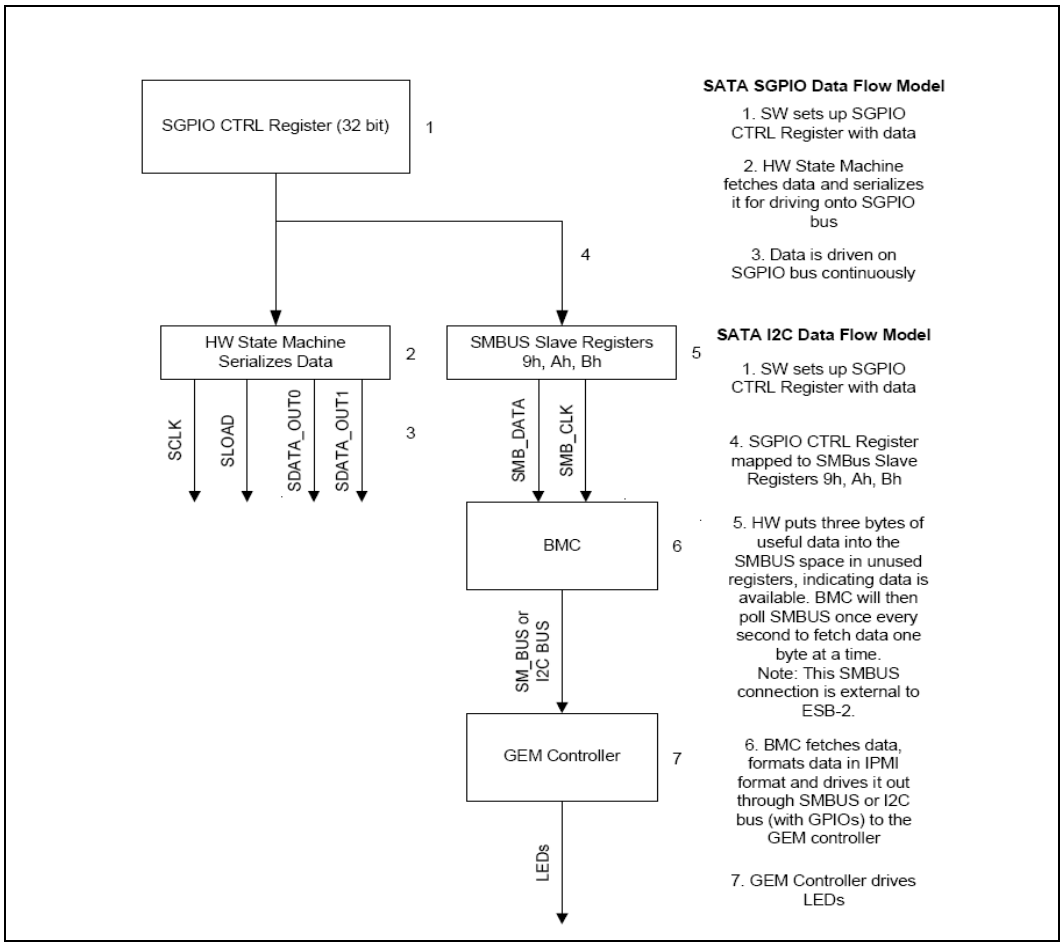
In RAID subsystems it is required to drive up to four output signals per device. These signals are:

1. Activity: indicates whether the drive is processing a command or is idle
2. Fault: indicates whether a drive currently is failing
3. Locate: indicates to an operator where to insert a drive or where to remove a drive from
4. Rebuild: indicates whether a drive that is currently being rebuilt

Typically the activity, fault and locate signals are shown as separate LEDs for each drive slot. The rebuild signal often results in the fault light being illuminated with a different color.

Intel® 631xESB/632xESB I/O Controller Hub supports driving LEDs through the SGPIO interface and the I2C interface. Figure 5-20 shows the data flow model for SATA SGPIO and SATA I2C schemes.

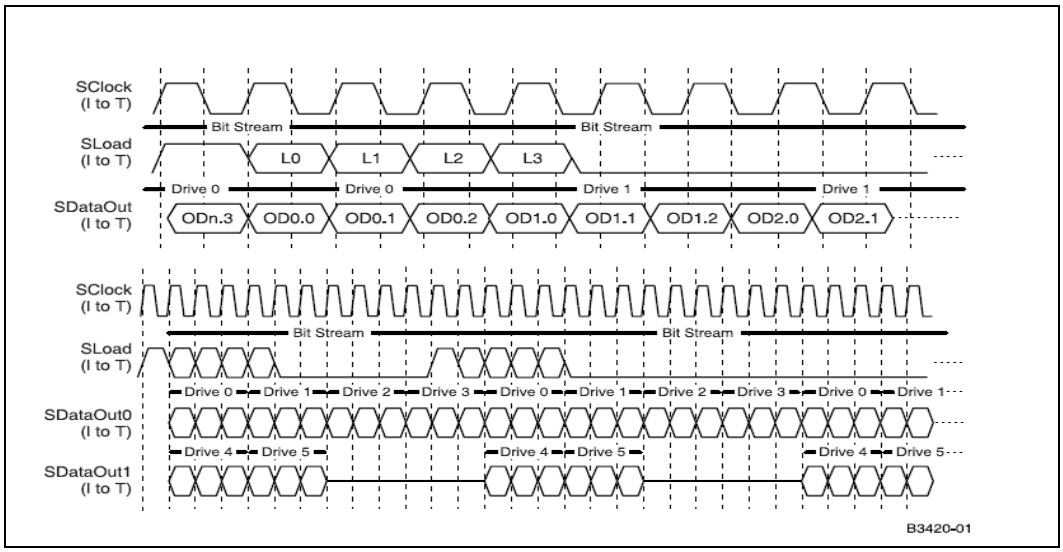
Figure 5-20. SATA Data Flow Model



When the SGPIO interface is used, a single 32-bit register (SGPIO control register) at offset A0h within AHCI Vendor Specific Range is used. Refer to EDS Volume 3, Section 23.3.1.6 for details of the SGPIO Control register. It is the responsibility of software to drive the data into this register. The data is comprised of three bits per drive. The bits may indicate activity, fault, locate and rebuild LED values to drive for each drive. If the activity LED is driven from the drive directly, then the three bits indicate only fault, locate and rebuild LEDs. Note that issues such as blink rate of LEDs are handled by the SGPIO target. That information is not included in the SGPIO control register.

Hardware reads the data from SGPIO Control register, serializes the data and drives the data out onto the four SGPIO pins. The four pins are SCLK, SLOAD, SDATAOUT0 and SDATAOUT1. Note that because software may change the data asynchronously with respect to the SGPIO bus clock, it is the responsibility of the hardware to make sure the data values are driven out correctly onto the SGPIO bus. Hardware updates the SGPIO data, after software changes it, only at the next available SLOAD change so the data driven onto SGPIO is not corrupted. The SGPIO clock frequency is 32 kHz. The four bits of Vendor Specific Messages are driven in the cycle immediately following SLOAD assertion. SDATAOUT0 drives out the data stream continuously from bit 4 to bit 15 (data to be driven out for drive 0, drive1, drive 2 and drive 3) of the SGPIO register and this process is repeated. SDATAOUT1 drives out the data stream continuously from bit 16 to bit 21 (data to be driven out for drive 4 and drive 5), then followed by six bits of zeros and this process repeated. This is shown in Figure 5-21.

Figure 5-21. SGPIO Signal Relationships



For the I^{2}C approach, the SGPIO Control Register is made visible in the SMBus Slave register space. SGPIO control register is mapped to SMBus Slave registers at offset 9h, Ah and Bh. The SM Link interface is externally connected to an unused SMBus on the BMC. BMC will read the data, encapsulate it in the IPMI format and drive that data through another SMBus or I2C bus to the GEM controller. GEM controller then updates the LED drivers with the updated status.

5.19 High-Precision Event Timers

This function provides a set of timers that can be used by the operating system. The timers are defined such that in the future, the operating system may be able to assign specific timers to be used directly by specific applications. Each timer can be configured to cause a separate interrupt.

Intel® 631xESB/632xESB I/O Controller Hub provides three timers. The three timers are implemented as a single counter each with its own comparator and value register. This counter increases monotonically. Each individual timer can generate an interrupt when the value in its value register matches the value in the main counter.

The registers associated with these timers are mapped to a memory space (much like the I/O APIC). However, it is not implemented as a standard PCI function. The BIOS reports to the operating system the location of the register space. The hardware can support an assignable decode space; however, the BIOS sets this space prior to handing it over to the operating system (See Section 11.5). It is not expected that the operating system will move the location of these timers once it is set by the BIOS.

Intel® 631xESB/632xESB I/O Controller Hub Specific Information

- This logic has not appeared in any prior Intel chipset.
- In the Intel® 631xESB/632xESB I/O Controller Hub, one timer block is implemented. The timer block has one counter-3 timers (comparators). Future devices may have a different number of implemented timers. Various capabilities registers indicate the number of timers and the capabilities of each.

5.19.1 Timer Accuracy

- The timers are accurate over any 1 ms period to within 0.05% of the time specified in the timer resolution fields.
- Within any 100 microsecond period, the timer reports a time that is up to two ticks too early or too late. Each tick is less than or equal to 100 ns, so this represents an error of less than 0.2%.
- The timer is monotonic. It does not return the same value on two consecutive reads (unless the counter has rolled over and reached the same value).
- The main counter is clocked by the 14.31818 MHz clock, synchronized into the 125 MHz domain. This results in a non-uniform duty cycle on the synchronized clock, but does have the correct average period. The accuracy of the main counter is as accurate as the 14.3818 MHz clock.

5.19.2 Interrupt Mapping

Mapping Option #1 (Legacy Replacement Option)

In this case, the Legacy Replacement Rout bit (LEG_RT_CNF) is set. This forces the mapping found in Table 5-61.

Table 5-61. Legacy Replacement Routing

Timer	8259 Mapping	APIC Mapping	Comment
0	IRQ0	IRQ2	In this case, the 8254 timer will not cause any interrupts
1	IRQ8	IRQ8	In this case, the RTC will not cause any interrupts.
2	Per IRQ Routing Field	Per IRQ Routing Field	

Mapping Option #2 (Standard Option)

In this case, the Legacy Replacement Rout bit (LEG_RT_CNF) is 0. Each timer has its own routing control. The supported interrupt values are IRQ 20, 21, 22, and 23.

5.19.3 Periodic Versus Non-Periodic Modes

Non-Periodic Mode

Timer 0 is configurable to 32 (default) or 64-bit mode, whereas Timers 1 and 2 support only 32-bit mode (See Section 26.1.5).

All three timers support non-periodic mode.

Consult section 2.3.9.2.1 of the IA-PC HPET Specification for a description of this mode.

Periodic Mode

Timer 0 is the only timer that supports periodic mode. Consult section 2.3.9.2.2 of the IA-PC HPET Specification for a description of this mode.

The following usage model is expected:

1. Software clears the ENABLE_CNF bit to prevent any interrupts
2. Software Clears the main counter by writing a value of 00h to it.

3. Software sets the TIMER0_VAL_SET_CNF bit.
4. Software writes the new value in the TIMER0_COMPARATOR_VAL register.
5. Software sets the ENABLE_CNF bit to enable interrupts.

The Timer 0 Comparator Value register cannot be programmed reliably by a single 64-bit write in a 32-bit environment except if only the periodic rate is being changed during run-time. If the actual Timer 0 Comparator Value needs to be reinitialized, then the following software solution will always work regardless of the environment:

1. Set TIMER0_VAL_SET_CNF bit.
2. Set the lower 32 bits of the Timer0 Comparator Value register.
3. Set TIMER0_VAL_SET_CNF bit.
4. Set the upper 32 bits of the Timer0 Comparator Value register.

5.19.4 Enabling the Timers

The BIOS or operating system PnP code should route the interrupts. This includes the Legacy Rout bit, Interrupt Rout bit (for each timer), interrupt type (to select the edge or level type for each timer)

The Device Driver code should do the following for an available timer:

1. Set the Overall Enable bit (Offset 04h, bit 0).
2. Set the timer type field (selects one-shot or periodic).
3. Set the interrupt enable.
4. Set the comparator value.

5.19.5 Interrupt Levels

Interrupts directed to the internal 8259s are active high. See Section 5.11 for information regarding the polarity programming of the I/O APIC for detecting internal interrupts.

If the interrupts are mapped to the I/O APIC and set for level-triggered mode, they can be shared with PCI interrupts. This may be shared although it's unlikely for the operating system to attempt to do this.

If more than one timer is configured to share the same IRQ (using the TIMERn_INT_ROUT_CNF fields), then the software must configure the timers to level-triggered mode. Edge-triggered interrupts cannot be shared.

5.19.6 Handling Interrupts

If each timer has a unique interrupt and the timer has been configured for edge-triggered mode, then there are no specific steps required. No read is required to process the interrupt.

If a timer has been configured to level-triggered mode, then its interrupt must be cleared by the software. This is done by reading the interrupt status register and writing a 1 back to the bit position for the interrupt to be cleared.

Independent of the mode, software can read the value in the main counter to see how time has passed between when the interrupt was generated and when it was first serviced.

If Timer 0 is set up to generate a periodic interrupt, the software can check to see how much time remains until the next interrupt by checking the timer value register.

5.19.7 Issues Related to 64-Bit Timers with 32-Bit Processors

A 32-bit timer can be read directly using processors that are capable of 32-bit or 64-bit instructions. However, a 32-bit processor may not be able to directly read 64-bit timer. A race condition comes up if a 32-bit processor reads the 64-bit register using two separate 32-bit reads. The danger is that just after reading one half, the other half rolls over and changes the first half.

If a 32-bit processor needs to access a 64-bit timer, it must first halt the timer before reading both the upper and lower 32-bits of the timer. If a 32-bit processor does not want to halt the timer, it can use the 64-bit timer as a 32-bit timer by setting the TIMERn_32MODE_CNF bit. This causes the timer to behave as a 32-bit timer. The upper 32-bits are always 0.

5.20 USB UHCI Host Controllers (D29:F0, F1, F2, and F3)

The Intel® 631xESB/632xESB I/O Controller Hub contains four USB 2.0 full/low-speed host controllers that support the standard Universal Host Controller Interface (UHCI), Revision 1.1. Each UHCI Host Controller (UHC) includes a root hub with two separate USB ports each, for a total of eight USB ports.

- Overcurrent detection on all eight USB ports is supported. The overcurrent inputs are not 5 V tolerant, and can be used as GPIs if not needed.
- The Intel® 631xESB/632xESB I/O Controller Hub's UHCI host controllers are arbitrated differently than standard PCI devices to improve arbitration latency.
- The UHCI controllers use the Analog Front End (AFE) embedded cell that allows support for USB full-speed signaling rates, instead of USB I/O buffers.

Note: New in Intel® 631xESB/632xESB I/O Controller Hub:

- New Manufacturer and Device ID for the USB controllers
- Trusted USB Port
- Dynamic Bus Mastering signals to the Power Management logic to properly indicate when memory accesses are pending.
- Updated Interrupt Pin reporting scheme
- Overcurrent pins are no longer 5 V tolerant. These I/O buffers are reduced to 3.3 V tolerance.

5.20.1 Data Structures in Main Memory

Section 3.1 - 3.3 of the *Universal Host Controller Interface, Revision 1.1* details the data structures used to communicate control, status, and data between software and the Intel® 631xESB/632xESB I/O Controller Hub.

5.20.2 Data Transfers to/from Main Memory

Section 3.4 of the *Universal Host Controller Interface, Revision 1.1* describes the details on how HCD and the Intel® 631xESB/632xESB I/O Controller Hub communicate by way of the Schedule data structures.

5.20.3 Data Encoding and Bit Stuffing

The Intel® 631xESB/632xESB I/O Controller Hub USB employs NRZI data encoding (Non-Return to Zero Inverted) when transmitting packets. Full details on this implementation are given in the *Universal Serial Bus Revision 2.0 Specification.*

5.20.4 Bus Protocol

5.20.4.1 Bit Ordering

Bits are sent out onto the bus least significant bit (LSb) first, followed by next LSb, through to the most significant bit (MSb) last.

5.20.4.2 SYNC Field

All packets begin with a synchronization (SYNC) field, which is a coded sequence that generates a maximum edge transition density. The SYNC field appears on the bus as IDLE followed by the binary string “KJKJKJKK,” in its NRZI encoding. It is used by the input circuitry to align incoming data with the local clock and is defined to be 8 bits in length. SYNC serves only as a synchronization mechanism and is not shown in the following packet diagrams. The last two bits in the SYNC field are a marker that is used to identify the first bit of the PID. All subsequent bits in the packet must be indexed from this point.

5.20.4.3 Packet Field Formats

All packets have distinct start and end of packet delimiters. Full details are given in the *Universal Serial Bus Revision 2.0 Specification* in section 8.3.1.

5.20.4.4 Address Fields

Function endpoints are addressed using the function address field and the endpoint field. Full details on this are given in the *Universal Serial Bus Revision 2.0 Specification* in section 8.3.2.

5.20.4.5 Frame Number Field

The frame number field is an 11-bit field that is incremented by the host on a per frame basis. The frame number field rolls over upon reaching its maximum value of 7FFh, and is sent only for SOF tokens at the start of each frame.

5.20.4.6 Data Field

The data field may range from 0 to 1023 bytes and must be an integral numbers of bytes. Data bits within each byte are shifted out LSB first.

5.20.4.7 Cyclic Redundancy Check (CRC)

CRC is used to protect the all non-PID fields in token and data packets. In this context, these fields are considered to be protected fields. Full details on this are given in the *Universal Serial Bus Revision 2.0 Specification* in section 8.3.5.

5.20.5 Packet Formats

The USB protocol calls out several packet types: token, data, and handshake packets. Full details on this are given in the *Universal Serial Bus Revision 2.0 Specification* in section 8.4.

5.20.6 USB Interrupts

There are two general groups of USB interrupt sources, those resulting from execution of transactions in the schedule, and those resulting from an Intel® 631xESB/632xESB I/O Controller Hub operation error. All transaction-based sources can be masked by software through the Intel® 631xESB/632xESB I/O Controller Hub's Interrupt Enable register. Additionally, individual transfer descriptors can be marked to generate an interrupt on completion.

When the Intel® 631xESB/632xESB I/O Controller Hub drives an interrupt for USB, it internally drives the PIRQA# pin for USB function #0 and USB function #3, PIRQD# pin for USB function #1, and the PIRQC# pin for USB function #2, until all sources of the interrupt are cleared. In order to accommodate some operating systems, the Interrupt Pin register must contain a different value for each function of this new multi-function device.

5.20.6.1 Transaction Based Interrupts

These interrupts are not signaled until after the status for the last complete transaction in the frame has been written back to host memory. This guarantees that software can safely process through (Frame List Current Index -1) when it is servicing an interrupt.

CRC Error / Time-Out

A CRC/Time-Out error occurs when a packet transmitted from the Intel® 631xESB/632xESB I/O Controller Hub to a USB device or a packet transmitted from a USB device to the Intel® 631xESB/632xESB I/O Controller Hub generates a CRC error. The Intel® 631xESB/632xESB I/O Controller Hub is informed of this event by a time-out from the USB device or by the Intel® 631xESB/632xESB I/O Controller Hub's CRC checker generating an error on reception of the packet. Additionally, a USB bus time-out occurs when USB devices do not respond to a transaction phase within 19-bit times of an EOP. Either of these conditions causes the C_ERR field of the TD to decrement.

When the C_ERR field decrements to 0, the following occurs:

- The Active bit in the TD is cleared.
- The Stalled bit in the TD is set.
- The CRC/Time-out bit in the TD is set.
- At the end of the frame, the USB Error Interrupt bit is set in the HC status register.

If the CRC/Time out interrupt is enabled in the Interrupt Enable register, a hardware interrupt will be signaled to the system.

Interrupt on Completion

Transfer Descriptors contain a bit that can be set to cause an interrupt on their completion. The completion of the transaction associated with that block causes the USB Interrupt bit in the HC Status Register to be set at the end of the frame in which

the transfer completed. When a TD is encountered with the IOC bit set to 1, the IOC bit in the HC Status register is set to 1 at the end of the frame if the active bit in the TD is set to 0 (even if it was set to 0 when initially read).

If the IOC Enable bit of Interrupt Enable register (bit 2 of I/O offset 04h) is set, a hardware interrupt is signaled to the system. The USB Interrupt bit in the HC status register is set either when the TD completes successfully or because of errors. If the completion is because of errors, the USB Error bit in the HC status register is also set.

Short Packet Detect

A transfer set is a collection of data which requires more than one USB transaction to completely move the data across the USB. An example might be a large print file which requires numerous TDs in multiple frames to completely transfer the data. Reception of a data packet that is less than the endpoint's Max Packet size during Control, Bulk or Interrupt transfers signals the completion of the transfer set, even if there are active TDs remaining for this transfer set. Setting the SPD bit in a TD indicates to the HC to set the USB Interrupt bit in the HC status register at the end of the frame in which this event occurs. This feature streamlines the processing of input on these transfer types. If the Short Packet Interrupt Enable bit in the Interrupt Enable register is set, a hardware interrupt is signaled to the system at the end of the frame where the event occurred.

Serial Bus Babble

When a device transmits on the USB for a time greater than its assigned Max Length, it is said to be babbling. Since isochrony can be destroyed by a babbling device, this error results in the Active bit in the TD being cleared to 0 and the Stalled and Babble bits being set to one. The C_ERR field is not decremented for a babble. The USB Error Interrupt bit in the HC Status register is set to 1 at the end of the frame. A hardware interrupt is signaled to the system.

If an EOF babble was caused by the Intel® 631xESB/632xESB I/O Controller Hub (due to incorrect schedule for instance), the Intel® 631xESB/632xESB I/O Controller Hub forces a bit stuff error followed by an EOP and the start of the next frame.

Stalled

This event indicates that a device/endpoint returned a STALL handshake during a transaction or that the transaction ended in an error condition. The TDs Stalled bit is set and the Active bit is cleared. Reception of a STALL does not decrement the error counter. A hardware interrupt is signaled to the system.

Data Buffer Error

This event indicates that an overrun of incoming data or a under-run of outgoing data has occurred for this transaction. This would generally be caused by the Intel® 631xESB/632xESB I/O Controller Hub not being able to access required data buffers in memory within necessary latency requirements. Either of these conditions causes the C_ERR field of the TD to be decremented.

When C_ERR decrements to 0, the Active bit in the TD is cleared, the Stalled bit is set, the USB Error Interrupt bit in the HC Status register is set to 1 at the end of the frame and a hardware interrupt is signaled to the system.

Bit Stuff Error

A bit stuff error results from the detection of a sequence of more that six 1s in a row within the incoming data stream. This causes the C_ERR field of the TD to be decremented. When the C_ERR field decrements to 0, the Active bit in the TD is cleared to 0, the Stalled bit is set to 1, the USB Error Interrupt bit in the HC Status register is set to 1 at the end of the frame and a hardware interrupt is signaled to the system.

5.20.6.2 Non-Transaction-Based Interrupts

If an Intel® 631xESB/632xESB I/O Controller Hub process error or system error occur, the Intel® 631xESB/632xESB I/O Controller Hub halts and immediately issues a hardware interrupt to the system.

Resume Received

This event indicates that the Intel® 631xESB/632xESB I/O Controller Hub received a RESUME signal from a device on the USB bus during a global suspend. If this interrupt is enabled in the Interrupt Enable register, a hardware interrupt is signaled to the system allowing the USB to be brought out of the suspend state and returned to normal operation.

Intel® 631xESB/632xESB I/O Controller Hub Process Error

The HC monitors certain critical fields during operation to ensure that it does not process corrupted data structures. These include checking for a valid PID and verifying that the MaxLength field is less than 1280. If it detects a condition that would indicate that it is processing corrupted data structures, it immediately halts processing, sets the HC Process Error bit in the HC Status register and signals a hardware interrupt to the system.

This interrupt cannot be disabled through the Interrupt Enable register.

Host System Error

The Intel® 631xESB/632xESB I/O Controller Hub sets this bit to 1 when a Parity error, Master Abort, or Target Abort occur. When this error occurs, the Intel® 631xESB/632xESB I/O Controller Hub clears the Run/Stop bit in the Command register to prevent further execution of the scheduled TDs. This interrupt cannot be disabled through the Interrupt Enable register.

5.20.7 USB Power Management

The Host controller can be put into a suspended state and its power can be removed. This requires that certain bits of information are retained in the resume power plane of the Intel® 631xESB/632xESB I/O Controller Hub so that a device on a port may wake the system. Such a device may be a fax-modem, which will wake up the machine to receive a fax or take a voice message. The settings of the following bits in I/O space will be maintained when the Intel® 631xESB/632xESB I/O Controller Hub enters the S3, S4, or S5 states.

Table 5-62. Bits Maintained in Low Power States

Register	Offset	Bit	Description
Command	00h	3	Enter Global Suspend Mode (EGSM)
Status	02h	2	Resume Detect
Port Status and Control	10h & 12h	2	Port Enabled/Disabled
		6	Resume Detect
		8	Low-speed Device Attached
		12	Suspend

When the Intel® 631xESB/632xESB I/O Controller Hub detects a resume event on any of its ports, it sets the corresponding USB_STS bit in ACPI space. If USB is enabled as a wake/break event, the system wakes up and an SCI generated.

5.20.8 USB Legacy Keyboard Operation

When a USB keyboard is plugged into the system, and a standard keyboard is not, the system may not boot, and MS-DOS legacy software will not run, because the keyboard will not be identified. The Intel® 631xESB/632xESB I/O Controller Hub implements a series of trapping operations which will snoop accesses that go to the keyboard controller, and put the expected data from the USB keyboard into the keyboard controller.

Note: The scheme described below assumes a keyboard controller (8042 or equivalent) on the LPC bus.

This legacy operation is performed through SMM space. Figure 5-22 shows the Enable and Status path. The latched SMI source (60R, 60W, 64R, 64W) is available in the Status Register. Because the enable is after the latch, it is possible to check for other events that didn't necessarily cause an SMI. It is the software's responsibility to logically AND the value with the appropriate enable bits.

Note also that the SMI is generated before the PCI cycle completes (for example, before TRDY# goes active) to ensure that the processor doesn't complete the cycle before the SMI is observed. This method is used on MPIIX and has been validated.

The logic also needs to block the accesses to the 8042. If there is an external 8042, then this is simply accomplished by not activating the 8042 CS. This is simply done by logically ANDing the four enables (60R, 60W, 64R, 64W) with the 4 types of accesses to determine if 8042CS should go active. An additional term is required for the “pass-through” case.

The state table for the diagram is shown in Table 5-63.

Figure 5-22. USB Legacy Keyboard Flow Diagram

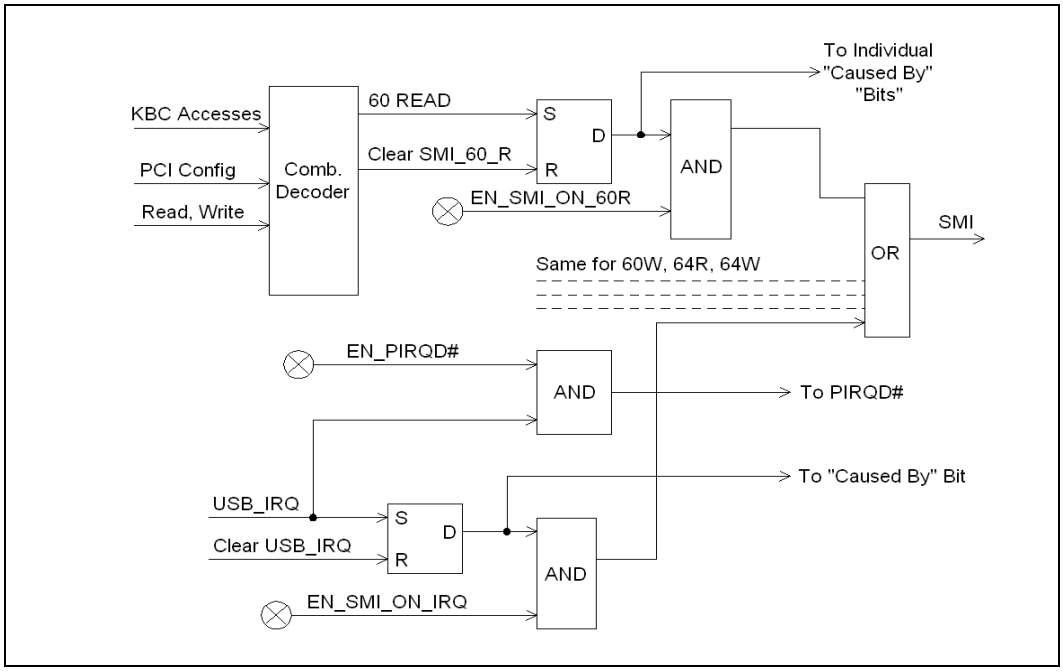


Table 5-63. USB Legacy Keyboard State Transitions

Current State	Action	Data Value	Next State	Comment
IDLE	64h / Write	D1h	GateState1	Standard D1 command. Cycle passed through to 8042. SMI# doesn't go active. PSTATE (offset C0, bit 6) goes to 1.
IDLE	64h / Write	Not D1h	IDLE	Bit 3 in Config Register determines if cycle passed through to 8042 and if SMI# generated.
IDLE	64h / Read	N/A	IDLE	Bit 2 in Config Register determines if cycle passed through to 8042 and if SMI# generated.
IDLE	60h / Write	Don't Care	IDLE	Bit 1 in Config Register determines if cycle passed through to 8042 and if SMI# generated.
IDLE	60h / Read	N/A	IDLE	Bit 0 in Config Register determines if cycle passed through to 8042 and if SMI# generated.
GateState1	60h / Write	XXh	GateState2	Cycle passed through to 8042, even if trap enabled in Bit 1 in Config Register. No SMI# generated. PSTATE remains 1. If data value is not DFh or DDh then the 8042 may chose to ignore it.
GateState1	64h / Write	D1h	GateState1	Cycle passed through to 8042, even if trap enabled by way of Bit 3 in Config Register. No SMI# generated. PSTATE remains 1. Stay in GateState1 because this is part of the double-trigger sequence.
GateState1	64h / Write	Not D1h	ILDE	Bit 3 in Config space determines if cycle passed through to 8042 and if SMI# generated. PSTATE goes to 0. If Bit 7 in Config Register is set, then SMI# should be generated.
GateState1	60h / Read	N/A	IDLE	This is an invalid sequence. Bit 0 in Config Register determines if cycle passed through to 8042 and if SMI# generated. PSTATE goes to 0. If Bit 7 in Config Register is set, then SMI# should be generated.
GateState1	64h / Read	N/A	GateState1	Just stay in same state. Generate an SMI# if enabled in Bit 2 of Config Register. PSTATE remains 1.
GateState2	64 / Write	FFh	IDLE	Standard end of sequence. Cycle passed through to 8042. PSTATE goes to 0. Bit 7 in Config Space determines if SMI# should be generated.
GateState2	64h / Write	Not FFh	IDLE	Improper end of sequence. Bit 3 in Config Register determines if cycle passed through to 8042 and if SMI# generated. PSTATE goes to 0. If Bit 7 in Config Register is set, then SMI# should be generated.
GateState2	64h / Read	N/A	GateState2	Just stay in same state. Generate an SMI# if enabled in Bit 2 of Config Register. PSTATE remains 1.
GateState2	60h / Write	XXh	IDLE	Improper end of sequence. Bit 1 in Config Register determines if cycle passed through to 8042 and if SMI# generated. PSTATE goes to 0. If Bit 7 in Config Register is set, then SMI# should be generated.
GateState2	60h / Read	N/A	IDLE	Improper end of sequence. Bit 0 in Config Register determines if cycle passed through to 8042 and if SMI# generated. PSTATE goes to 0. If Bit 7 in Config Register is set, then SMI# should be generated.

5.21 USB EHCI Host Controller (D29:F7)

The Intel® 631xESB/632xESB I/O Controller Hub contains an Enhanced Host Controller Interface (EHCI) compliant host controller which supports up to eight USB 2.0 high-speed compliant root ports. USB 2.0 allows data transfers up to 480 Mb/s using the same pins as the eight USB full-speed/low-speed ports. The Intel® 631xESB/632xESB I/O Controller Hub contains port-routing logic that determines whether a USB port is controlled by one of the UHCI controllers or by the EHCI controller. USB 2.0 based Debug Port is also implemented in the Intel® 631xESB/632xESB I/O Controller Hub.

A summary of the key architectural differences between the USB UHCI host controllers and the EHCI host controller are shown in Table 5-64.

Table 5-64. UHCI vs. EHCI

Parameter	USB UHCI	USB EHCI
Accessible by	I/O space	Memory Space
Memory Data Structure	Single linked list	Separated in to Periodic and Asynchronous lists
Differential Signaling Voltage	3.3 V	400 mV
Ports per Controller	2	8

5.21.1 EHC Initialization

The following descriptions step through the expected Intel® 631xESB/632xESB I/O Controller Hub Enhanced Host Controller (EHC) initialization sequence in chronological order, beginning with a complete power cycle in which the suspend well and core well have been off.

5.21.1.1 BIOS Initialization

BIOS performs a number of platform customization steps after the core well has powered up. Contact your Intel Field Representative for additional Intel® 631xESB/632xESB I/O Controller Hub BIOS information.

5.21.1.2 Driver Initialization

See Chapter 4 of the *Enhanced Host Controller Interface Specification for Universal Serial Bus, Revision 1.0*.

5.21.1.3 EHC Resets

In addition to the standard Intel® 631xESB/632xESB I/O Controller Hub hardware resets, portions of the EHC are reset by the HCRESET bit and the transition from the D3hot device power management state to the D0 state. The effects of each of these resets are:

Reset	Does Reset	Does not Reset	Comments
HCRESET bit set.	Memory space registers except Structural Parameters (which is written by BIOS).	Configuration registers.	The HCRESET must affect only registers that the EHCI driver controls. PCI Configuration space and BIOS-programmed parameters can not be reset.
Software writes the Device Power State from D3hot (11b) to D0 (00b).	Core well registers (except BIOS-programmed registers).	Suspend well registers; BIOS-programmed core well registers.	The D3-to-D0 transition must not cause wake information (suspend well) to be lost. It also must not clear BIOS-programmed registers because BIOS may not be invoked following the D3-to-D0 transition.

If the detailed register descriptions give exceptions to these rules, those exceptions override these rules. This summary is provided to help explain the reasons for the reset policies.

5.21.2 Data Structures in Main Memory

See Section 3 and Appendix B of the *Enhanced Host Controller Interface Specification for Universal Serial Bus, Revision 1.0* for details.

5.21.3 USB 2.0 Enhanced Host Controller DMA

The Intel® 631xESB/632xESB I/O Controller Hub USB 2.0 EHC implements three sources of USB packets. They are, in order of priority on USB during each microframe, 1) the USB 2.0 Debug Port (see Section 5.21.10), 2) the Periodic DMA engine, and 3) the Asynchronous DMA engine. The Intel® 631xESB/632xESB I/O Controller Hub always performs any currently-pending debug port transaction at the beginning of a microframe, followed by any pending periodic traffic for the current microframe. If there is time left in the microframe, then the EHC performs any pending asynchronous traffic until the end of the microframe (EOF1). Note that the debug port traffic is presented only on one port (Port #0), while the other ports are idle during this time.

5.21.4 Data Encoding and Bit Stuffing

See Chapter 8 of the *Universal Serial Bus Revision 2.0 Specification.*

5.21.5 Packet Formats

See Chapter 8 of the *Universal Serial Bus Revision 2.0 Specification*.

5.21.6 USB 2.0 Interrupts and Error Conditions

Section 4 of the *Enhanced Host Controller Interface Specification for Universal Serial Bus, Revision 1.0* goes into detail on the EHC interrupts and the error conditions that cause them. All error conditions that the EHC detects can be reported through the EHCI Interrupt status bits. Only Intel® 631xESB/632xESB I/O Controller Hub-specific

interrupt and error-reporting behavior is documented in this section. The EHCI Interrupts Section must be read first, followed by this section of the datasheet to fully comprehend the EHC interrupt and error-reporting functionality.

- Based on the EHC's Buffer sizes and buffer management policies, the Data Buffer Error can never occur on the Intel® 631xESB/632xESB I/O Controller Hub.
- Master Abort and Target Abort responses from hub interface on EHC-initiated read packets will be treated as Fatal Host Errors. The EHC halts when these conditions are encountered.
- The Intel® 631xESB/632xESB I/O Controller Hub may assert the interrupts which are based on the interrupt threshold as soon as the status for the last complete transaction in the interrupt interval has been posted in the internal write buffers. The requirement in the *Enhanced Host Controller Interface Specification for Universal Serial Bus, Revision 1.0* (that the status is written to memory) is met internally, even though the write may not be seen on the hub interface before the interrupt is asserted.
- Since the Intel® 631xESB/632xESB I/O Controller Hub supports the 1024-element Frame List size, the Frame List Rollover interrupt occurs every 1024 milliseconds.
- The Intel® 631xESB/632xESB I/O Controller Hub delivers interrupts using PIRQH#.
- The Intel® 631xESB/632xESB I/O Controller Hub does not modify the CERR count on an Interrupt IN when the "Do Complete-Split" execution criteria are not met.
- For complete-split transactions in the Periodic list, the "Missed Microframe" bit does not get set on a control-structure-fetch that fails the late-start test. If subsequent accesses to that control structure do not fail the late-start test, then the "Missed Microframe" bit will get set and written back.

5.21.6.1 Aborts on USB 2.0-Initiated Memory Reads

If a read initiated by the EHC is aborted, the EHC treats it as a fatal host error. The following actions are taken when this occurs:

- The Host System Error status bit is set
- The DMA engines are halted after completing up to one more transaction on the USB interface
- If enabled (by the Host System Error Enable), then an interrupt is generated
- If the status is Master Abort, then the Received Master Abort bit in configuration space is set
- If the status is Target Abort, then the Received Target Abort bit in configuration space is set
- If enabled (by the SERR Enable bit in the function's configuration space), then the Signaled System Error (SERR) bit in configuration bit is set.

5.21.7 USB 2.0 Power Management

5.21.7.1 Pause Feature

This feature allows platforms to dynamically enter low-power states during brief periods when the system is idle (that is, between keystrokes). This is useful for enabling power management features like Intel SpeedStep® technology in the Intel® 631xESB/632xESB I/O Controller Hub. The policies for entering these states typically are based on the recent history of system bus activity to incrementally enter deeper power management states. Normally, when the EHC is enabled, it regularly

accesses main memory while traversing the DMA schedules looking for work to do; this activity is viewed by the power management software as a non-idle system, thus preventing the power managed states to be entered. Suspending all of the enabled ports can prevent the memory accesses from occurring, but there is an inherent latency overhead with entering and exiting the suspended state on the USB ports that makes this unacceptable for the purpose of dynamic power management. As a result, the EHCI software drivers are allowed to pause the EHC's DMA engines when it knows that the traffic patterns of the attached devices can afford the delay. The pause prevents only the EHC from generating memory accesses; the SOF packets continue to be generated on the USB ports (unlike the suspended state).

5.21.7.2 Suspend Feature

The *Enhanced Host Controller Interface (EHCI) For Universal Serial Bus Specification*, Section 4.3 describes the details of Port Suspend and Resume.

5.21.7.3 ACPI Device States

The USB 2.0 function supports only the D0 and D3 PCI Power Management states. Notes regarding the Intel® 631xESB/632xESB I/O Controller Hub implementation of the Device States:

1. The EHC hardware does not inherently consume any more power when it is in the D0 state than it does in the D3 state. However, software is required to suspend or disable all ports prior to entering the D3 state such that the maximum power consumption is reduced.
2. In the D0 state, all implemented EHC features are enabled.
3. In the D3 state, accesses to the EHC memory-mapped I/O range will Master abort. Note that, since the Debug Port uses the same memory range, the Debug Port is operational only when the EHC is in the D0 state.
4. In the D3 state, the EHC interrupt must never assert for any reason. The internal PME# signal is used to signal wake events, and so forth.
5. When the Device Power State field is written to D0 from D3, an internal reset is generated. See section EHC Resets for general rules on the effects of this reset.
6. Attempts to write any other value into the Device Power State field other than 00b (D0 state) and 11b (D3 state) will complete normally without changing the current value in this field.

5.21.7.4 ACPI System States

The EHC behavior as it relates to other power management states in the system is summarized in the following list:

- The System is always in the S0 state when the EHC is in the D0 state. However, when the EHC is in the D3 state, the system may be in any power management state (including S0).
- When in D0, the Pause feature (See Section 5.21.7.1) enables dynamic processor low-power states to be entered.
- The PLL in the EHC is disabled when entering the S3HOT state (48 MHz clock stops), or the S3COLD/S4/S5 states (core power turns off).
- All core well logic is reset in the S3/S4/S5 states.

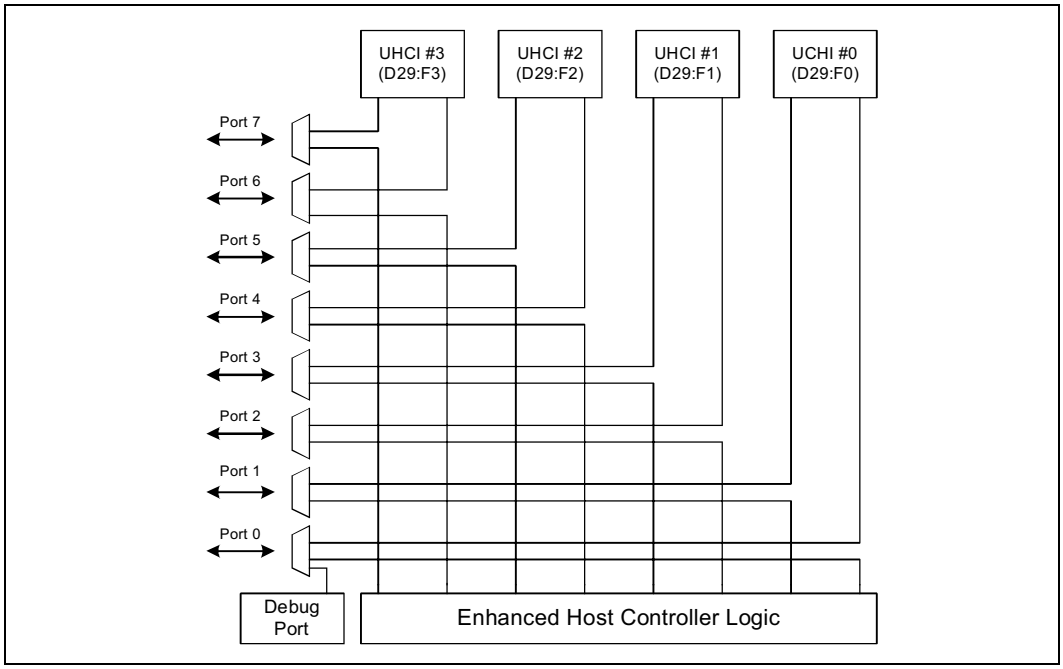
5.21.8 Interaction with UHCI Host Controllers

The Enhanced Host controller shares the eight USB ports with four UHCI Host controllers in the Intel® 631xESB/632xESB I/O Controller Hub. The UHC at D29:F0 shares ports 0 and 1; the UHC at D29:F1 shares ports 2 and 3; the UHC at D29:F2 shares ports 4 and 5; and the UHC at D29:F3 shares ports 6 and 7 with the EHC. There is very little interaction between the Enhanced and the UHCI controllers other than the muxing control which is provided as part of the EHC.Figure 5-23 shows the USB Port Connections at a conceptual level.

5.21.8.1 Port-Routing Logic

Integrated into the EHC functionality is port-routing logic, which performs the muxing between the UHCI and EHCI host controllers. The Intel® 631xESB/632xESB I/O Controller Hub conceptually implements this logic as described in Section 4.2 of the *Enhanced Host Controller Interface Specification for Universal Serial Bus, Revision 1.0.* If a device is connected that is not capable of USB 2.0's high-speed signaling protocol or if the EHCI software drivers are not present as indicated by the Configured Flag, then the UHCI controller owns the port. Owning the port means that the differential output is driven by the owner and the input stream is visible only to the owner. The host controller that is not the owner of the port internally sees a disconnected port.

Figure 5-23. Intel® 631xESB/632xESB I/O Controller Hub-USB Port Connections



Note: The port-routing logic is the only block of logic within the Intel® 631xESB/632xESB I/O Controller Hub that observes the physical (real) connect/disconnect information. The port status logic inside each of the host controllers observes the electrical connect/disconnect information that is generated by the port-routing logic.

Only the differential signal pairs are muxed/demuxed between the UHCI and EHCI host controllers. The other USB functional signals are handled as follows:

- The Overcurrent inputs (OC[7:0]#) are directly routed to both controllers. An overcurrent event is recorded in both controllers' status registers.

The Port-Routing logic is implemented in the Suspend power well so that re-enumeration and re-mapping of the USB ports is not required following entering and exiting a system sleep state in which the core power is turned off.

The Intel® 631xESB/632xESB I/O Controller Hub also allows the USB Debug Port traffic to be routed in and out of Port #0. When in this mode, the Enhanced Host controller is the owner of Port #0.

5.21.8.2 Device Connects

The *Enhanced Host Controller Interface Specification for Universal Serial Bus, Revision 1.0* describes the details of handling Device Connects in Section 4.2. There are four general scenarios that are summarized below.

1. Configure Flag = 0 and a full-speed/low-speed-only Device is connected
   - In this case, the UHC is the owner of the port both before and after the connect occurs. The EHC (except for the port-routing logic) never sees the connect occur. The UHCI driver handles the connection and initialization process.
2. Configure Flag = 0 and a high-speed-capable Device is connected
   - In this case, the UHC is the owner of the port both before and after the connect occurs. The EHC (except for the port-routing logic) never sees the connect occur. The UHCI driver handles the connection and initialization process. Since the UHC does not perform the high-speed chirp handshake, the device operates in compatible mode.
3. Configure Flag = 1 and a full-speed/low-speed-only Device is connected
   - In this case, the EHC is the owner of the port before the connect occurs. The EHCI driver handles the connection and performs the port reset. After the reset process completes, the EHC hardware has cleared (not set) the Port Enable bit in the EHC's PORTSC register. The EHCI driver then writes a 1 to the Port Owner bit in the same register, causing the UHC to see a connect event and the EHC to see an "electrical" disconnect event. The UHCI driver and hardware handle the connection and initialization process from that point on. The EHCI driver and hardware handle the perceived disconnect.
4. Configure Flag = 1 and a high-speed-capable Device is connected
   - In this case, the EHC is the owner of the port before, and remains the owner after, the connect occurs. The EHCI driver handles the connection and performs the port reset. After the reset process completes, the EHC hardware has set the Port Enable bit in the EHC's PORTSC register. The port is functional at this point. The UHC continues to see an unconnected port.

5.21.8.3 Device Disconnects

The *Enhanced Host Controller Interface Specification for Universal Serial Bus, Revision 1.0* describes the details of handling Device Connects in Section 4.2. There are three general scenarios that are summarized below.

1. Configure Flag = 0 and the device is disconnected
   - In this case, the UHC is the owner of the port both before and after the disconnect occurs. The EHC (except for the port-routing logic) never sees a device attached. The UHCI driver handles disconnection process.
2. Configure Flag = 1 and a full-speed/low-speed-capable Device is disconnected
   - In this case, the UHC is the owner of the port before the disconnect occurs. The disconnect is reported by the UHC and serviced by the associated UHCI driver. The port-routing logic in the EHC cluster forces the Port Owner bit to 0, indicating that the EHC owns the unconnected port.

3. Configure Flag = 1 and a high-speed-capable Device is disconnected
   — In this case, the EHC is the owner of the port before, and remains the owner after, the disconnect occurs. The EHCI hardware and driver handle the disconnection process. The UHC never sees a device attached.

5.21.8.4 Effect of Resets on Port-Routing Logic

As mentioned above, the Port Routing logic is implemented in the Suspend power well so that remuneration and re-mapping of the USB ports is not required following entering and exiting a system sleep state in which the core power is turned off.

Reset Event	Effect on Configure Flag	Effect on Port Owner Bits
Suspend Well Reset	cleared (0)	set (1)
Core Well Reset	no effect	no effect
D3-to-D0 Reset	no effect	no effect
HCRESET	cleared (0)	set (1)

5.21.9 USB 2.0 Legacy Keyboard Operation

The Intel® 631xESB/632xESB I/O Controller Hub must support the possibility of a keyboard downstream from either a full-speed/low-speed or a high-speed port. The description of the legacy keyboard support is unchanged from USB 1.1 (See Section 5.20.8).

The EHC provides the basic ability to generate SMIs on an interrupt event, along with more sophisticated control of the generation of SMIs.

5.21.10 USB 2.0 Based Debug Port

The Intel® 631xESB/632xESB I/O Controller Hub supports the elimination of the legacy COM ports by providing the ability for new debugger software to interact with devices on a USB 2.0 port.

High-level restrictions and features are:

- Operational before USB 2.0 drivers are loaded.
- Functions even when the port is disabled.
- Works even though non-configured port is default-routed to the UHCI. Note that the Debug Port can not be used to debug an issue that requires a full-speed/low-speed device on Port #0 using the UHCI drivers.
- Allows normal system USB 2.0 traffic in a system that may have only one USB port.
- Debug Port device (DPD) must be high-speed capable and connect directly to Port #0 on Intel® 631xESB/632xESB I/O Controller Hub systems (for example, the DPD cannot be connected to Port #0 through a hub).
- Debug Port FIFO always makes forward progress (a bad status on USB is simply presented back to software).
- The Debug Port FIFO is given only one USB access per microframe.

The Debug port facilitates operating system and device driver debug. It allows the software to communicate with an external console using a USB 2.0 connection. Because the interface to this link does not go through the normal USB 2.0 stack, it

allows communication with the external console during cases where the operating system is not loaded, the USB 2.0 software is broken, or where the USB 2.0 software is being debugged. Specific features of this implementation of a debug port are:

- Only works with an external USB 2.0 debug device (console)
- Implemented for a specific port on the host controller
- Operational anytime the port is not suspended AND the host controller is in D0 power state.
- Capability is interrupted when port is driving USB RESET

5.21.10.1 Theory of Operation

There are two operational modes for the USB debug port:

1. Mode 1 is when the USB port is in a disabled state from the viewpoint of a standard host controller driver. In Mode 1, the Debug Port controller is required to generate a “keepalive” packets less than 2 ms apart to keep the attached debug device from suspending. The keepalive packet should be a standalone 32-bit SYNC field.
2. Mode 2 is when the host controller is running (that is, host controller’s *Run/Stop#* bit is 1). In Mode 2, the normal transmission of SOF packets will keep the debug device from suspending.

Behavioral Rules

1. In both modes 1 and 2, the Debug Port controller must check for software requested debug transactions at least every 125 microseconds.
2. If the debug port is enabled by the debug driver, and the standard host controller driver resets the USB port, USB debug transactions are held off for the duration of the reset and until after the first SOF is sent.
3. If the standard host controller driver suspends the USB port, then USB debug transactions are held off for the duration of the suspend/resume sequence and until after the first SOF is sent.
4. The ENABLED_CNT bit in the debug register space is independent of the similar port control bit in the associated Port Status and Control register.

Table 5-65 shows the debug port behavior related to the state of bits in the debug registers as well as bits in the associated Port Status and Control register.

Table 5-65. Debug Port Behavior (Sheet 1 of 2)

OWNER_CNT	ENABLED_CT	Port Enable	Run / Stop	Suspend	Debug Port Behavior
0	X	X	X	X	Debug port is not being used. Normal operation.
1	0	X	X	X	Debug port is not being used. Normal operation.
1	1	0	0	X	Debug port in Mode 1. SYNC keepalives sent plus debug traffic
1	1	0	1	X	Debug port in Mode 2. SOF (and only SOF) is sent as keepalive. Debug traffic is also sent. Note that no other normal traffic is sent out this port, because the port is not enabled.
1	1	1	0	0	Illegal. Host controller driver should never put controller into this state (enabled, not running and not suspended).

Table 5-65. Debug Port Behavior (Sheet 2 of 2)

OWNER_CNT	ENABLED_CT	Port Enable	Run / Stop	Suspend	Debug Port Behavior
1	1	1	0	1	Port is suspended. No debug traffic sent.
1	1	1	1	0	Debug port in Mode 2. Debug traffic is interspersed with normal traffic.
1	1	1	1	1	Port is suspended. No debug traffic sent.

5.21.10.1.1 OUT Transactions

An Out transaction sends data to the debug device. It can occur only when the following are true:

- The debug port is enabled
- The debug software sets the GO_CNT bit
- The WRITE_READ#_CNT bit is set

The sequence of the transaction is:

1. Software sets the appropriate values in the following bits:
   - — USB_ADDRESS_CNF
   - — USB_ENDPOINT_CNF
   - — DATA_BUFFER[63:0]
   - — TOKEN_PID_CNT[7:0]
   - — SEND_PID_CNT[15:8]
   - — DATA_LEN_CNT
   - — WRITE_READ#_CNT (note: this will always be 1 for OUT transactions)
   - — GO_CNT (note: this will always be 1 to initiate the transaction)
2. The debug port controller sends a token packet consisting of:
   - — SYNC
   - — TOKEN_PID_CNT field
   - — USB_ADDRESS_CNT field
   - — USB_ENDPOINT_CNT field
   - — 5-bit CRC field
3. After sending the token packet, the debug port controller sends a data packet consisting of:
   - — SYNC
   - — SEND_PID_CNT field
   - — The number of data bytes indicated in DATA_LEN_CNT from the DATA_BUFFER
   - — 16-bit CRC

NOTE: A DATA_LEN_CNT value of 0 is valid in which case no data bytes would be included in the packet.

4. After sending the data packet, the controller waits for a handshake response from the debug device.

- If a handshake is received, the debug port controller:
  - — a. Places the received PID in the RECEIVED_PID_STS field

  - b. Resets the ERROR_GOOD#_STS bit
  - c. Sets the DONE_STS bit
- If no handshake PID is received, the debug port controller:
  - a. Sets the EXCEPTION_STS field to 001b
  - b. Sets the ERROR_GOOD#_STS bit
  - c. Sets the DONE_STS bit

5.21.10.1.2 IN Transactions

An IN transaction receives data from the debug device. It can occur only when the following are true:

- The debug port is enabled
- The debug software sets the GO_CNT bit
- The WRITE_READ#_CNT bit is reset

The sequence of the transaction is:

1. Software sets the appropriate values in the following bits:
   - USB_ADDRESS_CNF
   - USB_ENDPOINT_CNF
   - TOKEN_PID_CNT[7:0]
   - DATA_LEN_CNT
   - WRITE_READ#_CNT (note: this will always be 0 for IN transactions)
   - GO_CNT (note: this will always be 1 to initiate the transaction)
2. The debug port controller sends a token packet consisting of:
   - SYNC
   - TOKEN_PID_CNT field
   - USB_ADDRESS_CNT field
   - USB_ENDPOINT_CNT field
   - 5-bit CRC field.
3. After sending the token packet, the debug port controller waits for a response from the debug device.
   If a response is received:
   - The received PID is placed into the RECEIVED_PID_STS field
   - Any subsequent bytes are placed into the DATA_BUFFER
   - The DATA_LEN_CNT field is updated to show the number of bytes that were received after the PID.
4. If valid packet was received from the device that was one byte in length (indicating it was a handshake packet), then the debug port controller:
   - Resets the ERROR_GOOD#_STS bit
   - Sets the DONE_STS bit
5. If valid packet was received from the device that was more than one byte in length (indicating it was a data packet), then the debug port controller:
   - Transmits an ACK handshake packet
   - Resets the ERROR_GOOD#_STS bit

— Sets the DONE_STS bit

6. If no valid packet is received, then the debug port controller:
   — Sets the EXCEPTION_STS field to 001b
   — Sets the ERROR_GOOD#_STS bit
   — Sets the DONE_STS bit.

5.21.10.1.3 Debug Software

Enabling the Debug Port

There are two mutually exclusive conditions that debug software must address as part of its startup processing:

- The EHCI has been initialized by system software
- The EHCI has not been initialized by system software

Debug software can determine the current ‘initialized’ state of the EHCI by examining the Configure Flag in the EHCI USB 2.0 Command Register. If this flag is set, then system software has initialized the EHCI. Otherwise the EHCI should not be considered initialized. Debug software will initialize the debug port registers depending on the state the EHCI. However, before this can be accomplished, debug software must determine which root USB port is designated as the debug port.

Determining the Debug Port

Debug software can easily determine which USB root port has been designated as the debug port by examining bits 20:23 of the EHCI Host Controller Structural Parameters register. This 4-bit field represents the numeric value assigned to the debug port (that is, 0000=port 0).

Debug Software Startup with Non-Initialized EHCI

Debug software can attempt to use the debug port if after setting the OWNER_CNT bit, the Current Connect Status bit in the appropriate (See Determining the Debug Port) PORTSC register is set. If the Current Connect Status bit is not set, then debug software may choose to terminate or it may choose to wait until a device is connected.

If a device is connected to the port, then debug software must reset/enable the port. Debug software does this by setting and then clearing the Port Reset bit the PORTSC register. To guarantee a successful reset, debug software should wait at least 50 ms before clearing the Port Reset bit. Due to possible delays, this bit may not change to 0 immediately; reset is complete when this bit reads as 0. Software must not continue until this bit reads 0.

If a high-speed device is attached, the EHCI will automatically set the Port Enabled/Disabled bit in the PORTSC register and the debug software can proceed. Debug software should set the ENABLED_CNT bit in the Debug Port Control/Status register, and then reset (clear) the Port Enabled/Disabled bit in the PORTSC register (so that the system host controller driver does not see an enabled port when it is first loaded).

Debug Software Startup with Initialized EHCI

Debug software can attempt to use the debug port if the Current Connect Status bit in the appropriate (See Determining the Debug Port) PORTSC register is set. If the Current Connect Status bit is not set, then debug software may choose to terminate or it may choose to wait until a device is connected.

If a device is connected, then debug software must set the OWNER_CNT bit and then the ENABLED_CNT bit in the Debug Port Control/Status register.

Determining Debug Peripheral Presence

After enabling the debug port functionality, debug software can determine if a debug peripheral is attached by attempting to send data to the debug peripheral. If all attempts result in an error (Exception bits in the Debug Port Control/Status register indicates a Transaction Error), then the attached device is not a debug peripheral. If the debug port peripheral is not present, then debug software may choose to terminate or it may choose to wait until a debug peripheral is connected.

5.22 SMBus

The Intel® 631xESB/632xESB I/O Controller Hub provides an System Management Bus (SMBus) 2.0 compliant Host controller (D31:F3) as well as an SMBus Slave Interface in legacy I/O core, and, Intel® 631xESB/632xESB I/O Controller Hub provides another SMBus Slave interface in the PCI Express to PCI-X bridge. Also, In Intel® 631xESB/ 632xESB I/O Controller Hub BMC, there are 5 SMB interfaces which can be Master or Slave interface (refer to section Section 5.5.5.2 for details).Intel recommends using SMBus 3.

5.22.1 SMBus Controller (D31:F3)

This host controller provides a mechanism for the processor to initiate communications with SMBus peripherals (Slaves). The Intel® 631xESB/632xESB I/O Controller Hub is also capable of operating in a mode in which it can communicate with I^2C compatible devices.

The Intel® 631xESB/632xESB I/O Controller Hub can perform SMBus messages with either packet error checking (PEC) enabled or disabled. The actual PEC calculation and checking is performed in hardware by the Intel® 631xESB/632xESB I/O Controller Hub.

The Slave Interface allows an external Master to read from or write to the Intel® 631xESB/632xESB I/O Controller Hub. Write cycles can be used to cause certain events or pass messages, and the read cycles can be used to determine the state of various status bits. The Intel® 631xESB/632xESB I/O Controller Hub's internal host controller cannot access the Intel® 631xESB/632xESB I/O Controller Hub's internal Slave Interface.

The Intel® 631xESB/632xESB I/O Controller Hub SMBus logic exists in Device 31:Function 3 configuration space, and consists of a transmit data path, and host controller. The transmit data path provides the data flow logic needed to implement the seven different SMBus command protocols and is controlled by the host controller. The Intel® 631xESB/632xESB I/O Controller Hub SMBus controller logic is clocked by RTC clock.

The SMBus Address Resolution Protocol (ARP) is supported by using the existing host controller commands through software, except for the new Host Notify command (which is actually a received message).

The programming model of the host controller is combined into two portions: a PCI configuration portion, and a system I/O mapped portion. All static configuration, such as the I/O base address, is done by way of the PCI configuration space. Real-time programming of the Host interface is done in system I/O space.

The Intel® 631xESB/632xESB I/O Controller Hub SMBus host controller checks for parity errors as a target. If an error is detected, the detected parity error bit in the PCI Status Register (Device 31:Function 3:Offset 06h:bit 15) is set. If bit 6 and bit 8 of the PCI Command Register (Device 31:Function 3:Offset 04h) are set, an SERR# is generated and the signalled SERR# bit in the PCI Status Register (bit 14) is set.

5.22.1.1 Host Controller

The SMBus host controller is used to send commands to other SMBus Slave devices. Software sets up the host controller with an address, command, and, for writes, data and optional PEC; and then tells the controller to start. When the controller has finished transmitting data on writes, or receiving data on reads, it generates an SMI# or interrupt, if enabled.

The host controller supports 8 command protocols of the SMBus interface (see *System Management Bus (SMBus) Specification, Version 2.0*): Quick Command, Send Byte, Receive Byte, Write Byte/Word, Read Byte/Word, Process Call, Block Read/Write, Block Write–Block Read Process Call.

The SMBus host controller requires that the various data and command fields be setup for the type of command to be sent. When software sets the START bit, the SMBus Host controller performs the requested transaction, and interrupts the processor (or generates an SMI#) when the transaction is completed. Once a START command has been issued, the values of the “active registers” (Host Control, Host Command, Transmit Slave Address, Data 0, Data 1) should not be changed or read until the interrupt status bit (INTR) has been set (indicating the completion of the command). Any register values needed for computation purposes should be saved prior to issuing of a new command, as the SMBus host controller updates all registers while completing the new command.

Using the SMB host controller to send commands to the Intel® 631xESB/632xESB I/O Controller Hub’s SMB Slave port is supported. The Intel® 631xESB/632xESB I/O Controller Hub is fully compliant with the *System Management Bus (SMBus) Specification, Version 2.0*. Slave functionality, including the Host Notify protocol, is available on the SMBus pins. The SMLink and SMBus signals must be tied together externally.

5.22.1.1.1 Command Protocols

In all of the following commands, the Host Status Register (offset 00h) is used to determine the progress of the command. While the command is in operation, the HOST_BUSY bit is set. If the command completes successfully, the INTR bit will be set in the Host Status Register. If the device does not respond with an acknowledge, and the transaction times out, the DEV_ERR bit is set. If software sets the KILL bit in the Host Control Register while the command is running, the transaction will stop and the FAILED bit will be set.

Quick Command

When programmed for a Quick Command, the Transmit Slave Address Register is sent. The PEC byte is never appended to the Quick Protocol. Software should force the PEC_EN bit to 0 when performing the Quick Command. Software must force the I2C_EN bit to 0 when running this command. See section 5.5.1 of the *System Management Bus (SMBus) Specification, Version 2.0* for the format of the protocol.

Send Byte / Receive Byte

For the Send Byte command, the Transmit Slave Address and Device Command Registers are sent
For the Receive Byte command, the Transmit Slave Address Register is sent. The data received is stored in the DATA0 register. Software must force the I2C_EN bit to 0 when running this command.

The Receive Byte is similar to a Send Byte, the only difference is the direction of data transfer. See sections 5.5.2 and 5.5.3 of the *System Management Bus (SMBus) Specification, Version 2.0* for the format of the protocol.

Write Byte/Word

The first byte of a Write Byte/Word access is the command code. The next 1 or 2 bytes are the data to be written. When programmed for a Write Byte/Word command, the Transmit Slave Address, Device Command, and Data0 Registers are sent. In addition, the Data1 Register is sent on a Write Word command. Software must force the I2C_EN bit to 0 when running this command. See section 5.5.4 of the *System Management Bus (SMBus) Specification, Version 2.0* for the format of the protocol.

Read Byte/Word

Reading data is slightly more complicated than writing data. First the Intel® 631xESB/632xESB I/O Controller Hub must write a command to the Slave device. Then it must follow that command with a repeated start condition to denote a read from that device's address. The Slave then returns 1 or 2 bytes of data. Software must force the I2C_EN bit to 0 when running this command.

When programmed for the read byte/word command, the Transmit Slave Address and Device Command Registers are sent. Data is received into the DATA0 on the read byte, and the DAT0 and DATA1 registers on the read word. See section 5.5.5 of the *System Management Bus (SMBus) Specification, Version 2.0* for the format of the protocol.

Process Call

The process call is so named because a command sends data and waits for the Slave to return a value dependent on that data. The protocol is simply a Write Word followed by a Read Word, but without a second command or stop condition.

When programmed for the Process Call command, the Intel® 631xESB/632xESB I/O Controller Hub transmits the Transmit Slave Address, Host Command, DATA0 and DATA1 registers. Data received from the device is stored in the DATA0 and DATA1 registers. The Process Call command with I2C_EN set and the PEC_EN bit set produces undefined results. Software must force either I2C_EN or PEC_EN to 0 when running this command. See section 5.5.6 of the *System Management Bus (SMBus) Specification, Version 2.0* for the format of the protocol.

Note: For process call command, the value written into bit 0 of the Transmit Slave Address Register (SMB I/O register, offset 04h) needs to be 0.

Note: If the I2C_EN bit is set, the protocol sequence changes slightly: the Command Code (bits 18:11 in the bit sequence) are not sent – as a result, the Slave will not acknowledge (bit 19 in the sequence).

Block Read / Write

The Intel® 631xESB/632xESB I/O Controller Hub contains a 32-byte buffer for read and write data which can be enabled by setting bit 1 of the Auxiliary Control register at offset 0Dh in I/O space, as opposed to a single byte of buffering. This 32-byte buffer is filled with write data before transmission, and filled with read data on reception. In the Intel® 631xESB/632xESB I/O Controller Hub, the interrupt is generated only after a transmission or reception of 32 bytes, or when the entire byte count has been transmitted/received.

The byte count field is transmitted but ignored by the Intel® 631xESB/632xESB I/O Controller Hub as software will end the transfer after all bytes it cares about have been sent or received.

For a Block Write, software must either force the I2C_EN bit or both the PEC_EN and AAC bits to 0 when running this command.

The block write begins with a Slave address and a write condition. After the command code the Intel® 631xESB/632xESB I/O Controller Hub issues a byte count describing how many more bytes will follow in the message. If a Slave had 20 bytes to send, the first byte would be the number 20 (14h), followed by 20 bytes of data. The byte count may not be 0. A Block Read or Write is allowed to transfer a maximum of 32 data bytes.

When programmed for a block write command, the Transmit Slave Address, Device Command, and Data0 (count) registers are sent. Data is then sent from the Block Data Byte register; the total data sent being the value stored in the Data0 Register. On block read commands, the first byte received is stored in the Data0 register, and the remaining bytes are stored in the Block Data Byte register. See section 5.5.7 of the *System Management Bus (SMBus) Specification, Version 2.0* for the format of the protocol.

Note: For Block Write, if the I2C_EN bit is set, the format of the command changes slightly. The Intel® 631xESB/632xESB I/O Controller Hub will still send the number of bytes (on writes) or receive the number of bytes (on reads) indicated in the DATA0 register. However, it will not send the contents of the DATA0 register as part of the message. Also, the Block Write protocol sequence changes slightly: the Byte Count (bits 27:20 in the bit sequence) are not sent – as a result, the Slave will not acknowledge (bit 28 in the sequence).

I²C Read

This command allows the Intel® 631xESB/632xESB I/O Controller Hub to perform block reads to certain I^2C devices, such as serial E^2PROMs. The SMBus Block Read supports the 7-bit addressing mode only.

However, this does not allow access to devices using the I^2C “Combined Format” that has data bytes after the address. Typically these data bytes correspond to an offset (address) within the serial memory chips.

Note: This command is supported independent of the setting of the I2C_EN bit. The I^2C Read command with the PEC_EN bit set produces undefined results. Software must force both the PEC_EN and AAC bit to 0 when running this command.

For I^2C Read command, the value written into bit 0 of the Transmit Slave Address Register (SMB I/O register, offset 04h) needs to be 0.

The format that is used for the command is shown in Table 5-66.

Table 5-66. I²C* Block Read

Bit	Description
1	Start
8:2	Slave Address – 7 bits
9	Write
10	Acknowledge from Slave
18:11	Send DATA1 register
19	Acknowledge from Slave
20	Repeated Start
27:21	Slave Address – 7 bits
28	Read
29	Acknowledge from Slave
37:30	Data byte 1 from Slave – 8 bits
38	Acknowledge
46:39	Data byte 2 from Slave – 8 bits
47	Acknowledge
–	Data bytes from Slave / Acknowledge
–	Data byte N from Slave – 8 bits
–	NOT Acknowledge
–	Stop

The Intel® 631xESB/632xESB I/O Controller Hub will continue reading data from the peripheral until the NAK is received.

Block Write–Block Read Process Call

The block write-block read process call is a two-part message. The call begins with a Slave address and a write condition. After the command code the host issues a write byte count (M) that describes how many more bytes will be written in the first part of the message. If a Master has 6 bytes to send, the byte count field will have the value 6 (0000 0110b), followed by the 6 bytes of data. The write byte count (M) cannot be 0.

The second part of the message is a block of read data beginning with a repeated start condition followed by the Slave address and a Read bit. The next byte is the read byte count (N), which may differ from the write byte count (M). The read byte count (N) cannot be 0.

The combined data payload must not exceed 32 bytes. The byte length restrictions of this process call are summarized as follows:

- $M \geq 1$ byte
- $N \geq 1$ byte
- $M + N \leq 32$ bytes

The read byte count does not include the PEC byte. The PEC is computed on the total message beginning with the first Slave address and using the normal PEC computational rules. It is highly recommended that a PEC byte be used with the Block Write-Block Read Process Call. Software must do a read to the command register (offset 2h) to reset the 32 byte buffer pointer prior to reading the block data register.

Note: There is no STOP condition before the repeated START condition, and a NACK signifies the end of the read transfer.

Note: E32B bit in the Auxiliary Control register must be set when using this protocol.

See section 5.5.8 of the *System Management Bus (SMBus) Specification, Version 2.0* for the format of the protocol.

5.22.1.2 Bus Arbitration

Several Masters may attempt to get on the bus at the same time by driving the SMBDATA line low to signal a start condition. The Intel® 631xESB/632xESB I/O Controller Hub continuously monitors the SMBDATA line. When the Intel® 631xESB/632xESB I/O Controller Hub is attempting to drive the bus to a 1 by letting go of the SMBDATA line, and it samples SMBDATA low, then some other Master is driving the bus and the Intel® 631xESB/632xESB I/O Controller Hub will stop transferring data.

If the Intel® 631xESB/632xESB I/O Controller Hub sees that it has lost arbitration, the condition is called a collision. The Intel® 631xESB/632xESB I/O Controller Hub will set the BUS_ERR bit in the Host Status Register, and if enabled, generate an interrupt or SMI#. The processor is responsible for restarting the transaction.

When the Intel® 631xESB/632xESB I/O Controller Hub is a SMBus Master, it drives the clock. When the Intel® 631xESB/632xESB I/O Controller Hub is sending address or command as an SMBus Master, or data bytes as a Master on writes, it drives data relative to the clock it is also driving. It will not start toggling the clock until the start or stop condition meets proper setup and hold time. The Intel® 631xESB/632xESB I/O Controller Hub will also guarantee minimum time between SMBus transactions as a Master.

Note: The Intel® 631xESB/632xESB I/O Controller Hub supports the same arbitration protocol for both the SMBus and the System Management (SMLINK) interfaces.

5.22.1.3 Bus Timing

5.22.1.3.1 Clock Stretching

Some devices may not be able to handle their clock toggling at the rate that the Intel® 631xESB/632xESB I/O Controller Hub as an SMBus Master would like. They have the capability of stretching the low time of the clock. When the Intel® 631xESB/632xESB I/O Controller Hub attempts to release the clock (allowing the clock to go high), the clock will remain low for an extended period of time.

The Intel® 631xESB/632xESB I/O Controller Hub monitors the SMBus clock line after it releases the bus to determine whether to enable the counter for the high time of the clock. While the bus is still low, the high time counter must not be enabled. Similarly, the low period of the clock can be stretched by an SMBus Master if it is not ready to send or receive data.

5.22.1.3.2 Bus Time Out (Intel® 631xESB/632xESB I/O Controller Hub as SMBus Master)

If there is an error in the transaction, such that an SMBus device does not signal an acknowledge, or holds the clock lower than the allowed time-out time, the transaction will time out. The Intel® 631xESB/632xESB I/O Controller Hub will discard the cycle and set the DEV_ERR bit. The time out minimum is 25 ms (800 RTC clocks). The time-out counter inside the Intel® 631xESB/632xESB I/O Controller Hub will start after the last bit of data is transferred by the Intel® 631xESB/632xESB I/O Controller Hub and it is waiting for a response.

The 25 ms timeout counter will not count under the following conditions:

1. BYTE_DONE_STATUS bit (SMBus I/O Offset 00h, bit 7) is set
2. The SECOND_TO_STS bit (TCO I/O Offset 06h, bit 1) is not set (this indicates that the system has not locked up)

5.22.1.4 Interrupts / SMI#

The Intel® 631xESB/632xESB I/O Controller Hub SMBus controller uses PIRQB# as its interrupt pin. However, the system can alternatively be set up to generate SMI# instead of an interrupt, by setting the SMBUS_SMI_EN bit (Device 31:Function 0:Offset 40h:bit 1).

Table 5-67 to Table 5-69 specify how the various enable bits in the SMBus function control the generation of the interrupt, Host and Slave SMI, and Wake internal signals. The rows in the tables are additive, which means that if more than one row is true for a particular scenario then the Results for all of the activated rows will occur.

Table 5-67. Enable for SMBALERT#

Event	INTREN (Host Control I/O Register, Offset 02h, Bit 0)	SMB_SMI_EN (Host Configuration Register, D31:F3:Offset 40h, Bit 1)	SMBALERT_DIS (Slave Command I/O Register, Offset 11h, Bit 2)	Result
SMBALERT# asserted low (always reported in Host Status Register, Bit 5)	X	X	X	Wake generated
	X	1	0	Slave SMI# generated (SMBUS_SMI_STS)
	1	0	0	Interrupt generated

Table 5-68. Enables for SMBus Slave Write and SMBus Host Events

Event	INTREN (Host Control I/O Register, Offset 02h, Bit 0)	SMB_SMI_EN (Host Configuration Register, D31:F3:Offset 40h, Bit1)	Event
Slave Write to Wake/ SMI# Command	X	X	Wake generated when asleep. Slave SMI# generated when awake (SMBUS_SMI_STS).
Slave Write to SMLINK_SLAVE_SMI Command	X	X	Slave SMI# generated when in the S0 state (SMBUS_SMI_STS)
Any combination of Host Status Register [4:1] asserted	0	X	None
	1	0	Interrupt generated
	1	1	Host SMI# generated

Table 5-69. Enables for the Host Notify Command

HOST_NOTIFY_INTREN (Slave Control I/O Register, Offset 11h, bit 0)	SMB_SMI_EN (Host Config Register, D31:F3:Off40h, Bit 1)	HOST_NOTIFY_WKEN (Slave Control I/O Register, Offset 11h, bit 1)	Result
0	X	0	None
X	X	1	Wake generated
1	0	X	Interrupt generated
1	1	X	Slave SMI# generated (SMBUS_SMI_STS)

5.22.1.5 SMBALERT#

SMBALERT# is multiplexed with GPI[11]. When enable and the signal is asserted, The Intel® 631xESB/632xESB I/O Controller Hub can generate an interrupt, an SMI#, or a wake event from S1–S5.

Note: Any event on SMBALERT# (regardless whether it is programmed as a GPI or not), causes the event message to be sent in heartbeat mode.

5.22.1.6 SMBus CRC Generation and Checking

If the AAC bit is set in the Auxiliary Control register, the Intel® 631xESB/632xESB I/O Controller Hub automatically calculates and drives CRC at the end of the transmitted packet for write cycles, and will check the CRC for read cycles. It will not transmit the contents of the PEC register for CRC. The PEC bit must not be set in the Host Control register if this bit is set, or unspecified behavior will result.

If the read cycle results in a CRC error, the DEV_ERR bit and the CRCE bit in the Auxiliary Status register at offset 0Ch will be set.

5.22.1.7 SMBus Slave Interface

The Intel® 631xESB/632xESB I/O Controller Hub's SMBus Slave interface is accessed by way of the SMBus. The SMBus Slave logic will not generate or handle receiving the PEC byte and will only act as a Legacy Alerting Protocol device. The Slave interface allows the Intel® 631xESB/632xESB I/O Controller Hub to decode cycles, and allows an external microcontroller to perform specific actions. Key features and capabilities include:

- Supports decode of three types of messages: Byte Write, Byte Read, and Host Notify.
- Receive Slave Address register: This is the address that the Intel® 631xESB/632xESB I/O Controller Hub decodes. A default value is provided so that the Slave interface can be used without the processor having to program this register.
- Receive Slave Data register in the SMBus I/O space that includes the data written by the external microcontroller.
- Registers that the external microcontroller can read to get the state of the Intel® 631xESB/632xESB I/O Controller Hub.
- Status bits to indicate that the SMBus Slave logic caused an interrupt or SMI# due to the reception of a message that matched the Slave address.
  - — Bit 0 of the Slave Status Register for the Host Notify command
  - — Bit 16 of the SMI Status Register (Section 21.8.2.10) for all others

If a Master leaves the clock and data bits of the SMBus interface at 1 for 50 µs or more in the middle of a cycle, the Intel® 631xESB/632xESB I/O Controller Hub Slave logic's behavior is undefined. This is interpreted as an unexpected idle and should be avoided when performing management activities to the Slave logic.

Note: When an external microcontroller accesses the SMBus Slave Interface over the SMBus a translation in the address is needed to accommodate the least significant bit used for read/write control. For example, if the Intel® 631xESB/632xESB I/O Controller Hub Slave address (RCV_SLVA) is left at 44h (default), the external micro controller would use an address of 88h/89h (write/read).

5.22.1.7.1 Format of Slave Write Cycle

The external Master performs Byte Write commands to the Intel® 631xESB/632xESB I/O Controller Hub SMBus Slave I/F. The "Command" field (bits 11:18) indicate which register is being accessed. The Data field (bits 20:27) indicate the value that should be written to that register.

Table 5-70 has the values associated with the registers.

Table 5-70. Slave Write Registers

Register	Function
0	Command Register. See Table 5-71 below for legal values written to this register.
1–3	Reserved
4	Data Message Byte 0
5	Data Message Byte 1
6–7	Reserved
8	Reserved
9–FFh	Reserved

Note: The external microcontroller is responsible to make sure that it does not update the contents of the data byte registers until they have been read by the system processor. The Intel® 631xESB/632xESB I/O Controller Hub overwrites the old value with any new value received. A race condition is possible where the new value is being written to the register just at the time it is being read. Intel® 631xESB/632xESB I/O Controller Hub will not attempt to cover this race condition (that is, unpredictable results will result in this case).

Table 5-71. Command Types (Sheet 1 of 2)

Command Type	Description
0	Reserved.
1	**WAKE/SMI#.** This command wakes the system if it is not already awake. If system is already awake, an SMI# is generated. ***Note:*** The SMB_WAK_STS bit will be set by this command, even if the system is already awake. The SMI handler should then clear this bit.
2	**Unconditional Powerdown.** This command sets the PWRBTNOR_STS bit, and has the same effect as the Powerbutton Override occurring.
3	**HARD RESET WITHOUT CYCLING:** This command causes a hard reset of the system (does not include cycling of the power supply). This is equivalent to a write to the CF9h register with bits 2:1 set to 1, but bit 3 set to 0.
4	**HARD RESET SYSTEM.** This command causes a hard reset of the system (including cycling of the power supply). This is equivalent to a write to the CF9h register with bits 3:1 set to 1.
5	**Disable the TCO Messages.** This command will disable the Intel® 631xESB/632xESB I/O Controller Hub from sending Heartbeat and Event messages (as described in Section 5.16.2). Once this command has been executed, Heartbeat and Event message reporting can be re-enabled only by assertion and deassertion of the RSMRST# signal.

Table 5-71. Command Types (Sheet 2 of 2)

Command Type	Description
6	**WD RELOAD:** Reload watchdog timer.
7	Reserved.
8	**SMLINK_SLV_SMI.** When Intel® 631xESB/632xESB I/O Controller Hub detects this command type while in the S0 state, it sets the SMLINK_SLV_SMI_STS bit (see Section 21.9.6). This command should be used only if the system is in an S0 state. If the message is received during S1–S5 states, the Intel® 631xESB/632xESB I/O Controller Hub acknowledges it, but the SMLINK_SLV_SMI_STS bit does not get set. Note: It is possible that the system transitions out of the S0 state at the same time that the SMLINK_SLV_SMI command is received. In this case, the SMLINK_SLV_SMI_STS bit may get set but not serviced before the system goes to sleep. Once the system returns to S0, the SMI associated with this bit would then be generated. Software must be able to handle this scenario.
9–FFh	Reserved.

5.22.1.7.2 Format of Read Command

The external Master performs Byte Read commands to the Intel® 631xESB/632xESB I/O Controller Hub SMBus Slave I/F. The “Command” field (bits 18:11) indicate which register is being accessed. The Data field (bits 30:37) contain the value that should be read from that register. Table 5-72 shows Read Cycle Format. Table 5-73 shows Data Value for Slave Read Registers

Table 5-72. Read Cycle Format

Bit	Description	Driven By	Comment
1	Start	External Master	
8:2	Slave Address – 7 bits	External Master	Must match value in Receive Slave Address register
9	Write	External Master	Always 0
10	ACK	Intel® 631xESB/632xESB I/O Controller Hub	
18:11	Command Code– 8 bits	External Master	Indicates which register is being accessed. See Table 5-73
19	ACK	Intel® 631xESB/632xESB I/O Controller Hub	
20	Repeated Start	External Master	
27:21	Slave Address	External Master	Must match value in Receive Slave Address register
28	Read	External Master	Always 1
29	ACK	Intel® 631xESB/632xESB I/O Controller Hub	
37:30	Data Type	Intel® 631xESB/632xESB I/O Controller Hub	Value depends on register being accessed, see Table 5-73
38	NOT ACK	External Master	
39	Stop	External Master	

Table 5-73. Data Value for Slave Read Registers

Register	Bits	Description
0	7:0	Reserved
1	2:0	System Power State 000 = S0 001 = S1 010 = Reserved 011 = S3 100 = S4 101 = S5 110 = Reserved 111 = Reserved
	7:3	Reserved
2	3:0	Reserved
	7:4	Reserved
3	5:0	Watchdog Timer current value. Note that Watchdog Timer has 10 bits, but this field is only 6 bits. If the current value is greater than 3Fh, Intel® 631xESB/632xESB I/O Controller Hub will always report 3Fh in this field.
	7:6	Reserved
4	0	1 = The **Intruder Detect** (INTRD_DET) bit is set. This indicates that the system cover has probably been opened.
	1	1 = BTI **Temperature Event** occurred. This bit will be set if the Intel® 631xESB/632xESB I/O Controller Hub's THRM# input signal is active. Need to take after polarity control.
	2	**DOA processor Status**. This bit will be 1 to indicate that the processor is dead
	3	1 = **SECOND_TO_STS** bit set. This bit will be set after the second timeout (SECOND_TO_STS bit) of the Watchdog Timer occurs.
	6:4	Reserved. Will always be 0, but software should ignore.
	7	Reflects the value of the GPI[11]/SMBALERT# pin (and is dependent upon the value of the GPI_INV[11] bit. If the GPI_INV[11] bit is 1, then the value in this bit equals the level of the GPI[11]/SMBALERT# pin (high = 1, low = 0). If the GPI_INV[11] bit is 0, then the value of this bit will equal the inverse of the level of the GPI[11]/SMBALERT# pin (high = 0, low = 1).
5	0	**FWH bad bit.** This bit will be 1 to indicate that the FWH read returned FFh, which indicates that it is probably blank.
	1	**Battery Low Status.** '1' if the BATLOW# pin is a '0'.
	2	**CPU Power Failure Status:** '1' if the CPUPWR_FLR bit in the GEN_PMCON_2 register is set.
	7:3	Reserved
6	7:0	Contents of the Message 1 register. for the description of this register.
7	7:0	Contents of the Message 2 register. for the description of this register.
8	7:0	Contents of the WDSTATUS register. for the description of this register.
9~FFH	7:0	Reserved

Behavioral Notes

According to SMBus protocol, Read and Write messages always begin with a Start bit – Address– Write bit sequence. When the Intel® 631xESB/632xESB I/O Controller Hub detects that the address matches the value in the Receive Slave Address register, it will assume that the protocol is always followed and ignore the Write bit (bit 9) and signal an Acknowledge during bit 10. In other words, if a Start –Address–Read occurs (which

is illegal for SMBus Read or Write protocol), and the address matches the Intel® 631xESB/632xESB I/O Controller Hub's Slave Address, the Intel® 631xESB/632xESB I/O Controller Hub will still grab the cycle.

Also according to SMBus protocol, a Read cycle contains a Repeated Start–Address–Read sequence beginning at bit 20. Once again, if the Address matches the Intel® 631xESB/632xESB I/O Controller Hub's Receive Slave Address, it will assume that the protocol is followed, ignore bit 28, and proceed with the Slave Read cycle.

Note: An external microcontroller must not attempt to access the Intel® 631xESB/632xESB I/O Controller Hub's SMBus Slave logic until at least 1 second after both RTCRST# and RSMRST# are deasserted (high).

5.22.1.7.3 Format of Host Notify Command

The Intel® 631xESB/632xESB I/O Controller Hub tracks and responds to the standard Host Notify command as specified in the *System Management Bus (SMBus) Specification, Version 2.0*. The host address for this command is fixed to 0001000b. If the Intel® 631xESB/632xESB I/O Controller Hub already has data for a previously-received host notify command which has not been serviced yet by the host software (as indicated by the HOST_NOTIFY_STS bit), then it will NACK following the host address byte of the protocol. This allows the host to communicate non-acceptance to the Master and retain the host notify address and data values for the previous cycle until host software completely services the interrupt.

Note: Host software must always clear the HOST_NOTIFY_STS bit after completing any necessary reads of the address and data registers.

Table 5-74 shows the Host Notify format.

Table 5-74. Host Notify Format

Bit	Description	Driven By	Comment
1	Start	External Master	
8:2	SMB Host Address – 7 bits	External Master	Always 0001_000
9	Write	External Master	Always 0
10	ACK (or NACK)	Intel® 631xESB/632xESB I/O Controller Hub	Intel® 631xESB/632xESB I/O Controller Hub NACKs if HOST_NOTIFY_STS is 1
17:11	Device Address – 7 bits	External Master	Indicates the address of the Master; loaded into the Notify Device Address Register
18	Unused – Always 0	External Master	7-bit-only address; this bit is inserted to complete the byte
19	ACK	Intel® 631xESB/632xESB I/O Controller Hub	
27:20	Data Byte Low – 8 bits	External Master	Loaded into the Notify Data Low Byte Register
28	ACK	Intel® 631xESB/632xESB I/O Controller Hub	
36:29	Data Byte High – 8 bits	External Master	Loaded into the Notify Data High Byte Register
37	ACK	Intel® 631xESB/632xESB I/O Controller Hub	
38	Stop	External Master	

5.22.2 SMBus Slave Interface in PCI Express to PCI-X Bridge

The SMBus address is set upon PWROK by sampling SMBus[5] and SMBus[3:1]. When the pins are sampled, the resulting Intel® 631xESB/632xESB I/O Controller Hub address will be as follows:

Table 5-75. SMBus Address Configuration

Bit	Value
7	1
6	1
5	SMBUS[5]
4	0
3	SMBUS[3]
2	SMBUS[2]
1	SMBUS[1]

This SMBus controller has access to all internal registers in PCI Express Bridge/Switch. It can perform reads and writes from all registers through the particular interface's configuration or memory space. I/OxAPIC memory space is accessible through its configuration space. SHPC memory space is directly accessible from the SMBus controller via the SMBus memory command.

5.22.2.1 SMBUS Commands

This SMBus supports six SMBus commands:

- Block Write
- Block Read
- Word Write
- Word Read
- Byte Write
- Byte Read

Sequencing these commands will initiate internal accesses to Intel® 631xESB/632xESB I/O Controller Hub's configuration and memory registers. For high reliability, Intel® 631xESB/632xESB I/O Controller Hub also supports the optional Packet Error Checking feature (CRC-8) and is enabled or disabled with each transaction.

Every configuration and memory read or write first consists of an SMBus write sequence which initializes the Bus Number, Device, function number, memory address offset etc. The term sequence is used since these variables can be initialized by the SMBus Master with a single block write or multiple word or byte writes. The last write in the sequence that completes the initialization performs the internal configuration/ memory read or write. The SMBus Master can then initiate a read sequence which returns the status of the internal read or write command and also the data in case of a read.

Each SMBus transaction has an 8-bit command driven by the Master. The command encodes the following information:

Table 5-76. SMBus Command Encoding

Bit	Description
7	Begin: The Begin bit when set indicates the first transaction of the read or write sequence
6	End: The End bit when set indicates the last transaction of the read or write sequence
5	Memory/Config: Indicate whether memory or configuration space is being accesses in this SMBus sequence. Value of '1' indicates memory and a value of '0' indicate configuration.
4	PEC Enable: Indicates that PEC is enabled when set. When set, each transaction in the sequence ends with an extra CRC byte. PCI Express Bridge/Switch would check for CRC on writes and generate CRC on reads. PEC does not include the command byte itself
3:2	Internal Command: 00 – Read Dword 01 – Write Byte 10 – Write Word 11 – Write Dword All access are naturally aligned to the access width. This field specifies the internal command to be issued by the SMBus Slave logic to the PCI Express Bridge/Switch.
1:0	SMBus command: 00 – Byte 01 – Word 10 – Block 11 – *Rsvd* This field specifies the SMBus command to be issued on the SMBus. This field is used as an indication of the length of transfer so that the Slave knows when to expect the PEC packet (if enabled).

5.22.2.2 Initialization Sequence

All Configuration and memory read and writes are accomplished through an SMBus write(s) and later followed by an SMBus read (for a read command). The SMBus write sequence is used to initialize the:

- Bus Number,
- Device/Function and
- 12-bit Register Number (in 2 separate bytes on SMBus)

for the configuration access. Each of the parameters above is sent on SMBus in separate bytes. The register number parameter is initialized with two bytes and Intel® 631xESB/632xESB I/O Controller Hub ignores the most significant 4 bits of the second byte that initializes the register number. For memory reads and writes, the write sequence initializes the

- Destination memory
- 24-bit memory address offset (in 3 separate bytes on SMBus)

The destination memory is a byte of information that indicates the internal memory space to access in the Intel® 631xESB/632xESB I/O Controller Hub 64-bit PCI Hub. The 24-bit address offset is used to address any internal memory with up to an offset of 24 bits. The Intel® 631xESB/632xESB I/O Controller Hub 64-bit PCI Hub uses only

12 bits of address, and ignores the most significant 12 bits of the 24-bit address. The Intel® 631xESB/632xESB I/O Controller Hub 64-bit PCI Hub Slave interface always expects 24 bits of address from the SMBus Master though it uses only 12 bits.

The initialization of the information can be accomplished through any combination of the supported SMBus write commands (Block, Word or Byte). The Internal Command field for each write should specify the same internal command every time (read or write). After all the information is set up, the last write (End bit is set) initiates an internal read or write command. On an internal read if the data is not available before the Slave interface acknowledges this last write command (ACK), the Slave will clock stretch until the data returns to the SMBus interface unit. On a internal write, if the write is not complete before the Slave interface acknowledges this last write command (ACK), the salve will clock stretch until the write completes internally. If an error occurs (internal timeout, Target or Master abort on the internal switch) during the internal access, the last write command will receive a NACK.

5.22.2.3 Configuration And Memory Reads

Intel® 631xESB/632xESB I/O Controller Hub supports only read dword to internal register space. All Configuration and memory reads are accomplished through an SMBus write(s) and later followed by an SMBus read to read the status and the read data. For SMBus read transactions, the last byte of data (or the PEC byte if enabled) is NACKed by the Master to indicate the end of the transaction. The SMBus read command returns the status of the previous internal command and the data associated previous internal read command. Table 5-77 shows the status field encoding:

Table 5-77. SMBus Status Byte Encoding

Bit	Description
7	Internal Timeout. This bit is set if an SMBus request is not completed in 2ms internally.
6	Reserved
5	Internal Master Abort
4	Internal Target Abort
3:1	Reserved
0	Successful

Examples of configuration and memory reads are shown in Figure 5-24 to Figure 5-29. For the definition of the diagram conventions below, refer to the *System Management Bus (SMBus) Specification, Version 2.0.*

Figure 5-24. DWord Configuration Read Protocol (SMBus Block Write / Block Read, PEC Enabled)

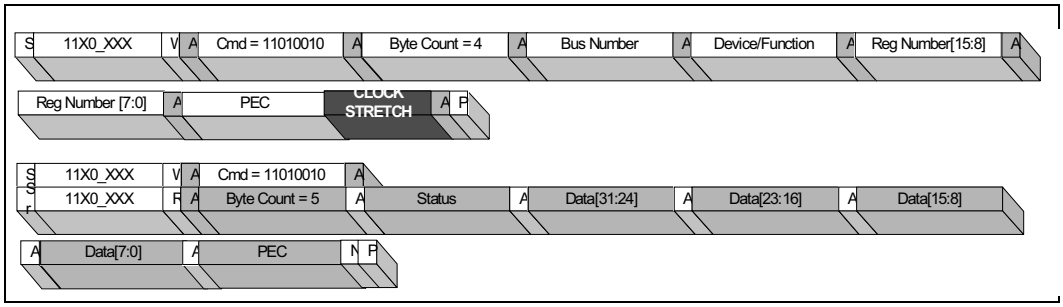


Figure 5-25. DWord Memory Read Protocol (SMBus Block Write / Block Read, PEC Enabled)

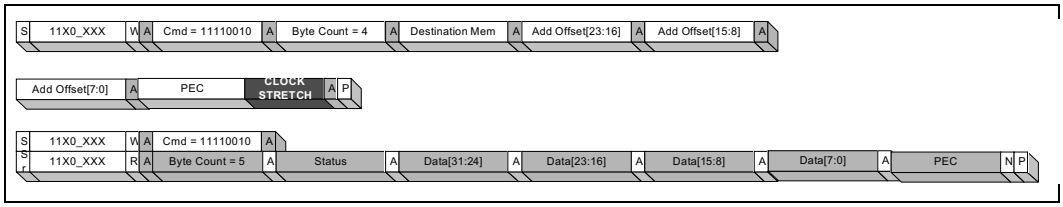


Figure 5-26. DWord Configuration Read Protocol (SMBus Word Write / Word Read, PEC Enabled)

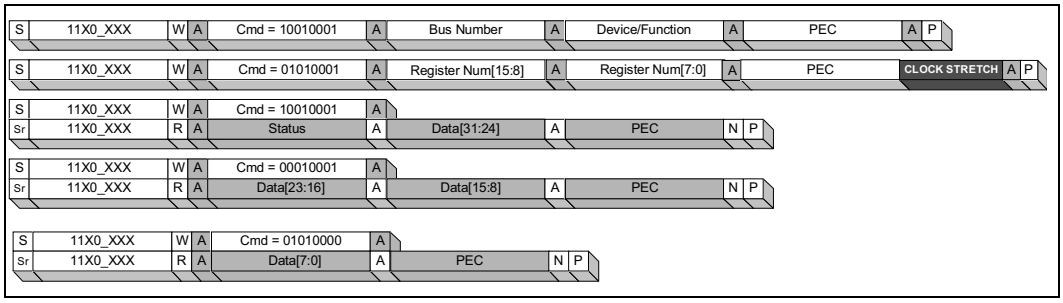


Figure 5-27. DWord Configuration Read Protocol (SMBus Block Write/Block Read, PEC Disabled)

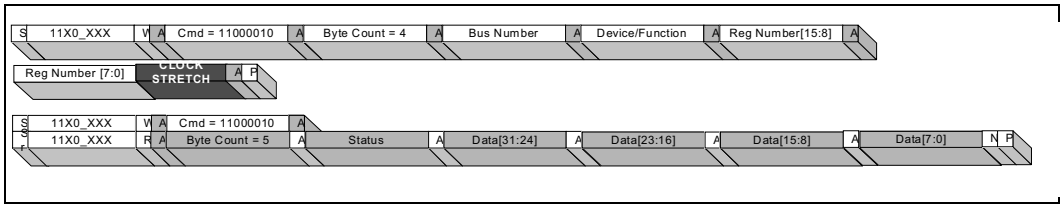


Figure 5-28. DWord Memory Read Protocol (SMBus Block Write/Block Read, PEC Disabled)

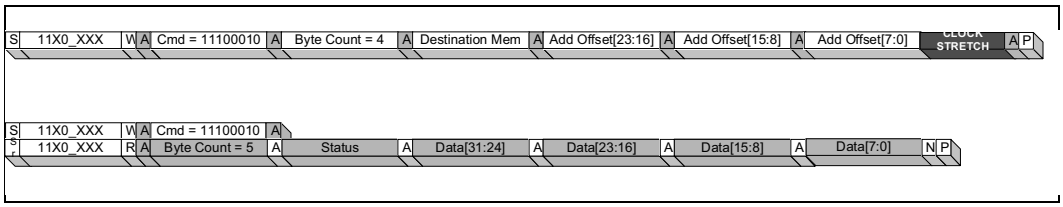
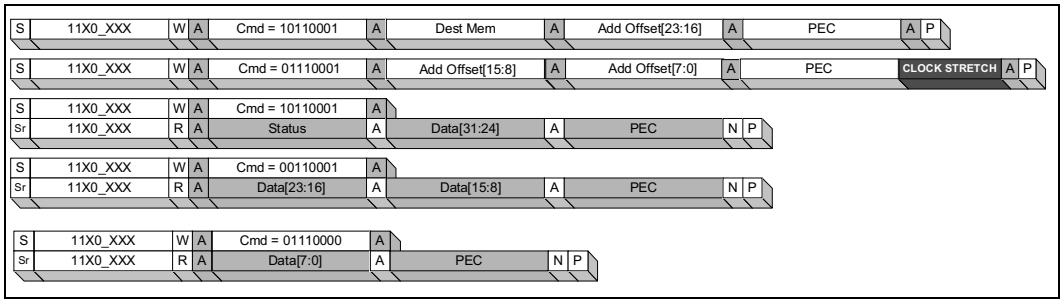


Figure 5-29. DWord Configuration Read Protocol (SMBus Word Write/Word Read, PEC Disabled)



5.22.2.4 Configuration and Memory Writes

Configuration and memory writes are accomplished through a series of SMBus writes. As with reads, a write sequence is first used to initialize the Bus Number, Device, Function, and Register Number for the configuration access and the destination memory, address offset for the memory write. The writing of this information can be accomplished through any combination of the supported SMBus write commands (Block, Word or Byte).

Note: On SMBus, there is no concept of byte enables. Therefore, the Register Number written to the Slave is assumed to be aligned to the length of the Internal Command. In other words, for a Write Byte internal command, the Register Number specifies the byte address. For a Write Dword internal command, the two least-significant bits of the Register Number are ignored. This is different from PCI where the byte enables are used to indicate the byte of interest.

After all the information is set up, the SMBus Master initiates one or more writes which sets up the data to be written. The final write (End bit is set) initiates an internal configuration or memory write. The Slave interface could potentially clock stretch the last data write until the write completes without error. If an error occurred, the SMBus interface NACKs the last write operation just before the stop bit.

Examples of configuration writes are illustrated below. Figure 5-30 to Figure 5-34 are with PEC Enabled. When PEC is disabled, there is no PEC byte in any of the sequences and the PEC enable bit in the command field is 0. For the definition of the diagram conventions below, refer to the *System Management Bus (SMBus) Specification, Version 2.0.*

Figure 5-30. DWord Configuration Write Protocol (SMBus Block Write, PEC Enabled)

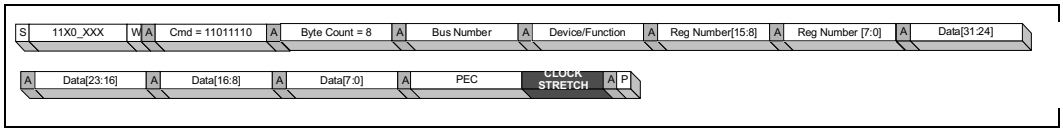


Figure 5-31. DWord Memory Write Protocol (SMBus Word Write, PEC Enabled)

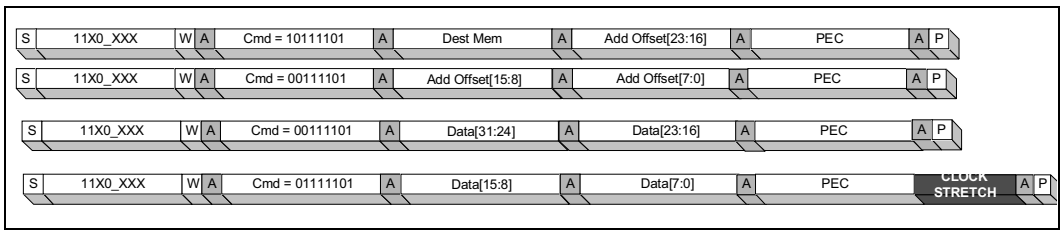


Figure 5-32. Word Configuration Write Protocol (SMBus Byte Write, PEC Enabled)

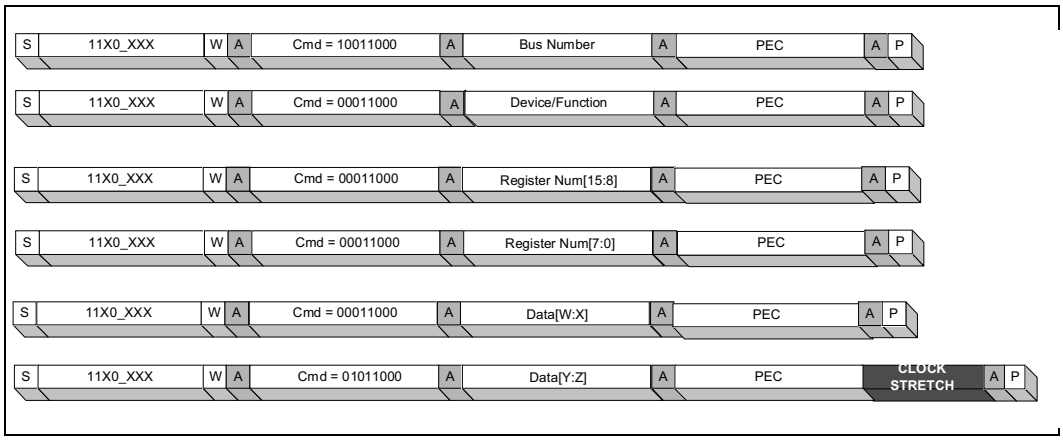


Figure 5-33. DWord Memory Read Protocol (SMBus Block Write / Block Read, PEC Disabled)

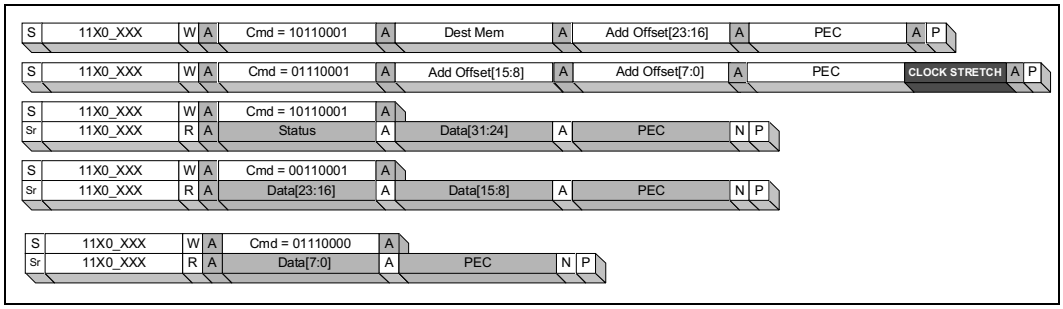
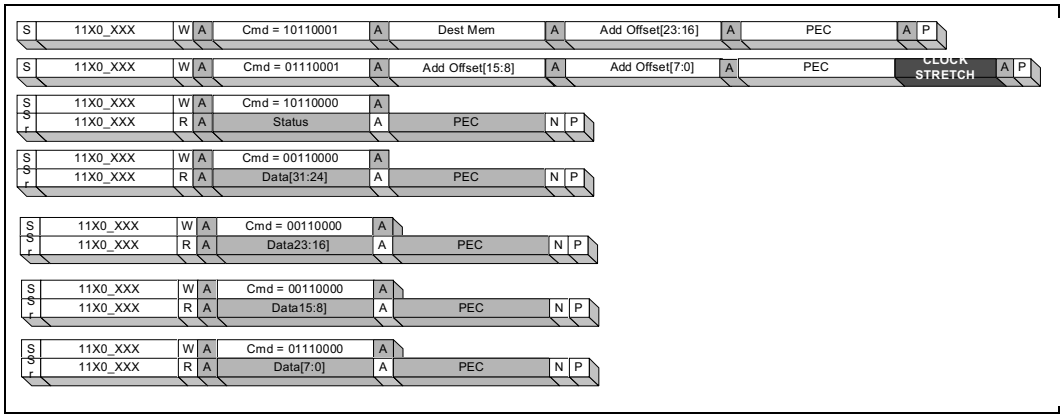


Figure 5-34. DWord Configuration Read Protocol (SMBus Word Write/Word Read, PEC Disabled)



5.22.2.5 Error Handling

The SMBus Slave interface handles two types of errors: internal and PEC. Internal errors can occur for example when the SMBus tries to access the APIC or SHPC config/memory space and these units in Intel® 631xESB/632xESB I/O Controller Hub are stuck servicing the PCI Express interface which is broke. Intel® 631xESB/632xESB I/O Controller Hub internally times out in such a case and this error manifests itself as a Not-Acknowledge (NACK) for the read or write command (End bit is set). Other internal errors include the read or write command receiving a Master or Target abort on the internal interface and these conditions also cause a NACK on the SMBus. If the Master receives a NACK, the entire transaction should be reattempted.

If the Master supports packet error checking (PEC) and the PEC enable bit in the command is set, then the PEC byte is checked in the Slave interface. If the check indicates a failure, then the Slave will NACK the PEC packet and not issue the command on the internal interface.

Note: An SMBus Master must either do PEC on all transactions in a sequence or not do it at all, that is, it cannot turn on PEC in the middle of a sequence.

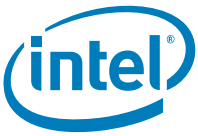
Note: A PEC error in the middle of a sequence must be re-started from the beginning of the sequence, that is, the begin bit set

5.22.2.6 SMBus Interface Reset

The Master in two ways can reset the Slave interface state machine in Intel® 631xESB/632xESB I/O Controller Hub:

- The Master holds SCL low for 25ms cumulative. Cumulative in this case means that all the "low time" for SCL is counted between the Start and Stop bit. If this totals 25ms before reaching the Stop bit, the interface is reset.
- The Master holds SCL continuously high for 50ms.

Besides these, the SMBus interface in Intel® 631xESB/632xESB I/O Controller Hub is also reset on a PWROK, RSTIN or an in-band warm reset from PCI Express.



5.22.2.7 Configuration Access Arbitration

If the CPU is currently accessing a unit, SM Bus cannot access it. Whoever gets in first wins arbitration. The other agent is stalled until the first agent finishes. The micro-architecture of this area is critical. The reason for the SM Bus interface is to access registers when the system may be unstable or locked, which can result with broken queues. Any register access through SM Bus must be able to proceed while the system is stuck.

5.23 AC'97 Controller (Audio D31:F5, Modem D31:F6)

Note: All references to AC'97 in this document refer to the *Audio Codec '97 Component Specification, Version 2.3.* For further information on the operation of the AC-link protocol, see the *Audio Codec '97 Component Specification, Version 2.3.*

The Intel® 631xESB/632xESB I/O Controller Hub AC'97 controller features include:

- Supports 20 bit samples for stereo PCM out
- Supports multiple sample rate AC'97 2.0 codecs (48 kHz and below)
- Independent PCI functions for audio and modem
- Independent Bus Master logic for dual Microphone input, dual PCM Audio input (2-channel stereo per input), PCM audio output (2-, 4- or 6-channel audio), Modem input, Modem output and S/PDIF output
- 20-bit sample resolution
- Support for 16 codec-implemented GPIOs
- Single modem line
- Configure up to three codecs with three ACZ_SDIN pins

Table 5-78 shows a detailed list of features supported by the Intel® 631xESB/632xESB I/O Controller Hub AC'97 digital controller

Table 5-78. Features Supported by Intel® 631xESB/632xESB I/O Controller Hub AC'97 Digital Controller

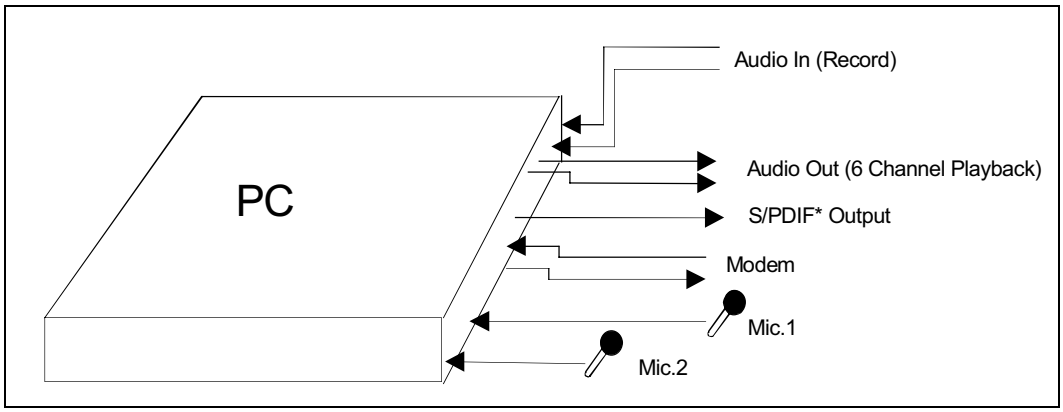
Feature	Description
System Interface	• Isochronous low latency Bus Master memory interface • Scatter/gather support for word-aligned buffers in memory (all mono or stereo 20-bit and 16-bit data types are supported, no 8-bit data types are supported) • Data buffer size in system memory from 3 to 65535 samples per input • Data buffer size in system memory from 0 to 65535 samples per output • Independent PCI audio and modem functions with configuration and I/O spaces • AC'97 codec registers are shadowed in system memory by way of driver • AC'97 codec register accesses are serialized by way of semaphore bit in PCI I/O space (new accesses are not allowed while a prior access is still in progress)
Power Management	• Power management by way of PCI Power Management
PCI Audio Function	• Read/write access to audio codec registers 00h–3Ah and vendor registers 5Ah–7Eh • 20-bit stereo PCM output, up to 48 kHz (L,R, Center, Sub-woofer, L-rear and R-rear channels on slots 3,4,6,7,8,9,10,11) • 16-bit stereo PCM input, up to 48 kHz (L,R channels on slots 3,4) • 16-bit mono mic in w/ or w/o mono mix, up to 48 kHz (L,R channel, slots 3,4) (mono mix supports mono hardware AEC reference for speakerphone) • 16-bit mono PCM input, up to 48 kHz from dedicated mic ADC (slot 6) (supports speech recognition or stereo hardware AEC ref for speakerphone) • During cold reset ACZ_RST# is held low until after POST and software deassertion of ACZ_RST# (supports passive PC_BEEP to speaker connection during POST)
PCI Modem function	• Read/write access to modem codec registers 3Ch–58h and vendor registers 5Ah–7Eh • 16-bit mono modem line1 output and input, up to 48 kHz (slot 5) • Low latency GPIO[15:0] by way of hardwired update between slot 12 and PCI I/O register • Programmable PCI interrupt on modem GPIO input changes by way of slot 12 GPIO_INT • SCI event generation on ACZ_SDIN[2:0] wake-up signal
AC-link	• AC'97 2.3 AC-link interface • Variable sample rate output support by way of AC'97 SLOTREQ protocol (slots 3,4,5,6,7,8,9,10,11) • Variable sample rate input support by way of monitoring of slot valid tag bits (slots 3,4,5,6) • 3.3 V digital operation meets AC'97 2.3 DC switching levels • AC-link I/O driver capability meets AC'97 2.3 triple codec specifications • Codec register status reads must be returned with data in the next AC-link frame, per *Audio Codec '97 Component Specification, Version 2.3*.
Multiple Codec	• Triple codec addressing: All AC'97 Audio codec register accesses are addressable to codec ID 00 (primary), codec ID 01 (secondary), or codec ID 10 (tertiary). • Modem codec addressing: All AC '97 Modem codec register accesses are addressable to codec ID 00 (primary) or codec ID 01 (secondary). • Triple codec receive capability by way of ACZ_SDIN[2:0] pins (ACZ_SDIN[2:0] frames are internally validated, synchronized, and OR'd depending on the Steer Enable bit status in the SDM register) • ACZ_SDIN mapping to DMA engine mapping capability allows for simultaneous input from two different audio codecs. ***Notes:*** 1. Audio Codec IDs are remappable and not limited to 00,01,10. 2. Modem Codec IDs are remappable and limited to 00, 01. 3. When using multiple codecs, the Modem Codec must be ID 01.

Note: Throughout this document, references to D31:F5 indicate that the audio function exists in PCI Device 31, Function 5. References to D31:F6 indicate that the modem function exists in PCI Device 31, Function 6.

Note: Throughout this document references to tertiary, third, or triple codecs refer to the third codec in the system connected to the ACZ_SDIN2 pin. The *Audio Codec '97*

Component Specification, Version 2.3 refers to non-primary codecs as multiple secondary codecs. To avoid confusion and excess verbiage, this datasheet refers to it as the third or tertiary codec.

Figure 5-35. Intel® 631xESB/632xESB I/O Controller Hub-Based Audio Codec'97 Specification, Version 2.3



5.23.1 PCI Power Management

This Power Management section applies for all AC'97 controller functions. After a power management event is detected, the AC'97 controller wakes the host system. The following sections describe these events and the AC'97 controller power states.

Device Power States

The AC'97 controller supports D0 and D3 PCI Power Management states. The following are notes regarding the AC'97 controller implementation of the Device States:

1. The AC'97 controller hardware does not inherently consume any more power when it is in the D0 state than it does in D3 state. However, software can halt the DMA engine prior to entering these low power states such that the maximum power consumption is reduced.
2. In the D0 state, all implemented AC'97 controller features are enabled.
3. In D3 state, accesses to the AC'97 controller memory-mapped or I/O range results in Master abort.
4. In D3 state, the AC'97 controller interrupt will never assert for any reason. The internal PME# signal is used to signal wake events, and so forth.
5. When the Device Power State field is written from $D3_{HOT}$ to D0, an internal reset is generated. See Section 20.1 for general rules on the effects of this reset.
6. AC'97 STS bit is set only when the audio or modem resume events were detected and their respective PME enable bits were set.
7. GPIO Status change interrupt no longer has a direct path to the AC'97 STS bit. This causes a wake up event only if the modem controller was in D3
8. Resume events on ACZ_SDIN[2:0] cause resume interrupt status bits to be set only if their respective controllers are not in D3.
9. Edge detect logic prevents the interrupts from being asserted in case the AC'97 controller is switched from D3 to D0 after a wake event.
10. Once the interrupt status bits are set, they will cause PIRQB# if their respective enable bits were set. One of the audio or the modem drivers will handle the interrupt.

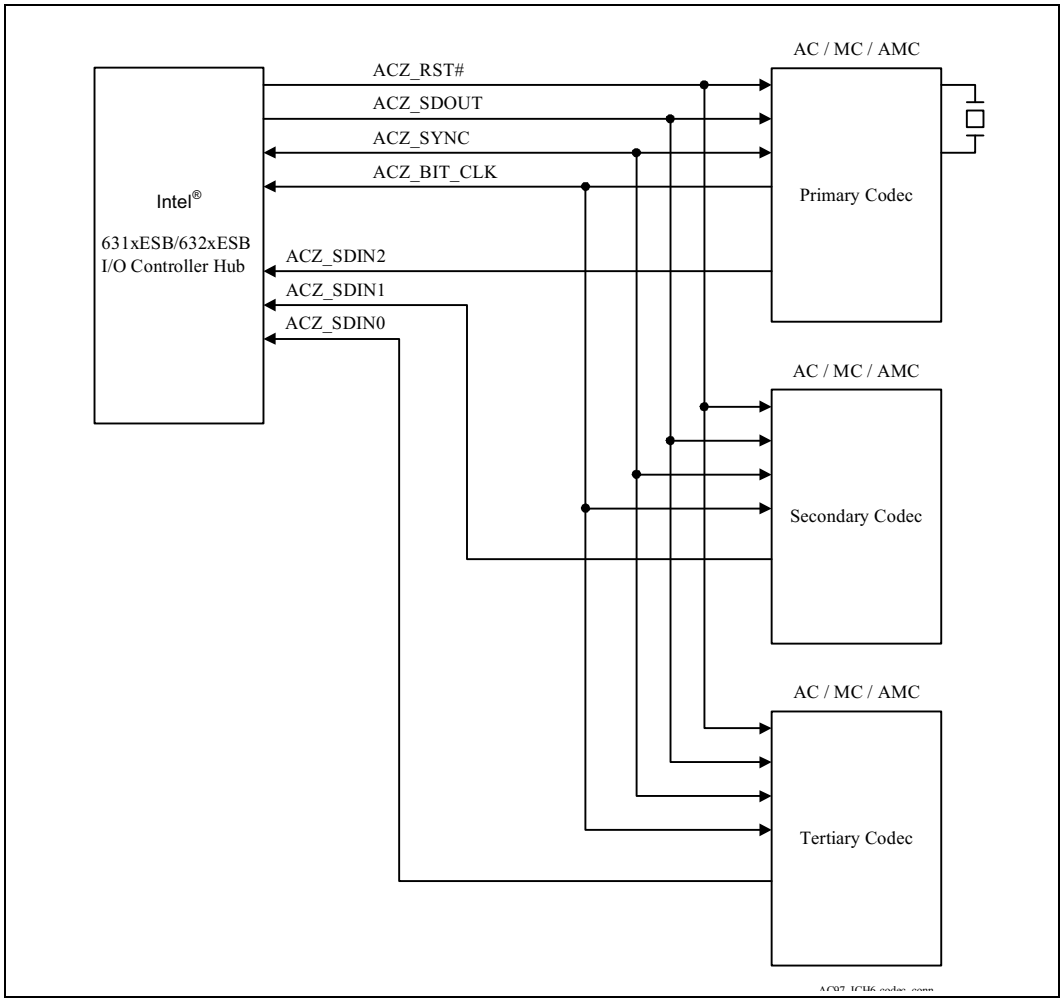
5.23.2 AC-Link Overview

The Intel® 631xESB/632xESB I/O Controller Hub is an AC'97 2.3 controller that communicates with companion codecs by way of a digital serial link called the AC-link. All digital audio/modem streams and command/status information is communicated over the AC-link.

The AC-link is a bi-directional, serial PCM digital stream. It handles multiple input and output data streams, as well as control register accesses, employing a time division multiplexed (TDM) scheme. The AC-link architecture provides for data transfer through individual frames transmitted in a serial fashion. Each frame is divided into 12 outgoing and 12 incoming data streams, or slots. The architecture of the Intel® 631xESB/632xESB I/O Controller Hub AC-link allows a maximum of three codecs to be connected. Figure 5-36 shows a three codec topology of the AC-link for the Intel® 631xESB/632xESB I/O Controller Hub. The AC-link consists of a five signal interface between the Intel® 631xESB/632xESB I/O Controller Hub and codec(s).

Note: The Intel® 631xESB/632xESB I/O Controller Hub's AC '97 controller shares the signal interface with the Intel High Definition Audio controller. However, only one controller may be enabled at a time.

Figure 5-36. AC'97 2.3 Controller-Codec Connection



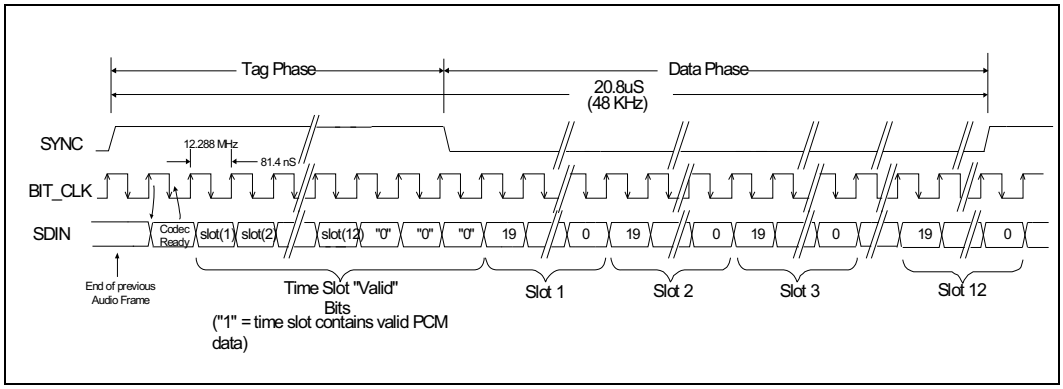
Intel® 631xESB/632xESB I/O Controller Hub core well outputs may be used as strapping options for the Intel® 631xESB/632xESB I/O Controller Hub, sampled during system reset. These signals may have weak pullups/pulldowns; however, this will not interfere with link operation. Intel® 631xESB/632xESB I/O Controller Hub inputs integrate weak pulldowns to prevent floating traces when a secondary and/or tertiary codec is not attached. When the Shut Off bit in the control register is set, all buffers will be turned off and the pins will be held in a steady state, based on these pullups/ pulldowns.

ACZ_BIT_CLK is fixed at 12.288 MHz and is sourced by the primary codec. It provides the necessary clocking to support the twelve 20-bit time slots. AC-link serial data is transitioned on each rising edge of ACZ_BIT_CLK. The receiver of AC-link data samples each serial bit on the falling edge of ACZ_BIT_CLK.

If ACZ_BIT_CLK makes no transitions for four consecutive PCI clocks, the Intel® 631xESB/632xESB I/O Controller Hub assumes the primary codec is not present or not working. It sets bit 28 of the Global Status Register (I/O offset 30h). All accesses to codec registers with this bit set will return data of FFh to prevent system hangs.

Synchronization of all AC-link data transactions is signaled by the AC'97 controller by way of the ACZ_SYNC signal, as shown in Figure 5-37. The primary codec drives the serial bit clock onto the AC-link, which the AC'97 controller then qualifies with the ACZ_SYNC signal to construct data frames. ACZ_SYNC, fixed at 48 kHz, is derived by dividing down ACZ_BIT_CLK. ACZ_SYNC remains high for a total duration of 16 ACZ_BIT_CLK at the beginning of each frame. The portion of the frame where ACZ_SYNC is high is defined as the tag phase. The remainder of the frame where ACZ_SYNC is low is defined as the data phase. Each data bit is sampled on the falling edge of ACZ_BIT_CLK.

Figure 5-37. AC-Link Protocol



The Intel® 631xESB/632xESB I/O Controller Hub has three ACZ_SDIN pins allowing a single, dual, or triple codec configuration. When multiple codecs are connected, the primary, secondary, and tertiary codecs can be connected to any ACZ_SDIN line. The Intel® 631xESB/632xESB I/O Controller Hub does not distinguish between codecs on its ACZ_SDIN[2:0] pins, however the registers do distinguish between ACZ_SDIN0, ACZ_SDIN1, and ACZ_SDIN2 for wake events, and so forth. If using a Modem Codec it is recommended to connect it to ACZ_SDIN1.

See your Platform Design Guide for a matrix of valid codec configurations. The Intel® 631xESB/632xESB I/O Controller Hub does not support optional test modes as outlined in the *Audio Codec '97 Component Specification, Version 2.3*.

5.23.2.1 Register Access

In the Intel® 631xESB/632xESB I/O Controller Hub implementation of the AC-link, up to three codecs can be connected to the SDOUT pin. The following mechanism is used to address the primary, secondary, and tertiary codecs individually.

The primary device uses bit 19 of slot 1 as the direction bit to specify read or write. Bits [18:12] of slot 1 are used for the register index. For I/O writes to the primary codec, the valid bits [14:13] for slots 1 and 2 must be set in slot 0, as shown in Table 5-79. Slot 1 is used to transmit the register address, and slot 2 is used to transmit data. For I/O reads to the primary codec, only slot 1 should be valid since only an address is transmitted. For I/O reads only slot 1 valid bit is set, while for I/O writes both slots 1 and 2 valid bits are set.

The secondary and tertiary codec registers are accessed using slots 1 and 2 as described above, however the slot valid bits for slots 1 and 2 are marked invalid in slot 0 and the codec ID bits [1:0] (bit 0 and bit 1 of slot 0) is set to a non-zero value. This allows the secondary or tertiary codec to monitor the slot valid bits of slots 1 and 2, and bits [1:0] of slot 0 to determine if the access is directed to the secondary or tertiary codec. If the register access is targeted to the secondary or tertiary codec, slot 1 and 2 will contain the address and data for the register access. Since slots 1 and 2 are marked invalid, the primary codec will ignore these accesses.

Table 5-79. Output Tag Slot 0

Bit	Primary Access Example	Secondary Access Example	Description
15	1	1	Frame Valid
14	1	0	Slot 1 Valid, Command Address bit (Primary codec only)
13	1	0	Slot 2 Valid, Command Data bit (Primary codec only)
12:3	X	X	Slot 3–12 Valid
2	0	0	Reserved
1:0	00	01	Codec ID (00 reserved for primary; 01 indicate secondary; 10 indicate tertiary)

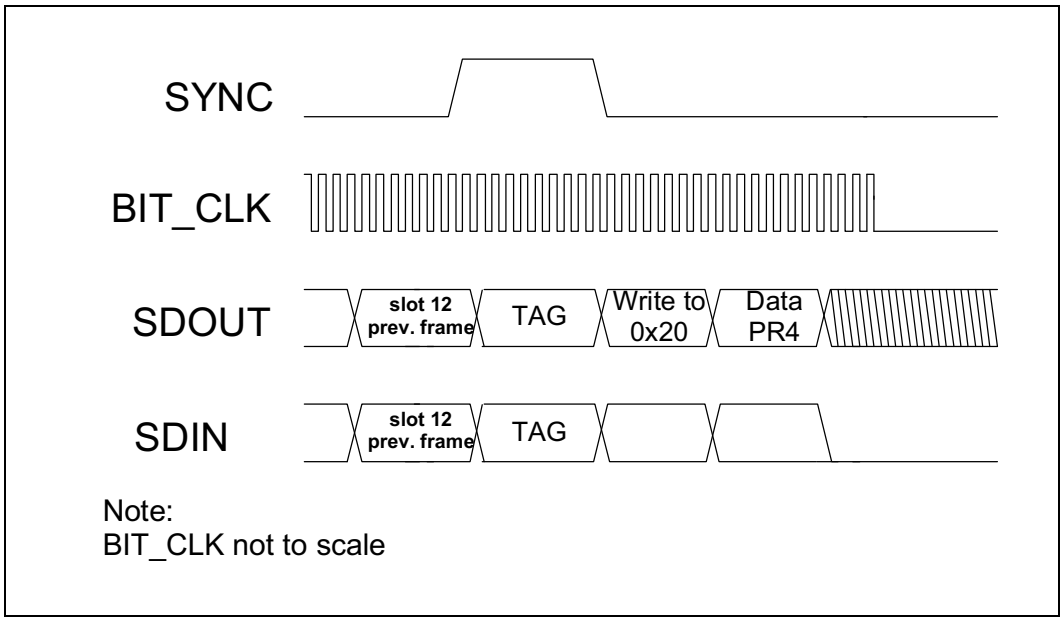
When accessing the codec registers, only one I/O cycle can be pending across the AC-link at any time. The Intel® 631xESB/632xESB I/O Controller Hub implements write posting on I/O writes across the AC-link (that is, writes across the link are indicated as complete before they are actually sent across the link). In order to prevent a second I/O write from occurring before the first one is complete, software must monitor the CAS bit in the Codec Access Semaphore register which indicates that a codec access is pending. Once the CAS bit is cleared, then another codec access (read or write) can go through. The exception to this being reads to offset 54h/D4h/154h (slot 12) which are returned immediately with the most recently received slot 12 data. Writes to offset 54h, D4h, and 154h (primary, secondary and tertiary codecs), get transmitted across the AC-link in slots 1 and 2 as a normal register access. Slot 12 is also updated immediately to reflect the data being written.

The controller does not issue back to back reads. It must get a response to the first read before issuing a second. In addition, codec reads and writes are executed only once across the link, and are not repeated.

5.23.3 AC-Link Low Power Mode

The AC-link signals can be placed in a low-power mode. When the AC'97 Powerdown register (26h), is programmed to the appropriate value, both ACZ_BIT_CLK and ACZ_SDIN will be brought to, and held at a logic low voltage level.

Figure 5-38. AC-Link Powerdown Timing



ACZ_BIT_CLK and ACZ_SDIN transition low immediately after a write to the Powerdown Register (26h) with PR4 enabled. When the AC'97 controller driver is at the point where it is ready to program the AC-link into its low-power mode, slots 1 and 2 are assumed to be the only valid stream in the audio output frame.

The AC'97 controller also drives ACZ_SYNC, and ACZ_SDOUT low after programming AC'97 to this low power, halted mode

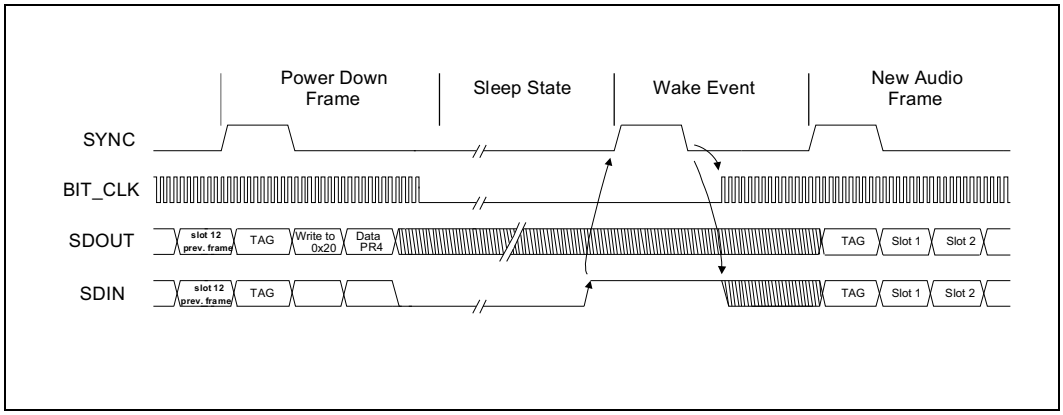
Once the codec has been instructed to halt, ACZ_BIT_CLK, a special wake up protocol must be used to bring the AC-link to the active mode since normal output and input frames can not be communicated in the absence of ACZ_BIT_CLK. Once in a low-power mode, the Intel® 631xESB/632xESB I/O Controller Hub provides three methods for waking up the AC-link; external wake event, cold reset and warm reset.

Note: Before entering any low-power mode where the link interface to the codec is expected to be powered down while the rest of the system is awake, the software must set the "Shut Off" bit in the control register.

5.23.3.1 External Wake Event

Codecs can signal the controller to wake the AC-link, and wake the system using ACZ_SDIN.

Figure 5-39. SDIN Wake Signaling



The minimum ACZ_SDIN wake up pulse width is 1 us. The rising edge of ACZ_SDIN0, ACZ_SDIN1 or ACZ_SDIN2 causes the Intel® 631xESB/632xESB I/O Controller Hub to sequence through an AC-link warm reset and set the AC97_STS bit in the GPE0_STS register to wake the system. The primary codec must wait to sample ACZ_SYNC high and low before restarting ACZ_BIT_CLK as diagrammed in Figure 5-39. The codec that signaled the wake event must keep its ACZ_SDIN high until it has sampled ACZ_SYNC having gone high, and then low.

The AC-link protocol provides for a cold reset and a warm reset. The type of reset used depends on the system's current power down state. Unless a cold or register reset (a write to the Reset register in the codec) is performed, wherein the AC'97 codec registers are initialized to their default values, registers are required to keep state during all power down modes.

Once powered down, activation of the AC-link by way of re-assertion of the ACZ_SYNC signal must not occur for a minimum of four audio frame times following the frame in which the power down was triggered. When AC-link powers up, it indicates readiness by way of the codec ready bit.

5.23.4 AC'97 Cold Reset

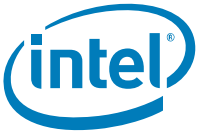
A cold reset is achieved by asserting ACZ_RST# for 1 µs. By driving ACZ_RST# low, ACZ_BIT_CLK, and ACZ_SDOUT will be activated and all codec registers will be initialized to their default power on reset values. ACZ_RST# is an asynchronous AC'97 input to the codec.

5.23.5 AC'97 Warm Reset

A warm reset re-activates the AC-link without altering the current codec register values. A warm reset is signaled by driving ACZ_SYNC high for a minimum of 1 µs in the absence of ACZ_BIT_CLK.

Within normal frames, ACZ_SYNC is a synchronous AC'97 input to the codec. However, in the absence of ACZ_BIT_CLK, ACZ_SYNC is treated as an asynchronous input to the codec used in the generation of a warm reset.

The codec must not respond with the activation of ACZ_BIT_CLK until ACZ_SYNC has been sampled low again by the codec. This prevents the false detection of a new frame.



Note: On receipt of wake up signalling from the codec, the digital controller issues an interrupt if enabled. Software then has to issue a warm or cold reset to the codec by setting the appropriate bit in the Global Control Register.

5.23.6 Hardware Assist to Determine ACZ_SDIN Used Per Codec

Software first performs a read to one of the audio codecs. The read request goes out on ACZ_SDOUT. Since the Intel® 631xESB/632xESB I/O Controller Hub allows one read to be performed at a time on the link, eventually the read data will come back in on one of the ACZ_SDIN[2:0] lines.

The codec does this by indicating that status data is valid in its TAG, then echoes the read address in slot 1 followed by the read data in slot 2.

The new function of the Intel® 631xESB/632xESB I/O Controller Hub hardware is to notice which ACZ_SDIN line contains the read return data, and to set new bits in the new register indicating which ACZ_SDIN line the register read data returned on. If it returned on ACZ_SDIN0, bits [1:0] contain the value 00. If it returned on ACZ_SDIN1, the bits contain the value 01, and so forth.

Intel® 631xESB/632xESB I/O Controller Hub hardware can set these bits every time register read data is returned from a function 5 read. No special command is necessary to cause the bits to be set. The new driver/BIOS software reads the bits from this register when it cares to, and can ignore it otherwise. When software is attempting to establish the codec-to-ACZ_SDIN mapping, it will single feed the read request and not pipeline to ensure it gets the right mapping, we cannot ensure the serialization of the access.

5.24 Intel® High Definition Audio Controller Overview

The Intel® 631xESB/632xESB I/O Controller Hub's Intel High Definition Audio controller shares pins with the AC'97 controller. However, only one controller may be enabled at a time.

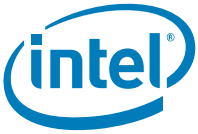
The Intel® 631xESB/632xESB I/O Controller Hub's controller communicates with the external codec(s) over the Intel High Definition Audio serial link. The controller consists of a set of DMA engines that are used to move samples of digitally encoded data between system memory and an external codec(s). The Intel® 631xESB/632xESB I/O Controller Hub implements four output DMA engines and 4 input DMA engines. The output DMA engines move digital data from system memory to a D-A converter in a codec. Intel® 631xESB/632xESB I/O Controller Hub implements a single Serial Data Output signal (ACZ_SDO) that is connected to all external codecs. The input DMA engines move digital data from the A-D converter in the codec to system memory. The Intel® 631xESB/632xESB I/O Controller Hub implements three Serial Digital Input signals (ACZ_SDI[2:0]) supporting up to three codecs.

Audio software renders outbound and processes inbound data to/from buffers in system memory. The location of individual buffers is described by a Buffer Descriptor List (BDL) that is fetched and processed by the controller. The data in the buffers is arranged in a predefined format. The output DMA engines fetch the digital data from memory and reformat it based on the programmed sample rate, bit/sample and number of channels. The data from the output DMA engines is then combined and serially sent to the external codecs over the Intel High Definition Audio link. The input DMA engines receive data from the codecs over the Intel High Definition Audio link and format the data based on the programmable attributes for that stream. The data is then written to memory in the predefined format for software to process. Each DMA

engine moves one stream of data. A single codec can accept or generate multiple streams of data, one for each A-D or D-A converter in the codec. Multiple codecs can accept the same output stream processed by a single DMA engine.

Codec commands and responses are also transported to and from the codecs by way of DMA engines.

§



6 Electrical Characteristics

This document only contains DC characteristics information. Please refer to *RS - Intel® 631xESB/632xESB I/O Controller Hub* EDS Addendum for AC characteristics (including AC timing diagrams for Intel® 631xESB/632xESB I/O Controller Hub).

Table 6-1. Intel® 631xESB/632xESB I/O Controller Hub Power Consumption Estimates with Wake-on-LAN (LAN tied to AUX power)

Platform Voltage Rail	Current in S0	Current in S3	Current in S4	Current in S5	Current in G3
Logic 1.5V Core	3.82 A	N/A	N/A	N/A	N/A
I/O 1.5V Core	1.98A	N/A	N/A	N/A	N/A
1.5V Aux	1.97A	0.62A	N/A	N/A	N/A
3.3V Core	1.8A	N/A	N/A	N/A	N/A
3.3V Sus	70mA	30mA	40mA	40mA	N/A
3.3V Aux	0.27A	0.07A	N/A	N/A	N/A
Vcc5REF	150uA	N/A	N/A	N/A	N/A
Vcc5REFSus	10mA	10mA	10mA	10mA	OFF
VccRTC	N/A	N/A	N/A	N/A	6uA

Table 6-2. Intel® 631xESB/632xESB I/O Controller Hub Power Consumption Estimates with Wake-on-LAN (LAN tied to CORE power)

Platform Voltage Rail	Current in S0	Current in S3	Current in S4	Current in S5	Current in G3
Logic 1.5V Core	5.54A	N/A	N/A	N/A	N/A
I/O 1.5V Core	2.23A	N/A	N/A	N/A	N/A
1.5V Aux	2.07	N/A	N/A	N/A	N/A
3.3V Core	N/A	N/A	N/A	N/A	N/A
3.3V Sus	70mA	30mA	40mA	40mA	N/A
3.3V Aux	N/A	N/A	N/A	N/A	N/A
Vcc5REF	150uA	N/A	N/A	N/A	N/A
Vcc5REFSus	10mA	10mA	10mA	10mA	N/A
VccRTC	N/A	N/A	N/A	N/A	6uA

Notes:
1. These numbers are pre-silicon estimates. Actual numbers will be included after measured.
2. The current numbers shown above are based on a X8 uPCI Express connection to the MCH, if a X4 uPCI Express connection is used, subtract 240 mA for the 1.5 V current draw.
3. Internal 2.5 V and 1.5 VSUS are assumed enabled: 1.5 VSUS rails (VCCSUS1/VCCSUS2/VCCUSB via INTVRMEN) as well as 2.5 V rails (VCCP25IDE and VCCP25PCI via GIO[25])
4. These numbers assume worst case RMS values

Table 6-3. DC Characteristic Input Signal Association

Symbol	Associated Signals
V_{IH1}/V_{IL1} (5 V Tolerant)	**PCI Signals:** AD[31:0], CBE[3:0]#, DEVSEL#, FRAME#, IRDY#, TRDY#, STOP#, PAR, PERR#, PLOCK#, SERR#, REQ[3:0]#, REQ[4}#/GPI[40], REQ[5}#/GPI[1], REQ[6}#/GPI[0] **PCI-X Signals:** PX133EN, PXAD[63:0], PxPME#, PXCBE[7:0]#, PXDEVSEL#, PXFRAME#, PXIRDY#, PXM66EN, PXPAR, PXPCIXCAP, PXPERR#, PXPLOCK#, PXPME#, PXREQ[5:0]#, PXSERR#, PXSTOP#, PXTRDY#, PXACK64#, PXPAR64, PXREQ64# **Interrupt Signals:** PIRQ[D:A]#,P IRQ[H:E]#/GPI[5:2] (open drain)
V_{IH2}/V_{IL2} (5 V Tolerant)	**Interrupt Signals:** IDEIRQ
V_{IH3}/V_{IL3}	**Clock Signals:** CLK48, CLK14 **Power Management Signals:** MCH_SYNC#, THRM#, VRMPWRGD **SATA Signals:** SATAGP[3:0]/GPI[31:29,26] **GPIO Signals:** GPI[13,12,8], GPIO[34,33]
V_{IH4}/V_{IL4}	**Clock Signals:** PCICLK, **LPC/Firmware Hub Signals:** LAD[3:0]/FWH[3:0],L DRQ[0]#, LDRQ[1]#/ GPI[41] **Power Management Signals:** LAN_PWR_GOOD **GPIO Signals:** Desktop: GPI[32,7,6] **Interrupt Signals:** SERIRQ **CPU Signals:** A20GATE,RCIN# **USB Signals:** OC[3:0]#,OC [5:4]#/GPI[10:9],OC [7:6]#/GPI[15:14]
V_{IH5}/V_{IL5}	**SMBus Signals:** SMBCLK, SMBDATA **System Management Signals:** SMBALERT#/GPI[11],SM LINK[1:0]
V_{IL6}/V_{IH6}	**LAN Signals:** SERN[1:0], SERP[1:0], SER_CLK_IN **Flash and EEPROM Signals:** FLSH_SO, EE_DO **Expansion Bus signals**: EBUS_AD[24:0] **RS-232 Signals**: RS232_CTS, RS232_DCD, RS232_DSR, RS232_RI, RS232_SIN
V_{IL7}/V_{IH7}	**Processor Signals:** FERR#, THRMTRIP#
V_{IMIN8}/V_{IMAX8}	**Enterprise Southbridge Interface Signals**: ESI[3:0]RX(P,N)
V_{IL9}/V_{IH9}	**Real Time Clock Signals:** RTCX1
VIMIN10/VIMAX10	**SATA Signals:** SATA[3:0]RX[P,N]
VIL11/VIH11	**AC'97/Intel® High Definition Audio Signals:** ACZ_SDIN[2:0] **AC'97 Signals:** ACZ_BIT_CLK
V_{IL12}/V_{IH12} /$V_{cross(abs)}$	**Clock Signals:** ESI_CLK100N, ESI_CLK100P, SATA_CLKN, SATA_CLKP
V_{IL13}/V_{IH13}	**Power Management Signals:** PWRBTN#, RI# SYS_RESET#, WAKE# **System Management Signals:** LINKALERT# **GPIO Signals:** GPIO[28, 27, 25, 24] **Other Signals:** TP[3]
V_{IL14}/V_{IH14}	**Power Management Signals:** PWROK, RSMRST#, RTCRST# **System Management Signals:** INTRUDER# **Other Signals:** INTVRMEN
V_{DI} / V_{CM} / V_{SE} (5 V Tolerant)	**USB Signals:** USBP[7:0][P,N] (Low-speed and Full-speed)
V_{HSSQ} / V_{HSDSC} / V_{HSCM} (5 V Tolerant)	**USB Signals:** USBP[7:0][P,N] (in High-speed Mode)

Table 6-4. DC Input Characteristics (Sheet 1 of 2)

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL1}	Input Low Voltage	−0.5	0.3*(Vcc33)	V	Note 9
V_{IH1}	Input High Voltage	0.5*(Vcc33)	V5REF + 0.5	V	
V_{IL2}	Input Low Voltage	−0.5	0.8	V	
V_{IH2}	Input High Voltage	2.0	V5REF + 0.5	V	
V_{IL3}	Input Low Voltage	−0.5	0.8	V	
V_{IH3}	Input High Voltage	2.0	Vcc33 + 0.5	V	
V_{IL4}	Input Low Voltage	−0.5	0.3*(Vcc33)	V	
V_{IH4}	Input High Voltage	0.5*(Vcc33)	Vcc33 + 0.5	V	
V_{IL5}	Input Low Voltage	−0.5	0.8	V	
V_{IH5}	Input High Voltage	2.1	VCCPSUS + 0.5	V	
V_{IL6}	Input Low Voltage	−0.5	0.3(Vcc33)	V	
V_{IH6}	Input High Voltage	0.6(Vcc33)	Vcc33 + 0.5	V	
V_{IL7}	Input Low Voltage	−0.5	0.58(V_CPU_IO)	V	
V_{IH7}	Input High Voltage	0.73(V_CPU_IO)	V_CPU_IO+0.5	V	
V_{IMIN8}	Minimum Input Voltage	175		mVp-p	Note 6
V_{IMAX8}	Maximum Input Voltage		1200	mVp-p	Note 6
V_{IL9}	Input Low Voltage	−0.5	0.10	V	
V_{IH9}	Input High Voltage	0.40	1.2	V	
V_{IMIN10}	Minimum Input Voltage	325		mVp-p	Note 7
V_{IMAX10}	Maximum Input Voltage		600	mVp-p	Note 7
V_{IL11}	Input Low Voltage	−0.5	0.35(Vcc33)	V	
V_{IH11}	Input High Voltage	0.65(Vcc33)	(Vcc33)+0.5	V	
V_{IL12}	Input Low Voltage	−0.150	0.150	V	
V_{IH12}	Input High Voltage	0.660	0.850	V	
V_{IL13}	Input Low Voltage	-0.5	0.8	V	
V_{IH13}	Input High Voltage	2.0	VCCPSUS+0.5	V	
V_{IL14}	Input Low Voltage	-0.5	0.8	V	
V_{IH14}	Input High Voltage	2.0	VccRTC+0.5	V	Note 8
$V_{Cross(abs)}$	Absolute Crossing Point	0.250	0.550	V	
V+	Low to high input threshold	1.5	2.0	V	Note 1
V−	High to low input threshold	1.0	1.5	V	Note 1
VHYS	Difference between input thresholds: (V+current value) − (V− current value)	320		mV	Note 1
VTHRAVG	Average of thresholds: ((V+current value) + (V− current value))/2	1.3	1.7	V	Note 1
VRING	AC Voltage at recipient connector	−1	6	V	Note 1,2
V_{DI}	Differential Input Sensitivity	0.2		V	Note 3,5
V_{CM}	Differential Common Mode Range	0.8	2.5	V	Note 4,5

Table 6-4. DC Input Characteristics (Sheet 2 of 2)

Symbol	Parameter	Min	Max	Unit	Notes
V_{SE}	Single-Ended Receiver Threshold	0.8	2.0	V	Note 5
V_{HSSQ}	HS Squelch Detection Threshold	100	150	mV	Note 5
V_{HSDSC}	HS Disconnect Detection Threshold	525	625	mV	Note 5
V_{HSCM}	HS Data Signaling Common Mode Voltage Range	−50	500	mV	Note 5
V_{HSSQ}	HS Squelch detection threshold	100	150	mV	Note 5
V_{HSDSC}	HS disconnect detection threshold	525	625	mV	Note 5
V_{HSCM}	HS data signaling common mode voltage range	−50	500	mV	Note 5

Notes:
1. Applies to Ultra DMA Modes greater than Ultra DMA Mode 4
2. This is an AC Characteristic that represents transient values for these signals
3. VDI = | USBPx[P] USBPx[N]
4. Includes VDI range
5. Applies to High-speed USB 2.0
6. PCI Express* mVdiff p-p = |PETp[x] - PETn[x]|
7. SATA Vdiff, tx (VIMAX/MIN10 is measured at the SATA connector on the transmit side (generally, the motherboard connector), where SATA mVdiff p-p = |SATA[x]TXP/RXP - SATA[x]TXN/RXN|
8. VccRTC is the voltage applied to the VccTRC well of the Intel® 631xESB/632xESB I/O Controller Hub. When the system is in a G3 state, this is generally supplied by the coin cell battery, but for S5 and greater, this is generally by VCCPSUS.
9. For PCI-X* signals, V_{IL1}=0.35*(Vcc33).

Table 6-5. DC Characteristic Output Signal Association (Sheet 1 of 2)

Symbol	Associated Signals
V_{OH1}/V_{OL1}	**IDE Signals:** DD[15:0], DIOW#/DSTOP, DIOR#/DWSTB/RDMARDY, DDACK#, DA[2:0], DCS[3,1]#
V_{OH2}/V_{OL2}	**Processor Signals:** A20M#, CPUSLP#, IGNNE#, INIT#, INTR, NMI, SMI#, STPCLK#
V_{OH3}/V_{OL3}	**PCI Signals:** AD[31:0],C/BE[3:0]#,DEVSEL#, FRAME#,IRDY#, PAR,PERR#, PLOCK#,SERR#,STOP#,TRDY# **PCI-X Signals**: PXPCLKO[6:0], RSTIN#, **AC'97/High Definition Audio Signals:** ACZ_RST#, ACZ_SDOUT, ACZ_SYNC **High Definition Audio Signals:** ACZ_BIT_CLK
V_{OL4}/V_{OH4}	**SMBus Signals:** SMBCLK (1), SMBDATA (1) **System Management Signals:** SMLINK[1:0](1)
V_{OL5}/V_{OH5}	**Power Management Signals:** PLTRST#,SL P_S3#, SLP_S4#,SL P_S5#,SU SCLK#, SUS_STAT# **GPIO Signals:** GPO[24,23,20:18], GPIO[34,33,28,27,25] **Other Signals:** SPKR **SATA Signal:** SATALED# **Processor Interface Signal:** INIT3_3V# **LAN Signals:** LAN_PWR_GOOD, SETN[1:0], SETP[1:0] **Flash and EEPROM Signals:** FLSH_SI, FLSH_SCK, FLSH_CE#, EE_CS#, EE_DI, EE_SK **Expansion Bus signals**: EBUS_ADV#/EBUS_RAS#, EBUS_ALAT/EBUS_CKE, EBUS_BE_[1:0]#, EBUS_CE_[2:1]#, EBUS_CLK_2, EBUS_FRST#, EBUS_OE#/ EBUS_CAS#, EBUS_WE# **RS-232 Signals**: RS232_DTR, RS232_RTS, RS232_SOUT
V_{OL6}/V_{OH6}	**USB Signals:** USBP[7:0][P,N] in Low and Full Speed Modes
V_{OMIN7}/V_{OMAX7}	**Enterprise Southbridge Interface Signals:** ESI[3:0]TX(P,N)

Table 6-5. DC Characteristic Output Signal Association (Sheet 2 of 2)

Symbol	Associated Signals
V_{OMIN8}/V_{OMAX8}	**SATA Signals:** SATA[3:0]TX[P,N]
V_{OL9}/V_{OH9}	**LPC/Firmware Hub Signals:** LAD[3:0]/FWH[3:0], LFRAME#/FWH[4] **PCI Signals:** PCIRST#, GNT[3:0]#, GNT[4]/GPIO[48], GNT[5]/GPO[17], GNT[6]/ GPO[16] **GPIO Signals:** GPO[21], GPIO[32] PCI-X Signals: PXGNT[5:0]#, PXPCIRST#
V_{OL10}/V_{OH10}	**Processor Signal:** CPUPWRGD/GPO[49](1)
V_{HSOI} V_{HSOH} V_{HSOL} V_{CHIRPJ} V_{CHIRPK}	**USB Signals:** USBP[7:0][P:N] in High Speed Modes

Note: These signals are open drain.

Table 6-6. DC Output Characteristics

Symbol	Parameter	Min	Max	Unit	I_{OL} / I_{OH}	Notes
V_{OL1}	Output Low Voltage		0.51	V		
V_{OH1}	Output High Voltage	Vcc33 – 0.51		V		
V_{OL2}	Output Low Voltage		0.255	V	3 mA	
V_{OH2}	Output High Voltage	V_CPU_IO-0.3		V	-0.3 mA	Note 1
V_{OL3}	Output Low Voltage		0.1(Vcc33)	V	6 mA	
V_{OH3}	Output High Voltage	0.9(Vcc33)		V	-0.5 mA	
V_{OL4}	Output Low Voltage		0.4	V	4 mA	
V_{OH4}	Output High Voltage	VCCPSUS - 0.5		V	2 mA	Note 1
V_{OL5}	Output Low Voltage		0.4	V	6 mA	
V_{OH5}	Output High Voltage	Vcc33 - 0.5		V	-2 mA	Note 1
V_{OL6}	Output Low Voltage		0.4	V	5 mA	
V_{OH6}	Output High Voltage	Vcc33 – 0.5		V	-2 mA	Note 1
V_{OMIN7}	Minimum Output Voltage	800		mVp-p		Note 2
V_{OMAX7}	Maximum Output Voltage		1200	mVp-p		Note 2
V_{OMIN8}	Minimum Output Voltage	400		mVp-p		Note 3
V_{OMAX8}	Maximum Output Voltage		600	mVp-p		Note 3
V_{OL9}	Output Low Voltage		0.1(Vcc33)	V	1.5 mA	
V_{OH9}	Output High Voltage	0.9(Vcc33)		V	-0.5 mA	
V_{OL10}	Output Low Voltage		0.25		6 mA	Note 4
V_{OH10}	Output High Voltage					Note 1
V_{HSOI}	HS Idle Level	–10.0	10.0	mV		
V_{HSOH}	HS Data Signaling High	360	440	mV		
V_{HSOL}	HS Data Signaling Low	–10.0	10.0	mV		
V_{CHIRPJ}	Chirp J Level	700	1100	mV		
V_{CHIRPK}	Chirp K Level	–900	–500	mV		

Notes:
1. The CPUPWRGD, SERR#, PIRQ[A:H], SMBDATA, SMBCLK, LINKALERT#, and SMLINK[1:0] signal has an open drain driver and SATALED# has an open collector driver, and the V_{OH} spec does not apply. This signal must have external pull up resistor.
2. PCI Express* mVdiff p-p = |PETp[x] - PETn[x]
3. SATA Vdiff, Tx (VOMAX/MIN8)is measured at the SATA connector on the transmit side (generally, the motherboard connector), where SATA mVdiff p-p = |SATA[x]TXP/RXP - SATA[x]TXN/RXN|
4. Maximum **Iol** for CPUPWRGD is 12 mA for short durations (<500 mS per 1.5 S) and 9 mA for long durations.

Table 6-7. Other DC Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
V5REF	Intel® 631xESB/632xESB I/O Controller Hub Core Well Reference Voltage	4.75	5.25	V	
Vcc33	I/O Buffer Voltage	3.135	3.465	V	Note 2
V_CPU_IO	Processor I/F	1.0	1.425	V	
V5REF_Sus	Suspend Well Reference Voltage	4.75	5.25	V	
VccPSUS	Suspend Well I/O Buffer Voltage	3.135	3.465	V	Note 2
VccAUX3_3	**BMC IO supply**	3.135	3.465	V	
VccRTC	Battery Voltage	2.0	3.6	V	
V_{IT+}	Hysteresis Input Rising Threshold	1.9		V	Applied to USBP[7:0][P,N]
V_{IT-}	Hysteresis Input Falling Threshold		1.3	V	Applied to USBP[7:0]P,N]
V_{DI}	Differential Input Sensitivity	0.2		V	|(USBPx+,USBPx–)|
V_{CM}	Differential Common Mode Range	0.8	2.5	V	Includes V_{DI}
V_{CRS}	Output Signal Crossover Voltage	1.3	2.0	V	
V_{SE}	Single Ended Rcvr Threshold	0.8	2.0	V	
I_{LI1}	ATA Input Leakage Current	–200	200	µA	(0 V < V_{IN} < 5 V)
I_{LI2}	PCI_3V Hi-Z State Data Line Leakage	–10	10	µA	(0 V < V_{IN} < 3.3 V)
I_{LI3}	PCI_5V Hi-Z State Data Line Leakage	–70	70	µA	Max V_{IN} = 2.7 V Min V_{IN} = 0.5 V
I_{LI4}	Input Leakage Current – Clock signals	–100	+100	µA	Note 1
C_{IN}	Input Capacitance – All Other		12	pF	F_C = 1 MHz
C_{OUT}	Output Capacitance		12	pF	F_C = 1 MHz
$C_{I/O}$	I/O Capacitance		12	pF	F_C = 1 MHz
		Typical Value			
C_L	XTAL1	6		pF	
C_L	XTAL2	6		pF	

Note:
1. Includes CLK14, CLK48, LAN_CLK and PCICLK.
2. VccAUBG, VccBGESI, VccA3_3 and VccASATABG are filtered voltages attached to the same source as Vcc33/VccPSUS, and must meet the same voltage tolerance at the input to their filters.

Table 6-8. Intel® 631xESB/632xESB I/O Controller Hub 1.5 V Supply Rail Tolerances

Symbol	Parameter	AC Min	DC Min	Nom	DC Max	ACMax	Unit	Notes
Vcc, VccSUS2, VREFPCI	1.5 V Supply Voltage	1.425	1.455	1.5	1.575	1.605	V	Note 1&2

Notes:
1. VccAPE, VccAUPLL, VccAPLL1_5 and VccAESI are filtered voltages attached to the same source as Vcc1_5/ VccSus1_5, and must meet the same voltage tolerance at the input to their filters.
2. If VccSUS is tied to VAUX, the tolerance spec for VccSUS will be +/– 3%.

Table 6-9. PCI Express* Differential Transmitter (TX) DC Output Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
$V_{TX-DIFFp-p}$	Differential Peak to Peak Output Voltage	0.800		1.2	V	$V_{TX-DIFFp-p} = 2*\|V_{TX-D+} - V_{TX-D-}\|$ See Note 1.
$V_{TX-DE-RATIO}$	De-Emphasized Differential Output Voltage (Ratio)	-3.0	-3.5	-4.0	dB	This is the ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition See Note 1.
$V_{TX-CM-ACp}$	AC Peak Common Mode Output Voltage			20	mV	$V_{TX-CM-ACp} = \|V_{TX-D+} + v_{TX-D-}\| / 2 - v_{TX-CM-DC}$ $v_{TX-CM-DC} = DC_{(avg)}$ of $\|V_{TX-D+} + V_{TX-D-}\| / 2$ See Note 1.
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	0		100	mV	$\|V_{TX-CM-DC-} V_{TX-CM-Idle-DC[During Electrical Idle]}\| = 100$ mV $V_{TX-CM-DC} = DC_{(avg)}$ of $\|V_{TX-D+} + V_{TX-D-}\| / 2$ [Electrical Idle] See Note 1.
$V_{TX-CM-DC-LINE-DELTA}$	Absolute Delta of DC Common Mode Voltage between D+ and D-.	0		25	mV	$\|V_{TX-CM-DC-D+} - V_{TX-CM-DC-D-}\| =$ 25 mV $V_{TX-CM-DC-D+} = DC_{(avg)}$ of $\|V_{TX-D+}\|$ $V_{TX-CM-DC-D-} = DC_{(avg)}$ of $\|V_{TX-D-}\|$ See Note 1.
$V_{TX-IDLE-DIFFp}$	Electrical Idle Differential Peak Output Voltage	0		20	mV	$V_{TX-IDLE-DIFFp} = \|V_{TX-Idle-D+} - V_{Tx-Idle-D-}\| = 20$ mV See Note 1.
$V_{TX-RCV-DETECT}$	Amount of voltage change allowed during Receiver Detection			600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance receiver is present.
$RL_{TX-DIFF}$	Differential Return Loss	12			dB	Measured over 50 MHz to 1.25 GHz See Note 2.
RL_{TX-CM}	Common Mode Return Loss	6			dB	Measured over 50 MHz to 1.25 GHz See Note 2.
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance	80	100	120	W	TX DC Differential Mode Low impedance
$Z_{TX-COM-DC}$	Transmitter Common Mode High Impedance State (DC)	40 k			W	Required TX D+ as well as D- DC impedance during all states.
C_{TX}	AC Coupling Capacitor	75		200	nF	All transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.

Notes:

1. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 6-1 and measured over any 250 consecutive TX UIs. (Also refer to the Transmitter Compliance Eye Diagram as shown in Figure 6-2.)
2. The transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 Ω probes – see Figure 6-1). Note that the series capacitors C_{TX} is optional for the return loss measurement.

Figure 6-1. Compliance Test/Measurement Load

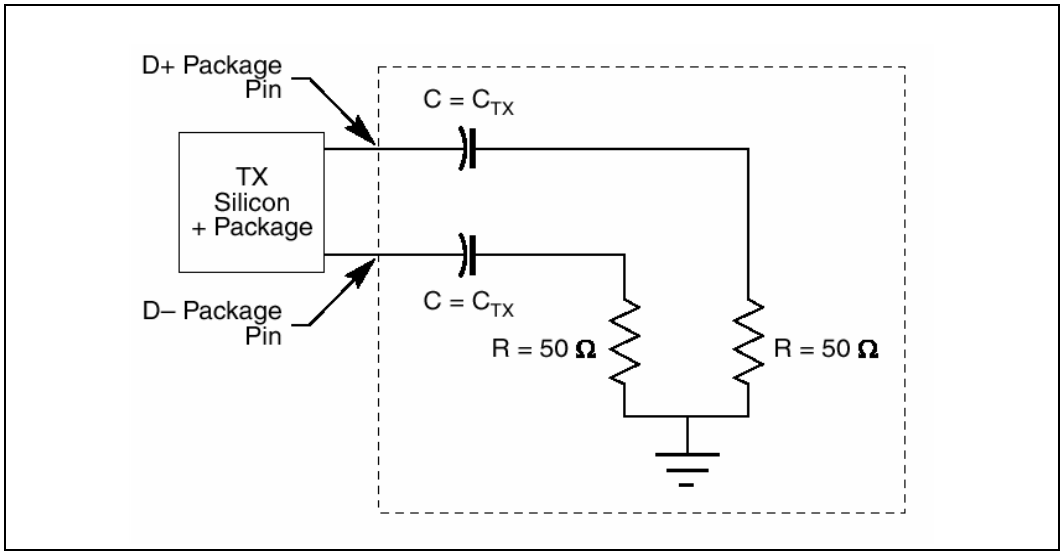


Figure 6-2. Minimum Transmitter Timing and Voltage Output Compliance Specification

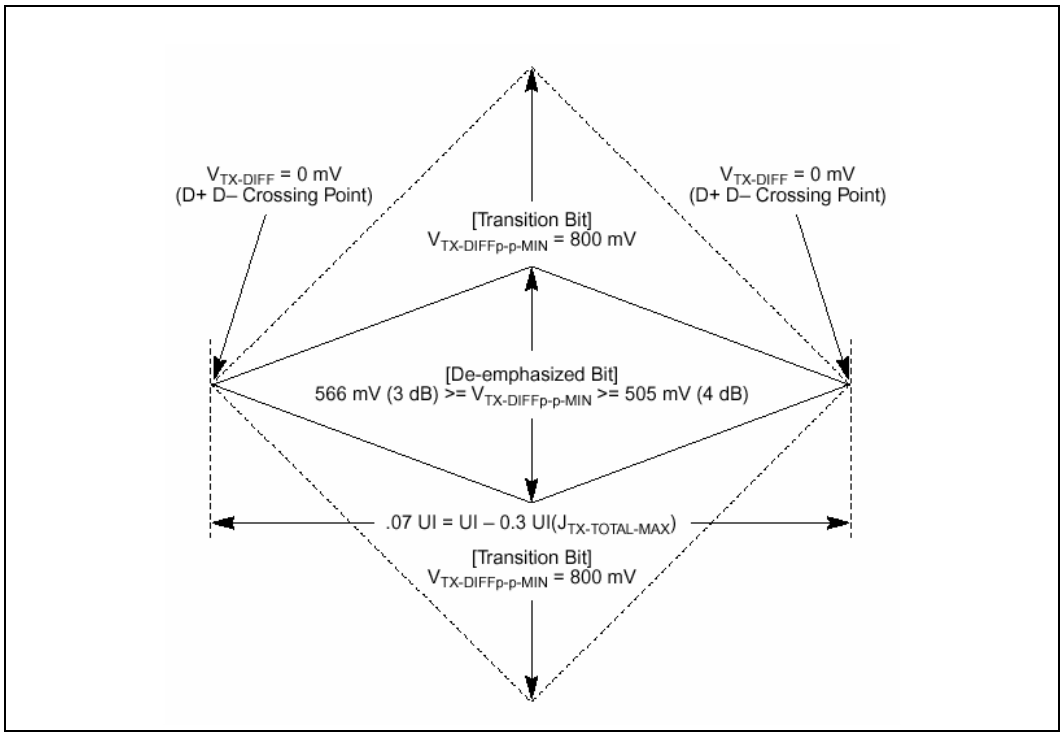


Figure 6-3. Minimum Receiver Eye Timing and Voltage Compliance Specification

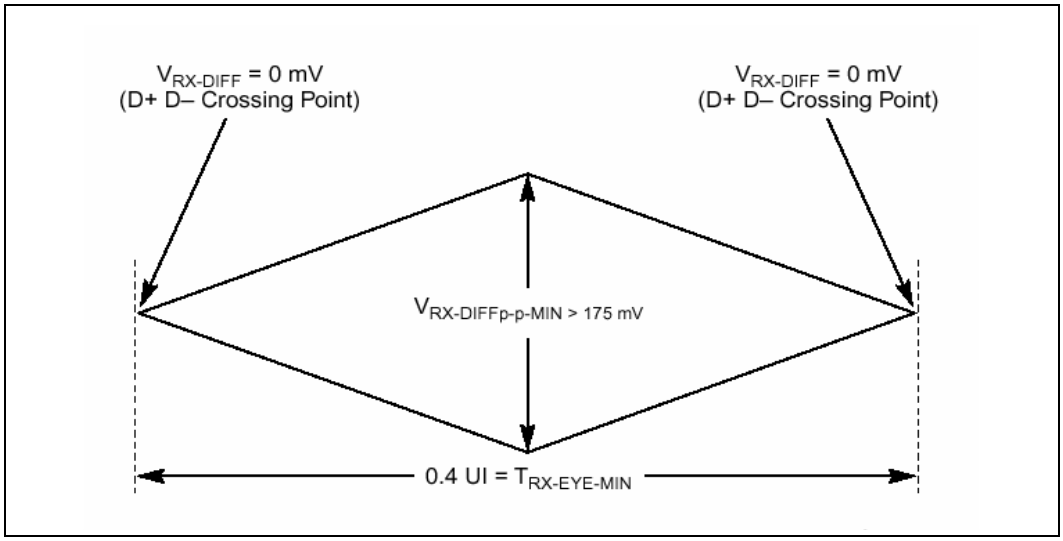


Table 6-10. PCI Express* Differential Receiver (RX) DC Input Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
$V_{RX-DIFFp-p}$	Differential Input Peak to Peak Voltage	0.175		1.200	V	$V_{RX-DIFFp-p} = 2*\|V_{RX-D+} - V_{RX-D-}\|$ See Note 1.
$V_{RX-CM-ACp}$	AC Peak Common Mode Input Voltage			150	mV	$V_{RX-CM-AC}=\|V_{RX-D+} + V_{RX-D-}\|/2 - V_{RX-CM-DC}$ $V_{RX-CM-DC} = DC_{(avg)}$ of $\|V_{RX-D+} + V_{RX-D-}\|/2$ during L0 See Note 1.
$RL_{RX-DIFF}$	Differential Return Loss	15			dB	Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at +300 mV and -300 mV, respectively. See Note 2.
RL_{RX-CM}	Common Mode Return Loss	6			dB	Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at 0 V. See Note 2
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance	80	100	120	W	RX DC Differential Mode impedance. See Note 3.
Z_{RX-DC}	DC Input Impedance	40	50	60	W	Required RX D+ as well as D- DC impedance (50 Ω ±20% tolerance). See Notes 1 and 3.
$Z_{RX-HIGH-IMP-DC}$	Powered Down DC Input Impedance	200 k			W	Required RX D+ as well as D- DC impedance when the receiver terminations do not have power. See Note 4.
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65		175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2*\|V_{RX-D+} - V_{RX-D-}\|$ Measured at the package pins of the Receiver.

Notes:

1. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 6-1 should be used as the RX device when taking measurements (also refer to the Receiver Compliance Eye Diagram as shown in Figure 6-3). If the clocks to the RX and TX are not derived from the same clock chip the TX UI must be used as a reference for the eye diagram.
2. The receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D- line biased to -300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 Ω probes - see Figure 6-1). Note: that the series capacitors C_{TX} is optional for the return loss measurement.
3. Impedance during all LTSSM states. When transition from a Fundamental Reset to Detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured Lanes of a Port.

Table 6-11. DC Specifications for PCI

Symbol	Parameter	PCI		Units	Condition	Notes
		Min	Max			
VCC33	Supply Voltage	3.0	3.6	V		
V_{ih}	Input High Voltage	0.5VCC33	VCC33 +0.5	V		
V_{il}	Input Low Voltage	-0.5	0.3VCC33	V		
V_{ipu}	Input Pull-up Voltage	0.7VCC33		V		1
I_{il}	Input Leakage Current		±10	µA	$0 < V_{in} < VCC33$	2

Table 6-11. DC Specifications for PCI

Symbol	Parameter	PCI		Units	Condition	Notes
		Min	Max			
V_{oh}	Output High Voltage	0.9VCC33		V	I_{out} = -500 µA	
V_{ol}	Output Low Voltage		0.1VCC33	V	I_{out} = 1500 µA	
C_{in}	Input Pin Capacitance		10	pF		3
C_{clk}	PxPCLKI Pin CapacitanceReserved	5Reserved	8Reserved	pFReserved		
C_{IDSEL}	IDSEL Pin Capacitance		8	pF		4
L_{pin}	Pin Inductance		20	nH		5

Table 6-12. DC Specifications for PCI and Mode 1 PCI-X* 3.3 V Signaling

Symbol	Parameter	PCI		PCI-X*		Units	Condition	Notes
		Min	Max	Min	Max			
VCC33	Supply Voltage	3.0	3.6	3.0	3.6	V		
V_{ih}	Input High Voltage	0.5VCC33	VCC33 +0.5	0.5VCC33	VCC33 +0.5	V		
V_{il}	Input Low Voltage	-0.5	0.3VCC33	-0.5	0.35VCC33	V		
V_{ipu}	Input Pull-up Voltage	0.7VCC33		0.7VCC33		V		1
I_{il}	Input Leakage Current		±10		±10	µA	$0 < V_{in} < VCC33$	2
V_{oh}	Output High Voltage	0.9VCC33		0.9VCC33		V	I_{out} = -500 µA	
V_{ol}	Output Low Voltage		0.1VCC33		0.1VCC33	V	I_{out} = 1500 µA	
C_{in}	Input Pin Capacitance		10		10	pF		3
C_{clk}	PxPCLKI Pin Capacitance	5	8	5	8	pF		
C_{IDSEL}	IDSEL Pin Capacitance		8		8	pF		4
L_{pin}	Pin Inductance		20		20	nH		5
I_{Off}	PxPME# input leakage		1		1	µA	$V_o \leq 3.6$ V VCC33 off or floating	6

Notes:
1. This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Applications sensitive to static power utilization must assure that the input buffer is conducting minimum current at this input voltage.
2. Input leakage currents include hi-Z output leakage for all bi-directional buffers with tri-state outputs.
3. Absolute maximum pin capacitance for a PCI/PCI-X* input except PxPCLKI and IDSEL.

4. For conventional PCI only, lower capacitance on this input-only pin allows for non-resistive coupling to PxAD[xx]. PCI-X configuration transactions drive the AD bus four clocks before PxFRAME# asserts (see Section 2.7.2.1 of the *PCI-X Protocol Addendum to the PCI Local Bus Specification, Revision 2.0a*).
5. For conventional PCI, this is a recommendation, not an absolute requirement. For PCI-X, this is a requirement.
6. This input leakage is the maximum allowable leakage into the PxPME# open drain driver when power is removed from VCC33 of the component. This assumes that no event has occurred to cause the device to attempt to assert PxPME#.

Table 6-13 summarizes the DC specifications for 1.5 V signaling.

Table 6-13. PCI Hot Plug Slot Power Requirements

Supply Voltage	Maximum Operating Current[1]	Maximum Adapter Card Decoupling Capacitance	Minimum Supply Voltage Skew Rate	Maximum Supply Voltage Skew Rate
+5 V	5 A	3000 µF	25 V/s	3300 V/s
+3.3 V	7.6 A	3000 µF	16.5 V/s	3300 V/s
+12 V	500 mA	300 µF	60 V/s	33000 V/s
-12 V	100 mA	150 µF	60 V/s	66000 V/s

Combined maximum power drawn by all supply voltages in any one slot must not exceed 25 W.

Table 6-14. General LAN DC Electrical Characteristic for 3.3 V I/O Pads

Symbol	Parameter	Conditions	Min	Max	Units
VOH	Output High Voltage	IOH = 10 mA, VCC=Min	2.40	VCC	V
VOL	Output Low Voltage	IOL = -10 mA, VCC=Min	VSS	0.4	V
VOH_mon	VOL in monitor mode	IOH = 10 mA	2.90	VCC	V
VOL_mon	VOL in monitor mode	IOL = -10 mA	0.57	1.03	V
VIH	Input High Voltage	VIH > VIH_Min; VCC=Min	2	–	V
VIL	Input Low Voltage	VIH > VIL_Max; VCC=Min	-	0.8	V
VHYST	Input Hysteresis	Inside VIH / VIL window	15	180	mV
IIH	Input High Current	VCC = Max; VIN = 3.3 V	-	100	uA
IIL	Input Low Current	VCC = Max; VIN = 0.4 V	-100		uA
IPOLD	Input Pull Down	VIN=PWRP	14.8	29.9	K
IPULU	Input Pull Up	VIN=VSS	15.3	29.7	K
IOFF	Current at IDDQ mode	For 3.3 V supply only	90	168	uA

Figure 6-4. Kumeran Transmitter Test Point (TP-T)

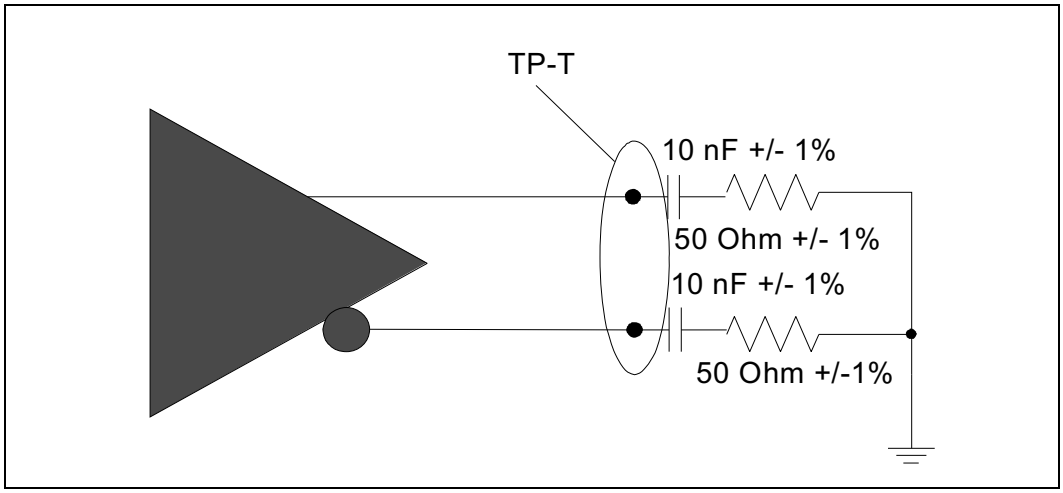


Table 6-15. Kumeran Transmit Specifications at TP-T

Description	Value	Units	Notes
Data rate	1000	Mb/s	Figure 6-4
Nominal signaling speed	1250	MBd(Mega Baud)	Figure 6-4
Clock tolerance	±100	ppm	Figure 6-4
Differential output amplitude (p-p)	750-1350	mV	Figure 6-4
Return loss	10	dB	Figure 6-4
Impedance at connection (TP-T)	100±30	W	Figure 6-4
Impedance at termination (TP-T)	100±10	W	Figure 6-4

Figure 6-5. Kumeran Receive Test Point (TP-R)

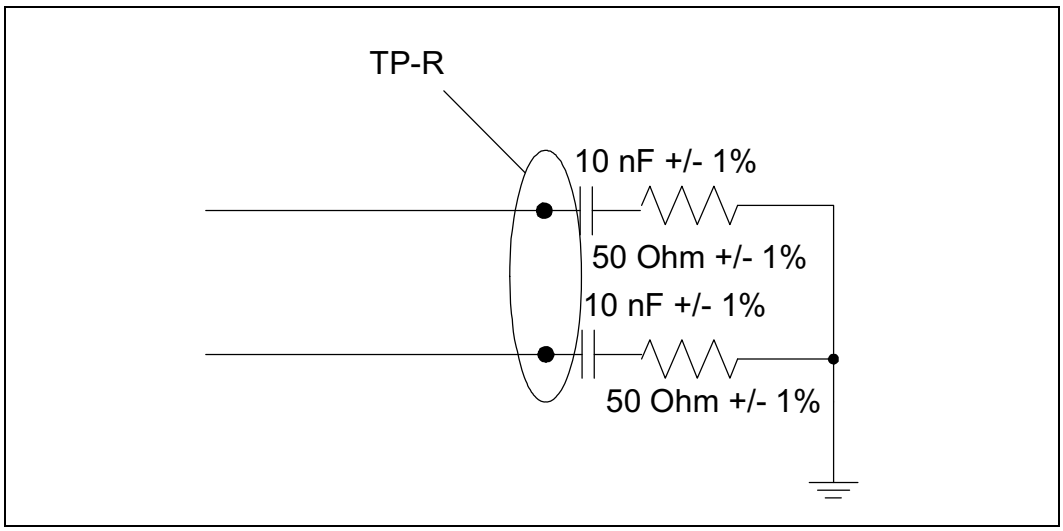


Table 6-16. Kumeran Receiver Specifications at TP-R

Description	Value	Units	Notes
Data rate	1000	Mb/s	Figure 6-5
Nominal signaling speed	1250	MBd(Mega Baud)	Figure 6-5
Clock tolerance	±100	ppm	Figure 6-5
Sensitivity (p-p)	200-1920	mV	Figure 6-5
Differential skew	175	ps	Figure 6-5
Differential return loss	10	dB	Figure 6-5
Common mode return loss	6	dB	Figure 6-5
Input impedance, each signal to ground with a 50 Ω resistor			
TDR (Time Domain Reflector) rise time TP-R	85	ps	Figure 6-5
Impedance at connection TP-R	100±30	W	Figure 6-5

Table 6-17. Kumeran Transmit Electrical Idle Characteristics

Parameter	Description	Min	Max	Units	Notes
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute delta of DC common mode voltage during L0 and electrical idle	0	100	mV	
$V_{TX-IDLE-DIFFp}$	Electrical idle differential peak output voltage	0	20	mV	
$T_{TX-IDLE-MIN}$	Minimum time spent in electrical idle	50		UI (bit times)	
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Electrical Idle after sending an Electrical Idle ordered set		20	UI (bit times)	
$T_{TX-IDLE-TO-TO-DIFF-DATA}$	Maximum time to transition to valid TX specifications after leaving an electrical Idle condition		20	UI (bit times)	

Table 6-18. Kumeran Receive Electrical Idle Characteristics

Parameter	Description	Min	Max	Units	Notes
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical idle detect threshold	65	200	mV	
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected electrical idle enter detect threshold integration time		10	ms	

Table 6-19. LAN and BMC general DC Electrical Characteristics for 3.3V I/O pads

Symbol	Parameter	Conditions	Min	Max	Units
VOH	Output High Voltage	IOH=10mA, VCC=Min	2.40	VCC	V
VOL	Output Low Voltage	IOH=-10mA, VCC=Min	VSS	0.4	V
VOH_mon	VOH in monitor mode	IOH=10mA	2.90	VCC	V
VOL_mon	VOL in monitor mode	IOL=-10mA	0.57	1.03	V
VIH	Input High Voltage	VIH>VIH_Min; VCC=Min	2	-	V
VIL	Input Low Voltage	VIL<VIL_Max; VCC=Min	-	0.8	V
VHYST	Input Hysteresis	Inside VIH/VIL window	15	180	mV
IIH	Input High Current	VCC=Max; VIN=3.3V	-	100	uA

Table 6-19. LAN and BMC general DC Electrical Characteristics for 3.3V I/O pads

Symbol	Parameter	Conditions	Min	Max	Units
IIL	Input Low Current	VCC=Max; VIN=0.4V	-100	-	uA
IPOLD	Input Pull Down	VIN=PWRP	14.8	29.9	KOhm
IPULU	Input Pull Up	VIN=VSS	15.3	29.7	KOhm
IOFF	Current at IDDQ mode	For 3.3V supply only	90	168	uA

§

7 Component Ballout

7.1 Intel® 631xESB/632xESB I/O Controller Hub Ballout

Note: All the Intel® 631xESB/632xESB I/O Controller Hub Ballouts in following tables are the superset of Intel® 631xESB/632xESB I/O Controller Hub SKU Definition (Section 1.3).

Table 7-1. Intel® 631xESB/632xESB I/O Controller Hub Ballout (Left Third) (Sheet 1 of 2)

	36	35	34	33	32	31	30	29	28	27	26	25	
AT			VSS	SDP2_7	VSS	RS232_CTS	RS232_SOUT	VCCAUX3_3	EBUS_FRST#	EBUS_ADV#/ EBUS_RAS#	VSS	EBUS_BE_0#	AT
AR		VSS	SDP2_6	VCCAUX3_3	RS232_DSR	RS232_DTR	VSS	RS232_RI	Reserved	VSS	EBUS_ALAT/ EBUS_CKE	EBUS_WE#	AR
AP	VSS	SDP2_5	VSS	SDP2_4	SDP1_2	VCCAUX3_3	RS232_DCD	RS232_RTS	VSS	EBUS_OE#/ EBUS_CAS#	EBUS_CLK_2	VSS	AP
AN	LAN_PWR_GOOD	VCCAUX3_3	SDP2_3	SDP2_2	VSS	SDP2_1	RS232_SIN	VSS	EBUS_AD[12]	EBUS_AD[10]	VSS	EBUS_AD[5]	AN
AM	VSS	FLBSINTEX1	PERST#	VCCAUX3_3	SDP2_0	SDP1_1	VCCAUX3_3	LAN1_DIS#	EBUS_AD[11]	VSS	EBUS_AD[7]	EBUS_AD[6]	AM
AL	FLBSINTEX0	FLBSD0	VSS	PE_WAKE#	SDP1_0	VSS	SDP0_2	LAN0_DIS#	VSS	EBUS_AD[9]	EBUS_AD[8]	VSS	AL
AK	FLBSD1	VSS	SMBD4	SMBALRT_4	VCCAUX3_3	SDP0_0	SDP0_1	VCCAUX3_3	EBUS_AD[24]	EBUS_AD[22]	VSS	EBUS_AD[19]	AK
AJ	VSS	FLSH_CE#	SMBCLK4	VSS	SMBALRT_3	SDRAM_BA0/ SDP3_2/ LED0_2	VSS	SDRAM_BA1/ SDP3_3/ LED0_3	EBUS_AD[23]	VCCAUX3_3	EBUS_AD[21]	EBUS_AD[20]	AJ
AH	FLSH_SI	FLSH_SCK	VSS	SMBD3	SMBCLK3	VCCAUX3_3	SDRAM_A10/ SDP3_6/ LED1_2	SDRAM_AD12/ SPD3_1/ LED0_1	VSS	SDRAM_A9/ SDP3_5/ LED1_1	SDRAM_A11/ SDP3_7/ LED1_3	VCCAUX3_3	AH
AG	FLSH_SO	VSS	SMBD1	SMBCLK1	VSS	SMBALRT_2	PXPWROK	VCCAUX3_3	TCK	TRST#	VSS	SDP3_0/ LED0_0	AG
AF	VSS	EE_DI	VSS	VSS	SMBD2	SMBCLK2	VSS	TDO	TDI	VCCAUX3_3	TMS	VCCAUX3_3	AF
AE	EE_SK	EE_DO	VSS	SMBCLK0	SMBD0	VSS	STRAP_1	RESERVED	VSS	RESERVED	STRAP_0	VSS	AE
AD	EE_CS#	VSS2	NC	RESERVED	VSS	ESB2_TEST2	RESERVED	VSS2	STRAP_2	RESERVED	VSS	NC	AD
AC	VSS	LINK_1	VSS	VSS2	VSS	VSS	VSS	RESERVED	VSS	VSS	VSS	VSS	AC
AB	Reserved	LINK_0	VSS	VSS	VSS	VSS2	VSS	VSS	VSS	VSS	VSS	VSS2	AB
AA	Reserved	VSS2	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS2	AA
Y	VSS	SETP1	SETN1	VCCSE	VSS	VSS	VCCSE	VSS	VSS	VCCSE	VSS	VCCSE	Y
W	SERP1	SERN1	VSS	SEICOMPI	SERCOMPO	VSS	SETN0	SETP0	VSS	VSS	VCCSE	VSS	W
V	SER_CLK_IN	VSS	VSSAPLL1_5	VCCAPLL1_5	VSS	VSSA3_3	VCCA3_3	VSS	SERN0	SERP0	VSS	NC	V
U	VSS	AD[18]	ACZ_RST#	VSS	ACZ_SDIN[2]	ACZ_SDIN[1]	VSS	VCC5REF1	ESB2_TEST0	VSS	ESB2_TEST1	NC	U
T	AD[0]	AD[1]	VSS	ACZ_SYNC	ACZ_BIT_CLK	VSS	AD[16]	FRAME#	VSS	VCCP25PCI	VCCPPCI	VSS	T
R	AD[2]	VSS	AD[21]	ACZ_SDIN[0]	VSS	ACZ_SDOUT	AD[17]	VCCPPCI	NC	VCCPPCI	VSS	VCCPPCI	R
P	VCCPPCI	GNT[3]#	GNT[4]#/ GPIO[48]	VCCPPCI	PLTRST#	PME#	VSS	GNT[1]#	TRDY#	VCCPPCI	VCCPPCI	VCCPPCI	P
N	AD[8]	AD[9]	VSS	AD[3]	AD[4]	VCCPPCI	CBE[2]#	IRDY#	VSS	VCCSUS2	VCCPPCI	VSS	N
M	AD[11]	VCCPPCI	AD[6]	AD[5]	VSS	AD[19]	AD[20]	VCCPPCI	PCICLK	VCCSUS1	VSS	VCCPSUS	M
L	VSS	CBE[1]#	AD[10]	VCCPPCI	AD[23]	AD[22]	VSS	AD[7]	REQ[2]#	VSS	VCCPSUS	VCCPSUS	L
K	AD[15]	PAR	VSS	AD[12]	AD[13]	VCCPPCI	REQ[4]#/ GPI[40]	CBE[0]#	VCCPSUS	STRAP_4	VCCPSUS	VCCPSUS	K
J	SERR#	VSS	AD[14]	CBE[3]#	VSS	AD[26]	AD[25]	VSS	GPIO[28]	RI#	VSS	SATARBIAS	J
H	VSS	PLOCK#	AD[24]	VSS	AD[28]	REQ[0]#	VCCPSUS	SMBDATA	SUS_STAT#/ LPCPD#	VSS	VCCSATA	SATARBIAS#	H
G	PERR#	STOP#	VSS	AD[27]	AD[31]	VSS	SMBCLK	SLP_S5#	VSS	GPI[8]	VCCAPLL	VSS	G
F	DEVSEL#	NC	AD[29]	AD[30]	VCCPSUS	PIRQ[G]#/ GPI[4]	SMLINK1	VSS	PWRBTN#	GPIO[25]	VSS	SUSCLK	F
E	VSS	REQ[3]#	REQ[1]#	VSS	PIRQ[H]#/ GPI[5]	PIRQ[F]#/ GPI[3]	VSS	SLP_S4#	RESERVED	VSS	SMBALERT#/ GPI[11]	WAKE#	E
D	GNT[6]#/ GPO[16]	REQ[5]#/ GPI[1]	VCCPSUS	GNT[0]#	PIRQ[E]#/ GPI[2]	VSS	SMLINK0	SLP_S3#	VSS	ESIDCAC	GPIO[24]	VSS	D

Note: All the Intel® 631xESB/632xESB I/O Controller Hub Ballouts in following tables are the superset of Intel® 631xESB/632xESB I/O Controller Hub SKU Definition (Section 1.3).

Table 7-1. Intel® 631xESB/632xESB I/O Controller Hub Ballout (Left Third) (Sheet 2 of 2)

C	VSS	VSS	PCIRST#	SPKR	VSS	PIRQ[A]#	PIRQ[D]#	VSS	INTRUDER#	VCCPRTC	VSS	INTVRMEN	C
B		VSS	CLK14	VSS	THRMTRIP#	GNT[2]#	VSS	PIRQ[C]#	GPIO[27]	VSS	RTCX1	PWROK	B
A			VSS	REQ[6]# / GPI[0]	GNT[5]# / GPO[17]	VSS	PIRQ[B]#	RTCRST#	VSS	RTCX2	RSMRST#	VSS	A
	36	35	34	33	32	31	30	29	28	27	26	25	

Table 7-2. Intel® 631xESB/632xESB I/O Controller Hub Ballout (Middle Third) (Sheet 1 of 2)

	24	23	22	21	20	19	18	17	16	15	14	13	
AT	EBUS_BE_1#	VSS	HPX_SOL/ HXBUTTON2#	HPX_SIC/ HXPWRLED2#	VSS	HPX_SOC/ HXPCIXCAP2_2	HPX_SLOT[3]/ HXPWRLED1#	VCC33	HPX_SID/ HXPCIXCAP1_2	PXIRQ[8]# / HXBUTTON_1#	VCC33	PXIRQ[10]# / HXPCIXCAP1_1	AT
AR	VSS	HPX_SLOT[2]	HPX_SLOT[1]/ HXPRSNT1_1#	VSS	HPX_SLOT[0]/ HXMRL_2#	HPX_SIL# / HXCLKEN_1#	VSS	PXIRQ[4]#	PXIRQ[7]#	VSS	PXIRQ[11]# / HXM66EN_1	PXIRQ[12]# / HXM66EN_2	AR
AP	EBUS_CE_1#	EBUS_CE_2#	VSS	HPX_RST2#	HPX_SOLR/ HXATNLED2#	VSS	HPX_PRST# / HXRST1#	HPX_SOD/ HXCLKEN_2#	VCC33	PXIRQ[6]#	PXIRQ[9]# / HXPCIXCAP2_1	VCC33	AP
AN	EBUS_AD[4]	VSS	EBUS_AD[1]	SMBUS[2]	VSS	VSS	RESERVED	VSS	PXAD[14]	PXIRQ[5]#	VSS	PXAD[9]	AN
AM	VSS	EBUS_AD[2]	EBUS_AD[0]	VSS	NPECFG	SPECFG	VSS	NC	PXCBE[1]#	VCC33	PXAD[11]	PXCBE[0]#	AM
AL	EBUS_AD[3]	EBUS_AD[15]	VSS	SMBUS[5]	PASTRAP0	VSS	PXPCIXCAP	NC	VSS	PXAD[13]	PXAD[10]	VSS	AL
AK	EBUS_AD[18]	VSS	EBUS_AD[13]	STRAP_3	VSS	SMBUS[1]	HPDTA	VCC33	PXAD[15]	PXAD[12]	VSS	PXAD[27]	AK
AJ	VSS	EBUS_AD[16]	EBUS_AD[14]	VSS	SCLK	RSTIN#	VSS	HPCLK	PXPAR	VSS	PXAD[31]	PXAD[28]	AJ
AH	SDP3_4/ LED1_0	EBUS_AD[17]	VSS	SMBUS[3]	SDTA	VSS	RESERVED	RESERVED	VSS	PXGNT[2]#	PXAD[30]	VCC33	AH
AG	VCCAUX3_3	VSS	EXTINTR#	RESERVED	VSS	RESERVED	RESERVED	VCC33	PXGNT[4]# / HXBUSEN_2#	PXGNT[3]# / HXPWREN_2	VSS	PXAD[29]	AG
AF	VSS	NC	NC	STRAP_6	STRAP_5	RESERVED	NC	VCC33	PXREQ[5]# / HXPRSNT1_2#	VSS	NC	VSS	AF
AE	VCCAUX3_3	NC	VSS	VSS	VSS	VSS	VCC33	VCC33	VSS	VCC33	VSS	NC	AE
AD	VSS	VCCAUX1_5	VSS	VCCAUX1_5	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	AD
AC	VSS	VSS	VCCAUX1_5	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	AC
AB	VSS2	VCCAUX1_5	VSS	VCCAUX1_5	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	AB
AA	VSS	VSS	VCCAUX1_5	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	AA
Y	VCCSE	VCCAUX1_5	VSS	VCCAUX1_5	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	Y
W	VCCSE	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	W
V	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	V
U	VSS	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	U
T	VCCPPCI	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	T
R	VSS	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	R
P	NC	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	P
N	VCCPPCI	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	N
M	NC	NC	VSS	NC	VSS	VSS	VCCATX	VSS	VCCARX	NC	VSS	VCCPIDE	M
L	VSS	VSS	NC	VSS	SATA5TXN	SATA5TXP	VCCATX	SATA2TXN	SATA2TXP	VSS	VCCPIDE	VCCPIDE	L
K	SYS_RESET#	SATALED#	VRMPWRGD	SATA4RXP	SATA4RXN	VSS	SATA2RXP	SATA2RXN	VCCARX	SATA0RXP	SATA0RXN	VCCPIDE	K
J	SERIRQ	VSS	SATA4TXN	SATA4TXP	VSS	VSSASATABG	VCCASATABG	VSS	SATA1TXN	SATA1TXP	VSS	USBRBIAS#	J
H	VSS	SATA5RXP	SATA5RXN	VSS	SATA3TXN	SATA3TXP	VCCATX	SATA1RXP	SATA1RXN	VCCPIDE	SATA0TXN	SATA0TXP	H
G	SATACLKP	SATACLKN	VSS	SATA3RXP	SATA3RXN	VCCATX	SATA4GP/ GPI[12]	GPI[6]	VSS	DD[14]	DD[13]	VSS	G
F	THRM#	VSS	CPUPWRGD/ GPO[49]	LDRQ[1]# / GPI[41]	VCCATX	STRAP_7	SATA1GP/ GPI[29]	VCCATX	SDATAOUT1/ GPIO[32]	VCCARX	VSS	DD[11]	F
E	VSS	INIT3_3V#	A20GATE	VSS	LDRQ[0]#	SATA3GP/ GPI[31]	VSS	GPI[7]	GPIO[33]	VSS	DD[12]	DD[10]	E
D	VCCPCPU	INIT#	VSS	CPUSLP#	FWH[4]/ LFRAME#	VSS	SATA0GP/ GPI[26]	GPIO[34]	VCCARX	NC	VCC5REF2	VSS	D

Table 7-2. Intel® 631xESB/632xESB I/O Controller Hub Ballout (Middle Third) (Sheet 2 of 2)

C	RCIN#	VCCPCPU	STPCLK#	INTR	VSS	FWH[3]/ LAD[3]	SATA2GP/ GPI[30]	VSS	SLOAD/ GPO[21]	SDATAOUT0/ GPO[23]	VCCPIDE	DD[8]	C
B	VCCPCPU	SMI#	NMI	VSS	FWH[1]/ LAD[1]	FWH[2]/ LAD[2]	VCCARX	GPO[18]	SCLK/GPO[20]	VSS	DIOW# / DSTOP	DIOR# / DWSTB / RDMARDY#	B
A	FERR#	IGNNE#	VSS	A20M#	FWH[0]/ LAD[0]	VSS	SATA5GP/ GPI[13]	GPO[19]	VCCARX	DD[15]	DDREQ	VCCPIDE	A
	24	23	22	21	20	19	18	17	16	15	14	13	

Table 7-3. Intel® 631xESB/632xESB I/O Controller Hub Ballout (Right Third) (Sheet 1 of 2)

	12	11	10	9	8	7	6	5	4	3	2	1	
AT	PXIRQ[14]#/ HXPWRFLT_1#	VCC33	PXIRQ[0]#	PXPCLKO[0]	VSS	PXPCLKO[1]	PXPCLKO[6]	VSS	PXPCLKO[2]	VSS			AT
AR	VSS	PXIRQ[1]#	PXIRQ[2]#	VSS	PXPCLKO[4]	PXPCLKO[5]	VSS	PXPCLKO[3]	PXPCLKI	VSS	VSS		AR
AP	PXIRQ[13]#/ HXPWRFLT_2#	PXIRQ[15]#/ HXMRL1#	VCC33	PXIRQ[3]#	PXAD[0]	VSS	PXPME#	PXPCIRST#	VSS	PXGNT[5]#/ HXBUSEN_1#	PXREQ[1]#	VSS	AP
AN	PXAD[8]	VSS	PXAD[4]	PXAD[2]	VSS	HPX_PWREN_1	PXREQ[3]#/ HXPRSNT2_1#	VSS	PXGNT[0]#	PXREQ[0]#	VSS	PXREQ[4]#/ HXPRSNT2_2#	AN
AM	VCC33	PXAD[6]	PXAD[3]	VCC33	PXACK64#	PXCBE[7]#	VSS	PXCBE[6]#	PXGNT[1]#	PXFRAME#	PXIRDY#	PXTRDY#	AM
AL	PXAD[7]	PXAD[5]	VSS	PXAD[1]	PXREQ64#	VSS	PXCBE[4]#	PXREQ[2]#	VSS	PXAD[49]	PXAD[48]	VSS	AL
AK	PXAD[25]	VCC33	PX133EN	RESERVED	VSS	PXCBE[5]#	PXPAR64	VSS	PXAD[46]	PXAD[47]	VSS	PXDEVSEL#	AK
AJ	VSS	PXAD[24]	PXAD[22]	VSS	PXAD[18]	PXAD[63]	VSS	PXAD[62]	PXAD[45]	VSS	PXAD[44]	PXSTOP#	AJ
AH	PXAD[26]	PXCBE[3]#	VSS	PXAD[20]	PXAD[17]	VSS	PXAD[61]	PXAD[60]	VSS	PXAD[43]	PXAD[41]	PXPLOCK#	AH
AG	VCC15	VSS	PXAD[21]	PXAD[16]	VSS	PXAD[59]	PXAD[57]	VSS	PXAD[42]	PXAD[40]	VSS	PXPERR#	AG
AF	VSS	PXAD[23]	PXAD[19]	VSS	PXCBE[2]#	PXAD[58]	VSS	PXAD[56]	PXAD[38]	VSS	PXAD[39]	PXAD[36]	AF
AE	VCC15	VCCAP1	VSS	HXATNLED_1#	PXAD[53]	VSS	PXAD[55]	PXAD[54]	VSS	PXAD[37]	PXAD[35]	VSS	AE
AD	VCC15	VCC15	VCCAP3	PXAD[52]	VSS	PXAD[50]	PXAD[51]	VSS	PXAD[34]	PXAD[33]	VSS	PXAD[32]	AD
AC	VCC15	VREFPCIPAD	RCOMP	VSS	PE2RN2	PE2RP2	VCC15	PE2TN1	PE2TP1	VSS	PXSERR#	PXM66EN	AC
AB	VCC15	VCC15	VCC15	PE2TN3	PE2TP3	VCC15	PE2RN1	PE2RP1	VSS	PE2TN0	PE2TP0	VSS	AB
AA	VCCPE	VSS	PE2RN3	PE2RP3	VSS	PE2TN2	PE2TP2	VSS	PE2RN0	PE2RP0	VSS	VSSBGPE	AA
Y	VCCPE	PE1RN3	PE1RP3	VCCPE	PE1RP0	PE1RN0	VSS	PE1TP2	PE1TN2	VCCPE	PE1TN3	PE1TP3	Y
W	VCCPE	PERCOMPO	VSS	PE1TP0	PE1TN0	VCCPE	PE1RP1	PE1RN1	VSS	PE1RN2	PE1RP2	VSS	W
V	VSS	VCCPE	PECLKN	PECLKP	VSS	VCCAPE	VSSAPE	VCCPE	PE1TP1	PE1TN1	VSS	VCCBGPE	V
U	VCCPE	PE4RP0	PE4RN0	VSS	PE4TP1	PE4TN1	VSS	PE4TP2	PE4TN2	VCCPE	PE4RP3	PE4RN3	U
T	VCCPE	PEICOMPI	VSS	PE4RP1	PE4RN1	VCCPE	PE4RP2	PE4RN2	VSS	PE4TP3	PE4TN3	VSS	T
R	VSS	VSS	PE4TP0	PE4TN0	VSS	PE4TN6	PE4TP6	VCCPE	PE4RN4	PE4RP4	VCCPE	NC	R
P	VCCPE	NC	NC	VCCPE	PE4RN7	PE4RP7	VSS	PE4TN5	PE4TP5	VSS	PE4TN4	PE4TP4	P
N	VCCPE	VCCP25IDE	VSS	PE4TN7	PE4TP7	VCCPE	PE4RN6	PE4RP6	VCCPE	PE4RN5	PE4RP5	VSS	N
M	NC	VCCPE	NC	VCCAESI	VSS	PE0TN0	PE0TP0	VSS	PE0RN3	PE0RP3	VCCPE	ESICLK100P	M
L	VSS	VCCBGESI	VSSBGESI	VSS	PE0RN0	PE0RP0	VSS	PE0TN3	PE0TP3	VSS	ESIICOMPI	ESICLK100N	L
K	VCCAUBG	VSSAUBG	VSS	VCCUSBCORE	VCCUSBCORE	VSS	PE0RN2	PE0RP2	VSS	PE0TP2	PE0TN2	VSS	K
J	USBRBIAS	VSS	ESIRXN[3]	ESIRXP[3]	VCCUSBCORE	ESITXN[2]	ESITXP[2]	VSS	PE0RP1	PE0RN1	VSS	ESIRCOMPO	J
H	VSS	CLK48	VCCUSB	VSS	ESIRXN[2]	ESIRXP[2]	VSS	ESITXN[1]	ESITXP[1]	VSS	PE0TP1	PE0TN1	H
G	DD[5]	DD[3]	VSS	ESITXN[3]	ESITXP[3]	VCCPUSB	ESIRXN[1]	ESIRXP[1]	VCCUSBCORE	ESITXN[0]	ESITXP[0]	VSS	G
F	DD[4]	VSS	DD[1]	VCCAUPLL	VSS	OC[7] #/ GPI[15]	OC[6]#/ GPI[14]	VSS	ESIRXN[0]	ESIRXP[0]	VSS	OC[5]#/ GPI[10]	F
E	VCCPIDE	DD[2]	DD[0]	VSS	USBP2P	USBP2N	VCCPUSB	VCC5REFSUS	OC[4]#/ GPI[9]	VSS	OC[2]#	OC[3]#	E
D	DD[9]	DD[6]	VSS	USBP1P	USBP1N	VSS	OC[1]#	OC[0]#	VSS	USBP7P	USBP7N	VCCUSBCORE	D
C	DD[7]	VSS	USBP0P	USBP0N	VSS	USBP3P	USBP3N	VCCPUSB	USBP6P	USBP6N	VSS	VSS	C
B	VSS	IDEIRQ	DA[1]	VSS	DCS1#	DCS3#	VSS	USBP5P	USBP5N	VCCPUSB	VSS		B

Table 7-3. Intel® 631xESB/632xESB I/O Controller Hub Ballout (Right Third) (Sheet 2 of 2)

A	IORDY / DRSTB / WDMARDY#	DDACK#	VSS	DA[0]	DA[2]	VSS	USBP4P	USBP4N	VCCPUSB	VSS			A
	12	11	10	9	8	7	6	5	4	3	2	1	

§

8 Signal Lists

8.1 Intel® 631xESB/632xESB I/O Controller Hub Signal List (Sorted by Signal Name)

Note: All the Pinlists in following tables are the superset of Intel® 631xESB/632xESB I/O Controller Hub SKU Definition (Section 1.3).

Pin Name	Pin Number
A20GATE	E22
A20M#	A21
ACZ_BIT_CLK	T32
ACZ_RST#	U34
ACZ_SDIN[0]	R33
ACZ_SDIN[1]	U31
ACZ_SDIN[2]	U32
ACZ_SDOUT	R31
ACZ_SYNC	T33
AD[0]	T36
AD[1]	T35
AD[10]	L34
AD[11]	M36
AD[12]	K33
AD[13]	K32
AD[14]	J34
AD[15]	K36
AD[16]	T30
AD[17]	R30
AD[18]	U35
AD[19]	M31
AD[2]	R36
AD[20]	M30
AD[21]	R34
AD[22]	L31
AD[23]	L32
AD[24]	H34
AD[25]	J30
AD[26]	J31
AD[27]	G33
AD[28]	H32
AD[29]	F34
AD[3]	N33

Pin Name	Pin Number
AD[30]	F33
AD[31]	G32
AD[4]	N32
AD[5]	M33
AD[6]	M34
AD[7]	L29
AD[8]	N36
AD[9]	N35
CBE[0]#	K29
CBE[1]#	L35
CBE[2]#	N30
CBE[3]#	J33
CLK14	B34
CLK48	H11
CPUPWRGD/GPO[49]	F22
CPUSLP#	D21
DA[0]	A9
DA[1]	B10
DA[2]	A8
DCS1#	B8
DCS3#	B7
DD[0]	E10
DD[1]	F10
DD[10]	E13
DD[11]	F13
DD[12]	E14
DD[13]	G14
DD[14]	G15
DD[15]	A15
DD[2]	E11
DD[3]	G11
DD[4]	F12
DD[5]	G12

Pin Name	Pin Number
DD[6]	D11
DD[7]	C12
DD[8]	C13
DD[9]	D12
DDACK#	A11
DDREQ	A14
DEVSEL#	F36
DIOR# / DWSTB / RDMARDY#	B13
DIOW# / DSTOP	B14
EBUS_AD[0]	AM22
EBUS_AD[1]	AN22
EBUS_AD[10]	AN27
EBUS_AD[11]	AM28
EBUS_AD[12]	AN28
EBUS_AD[13]	AK22
EBUS_AD[14]	AJ22
EBUS_AD[15]	AL23
EBUS_AD[16]	AJ23
EBUS_AD[17]	AH23
EBUS_AD[18]	AK24
EBUS_AD[19]	AK25
EBUS_AD[2]	AM23
EBUS_AD[20]	AJ25
EBUS_AD[21]	AJ26
EBUS_AD[22]	AK27
EBUS_AD[23]	AJ28
EBUS_AD[24]	AK28
EBUS_AD[3]	AL24
EBUS_AD[4]	AN24
EBUS_AD[5]	AN25
EBUS_AD[6]	AM25
EBUS_AD[7]	AM26
EBUS_AD[8]	AL26
EBUS_AD[9]	AL27
EBUS_ADV#/EBUS_RAS#	AT27
EBUS_ALAT/EBUS_CKE	AR26
EBUS_BE_0#	AT25
EBUS_BE_1#	AT24
EBUS_CE_1#	AP24
EBUS_CE_2#	AP23
Reserved	AR28
EBUS_CLK_2	AP26

Pin Name	Pin Number
EBUS_FRST#	AT28
EBUS_OE#/EBUS_CAS#	AP27
EBUS_WE#	AR25
EE_CS#	AD36
EE_DI	AF35
EE_DO	AE35
EE_SK	AE36
Reserved	AE27
ESB2_TEST0	U28
ESB2_TEST1	U26
ESB2_TEST2	AD31
ESICLK100N	L1
ESICLK100P	M1
ESIDCAC	D27
ESIICOMPI	L2
ESIRCOMPO	J1
ESIRXN[0]	F4
ESIRXN[1]	G6
ESIRXN[2]	H8
ESIRXN[3]	J10
ESIRXP[0]	F3
ESIRXP[1]	G5
ESIRXP[2]	H7
ESIRXP[3]	J9
ESITXN[0]	G3
ESITXN[1]	H5
ESITXN[2]	J7
ESITXN[3]	G9
ESITXP[0]	G2
ESITXP[1]	H4
ESITXP[2]	J6
ESITXP[3]	G8
EXTINTR#	AG22
FERR#	A24
FLBSD0	AL35
FLBSD1	AK36
FLBSINTEX0	AL36
FLBSINTEX1	AM35
FLSH_CE#	AJ35
FLSH_SCK	AH35
FLSH_SI	AH36
FLSH_SO	AG36
FRAME#	T29

Pin Name	Pin Number
FWH[0]/LAD[0]	A20
FWH[1]/LAD[1]	B20
FWH[2]/LAD[2]	B19
FWH[3]/LAD[3]	C19
FWH[4]/LFRAME#	D20
GNT[0]#	D33
GNT[1]#	P29
GNT[2]#	B31
GNT[3]#	P35
GNT[4]#/GPIO[48]	P34
GNT[5]#/GPO[17]	A32
GNT[6]#/GPO[16]	D36
GPI[6]	G17
GPI[7]	E17
GPI[8]	G27
GPIO[24]	D26
GPIO[25]	F27
GPIO[27]	B28
GPIO[28]	J28
GPIO[33]	E16
GPIO[34]	D17
GPO[18]	B17
GPO[19]	A17
HPCLK	AJ17
HPDTA	AK18
HPX_PRST#/*HXRST1#*	AP18
HPX_PWREN_1	AN7
HPX_RST2#	AP21
HPX_SIC/*HXPWRLED2#*	AT21
HPX_SID/*HXPCIXCAP1_2*	AT16
HPX_SIL#/*HXCLKEN_1#*	AR19
HPX_SLOT[0]/*HXMRL_2#*	AR20
HPX_SLOT[1]/ *HXPRSNT1_1#*	AR22
HPX_SLOT[2]	AR23
HPX_SLOT[3]/*HXPWRLED1#*	AT18
HPX_SOC/*HXPCIXCAP2_2*	AT19
HPX_SOD/*HXCLKEN_2#*	AP17
HPX_SOL/*HXBUTTON2#*	AT22
HPX_SOLR/*HXATNLED2#*	AP20
HXATNLED_1#	AE9
IDEIRQ	B11
IGNNE#	A23

Pin Name	Pin Number
INIT#	D23
INIT3_3V#	E23
INTR	C21
INTRUDER#	C28
INTVRMEN	C25
IORDY / DRSTB / WDMARDY#	A12
IRDY#	N29
LAN_PWR_GOOD	AN36
LAN0_DIS#	AL29
LAN1_DIS#	AM29
LDRQ[0]#	E20
LDRQ[1]#/GPI[41]	F21
LINK_0	AB35
LINK_1	AC35
NC	AD25
NC	AD34
NC	AE13
NC	AE23
NC	AF14
NC	AF18
NC	AF22
NC	AF23
NC	AL17
NC	AM17
NC	D15
NC	F35
NC	L22
NC	M10
NC	M12
NC	M15
NC	M21
NC	M23
NC	M24
NC	P10
NC	P11
NC	P24
NC	R1
NC	R28
NC	U25
NC	V25
NMI	B22
NPECFG	AM20

Pin Name	Pin Number
OC[0]#	D5
OC[1]#	D6
OC[2]#	E2
OC[3]#	E1
OC[4]#/GPI[9]	E4
OC[5]#/GPI[10]	F1
OC[6]#/GPI[14]	F6
OC[7]#/GPI[15]	F7
PAR	K35
PASTRAP0	AL20
PCICLK	M28
PCIRST#	C34
PE_WAKE#	AL33
PE0RN0	L8
PE0RN1	J3
PE0RN2	K6
PE0RN3	M4
PE0RP0	L7
PE0RP1	J4
PE0RP2	K5
PE0RP3	M3
PE0TN0	M7
PE0TN1	H1
PE0TN2	K2
PE0TN3	L5
PE0TP0	M6
PE0TP1	H2
PE0TP2	K3
PE0TP3	L4
PE1RN0	Y7
PE1RN1	W5
PE1RN2	W3
PE1RN3	Y11
PE1RP0	Y8
PE1RP1	W6
PE1RP2	W2
PE1RP3	Y10
PE1TN0	W8
PE1TN1	V3
PE1TN2	Y4
PE1TN3	Y2
PE1TP0	W9
PE1TP1	V4

Pin Name	Pin Number
PE1TP2	Y5
PE1TP3	Y1
PE2RN0	AA4
PE2RN1	AB6
PE2RN2	AC8
PE2RN3	AA10
PE2RP0	AA3
PE2RP1	AB5
PE2RP2	AC7
PE2RP3	AA9
PE2TN0	AB3
PE2TN1	AC5
PE2TN2	AA7
PE2TN3	AB9
PE2TP0	AB2
PE2TP1	AC4
PE2TP2	AA6
PE2TP3	AB8
PE4RN0	U10
PE4RN1	T8
PE4RN2	T5
PE4RN3	U1
PE4RN4	R4
PE4RN5	N3
PE4RN6	N6
PE4RN7	P8
PE4RP0	U11
PE4RP1	T9
PE4RP2	T6
PE4RP3	U2
PE4RP4	R3
PE4RP5	N2
PE4RP6	N5
PE4RP7	P7
PE4TN0	R9
PE4TN1	U7
PE4TN2	U4
PE4TN3	T2
PE4TN4	P2
PE4TN5	P5
PE4TN6	R7
PE4TN7	N9
PE4TP0	R10

Pin Name	Pin Number
PE4TP1	U8
PE4TP2	U5
PE4TP3	T3
PE4TP4	P1
PE4TP5	P4
PE4TP6	R6
PE4TP7	N8
PECLKN	V10
PECLKP	V9
PEICOMPI	T11
PERCOMPO	W11
PERR#	G36
PERST#	AM34
Reserved	AA36
Reserved	AB36
PIRQ[A]#	C31
PIRQ[B]#	A30
PIRQ[C]#	B29
PIRQ[D]#	C30
PIRQ[E]#/GPI[2]	D32
PIRQ[F]#/GPI[3]	E31
PIRQ[G]#/GPI[4]	F31
PIRQ[H]#/GPI[5]	E32
PLOCK#	H35
PLTRST#	P32
PME#	P31
PWRBTN#	F28
PWROK	B25
PX133EN	AK10
PXACK64#	AM8
PXAD[0]	AP8
PXAD[1]	AL9
PXAD[10]	AL14
PXAD[11]	AM14
PXAD[12]	AK15
PXAD[13]	AL15
PXAD[14]	AN16
PXAD[15]	AK16
PXAD[16]	AG9
PXAD[17]	AH8
PXAD[18]	AJ8
PXAD[19]	AF10
PXAD[2]	AN9

Pin Name	Pin Number
PXAD[20]	AH9
PXAD[21]	AG10
PXAD[22]	AJ10
PXAD[23]	AF11
PXAD[24]	AJ11
PXAD[25]	AK12
PXAD[26]	AH12
PXAD[27]	AK13
PXAD[28]	AJ13
PXAD[29]	AG13
PXAD[3]	AM10
PXAD[30]	AH14
PXAD[31]	AJ14
PXAD[32]	AD1
PXAD[33]	AD3
PXAD[34]	AD4
PXAD[35]	AE2
PXAD[36]	AF1
PXAD[37]	AE3
PXAD[38]	AF4
PXAD[39]	AF2
PXAD[4]	AN10
PXAD[40]	AG3
PXAD[41]	AH2
PXAD[42]	AG4
PXAD[43]	AH3
PXAD[44]	AJ2
PXAD[45]	AJ4
PXAD[46]	AK4
PXAD[47]	AK3
PXAD[48]	AL2
PXAD[49]	AL3
PXAD[5]	AL11
PXAD[50]	AD7
PXAD[51]	AD6
PXAD[52]	AD9
PXAD[53]	AE8
PXAD[54]	AE5
PXAD[55]	AE6
PXAD[56]	AF5
PXAD[57]	AG6
PXAD[58]	AF7
PXAD[59]	AG7

Pin Name	Pin Number
PXAD[6]	AM11
PXAD[60]	AH5
PXAD[61]	AH6
PXAD[62]	AJ5
PXAD[63]	AJ7
PXAD[7]	AL12
PXAD[8]	AN12
PXAD[9]	AN13
PXCBE[0]#	AM13
PXCBE[1]#	AM16
PXCBE[2]#	AF8
PXCBE[3]#	AH11
PXCBE[4]#	AL6
PXCBE[5]#	AK7
PXCBE[6]#	AM5
PXCBE[7]#	AM7
PXDEVSEL#	AK1
PXFRAME#	AM3
PXGNT[0]#	AN4
PXGNT[1]#	AM4
PXGNT[2]#	AH15
PXGNT[3]#/*HXPWREN_2*	AG15
PXGNT[4]#/*HXBUSEN_2#*	AG16
PXGNT[5]#/*HXBUSEN_1#*	AP3
PXIRDY#	AM2
PXIRQ[0]#	AT10
PXIRQ[1]#	AR11
PXIRQ[10]#/*HXPCIXCAP1_1*	AT13
PXIRQ[11]#/*HXM66EN_1*	AR14
PXIRQ[12]#/*HXM66EN_2*	AR13
PXIRQ[13]#/*HXPWRFLT_2#*	AP12
PXIRQ[14]#/*HXPWRFLT_1#*	AT12
PXIRQ[15]#/*HXMRL1#*	AP11
PXIRQ[2]#	AR10
PXIRQ[3]#	AP9
PXIRQ[4]#	AR17
PXIRQ[5]#	AN15
PXIRQ[6]#	AP15
PXIRQ[7]#	AR16
PXIRQ[8]#/*HXBUTTON_1#*	AT15
PXIRQ[9]#/*HXPCIXCAP2_1*	AP14
PXM66EN	AC1

Pin Name	Pin Number
PXPAR	AJ16
PXPAR64	AK6
PXPCIRST#	AP5
PXPCIXCAP	AL18
PXPCLKI	AR4
PXPCLKO[0]	AT9
PXPCLKO[1]	AT7
PXPCLKO[2]	AT4
PXPCLKO[3]	AR5
PXPCLKO[4]	AR8
PXPCLKO[5]	AR7
PXPCLKO[6]	AT6
PXPERR#	AG1
PXPLOCK#	AH1
PXPME#	AP6
PXPWROK	AG30
PXREQ[0]#	AN3
PXREQ[1]#	AP2
PXREQ[2]#	AL5
PXREQ[3]#/*HXPRSNT2_1#*	AN6
PXREQ[4]#/*HXPRSNT2_2#*	AN1
PXREQ[5]#/*HXPRSNT1_2#*	AF16
PXREQ64#	AL8
PXSERR#	AC2
PXSTOP#	AJ1
PXTRDY#	AM1
RCIN#	C24
RCOMP	AC10
REQ[0]#	H31
REQ[1]#	E34
REQ[2]#	L28
REQ[3]#	E35
REQ[4]#/GPI[40]	K30
REQ[5]#/GPI[1]	D35
REQ[6]#/GPI[0]	A33
RESERVED	AC29
RESERVED	AD27
RESERVED	AD30
RESERVED	AD33
RESERVED	AE29
STRAP_8	AF19
RESERVED	AG18
RESERVED	AG19

Pin Name	Pin Number
RESERVED	AG21
RESERVED	AH17
RESERVED	AH18
RESERVED	AK9
RESERVED	AN18
VSS	AN19
RI#	J27
RS232_CTS	AT31
RS232_DCD	AP30
RS232_DSR	AR32
RS232_DTR	AR31
RS232_RI	AR29
RS232_RTS	AP29
RS232_SIN	AN30
RS232_SOUT	AT30
RSMRST#	A26
RSTIN#	AJ19
RTCRST#	A29
RTCX1	B26
RTCX2	A27
SATA0GP/GPI[26]	D18
SATA0RXN	K14
SATA0RXP	K15
SATA0TXN	H14
SATA0TXP	H13
SATA1GP/GPI[29]	F18
SATA1RXN	H16
SATA1RXP	H17
SATA1TXN	J16
SATA1TXP	J15
SATA2GP/GPI[30]	C18
SATA2RXN	K17
SATA2RXP	K18
SATA2TXN	L17
SATA2TXP	L16
SATA3GP/GPI[31]	E19
SATA3RXN	G20
SATA3RXP	G21
SATA3TXN	H20
SATA3TXP	H19
SATA4GP/GPI[12]	G18
SATA4RXN	K20
SATA4RXP	K21

Pin Name	Pin Number
SATA4TXN	J22
SATA4TXP	J21
SATA5GP/GPI[13]	A18
SATA5RXN	H22
SATA5RXP	H23
SATA5TXN	L20
SATA5TXP	L19
SATACLKN	G23
SATACLKP	G24
SATALED#	K23
SATARBIAS	J25
SATARBIAS#	H25
SCLK	AJ20
SCLK/GPO[20]	B16
SDATAOUT0/GPO[23]	C15
SDATAOUT1/GPIO[32]	F16
SDP0_0	AK31
SDP0_1	AK30
SDP0_2	AL30
SDP1_0	AL32
SDP1_1	AM31
SDP1_2	AP32
SDP2_0	AM32
SDP2_1	AN31
SDP2_2	AN33
SDP2_3	AN34
SDP2_4	AP33
SDP2_5	AP35
SDP2_6	AR34
SDP2_7	AT33
SDP3_0/LED0_0	AG25
SDP3_4/LED1_0	AH24
SDRAM_A10/SDP3_6/ LED1_2	AH30
SDRAM_A11/SDP3_7/ LED1_3	AH26
SDRAM_A9/SDP3_5/LED1_1	AH27
SDRAM_AD12/SPD3_1/ LED0_1	AH29
SDRAM_BA0/SDP3_2/ LED0_2	AJ31
SDRAM_BA1/SDP3_3/ LED0_3	AJ29
SDTA	AH20
SEICOMPI	W33

Pin Name	Pin Number
SER_CLK_IN	V36
SERCOMPO	W32
SERIRQ	J24
SERN0	V28
SERN1	W35
SERP0	V27
SERP1	W36
SERR#	J36
SETN0	W30
SETN1	Y34
SETP0	W29
SETP1	Y35
SLOAD/GPO[21]	C16
SLP_S3#	D29
SLP_S4#	E29
SLP_S5#	G29
SMBALERT#/GPI[11]	E26
SMBALRT_2	AG31
SMBALRT_3	AJ32
SMBALRT_4	AK33
SMBCLK	G30
SMBCLK0	AE33
SMBCLK1	AG33
SMBCLK2	AF31
SMBCLK3	AH32
SMBCLK4	AJ34
SMBD0	AE32
SMBD1	AG34
SMBD2	AF32
SMBD3	AH33
SMBD4	AK34
SMBDATA	H29
SMBUS[1]	AK19
SMBUS[2]	AN21
SMBUS[3]	AH21
SMBUS[5]	AL21
SMI#	B23
SMLINK0	D30
SMLINK1	F30
SPECFG	AM19
SPKR	C33
STOP#	G35
STPCLK#	C22

Pin Name	Pin Number
STRAP_0	AE26
STRAP_1	AE30
STRAP_2	AD28
STRAP_3	AK21
STRAP_4	K27
STRAP_5	AF20
STRAP_6	AF21
STRAP_7	F19
SUS_STAT#/LPCPD#	H28
SUSCLK	F25
SYS_RESET#	K24
TCK	AG28
TDI	AF28
TDO	AF29
THRM#	F24
THRMTRIP#	B32
TMS	AF26
TP[0]	E28
TRDY#	P28
TRST#	AG27
USBP0N	C9
USBP0P	C10
USBP1N	D8
USBP1P	D9
USBP2N	E7
USBP2P	E8
USBP3N	C6
USBP3P	C7
USBP4N	A5
USBP4P	A6
USBP5N	B4
USBP5P	B5
USBP6N	C3
USBP6P	C4
USBP7N	D2
USBP7P	D3
USBRBIAS	J12
USBRBIAS#	J13
VCC	AA14
VCC	AA16
VCC	AA18
VCC	AA20
VCC	AB13

Pin Name	Pin Number
VCC	AB15
VCC	AB17
VCC	AB19
VCC	AC14
VCC	AC16
VCC	AC18
VCC	AC20
VCC	AD13
VCC	AD15
VCC	AD17
VCC	AD19
VCC	N14
VCC	N16
VCC	N18
VCC	N20
VCC	N22
VCC	P13
VCC	P15
VCC	P17
VCC	P19
VCC	P21
VCC	P23
VCC	R14
VCC	R16
VCC	R18
VCC	R20
VCC	R22
VCC	T13
VCC	T15
VCC	T17
VCC	T19
VCC	T21
VCC	T23
VCC	U14
VCC	U16
VCC	U18
VCC	U20
VCC	U22
VCC	V13
VCC	V15
VCC	V17
VCC	V19
VCC	V21

Pin Name	Pin Number
VCC	V23
VCC	W14
VCC	W16
VCC	W18
VCC	W20
VCC	W22
VCC	Y13
VCC	Y15
VCC	Y17
VCC	Y19
VCC15	AB10
VCC15	AB11
VCC15	AB12
VCC15	AB7
VCC15	AC12
VCC15	AC6
VCC15	AD11
VCC15	AD12
VCC15	AE12
VCC15	AG12
VCC33	AE15
VCC33	AE17
VCC33	AE18
VCC33	AF17
VCC33	AG17
VCC33	AH13
VCC33	AK11
VCC33	AK17
VCC33	AM12
VCC33	AM15
VCC33	AM9
VCC33	AP10
VCC33	AP13
VCC33	AP16
VCC33	AT11
VCC33	AT14
VCC33	AT17
VCC5REF1	U29
VCC5REF2	D14
VCC5REFSUS	E5
VCCA3_3	V30
VCCAESI	M9
VCCAP1	AE11

Pin Name	Pin Number
VCCAP3	AD10
VCCAPE	V7
VCCAPLL	G26
VCCAPLL1_5	V33
VCCARX	A16
VCCARX	B18
VCCARX	D16
VCCARX	F15
VCCARX	K16
VCCARX	M16
VCCASATABG	J18
VCCATX	F17
VCCATX	F20
VCCATX	G19
VCCATX	H18
VCCATX	L18
VCCATX	M18
VCCAUBG	K12
VCCAUPLL	F9
VCCAUX1_5	AA22
VCCAUX1_5	AB21
VCCAUX1_5	AB23
VCCAUX1_5	AC22
VCCAUX1_5	AD21
VCCAUX1_5	AD23
VCCAUX1_5	Y21
VCCAUX1_5	Y23
VCCAUX3_3	AE24
VCCAUX3_3	AF25
VCCAUX3_3	AF27
VCCAUX3_3	AG24
VCCAUX3_3	AG29
VCCAUX3_3	AH25
VCCAUX3_3	AH31
VCCAUX3_3	AJ27
VCCAUX3_3	AK29
VCCAUX3_3	AK32
VCCAUX3_3	AM30
VCCAUX3_3	AM33
VCCAUX3_3	AN35
VCCAUX3_3	AP31
VCCAUX3_3	AR33
VCCAUX3_3	AT29

Pin Name	Pin Number
VCCBGESI	L11
VCCBGPE	V1
VCCP25IDE	N11
VCCP25PCI	T27
VCCPCPU	B24
VCCPCPU	C23
VCCPCPU	D24
VCCPE	AA12
VCCPE	M11
VCCPE	M2
VCCPE	N12
VCCPE	N4
VCCPE	N7
VCCPE	P12
VCCPE	P9
VCCPE	R2
VCCPE	R5
VCCPE	T12
VCCPE	T7
VCCPE	U12
VCCPE	U3
VCCPE	V11
VCCPE	V5
VCCPE	W12
VCCPE	W7
VCCPE	Y12
VCCPE	Y3
VCCPE	Y9
VCCPIDE	A13
VCCPIDE	C14
VCCPIDE	E12
VCCPIDE	H15
VCCPIDE	K13
VCCPIDE	L13
VCCPIDE	L14
VCCPIDE	M13
VCCPPCI	K31
VCCPPCI	L33
VCCPPCI	M29
VCCPPCI	M35
VCCPPCI	N24
VCCPPCI	N26
VCCPPCI	N31

Pin Name	Pin Number
VCCPPCI	P25
VCCPPCI	P26
VCCPPCI	P27
VCCPPCI	P33
VCCPPCI	P36
VCCPPCI	R25
VCCPPCI	R27
VCCPPCI	R29
VCCPPCI	T24
VCCPPCI	T26
VCCPRTC	C27
VCCPSUS	D34
VCCPSUS	F32
VCCPSUS	H30
VCCPSUS	K25
VCCPSUS	K26
VCCPSUS	K28
VCCPSUS	L25
VCCPSUS	L26
VCCPSUS	M25
VCCPUSB	A4
VCCPUSB	B3
VCCPUSB	C5
VCCPUSB	E6
VCCPUSB	G7
VCCSATA	H26
VCCSE	W24
VCCSE	W26
VCCSE	Y24
VCCSE	Y25
VCCSE	Y27
VCCSE	Y30
VCCSE	Y33
VCCSUS1	M27
VCCSUS2	N27
VCCUSB	H10
VCCUSBCORE	D1
VCCUSBCORE	G4
VCCUSBCORE	J8
VCCUSBCORE	K8
VCCUSBCORE	K9
VREFPCIPAD	AC11
VRMPWRGD	K22

Pin Name	Pin Number
VSS	A10
VSS	A19
VSS	A22
VSS	A25
VSS	A28
VSS	A3
VSS	A31
VSS	A34
VSS	A7
VSS	AA11
VSS	AA13
VSS	AA15
VSS	AA17
VSS	AA19
VSS	AA2
VSS	AA21
VSS	AA23
VSS	AA24
VSS	AA26
VSS	AA27
VSS	AA28
VSS	AA29
VSS	AA30
VSS	AA31
VSS	AA32
VSS	AA33
VSS	AA34
VSS	AA5
VSS	AA8
VSS	AB1
VSS	AB14
VSS	AB16
VSS	AB18
VSS	AB20
VSS	AB22
VSS	AB26
VSS	AB27
VSS	AB28
VSS	AB29
VSS	AB30
VSS	AB32
VSS	AB33
VSS	AB34

Pin Name	Pin Number
VSS	AB4
VSS	AC13
VSS	AC15
VSS	AC17
VSS	AC19
VSS	AC21
VSS	AC23
VSS	AC24
VSS	AC25
VSS	AC26
VSS	AC27
VSS	AC28
VSS	AC3
VSS	AC30
VSS	AC31
VSS	AC32
VSS	AC34
VSS	AC36
VSS	AC9
VSS	AD14
VSS	AD16
VSS	AD18
VSS	AD2
VSS	AD20
VSS	AD22
VSS	AD24
VSS	AD26
VSS	AD32
VSS	AD5
VSS	AD8
VSS	AE1
VSS	AE10
VSS	AE14
VSS	AE16
VSS	AE19
VSS	AE20
VSS	AE21
VSS	AE22
VSS	AE25
VSS	AE28
VSS	AE31
VSS	AE34
VSS	AE4

Pin Name	Pin Number
VSS	AE7
VSS	AF12
VSS	AF13
VSS	AF15
VSS	AF24
VSS	AF3
VSS	AF30
VSS	AF33
VSS	AF34
VSS	AF36
VSS	AF6
VSS	AF9
VSS	AG11
VSS	AG14
VSS	AG2
VSS	AG20
VSS	AG23
VSS	AG26
VSS	AG32
VSS	AG35
VSS	AG5
VSS	AG8
VSS	AH10
VSS	AH16
VSS	AH19
VSS	AH22
VSS	AH28
VSS	AH34
VSS	AH4
VSS	AH7
VSS	AJ12
VSS	AJ15
VSS	AJ18
VSS	AJ21
VSS	AJ24
VSS	AJ3
VSS	AJ30
VSS	AJ33
VSS	AJ36
VSS	AJ6
VSS	AJ9
VSS	AK14
VSS	AK2

Pin Name	Pin Number
VSS	AK20
VSS	AK23
VSS	AK26
VSS	AK35
VSS	AK5
VSS	AK8
VSS	AL1
VSS	AL10
VSS	AL13
VSS	AL16
VSS	AL19
VSS	AL22
VSS	AL25
VSS	AL28
VSS	AL31
VSS	AL34
VSS	AL4
VSS	AL7
VSS	AM18
VSS	AM21
VSS	AM24
VSS	AM27
VSS	AM36
VSS	AM6
VSS	AN11
VSS	AN14
VSS	AN17
VSS	AN2
VSS	AN20
VSS	AN23
VSS	AN26
VSS	AN29
VSS	AN32
VSS	AN5
VSS	AN8
VSS	AP1
VSS	AP19
VSS	AP22
VSS	AP25
VSS	AP28
VSS	AP34
VSS	AP36
VSS	AP4

Pin Name	Pin Number
VSS	AP7
VSS	AR12
VSS	AR15
VSS	AR18
VSS	AR2
VSS	AR21
VSS	AR24
VSS	AR27
VSS	AR3
VSS	AR30
VSS	AR35
VSS	AR6
VSS	AR9
VSS	AT20
VSS	AT23
VSS	AT26
VSS	AT3
VSS	AT32
VSS	AT34
VSS	AT5
VSS	AT8
VSS	B12
VSS	B15
VSS	B2
VSS	B21
VSS	B27
VSS	B30
VSS	B33
VSS	B35
VSS	B6
VSS	B9
VSS	C1
VSS	C11
VSS	C17
VSS	C2
VSS	C20
VSS	C26
VSS	C29
VSS	C32
VSS	C35
VSS	C36
VSS	C8
VSS	D10

Pin Name	Pin Number
VSS	D13
VSS	D19
VSS	D22
VSS	D25
VSS	D28
VSS	D31
VSS	D4
VSS	D7
VSS	E15
VSS	E18
VSS	E21
VSS	E24
VSS	E27
VSS	E3
VSS	E30
VSS	E33
VSS	E36
VSS	E9
VSS	F11
VSS	F14
VSS	F2
VSS	F23
VSS	F26
VSS	F29
VSS	F5
VSS	F8
VSS	G1
VSS	G10
VSS	G13
VSS	G16
VSS	G22
VSS	G25
VSS	G28
VSS	G31
VSS	G34
VSS	H12
VSS	H21
VSS	H24
VSS	H27
VSS	H3
VSS	H33
VSS	H36
VSS	H6

Pin Name	Pin Number
VSS	H9
VSS	J11
VSS	J14
VSS	J17
VSS	J2
VSS	J20
VSS	J23
VSS	J26
VSS	J29
VSS	J32
VSS	J35
VSS	J5
VSS	K1
VSS	K10
VSS	K19
VSS	K34
VSS	K4
VSS	K7
VSS	L12
VSS	L15
VSS	L21
VSS	L23
VSS	L24
VSS	L27
VSS	L3
VSS	L30
VSS	L36
VSS	L6
VSS	L9
VSS	M14
VSS	M17
VSS	M19
VSS	M20
VSS	M22
VSS	M26
VSS	M32
VSS	M5
VSS	M8
VSS	N1
VSS	N10
VSS	N13
VSS	N15
VSS	N17

Pin Name	Pin Number
VSS	N19
VSS	N21
VSS	N23
VSS	N25
VSS	N28
VSS	N34
VSS	P14
VSS	P16
VSS	P18
VSS	P20
VSS	P22
VSS	P3
VSS	P30
VSS	P6
VSS	R11
VSS	R12
VSS	R13
VSS	R15
VSS	R17
VSS	R19
VSS	R21
VSS	R23
VSS	R24
VSS	R26
VSS	R32
VSS	R35
VSS	R8
VSS	T1
VSS	T10
VSS	T14
VSS	T16
VSS	T18
VSS	T20
VSS	T22
VSS	T25
VSS	T28
VSS	T31
VSS	T34
VSS	T4
VSS	U13
VSS	U15
VSS	U17
VSS	U19

Pin Name	Pin Number
VSS	U21
VSS	U23
VSS	U24
VSS	U27
VSS	U30
VSS	U33
VSS	U36
VSS	U6
VSS	U9
VSS	V12
VSS	V14
VSS	V16
VSS	V18
VSS	V2
VSS	V20
VSS	V22
VSS	V24
VSS	V26
VSS	V29
VSS	V32
VSS	V35
VSS	V8
VSS	W1
VSS	W10
VSS	W13
VSS	W15
VSS	W17
VSS	W19
VSS	W21
VSS	W23
VSS	W25
VSS	W27
VSS	W28
VSS	W31
VSS	W34
VSS	W4
VSS	Y14
VSS	Y16
VSS	Y18
VSS	Y20
VSS	Y22
VSS	Y26
VSS	Y28

Pin Name	Pin Number
VSS	Y29
VSS	Y31
VSS	Y32
VSS	Y36
VSS	Y6
VSS2	AA25
VSS2	AA35
VSS2	AB24
VSS2	AB25
VSS2	AB31
VSS2	AC33
VSS2	AD29
VSS2	AD35
VSSA3_3	V31
VSSAPE	V6
VSSAPLL1_5	V34
VSSASATABG	J19
VSSAUBG	K11
VSSBGESI	L10
VSSBGPE	AA1
WAKE#	E25

8.2 Intel® 631xESB/632xESB I/O Controller Hub Signal List (Sorted by Ball Number)

Pin Name	Pin Number
A10	VSS
A11	DDACK#
A12	IORDY / DRSTB / WDMARDY#
A13	VCCPIDE
A14	DDREQ
A15	DD[15]
A16	VCCARX
A17	GPO[19]
A18	SATA5GP/GPI[13]
A19	VSS
A20	FWH[0]/LAD[0]
A21	A20M#
A22	VSS
A23	IGNNE#
A24	FERR#
A25	VSS
A26	RSMRST#
A27	RTCX2
A28	VSS
A29	RTCRST#
A3	VSS
A30	PIRQ[B]#
A31	VSS
A32	GNT[5]#/GPO[17]
A33	REQ[6]#/GPI[0]
A34	VSS
A4	VCCPUSB
A5	USBP4N
A6	USBP4P
A7	VSS
A8	DA[2]
A9	DA[0]
AA1	VSSBGPE
AA10	PE2RN3
AA11	VSS
AA12	VCCPE
AA13	VSS
AA14	VCC
AA15	VSS

Pin Name	Pin Number
AA16	VCC
AA17	VSS
AA18	VCC
AA19	VSS
AA2	VSS
AA20	VCC
AA21	VSS
AA22	VCCAUX1_5
AA23	VSS
AA24	VSS
AA25	VSS2
AA26	VSS
AA27	VSS
AA28	VSS
AA29	VSS
AA3	PE2RP0
AA30	VSS
AA31	VSS
AA32	VSS
AA33	VSS
AA34	VSS
AA35	VSS2
AA36	Reserved
AA4	PE2RN0
AA5	VSS
AA6	PE2TP2
AA7	PE2TN2
AA8	VSS
AA9	PE2RP3
AB1	VSS
AB10	VCC15
AB11	VCC15
AB12	VCC15
AB13	VCC
AB14	VSS
AB15	VCC
AB16	VSS
AB17	VCC
AB18	VSS

Pin Name	Pin Number
AB19	VCC
AB2	PE2TP0
AB20	VSS
AB21	VCCAUX1_5
AB22	VSS
AB23	VCCAUX1_5
AB24	VSS2
AB25	VSS2
AB26	VSS
AB27	VSS
AB28	VSS
AB29	VSS
AB3	PE2TN0
AB30	VSS
AB31	VSS2
AB32	VSS
AB33	VSS
AB34	VSS
AB35	LINK_0
AB36	Reserved
AB4	VSS
AB5	PE2RP1
AB6	PE2RN1
AB7	VCC15
AB8	PE2TP3
AB9	PE2TN3
AC1	PXM66EN
AC10	RCOMP
AC11	VREFPCIPAD
AC12	VCC15
AC13	VSS
AC14	VCC
AC15	VSS
AC16	VCC
AC17	VSS
AC18	VCC
AC19	VSS
AC2	PXSERR#
AC20	VCC
AC21	VSS
AC22	VCCAUX1_5
AC23	VSS
AC24	VSS

Pin Name	Pin Number
AC25	VSS
AC26	VSS
AC27	VSS
AC28	VSS
AC29	RESERVED
AC3	VSS
AC30	VSS
AC31	VSS
AC32	VSS
AC33	VSS2
AC34	VSS
AC35	LINK_1
AC36	VSS
AC4	PE2TP1
AC5	PE2TN1
AC6	VCC15
AC7	PE2RP2
AC8	PE2RN2
AC9	VSS
AD1	PXAD[32]
AD10	VCCAP3
AD11	VCC15
AD12	VCC15
AD13	VCC
AD14	VSS
AD15	VCC
AD16	VSS
AD17	VCC
AD18	VSS
AD19	VCC
AD2	VSS
AD20	VSS
AD21	VCCAUX1_5
AD22	VSS
AD23	VCCAUX1_5
AD24	VSS
AD25	NC
AD26	VSS
AD27	RESERVED
AD28	STRAP_2
AD29	VSS2
AD3	PXAD[33]
AD30	RESERVED

Pin Name	Pin Number
AD31	ESB2_TEST2
AD32	VSS
AD33	RESERVED
AD34	NC
AD35	VSS2
AD36	EE_CS#
AD4	PXAD[34]
AD5	VSS
AD6	PXAD[51]
AD7	PXAD[50]
AD8	VSS
AD9	PXAD[52]
AE1	VSS
AE10	VSS
AE11	VCCAP1
AE12	VCC15
AE13	NC
AE14	VSS
AE15	VCC33
AE16	VSS
AE17	VCC33
AE18	VCC33
AE19	VSS
AE2	PXAD[35]
AE20	VSS
AE21	VSS
AE22	VSS
AE23	NC
AE24	VCCAUX3_3
AE25	VSS
AE26	STRAP_0
AE27	Reserved
AE28	VSS
AE29	RESERVED
AE3	PXAD[37]
AE30	STRAP_1
AE31	VSS
AE32	SMBD0
AE33	SMBCLK0
AE34	VSS
AE35	EE_DO
AE36	EE_SK
AE4	VSS

Pin Name	Pin Number
AE5	PXAD[54]
AE6	PXAD[55]
AE7	VSS
AE8	PXAD[53]
AE9	HXATNLED_1#
AF1	PXAD[36]
AF10	PXAD[19]
AF11	PXAD[23]
AF12	VSS
AF13	VSS
AF14	NC
AF15	VSS
AF16	PXREQ[5]#/*HXPRSNT1_2#*
AF17	VCC33
AF18	NC
AF19	STRAP_8
AF2	PXAD[39]
AF20	STRAP_5
AF21	STRAP_6
AF22	NC
AF23	NC
AF24	VSS
AF25	VCCAUX3_3
AF26	TMS
AF27	VCCAUX3_3
AF28	TDI
AF29	TDO
AF3	VSS
AF30	VSS
AF31	SMBCLK2
AF32	SMBD2
AF33	VSS
AF34	VSS
AF35	EE_DI
AF36	VSS
AF4	PXAD[38]
AF5	PXAD[56]
AF6	VSS
AF7	PXAD[58]
AF8	PXCBE[2]#
AF9	VSS
AG1	PXPERR#
AG10	PXAD[21]

Pin Name	Pin Number
AG11	VSS
AG12	VCC15
AG13	PXAD[29]
AG14	VSS
AG15	PXGNT[3]#/*HXPWREN_2*
AG16	PXGNT[4]#/*HXBUSEN_2#*
AG17	VCC33
AG18	RESERVED
AG19	RESERVED
AG2	VSS
AG20	VSS
AG21	RESERVED
AG22	EXTINTR#
AG23	VSS
AG24	VCCAUX3_3
AG25	SDP3_0/LED0_0
AG26	VSS
AG27	TRST#
AG28	TCK
AG29	VCCAUX3_3
AG3	PXAD[40]
AG30	PXPWROK
AG31	SMBALRT_2
AG32	VSS
AG33	SMBCLK1
AG34	SMBD1
AG35	VSS
AG36	FLSH_SO
AG4	PXAD[42]
AG5	VSS
AG6	PXAD[57]
AG7	PXAD[59]
AG8	VSS
AG9	PXAD[16]
AH1	PXPLOCK#
AH10	VSS
AH11	PXCBE[3]#
AH12	PXAD[26]
AH13	VCC33
AH14	PXAD[30]
AH15	PXGNT[2]#
AH16	VSS
AH17	RESERVED

Pin Name	Pin Number
AH18	RESERVED
AH19	VSS
AH2	PXAD[41]
AH20	SDTA
AH21	SMBUS[3]
AH22	VSS
AH23	EBUS_AD[17]
AH24	SDP3_4/LED1_0
AH25	VCCAUX3_3
AH26	SDRAM_A11/SDP3_7/ LED1_3
AH27	SDRAM_A9/SDP3_5/LED1_1
AH28	VSS
AH29	SDRAM_AD12/SPD3_1/ LED0_1
AH3	PXAD[43]
AH30	SDRAM_A10/SDP3_6/ LED1_2
AH31	VCCAUX3_3
AH32	SMBCLK3
AH33	SMBD3
AH34	VSS
AH35	FLSH_SCK
AH36	FLSH_SI
AH4	VSS
AH5	PXAD[60]
AH6	PXAD[61]
AH7	VSS
AH8	PXAD[17]
AH9	PXAD[20]
AJ1	PXSTOP#
AJ10	PXAD[22]
AJ11	PXAD[24]
AJ12	VSS
AJ13	PXAD[28]
AJ14	PXAD[31]
AJ15	VSS
AJ16	PXPAR
AJ17	HPCLK
AJ18	VSS
AJ19	RSTIN#
AJ2	PXAD[44]
AJ20	SCLK
AJ21	VSS

Pin Name	Pin Number
AJ22	EBUS_AD[14]
AJ23	EBUS_AD[16]
AJ24	VSS
AJ25	EBUS_AD[20]
AJ26	EBUS_AD[21]
AJ27	VCCAUX3_3
AJ28	EBUS_AD[23]
AJ29	SDRAM_BA1/SDP3_3/ LED0_3
AJ3	VSS
AJ30	VSS
AJ31	SDRAM_BA0/SDP3_2/ LED0_2
AJ32	SMBALRT_3
AJ33	VSS
AJ34	SMBCLK4
AJ35	FLSH_CE#
AJ36	VSS
AJ4	PXAD[45]
AJ5	PXAD[62]
AJ6	VSS
AJ7	PXAD[63]
AJ8	PXAD[18]
AJ9	VSS
AK1	PXDEVSEL#
AK10	PX133EN
AK11	VCC33
AK12	PXAD[25]
AK13	PXAD[27]
AK14	VSS
AK15	PXAD[12]
AK16	PXAD[15]
AK17	VCC33
AK18	HPDTA
AK19	SMBUS[1]
AK2	VSS
AK20	VSS
AK21	STRAP_3
AK22	EBUS_AD[13]
AK23	VSS
AK24	EBUS_AD[18]
AK25	EBUS_AD[19]
AK26	VSS
AK27	EBUS_AD[22]

Pin Name	Pin Number
AK28	EBUS_AD[24]
AK29	VCCAUX3_3
AK3	PXAD[47]
AK30	SDP0_1
AK31	SDP0_0
AK32	VCCAUX3_3
AK33	SMBALRT_4
AK34	SMBD4
AK35	VSS
AK36	FLBSD1
AK4	PXAD[46]
AK5	VSS
AK6	PXPAR64
AK7	PXCBE[5]#
AK8	VSS
AK9	RESERVED
AL1	VSS
AL10	VSS
AL11	PXAD[5]
AL12	PXAD[7]
AL13	VSS
AL14	PXAD[10]
AL15	PXAD[13]
AL16	VSS
AL17	NC
AL18	PXPCIXCAP
AL19	VSS
AL2	PXAD[48]
AL20	PASTRAP0
AL21	SMBUS[5]
AL22	VSS
AL23	EBUS_AD[15]
AL24	EBUS_AD[3]
AL25	VSS
AL26	EBUS_AD[8]
AL27	EBUS_AD[9]
AL28	VSS
AL29	LAN0_DIS#
AL3	PXAD[49]
AL30	SDP0_2
AL31	VSS
AL32	SDP1_0
AL33	PE_WAKE#

Pin Name	Pin Number
AL34	VSS
AL35	FLBSD0
AL36	FLBSINTEX0
AL4	VSS
AL5	PXREQ[2]#
AL6	PXCBE[4]#
AL7	VSS
AL8	PXREQ64#
AL9	PXAD[1]
AM1	PXTRDY#
AM10	PXAD[3]
AM11	PXAD[6]
AM12	VCC33
AM13	PXCBE[0]#
AM14	PXAD[11]
AM15	VCC33
AM16	PXCBE[1]#
AM17	NC
AM18	VSS
AM19	SPECFG
AM2	PXIRDY#
AM20	NPECFG
AM21	VSS
AM22	EBUS_AD[0]
AM23	EBUS_AD[2]
AM24	VSS
AM25	EBUS_AD[6]
AM26	EBUS_AD[7]
AM27	VSS
AM28	EBUS_AD[11]
AM29	LAN1_DIS#
AM3	PXFRAME#
AM30	VCCAUX3_3
AM31	SDP1_1
AM32	SDP2_0
AM33	VCCAUX3_3
AM34	PERST#
AM35	FLBSINTEX1
AM36	VSS
AM4	PXGNT[1]#
AM5	PXCBE[6]#
AM6	VSS
AM7	PXCBE[7]#

Pin Name	Pin Number
AM8	PXACK64#
AM9	VCC33
AN1	PXREQ[4]#/*HXPRSNT2_2#*
AN10	PXAD[4]
AN11	VSS
AN12	PXAD[8]
AN13	PXAD[9]
AN14	VSS
AN15	PXIRQ[5]#
AN16	PXAD[14]
AN17	VSS
AN18	RESERVED
AN19	VSS
AN2	VSS
AN20	VSS
AN21	SMBUS[2]
AN22	EBUS_AD[1]
AN23	VSS
AN24	EBUS_AD[4]
AN25	EBUS_AD[5]
AN26	VSS
AN27	EBUS_AD[10]
AN28	EBUS_AD[12]
AN29	VSS
AN3	PXREQ[0]#
AN30	RS232_SIN
AN31	SDP2_1
AN32	VSS
AN33	SDP2_2
AN34	SDP2_3
AN35	VCCAUX3_3
AN36	LAN_PWR_GOOD
AN4	PXGNT[0]#
AN5	VSS
AN6	PXREQ[3]#/*HXPRSNT2_1#*
AN7	HPX_PWREN_1
AN8	VSS
AN9	PXAD[2]
AP1	VSS
AP10	VCC33
AP11	PXIRQ[15]#/*HXMRL1#*
AP12	PXIRQ[13]#/*HXPWRFLT_2#*

Pin Name	Pin Number
AP13	VCC33
AP14	PXIRQ[9]#/*HXPCIXCAP2_1*
AP15	PXIRQ[6]#
AP16	VCC33
AP17	HPX_SOD/*HXCLKEN_2#*
AP18	HPX_PRST#/*HXRST1#*
AP19	VSS
AP2	PXREQ[1]#
AP20	HPX_SOLR/*HXATNLED2#*
AP21	HPX_RST2#
AP22	VSS
AP23	EBUS_CE_2#
AP24	EBUS_CE_1#
AP25	VSS
AP26	EBUS_CLK_2
AP27	EBUS_OE#/EBUS_CAS#
AP28	VSS
AP29	RS232_RTS
AP3	PXGNT[5]#/*HXBUSEN_1#*
AP30	RS232_DCD
AP31	VCCAUX3_3
AP32	SDP1_2
AP33	SDP2_4
AP34	VSS
AP35	SDP2_5
AP36	VSS
AP4	VSS
AP5	PXPCIRST#
AP6	PXPME#
AP7	VSS
AP8	PXAD[0]
AP9	PXIRQ[3]#
AR10	PXIRQ[2]#
AR11	PXIRQ[1]#
AR12	VSS
AR13	PXIRQ[12]#/*HXM66EN_2*
AR14	PXIRQ[11]#/*HXM66EN_1*
AR15	VSS
AR16	PXIRQ[7]#
AR17	PXIRQ[4]#
AR18	VSS
AR19	HPX_SIL#/*HXCLKEN_1#*
AR2	VSS

Pin Name	Pin Number
AR20	HPX_SLOT[0]/*HXMRL_2#*
AR21	VSS
AR22	HPX_SLOT[1]/ *HXPRSNT1_1#*
AR23	HPX_SLOT[2]
AR24	VSS
AR25	EBUS_WE#
AR26	EBUS_ALAT/EBUS_CKE
AR27	VSS
AR28	Reserved
AR29	RS232_RI
AR3	VSS
AR30	VSS
AR31	RS232_DTR
AR32	RS232_DSR
AR33	VCCAUX3_3
AR34	SDP2_6
AR35	VSS
AR4	PXPCLKI
AR5	PXPCLKO[3]
AR6	VSS
AR7	PXPCLKO[5]
AR8	PXPCLKO[4]
AR9	VSS
AT10	PXIRQ[0]#
AT11	VCC33
AT12	PXIRQ[14]#/*HXPWRFLT_1#*
AT13	PXIRQ[10]#/*HXPCIXCAP1_1*
AT14	VCC33
AT15	PXIRQ[8]#/*HXBUTTON_1#*
AT16	HPX_SID/*HXPCIXCAP1_2*
AT17	VCC33
AT18	HPX_SLOT[3]/*HXPWRLED1#*
AT19	HPX_SOC/*HXPCIXCAP2_2*
AT20	VSS
AT21	HPX_SIC/*HXPWRLED2#*
AT22	HPX_SOL/*HXBUTTON2#*
AT23	VSS
AT24	EBUS_BE_1#
AT25	EBUS_BE_0#
AT26	VSS
AT27	EBUS_ADV#/EBUS_RAS#
AT28	EBUS_FRST#

Pin Name	Pin Number
AT29	VCCAUX3_3
AT3	VSS
AT30	RS232_SOUT
AT31	RS232_CTS
AT32	VSS
AT33	SDP2_7
AT34	VSS
AT4	PXPCLKO[2]
AT5	VSS
AT6	PXPCLKO[6]
AT7	PXPCLKO[1]
AT8	VSS
AT9	PXPCLKO[0]
B10	DA[1]
B11	IDEIRQ
B12	VSS
B13	DIOR# / DWSTB / RDMARDY#
B14	DIOW# / DSTOP
B15	VSS
B16	SCLK/GPO[20]
B17	GPO[18]
B18	VCCARX
B19	FWH[2]/LAD[2]
B2	VSS
B20	FWH[1]/LAD[1]
B21	VSS
B22	NMI
B23	SMI#
B24	VCCPCPU
B25	PWROK
B26	RTCX1
B27	VSS
B28	GPIO[27]
B29	PIRQ[C]#
B3	VCCPUSB
B30	VSS
B31	GNT[2]#
B32	THRMTRIP#
B33	VSS
B34	CLK14
B35	VSS
B4	USBP5N

Pin Name	Pin Number
B5	USBP5P
B6	VSS
B7	DCS3#
B8	DCS1#
B9	VSS
C1	VSS
C10	USBP0P
C11	VSS
C12	DD[7]
C13	DD[8]
C14	VCCPIDE
C15	SDATAOUT0/GPO[23]
C16	SLOAD/GPO[21]
C17	VSS
C18	SATA2GP/GPI[30]
C19	FWH[3]/LAD[3]
C2	VSS
C20	VSS
C21	INTR
C22	STPCLK#
C23	VCCPCPU
C24	RCIN#
C25	INTVRMEN
C26	VSS
C27	VCCPRTC
C28	INTRUDER#
C29	VSS
C3	USBP6N
C30	PIRQ[D]#
C31	PIRQ[A]#
C32	VSS
C33	SPKR
C34	PCIRST#
C35	VSS
C36	VSS
C4	USBP6P
C5	VCCPUSB
C6	USBP3N
C7	USBP3P
C8	VSS
C9	USBP0N
D1	VCCUSBCORE
D10	VSS

Pin Name	Pin Number
D11	DD[6]
D12	DD[9]
D13	VSS
D14	VCC5REF2
D15	NC
D16	VCCARX
D17	GPIO[34]
D18	SATA0GP/GPI[26]
D19	VSS
D2	USBP7N
D20	FWH[4]/LFRAME#
D21	CPUSLP#
D22	VSS
D23	INIT#
D24	VCCPCPU
D25	VSS
D26	GPIO[24]
D27	ESIDCAC
D28	VSS
D29	SLP_S3#
D3	USBP7P
D30	SMLINK0
D31	VSS
D32	PIRQ[E]#/GPI[2]
D33	GNT[0]#
D34	VCCPSUS
D35	REQ[5]#/GPI[1]
D36	GNT[6]#/GPO[16]
D4	VSS
D5	OC[0]#
D6	OC[1]#
D7	VSS
D8	USBP1N
D9	USBP1P
E1	OC[3]#
E10	DD[0]
E11	DD[2]
E12	VCCPIDE
E13	DD[10]
E14	DD[12]
E15	VSS
E16	GPIO[33]
E17	GPI[7]

Pin Name	Pin Number
E18	VSS
E19	SATA3GP/GPI[31]
E2	OC[2]#
E20	LDRQ[0]#
E21	VSS
E22	A20GATE
E23	INIT3_3V#
E24	VSS
E25	WAKE#
E26	SMBALERT#/GPI[11]
E27	VSS
E28	TP[0]
E29	SLP_S4#
E3	VSS
E30	VSS
E31	PIRQ[F]#/GPI[3]
E32	PIRQ[H]#/GPI[5]
E33	VSS
E34	REQ[1]#
E35	REQ[3]#
E36	VSS
E4	OC[4]#/GPI[9]
E5	VCC5REFSUS
E6	VCCPUSB
E7	USBP2N
E8	USBP2P
E9	VSS
F1	OC[5]#/GPI[10]
F10	DD[1]
F11	VSS
F12	DD[4]
F13	DD[11]
F14	VSS
F15	VCCARX
F16	SDATAOUT1/GPIO[32]
F17	VCCATX
F18	SATA1GP/GPI[29]
F19	STRAP_7
F2	VSS
F20	VCCATX
F21	LDRQ[1]#/GPI[41]
F22	CPUPWRGD/GPO[49]
F23	VSS

Pin Name	Pin Number
F24	THRM#
F25	SUSCLK
F26	VSS
F27	GPIO[25]
F28	PWRBTN#
F29	VSS
F3	ESIRXP[0]
F30	SMLINK1
F31	PIRQ[G]#/GPI[4]
F32	VCCPSUS
F33	AD[30]
F34	AD[29]
F35	NC
F36	DEVSEL#
F4	ESIRXN[0]
F5	VSS
F6	OC[6]#/GPI[14]
F7	OC[7]#/GPI[15]
F8	VSS
F9	VCCAUPLL
G1	VSS
G10	VSS
G11	DD[3]
G12	DD[5]
G13	VSS
G14	DD[13]
G15	DD[14]
G16	VSS
G17	GPI[6]
G18	SATA4GP/GPI[12]
G19	VCCATX
G2	ESITXP[0]
G20	SATA3RXN
G21	SATA3RXP
G22	VSS
G23	SATACLKN
G24	SATACLKP
G25	VSS
G26	VCCAPLL
G27	GPI[8]
G28	VSS
G29	SLP_S5#
G3	ESITXN[0]

Pin Name	Pin Number
G30	SMBCLK
G31	VSS
G32	AD[31]
G33	AD[27]
G34	VSS
G35	STOP#
G36	PERR#
G4	VCCUSBCORE
G5	ESIRXP[1]
G6	ESIRXN[1]
G7	VCCPUSB
G8	ESITXP[3]
G9	ESITXN[3]
H1	PE0TN1
H10	VCCUSB
H11	CLK48
H12	VSS
H13	SATA0TXP
H14	SATA0TXN
H15	VCCPIDE
H16	SATA1RXN
H17	SATA1RXP
H18	VCCATX
H19	SATA3TXP
H2	PE0TP1
H20	SATA3TXN
H21	VSS
H22	SATA5RXN
H23	SATA5RXP
H24	VSS
H25	SATARBIAS#
H26	VCCSATA
H27	VSS
H28	SUS_STAT#/LPCPD#
H29	SMBDATA
H3	VSS
H30	VCCPSUS
H31	REQ[0]#
H32	AD[28]
H33	VSS
H34	AD[24]
H35	PLOCK#
H36	VSS

Pin Name	Pin Number
H4	ESITXP[1]
H5	ESITXN[1]
H6	VSS
H7	ESIRXP[2]
H8	ESIRXN[2]
H9	VSS
J1	ESIRCOMPO
J10	ESIRXN[3]
J11	VSS
J12	USBRBIAS
J13	USBRBIAS#
J14	VSS
J15	SATA1TXP
J16	SATA1TXN
J17	VSS
J18	VCCASATABG
J19	VSSASATABG
J2	VSS
J20	VSS
J21	SATA4TXP
J22	SATA4TXN
J23	VSS
J24	SERIRQ
J25	SATARBIAS
J26	VSS
J27	RI#
J28	GPIO[28]
J29	VSS
J3	PE0RN1
J30	AD[25]
J31	AD[26]
J32	VSS
J33	CBE[3]#
J34	AD[14]
J35	VSS
J36	SERR#
J4	PE0RP1
J5	VSS
J6	ESITXP[2]
J7	ESITXN[2]
J8	VCCUSBCORE
J9	ESIRXP[3]
K1	VSS

Pin Name	Pin Number
K10	VSS
K11	VSSAUBG
K12	VCCAUBG
K13	VCCPIDE
K14	SATA0RXN
K15	SATA0RXP
K16	VCCARX
K17	SATA2RXN
K18	SATA2RXP
K19	VSS
K2	PE0TN2
K20	SATA4RXN
K21	SATA4RXP
K22	VRMPWRGD
K23	SATALED#
K24	SYS_RESET#
K25	VCCPSUS
K26	VCCPSUS
K27	STRAP_4
K28	VCCPSUS
K29	CBE[0]#
K3	PE0TP2
K30	REQ[4]#/GPI[40]
K31	VCCPPCI
K32	AD[13]
K33	AD[12]
K34	VSS
K35	PAR
K36	AD[15]
K4	VSS
K5	PE0RP2
K6	PE0RN2
K7	VSS
K8	VCCUSBCORE
K9	VCCUSBCORE
L1	ESICLK100N
L10	VSSBGESI
L11	VCCBGESI
L12	VSS
L13	VCCPIDE
L14	VCCPIDE
L15	VSS
L16	SATA2TXP

Pin Name	Pin Number
L17	SATA2TXN
L18	VCCATX
L19	SATA5TXP
L2	ESIICOMPI
L20	SATA5TXN
L21	VSS
L22	NC
L23	VSS
L24	VSS
L25	VCCPSUS
L26	VCCPSUS
L27	VSS
L28	REQ[2]#
L29	AD[7]
L3	VSS
L30	VSS
L31	AD[22]
L32	AD[23]
L33	VCCPPCI
L34	AD[10]
L35	CBE[1]#
L36	VSS
L4	PE0TP3
L5	PE0TN3
L6	VSS
L7	PE0RP0
L8	PE0RN0
L9	VSS
M1	ESICLK100P
M10	NC
M11	VCCPE
M12	NC
M13	VCCPIDE
M14	VSS
M15	NC
M16	VCCARX
M17	VSS
M18	VCCATX
M19	VSS
M2	VCCPE
M20	VSS
M21	NC
M22	VSS

Pin Name	Pin Number
M23	NC
M24	NC
M25	VCCPSUS
M26	VSS
M27	VCCSUS1
M28	PCICLK
M29	VCCPPCI
M3	PE0RP3
M30	AD[20]
M31	AD[19]
M32	VSS
M33	AD[5]
M34	AD[6]
M35	VCCPPCI
M36	AD[11]
M4	PE0RN3
M5	VSS
M6	PE0TP0
M7	PE0TN0
M8	VSS
M9	VCCAESI
N1	VSS
N10	VSS
N11	VCCP25IDE
N12	VCCPE
N13	VSS
N14	VCC
N15	VSS
N16	VCC
N17	VSS
N18	VCC
N19	VSS
N2	PE4RP5
N20	VCC
N21	VSS
N22	VCC
N23	VSS
N24	VCCPPCI
N25	VSS
N26	VCCPPCI
N27	VCCSUS2
N28	VSS
N29	IRDY#

Pin Name	Pin Number
N3	PE4RN5
N30	CBE[2]#
N31	VCCPPCI
N32	AD[4]
N33	AD[3]
N34	VSS
N35	AD[9]
N36	AD[8]
N4	VCCPE
N5	PE4RP6
N6	PE4RN6
N7	VCCPE
N8	PE4TP7
N9	PE4TN7
P1	PE4TP4
P10	NC
P11	NC
P12	VCCPE
P13	VCC
P14	VSS
P15	VCC
P16	VSS
P17	VCC
P18	VSS
P19	VCC
P2	PE4TN4
P20	VSS
P21	VCC
P22	VSS
P23	VCC
P24	NC
P25	VCCPPCI
P26	VCCPPCI
P27	VCCPPCI
P28	TRDY#
P29	GNT[1]#
P3	VSS
P30	VSS
P31	PME#
P32	PLTRST#
P33	VCCPPCI
P34	GNT[4]#/GPIO[48]
P35	GNT[3]#

Pin Name	Pin Number
P36	VCCPPCI
P4	PE4TP5
P5	PE4TN5
P6	VSS
P7	PE4RP7
P8	PE4RN7
P9	VCCPE
R1	NC
R10	PE4TP0
R11	VSS
R12	VSS
R13	VSS
R14	VCC
R15	VSS
R16	VCC
R17	VSS
R18	VCC
R19	VSS
R2	VCCPE
R20	VCC
R21	VSS
R22	VCC
R23	VSS
R24	VSS
R25	VCCPPCI
R26	VSS
R27	VCCPPCI
R28	NC
R29	VCCPPCI
R3	PE4RP4
R30	AD[17]
R31	ACZ_SDOUT
R32	VSS
R33	ACZ_SDIN[0]
R34	AD[21]
R35	VSS
R36	AD[2]
R4	PE4RN4
R5	VCCPE
R6	PE4TP6
R7	PE4TN6
R8	VSS
R9	PE4TN0

Pin Name	Pin Number
T1	VSS
T10	VSS
T11	PEICOMPI
T12	VCCPE
T13	VCC
T14	VSS
T15	VCC
T16	VSS
T17	VCC
T18	VSS
T19	VCC
T2	PE4TN3
T20	VSS
T21	VCC
T22	VSS
T23	VCC
T24	VCCPPCI
T25	VSS
T26	VCCPPCI
T27	VCCP25PCI
T28	VSS
T29	FRAME#
T3	PE4TP3
T30	AD[16]
T31	VSS
T32	ACZ_BIT_CLK
T33	ACZ_SYNC
T34	VSS
T35	AD[1]
T36	AD[0]
T4	VSS
T5	PE4RN2
T6	PE4RP2
T7	VCCPE
T8	PE4RN1
T9	PE4RP1
U1	PE4RN3
U10	PE4RN0
U11	PE4RP0
U12	VCCPE
U13	VSS
U14	VCC
U15	VSS

Pin Name	Pin Number
U16	VCC
U17	VSS
U18	VCC
U19	VSS
U2	PE4RP3
U20	VCC
U21	VSS
U22	VCC
U23	VSS
U24	VSS
U25	NC
U26	ESB2_TEST1
U27	VSS
U28	ESB2_TEST0
U29	VCC5REF1
U3	VCCPE
U30	VSS
U31	ACZ_SDIN[1]
U32	ACZ_SDIN[2]
U33	VSS
U34	ACZ_RST#
U35	AD[18]
U36	VSS
U4	PE4TN2
U5	PE4TP2
U6	VSS
U7	PE4TN1
U8	PE4TP1
U9	VSS
V1	VCCBGPE
V10	PECLKN
V11	VCCPE
V12	VSS
V13	VCC
V14	VSS
V15	VCC
V16	VSS
V17	VCC
V18	VSS
V19	VCC
V2	VSS
V20	VSS
V21	VCC

Pin Name	Pin Number
V22	VSS
V23	VCC
V24	VSS
V25	NC
V26	VSS
V27	SERP0
V28	SERN0
V29	VSS
V3	PE1TN1
V30	VCCA3_3
V31	VSSA3_3
V32	VSS
V33	VCCAPLL1_5
V34	VSSAPLL1_5
V35	VSS
V36	SER_CLK_IN
V4	PE1TP1
V5	VCCPE
V6	VSSAPE
V7	VCCAPE
V8	VSS
V9	PECLKP
W1	VSS
W10	VSS
W11	PERCOMPO
W12	VCCPE
W13	VSS
W14	VCC
W15	VSS
W16	VCC
W17	VSS
W18	VCC
W19	VSS
W2	PE1RP2
W20	VCC
W21	VSS
W22	VCC
W23	VSS
W24	VCCSE
W25	VSS
W26	VCCSE
W27	VSS
W28	VSS

Pin Name	Pin Number
W29	SETP0
W3	PE1RN2
W30	SETN0
W31	VSS
W32	SERCOMPO
W33	SEICOMPI
W34	VSS
W35	SERN1
W36	SERP1
W4	VSS
W5	PE1RN1
W6	PE1RP1
W7	VCCPE
W8	PE1TN0
W9	PE1TP0
Y1	PE1TP3
Y10	PE1RP3
Y11	PE1RN3
Y12	VCCPE
Y13	VCC
Y14	VSS
Y15	VCC
Y16	VSS
Y17	VCC
Y18	VSS
Y19	VCC
Y2	PE1TN3
Y20	VSS
Y21	VCCAUX1_5
Y22	VSS
Y23	VCCAUX1_5
Y24	VCCSE
Y25	VCCSE
Y26	VSS
Y27	VCCSE
Y28	VSS
Y29	VSS
Y3	VCCPE
Y30	VCCSE
Y31	VSS
Y32	VSS
Y33	VCCSE
Y34	SETN1

Pin Name	Pin Number
Y35	SETP1
Y36	VSS
Y4	PE1TN2
Y5	PE1TP2
Y6	VSS
Y7	PE1RN0
Y8	PE1RP0
Y9	VCCPE

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9 Mechanical Specifications

Please refer to *Intel® 631xESB /632xESB I/O controller Hub Thermal/Mechanical Design Guidelines* for more detail mechanical and thermal specification.

Figure 9-1. Mechanical Layout

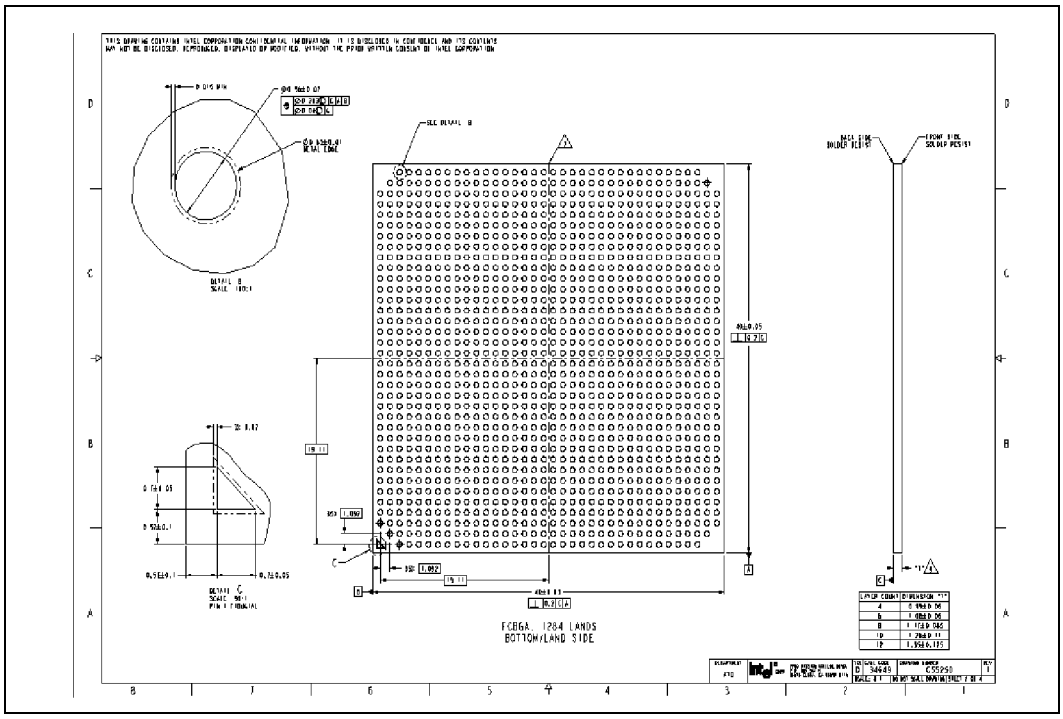


Figure 9-2. Mechanical Layout

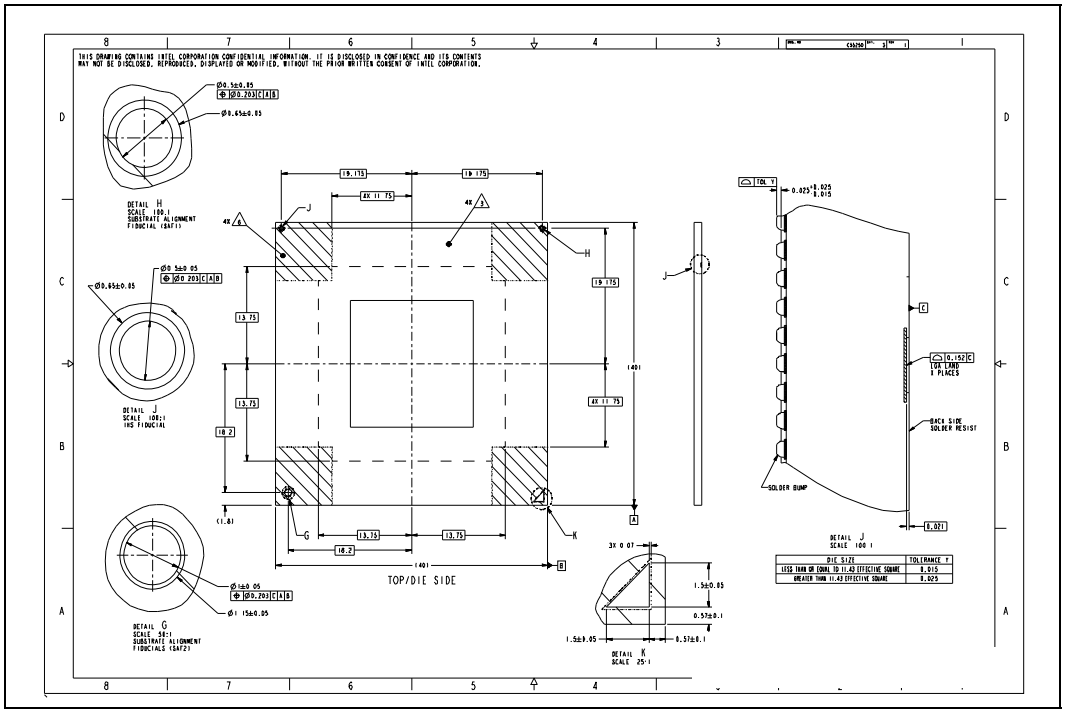


Figure 9-3. Mechanical Layout

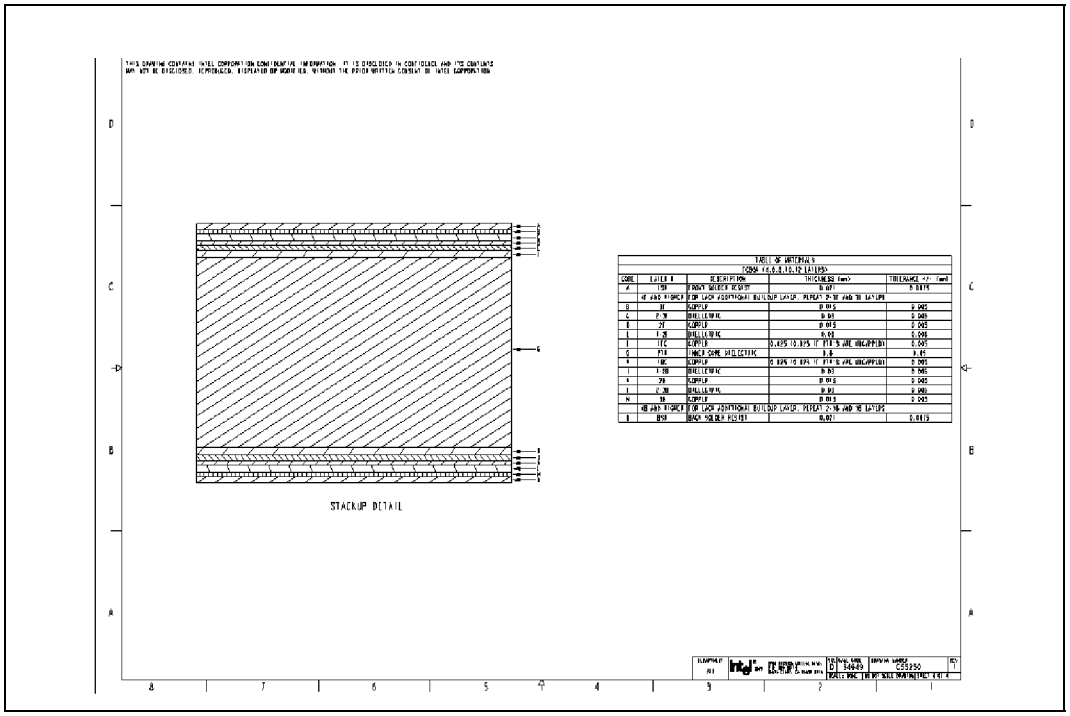
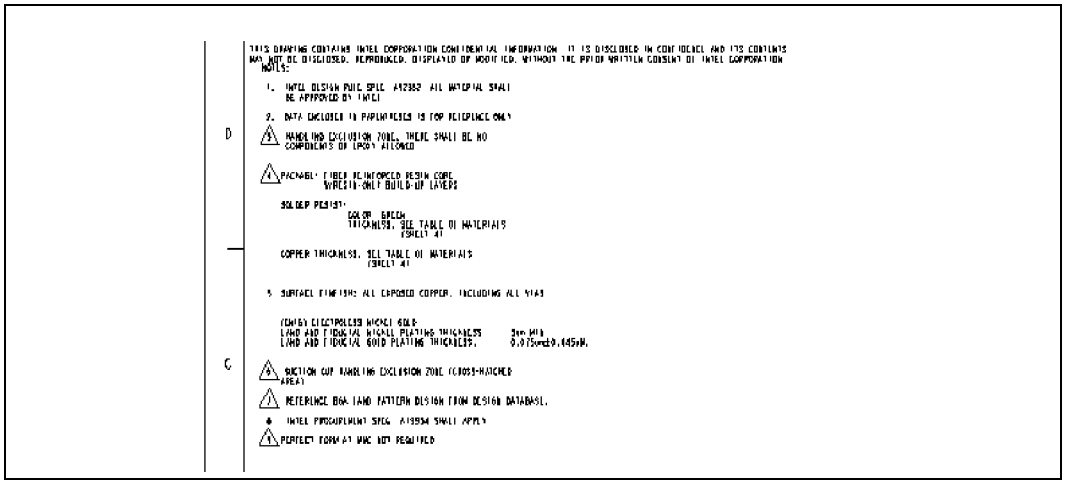


Figure 9-4. Mechanical Layout



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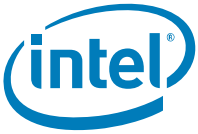


10 Testability

10.1 JTAG Test Mode Description

The Intel® 631xESB/632xESB I/O Controller Hub includes a JTAG (TAP) port compliant with the *IEEE Standard Test Access Port and Boundary Scan Architecture 1149.1 Specification*. The TAP controller is accessed serially through the five dedicated pins TCK, TMS, TDI, TDO, and TRST#. TMS, TDI, and TDO operate synchronously with TCK which is independent of all other clock within the Intel® 631xESB/632xESB I/O Controller Hub. TRST# is an asynchronous test reset input signal. This 5-pin interface operates according to the *IEEE Standard Test Access Port and Boundary Scan Architecture 1149.1 Specification*. This can be used for test and debug purposes. System board interconnects can be DC tested using the boundary scan logic in pads. The Intel® 631xESB/632xESB I/O Controller Hub does *not* provide for accesses to the internal register space through JTAG. SMBus must instead be used. Table 10-1 shows TAP controller related pin descriptions.

Table 10-1. TAP Controller Pins

Signal	I/O	Description
TCK	I	Test clock input for the test logic defined by IEEE1149.1. If utilizing JTAG, connect to this signal ground through a 1 kΩ pull-down resistor.
TDI	I	Test Data Input. Serial test instructions and data are received by the test logic at this pin. If utilizing JTAG, connect this signal to VCC33 through a 1 kΩ pull-up resistor.
TDO	O	Test Data Output. The serial output for the test instructions and data from the test logic defined in IEEE1149.1. If utilizing JTAG, connect this signal to VCC33 through a 1 kΩ pull-up resistor.
TMS	I	Test Mode Select input. The signal received at TMS is decoded by the TAP controller to control test operations. If utilizing JTAG, This pin should have an external 1 kΩ pull-up to VCC33.
TRST#	I	Test Reset input. The optional TRST# input provides for asynchronous initialization of the TAP controller. If utilizing JTAG, connect this signal to ground through a 1 kΩ pull-down resistor.

Table 10-2. TAP Instructions Supported By the Intel® 631xESB/632xESB I/O Controller Hub (Sheet 1 of 2)

Instruction	Description	Comment
BYPASS	The BYPASS command selects the Bypass Register, a single bit register connected between TDI and TDO pins. This allows more rapid movement of test data to and from other components in the system.	IEEE 1149.1 Std. Instruction
EXTEST	The EXTEST Instruction allows circuitry or wiring external to the devices to be tested. Boundary-scan Register Cells at outputs are used to apply stimulus while Boundary-scan cells at input pins are used to capture data.	IEEE 1149.1 Std. Instruction

Table 10-2. TAP Instructions Supported By the Intel® 631xESB/632xESB I/O Controller Hub (Sheet 2 of 2)

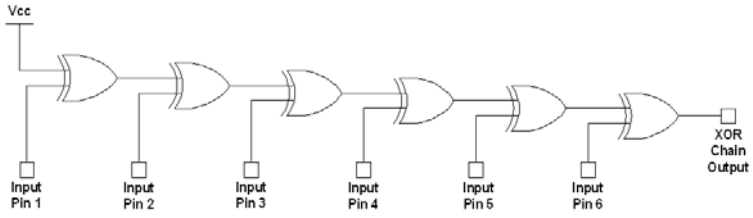
SAMPLE / PRELOAD	The SAMPLE/PRELOAD instruction is used to allow scanning of the boundary scan register without causing interference to the normal operation of the device. Two functions can be performed by use of the Sample/ Preload instruction. SAMPLE – allows a snapshot of the data flowing into and out of a device to be taken without affecting the normal operation of the device. PRELOAD – allows an initial pattern to be placed into the boundary scan register cells. This allows initial known data to be present prior to the selection of another boundary-scan test operation.	IEEE 1149.1 Std. Instruction
IDCODE	The IDCODE instruction is forced into the parallel output latches of the instruction register during the Test-Logic-Reset TAP state. This allows the device identification register to be selected by manipulation of the broadcast TMS and TCK signals for testing purposes, as well as by a conventional instruction register scan operation.	IEEE 1149.1 Std. Instruction
CLAMP	This allows static "guarding values" to be set onto components that are not specifically being tested while maintaining the Bypass register as the serial path through the device.	IEEE 1149.1 Std. Instruction
HIGHZ	The HIGHZ instruction is used to force all outputs of the device (except TDO) into a high impedance state. This instruction shall select the Bypass Register to be connected between TDI and TDO in the Shift-DR controller state.	IEEE 1149.1 Std. Instruction

10.2 XOR Chain Test Mode Description

The Intel® 631xESB/632xESB I/O Controller Hub supports XOR Chain test mode. This non-functional test mode is a dedicated test mode when the chip is not operating in its normal manner. The XOR Chain Mode is entered when ACZ_SDOUT is sampled at high and TP[0] is sampled low upon the assertion of PWROK. REQ[4:1]# straps are used to determine the XOR chain that is selected. See the table below:

REQ# Settings	XOR Chain
REQ[4:1]# = 0000	XOR 1
REQ[4:1]# = 0001	XOR 2
REQ[4:1]# = 0010	XOR 3
REQ[4:1]# = 0011	XOR 4
REQ[4:1]# = 0100	XOR 5

Figure 10-1. Example XOR Chain Circuitry



10.2.1 XOR Chain Testability Algorithm Example

XOR chain testing allows motherboard manufacturers to check component connectivity (for example.,opens and shorts to VCC or GND). An example algorithm is shown in Table 10-3.

Table 10-3. XOR Test Pattern Example

Vector	Input Pin 1	Input Pin 2	Input Pin 3	Input Pin 4	Input Pin 5	Input Pin 6	XOR Output
1	0	0	0	0	0	0	1
2	1	0	0	0	0	0	0
3	1	1	0	0	0	0	1
4	1	1	1	0	0	0	0
5	1	1	1	1	0	0	1
6	1	1	1	1	1	0	0
7	1	1	1	1	1	1	1

In this example, Vector 1 applies all 0's to the chain inputs. The outputs being non-inverting will consistently produce a 1 at the XOR output on a good board. One short to VCC (or open floating to VCC) will result in a 0 at the chain output, signaling a defect.

Likewise, applying Vector 7 (all 1s) to the chain inputs (given that there are an even number of input signals in the chain), will consistently produce a 1 at the XOR chain output on a good board. One short to VSS (or open floating to VSS) will result in a 0 at the chain output, signaling a defect. It is important to note that the number of inputs pulled to 1 will affect the expected chain output value. If the number of chain inputs pulled to 1 is even, then expect 1 at the output. If the number of chain inputs pulled to 1 is odd, expect 0 at the output.

Continuing with the example in Table 10-3, as the input pins are driven to 1 across the chain in sequence, the XOR Output will toggle between 0 and 1. Any break in the toggling sequence (for example, "1011") will identify the location of the short or open.

10.3 XOR Chain Tables

Table 10-4. XOR Chain #1 (REQ[4:1]# = 0000) (Sheet 1 of 2)

Pin Name	Ball #	Notes
CLK48	H11	Top of XOR Chain
DA[0]	A09	2nd signal in XOR
DA[1]	B10	
DA[2]	A08	
DCS3#	B07	
DCS1#	B08	
DD[2]	E11	
DD[1]	F10	
DD[0]	E10	
DD[3]	G11	

Pin Name	Ball #	Notes
DD[7]	C12	15th signal in XOR
DD[4]	F12	
DD[5]	G12	
IORDY/DRSTB/ WDMARDY#	A12	
DIOR#/DWSTB/ RDMARDY	B13	
DD[10]	E13	
DD[8]	C13	
DIOW#/DSTOP	B14	
DDREQ	A14	
DD[12]	E14	

Table 10-4. XOR Chain #1 (REQ[4:1]# = 0000) (Sheet 2 of 2)

Pin Name	Ball #	Notes
DD[6]	D11	
IDEIRQ	B11	
DDACK#	A11	
DD[9]	D12	

Pin Name	Ball #	Notes
DD[11]	F13	
DD[13]	G14	
DD[14]	G15	
DD[15]	A15	
RI#	J27	XOR Chain #1 OUTPUT

Table 10-5. XOR Chain #2 (REQ[4:1]# = 0001)

Pin Name	Ball #	Notes
SATARBIAS#	H25	Top of XOR Chain
SATARBIAS	J25	2nd signal in XOR
SATA0RXN	K14	
SATA0RXP	K15	
SATA0TXN	H14	
SATA0TXP	H13	
SATA1RXN	H16	
SATA1RXP	H17	
SATA1TXN	J16	
SATA1TXP	J15	
GPIO[32]/ SDATAOUT1	F16	
GPIO[33]	E16	
SLOAD/GPO[21]	C16	
GPO[23]/ SDATAOUT0	C15	
GPIO[34]	D17	
GPO[18]	B17	
GPO[19]	A17	
GPO[20]/SCLK	B16	
GPI[6]	G17	
GPI[13]/SATA5GP	A18	
GPI[30]/SATA2GP	C18	

Pin Name	Ball #	Notes
GPI[7]	E17	22nd signal in XOR
GPI[31]/ SATA3GP	E19	
GPI[12]/ SATA4GP	G18	
GPI[29]/ SATA1GP	F18	
GPI[26]/ SATA0GP	D18	
THRM#	F24	
VRMPWRGD	K22	
STRAP_7	F19	
SATALED#	K23	
SERIRQ	J24	
RCIN#	C24	
A20GATE	E22	
INIT3_3V#	E23	
LAD[3]/FWH[3]	C19	
LAD[2]/FWH[2]	B19	
LAD[1]/FWH[1]	B20	
ESIDCAC	D27	
LAD[0]/FWH[0]	A20	
LFRAME#/ FWH[4]	D20	
LDRQ[0]#	E20	
GPI[41]/ LDRQ[1]#	F21	
REQ[5]#/GPI[1]	D35	XOR Chain #2 OUTPUT

Table 10-6. XOR Chain #3 (REQ[4:1]# = 0010)

Pin Name	Ball #	Notes
STPCLK#	C22	Top of XOR Chain
A20M#	A21	2nd signal in XOR
CPUSLP#	D21	
INTR	C21	
NMI	B22	
GPO[49]/ CPUPWRGD	F22	
INIT#	D23	
SMI#	B23	
IGNNE#	A23	
FERR#	A24	
THRMTRIP#	B32	
INTRUDER#	C28	
INTVRMEN	C25	
GPI[11]/ SMBALERT#	E26	
SYS_RESET#	K24	
SUSCLK	F25	
WAKE#	E25	
GPIO[27]	B28	

Pin Name	Ball #	Notes
SUS_STAT#/ LPCPD#	H28	19th signal in XOR
GPIO[25]	F27	
RESERVED	E28	
GPIO[24]	D26	
PWRBTN#	F28	
RI#	J27	
GPI[8]	G27	
GPIO[28]	J28	
SLP_S3#	D29	
SLP_S4#	E29	
SLP_S5#	G29	
SMBDATA	H29	
SMBCLK	G30	
SMLINK1	F30	
SMLINK0	D30	
PME#	P31	
PCIRST#	C34	
PLTRST#	P32	
REQ[5]#/GPI[1]	D35	XOR Chain #3 OUTPUT

Table 10-7. XOR Chain #4-1 (REQ[4:1]# = 0011) (Sheet 1 of 2)

Pin Name	Ball #	Notes
SATA2RXN	K17	Top of XOR Chain
SATA2RXP	K18	2nd signal in XOR
SATA2TXN	L17	
SATA2TXP	L16	
SATA3RXN	G20	
SATA3RXP	G21	
SATA3TXN	H20	
SATA3TXP	H19	
GPI[12]/SATA4GP	G18	
PIRQ[D]#	C30	
SPKR	C33	
CLK14	B34	
GPI[5]/PIRQ[H]#	E32	
GPI[4]/PIRQ[G]#	F31	
GPI[3]/PIRQ[F]#	E31	

Pin Name	Ball #	Notes
AD[30]	F33	37th signal in XOR
SERR#	J36	
AD[14]	J34	
CBE[3]#	J33	
AD[26]	J31	
AD[13]	K32	
AD[12]	K33	
GPI[40]/ REQ[4]#	K30	
CBE[0]#	K29	
REQ[2]#	L28	
AD[7]	L29	
AD[15]	K36	
PAR	K35	
CBE[1]#	L35	
AD[10]	L34	

Table 10-7. XOR Chain #4-1 (REQ[4:1]# = 0011) (Sheet 2 of 2)

Pin Name	Ball #	Notes
GPI[2]/PIRQ[E]#	D32	
PIRQ[A]#	C31	
PIRQ[B]#	A30	
PIRQ[C]#	B29	
GPI[0]/REQ[6]#	A33	
GPO[16]/GNT[6]#	D36	
GPI[1]/REQ[5]#	D35	
GNT[2]#	B31	
GPO[17]/GNT[5]#	A32	
DEVSEL#	F36	
REQ[1]#	E34	
GNT[0]#	D33	
PERR#	G36	
STOP#	G35	
AD[27]	G33	
REQ[3]#	E35	
AD[29]	F34	
AD[24]	H34	
PLOCK#	H35	
AD[28]	H32	
AD[25]	J30	
REQ[0]#	H31	38th signal in XOR
AD[31]	G32	
AD[0]	T36	
AD[1]	T35	
AD[16]	T30	
ACZ_SYNC	T33	
ACZ_BIT_CLK	T32	
ACZ_SDOUT	R31	

Pin Name	Ball #	Notes
AD[22]	L31	
AD[23]	L32	
PCICLK	M28	
AD[20]	M30	
AD[19]	M31	
AD[6]	M34	
CBE[2]#	N30	
AD[5]	M33	
AD[11]	M36	
IRDY#	N29	
AD[9]	N35	
AD[8]	N36	
AD[4]	N32	
AD[3]	N33	
TRDY#	P28	
GNT[1]#	P29	
GPIO[48]/ GNT[4]#	P34	
GNT[3]#	P35	
AD[17]	R30	
AD[21]	R34	
FRAME#	T29	
AD[2]	R36	46th signal in XOR
AD[18]	U35	
ACZ_RST#	U34	
ACZ_SDIN[2]	U32	
ACZ_SDIN[1]	U31	
ACZ_SDIN[0]	R33	
GPI[11]/ SMBALERT#	E26	
RI#	J27	XOR Chain #4 OUTPUT

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Table 10-8. XOR Chain #5 (REQ[4:1]# = 0100)

Pin Name	Ball #	Notes
ESITXN[0]	G03	Top of XOR Chain
ESITXP[0]	G02	2nd signal in XOR
ESIRXN[0]	F04	
ESIRXP[0]	F03	
ESITXN[1]	H05	
ESITXP[1]	H04	
ESIRXN[1]	G06	
ESIRXP[1]	G05	
ESITXN[2]	J07	
ESITXP[2]	J06	
ESIRXN[2]	H08	
ESIRXP[2]	H07	
ESITXN[3]	G09	
ESITXP[3]	G08	
ESIRXN[3]	J10	
ESIRXP[3]	J09	
PE0TN0	M07	
PE0TP0	M06	
PE0RN0	L08	
PE0RP0	L07	
PE0TN1	H01	
PE0TP1	H02	
PE0RN1	J03	
PE0RP1	J04	
PE0TN2	K02	
PE0TP2	K03	
PE0RN2	K06	
PE0RP2	K05	
PE0TN3	L05	
PE0TP3	L04	
PE0RN3	M04	
PE0RP3	M03	

Pin Name	Ball #	Notes
SATA4RXN	K20	25th signal in XOR
SATA4RXP	K21	
SATA4TXN	J22	
SATA4TXP	J21	
SATA5RXN	H22	
SATA5RXP	H23	
SATA5TXN	L20	
SATA5TXP	L19	
GPI[9]/OC[4]#	E04	
GPI[10]/OC[5]#	F01	
GPI[14]/OC[6]#	F06	
GPI[15]/OC[7] #	F07	
OC[3]#	E01	
OC[2]#	E02	
OC[1]#	D06	
OC[0]#	D05	
USBP0N	C09	
USBP0P	C10	
USBP1N	D08	
USBP1P	D09	
USBP2N	E07	
USBP2P	E08	
USBP3N	C06	
USBP3P	C07	
USBP4N	A05	
USBP4P	A06	
USBP5N	B04	
USBP5P	B05	
USBP6N	C03	
USBP6P	C04	
USBP7N	D02	
USBP7P	D03	
REQ[5]#/GPI[1]	D35	XOR Chain #5 OUTPUT

Note: All the Pin Name and Ball # in above tables are the superset of Intel® 631xESB/632xESB I/O Controller Hub SKU Definition (Section 1.3) in Chapter 1.

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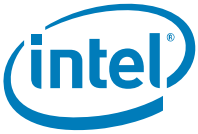

11 Register and Memory Mapping

The Intel® 631xESB/632xESB I/O Controller Hub contains registers that are located in the processor's I/O space and memory space and sets of PCI configuration registers that are located in PCI configuration space. This section describes the Intel® 631xESB/632xESB I/O Controller Hub I/O and memory maps at the register-set level. Register access is also described. Register-level address maps and individual register bit descriptions are provided in the following sections. The following notations and definitions are used in the register/instruction description sections.

11.1 Register Nomenclature and Access Attributes

Table 11-1. Register Nomenclature and Access Attributes

Symbol	Description
RO	**Read Only.** If a register is read only, writes to this register have no effect.However, in other cases, two separate registers are located at the same location where a read accesses one of the registers and a write accesses the other register. See the I/O and memory map tables for details.
WO	**Write Only.** In some cases, If a register is write only, reads to this register location have no effect. However, in other cases, two separate registers are located at the same location where a read accesses one of the registers and a write accesses the other register. See the I/O and memory map tables for details.
ROS	**Read-Only Sticky**. Register bits are read-only and cannot be altered by software. Bits are not cleared by reset and can only be reset with the PWROK reset condition.
RW	**Read / Write.** A register with this attribute can be read and written.
RWC	**Read / Write Clear.** A register bit with this attribute can be read and written. However, a write of a 1 clears (sets to 0) the corresponding bit and a write of a 0 has no effect.
RWCS	**Read and Write One to Clear and Sticky.** through reset. Software needs to write a 1 to this bit to clear it when set. Write of 0 has no effect on this bit. Only a PWROK reset can reset this bit.
RWO	**Read / Write Once.** A register bit with this attribute can be written to only once after power up. After the first write, the bit becomes read only.
RWS	**Read-Write and Sticky.** Software can read and write from this bit and only a PWROK reset can reset this bit.
Reserved Bits	Some of the registers described in the registers section contain reserved bits. These bits are labeled "Reserved". Software must deal correctly with fields that are Reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back. Note the software does not need to perform read, merge, and write operations for the configuration address register.
Reserved Registers	In addition to reserved bits within a register, some address locations in the configuration space that are marked "Reserved". When a "Reserved" register location is read, a random value can be returned. ("Reserved" registers can be 8-, 16-, or 32-bit in size). Registers that are marked as "Reserved" must not be modified by system software. Writes to "Reserved" registers may cause system failure.
Default Value Upon Reset	Upon a Full Reset, the Intel® 631xESB/632xESB I/O Controller Hub sets its internal configuration registers to predetermined **default** states. The default state represents the minimum functionality feature set required to successfully bring up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software (usually BIOS) to properly determine the operating parameters and optional system features that are applicable, and to program the registers accordingly.
Bold	Register bits that are highlighted in bold text indicate that the bit is implemented in the Intel® 631xESB/632xESB I/O Controller Hub. Register bits that are not implemented or are hardwired will remain in plain text.

11.2 PCI Devices and Functions

The Intel® 631xESB/632xESB I/O Controller Hub incorporates a variety of PCI functions as shown in Table 11-2. These functions are divided into seven logical devices (B0:D0, B0:D30, B0:D31, B0:D29, B0:D28, B0:D27 and B1:D8). D0 device contains the PCI Express to PCI-X bridge, I/OxAPIC controller, and PCI Express upstream port. D30 contains the ESI interface-to-PCI bridge and the AC'97 Audio and Modem controller. D31 contains the PCI-to-LPC bridge, IDE controller, SATA controller, and the SMBus controller. D29 contains the four USB UHCI controllers and one USB EHCI controller. Lastly, D27 contains the Azalia controller.

If for some reason, the particular system platform does not want to support any one of the Device Functions, with the exception of D30:F0, they can be individually disabled. When a function is disabled, it does not appear at all to the software. A disabled function will not respond to any register reads or writes. This is intended to prevent software from thinking that a function is present (and reporting it to the end-user).

Table 11-2. PCI Devices and Functions (Sheet 1 of 2)

Bus:Device:Function	Function Description
Bus M:Device 0:Function 0	PCI Express upstream port
Bus M:Device 0:Function 1	I/OxAPIC controller
Bus M:Device 0:Function 3	PCI Express-to-PCI-X Bridge
Bus P:Device 0:Function 0	PCI Express downstream port E1
Bus P:Device 1:Function 0	PCI Express downstream port E2
Bus P:Device 2:Function 0	PCI Express downstream port E3
Bus 0:Device 30:Function 0	PCI-to-PCI Bridge
Bus 0:Device 30:Function 2	AC'97 Audio Controller
Bus 0:Device 30:Function 3	AC'97 Modem Controller
Bus 0:Device 31:Function 0	LPC Controller[1]
Bus 0:Device 31:Function 1	IDE Controller
Bus 0:Device 31:Function 2	SATA Controller
Bus 0:Device 31:Function 3	SMBus Controller
Bus 0:Device 29:Function 0	USB UHCI Controller #1
Bus 0:Device 29:Function 1	USB UHCI Controller #2
Bus 0:Device 29:Function 2	USB UHCI Controller #3
Bus 0:Device 29:Function 3	USB UHCI Controller #4
Bus 0:Device 29:Function 7	USB 2.0 EHCI Controller
Bus 0:Device 28:Function 0	PCI Express Port 1
Bus 0:Device 28:Function 1	PCI Express Port 2
Bus 0:Device 28:Function 2	PCI Express Port 3
Bus 0:Device 28:Function 3	PCI Express Port 4
Bus 0:Device 27:Function 0	Azalia Controller
Bus n:Device 8:Function 0	LAN 0/LAN 1 Controller
Bus n:Device 8:Function 1	LAN 0/LAN 1 Controller
Bus n:Device 8:Function 2	IDE Redirection Controller
Bus n:Device 8:Function 3	Serial Port Redirection Controller

Table 11-2. PCI Devices and Functions (Sheet 2 of 2)

Bus:Device:Function	Function Description
Bus n:Device 8:Function 4	IPMI/KCS0
Bus n:Device 8:Function 5	UHCI Redirection Controller
Bus n:Device 8:Function 7	BT Controller

Note: The LPC controller contains registers that control LPC, Power Management, System Management, GPIO, processor Interface, RTC, Interrupts, Timers, and DMA.

11.3 PCI Configuration Map

Each PCI function on the Intel® 631xESB/632xESB I/O Controller Hub has a set of PCI configuration registers. The register address map tables for these register sets are included at the beginning of the section for the particular function.

Configuration Space registers are accessed through configuration cycles on the PCI bus by the Host bridge using configuration mechanism #1 detailed in the *PCI Local Bus Specification, Revision 2.3*.

Some of the PCI registers contain reserved bits. Software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back. Note the software does not need to perform read, merge, write operation for the configuration address register.

In addition to reserved bits within a register, the configuration space contains reserved locations. Software should not write to reserved PCI configuration locations in the device-specific region (above address offset 3Fh).

11.4 I/O Map

The I/O map is divided into Fixed and Variable address ranges. Fixed ranges cannot be moved, but in some cases can be disabled. Variable ranges can be moved and can also be disabled.

11.4.1 Fixed I/O Address Ranges

Table 11-3 shows the Fixed I/O decode ranges from the processor perspective. Note that for each I/O range, there may be separate behavior for reads and writes. ESI (Enterprise Southbridge Interface) cycles that go to target ranges that are marked as “Reserved” will not be decoded by the Intel® 631xESB/632xESB I/O Controller Hub, and will be passed to PCI. If a PCI master targets one of the fixed I/O target ranges, it will be positively decoded by the Intel® 631xESB/632xESB I/O Controller Hub in medium speed.

Table 11-3. Fixed I/O Ranges Decoded by the Intel® 631xESB/632xESB I/O Controller Hub (Sheet 1 of 2)

I/O Address	Read Target	Write Target	Internal Unit
00h–08h	DMA Controller	DMA Controller	DMA
09h–0Eh	RESERVED	DMA Controller	DMA
0Fh	DMA Controller	DMA Controller	DMA
10h–18h	DMA Controller	DMA Controller	DMA
19h–1Eh	RESERVED	DMA Controller	DMA
1Fh	DMA Controller	DMA Controller	DMA
20h–21h	Interrupt Controller	Interrupt Controller	Interrupt
24h–25h	Interrupt Controller	Interrupt Controller	Interrupt
28h–29h	Interrupt Controller	Interrupt Controller	Interrupt
2Ch–2Dh	Interrupt Controller	Interrupt Controller	Interrupt
2E–2F	LPC SIO	LPC SIO	Forwarded to LPC
30h–31h	Interrupt Controller	Interrupt Controller	Interrupt
34h–35h	Interrupt Controller	Interrupt Controller	Interrupt
38h–39h	Interrupt Controller	Interrupt Controller	Interrupt
3Ch–3Dh	Interrupt Controller	Interrupt Controller	Interrupt
40h–42h	Timer/Counter	Timer/Counter	PIT (8254)
43h	RESERVED	Timer/Counter	PIT
4E–4F	LPC SIO	LPC SIO	Forwarded to LPC
50h–52h	Timer/Counter	Timer/Counter	PIT
53h	RESERVED	Timer/Counter	PIT
60h	Microcontroller	Microcontroller	Forwarded to LPC
61h	NMI Controller	NMI Controller	Processor I/F
62h	Microcontroller	Microcontroller	Forwarded to LPC
63h	NMI Controller	NMI Controller	Processor I/F
64h	Microcontroller	Microcontroller	Forwarded to LPC
65h	NMI Controller	NMI Controller	Processor I/F
66h	Microcontroller	Microcontroller	Forwarded to LPC
67h	NMI Controller	NMI Controller	Processor I/F
70h	RESERVED	NMI and RTC Controller	RTC
71h	RTC Controller	RTC Controller	RTC
72h	RTC Controller	NMI and RTC Controller	RTC
73h	RTC Controller	RTC Controller	RTC
74h	RTC Controller	NMI and RTC Controller	RTC
75h	RTC Controller	RTC Controller	RTC
76h	RTC Controller	NMI and RTC Controller	RTC
77h	RTC Controller	RTC Controller	RTC
80h	DMA Controller, or LPC, or PCI	DMA Controller and LPC or PCI	DMA
81h–83h	DMA Controller	DMA Controller	DMA
84h–86h	DMA Controller	DMA Controller and LPC or PCI	DMA
87h	DMA Controller	DMA Controller	DMA

Table 11-3. Fixed I/O Ranges Decoded by the Intel® 631xESB/632xESB I/O Controller Hub (Sheet 2 of 2)

I/O Address	Read Target	Write Target	Internal Unit
88h	DMA Controller	DMA Controller and LPC or PCI	DMA
89h–8Bh	DMA Controller	DMA Controller	DMA
8Ch–8Eh	DMA Controller	DMA Controller and LPC or PCI	DMA
08Fh	DMA Controller	DMA Controller	DMA
90h–91h	DMA Controller	DMA Controller	DMA
92h	Reset Generator	Reset Generator	Processor I/F
93h–9Fh	DMA Controller	DMA Controller	DMA
A0h–A1h	Interrupt Controller	Interrupt Controller	Interrupt
A4h–A5h	Interrupt Controller	Interrupt Controller	Interrupt
A8h–A9h	Interrupt Controller	Interrupt Controller	Interrupt
ACh–ADh	Interrupt Controller	Interrupt Controller	Interrupt
B0h–B1h	Interrupt Controller	Interrupt Controller	Interrupt
B2h–B3h	Power Management	Power Management	Power Management
B4h–B5h	Interrupt Controller	Interrupt Controller	Interrupt
B8h–B9h	Interrupt Controller	Interrupt Controller	Interrupt
BCh–BDh	Interrupt Controller	Interrupt Controller	Interrupt
C0h–D1h	DMA Controller	DMA Controller	DMA
D2h–DDh	RESERVED	DMA Controller	DMA
DEh–DFh	DMA Controller	DMA Controller	DMA
F0h	PCI and Master Abort[1]	FERR#/IGNNE# / Interrupt Controller	Processor I/F
170h–177h	IDE Controller, SATA Controller, or PCI	IDE Controller, SATA Controller, or PCI	Forwarded to IDE or SATA
1F0h–1F7h	IDE Controller, SATA Controller, or PCI [2]	IDE Controller, SATA Controller, or PCI	Forwarded to IDE or SATA
376h	IDE Controller, SATA Controller, or PCI	IDE Controller, SATA Controller, or PCI	Forwarded to IDE or SATA
3F6h	IDE Controller, SATA Controller, or PCI [2]	IDE Controller, SATA Controller, or PCI	Forwarded to IDE or SATA
4D0h–4D1h	Interrupt Controller	Interrupt Controller	Interrupt
CF9h	Reset Generator	Reset Generator	Processor I/F

Notes:
1. A read to this address will subtractively go to PCI, where it will master abort.
2. Only if IDE I/O space is enabled (D31:F1:40 bit 15) and the IDE controller is in legacy mode. Otherwise, the target is PCI.

11.4.2 Variable I/O Decode Ranges

Table 11-4 shows the Variable I/O Decode Ranges. They are set using Base Address Registers (BARs) or other configuration bits in the various PCI configuration spaces. The PNP software (PCI or ACPI) can use their configuration mechanisms to set and adjust these values.

Warning: The Variable I/O Ranges should not be set to conflict with the Fixed I/O Ranges. Unpredictable results if the configuration software allows conflicts to occur. The Intel® 631xESB/632xESB I/O Controller Hub does not perform any checks for conflicts.

Table 11-4. Variable I/O Decode Ranges

Range Name	Mappable	Size (Bytes)	Target
ACPI	Anywhere in 64 KB I/O Space	64	Power Management
IDE Bus Master	Anywhere in 64 KB I/O Space	16	IDE Unit
USB UHCI Controller #1	Anywhere in 64 KB I/O Space	32	USB Unit 1
SMBus	Anywhere in 64 KB I/O Space	32	SMB Unit
AC'97 Audio Mixer	Anywhere in 64 KB I/O Space	256	AC'97 Unit
AC'97 Audio Bus Master	Anywhere in 64 KB I/O Space	64	AC'97 Unit
AC'97 Modem Mixer	Anywhere in 64 KB I/O Space	256	AC'97 Unit
AC'97 Modem Bus Master	Anywhere in 64 KB I/O Space	128	AC'97 Unit
TCO	96 Bytes above ACPI Base	32	TCO Unit
GPIO	Anywhere in 64 KB I/O Space	64	GPIO Unit
Parallel Port	3 Ranges in 64 KB I/O Space	8	LPC Peripheral
Serial Port 1/2	8 Ranges in 64 KB I/O Space	8	LPC Peripheral
Floppy Disk Controller	2 Ranges in 64 KB I/O Space	8	LPC Peripheral
USB UHCI Controller 2/3/4	Anywhere in 64 KB I/O Space	32	USB Unit 2/3/4
LPC Generic 1	Anywhere in 64 KB I/O Space	128	LPC Peripheral
LPC Generic 2	Anywhere in 64 KB I/O Space	16	LPC Peripheral
I/O Trapping Ranges	Anywhere in 64 KB I/O Space	1 to 256	Trap on Backbone
Native IDE Command	Anywhere in 64 KB I/O Space	8	IDE Unit
Native IDE Control	Anywhere in 64 KB I/O Space	4	IDE Unit
LAN I/O Space 0/1	Anywhere in 64 KB I/O Space	32	LAN Unit
Serial Port	Anywhere in 64 KB I/O Space	8	LAN/Serial Port for remote Keyboard and Text redirection
IDE Command	Anywhere in 64 KB I/O Space	8	LAN/Remote Boot and Installations
IDE IO Control	Anywhere in 64 KB I/O Space	4	LAN/Remote Boot and Installations
IDE IO Bus Master	Anywhere in 64 KB I/O Space	16	LAN/Remote Boot and Installations
IPMI/KCS	Anywhere in 64 KB I/O Space	4	LAN/Enhanced manageability functionality
UHCI	Anywhere in 64 KB I/O Space	32	LAN/Enhanced manageability functionality
BT	Anywhere in 64 KB I/O Space	4	LAN/Enhanced manageability functionality

11.5 Memory Map

Table 11-5 shows (from the processor perspective) the memory ranges that the Intel® 631xESB/632xESB I/O Controller Hub decodes. Cycles that arrive from ESI that are not directed to any of the internal memory targets that decode directly from ESI will be driven out on PCI.

PCI cycles generated by external PCI masters will be positively decoded unless they fall in the PCI-to-PCI bridge memory forwarding ranges. Software must not attempt locks to the Intel® 631xESB/632xESB I/O Controller Hub's memory-mapped I/O ranges for USB2, and HPET. If attempted, the lock is not honored which means potential deadlock conditions may occur.

Table 11-5. Memory Decode Ranges from Processor Perspective (Sheet 1 of 2)

Memory Range	Target	Dependency/Comments
0000 0000h–000D FFFFh 0010 0000h–TOM (Top of Memory)	Main Memory	TOM registers in Host controller
000E 0000h–000E FFFFh	Firmware Hub	Bit 6 in Firmware Hub Decode Enable register is set
000F 0000h–000F FFFFh	Firmware Hub	Bit 7 in Firmware Hub Decode Enable register is set
FEC0 0000h–FEC0 0100h	I/O APIC inside Intel® 631xESB/632xESB I/O Controller Hub	
FFC0 0000h–FFC7 FFFFh FF80 0000h–FF87 FFFFh	Firmware Hub (or PCI)[3]	Bit 8 in Firmware Hub Decode Enable register is set
FFC8 0000h–FFCF FFFFh FF88 0000h–FF8F FFFFh	Firmware Hub (or PCI)[3]	Bit 9 in Firmware Hub Decode Enable register is set
FFD0 0000h–FFD7 FFFFh FF90 0000h–FF97 FFFFh	Firmware Hub (or PCI)[3]	Bit 10 in Firmware Hub Decode Enable register is set
FFD8 0000h–FFDF FFFFh FF98 0000h–FF9F FFFFh	Firmware Hub (or PCI)[3]	Bit 11 in Firmware Hub Decode Enable register is set
FFE0 000h–FFE7 FFFFh FFA0 0000h–FFA7 FFFFh	Firmware Hub (or PCI)[3]	Bit 12 in Firmware Hub Decode Enable register is set
FFE8 0000h–FFEF FFFFh FFA8 0000h–FFAF FFFFh	Firmware Hub (or PCI)[3]	Bit 13 in Firmware Hub Decode Enable register is set
FFF0 0000h–FFF7 FFFFh FFB0 0000h–FFB7 FFFFh	Firmware Hub (or PCI)[3]	Bit 14 in Firmware Hub Decode Enable register is set
FFF8 0000h–FFFF FFFFh FFB8 0000h–FFBF FFFFh	Firmware Hub (or PCI)[3]	Always enabled. The top two 64 KB blocks of this range can be swapped.
FF70 0000h–FF7F FFFFh FF30 0000h–FF3F FFFFh	Firmware Hub (or PCI)[3]	Bit 3 in Firmware Hub Decode Enable register is set
FF60 0000h–FF6F FFFFh FF20 0000h–FF2F FFFFh	Firmware Hub (or PCI)[3]	Bit 2 in Firmware Hub Decode Enable register is set
FF50 0000h–FF5F FFFFh FF10 0000h–FF1F FFFFh	Firmware Hub (or PCI)[3]	Bit 1 in Firmware Hub Decode Enable register is set
FF40 0000h–FF4F FFFFh FF00 0000h–FF0F FFFFh	Firmware Hub (or PCI)[3]	Bit 0 in Firmware Hub Decode Enable register is set
1 KB anywhere in 4-GB range	USB EHCI Controller 2	Enable via standard PCI mechanism (Device 29, Function 7)
512 B anywhere in 4-GB range	AC'97 Host Controller (Mixer)	Enable via standard PCI mechanism (Device 30, Function 2)
256 B anywhere in 4-GB range	AC'97 Host Controller (Bus Master)	Enable via standard PCI mechanism (Device 30, Function 3)
512 B anywhere in 64-bit addressing space	Intel High Definition Audio Host Controller	Enable via standard PCI mechanism (Device 30, Function 1)
FED0 X000h–FED0 X3FFh	High Precision Event Timers[2]	BIOS determines the "fixed" location which is one of four, 1-KB ranges where X (in the first column) is 0h, 1h, 2h, or 3h.
128 KB anywhere in 4-GB range, 64-bit range	Integrated LAN Controller[1] (Mem Space)	Enable via BAR in Device Bn:Function 0/1 (Integrated LAN Controller)
64 KB to 8 MB anywhere in 4-GB, 64-bit range	Integrated LAN Controller[1] (Flash Space)	Enable via BAR in Device Bn:Function 0 (Integrated LAN Controller)

Table 11-5. Memory Decode Ranges from Processor Perspective (Sheet 2 of 2)

Memory Range	Target	Dependency/Comments
4 KB anywhere in 4-GB range, 64-bit range	Integrated LAN Controller[1] (IDE)	Enable via BAR in Device Bn:Function 2(Integrated LAN Controller)
4 KB anywhere in 4-GB range, 64-bit range	Integrated LAN Controller[1] (Serial)	Enable via BAR in Device Bn:Function 3(Integrated LAN Controller)
4 KB anywhere in 4-GB range, 64-bit range	Integrated LAN Controller[1] (IPMI/KCS)	Enable via BAR in Device Bn:Function 4(Integrated LAN Controller)
4 KB anywhere in 4-GB range, 64-bit range	Integrated LAN Controller[1] (UHCI)	Enable via BAR in Device Bn:Function 5(Integrated LAN Controller)
4 KB anywhere in 4-GB range, 64-bit range	Integrated LAN Controller[1] (BT)	Enable via BAR in Device Bn:Function 7(Integrated LAN Controller)
anywhere in 4-GB, 64-bit range4	Intel® 631xESB/632xESB I/O Controller Hub PCI Express Switch (Prefetch Memory)	Enable via BAR in Bm:Device 0:Function 0
4 KB anywhere in 64-bit range	Intel® 631xESB/632xESB I/O Controller Hub PCI Express Switch (SHPC)	Enable via BAR in Bm:Device 0:Function 0
4 KB anywhere in 4-GB range	Intel® 631xESB/632xESB I/O Controller Hub IOxAPIC (Bm:D0:F1)	Enable via MBAR in Bm:Device 0:Function 1

Notes:
1. Only LAN cycles can be seen on PCI.
2. Software must not attempt locks to memory mapped I/O ranges for USB EHCI or High Precision Event Timers. If attempted, the lock is not honored, which means potential deadlock conditions may occur.
3. PCI is the target when the Boot BIOS Destination selection bit is low (Chipset Config Registers:Offset 3401:bit 3). When PCI selected, the Firmware Hub Decode Enable bits have no effect.
4. Programmable range.

§§

12 Chipset Configuration Registers

This section describes all registers and base functionality that is related to chipset configuration and not a specific interface (such as LPC, PCI, or PCI Express). It contains the root complex register block, which describes the behavior of the upstream internal link.

This block is mapped into memory space, using register RCBA of the PCI-to-LPC bridge. Accesses in this space must be limited to 32-(DW) bit quantities. Burst accesses are not allowed.

12.1 Chipset Configuration Registers (Memory Space)

Note: Address locations that are not shown should be treated as Reserved (see Section 11.1 for details).

Table 12-1. Chipset Configuration Register Memory Map (Memory Space) (Sheet 1 of 3)

Offset	Mnemonic	Register Name	Default	Type
0000–0003h	VCH	Virtual Channel Capability Header	10010002h	RO
0004–0007h	VCAP1	Virtual Channel Capability #1	00000801h	RO
0008–000Bh	VCAP2	Virtual Channel Capability #2	00000001h	RO
000C–000Dh	PVC	Port VC Control	0000h	R/W, RO
000E–000Fh	PVS	Port VC Status	0000h	RO
0010–0013h	V0CAP	VC 0 Resource Capability	00000001h	RO
0014–0017h	V0CTL	VC 0 Resource Control	800000FFh	R/W, RO
001A–001Bh	V0STS	VC 0 Resource Status	0000h	RO
001C–001Fh	V1CAP	VC 1 Resource Capability	30008010h	R/WO, RO
0020–0023h	V1CTL	VC 1 Resource Control	00000000h	R/W, RO
0026–0027h	V1STS	VC 1 Resource Status	0000h	RO
0030–006Fh	PAT[0–F]	Port Arbitration Table	See bit description	RO
0084–0087h	UES	Uncorrectable Error Status	00000000h	R/WC, RO
0088–008Bh	UEM	Uncorrectable Error Mask	00000000h	R/WO, RO
008C–008Dh	UEV	Uncorrectable Error Severity	00000000h	R/W, RO
0090–0093h	CES	Correctable Error Status	00000000h	R/WC
0094–0097h	CEM	Correctable Error Mask	00000000h	R/WO
0098–009Bh	AECC	Advanced Error Capabilities and Control	00000000h	RO
00B0–00B3h	RES	Root Error Status	00000000h	R/WC, RO
00B4–00B7h	ESID	Error Source Identification	00000000h	RO
0100–0103h	RCTCL	Root Complex Topology Capability List	1A010005h	RO
0104–0107h	ESD	Element Self Description	00000502h	R/WO, RO
0110–0113h	ULD	Upstream Link Descriptor	00000001h	R/WO, RO
0114–011Bh	ULBA	Upstream Link Base Address	0000000000000000h	R/WO
0120–0123h	RP0D	Root Port 0 Descriptor	01xx0002h	R/WO, RO
0128–012Fh	RP0BA	Root Port 0 Base Address	00000000000E0000h	RO

Table 12-1. Chipset Configuration Register Memory Map (Memory Space) (Sheet 2 of 3)

Offset	Mnemonic	Register Name	Default	Type
0130–0133h	RP1D	Root Port 1 Descriptor	02xx0002h	R/WO, RO
0138–013Fh	RP1BA	Root Port 1 Base Address	00000000000E1000h	RO
0140–0143h	RP2D	Root Port 2 Descriptor	03xx0002h	R/WO, RO
0148–014Fh	RP2BA	Root Port 2 Base Address	00000000000E2000h	RO
0150–0153h	RP3D	Root Port 3 Descriptor	04xx0002h	R/WO, RO
0158–015Fh	RP3BA	Root Port 3 Base Address	00000000000E3000h	RO
0160–0163h	AZD	Intel High Definition Audio Descriptor	05xx0002h	R/WO, RO
0168–016Fh	AZBA	Intel High Definition Audio Base Address	00000000000D8000h	RO
01A0–01A3h	ILCL	Internal Link Capability List	00010006h	RO
01A4–01A7h	LCAP	Link Capabilities	00012441h	R/W, RO
01A8–01A9h	LCTL	Link Control	0000h	R/W
01AA–01ABh	LSTS	Link Status	0041h	RO
01F0–01F3h	VPCAP	Private Virtual Channel Resource Capability	00000001h	RO
01F4–01F7h	VPCTL	Private Virtual Channel Resource Control	00000000h	R/W, RO
01FA–01FBh	VPSTS	Private Virtual Channel Resource Status	0000h	RO
01FC–01FFh	VPR	Private Virtual Channel Routing	00000000h	R/W
0200–0203h	L3A	Level 3 Backbone Arbiter Configuration	01100220h	R/W
0208–020Bh	L2A	Level 2 Backbone Arbiter Configuration	00000404h	R/W
020C–020Fh	L1A	Level 1 Backbone Arbiter Configuration	00201004h	R/W
0210–0213h	DA	Downstream Arbiter Configuration	0000F711h	R/W
0214–0217h	UNRL	Upstream Non-Posted Request Limits	100E0E8Eh	R/W
0218–021Bh	UMR	Upstream Minimum Reserved	00010101h	R/W
021C–021Fh	QL	Queue Limits	00000000h	R/W
0220–0223h	GBC	Generic Backbone Configuration	00000000h	R/W
0224–0227h	RPC	Root Port Configuration	00000000h	R/W
0228–022Bh	BAC	Bandwidth Allocation Configuration	141200AAh	R/W
022C–022Fh	AS	Arbiter Status	00000000h	R/WC
3000–3001h	TCTL	TCO Control	00h	R/W
3100–3103h	D31IP	Device 31 Interrupt Pin	00042210h	R/W, RO
3104–3107h	D30IP	Device 30 Interrupt Pin	00002100h	R/W, RO
3108–310Bh	D29IP	Device 29 Interrupt Pin	10004321h	R/W
310C–310Fh	D28IP	Device 28 Interrupt Pin	00004321h	R/W
3110–3113h	D27IP	Device 27 Interrupt Pin	00000001h	R/W
3140–3141h	D31IR	Device 31 Interrupt Route	3210h	R/W
3142–3143h	D30IR	Device 30 Interrupt Route	3210h	R/W
3144–3145h	D29IR	Device 29 Interrupt Route	3210h	R/W
3146–3147h	D28IR	Device 28 Interrupt Route	3210h	R/W
3148–3149h	D27IR	Device 27 Interrupt Route	3210h	R/W
31FF–31FFh	OIC	Other Interrupt Control	00h	R/W

Table 12-1. Chipset Configuration Register Memory Map (Memory Space) (Sheet 3 of 3)

Offset	Mnemonic	Register Name	Default	Type
3400–3403h	RC	RTC Configuration	00000000h	R/W, R/WO
3404–3407h	HPTC	High Precision Timer Configuration	00000000h	R/W
3410–3413h	GCS	General Control and Status	0000000xh	R/W, R/WO
3414–3414h	BUC	Backed Up Control	0000000xb	R/W
3418–341Bh	FD	Function Disable	See bit description	R/W, RO
341C–341Fh	CG	Clock Gating	00000000h	R/W, RO

12.1.1 VCH – Virtual Channel Capability Header Register

Offset Address: 0000–0003h Attribute: RO
Default Value: 10010002h Size: 32-bit

Bit	Description
31:20	**Next Capability Offset (NCO)** – RO. Indicates the next item in the list.
19:16	**Capability Version (CV)** – RO. Indicates this is version 1 of the capability structure by the PCI SIG.
15:0	**Capability ID (CID)** – RO. Indicates this is the Virtual Channel capability item.

12.1.2 VCAP1 – Virtual Channel Capability #1 Register

Offset Address: 0004–0007h Attribute: RO
Default Value: 00000801h Size: 32-bit

Bit	Description
31:12	Reserved
11:10	**Port Arbitration Table Entry Size (PATS)** – RO. Indicates the size of the port arbitration table is 4 bits (to allow up to 8 ports).
9:8	**Reference Clock (RC)** – RO. Fixed at 100ns for this version of the PCI Express specification.
7	Reserved
6:4	**Low Priority Extended VC Count (LPEVC)** – RO. Indicates that there are no additional VCs of low priority with extended capabilities.
3	Reserved
2:0	**Extended VC Count (EVC)** – RO. Indicates that there is one additional VC (VC1) that exists with extended capabilities

12.1.3 VCAP2 – Virtual Channel Capability #2 Register

Offset Address: 0008–000Bh Attribute: RO
Default Value: 00000001h Size: 32-bit

Bit	Description
31:24	**VC Arbitration Table Offset (ATO)** – RO. Indicates that no table is present for VC arbitration since it is fixed.
23:8	Reserved
7:0	**VC Arbitration Capability (AC)** – RO. Indicates that the VC arbitration is fixed in the root complex. VC1 is highest priority, VCp (the private VC) is next in priority, and VC0 is lowest priority.

12.1.4 PVC – Port Virtual Channel Control Register

Offset Address: 000C–000Dh Attribute: R/W, RO
Default Value: 0000h Size: 16-bit

Bit	Description
15:04	Reserved
3:1	**VC Arbitration Select (AS)** – RO. Indicates which VC should be programmed in the VC arbitration table. The root complex takes no action on the setting of this field since there is no arbitration table.
0	**Load VC Arbitration Table (LAT)** – RO. Indicates that the table programmed should be loaded into the VC arbitration table. This bit is defined as read/write with always returning 0 on reads.

12.1.5 PVS – Port Virtual Channel Status Register

Offset Address: 000E–000Fh Attribute: RO
Default Value: 0000h Size: 16-bit

Bit	Description
15:01	Reserved
0	**VC Arbitration Table Status (VAS)** – RO. Indicates the coherency status of the VC Arbitration table when it is being updated. This field is always 0 in the root complex since there is no VC arbitration table.

12.1.6 V0CAP – Virtual Channel 0 Resource Capability Register

Offset Address: 0010–0013h Attribute: RO
Default Value: 00000001h Size: 32-bit

Bit	Description
31:24	**Port Arbitration Table Offset (AT)** – RO. This VC implements no port arbitration table since the arbitration is fixed.
23	Reserved
22:16	**Maximum Time Slots (MTS)** – RO. This VC implements fixed arbitration, and therefore this field is not used.
15	**Reject Snoop Transactions (RTS)** – RO. This VC must be able to take snoopable transactions.
14	**Advanced Packet Switching (APS)** – RO. This VC is capable of all transactions, not just advanced packet switching transactions.
13:8	Reserved
7:0	**Port Arbitration Capability (PAC)** – RO. Indicates that this VC uses fixed port arbitration.

12.1.7 V0CTL – Virtual Channel 0 Resource Control Register

Offset Address: 0014–0017h Attribute: R/W, RO
Default Value: 800000FFh Size: 32-bit

Bit	Description
31	**Virtual Channel Enable (EN)** – RO. Enables the VC when set. Disables the VC when cleared.
30:27	Reserved
26:24	**Virtual Channel Identifier (ID)** – RO. Indicates the ID to use for this virtual channel.
23:20	Reserved

Bit	Description
19:17	**Port Arbitration Select (PAS)** – RW. Indicates which port table is being programmed. The root complex takes no action on this setting since the arbitration is fixed and there is no arbitration table.
16	**Load Port Arbitration Table (LAT)** – RO. The root complex does not implement an arbitration table for this virtual channel.
15:8	Reserved
7:1	**Transaction Class / Virtual Channel Map (TVM)** – RW. Indicates which transaction classes are mapped to this virtual channel. When a bit is set, this transaction class is mapped to the virtual channel.
0	Reserved

12.1.8 V0STS – Virtual Channel 0 Resource Status Register

Offset Address: 001A–001Bh Attribute: RO
Default Value: 0000h Size: 16-bit

Bit	Description
15:02	Reserved
1	**VC Negotiation Pending (NP)** – RO. When set, indicates the virtual channel is still being negotiated with ingress ports.
0	**Port Arbitration Tables Status (ATS)** – R0. There is no port arbitration table for this VC, so this bit is reserved at 0.

12.1.9 V1CAP – Virtual Channel 1 Resource Capability Register

Offset Address: 001C–001Fh Attribute: R/WO, RO
Default Value: 30008010h Size: 32-bit

Bit	Description
31:24	**Port Arbitration Table Offset (AT)** – RO. Indicates the location of the port arbitration table in the root complex. A value of 3h indicates the table is at offset 30h.
23	Reserved
22:16	**Maximum Time Slots (MTS)** – RWO. This value is updated by platform BIOS based upon the determination of the number of time slots available in the platform.
15	**Reject Snoop Transactions (RTS)** – RO. All snoopable transactions on VC1 are rejected. This VC is for isochronous transfers only.
14	**Advanced Packet Switching (APS)** – RO. This VC is capable of all transactions, not just advanced packet switching transactions.
13:8	Reserved
7:0	**Port Arbitration Capability (PAC)** – RO. Indicates the port arbitration capability is time-based WRR of 128 phases.

12.1.10 V1CTL – Virtual Channel 1 Resource Control Register

Offset Address: 0020–0023h Attribute: R/W, RO
Default Value: 00000000h Size: 32-bit

Bit	Description
31	**Virtual Channel Enable (EN)** – R/W. Enables the VC when set. Disables the VC when cleared.
30:27	Reserved
26:24	**Virtual Channel Identifier (ID)** – R/W. Indicates the ID to use for this virtual channel.
23:20	Reserved
19:17	**Port Arbitration Select (PAS)** – RW. Indicates which port table is being programmed. The only permissible value of this field is 4h for the time-based WRR entries.
16	**Load Port Arbitration Table (LAT)** – RO/W. When set, the port arbitration table loaded based upon the PAS field in this register. This bit always returns 0 when read.
15:8	Reserved
7:1	**Transaction Class / Virtual Channel Map (TVM)** – RW. Indicates which transaction classes are mapped to this virtual channel. When a bit is set, this transaction class is mapped to the virtual channel.
0	Reserved

12.1.11 V1STS – Virtual Channel 1 Resource Status Register

Offset Address: 0026–0027h Attribute: RO
Default Value: 0000h Size: 16-bit

Bit	Description
15:02	Reserved
1	**VC Negotiation Pending (NP)** – RO. When set, indicates the virtual channel is still being negotiated with ingress ports.
0	**Port Arbitration Tables Status (ATS)** – R0. Indicates the coherency status of the port arbitration table. This bit is set during a table update, and cleared after the table has been updated.

12.1.12 PAT[0-F] – Port Arbitration Table Register

Offset Address: 0030–006Fh Attribute: RO
Default Value: See Description Size: 64-Byte

This is a 64-byte register that contains the arbitration table to be loaded into the port arbitration table. Every 4-bits contains an entry for one of the downstream PCI Express ports or a 0h to indicate idle. The ports are mapped as follows:

- Port 0: Value used is 1h.
- Port 1: Value used is 2h.
- Port 2: Value used is 3h
- Port 3: Value used is 4h

This table is copied to an internal structure used during port arbitration when V1CTL.PAS (offset 0020h, bits 19:17) is set to 4h, and V1CTL.LAT (offset 0020h, bits 16) is set to 1.

12.1.13 UES – Uncorrectable Error Status Register

Offset Address: 0084–0087h
Default Value: 00000000h
Attribute: R/WC, RO
Size: 32-bit

Bit	Description
31:21	Reserved
20	**Unsupported Request Error Status (URE)** – R/WC. Indicates an unsupported request was received.
19	ECRC Error Status (EE) – RO. ECRC is not supported.
18	**Malformed TLP Status (MT)** – R/WC. Indicates a malformed TLP was received.
17	**Receiver Overflow Status (RO)** – R/WC. Indicates a receiver overflow occurred.
16	**Unexpected Completion Status (UC)** – R/WC. Indicates an unexpected completion was received.
15	**Completer Abort Status (CA)** – R/WC. Indicates a completer abort was received.
14	**Completion Timeout Status (CT)** – R/WC. Indicates a completion timed out.
13	**Flow Control Protocol Error Status (FCPE)** – R/WC. Indicates a flow control protocol error occurred.
12	**Poisoned TLP Status (PT)** – R/WC. Indicates a poisoned TLP was received.
11:5	Reserved
4	**Data Link Protocol Error Status (DLPE)** – R/WC. Indicates a data link protocol error occurred.
3:1	Reserved
0	**Training Error Status (TE)** – RO. Not supported.

12.1.14 UEM – Uncorrectable Error Mask Register

Offset Address: 0088–008Bh
Default Value: 00000000h
Attribute: R/WO, RO
Size: 32-bit

When set, the corresponding error in the UES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled.

Bit	Description
31:21	Reserved
20	**Unsupported Request Error Mask (URE)** – R/WO. Mask for uncorrectable errors.
19	ECRC Error Mask (EE) – RO. ECRC is not supported.
18	**Malformed TLP Mask (MT)** – R/WO. Mask for malformed TLPs.
17	**Receiver Overflow Mask (RO)** – R/WO. Mask for receiver overflows.
16	**Unexpected Completion Mask (UC)** – R/WO. Mask for unexpected completions.
15	**Completer Abort Mask (CA)** – R/WO. Mask for completer abort.
14	**Completion Timeout Mask (CT)** – R/WO. Mask for completion timeouts.
13	**Flow Control Protocol Error Mask (FCPE)** – R/WO. Mask for flow control protocol errors.
12	**Poisoned TLP Mask (PT)** – R/WO. Mask for poisoned TLPs.
11:5	Reserved
4	**Data Link Protocol Error Mask (DLPE)** – R/WO. Mask for data link protocol errors.
3:1	Reserved
0	**Training Error Mask (TE)** – RO. Not supported.

12.1.15 UEV – Uncorrectable Error Severity Register

Offset Address: 008C–008Fh Attribute: R/W, RO
Default Value: 00000000h Size: 32-bit

Bit	Description
31:21	Reserved
20	**Unsupported Request Error Severity (URE)** – R/W. Severity for unsupported request reception.
19	ECRC Error Severity (EE) – RO. ECRC is not supported.
18	**Malformed TLP Severity (MT)** – R/W. Severity for malformed TLP reception.
17	**Receiver Overflow Severity (RO)** – R/W. Severity for receiver overflow occurrences.
16	**Unexpected Completion Severity (UC)** – R/W. Severity for unexpected completion reception.
15	**Completer Abort Severity (CA)** – R/W. Severity for completer.
14	**Completion Timeout Severity (CT)** – R/W. Severity for completion timeout.
13	**Flow Control Protocol Error Severity (FCPE)** – R/W. Severity for flow control protocol errors.
12	**Poisoned TLP Severity (PT)** – R/W. Severity for poisoned TLP reception.
11:5	Reserved
4	**Data Link Protocol Error Severity (DLPE)** – R/W. Severity for data link protocol errors.
3:1	Reserved
0	**Training Error Severity (TE)** – R/W. Severity for training errors.

12.1.16 CES – Correctable Error Status Register

Offset Address: 0090–0093h Attribute: R/WC
Default Value: 00000000h Size: 32-bit

Bit	Description
31:13	Reserved
12	**Replay Timer Timeout Status (RTT)** – R/WC. Indicates the replay timer timed out.
11:9	Reserved.
8	**Replay Number Rollover Status (RNR)** – R/WC. Indicates the replay number rolled over.
7	**Bad DLLP Status (BD)** – R/WC. Indicates a bad DLLP was received.
6	**Bad TLP Status (BT)** – R/WC. Indicates a bad TLP was received.
5:1	Reserved.
0	**Receiver Error Status (RE)** – R/WC. Indicates a receiver error occurred.

12.1.17 CEM – Correctable Error Mask Register

Offset Address: 0094–0097h Attribute: R/WO
Default Value: 00000000h Size: 32-bit

When set, the corresponding error in the CES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled.

Bit	Description
31:13	Reserved
12	**Replay Timer Timeout Mask (RTT)** – R/WO. Mask for replay timer timeout.
11:9	Reserved.

Bit	Description
8	**Replay Number Rollover Mask (RNR)** – R/WO. Mask for replay number rollover.
7	**Bad DLLP Mask (BD)** – R/WO. Mask for bad DLLP reception.
6	**Bad TLP Mask (BT)** – R/WO. Mask for bad TLP reception.
5:1	Reserved.
0	**Receiver Error Mask (RE)** – R/WO. Mask for receiver errors.

12.1.18 AECC – Advanced Error Capabilities and Control Register

Offset Address: 0098–009Bh Attribute: RO
Default Value: 00000000h Size: 32-bit

Bit	Description
31:9	Reserved
8	ECRC Check Enable (ECE) – RO. ECRC is not supported.
7	ECRC Check Capable (ECC) – RO. ECRC is not supported.
6	ECRC Generation Enable (EGE) – RO. ECRC is not supported.
5	ECRC Generation Capable (EGC) – RO. ECRC is not supported.
4:0	First Error Pointer (FEP) – RO.

12.1.19 RES – Root Error Status Register

Offset Address: 00B0–00B3h Attribute: R/WC, RO
Default Value: 00000000h Size: 32-bit

The Intel® 631xESB/632xESB I/O Controller Hub allows only one error to be captured.

Bit	Description
31:27	Advanced Error Interrupt Message Number (AEMN) – RO. There is only one error interrupt allocated.
26:4	Reserved.
3	Multiple ERR_FATAL/NONFATAL Received (MENR) – RO. This is not supported.
2	**ERR_FATAL/NONFATAL Received (ENR)** – R/WC. Set when either a fatal or a non-fatal error message is received or an internal fatal error is detected (all internal uncorrectable errors are fatal).
1	Multiple ERR_COR Received (MCR) – RO. This is not supported.
0	**ERR_COR Received (CR)** – R/WC. Set when a correctable error message is received or an internal correctable error is detected.

12.1.20 ESID – Error Source Identification Register

Offset Address: 00B4–00B7h Attribute: RO
Default Value: 00000000h Size: 32-bit

Bit	Description
31:16	**ERR_FATAL/NONFATAL Source Identification (ENSID)** – RO. Loaded with the requester ID indicated in the received ERR_FATAL or ERR_NONFATAL message when RES.ENR (offset 00B0h, bit 2) is first set, or the internal requestor ID if an internally detected error.
15:0	**ERR_COR Source Identification (CSID)** – RO. Loaded with the requester ID indicated in the received ERR_COR message when RES.CR (offset 00B0h, bit 0) is first set, or the internal requester ID if an internally detected error.

12.1.21 RCTCL – Root Complex Topology Capabilities List Register

Offset Address: 0100–0103h Attribute: RO
Default Value: 1A010005h Size: 32-bit

Bit	Description
31:20	**Next Capability (NEXT)** – RO. Indicates the next item in the list.
19:16	**Capability Version (CV)** – RO. Indicates the version of the capability structure.
15:0	**Capability ID (CID)** – RO. Indicates this is a PCI Express link capability section of an RCRB.

12.1.22 ESD – Element Self Description Register

Offset Address: 0104–0107h Attribute: R/WO, RO
Default Value: 00000502h Size: 32-bit

Bit	Description
31:24	**Port Number (PN)** – RO. A value of 0 to indicate the egress port for the Intel® 631xESB/ 632xESB I/O Controller Hub.
23:16	**Component ID (CID)** – R/WO. Indicates the component ID assigned to this element by software. This is written once by platform BIOS and is locked until a platform reset.
15:8	**Number of Link Entries (NLE)** – RO. Indicates that one link entry (corresponding to ESI) and 4 root port entries (for the downstream port) is described by this RCRB.
7:4	Reserved
3:0	**Element Type (ET)** – RO. Indicates that the element type is a root complex internal link.

12.1.23 ULD – Upstream Link Descriptor Register

Offset Address: 0110–0113h Attribute: R/WO, RO
Default Value: 00000001h Size: 32-bit

Bit	Description
31:24	**Target Port Number (PN)** – R/WO. This field is programmed by platform BIOS to match the port number of the MCH RCRB that is attached to this RCRB.
23:16	**Target Component ID (TCID)** – R/WO. This field is programmed by platform BIOS to match the component ID of the MCH RCRB that is attached to this RCRB.
15:2	Reserved
1	**Link Type (LT)** – RO. Indicates that the link points to the MCH RCRB.
0	**Link Valid (LV)** – RO. Indicates that the link entry is valid.

12.1.24 ULBA – Upstream Link Base Address Register

Offset Address: 0114–011Bh Attribute: R/WO
Default Value: 0000000000000000h Size: 64-bit

Bit	Description
63:32	**Base Address Upper (BAU)** – R/WO. This field is programmed by platform BIOS to match the upper 32-bits of base address of the MCH RCRB that is attached to this RCRB.
31:0	**Base Address Lower (BAL)** – R/WO. This field is programmed by platform BIOS to match the lower 32-bits of base address of the MCH RCRB that is attached to this RCRB.

12.1.25 RP0D – Root Port 0 Descriptor Register

Offset Address: 0120–0123h Attribute: R/WO, RO
Default Value: 01xx0002h Size: 32-bit

Bit	Description
31:24	**Target Port Number (PN)** – RO. Indicates the target port number is 1h (root port #0).
23:16	**Target Component ID (TCID)** – R/WO. This field returns the value of the ESD.CID (offset 0104h, bits 23:16) field programmed by platform BIOS, since the root port is in the same component as the RCRB.
15:2	Reserved
1	**Link Type (LT)** – RO. Indicates that the link points to a root port.
0	**Link Valid (LV)** – RO. When FD.PE1D (offset 3418h, bit 16) is set, this link is not valid (returns 0). When FD.PE1D is cleared, this link is valid (returns 1).

12.1.26 RP0BA – Root Port 0 Base Address Register

Offset Address: 0128–012Fh Attribute: RO
Default Value: 00000000000E0000h Size: 64-bit

Bit	Description
63:32	Reserved
31:28	Reserved
27:20	**Bus Number (BN)** – RO. Indicates the root port is on bus #0.
19:15	**Device Number (DN)** – RO. Indicates the root port is on device #28.
14:12	**Function Number (FN)** – RO. Indicates the root port is on function #0.
11:0	Reserved

12.1.27 RP1D – Root Port 1 Descriptor Register

Offset Address: 0130–0133h Attribute: R/WO, RO
Default Value: 02xx0002h Size: 32-bit

Bit	Description
31:24	**Target Port Number (PN)** – RO. Indicates the target port number is 2h (root port #1).
23:16	**Target Component ID (TCID)** – R/WO. This field returns the value of the ESD.CID (offset 0104h, bits 23:16) field programmed by platform BIOS, since the root port is in the same component as the RCRB.
15:2	Reserved
1	**Link Type (LT)** – RO. Indicates that the link points to a root port.
0	**Link Valid (LV)** – RO. When RPC.PC (offset 0224h, bits 1:0) is ‘01’, ‘10’, or ‘11’, or FD.PE2D (offset 3418h, bit 17) is set, the link for this root port is not valid (return 0). When RPC.PC is ‘00’ and FD.PE2D is cleared, the link for this root port is valid (return 1).

12.1.28 RP1BA – Root Port 1 Base Address Register

Offset Address: 0138–013Fh Attribute: RO
Default Value: 00000000000E1000h Size: 64-bit

Bit	Description
63:32	Reserved
31:28	Reserved
27:20	**Bus Number (BN)** – RO. Indicates the root port is on bus #0.
19:15	**Device Number (DN)** – RO. Indicates the root port is on device #28.
14:12	**Function Number (FN)** – RO. Indicates the root port is on function #1.
11:0	Reserved

12.1.29 RP2D – Root Port 2 Descriptor Register

Offset Address: 0140–0143h Attribute: R/WO, RO
Default Value: 03xx0002h Size: 32-bit

Bit	Description
31:24	**Target Port Number (PN)** – RO. Indicates the target port number is 3h (root port #2).
23:16	**Target Component ID (TCID)** – R/WO. This field returns the value of the ESD.CID (offset 0104h, bits 23:16) field programmed by platform BIOS, since the root port is in the same component as the RCRB.
15:2	Reserved
1	**Link Type (LT)** – RO. Indicates that the link points to a root port.
0	**Link Valid (LV)** – RO. When RPC.PC (offset 0224h, bits 1:0) is '11', or FD.PE3D (offset 3418h, bit 18) is set, the link for this root port is not valid (return 0). When RPC.PC is '00', '01', or "10', and FD.PE3D is cleared, the link for this root port is valid (return 1).

12.1.30 RP2BA – Root Port 2 Base Address Register

Offset Address: 0148–014Fh Attribute: RO
Default Value: 00000000000E2000h Size: 64-bit

Bit	Description
63:32	Reserved
31:28	Reserved
27:20	**Bus Number (BN)** – RO. Indicates the root port is on bus #0.
19:15	**Device Number (DN)** – RO. Indicates the root port is on device #28.
14:12	**Function Number (FN)** – RO. Indicates the root port is on function #2.
11:0	Reserved

12.1.31 RP3D – Root Port 3 Descriptor Register

Offset Address: 0150–0153h Attribute: R/WO, RO
Default Value: 04xx0002h Size: 32-bit

Bit	Description
31:24	**Target Port Number (PN)** – RO. Indicates the target port number is 4h (root port #3).
23:16	**Target Component ID (TCID)** – R/WO. This field returns the value of the ESD.CID (offset 0104h, bits 23:16) field programmed by platform BIOS, since the root port is in the same component as the RCRB.
15:2	Reserved
1	**Link Type (LT)** – RO. Indicates that the link points to a root port.
0	**Link Valid (LV)** – RO. When RPC.PC (offset 0224h, bits 1:0) is '10' or '11', or FD.PE4D (offset 3418h, bit 19) is set, the link for this root port is not valid (return 0). When RPC.PC is '00' or '01' and FD.PE4D is cleared, the link for this root port is valid (return 1).

12.1.32 RP3BA – Root Port 3 Base Address Register

Offset Address: 0158–015Fh Attribute: RO
Default Value: 00000000000E3000h Size: 64-bit

Bit	Description
63:32	Reserved
31:28	Reserved
27:20	**Bus Number (BN)** – RO. Indicates the root port is on bus #0.
19:15	**Device Number (DN)** – RO. Indicates the root port is on device #28.
14:12	**Function Number (FN)** – RO. Indicates the root port is on function #3.
11:0	Reserved

12.1.33 AZD – High Definition Audio Descriptor Register

Offset Address: 0160–0163h Attribute: R/WO, RO
Default Value: 05xx0002h Size: 32-bit

Bit	Description
31:24	**Target Port Number (PN)** – RO. Indicates the target port number is 5h (Intel High Definition Audio).
23:16	**Target Component ID (TCID)** – R/WO. This field returns the value of the ESD.CID (offset 0104h, bits 23:16) field programmed by platform BIOS, since the root port is in the same component as the RCRB.
15:2	Reserved
1	**Link Type (LT)** – RO. Indicates that the link points to a root port.
0	**Link Valid (LV)** – RO. When FD.ZD (offset 3418h, bit 4) is set, the link to Intel High Definition Audio is not valid (return 0). When FD.ZD is cleared, the link to Intel High Definition Audio is valid (return 1).

12.1.34 AZBA – High Definition Audio Base Address Register

Offset Address: 0168–016Fh Attribute: RO
Default Value: 00000000000D8000h Size: 64-bit

Bit	Description
63:32	Reserved
31:28	Reserved
27:20	**Bus Number (BN)** – RO. Indicates the root port is on bus #0.
19:15	**Device Number (DN)** – RO. Indicates the root port is on device #27.
14:12	**Function Number (FN)** – RO. Indicates the root port is on function #0.
11:0	Reserved

12.1.35 ILCL – Internal Link Capabilities List Register

Offset Address: 01A0–01A3h Attribute: RO
Default Value: 00010006h Size: 32-bit

Bit	Description
31:20	**Next Capability Offset (NEXT)** – RO. Indicates this is the last item in the list.
19:16	**Capability Version (CV)** – RO. Indicates the version of the capability structure.
15:0	**Capability ID (CID)** – RO. Indicates this is capability for ESI.

12.1.36 LCAP – Link Capabilities Register

Offset Address: 01A4–01A7h Attribute: R/W, RO
Default Value: 00012441h Size: 32-bit

Bit	Description
31:18	Reserved
17:15	**L1 Exit Latency (EL1)** – RO. Indicates that the exit latency is 2 µs to less than 4 µs.
14:12	**L0s Exit Latency (EL0)** – R/W. This field is updateable by BIOS. It defaults to 128 ns to less than 256 ns, assuming a common-clock configuration between MCH and Intel® 631xESB/ 632xESB I/O Controller Hub. If a unique clock value is used, it is recommended that BIOS update this field to 100b (512 ns to less than 1 µs).
11:10	Active State Link PM Support (APMS) – R/O. Indicates what level of active state link power management is supported on the ESI port. BitsDefinition 00 Neither L0s nor L1 are supported 01 L0s Entry Supported 10 Reserved, L1is not supported on ESI 11 Reserved, L1is not supported on ESI
9:4	**Maximum Link Width (MLW)** – RO. Indicates the maximum link width is 4 ports.
3:0	**Maximum Link Speed (MLS)** – RO. Indicates the link speed is 2.5 Gb/s.

12.1.37 LCTL – Link Control Register

Offset Address: 01A8–01A9h
Default Value: 0000h
Attribute: R/W
Size: 16-bit

Bit	Description
15:8	Reserved
7	**Extended Synch (ES)** – R/W. When set, forces extended transmission of FTS ordered sets when exiting L0s prior to entering L0 and extra TS1 sequences at exit from L1 prior to entering L0.
6:2	Reserved
1:0	**Active State Link PM Control (APMC)** – R/W. Indicates whether ESI should enter L0s or L1 or both. 00 = Disabled 01 = L0s entry supported 10 = Reserved 11 = L0s and L1 entry supported.

12.1.38 LSTS – Link Status Register

Offset Address: 01AA–01ABh
Default Value: 0041h
Attribute: RO
Size: 16-bit

Bit	Description
15:10	Reserved
9:4	**Negotiated Link Width (NLW)** – RO. Minimum negotiated link width is a x4 port.
3:0	**Link Speed (LS)** – RO. Link is 2.5 Gb/s.

12.1.39 VPCAP – Private Virtual Channel Resource Capability Register

Offset Address: 01F0–01F3h
Default Value: 00000001h
Attribute: RO
Size: 32-bit

Bit	Description
31:24	**Port Arbitration Table Offset (AT)** – RO. This VC implements no port arbitration table since the arbitration is fixed.
23	Reserved
22:16	**Maximum Time Slots (MTS)** – RO. This VC implements fixed arbitration, and therefore this field is not used.
15	**Reject Snoop Transactions (RTS)** – RO. This VC must be able to take snoopable transactions.
14	**Advanced Packet Switching (APS)** – RO. This VC is capable of all transactions, not just advanced packet switching transactions.
13:8	Reserved
7:0	**Port Arbitration Capability (PAC)** – RO. Indicates that this VC uses fixed port arbitration.

12.1.40 VPCTL – Private Virtual Channel Resource Control Register

Offset Address: 01F4–01F7h Attribute: R/W, RO
Default Value: 00000000h Size: 32-bit

Bit	Description
31	**Virtual Channel Enable (EN)** – R/W. Enables the VC when set. Disables the VC when cleared.
30:27	Reserved
26:24	**Virtual Channel Identifier (ID)** – R/W. Indicates the ID to use for this virtual channel.
19:17	**Port Arbitration Select (PAS)** – R/W. Indicates which port table is being programmed. The root complex takes no action on this setting since the arbitration is fixed and there is no arbitration table.
16	**Load Port Arbitration Table (LAT)** – RO. The root complex does not implement an arbitration table for this virtual channel.
15:8	Reserved
7:0	**Transaction Class / Virtual Channel Map (TVM)** – RO. Indicates which transaction classes are mapped to this virtual channel. When a bit is set, this transaction class is mapped to the virtual channel.

12.1.41 VPSTS – Private Virtual Channel Resource Status Register

Offset Address: 01FA–01FBh Attribute: RO
Default Value: 0000h Size: 16-bit

Bit	Description
15:02	Reserved
1	**VC Negotiation Pending (NP)** – RO. When set, indicates the virtual channel is still being negotiated with ingress ports.
0	**Port Arbitration Tables Status (ATS)** – RO. There is no port arbitration table for this VC, so this bit is reserved at 0.

12.1.42 VPR – Private Virtual Channel Routing Register

Offset Address: 01FC–01FFh Attribute: R/W
Default Value: 00000000h Size: 32-bit

Bit	Description
15:11	Reserved
10:8	**VCp Traffic Class (VPTC)** – R/W. When any of the below interfaces are enabled to use VCp, they must use this traffic class. When the interface is not enabled to use VCp, they must use TC0 as their traffic class. The one exception to this is Intel High Definition Audio, which may be enabled for VC1. In this case, the TC assigned to VC1 is used.
7:4	Reserved
3	High Definition Audio VCp Enable (ZPE) – R/W. 0 = The Intel High Definition Audio audio and modem controllers will use VC0, unless OS software enables Intel High Definition Audio to use VC1, in which case VC1 will be used. 1 = The Intel High Definition Audio audio and modem controllers will use VCp as its virtual channel, unless OS software enables Intel High Definition Audio to use VC1, in which case VC1 will be used.

Bit	Description
2	**AC'97 VCp Enable (APE)** – R/W. 0 = The AC'97 audio and modem controllers will use VC0. 1 = The AC'97 audio and modem controllers will use VCp as its virtual channel.
1	**EHCI VCp Enable (EPE)** – R/W. 0 = The EHCI controller will use VC0. 1 = The EHCI controller will use VCp as its virtual channel.
0	**UHCI VCp Enable (EPE)** – R/W. 0 = The UHCI controllers will use VC0. 1 = The UHCI controllers will use VCp as their virtual channel.

12.1.43 L3A – Level 3 Backbone Arbiter Configuration Register

Offset Address: 0200–0203h Attribute: R/W
Default Value: 01100220h Size: 32-bit

The bits in this register are 1's based; that is, a value of 1h means a count of 1, a count of 10h means a count of 16, and so on. BIOS should not program a value of 00h into these registers, as that will result in no grants for the particular type.

Bit	Description
31	**Grant Count Disable (GCD)** – R/W. 0 = Grant count enabled. 1 = Indicates that the grant counter for this arbiter level is disabled, and all grant counts for this level are treated as unlimited.
30	Reserved
29:24	**Peer Grant Count (PGC)** – R/W. Indicates the grant count to load on peer requests into the level 3 arbiter.
23:22	Reserved
21:16	**Private Virtual Channel Grant Count (VPGC)** – R/W. Indicates the grant count to load on VCp requests into the level 3 arbiter.
15:14	Reserved
13:8	**Virtual Channel 1 Grant Count (V1GC)** – R/W. Indicates the grant count to load on VC1 requests into the level 3 arbiter.
7:6	Reserved
5:0	**Virtual Channel 0 Grant Count (V0GC)** – R/W. Indicates the grant count to load on VC0 requests into the level 3 arbiter.

12.1.44 L2A – Level 2 Backbone Arbiter Configuration Register

Offset Address: 0208–020Bh Attribute: R/W
Default Value: 00000404h Size: 32-bit

The bits in this register are 1's based; that is, a value of 1h means a count of 1, a count of 10h means a count of 16, and so on. BIOS should not program a value of 00h into these registers, as that will result in no grants for the particular type.

Bit	Description
31	**Grant Count Disable (GCD)** – R/W. 0 = Grant count enabled. 1 = Indicates that the grant counter for this arbiter level is disabled, and all grant counts for this level are treated as unlimited.
30:14	Reserved
13:8	**Posted Grant Count (PGC)** – R/W. Indicates the grant count to load on peer requests into the level 2 arbiter.
7:6	Reserved
5:0	**Non-posted Grant Count (NGC)** – R/W. Indicates the grant count to load on non-posted requests into the level 2 arbiter.

12.1.45 L1A – Level 1 Backbone Arbiter Configuration Register

Offset Address: 020C–020Fh Attribute: R/W
Default Value: 00201004h Size: 32-bit

The bits in this register are 1's based; that is, a value of 1h means a count of 1, a count of 10h means a count of 16, and so on. BIOS should not program a value of 00h into these registers, as that will result in no grants for the particular type.

Bit	Description
31	**Grant Count Disable (GCD)** – R/W. 0 = Grant count enabled. 1 = Indicates that the grant counter for this arbiter level is disabled, and all grant counts for this level are treated as unlimited.
30:22	Reserved
21:16	**High Bandwidth Grant Count (HGC)** – R/W. Indicates the grant count to load on high bandwidth requests into the level 1 arbiter.
15:14	Reserved
13:8	**Medium Bandwidth Grant Count (MGC)** – R/W. Indicates the grant count to load on medium bandwidth requests into the level 1 arbiter.
7:6	Reserved
5:0	**Low Bandwidth Grant Count (MGC)** – R/W. Indicates the grant count to load on low bandwidth requests into the level 1 arbiter.

12.1.46 DA – Downstream Arbiter Configuration Register

Offset Address: 0210–0213h Attribute: R/W
Default Value: 0000F711h Size: 32-bit

The bits in this register are 1's based; that is, a value of 1h means a count of 1, a count of 10h means a count of 16, and so on. BIOS should not program a value of 00h into these registers, as that will result in no grants for the particular type.

Bit	Description
31	**Grant Count Disable (GCD)** – R/W. 0 = Grant count enabled. 1 = Indicates that the grant counter for this arbiter level is disabled, and all grant counts for this level are treated as unlimited.
30:16	Reserved
15:12	**VC1 Completion Grant Counter (V1GC)** – R/W. Specifies the default value for downstream VC1 completion grant count.
11:8	**Private VC Completion Grant Count (VPGC)** – R/W. Specifies the default value for downstream VCp completion grant count.
7:4	**VC0 Completion / Peer Posted Grant Count (V0PGC)** – R/W. Specifies the default value for VC0 completions and peer posted requests.
3:0	**Missing Completion Grant Count (MCGC)** – R/W. Specifies the default value for missing completion grant count.

12.1.47 UNRL – Upstream Non-posted Request Limits Register

Offset Address: 0214–0217h Attribute: R/W
Default Value: 100E0E8Eh Size: 32-bit

The bits in this register are 1's based; that is, a value of 1h means a count of 1, a count of 10h means a count of 16, and so on. BIOS should not program a value of 00h into these registers, as that will result in no grants for the particular type.

Bit	Description
31:29	Reserved
28:24	**Total Non-posted Upstream Request Limit (T)** – R/W. Request limit for the total count of non-posted upstream requests. This value must be programmed to be greater than the sum of the minimum reserved fields. This register has no meaning if the V0D, V1D, and VPD bits are set.
23	**VCp Upstream Request Limit Disable (VPD)** – R/W. 0 = Enabled. 1 = The VP bit in this register and UMR.VP (offset 0218h, bits 20:16) will be disregarded, and there will be no limit to the number of outstanding VC0 upstream non-posted requests. Completion timeouts and unexpected completions will not be generated.
22	**VCp Non-Posted Data Required (VPDR)** – R/W. 0 = Non-posted data free is not required for this VC. 1 = Indicates that a maximum data length (128 bytes) is required in the upstream data buffer for the arbiter to grant an upstream non-posted request for this VC.
21	Reserved
20:16	**Private Virtual Channel Non-posted Upstream Request Limit (VP)** – R/W. Request limit for VCp non-posted upstream requests. This field has no meaning if VPD in this register is set.
15	**VC1 Upstream Request Limit Disable (V1D)** – R/W. 0 = Enabled. 1 = The V1 bit in this register and UMR.V1 (offset 0218h, bits 12:8) will be disregarded, and there will be no limit to the number of outstanding VC0 upstream non-posted requests. Completion timeouts and unexpected completions will not be generated.
14	**VC1 Non-Posted Data Required (V1DR)** – R/W. 0 = Non-posted data free is not required for this VC. 1 = Indicates that a maximum data length (128 bytes) is required in the upstream data buffer for the arbiter to grant an upstream non-posted request for this VC.
13	Reserved
12:8	**Virtual Channel 1 Non-posted Upstream Request Limit (V1)** – R/W. Request limit for VC1 upstream non-posted requests. This field has no meaning if V1D in this register is set.

Bit	Description
7	**VC0 Upstream Request Limit Disable (V0D)** – R/W. 0 = Enabled. 1 = The V0 bit in this register and UMR.V0 (offset 0218h, bits 4:0) will be disregarded, and there will be no limit to the number of outstanding VC0 upstream non-posted requests. Completion timeouts and unexpected completions will not be generated.
6	**VC0 Non-Posted Data Required (V0DR)** – R/W. 0 = The upstream arbiter will not look at these conditions when granting a non-posted request for this VC. 1 = Indicates that a maximum data length (128 bytes) is required in the upstream data buffer and at least 1 non-posted data credit for this VC is required for the upstream arbiter to grant an non-posted request for this VC.
5	Reserved
4:0	**Virtual Channel 0 Non-posted Upstream Request Limit (V0)** – R/W. Request limit for VC0 upstream non-posted requests. This field has no meaning if V0D in this register is set.

12.1.48 UMR – Upstream Minimum Reserved Register

Offset Address: 0218–021Bh Attribute: R/W
Default Value: 00010101h Size: 32-bit

The bits in this register are 1's based; that is, a value of 1h means a count of 1, a count of 10h means a count of 16, and so on. BIOS should not program a value of 00h into these registers, as that will result in no grants for the particular type.

Bit	Description
31:21	Reserved
20:16	**Private Virtual Channel Minimum Reserved (VP)** – R/W. Indicates the minimum number of slots in the sideways queue reserved for VCp non-posted upstream requests. This value must be less than UNRL.VP (offset 0214h, bits 20;16), and the sum of the VP, V1 and V0 fields in this register must be less than UNRL.T (offset 0214h, bits 28;24). This field has no meaning if UNRL.VPD (offset 0214h, bit 23) is set.
15:13	Reserved
12:8	**Virtual Channel 1 Minimum Reserved (V1)** – R/W. Indicates the minimum number of slots in the sideways queue reserved for VC1 non-posted upstream requests. This value must be less than UNRL.V1 (offset 0214h, bits 12;8), and the sum of the VP, V1 and V0 fields in this register must be less than UNRL.T (offset 0214h, bits 28;24). This field has no meaning if UNRL.V1D (offset 0214h, bit 15) is set.
7:5	Reserved
4:0	**Virtual Channel 0 Minimum Reserved (V0)** – R/W. Indicates the minimum number of slots in the sideways queue reserved for VC0 non-posted upstream requests. This value must be less than UNRL.V0 (offset 0214h, bits 4;0), and the sum of the VP, V1 and V0 fields in this register must be less than UNRL.T (offset 0214h, bits 28;24). This field has no meaning if UNRL.V0D (offset 0214h, bit 7) is set.

12.1.49 QL – Queue Limits Register

Offset Address: 021C–021Fh Attribute: R/W
Default Value: 00000000h Size: 32-bit

Bit	Description
31:4	Reserved
3	**Upstream Command Queue Size Limit Enable (UCQLE)** – R/W. Indicates the value of the UCQL field is valid.
2:0	**Upstream Command Queue Size Limit (UCQL)** – R/W. 0's based value which limits the number of upstream requests in the command queue. This is only valid if UCQLE is set in this register.

12.1.50 GBC – Generic Backbone Configuration Register

Offset Address: 0220–0223h
Default Value: 00000000h
Attribute: R/W
Size: 32-bit

Bit	Description
31	Reserved
30:28	**Upstream Arbiter Back-2-Back Delay (UAD)** – R/W. Indicates the number of backbone clocks injected into the upstream arbiter before the next evaluation phase. A value of 0 means no delay is added.
27	Reserved
26:24	**Downstream Arbiter Back-2-Back Delay (DAD)** – R/W. Indicates the number of backbone clocks injected into the downstream arbiter before the next evaluation phase. A value of 0 means no delay is added.
23	**Transaction Layer Packet Fast Transmit Mode (TLPF)** – R/W. 0 = Disabled. 1 = The backbone will transmit the packet header in the upstream command queue without waiting for the corresponding data to be available.
22:20	Reserved
19:16	**Flow Control Update Policy (FCP)** – R/W. Indicates how long a flow control update should wait for transmit in the presence of TLPs to transmit. When the link is idle, a flow control update will occur immediately when it becomes available. Additionally, if a 2nd update becomes available, the flow control update will occur next, regardless of the clock count. Encodings are: 101 = Wait 128-160 link clocks before sending the update 100 = Wait 96-128 link clocks before sending the update 011 = Wait 64-96 link clocks before sending the update 010 = Wait 32-64 link clocks before sending the update. 000 = Never wait – send flow control update immediately All values other than the ones specified will alias to “000”.
15:8	Reserved
7	**Completer Timeout Disable (CTD)** – R/W. 0 = Enabled. 1 = Disables the timeout mechanism for transactions. The backbone downstream will not timeout any completion nor generate any completer abort messages.
6	**Credit Allocated Update Mode (CAM)** – R/W. 0 = The credit update will not occur until the last data phase of the transaction. 1 = The credit update to the backbone upstream arbiter will occur on the clock the cycle is accepted on the backbone, ahead of the data transfer.
5	**Virtual Channel 1 Optimized (V1O)** – R/W. 0 = Disabled. 1 = One slot is reserved for VC1 traffic when VC1 is enabled. VC0 and VCP traffic will only be granted if there are 2 free entries in the upstream queue.

Bit	Description
4	Reserved
3:2	**Lock Non-snoop Request Enable (NREL)** – R/W. Indicates the policy of the upstream arbiter in the presence of non-snoop requests when the CPU is locked and the arbiter is considered disabled. Encodings are: 11 = Allow all non-snoop requests to continue upstream 10 = Allow VC1 and VCP non-snoop requests to continue upstream 01 = Allow VC1 non-snoop requests to continue upstream 00 = Do not allow any non-snoop requests to continue upstream (default)
1:0	**C3 Non-snoop Request Enable (NRE3)** – R/W. Indicates the policy of the upstream arbiter in the presence of non-snoop requests when the CPU is in a C3 state and the arbiter is considered disabled by the operating system. Encodings are: 11 = Allow all non-snoop requests to continue upstream 10 = Allow VC1 and VCP non-snoop requests to continue upstream 01 = Allow VC1 non-snoop requests to continue upstream 00 = Do not allow any non-snoop requests to continue upstream (default)

12.1.51 RPC – Root Port Configuration Register

Offset Address: 0224–0227h Attribute: R/W
Default Value: 00000000h Size: 32-bit

Bit	Description
31:8	Reserved
7	**High Priority Port Enable (HPE)** – R/W. 0 = The high priority path is not enabled. 1 = The port selected by the HPP field in this register is enabled for high priority. It will be arbitrated just below any VCp devices, and above all other VC0 (including integrated VC0) devices.
6	Reserved
5:4	**High Priority Port (HPP)** – R/W. This controls which port is enabled for high priority when the HPE bit in this register is set. 11 = Port 3 10 = Port 2 01 = Port 1 00 = Port 0
3:2	Reserved
1:0	**Port Configuration (PC)** – R/W. This controls how the PCI bridges are organized in various modes of operation. For the following mappings, if a port is not shown, it is considered a x1 port with no connection. 11 = 1 x4, Port 0 (x4) 10 = Reserved 01 = Reserved 00 = 4 x1s, Port 0 (x1), Port 1 (x1), Port 2 (x1), Port 3 (x1) These bits live in the resume well and are only reset by RSMRST#.

12.1.52 BAC – Bandwidth Allocation Configuration Register

Offset Address: 0228–022Bh Attribute: R/W
Default Value: 141200AAh Size: 32-bit

The devices listed below will use as their bandwidth the value located in these register fields. The encoding is as follows:

00 = Low Bandwidth (less than 50 MB/s)
01 = Medium Bandwidth (50 MB/s to 200 MB/s)
10 = High Bandwidth (>200 MB/s)
11 = Reserved

Bit	Description
31:30	**AC97 Bandwidth (A97B)** – R/W. Default is the AC'97 controller is of low bandwidth.
29:28	**PATA Bandwidth (PAB)** – R/W. Default is the PATA controller is of medium bandwidth.
27:26	**PCI Bridge Bandwidth (P2PB)** – R/W. Default is the PCI bridge is of medium bandwidth.
25:24	**USB 1.1 Bandwidth (U1B)** – R/W. Default is the USB 1.1 (UHCI) controllers are of low bandwidth.
23:22	**Legacy Device Bandwidth (LDB)** – R/W. Default is the legacy devices are of low bandwidth.
21:20	**USB2 Bandwidth (U2B)** – R/W. Default is the USB2 (EHCI) controller is of medium bandwidth.
19:18	High Definition Audio Bandwidth (AZB) – R/W. Default is the Intel High Definition Audio controller is of low bandwidth.
17:16	**SATA Bandwidth (SAB)** – R/W. Default is the SATA controller is of high bandwidth.
15:8	Reserved for future root ports.
7:6	**Root Port 3 Bandwidth (RP4B)** – R/W. Default is south port #3 is of high bandwidth.
5:4	**Root Port 2 Bandwidth (RP3B)** – R/W. Default is south port #2 is of high bandwidth.
3:2	**Root Port 1 Bandwidth (RP2B)** – R/W. Default is south port #1 is of high bandwidth.
1:0	**Root Port 0 Bandwidth (RP1B)** – R/W. Default is south port #0 is of high bandwidth.

12.1.53 AS – Arbiter Status Register

Offset Address: 022C–022Fh Attribute: R/WC
Default Value: 00000000h Size: 32-bit

Bit	Description
31:1	Reserved
0	**VC1 Grant Order Queue Overflow (V1G0)** – R/WC. 0 = The high priority path is not enabled. 1 = Indicates that the VC1 TWRR Grant Order Queue has overflowed and VC1 isochronous traffic bandwidth will not be guaranteed.

12.1.54 TRSR – Trap Status Register

Offset Address: 1E00–1E03h Attribute: R/WC, RO
Default Value: 00000000h Size: 32-bit

Bits	Description
31:4	Reserved.
3:0	**Cycle Trap SMI# Status (CTSS) –** R/WC. These bits are set by hardware when the corresponding Cycle Trap register is enabled and a matching cycle is received (and trapped). These bits are OR'd together to create a single status bit in the Power Management register space. Note that the SMI# and trapping must be enabled in order to set these bits. These bits are set before the completion is generated for the trapped cycle, thereby guaranteeing that the processor can enter the SMI# handler when the instruction completes. Each status bit is cleared by writing a 1 to the corresponding bit location in this register.

12.1.55 TRCR – Trapped Cycle Register

Offset Address: 1E10–1E17h Attribute: RO
Default Value: 0000000000000000h Size: 64-bit
This register saves information about the I/O Cycle that was trapped and generated the SMI# for software to read.

Bits	Description
63:25	Reserved.
24	**Read/Write# (RWI) –** RO. 0 = Trapped cycle was a write cycle. 1 = Trapped cycle was a read cycle.
23:20	Reserved.
19:16	**Active-high Byte Enables (AHBE) –** RO. This is the dword-aligned byte enables associated with the trapped cycle. A 1 in any bit location indicates that the corresponding byte is enabled in the cycle.
15:2	**Trapped I/O Address (TIOA) –** RO. This is the dword-aligned address of the trapped cycle.
1:0	Reserved.

12.1.56 TWDR – Trapped Write Data Register

Offset Address: 1E18–1E1Fh Attribute: RO
Default Value: 0000000000000000h Size: 64-bit
This register saves the data from I/O write cycles that are trapped for software to read.

Bits	Description
63:32	Reserved.
31:0	**Trapped I/O Data (TIOD) –** RO. Dword of I/O write data. This field is undefined after trapping a read cycle.

12.1.57 IOTRn – I/O Trap Register (0-3)

Offset Address: 1E80–1E87h Register 0 Attribute: R/W, RO
1E88–1E8Fh Register 1
1E90–1E97h Register 2
1E98–1E9Fh Register 3
Default Value: 0000000000000000h Size: 32-bit
These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Bits	Description
63:50	Reserved.
49	**Read/Write Mask (RWM) –** R/W. 0 = The cycle must match the type specified in bit 48. 1 = Trapping logic will operate on both read and write cycles.
48	**Read/Write# (RWIO) –** R/W. 0 = Write 1 = Read **NOTE:** The value in this field does not matter if bit 49 is set.
47:40	Reserved.
39:36	**Byte Enable Mask (BEM) –** R/W. A 1 in any bit position indicates that any value in the corresponding byte enable bit in a received cycle will be treated as a match. The corresponding bit in the Byte Enables field, below, is ignored.
35:32	**Byte Enables (TBE) –** R/W. Active-high dword-aligned byte enables.
31:24	Reserved.

Bits	Description
23:18	**Address[7:2] Mask (ADMA) –** R/W. A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the dword address, allowing for traps on address ranges up to 256 bytes in size.
17:16	Reserved.
15:2	**I/O Address[15:2] (IOAD) –** R/W. dword-aligned address
1	Reserved.
0	**Trap and SMI# Enable (TRSE) –** R/W. 0 = Trapping and SMI# logic disabled. 1 = The trapping logic specified in this register is enabled.

12.1.58 TCTL – TCO Configuration Register

Offset Address: 3000–3001h Attribute: R/W
Default Value: 00h Size: 8-bit

Bit	Description
7	**TCO IRQ Enable (IE)** – R/W. 0 = TCO IRQ is disabled. 1 = TCO IRQ is enabled, as selected by the TCO_IRQ_SEL field.
6:3	Reserved
2:0	**TCO IRQ Select (IS)** – R/W. Specifies on which IRQ the TCO will internally appear. If not using the APIC, the TCO interrupt must be routed to IRQ9-11, and that interrupt is not sharable with the SERIRQ stream, but is shareable with other PCI interrupts. If using the APIC, the TCO interrupt can also be mapped to IRQ20-23, and can be shared with other interrupt. 000 = IRQ 9 001 = IRQ 10 010 = IRQ 11 011 = Reserved 100 = IRQ 20 (only if APIC enabled) 101 = IRQ 21 (only if APIC enabled) 110 = IRQ 22 (only if APIC enabled) 111 = IRQ 23 (only if APIC enabled) When setting the these bits, the IE bit should be cleared to prevent glitching. When the interrupt is mapped to APIC interrupts 9, 10 or 11, the APIC should be programmed for active-high reception. When the interrupt is mapped to APIC interrupts 20 through 23, the APIC should be programmed for active-low reception.

12.1.59 D31IP – Device 31 Interrupt Pin Register

Offset Address: 3100–3103h Attribute: R/W, RO
Default Value: 00042210h Size: 32-bit

Bit	Description
31:16	Reserved
15:12	**SM Bus Pin (SMIP)** – R/W. Indicates which pin the SMBus controller drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# 3h = INTC# 4h = INTD# 5h-7h = Reserved
11:8	**SATA Pin (SIP)** – R/W. Indicates which pin the SATA controller drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# 3h = INTC# 4h = INTD# 5h-7h = Reserved
7:4	**PATA Pin (SMIP)** – R/W. Indicates which pin the PATA controller drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# 3h = INTC# 4h = INTD# 5h-7h = Reserved
3:0	**PCI Bridge Pin (PIP)** – RO. Currently, the PCI bridge does not generate an interrupt, so this field is read-only and 0.

12.1.60 D30IP – Device 30 Interrupt Pin Register

Offset Address: 3104–3107h Attribute: R/W, RO
Default Value: 00002100h Size: 32-bit

Bit	Description
31:16	Reserved
15:12	**AC '97 Modem Pin (AMIP)** – R/W. Indicates which pin the AC '97 Modem controller drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# 3h = INTC# 4h = INTD# 5h-7h = Reserved
11:8	**AC '97 Audio Pin (AAIP)** – R/W. Indicates which pin the AC '97 audio controller drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# 3h = INTC# 4h = INTD# 5h-7h = Reserved
7:4	Reserved
3:0	**LPC Bridge Pin (LIP)** – RO. Currently, the LPC bridge does not generate an interrupt, so this field is read-only and 0.

12.1.61 D29IP – Device 29 Interrupt Pin Register

Offset Address: 3108–310Bh
Default Value: 10004321h
Attribute: R/W
Size: 32-bit

Bit	Description
31:28	**EHCI Pin (EIP)** – R/W. Indicates which pin the EHCI controller drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# 3h = INTC# 4h = INTD# 5h-7h = Reserved
27:16	Reserved
15:12	**UHCI #3 Pin (U3P)** – R/W. Indicates which pin the UHCI controller #3 (ports 6 and 7) drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# 3h = INTC# 4h = INTD# 5h-7h = Reserved
11:8	**UHCI #2 Pin (U2P)** – R/W. Indicates which pin the UHCI controller #2 (ports 4 and 5) drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# 3h = INTC# 4h = INTD# 5h-7h = Reserved
7:4	**UHCI #1 Pin (U1P)** – R/W. Indicates which pin the UHCI controller #1 (ports 2 and 3) drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# 3h = INTC# 4h = INTD# 5h-7h = Reserved
3:0	**UHCI #0 Pin (U0P)** – R/W. Indicates which pin the UHCI controller #0 (ports 0 and 1) drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# 3h = INTC# 4h = INTD# 5h-7h = Reserved

12.1.62 D28IP – Device 28 Interrupt Pin Register

Offset Address: 310C–310Fh
Default Value: 00004321h
Attribute: R/W
Size: 32-bit

Bit	Description
31:16	Reserved
15:12	**PCI Express #4 Pin (P4IP)** – R/W. Indicates which pin the PCI Express port #3 drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# 3h = INTC# 4h = INTD# 5h-7h = Reserved
11:8	**PCI Express #3 Pin (P3IP)** – R/W. Indicates which pin the PCI Express port #2 drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# 3h = INTC# 4h = INTD# 5h-7h = Reserved
7:4	**PCI Express #2 Pin (P2IP)** – R/W. Indicates which pin the PCI Express port #1 drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# 3h = INTC# 4h = INTD# 5h-7h = Reserved
3:0	**PCI Express #1 Pin (P1IP)** – R/W. Indicates which pin the PCI Express port #0 drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# 3h = INTC# 4h = INTD# 5h-7h = Reserved

12.1.63 D27IP – Device 27 Interrupt Pin Register

Offset Address: 3110–3113h
Default Value: 00000001h
Attribute: R/W
Size: 32-bit

Bit	Description
31:4	Reserved
3:0	High Definition Audio Pin (ZIP) – R/W. Indicates which pin the Intel High Definition Audio controller drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# 3h = INTC# 4h = INTD# 5h-7h = Reserved

12.1.64 D31IR – Device 31 Interrupt Route Register

Offset Address: 3140–3141h
Default Value: 3210h
Attribute: R/W
Size: 16-bit

Bit	Description
15	Reserved
14:12	**Interrupt D Pin Route (IDR)** – R/W. Indicates which physical pin on the Intel® 631xESB/ 632xESB I/O Controller Hub is connected to the INTD# pin reported for device 31 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
11	Reserved
10:8	**Interrupt C Pin Route (ICR)** – R/W. Indicates which physical pin on the Intel® 631xESB/ 632xESB I/O Controller Hub is connected to the INTC# pin reported for device 31 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
7	Reserved
6:4	**Interrupt B Pin Route (ICR)** – R/W. Indicates which physical pin on the Intel® 631xESB/ 632xESB I/O Controller Hub is connected to the INTB# pin reported for device 31 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
3	Reserved
2:0	**Interrupt A Pin Route (ICR)** – R/W. Indicates which physical pin on the Intel® 631xESB/ 632xESB I/O Controller Hub is connected to the INTA# pin reported for device 31 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#

12.1.65 D30IR – Device 30 Interrupt Route Register

Offset Address: 3142–3143h
Default Value: 3210h
Attribute: R/W
Size: 16-bit

Bit	Description
15	Reserved
14:12	**Interrupt D Pin Route (IDR)** – R/W. Indicates which physical pin on the Intel® 631xESB/ 632xESB I/O Controller Hub is connected to the INTD# pin reported for device 30 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
11	Reserved
10:8	**Interrupt C Pin Route (ICR)** – R/W. Indicates which physical pin on the Intel® 631xESB/ 632xESB I/O Controller Hub is connected to the INTC# pin reported for device 30 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
7	Reserved
6:4	**Interrupt B Pin Route (ICR)** – R/W. Indicates which physical pin on the Intel® 631xESB/ 632xESB I/O Controller Hub is connected to the INTB# pin reported for device 30 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
3	Reserved
2:0	**Interrupt A Pin Route (ICR)** – R/W. Indicates which physical pin on the Intel® 631xESB/ 632xESB I/O Controller Hub is connected to the INTA# pin reported for device 30 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#

12.1.66 D29IR – Device 29 Interrupt Route Register

Offset Address: 3144–3145h
Default Value: 3210h
Attribute: R/W
Size: 16-bit

Bit	Description
15	Reserved
14:12	**Interrupt D Pin Route (IDR)** – R/W. Indicates which physical pin on the Intel® 631xESB/ 632xESB I/O Controller Hub is connected to the INTD# pin reported for device 29 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
11	Reserved
10:8	**Interrupt C Pin Route (ICR)** – R/W. Indicates which physical pin on the Intel® 631xESB/ 632xESB I/O Controller Hub is connected to the INTC# pin reported for device 29 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
7	Reserved
6:4	**Interrupt B Pin Route (ICR)** – R/W. Indicates which physical pin on the Intel® 631xESB/ 632xESB I/O Controller Hub is connected to the INTB# pin reported for device 29 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
3	Reserved
2:0	**Interrupt A Pin Route (ICR)** – R/W. Indicates which physical pin on the Intel® 631xESB/ 632xESB I/O Controller Hub is connected to the INTA# pin reported for device 29 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#

12.1.67 D28IR – Device 28 Interrupt Route Register

Offset Address: 3146–3147h
Default Value: 3210h
Attribute: R/W
Size: 16-bit

Bit	Description
15	Reserved
14:12	**Interrupt D Pin Route (IDR)** – R/W. Indicates which physical pin on the Intel® 631xESB/632xESB I/O Controller Hub is connected to the INTD# pin reported for device 28 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
11	Reserved
10:8	**Interrupt C Pin Route (ICR)** – R/W. Indicates which physical pin on the Intel® 631xESB/632xESB I/O Controller Hub is connected to the INTC# pin reported for device 28 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
7	Reserved
6:4	**Interrupt B Pin Route (ICR)** – R/W. Indicates which physical pin on the Intel® 631xESB/632xESB I/O Controller Hub is connected to the INTB# pin reported for device 28 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
3	Reserved
2:0	**Interrupt A Pin Route (ICR)** – R/W. Indicates which physical pin on the Intel® 631xESB/632xESB I/O Controller Hub is connected to the INTA# pin reported for device 28 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#

12.1.68 D27IR – Device 27 Interrupt Route Register

Offset Address: 3148–3149h
Default Value: 3210h
Attribute: R/W
Size: 16-bit

Bit	Description
15	Reserved
14:12	**Interrupt D Pin Route (IDR)** – R/W. Indicates which physical pin on the Intel® 631xESB/ 632xESB I/O Controller Hub is connected to the INTD# pin reported for device 27 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
11	Reserved
10:8	**Interrupt C Pin Route (ICR)** – R/W. Indicates which physical pin on the Intel® 631xESB/ 632xESB I/O Controller Hub is connected to the INTC# pin reported for device 27 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
7	Reserved
6:4	**Interrupt B Pin Route (ICR)** – R/W. Indicates which physical pin on the Intel® 631xESB/ 632xESB I/O Controller Hub is connected to the INTB# pin reported for device 27 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
3	Reserved
2:0	**Interrupt A Pin Route (ICR)** – R/W. Indicates which physical pin on the Intel® 631xESB/ 632xESB I/O Controller Hub is connected to the INTA# pin reported for device 27 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#

12.1.69 OIC – Other Interrupt Control Register

Offset Address: 31FF–31FFh
Default Value: 00h
Attribute: R/W
Size: 8-bit

Bit	Description
7:2	Reserved
1	**Coprocessor Error Enable (CEN)** – R/W. 0 = FERR# will not generate IRQ13 nor IGNNE#. 1 = If FERR# is low, IRQ13 generates internally and holds it until an I/O port F0h write. It will also drive IGNNE# active.
0	**APIC Enable (AEN)** – R/W. 0 = The internal IOxAPIC is disabled. 1 = Enables the internal IOxAPIC and its address decode.

12.1.70 RC – RTC Configuration Register

Offset Address: 3400–3403h
Default Value: 00000000h
Attribute: R/W R/WO
Size: 32-bit

Bit	Description
31:5	Reserved
4	**Upper 128 Byte Lock (UL)** – R/WO. 0 = Bytes not locked. 1 = Bytes 38h-3Fh in the upper 128 byte bank of RTC RAM are locked and cannot be accessed. Writes will be dropped and reads will not return any guaranteed data. Bit reset on system reset.
3	**Lower 128 Byte Lock (LL)** – R/WO. 0 = Bytes not locked. 1 = Bytes 38h-3Fh in the lower128 byte bank of RTC RAM are locked and cannot be accessed. Writes will be dropped and reads will not return any guaranteed data. Bit reset on system reset.
2	**Upper 128 Byte Enable (UE)** – R/W. 0 = Bytes locked. 1 = The upper 128 byte bank of RTC RAM can be accessed.
1:0	Reserved

12.1.71 HPTC – High Precision Timer Configuration Register

Offset Address: 3404–3407h
Default Value: 00000000h
Attribute: R/W
Size: 32-bit

Bit	Description
31:8	Reserved
7	**Address Enable (AE)** – R/W. 0 = Address disabled. 1 = Decode the High Precision Timer memory address range selected by bits 1:0 below.
6:2	Reserved
1:0	**Address Select (AS)** – R/W. This 2-bit field selects 1 of 4 possible memory address ranges for the High Precision Timer functionality. The encodings are: 00 = FED0_0000h - FED0_03FFh 01 = FED0_1000h - FED0_13FFh 10 = FED0_2000h - FED0_23FFh 11 = FED0_3000h - FED0_33FFh

12.1.72 GCS – General Control and Status Register

Offset Address: 3410–3413h Attribute:R/W, R/WO
Default Value: 0000000yh y=(00x0x000b) Size:32-bit

Bit	Description
31:24	Reserved
23:16	**BIST_DELAY_SEL** – R/W. This field determines the amount of time, measured in 125 MHz clocks, waits to deassert the INIT# signal after sending the CPU_RESET_DONE_ACK message. Notes 1. This field only has meaning if the BIST_EN bit (Bit 2 in the BUC register) is also set. 2. A value of 00h or 01h in this field is not permitted. 3. A1 clock variation permitted in the actual-time the INIT# signal goes inactive. 4. This field is in the core well. 5. This field is not reset by a CF9 reset with value 06h. Implementation choice: This register does not need to be reset by any reset.
15:10	Reserved
9	**Server Error Reporting Mode (SERM)** – R/W. 0 = the Intel® 631xESB/632xESB I/O Controller Hub is the final target of all errors. The MCH sends a messages to the Intel® 631xESB/632xESB I/O Controller Hub for the purpose of generating NMI. 1 = The MCH is the final target of all errors from PCI Express and ESI. In this mode, if a fatal, non-fatal, or correctable error on ESI or its downstream ports is detected, it sends a message to the MCH. If an ERR_* message is received from the downstream port, it sends that message to the MCH.
8	Reserved
7	Reserved
6	**FERR# MUX Enable (FME)** – R/W. This bit enables FERR# to be a CPU break event indication. 0 = Disabled. 1 = FERR# is examined during a C2, C3, or C4 state as a break event.
5	**No Reboot (NR)** – R/W. This bit is set when the “No Reboot” strap (SPKR pin on Intel® 631xESB/632xESB I/O Controller Hub) is sampled high on PWROK. This bit may be set or cleared by software if the strap is sampled low but may not override the strap when it indicates “No Reboot”. 0 = System will reboot upon the second timeout of the TCO timer. 1 = The TCO timer will count down and generate the SMI# on the first timeout, but will not reboot on the second timeout.
4	**Alternate Access Mode Enable (AME)** – R/W. 0 = Disabled. 1 = Alternate access read only registers can be written, and write only registers can be read. Before entering a low power state, several registers from powered down parts may need to be saved. In the majority of cases, this is not an issue, as registers have read and write paths. However, several of the ISA compatible registers are either read only or write only. To get data out of write-only registers, and to restore data into read-only registers, the Intel® 631xESB/632xESB I/O Controller Hub implements an alternate access mode.

Bit	Description
3	**Boot BIOS Destination (BBD)** – R/W. The default value of this bit is determined by a strap allowing systems with corrupted or unprogrammed flash to boot from a PCI device. The value of the strap can be overwritten by software. When this bit is 0, the PCI-to-PCI bridge Memory Space Enable bit does not need to be set (nor any other bits) in order for these cycles to go to PCI. Note that BIOS enable ranges and the other BIOS protection and update bits associated with the FWH interface have no effect when this bit is 0. 0 = The top 16MB of memory below 4GB (FF00_0000h to FFFF_FFFFh) is accepted by the primary side of the PCI P2P bridge and forwarded to the PCI bus. 1 = The top 16MB of memory below 4GB (FF00_0000h to FFFF_FFFFh) is not decoded to PCI and the LPC bridge claims these cycles based on the FWH Decode Enable bits.
2	**Reserved Page Route (RPR)** – R/W. Determines where to send the reserved page registers. These addresses are sent to PCI or LPC for the purpose of generating POST codes. The I/O addresses modified by this field are: 80h, 84h, 85h, 86h, 88h, 8Ch, 8Dh, and 8Eh. 0 = Writes will be forwarded to LPC, shadowed within the Intel® 631xESB/632xESB I/O Controller Hub, and reads will be returned from the internal shadow 1 = Writes will be forwarded to PCI, shadowed within the Intel® 631xESB/632xESB I/O Controller Hub, and reads will be returned from the internal shadow. Note, if some writes are done to LPC/PCI to these I/O ranges, and then this bit is flipped, such that writes will now go to the other interface, the reads will not return what was last written. Shadowing is performed on each interface. The aliases for these registers, at 90h, 94h, 95h, 96h, 98h, 9Ch, 9Dh, and 9Eh, are always decoded to LPC.
1	Reserved
0	**Top Swap Lock-Down (TSLD)** – R/WO. 0 = Disabled. 1 = Prevents BUC.TS (offset 3414, bit 0) from being changed. This bit can only be written from 0 to 1 once.

12.1.73 BUC – Backed Up Control Register

Offset Address: 3414–3414h Attribute: R/W
Default Value: 0000000xb Size: 8-bit

All bits in this register are in the RTC well and only cleared by RTCRST#

Bit	Description
7:3	Reserved
2	**CPU BIST Enable (CBE)** – R/W. This bit is in the resume well and is reset by RSMRST#, but not PLTRST# nor CF9h writes. 0 = Disabled. 1 = The INIT# signals will be driven active when CPURST# is active. INIT# and INIT3_3# will go inactive with the same timings as the other CPU I/F signals (hold time after CPURST# inactive).
1	Reserved.
0	**Top Swap (TS)** – R/W. 0 = Don't invert A16. 1 = Invert A16 for cycles going to the BIOS space (but not the feature space) in the FWH. If Intel® 631xESB/632xESB I/O Controller Hub is strapped for Top-Swap (GNT[6]# is low at rising edge of PWROK), then this bit cannot be cleared by software. The strap jumper should be removed and the system rebooted.

12.1.74 FD – Function Disable Register

Offset Address:	3418–341Bh	Attribute:	R/W, RO
Default Value:	See bit description	Size:	32-bit

The USB1 functions must be disabled from highest function number to lowest. For example, if only three USB1 host controllers are wanted, software must disable USB1 #4 (UD4 bit set). When disabling USB1 host controllers, the USB2 EHCI Structural Parameters Registers must be updated with coherent information in “Number of Companion Controllers” and “N_Ports” fields.

When disabling a function, only the configuration space is disabled. Software must ensure that all functionality within a controller that is not desired (such as memory spaces, I/O spaces, and DMA engines) is disabled prior to disabling the function.

Bit	Description
31:20	Reserved
19	PCI Express 4 Disable (PE4D) – R/W. Default is 0. When disabled, the link for this port is put into the “link down” state. 0 = PCI Express port #3 is enabled. 1 = PCI Express port #3 is disabled.
18	PCI Express 3 Disable (PE3D) – R/W. Default is 0. When disabled, the link for this port is put into the “link down” state. 0 = PCI Express port #2 is enabled. 1 = PCI Express port #2 is disabled.
17	PCI Express 2 Disable (PE2D) – R/W. Default is 0. When disabled, the link for this port is put into the “link down” state. 0 = PCI Express port #1 is enabled. 1 = PCI Express port #1 is disabled.
16	PCI Express 1 Disable (PE1D) – R/W. Default is 0. When disabled, the link for this port is put into the “link down” state. 0 = PCI Express port #0 is enabled. 1 = PCI Express port #0 is disabled.
15	USB2 Disable (U2D) – R/W. Default is 0. 0 = The USB2 Host Controller is enabled. 1 = The USB2 Host Controller is disabled.
14	LPC Bridge Disable (LBD) – R/W. Default is 0. 0 = The LPC bridge is enabled. 1 = The LPC bridge is disabled. Unlike the other disables in this register, the following additional spaces will no longer be decoded by the LPC bridge: • · Memory cycles below 16MB (1000000h) • · I/O cycles below 64kB (10000h) • · The Internal I/OxAPIC at FEC0_0000 to FECF_FFFF Memory cycles in the LPC BIOS range below 4GB will still be decoded when this bit is set, but the aliases at the top of 1MB (the E and F segment) no longer will be decoded.
13:12	Reserved
11	USB1 #4 Disable (U4D) – R/W. Default is 0. 0 = The 4th USB 1.1 controller (ports 6 and 7) is enabled. 1 = The 4th USB 1.1 controller (ports 6 and 7) is disabled.
10	USB1 #3 Disable (U3D) – R/W. Default is 0. 0 = The 3rd USB 1.1 controller (ports 4 and 5) is enabled. 1 = The 3rd USB 1.1 controller (ports 4 and 5) is disabled.
9	USB1 #2 Disable (U2D) – R/W. Default is 0. 0 = The 2nd USB 1.1 controller (ports 2 and 3) is enabled. 1 = The 2nd USB 1.1 controller (ports 2 and 3) is disabled.
8	USB1 #1 Disable (U1D) – R/W. Default is 0. 0 = The 1st USB 1.1 controller (ports 0 and 1) is enabled. 1 = The 1st USB 1.1 controller (ports 0 and 1) is disabled.

Bit	Description
7	Reserved
6	AC '97 Modem Disable (AMD) – R/W. Default is 0. 0 = The AC '97 modem function is enabled. 1 = The AC '97 modem function is disabled.
5	AC '97 Audio Disable (AAD) – R/W. Default is 0. 0 = The AC '97 audio function is enabled. 1 = The AC '97 audio function is disabled.
4	High Definition Audio Disable (ZD) – R/W. Default is 0. 0 = The High Definition Audio controller is enabled. 1 = The High Definition Audio controller is disabled and its PCI configuration space is not accessible.
3	SM Bus Disable (SD) – R/W. Default is 0. 0 = The SM Bus controller is enabled. 1 = The SM Bus controller is disabled. In ICH5 and previous, this also disabled the I/O space. In Intel® 631xESB/632xESB I/O Controller Hub, it disables only the configuration space.
2	Serial ATA Disable (SAD) – R/W. Default is 0. 0 = The SATA controller is enabled. 1 = The SATA controller is disabled.
1	Parallel ATA Disable (PAD) – R/W. Default is 0. 0 = The PATA controller is enabled. 1 = The PATA controller is disabled and its PCI configuration space is not accessible.
0	Reserved

12.1.75 CG – Clock Gating

Offset Address: 341C–341Fh Attribute: R/W, RO
Default Value: 00000000h Size: 32-bit

Bit	Description
31:01	Reserved
0	PCI Express root port Static Clock Gate Enable (PESCG) – R/W. 0 = Static Clock Gating is Disabled for the PCI Express Root Port. 1 = Static Clock Gating is Enabled for the PCI Express Root Port when the corresponding port is disabled in the Function Disable register (Chipset Config Registers:Offset 3418h) FD.PE1D, FD.PE2D, FD.PE3D or FD.PE4D. In addition to the PCI Express function disable register, the PCI Express root port physical layer static clock gating is also qualified by the Root Port Configuration RPC.PC (Chipset Config Registers:Offset 0224h:bits 1:0) as the physical layer may be required by an enabled port in a x2 or a x4 configuration.

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13 PCI Express* Bridge, Switch, and Endpoints Registers (Bm:D0:F0/F1/F3, Bp:D0:F0, Bp:D1:F0, Bp:D2:F0)

The Intel® 631xESB/632xESB I/O Controller Hub integrates PCI Express to PCI-X bridge that also contains registers for its Standard Hot-Plug Controller, I/OxAPIC controller, PCI Express switch which contains upstream and downstream ports, and one SMBus interface. This section describes these registers. A detailed bit description is also provided.

There are multiple functions can be seen from PCI Express—one I/OxAPIC function, one PCI bridge function, one upstream PCI Express switch function. All of the functions have the same device number of 0, but with different function numbers (refer to Figure 5-6 and Figure 5-14 for device diagram information).

13.1 PCI Configuration Registers

As Figure 5-6 shows, Intel® 631xESB/632xESB I/O Controller Hub couples on its 'south' interfaces to three individual x4 PCI Express links (one is the internal link for Intel® 631xESB/632xESB I/O Controller Hub LAN controller, the other two external links may be combined into a single x8 link by using a strapping pin during reset) and to one 64-bit PCI/PCI-X secondary bus interface.

The "north" PCI Express interface is the logical primary bus. The physical PCI-X bus segment becomes a separate secondary bus with a PCI Express to PCI-X bridge corresponding to Function 3. The upstream PCI Express port provides the link to another secondary PCI bus with a PCI Express switch model. The Standard Hot-Plug Controller (SHPC) associated with the PCI-X bus segment appears as a capability of the PCI Express to PCI-X bridge. The I/OxAPIC controller resides as a separate PCI function.

- **PCI Express Upstream port (Bm:D0:F0)**. Intel® 631xESB/632xESB I/O Controller Hub implements an upstream PCI Express port that provides the link to another secondary PCI bus with a PCI Express switch model.
- **PCI Express Downstream port (Bp:D0:F0, Bp:D1:F0, Bp:D2:F0).** Intel® 631xESB/632xESB I/O Controller Hub implements three downstream PCI Express ports that provide links to other secondary PCI buses with a PCI Express switch model.
- **I/OxAPIC Devices (Bm:D0:F1).** Intel® 631xESB/632xESB I/O Controller Hub implements a variation of the APIC known as the I/OxAPIC. It resides on the primary bus.
- **Standard Hot-Plug Controller(Bm:D0:F3).** Intel® 631xESB/632xESB I/O Controller Hub supports a single SHPC controller. This Standard Hot-Plug Controller appears as a capability of its associated PCI Express to PCI-X bridge.
- **PCI Express to PCI-X bridge (Bm:D0:F3).** Intel® 631xESB/632xESB I/O Controller Hub implements the buffering and control logic between the PCI Express and the PCI-X buses. The PCI bus arbitration is handled by these PCI devices. The

PCI decoder in this device must decode the ranges for PCI Express to the MCH. This register set also provides support for Reliability, Availability, and Serviceablity (RAS).

13.2 Memory-Mapped Registers

- **I/OxAPIC.** In addition to the PCI Configuration Registers mentioned above, the I/OxAPIC memory-mapped registers are located in the processor memory space located by the MBAR Register (PCI offset 10h) and ABAR Register (PCI offset 40h). MBAR and ABAR are located in the I/OxAPIC PCI Configuration space.
- **Standard Hot-Plug Controller.** In addition to the PCI Configuration Registers mentioned above, the Hot-Plug controller memory-mapped registers are located in the processor memory space located by the MBAR Register (PCI offset 10h). the "MBAR" is located in the PCI Express to PCI-X bridge PCI configuration space.

13.3 PCI Express* Switch, Upstream/Downstream Port Registers (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

The PCI Express upstream port configuration registers reside on Bus M, Device 0, Function 0, where Bus M is the bus attached to the upstream port. The configuration registers for the PCI Express downstream ports reside on PCI Express bus (Bus P), Device 0 Function 0, Device 1 Function 0, and Device 2 Function 0 (refer to Figure 5-6 and Figure 5-14 for more information).

13.3.1 Configuration Registers

Table 13-1 shows the PCI Express Switch configuration registers and their address byte offset values.

Note: Registers that are not shown should be treated as Reserved.

Table 13-1. Configuration Register Summary (Sheet 1 of 3)

Address Offset	Symbol	Register Name	Default	Access
00–01h	VID	Vendor ID Register	8086h	RO
02–03h	DID	Device ID Register	check register description	RO
04–05h	PCICMD	Command Register	0000h	RW, RO
06–07h	PCISTS	Status Register	0010h	RWC, RO
08h	RID	Revision ID Register	00h	RO
09–0Bh	CC	Class Code Register	060400h	RO
0Ch	CLS	Cache Line Size Register	00	RW
0Dh	PLT	Primary Latency Timer Register	00h	RW
0Eh	HTYPE	Header Type Register	80h (Upstream) 00 (Downstream)	RO
18-1Ah	BNUM	Bus Number Register	000000h	RW
1Bh	SLT	Secondary Latency Timer Register	00h	RW
1C-1Dh	IOBL	I/O Base and Limit Register	0000h	RW, RO
1E–1Fh	SECSTS	Secondary Status Register	0000h	RWC,RO

Table 13-1. Configuration Register Summary (Sheet 2 of 3)

Address Offset	Symbol	Register Name	Default	Access
20–21h	MB	Memory Base Register	0000h	RW
22-23h	ML	Memory Limit Register	0000h	RW
24–27h	PMBL	Prefetchable Memory Base and Limit Register	00010001h	RW, RO
28–2Bh	PB_UPPER	Prefetchable Base Upper 32 Bits Register	00000000h	RW
2C–2Fh	PL_UPPER	Prefetchable Limit Upper 32 Bits Register	00000000h	RW
34h	CAPP	Capabilities Pointer Register	44h	RO
3C-3Dh	INTR	Interrupt Information Register	0100h	RO
3E–3Fh	BCTRL	Bridge Control Register	0000h	RW, RWC, RO
40–41h	CNF	PCI Express Configuration Register	check register description	RW, RO
42-43h	EXP_CMMPC	PCI Express Compliance Measurement Mode Port Control	0000h	RWS
44h	EXP_CAPID	PCI Express Capability Identifier Register	10h	RO
45h	EXP_NXTP	PCI Express Next Item Pointer Register	70h (Upstream) 60 (Downstream)	RO
46–47h	EXP_CAP	PCI Express Capability Designator Register	51h (Upstream) 61 (Downstream)	RO
48–4B	EXP_DCAP	PCI Express Device Capabilities Register	0001h	RW, RO
4C–4D	EXP_DCTL	PCI Express Device Control Register	5020h	RW, RO
4E-4F	EXP_DSTS	PCI Express Device Status Register	0	RWC, RO
50-53h	EXP_LCAP	PCI Express Link Capabilities Register	0003F481h (Up) 0003F441 (Down)	RO
54-55h	EXP_LCTL	PCI Express Link Control Register	0040h	RW, RO
56–57h	EXP_LSTS	PCI Express Link Status Register	0000h	RO
58-5B	EXP_SCAP	PCI Express Slot Capabilities Register	00000000	RW,RO
5C-5Dh	EXP_SCTL	PCI Express Slot Control Register	03C0	RW, RO
5E-5Fh	EXP_SSTS	PCI Express Slot Status Register	0000	RWC,RO
60h	MSI_CAPID	PCI Express MSI Capability Identifier Register	00h (Upstream) 05 (Downstream)	RO
61h	MSI_NXTP	PCI Express MSI Next Pointer Register	70	RO
62h	MSI_MC	PCI Express MSI Message Control	80	RW,RO
64h	MSI_MA	PCI Express MSI Message Address	00	RW,RO
6C-6Dh	MSI_MD	PCI Express MSI Message Data	0000	RW
70h	EXPPM_CAPID	Power Management Capability Register	01h	RO
71h	EXPPM_NXTP	PCI Express Bridge Power Management Next Item Pointer	00	RO
72-73h	EXPPM_PMC	PCI Express Bridge Power Management Capabilities Register	C802h	RO
74h	EXPPM_PMCSR	Power Management Data Register	0000h	RO
76h	EXPPM_BSE	PCI Express Bridge Power Management Bridge Support Extensions	00h	RO

Table 13-1. Configuration Register Summary (Sheet 3 of 3)

Address Offset	Symbol	Register Name	Default	Access
77h	EXPPM_DATA	PCI Express Bridge Power Management Data field	00h	RO
FCh	EXP_PHC	PCI Express Port Hide Control	0003h	RWS
100-103h	ERR_CAPHDR	PCI Express Advanced Error Capability Identifier	30010001(Up) 00010001(Down)	RO
104-107h	ERRUNC_STS	PCI Express Uncorrectable Error Status Register	0000h	RWC
108-10Bh	ERRUNC_MSK	PCI Express Uncorrectable Error Mask Register	0000h	RWC
10C-10Fh	ERRUNC_SEV	PCI Express Uncorrectable Error Severity Register	00060010h	RWC
110-113h	ERRCOR_STS	PCI Express Correctable Error Status Register	0000h	RWC
114-117h	ERRCOR_MSK	PCI Express Correctable Error Mask Register	0000h	RWC
118-11Bh	ADVERR_CTL	Advanced Error Control and Capabilities Register	0000h	RWC
11C-12Bh	EXPHDRLOG	PCI Express HDR LOG Register	0000h	RWC
168h	RAS_STS	Miscellaneous Error Status Register	0000h	RO
170h	PEXH_STS	Intel® 631xESB/632xESB I/O Controller Hub PCI Express to PCI-X Bridge Strap Status Register	0000h	RO
172	PXB_STRAP	Intel® 631xESB/632xESB I/O Controller Hub PCI Express Upstream and Downstream Strap Status Register	00h	RO
190h	EVTCTRL	Event Logic Control	0h	RO

13.3.1.1 Offset 00h: VID—Vendor ID Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 00–01h
Default Value: 8086h
Attribute: RO
Size: 16 bits

Bits	Type	Reset	Description
15:00	RO	8086h	**Vendor ID (VID):** 16-bit vendor ID assigned to Intel VID=8086h.

13.3.1.2 Offset 02h: DID—Device ID Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 02–03h
Default Value: See Description (Function 0)
Attribute: RO
Size: 16 bits

Bits	Type	Reset	Description
15:0	RO	For Upstream Port: 3500h - 3503h depending on SKU. For Downstream Port 1 (device 0): 3510h - 3513h depending on SKU. For Downstream Port 2 (device 1): 3514h - 3517h depending on SKU. For Downstream Port 3 (device 2): 3518h - 351Bh depending on SKU.	**Device ID (DID):** Device number of the Intel® 631xESB/632xESB I/O Controller Hub upstream and downstream PCI Express functions.

13.3.1.3 Offset 04h: PCICMD—PCI Command Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 04–05h
Default Value: 0000h
Attribute: RW, RO
Size: 16 bits

Bits	Type	Reset	Description
15:11	RO	0	Reserved.
10	RW	0	**Interrupt Mask (INTMASK):** This bit disables the SHPC from asserting IRQ[23]#. This bit is valid only when the MSI is disabled; that is, the MSI enable bit (bit 0) in the MSC_MC register (offset 5Eh) is a zero. A value of 0 for this bit enables the assertion of its IRQ[23]# signal. A value of 1 disables the assertion of its IRQ[23]# signal. If IRQ[23]# is already asserted when this bit is set, it must be de-asserted.
9	RO	0	**Fast Back-to-Back Transactions Enable (FBTE):** This bit has no meaning on the PCI Express interface. It is hardwired to '0'.
8	RW	0	**SERR Enable (SEE):** Controls the enable for PCI-compatible SERR reporting on the PCI Express interface (along with the Status Register (STS REG, offset 06h, bit 14). 0 = Disable SERR reporting 1 = Enable SERR reporting Note that this bit does not affect the setting of the PCI Express error bits in the PCI Express Capability Structure.
7	RO	0	Wait Cycle Control (WCC): Reserved.
6	RW	0	**Parity Error Response (PER):** Controls the response to data parity errors forwarded from the PCI Express interface and peer PCI on read completions. 0 = Disable. Ignore errors on the PCI Express interface and the peer-PCI interface. 1 = Enable. Report read completion data parity errors on the PCI E interface and set the Master Data Parity Detected (MDPD) bit in the status register. Note that this bit does not affect the setting of the PCI Express error bits in the PCI Express Capability Structure.
5	RO	0	VGA Palette Snoop (VGA_PS): Reserved.
4	RO	0	**Memory Write and Invalidate (MWIE):** The Intel® 631xESB/632xESB I/O Controller Hub does not generate memory write and invalidate transactions, as the PCI Express interface does not have a corresponding transfer type.
3	RO	0	Special Cycle Enable (SCE): Reserved.
2	RW	0	**Bus Master Enable (BME):** Controls the ability to act as a master on PCI Express when forwarding memory transactions from PCI (memory, I/O, and configuration) or when generating MSI transaction on behalf of the SHPC. 0 = Disable. 1 = Enable. Note that this bit does not stop Intel® 631xESB/632xESB I/O Controller Hub from issuing completions on PCI Express. Software must guarantee that when this bit is set, all inbound posted transactions are flushed in the bridge segment. Otherwise, delayed completions (for example, configuration read completions) could be stuck behind a posted write and cannot proceed from PCI to PCI Express.
1	RW	0	**Memory Space Enable (MSE):** Controls the response as a target to memory accesses on the PCI Express interface that address a device behind the PCI Express Switch. 0 = These transactions are master aborted on the PCI Express interface. 1 = To allowed memory transaction from PCI to be passed to the PCI Express.
0	RW	0	**I/O Space Enable (IOSE):** Controls the PCI Express to PCI-X bridge's response as a target to I/O transactions on the PCI Express interface that addresses a device that resides behind the PCI Express to PCI-X bridge. 0 = These transactions are master aborted on the PCI Express interface. 1 = Enables response to I/O transaction initiated on the PCI Express interface.

13.3.1.4 Offset 06h: PCISTS—Status Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 06–07h
Default Value: 0010h
Attribute: RWC, RO
Size: 16 bits

Bits	Type	Reset	Description
15	RWC	0	**Detected Parity Error (DPE):** 0 = Software clears this bit by writing a 1 to it. 1 = Data parity error on the PCI Express bus interface or peer PCI segment is detected. This bit gets set even if the Parity Error Response (bit 6 of the command register) is not set.
14	RWC	0	**Signaled System Error (SSE):** This bit is used for PCI-compatible error signaling on the PCI Express bus. 0 = Software clears this bit by writing a 1 to it. 1 = SERR# is reported to the PCI Express interface.
13	RWC	0	**Received Master-Abort (RMA):** 0 = Software clears this bit by writing a 1 to it. 1 = Intel® 631xESB/632xESB I/O Controller Hub is acting as master on the PCI Express interface and receives a completion packet with master abort status.
12	RWC	0	**Received Target-Abort (RTA):** 0 = Software clears this bit by writing a 1 to it. 1 = Intel® 631xESB/632xESB I/O Controller Hub is acting as master on the PCI Express interface and receives a completion packet with target abort status.
11	RWC	0	**Signaled Target Abort (STA):** This bit is set whenever the PCI Express Switch generates a completion packet with CA status on PCI Express (either forwarded from PCI interface or internally signaled by SHPC) 0 = Target Abort not signaled on the PCI interface. 1 = Target Abort signaled on the PCI interface. Software clears this bit by writing a 1 to it.
10:9	RO	0	**DEVSEL# Timing (DVT):** These bits have no meaning on the PCI Express interface. Hardwired to 0.
8	RWC	0	**Master Data Parity Error (MDP):** 0 = Software clears this bit by writing a 1 to it. 1 = PCI Express Switch receives a completion packet from the PCI Express interface from a previous request, and detects a data parity error, and the Parity Error Response (PER) bit in the Command Register (offset 04h, bit 6) is set.
7	RO	0	**Fast Back-to-Back Transactions Capable (FBC):** Does not apply to PCI Express. Hardwired to 0.
6	RO	0	Reserved.
5	RO	0	**66 MHz Enable (66EN):** Does not apply to PCI Express. Hardwired to 0.
4	RO	1	**Capabilities List (CAPL):** Indicates that the PCI Express Switch contains the capabilities pointer in the bridge. Offset 34h (Capabilities List Pointer - CAPP) indicates the offset for the first entry in the linked list of capabilities.
3	RO	0	**Interrupt Status (INTSTS):** This bit reflects the state of the SHPC interrupt, when the interrupt is generated via the IRQ[23]# wire (not via MSI). Only when the INTx mask bit in the command register is a 0 and this Interrupt Status bit is a 1, and MSI is disabled will the SHPC assert the IRQ[23]# signal to the I/OxAPIC. Setting the INTx mask bit to a 1 has no effect on the setting of this bit.
2:0	RO	0	Reserved.

13.3.1.5 Offset 08h: RID—Revision ID Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 08h
Default Value: 00h
Attribute: RO
Size: 8 bits

Bits	Type	Description
7:0	RO	**Revision ID (REVID):** This indicates the stepping of the Intel® 631xESB/ 632xESB I/O Controller Hub PCI Express Switch. 00 = A0 stepping 01 = A1 stepping

13.3.1.6 Offset 09h: CC—Class Code Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 09–0Bh
Default Value: 060400h
Attribute: RO
Size: 24 bits

This contains the class code, sub class code, and programming interface for the device.

Bits	Type	Reset	Description
23:16	RO	06h	**Base Class Code (BCC):** The value of "06h" indicates that this is a bridge device.
15:8	ROS	04h	**Sub Class Code (SCC):** 8-bit value that indicates this is of type PCI-to-PCI bridge.
7:0	RO	0	**Programming Interface (PIF):** Indicates that this is standard (non-subtractive) PCI-to-PCI bridge.

13.3.1.7 Offset 0Ch: CLS—Cache Line Size Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 0Ch
Default Value: 00h
Attribute: RW
Size: 8 bits

This indicates the cache line size of the system.

Bits	Type	Reset	Description
7:0	RW	0	**Cache Line Size (CLS):** This field is implemented by PCI Express devices as a RW field for legacy compatibility purposes but has no impact on any PCI Express device functionality.

13.3.1.8 Offset 0Dh: PLT—Primary Latency Timer Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 0Dh
Default Value: 00h
Attribute: RW
Size: 8 bits

This register does not apply to the PCI Express interface.

Bits	Type	Reset	Description
7:3	RO	0	**Time Value (TV):** Read only register since PCI Express does not have an equivalent functionality.
2:0	RO	0	Reserved.

13.3.1.9 Offset 0Eh: HTYPE—Header Type Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 0Eh
Default Value: 81h
Attribute: RW
Size: 8 bits

This register is used to indicate the layout for bytes 10h through 3Fh of the device's configuration space.

Bits	Type	Reset	Description
Upstream Port			
7	RO	1	**Multi-Function Device (MFD):** Reserved as '1' to indicate the bridge is a multi-function device.
Downstream Port			
7	RO	0	**Multi-Function Device (MFD):** Reserved as '0' to indicate the bridge is not a multi-function device.
6:0	RO	01h	**Header Type (HTYPE):** Defines the layout of addresses 10h through 3Fh in configuration space. Reads as 01h to indicate that the register layout conforms to the standard PCI Express-to-PCI bridge layout.

13.3.1.10 Offset 18h: PBN— Primary Bus Number Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 18h
Default Value: 00h
Attribute: RW
Size: 8 bits

This register is used to record the bus number of the logical PCI bus segment to which the primary interface of the bridge is connected.

Bits	Type	Reset	Description
23:16	RW	00	**Subordinate Bus Number (SBBN):** Indicates the highest PCI bus number below this bridge. Any type one configuration cycle on PCI Express whose bus number is greater than the secondary bus number and less than or equal to the subordinate bus number will be run as a type one configuration cycle.
15:08	RW	00	**Secondary Bus Number (SCBN):** Indicates the bus number of the PCI Express bus to the south of this port. For the upstream port, this is the bus number for the PCI Express bus internal to the PCI Express Switch which connects the PCI Express upstream port to the PCI Express downstream ports. Any type one configuration cycle matching this bus number will be translated to a type 0 configuration cycle and passed to the appropriate downstream port.
7:0	RW	0	**Primary Bus Number (PBN):** This field indicates the bus number of the PCI Express interface. Configuration software programs the value in this register. Any type 1 configuration cycle with a bus number less than this number will not be accepted by this portion of the Intel® 631xESB/632xESB I/O Controller Hub.

13.3.1.11 Offset 1Bh: SLT—Secondary Latency Timer (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 1Bh
Default Value: 00h (PCI)
40h (PCI-X)
Attribute: RW, RO
Size: 8 bits

This timer controls the amount of time that the PCI Express Switch will continue to burst data on its secondary interface. The counter starts counting down from the assertion of PxFRAME#. If the grant is removed, the expiration of this counter will result in the de-assertion of PxFRAME#. If the grant has not been removed, then the

PCI Express Switch may continue ownership of the bus. Secondary latency timer's default value should be 64 in PCI-X mode (refer to Section 1.12.2 of the *PCI-X* Protocol Addendum to the PCI Local Bus Specification*, Revision 2.0a, Rule 11).

Bits	Type	Reset	Description
7:3	RO	0	**Secondary Latency Timer (SLT):** hard wired to 0
2:0	RO	0	Reserved.

13.3.1.12 Offset 1Ch: IOB—I/O Base Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 1Ch Attribute: RW, RO
Default Value: 00h Size: 8 bits

This register defines the base and limit (aligned to a 4-Kbyte boundary) of the I/O area of the bridge. Accesses from the PCI Express interface that are within the ranges specified in this register will be sent to PCI if the I/O space enable bit is set. Accesses from PCI that are outside the ranges specified will master abort.

Bits	Type	Reset	Description
7:4	RW	0	**I/O Base Address Bits [15:12] (IOBA):** This field defines the bottom address of an address range to determine when to forward I/O transactions from one interface to the other. These bits correspond to address lines 15:12 for 4 KB alignment. Bits 11:0 are assumed to be 000h.
3:2	RO	0	**I/O Base Address Bits [11:10] (IOBA1K):** When the EN1K bit is set in the Intel® 631xESB/632xESB I/O Controller Hub Configuration register (CNF), these bits become read/write and are compared with I/O address bits [11:10] to determine the 1 KB base address. When the EN1K bit is cleared, this field becomes Read Only.
1:0	RO	0	**I/O Base Addressing Capability (IOBC):** These are hardwired to '0', indicating support for only 16-bit I/O addressing.

13.3.1.13 Offset 1Dh: IOL—I/O Limit Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 1Dh Attribute: RW, RO
Default Value: 00h Size: 8 bits

This register defines the limit (aligned to a 4-Kbyte boundary) of the I/O area of the bridge. Accesses from the PCI Express interface that are within the ranges specified in this register will be sent to PCI if the I/O space enable bit is set. Accesses from PCI that are outside the ranges specified will master abort.

Bits	Type	Reset	Description
7:4	RW	0	**I/O Limit Address Bits [15:12] (IOLA):** Defines the top address of an address range to determine when to forward I/O transactions from PCI Express to PCI. These bits correspond to address lines 15:12 for 4 KB alignment. Bits [11:0] are assumed to be FFFh.
3:2	RO	0	**I/O Limit Address Bits [11:10] (IOLA1K):** When the EN1K bit is set in the Intel® 631xESB/632xESB I/O Controller Hub Configuration register (CNF), these bits become read/write and are compared with I/O address bits [11:10] to determine the 1 KB limit address. When the EN1K bit is cleared, this field becomes Read Only.
1:0	RO	0	**I/O Limit Addressing Capability (IOLC):** These bits are hardwired to '0', indicating support for only 16-bit I/O addressing.

13.3.1.14 Offset 1Eh: SSTS—Secondary Status Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 1E–1Fh
Default Value: 02A0h
Attribute: RWC, RO
Size: 16 bits

Bits	Type	Reset	Description
15	RWC	0	**Detected Parity Error (DPE):** This bit reports the detection of an uncorrectable address, attribute or data error by the Intel® 631xESB/632xESB I/O Controller Hub's PCI interface. This bit is set when any one of the following three conditions are true: • An uncorrectable address or attribute error as a potential target is detected. • An uncorrectable data error when the target of a write transaction. • An uncorrectable data error when the master of a read transaction (immediate read data) is detected. This bit gets set even if the Parity Error Response Enable bit (bit 0 of offset 3E–3Fh) of the Bridge Control Register. 0 = Uncorrectable address, attribute or data error not detected on the PCI interface. 1 = Uncorrectable address, attribute or data error detected on the PCI interface. Software clears this bit by writing a 1 to it.
14	RWC	0	**Received System Error (RSE):** This bit reports the detection of a SERR# assertion on the PCI interface. 0 = SERR# assertion on the PCI interface has not been detected. 1 = SERR# assertion on the PCI interface has been detected. Software clears this bit by writing a 1 to it.
13	RWC	0	Received Master Abort (RMA): This bit reports the detection of a Master-Abort termination when the PCI Express Switch is acting as a PCI master. 0 = Master-Abort not detected on the PCI interface. 1 = Master-Abort detected on the PCI interface Software clears this bit by writing a 1 to it.
12	RWC	0	Received Target Abort (RTA): This bit reports the detection of a Target-Abort termination when the PCI Express Switch is acting as a PCI master 0 = Target-Abort not detected on the PCI interface. 1 = Target-Abort detected on the PCI interface Software clears this bit by writing a 1 to it.
11	RWC	0	Signaled Target Abort (STA): This bit reports the signaling of a Target-Abort termination by the PCI Express Switch when it responds as the target of a transaction on the PCI interface. 0 = Target-Abort not signaled on the PCI interface. 1 = Target-Abort signaled on the PCI interface. Software clears this bit by writing a 1 to it.
10:9	RO	01b	**DEVSEL# Timing (DVT):** This field indicates that the PCI Express Switch responds in medium decode time to all cycles targeting the PCI Express interface.

Bits	Type	Reset	Description
8	RWC	0	**Master Data Parity Error (MDP):** This bit is used to report the detection of an uncorrectable data error. This Bit is set if the PCI Express Switch is the bus master of the transaction on the PCI interface, the Parity Error Response bit in the Bridge Control register is set, and either of the following two conditions occur: • The PCI Express Switch asserts PERR# on a read transaction • The PCI Express Switch detects PERR# asserted on a write transaction 0 = No uncorrectable data error detected on the PCI interface. 1 = Uncorrectable data error detected on the PCI interface. Once set, this bit remains set until it is reset by writing a 1 to this bit location. If the Parity Error Response bit is cleared, this bit is never set.
7	RO	1	**Fast Back-to-Back Transactions Capable (FBTC):** Indicates that the secondary interface can receive fast back-to-back cycles.
6	RO	0	Reserved.
5	RO	1	**66 MHz Capable (C66):** Indicates the secondary interface of the bridge is 66 MHz capable.
4:0	RO	0	Reserved.

13.3.1.15 Offset 20h: MB—Memory Base Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 20–21h Attribute: RW, RO
Default Value: 0000h Size: 16 bits

This register defines the base (aligned to a 1-Mbyte boundary) of the prefetchable memory area of the bridge. Accesses from the PCI Express interface that are within the range specified in this register will be sent to PCI if the memory space enable bit is set.

Accesses from PCI that are outside the range specified will be forwarded to the PCI Express interface if the bus master enable bit is set.

Bits	Type	Reset	Description
15:4	RW	0	**Memory Base (MB):** These bits are compared with bits [31:20] of the incoming address to determine the lower 1 MB aligned value (inclusive) of the range. The incoming address must be greater than or equal to this value.
3:0	RO	0	Reserved.

13.3.1.16 Offset 22h: ML—Memory Limit Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 22–23h Attribute: RW, RO
Default Value: 0000h Size: 16 bits

This register defines the limit (aligned to a 1 MByte boundary) of the prefetchable memory area of the bridge. Accesses from the PCI Express interface that are within the range specified in this register will be sent to PCI if the memory space enable bit is set.

Accesses from PCI that are outside the range specified will be forwarded to the PCI Express interface if the bus master enable bit is set.

Bits	Type	Reset	Description
15:4	RW	0	**Memory Limit (ML):** These bits are compared with bits [31:20] of the incoming address to determine the upper 1MByte aligned value (exclusive) of the range. The incoming address must be less than this value.
3:0	RO	0	Reserved.

13.3.1.17 Offset 24h: PMBL—Prefetchable Memory Base and Limit Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset:	24–27h	Attribute:	RW, RO
Default Value:	00010001h	Size:	32 bits

Defines the base (aligned to a 1 MByte boundary) of the prefetchable memory area of the bridge. Accesses from the PCI Express interface that are within the ranges specified in this register will be sent to PCI if the memory space enable bit is set.

Accesses from PCI that are outside the ranges specified will be forwarded to the PCI Express interface if the bus master enable bit is set.

Note that even though this register specifies a valid prefetchable memory window, the PCI Express Switch does not prefetch through this window in the outbound direction (reads from PCI Express to PCI). In the inbound direction, prefetchability through this window is controlled through the PCI Express Switch configuration register bits 4:3, at offset 40h.

Bits	Type	Reset	Description
31:20	RW	0	**Prefetchable Memory Limit (PML):** These bits are compared with bits [31:20] of the incoming address to determine the upper 1MByte aligned value (exclusive) of the range. The incoming address must be less than this value.
19:16	RO	1	**64-bit Indicator (IS64L):** Indicates that 64-bit addressing is supported for the limit. This value must be in agreement with the IS64B field.
15:4	RW	0	**Prefetchable Memory Base (PMB):** These bits are compared with bits [31:20] of the incoming address to determine the lower 1 MB aligned value (inclusive) of the range. The incoming address must be greater than or equal to this value.
3:0	RO	1	**64-bit Indicator (IS64B):** Indicates that 64-bit addressing is supported for the limit. This value must be in agreement with the IS64L field.

13.3.1.18 Offset 28h: PMBU32—Prefetchable Base Upper 32 Bits Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset:	28–2Bh	Attribute:	RW, RO
Default Value:	00000000h	Size:	32 bits

This defines the upper 32 bits of the prefetchable address base register.

Bits	Type	Reset	Description
31:0	RW	0	**Prefetchable Memory Base Upper Portion (PMBU):** All bits are read/ writeable; full 64-bit addressing supported.

13.3.1.19 Offset 2Ch: PMLU32—Prefetchable Limit Upper 32 Bits Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset:	2C–2Fh	Attribute:	RW
Default Value:	00000000h	Size:	32 bits

This defines the upper 32 bits of the prefetchable address limit register.

Bits	Type	Reset	Description
31:0	RW	0	**Prefetchable Memory Limit Upper Portion (PMLU):** All bits are read/ writeable; full 64-bit addressing supported.

13.3.1.20 Offset 34h: CAPP—Capabilities Pointer Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 34h
Default Value: 44h
Attribute: RO
Size: 8 bits

This register is used to point to a linked list of additional capabilities.

Bits	Type	Reset	Description
7:0	RO	44h	**Capabilities Pointer (PTR):** This field indicates that the pointer for the first entry in the PCI Express Capability List is at offset 44h in configuration space.

13.3.1.21 Offset 3Ch: INTR—Interrupt Information Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 3C-3Dh
Default Value: 00h
Attribute: RWO, RO
Size: 16 bits

This register communicates interrupt information.

Bits	Type	Reset	Description
15:8	RWO	01h	**Interrupt Pin (INTR):** The logical primary bus interrupt pin is INTA# for the upstream port with a corresponding register value of 01h.
7:0	RO	00h	**Interrupt line(line):** This register is used to convey the interrupt line routine information. Not used because PCI Express does not have interrupt lines

13.3.1.22 Offset 3Eh: BCTRL—Bridge Control Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 3E–3Fh
Default Value: 0000h
Attribute: RW, RWC; RO
Size: 16 bits

This register provides extensions to the Command register that are specific to a bridge. The Bridge Control register provides many of the same controls for the secondary interface that are provided by the Command register for the primary interface. Some bits affect operation of both interfaces of the bridge.

Bits	Type	Reset	Description
15:12	RO	0	Reserved.
11	RO	0	**Discard Timer SERR Enable (DTSE):** Not applicable to PCI Express. Hardwired to 0.
10	RO	0	**Discard Timer Status (DTS):** Not applicable to PCI Express. Hardwired to 0.
9	RO	0	**Secondary Discard Timer (SDT):** Not applicable to PCI Express. Hardwired to 0.
8	RO	0	**Primary Discard Timer (PDT):** Not relevant to the PCI Express interface. This bit is RW for software compatibility only.
7	RO	0	**Fast Back-to-Back Enable (FBE):** Not applicable to PCI Express. Hardwired to 0.
6	RW	0	**Secondary** Bus Reset (SBR): Setting this bit triggers a hot reset on the downstream link for the corresponding PCI Express port and the PCI Express hierarchy domain subordinate to the port. In Intel® 631xESB/632xESB I/O Controller Hub, setting this bit for the upstream port causes the corresponding SBR bits in the downstream ports to get set. Note that it is the responsibility of software to make sure that all pending transactions with the bus segment are complete before setting this bit. Failing which, transactions could be lost.
5	RO	0	**Master Abort Mode (MAM):** Not applicable to PCI Express. Hardwired to 0.

Bits	Type	Reset	Description
4	RW	0	**VGA 16-bit Decode (V16D):** This bit enables the bridge to provide 16-bit decoding of the VGA I/O address precluding the decode of VGA alias addresses every 1 KB. This bit requires the VGA enable bit (bit 3 of this register) to be set to 1. 0 = Disable 1 = Enable
3	RW	0	**VGA Enable (VGAE):** Modifies the response to VGA compatible address. 1 = the following transactions from the PCI Express interface to PCI regardless of the value of the I/O base and I/O limit registers is forwarded. The transactions are qualified by the memory enable and I/O enable in the command register. Memory addresses: 000A0000h–000BFFFFh I/O addresses: 3B0h–3BBh and 3C0h-3DFh. For the I/O addresses, bits [63:16] of the address must be '0', and bits [15:10] of the address are ignored (that is, aliased). 0 = The same holds true from secondary accesses to the primary interface in reverse. That is, when the bit is 0, memory and I/O addresses on the secondary interface between the above ranges will be forwarded to the PCI Express interface.
2	RW	0	**ISA Enable (IE):** Modifies the response by the bridge to ISA I/O addresses. This only applies to I/O addresses that are enabled by the I/O Base and I/O Limit registers and are in the first 64 KB of PCI I/O space. 0 = Disable. 1 = Enable. The bridge will block any forwarding from primary to secondary of I/O transactions addressing the last 768 bytes in each 1 KB block (offsets 100h to 3FFh). This bit has no effect on transfers originating on the secondary bus as the Intel® 631xESB/632xESB I/O Controller Hub does not forward I/O transactions across the bridge.
1	RW	0	**SERR Enable (SE):** Controls the forwarding of secondary interface SERR# assertions on the primary interface. 0 = Disable. 1 = Enable. The Intel® 631xESB/632xESB I/O Controller Hub will send a PCI Express interface SERR cycle when all of the following are true: SERR# is asserted on the secondary interface This bit is set The SERR Enable bit in the Command Register is set
0	RW	0	**Parity Error Response Enable (PERE):** Controls the response to address and data parity errors on the secondary interface. 0 = The bridge must ignore any parity errors that it detects and continue normal operation. The Intel® 631xESB/632xESB I/O Controller Hub must generate parity even if parity error reporting is disabled. 1 = Report parity errors.

13.3.1.23 Offset 40h: CNF—PCI Express* Configuration Register (Bm:D0:F0, Bp:D0:F0, Bp:D1:F0, Bp:D2:F0)

Offset:	40–41h	Attribute:	RW, RO
Default Value:	See Register Description	Size:	16 bits

Intel® 631xESB/632xESB I/O Controller Hub PCI Express Endpoint function-specific control bits.

For the downstream ports, these bits are disabled.

Bits	Type	Reset	Description
15:14	RO	00	**PCI Mode (PMODE):** Not used for PCI Express.
13	RWS	1	I/OxAPIC Config Space Disable (ICSD): 0 = I/OxAPIC configuration space is enabled. 1 = Disables all configuration accesses to I/OxAPIC configuration space from PCI Express. All configuration accesses from PCI Express to I/OxAPIC are master aborted. This bit has no affect on the SMBus or memory accesses to I/OxAPIC configuration space. By default the APIC configuration space is hidden.
12	RO	0	**Enable I/O Space to 1 KB Granularity (EN1K):** Reserved, not used for PCI Express. This field exists in the PCIX_CONFIG register.
11	RO	1	Reserved
10:9	RO	0	**PCI Frequency (PFREQ):** Reserved, not used for PCI Express. This field exists in the PCIX_CONFIG register.
8	RO	0	Reserved
7	RW	1	Reserved
6	RO	0	Reserved
5	RO	0	Reserved
4	RO	0	Reserved
3	RW	0	Reserved
2	RW	0	Reserved
1:0	RO	00	Maximum Inbound Delayed Transactions (MDT): Controls the maximum number of inbound delayed transactions Intel® 631xESB/632xESB I/O Controller Hub is allowed to have: 00: 4 active, 4 pending 01: 1 active, 1 pending 10: 2 active, 2 pending 11: Reserved

13.3.1.24 Offset 42h: EXP_CMMPC—PCI Express* Compliance Measurement Mode (CMM) Port Control (Bp:D0:F0,Bp:D1:F0)

Offset:	42-43h	Attribute:	RWS
Default Value:	0000h	Size:	16 bits

The Intel® 631xESB/632xESB I/O Controller Hub downstream PCI Express ports PE1 and PE2 Compliance Measurement Mode (CMM) is supported in test mode environment only that can be used to obtain the characteristics of the transmitter and receiver (that is, DFT tests focused). In normal operation, the CMM is disabled by default.

The compliance mode can be entered by setting PE1 offset 0x42h bit [5] to ‘1’ and using a valid compliance load plugged into the port. PE1 bit [5] controls PE1 and PE2 and the default setting is ‘0’, meaning disabled. A warm reset of the system is required after setting this bit to ‘1.’ Upon reset, Intel® 631xESB/632xESB I/O Controller Hub detects the presence of a valid compliance load card on this port and enters the compliance mode.

Note that for Hot-Plug design, hardware/software considerations are required for power controller and CMM enable state.

Bits	Type	Reset	Description
15:6	RV	0h	Reserved
5	RWS	0h	0= Normal Operation (Disable Compliance) 1= Enable Compliance (LTSSM)
4:0	RV	0h	Reserved

13.3.1.25 Offset 44h: EXP_CAPID—PCI Express* Capability Identifier Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 44h
Default Value: 10h
Attribute: RO
Size: 8 bits

Bits	Type	Reset	Description
7:0	RO	10h	**PCI Express Capability Identifier (PCI ExpressCAPI):** Indicates PCI Express capability.

13.3.1.26 Offset 45h: EXP_NXTP—PCI Express* Next Pointer Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 45h
Default Value: 70h or 60h
Attribute: RO
Size: 8 bits

Bits	Type	Reset	Description
Upstream Port			
7:0	RO	70h	Next Capability Pointer (MNPTR): Points to the next capabilities list pointer which is the PCI Express power management capability
Downstream Port			
7:0	RO	60h	**Next Pointer (MNPTR):** Points to the next capabilities list pointer, which is the MSI capability.

13.3.1.27 Offset 46h: EXP_CAP—PCI Express* Capability Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 46 - 47h
Default Value: 0051h(Upstream)
0061h(Downstream
Attribute: RO
Size: 16 bits

Bits	Type	Reset	Description
15:14	RO	0	Reserved.
Upstream Port			
13:9	RO	0	Interrupt Message Number: Not used.
8	RO	0	Slot Implemented: 1: Indicates the PCI Express link associated with this port is connected to a slot 0: Indicates no slot is connected to this port Upstream Port and downstream port attached to internal core: This bit is hardwired to 0
7:4	RO	5h	**Device/Port Type (DEVPORT):** Indicates the type of PCI Express logical device. Value of 5h indicates that this is a upstream port of a PCI Express switch
Downstream Port			

Bits	Type	Reset	Description
13:9	RO	0	Interrupt Message Number: This field indicates the interrupt message number that is generated from the PCI Express port. When there is more than one MSI interrupt number, this register field is required to contain the offset between the base Message Data and the MSI Message that is generated when the status bits in the slot status register or root port status registers are set. The chipset is required to update the field if the number of MSI messages changes.
8	RO or RWO	0	Slot Implemented: 1: Indicates the PCI Express link associated with this port is connected to a slot 0: Indicates no slot is connected to this port Downstream Ports attached to external links: This bit is RWO
7:4	RO	6h	**Device/Port Type (DEVPORT):** Indicates the type of PCI Express logical device. Value of 6h indicates that this is a downstream port of a PCI Express switch.
3:0	RO	1h	**Capability Version (CAPVER):** Indicates PCI-SIG defined PCI Express capability structure version number. Must be 1h for this version.

13.3.1.28 Offset 48h: EXP_DCAP—PCI Express* Device Capabilities Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 48 – 4Bh
Default Value: 00000001h
Attribute: RO
Size: 32 bits

This register contains information about the PCI Express link capabilities.

Bits	Type	Reset	Description
31:28	RO	0	Reserved.
27:26	RO	0	**Captured Slot Power Limit Scale:** For Upstream Port: In combination with the Slot Power Limit value, specifies the upper limit on power supplied by slot. Power limit (in Watts) calculated by multiplying the value in this field by the value in the Slot Power Limit Value field. This value is set by the Set_Slot_Power_Limit message. For Downstream Ports: Not used. Hardwired to 0.
25:18	RO	000h	**Captured Slot Power Limit Value**: For Upstream Port: In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot. Power limit (in Watts) calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field. This value is set by the Set_Slot_Power_Limit message. For Downstream Ports: Not used. Hardwired to 0.
17:15	RO	0	Reserved
14	RO	0	**Power Indicator Present:** Not used. Hardwired to 0.
13	RO	0	**Attention Indicator Present:** Not used. Hardwired to 0.
12	RO	0	**Attention Button Present:** Not used. Hardwired to 0.
11:9	RO	0	**Endpoint L1 Acceptable Latency (L1AL):** The PCI Express Switch does not support L1 Link State Power Management (LSPM).
8:6	RO	0	**Endpoint L0s Acceptable Latency (L0AL):** The PCI Express Switch wants the least possible latency out of L0s.

Bits	Type	Reset	Description
5	RO	0	**Extended Tag Field Supported (ETFS):** This field indicates the maximum supported size of the Tag Field. Defined encodings are: 0 = 5-bit Tag field supported 1 = 8-bit Tag field supported The PCI Express Switch supports only a 5-bit tag.
4:3	RO	0	Reserved.
2:0	RO	1	**Supported Maximum Payload Size (SMPS):** The PCI Express Switch supports a max payload size of 256 byte packets.

13.3.1.29 Offset 4Ch: EXP_DCTL—PCI Express* Device Control Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 4C – 4Dh
Default Value: 5020h
Attribute: RW, RO
Size: 16 bits

This register contains command bits that control the PCI Express Switch behavior on the PCI Express bus.

Bits	Type	Reset	Description
15	RO	0	Reserved
14:12	RW	101b	**MaX_Read_Request Size (MRRS):** The PCI Express Switch cannot send requests greater than the size indicated by this field. Encodings are: Value Request Size 000b 128 bytes 001b 256 bytes 010b 512 bytes 011b 1024 bytes 100b 2048 bytes 101b 4096 bytes 110b Reserved 111b Reserved
11	RO	0	**Enable No Snoop (ENS):** This does not apply to the PCI Express SwitchPCI Express Switch since it does not set the No Snoop bit on MSI transactions it generates.
10	RO	0	**Auxiliary (AUX) Power PM Enable (AUXPWRPM_EN):** The PCI Express Switch ignores this since it does not support Aux Power.
9	RO	0	**Phantom Function Enable (PFE):** The PCI Express Switch ignores this since it does not support Phantom functions.
8	RO	0	**Extended Tag Field Enable (ETFE):** Always a 0 since the PCI Express Switch only supports a 5-bit tag.
7:5	RW	001	**Maximum Payload Size (MPS):** For PCI Express Switch this must be programmed to either 000 (128B) or 001(256B). Any other value will default to a behavior of 128B.
4	RW	0	Reserved.
3	RW	0	**Unsupported Request Reporting Enable (URRE):** Enables reporting of unsupported requests.

Bits	Type	Reset	Description
2	RW	0	**Fatal Error Reporting Enabled (FERE):** Controls reporting of fatal errors. 0 = Disable. 1 = PCI Express Switch will report fatal errors.
1	RW	0	**Non-Fatal Error Reporting Enabled (NFERE):** Controls reporting of non-fatal errors. 0 = Disable. 1 = PCI Express Switch will report uncorrectable errors.
0	RW	0	**Correctable Error Reporting Enable (CERE):** Controls reporting of correctable errors. 0 = Disable. 1 = Report correctable errors.

13.3.1.30 Offset 4Eh: EXP_DSTS—PCI Express* Device Status Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 4E – 4Fh Attribute: RWC; RO
Default Value: 0000h Size: 16 bits

This register contains information on the PCI Express device status.

Bits	Type	Reset	Description
15:6	RO	0	Reserved.
5	RO	0	**Transactions Pending (TP):** Reserved
4	RO	0	**Aux Power Detected (APD):** The PCI Express Switch does not support aux power and hence this bit is reserved.
3	RWC	0	**Unsupported Request Detected URD):** The PCI Express Switch sets this bit when any unsupported request from PCI Express is received. This includes requests that are not claimed by any functions within the PCI Express Switch, but does NOT include any request that is forwarded to the PCI interface with completions returned with an unsupported request status.
2	RWC	0	**Fatal Error Detected (FERRD):** When set, a fatal error has been detected (regardless of whether an error message was generated or not). This bit remains set until software writes a 1 to clear it.
1	RWC	0	**Non-Fatal Error Detected (NFERRD):** When set, a nonfatal error has been detected (regardless of whether the mask bit was set in advanced error capability or not). This bit remains set until software writes a 1 to clear it.
0	RWC	0	**Correctable Error Detected (CERRD):** When set, a correctable error has been detected (regardless of whether an error message was generated). This bit remains set until software writes a 1 to clear it.

13.3.1.31 Offset 50h: EXP_LCAP—PCI Express* Link Capabilities Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 50 – 53h Attribute: RO
Default Value: see reg desc. Size: 32 bits

This register identifies PCI Express Link specific capabilities.

Bits	Type	Reset	Description
Upstream Port			
31:24	RO	0	Reserved.
Downstream Port			
31:24	RWO	0	**Port Number:** This field indicates the PCI Express port number assigned to this link. This can be over-written and initialized by firmware.
23:18	RO	0	Reserved.
17:15	RO	111b	**L1 Exit Latency (L1EL):** L1 transition is not supported.

Bits	Type	Reset	Description
14:12	RO	111b	**L0s Exit Latency (L0EL):** The value in these bits is influenced by bit 6 in the link control register. Note that software could write the bit 6 in link control register to either a 1 or 0 and these bits should change accordingly. The mapping is shown below: Bit 6 in EXP_LCTL — Bits 14:12 in EXP_LCAP 0 — 111b 1 — Derived from Hardware BIOS should insure the L0s exit latency for upstream port function 0 matches the L0s exit latency for upstream port function 3.
11:10	RO	1h	**Active State Link PM Support (ASLPMS):** Only Active State L0s supported.
Upstream Port			
9:4	RO	08h	**Maximum Link Width (MLW):** Support a X8, X4 link maximum.
Downstream Port			
9:4	RO	04h or 08h	**Maximum Link Width (MLW):** Support a X4 or X8 link maximum.
3:0	RO	1h	**Maximum Link Speed (MLS):** Support 2.5 Gbps.

13.3.1.32 Offset 54h: EXP_LCTL– PCI Express* Link Control Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 54 – 55h
Attribute: RW, RO
Default Value: 0040h
Size: 16 bits

This register controls PCI Express Link specific parameters.

Bits	Type	Reset	Description
15:8	RO	0	Reserved.
7	RW	0	**Extended Synch (EXTS):** This bit when set forces extended transmission of 4096 fast training sequence (FTS) ordered sets in FTS and an extra 1024 training sequence one (TS1) at exit from L1 prior to entering L0. This mode provides external devices monitoring the link time to achieve bit and symbol lock before the link enters L0 state and resumes communication. Default value for this bit is 0.
6	RW	0	**Common Clock Configuration** (CCC): This bit when set indicates that this port and the port at the opposite end of this Link are operating with a distributed common reference clock. A value of 0 indicates that this component and the component at the opposite end of this Link are operating with asynchronous reference clock. Note that this bit is used to reflect the proper L0s exit latency value in the PCIE_LCAP register.
Upstream Port			
5:4	RO	0	Reserved.
Downstream Port			
5	RW	0	**Retrain Link:** This bit, when set, initiates link retraining in the given PCI Express port. It always returns 0 when read.
4	RW	0	**Disable Link:** This bit, when set, disables the link for the given PCI Express port.
3:2	RO	0	Reserved.
1:0	RW	0	**Active State Link PM Control (ASLPMC):** Enables the PCI Express Switch to enter L0s 00 = L0s entry disabled 01 = PCI Express Switch enters L0s per the specification requirements for L0s entry. 10 =Reserved 11 = Reserved

13.3.1.33 Offset 56h: EXP_LSTS – PCI Express* Link Status Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 56 – 57h
Default Value: see reg. desc.
Attribute: RO
Size: 16 bits

This register provides information about PCI Express Link specific parameters.

Bits	Type	Reset	Description
15:13	RO	0	Reserved.
12	ROS	0	**Slot Clock Configuration** – This bit indicates that when Intel® 631xESB/632xESB I/O Controller Hub is on a PCI Express connector, that it is using the same reference clock as is provided at the connector. A value of 0 indicates independent reference clock and a value of 1 indicates same reference clock. Note that this bit becomes RWS when ACNF[2] is set.
Upstream Port			
11:10	RO	0	Reserved.
Downstream Port			
11	RO	x	**Link Training:** This read-only bit indicates the Physical Layer LTSSM is in the Configuration or Recovery state, or that 1b was written to the Retrain Link bit but Link training has not yet begun. Hardware clears this bit when the LTSSM exits the Configuration/Recovery state.
10	RO	x	**Undefined –** The value read from this bit is undefined. In previous versions of this specification, this bit was used to indicate a Link Training Error. System software must ignore the value read from this bit. System software is permitted to write any value to this bit.
9:4	RO	x	**Negotiated Link Width (NLW):** This field indicates the negotiated width of PCI Express Link. Defined encodings are: 000100b X4 001000b X8
3:0	RO	0001b	**Link Speed (LS):** This field indicates the negotiated Link speed of the PCI Express Link. The Intel® 631xESB/632xESB I/O Controller Hub supports only 2.5 Gbps.

13.3.1.34 Offset 58h: EXP_SCAP – PCI Express* Slot Capabilities Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 58 – 5Bh
Default Value: 0h
Attribute: RO
Size: 32 bits

This register is used only by downstream ports in which the SLOTIMP bit in the PCIE_CAP register is 1. This includes all downstream ports that have Hot-Plug-capable devices attached.

Bits	Type	Reset	Description
Downstream Port			
31:19	RWO	0	**Physical Slot Number** – This hardware initialized field indicates the physical slot number attached to this port. This field must be hardware initialized to a value that assigns a slot number that is globally unique within the chassis. These registers should be initialized to 0 for ports connected to devices that are either integrated on the motherboard or integrated within the same silicon as the switch device or root port.
18:17	RO	0	Reserved.
16:15	RWO	00b	**Slot Power Limit Scale** – Specifies the scale used for the Slot Power Limit Value. 00 = 1.0X (25.5 - 255) 01 = 0.1X (2.55 – 25.5) 10 = 0.01X (0.255 – 2.55) 11 = 0.001X (0.0 – 0.255)

Bits	Type	Reset	Description
14:7	RWO	0	**Slot Power Limit Value** – In combination with the Slot Power Limit Scale value, this register specifies the upper limit on power supplied by slot. Power limit (in watts) calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field. This value is set by the Set_Slot_Power_Limit message or hardwired to 00h.
6	RWO	0	**Hot-Plug capable –** This bit when set indicates that this slot is capable of supporting Hot-Plug operations. Used as Hot-Plug enable for the Hot-Plug controller.
5	RO	0	**Hot-Plug Surprise** – This bit when set indicates that a device present in this slot might be removed from the system without any prior notification. Intel® 631xESB/632xESB I/O Controller Hub does not support this feature, the bit should always be 0.
4	RWO	0	**Power Indicator Present** – This bit when set indicates that a Power Indicator is implemented on the chassis for this slot.
3	RWO	0	**Attention Indicator Present** – This bit when set indicates that an Attention Indicator is implemented on the chassis for this slot.
2	RWO	0	**MRL Sensor Present** – This bit when set indicates that an MRL Sensor is implemented on the chassis for this slot.
1	RWO	0	**Power Controller Present** – This bit when set indicates that a Power Controller is implemented for this slot
0	RWO	0	**Attention Button Present** – This bit when set indicates than an Attention Button is implemented on the chassis for this slot.

13.3.1.35 Offset 5Ch: EXP_SCTL— PCI Express* Slot Control Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 5Ch Attribute: RW, RO
Default Value: 3Ch Size: 16 bits

Note: This register is used only by downstream ports in which the SLOTIMP bit in the PCIE_CAP register is 1. This includes all downstream ports that have Hot-Plug-capable devices attached.

Bits	Type	Reset	Description
15:11	RO	0	Reserved.
10	RWS	0h	**Power Controller Control** – When read this register returns the current state of the Power Applied to the slot; when written sets the power state of the slot per the defined encodings. 0 – Power On 1 – Power Off
9:8	RWS	11b	**Power Indicator Control** – Read to this register return the current state of the Power Indicator; writes to this register set the Power Indicator. Defined Encodings are: 00 – Reserved 01– On 10 – Blink 11 – Off
7:6	RWS	11b	**Attention Indicator Control** – Read to this register return the current state of the Attention Indicator; writes to this register set the Attention Indicator. Defined Encodings are: 00 – Reserved 01 – On 10 – Blink 11 – Off
5	RWS	0h	**Hot-Plug Interrupt Enable** – This bit when set enables generation of Hot-Plug interrupt on enabled Hot-Plug events.

Bits	Type	Reset	Description
4	RWS	0h	**Command Complete Interrupt Enable** - This bit when set enables the generation of Hot-Plug interrupt or wake message when the controller is ready to accept another command. (This may mean that the command has not actually finished executing.)
3	RWS	0h	**Presence Detect Changed Enable** - This bit when set enables the generation of Hot-Plug interrupt or wake message on an presence detect changed event.
2	RWS	0h	**MRL Sensor Changed Enable** - This bit when set enables the generation of Hot-Plug interrupt or wake message on an MRL sensor changed event.
1	RWS	0h	**Power Fault Detected Enable** – This bit when set enables the generation of Hot-Plug interrupt or wake message on a power fault event.
0	RWS	0h	**Attention Button Pressed Enable** – This bit when set enables the generation of Hot-Plug interrupt or wake message on an attention button pressed event.

13.3.1.36 Offset 5Eh: EXP_SSTS—PCI Express* Slot Status Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 5E – 5Fh Attribute: RW; RO
Default Value: 0000h Size: 16 bits

Note: This register is used only by downstream ports in which the SLOTIMP bit in the PCIE_CAP register is 1. This includes all downstream ports that have Hot-Plug-capable devices attached.

Bits	Type	Reset	Description
15:7	RO	0	Reserved.
6	RO	0	**Presence Detect State** – This bit indicates the presence of a card in the slot. This bit reflects the status of the Presence Detect Pin. This register required if a slot is implemented. 0 – Slot Empty 1 – Card Present in slot
5	RO	0	**MRL Sensor State** – This register reports the status of the MRL sensor if it is implemented. 0 – MRL Closed 1 – MRL Open
4	RWC	0	**Command Completed** – This bit is set when the Hot-Plug controller completes an issued command.
3	RWC	0	**Presence Detect Changed** – This bit is set when a Presence Detect change is detected.
2	RWC	0	**MRL Sensor Changed** – This bit is set when a MRL Sensor state change is detected.
1	RWC	0	**Power Fault Detected** – This bit is set when the Power Controller detects a power fault at this slot.
0	RWC	0	**Attention Button Pressed** – This bit is set when the attention button is pressed.

13.3.1.37 Offset 60h: MSI_CAPID—PCI Express* MSI Capability Identifier Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 60h
Default Value: 00h, 05h
Attribute: RO
Size: 8 bits

Bits	Type	Reset	Description
Upstream Port			
7:0	RO	0	Reserved.
Downstream Port			
7:0	RO	05	**Capability ID(MCID):** Capabilities ID indicates MSI.

13.3.1.38 Offset 61h: MSI_NXTP—PCI Express* Next Item Pointer Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 61h
Default Value: 70h
Attribute: RO
Size: 8 bits

Bits	Type	Reset	Description
7:0	RO	70	**Next Pointer:** Points to the next capabilities list pointer which is the PCI Express power management capability.

13.3.1.39 Offset 62h: MSI_MC—PCI Express* MSI Message Control Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 62 – 63h
Default Value: 0080h
Attribute: RW, RO
Size: 16 bits

Bits	Type	Reset	Description
15:8	RO	0	Reserved.
7	RO	1	**64 Bit Address Capable:** PCI Express Switch is capable of generating a 64-bit message address
6:4	RW	000	**Multiple Message Enable:** PCI Express Switch supports only one message and these bits are R/W for software compatibility.
3:1	RO	000	**Multiple Message Capable:** PCI Express Switch supports only one message.
0	RW	0	**MSI Enable:** If set, MSI is enabled and does not use internal wires to the internal APIC to generate interrupts.

13.3.1.40 Offset 64h: MSI_MA—PCI Express* MSI Message Address Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 64 – 6Bh
Default Value: 0000h
Attribute: RW,RO
Size: 64 bits

Bits	Type	Reset	Description
63:2	RW	0	**Address (ADDR):** System specified message address, always DWORD aligned.
1:0	RO	00	Reserved.

13.3.1.41 Offset 6Ch: MSI_MD – PCI Express* MSI Message Data Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 6Ch Attribute: RW
Default Value: 0000h Size: 16 bits

This register identifies specific PCI Express Power Management capabilities.

Bits	Type	Reset	Description
15:0	RW	0h	**Data (DATA):** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (D[15:0]) of the MSI memory write transaction.

13.3.1.42 Offset 70h: EXPPM_CAPID – PCI Express* Bridge Power Management Capability Identifier Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 70h Attribute: RO
Default Value: 01h Size: 8 bits

Bits	Type	Reset	Description
7:0	RO	01	**Capability ID:** Capabilities ID indicates PCI compatible PM.

13.3.1.43 Offset 71h: EXPPM_NXTP – PCI Express* Bridge Power Management Next Item Pointer Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 71h Attribute: RO
Default Value: 00h Size: 8 bits

Bits	Type	Reset	Description
7:0	RO	80	Points to the next capabilities list pointer which is the SVID capability.

13.3.1.44 Offset 72h: EXPPM_PMC—PCI Express* Bridge Power Management Capabilities (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 72h Attribute: RO
Default Value: C802h Size: 16 bits

Bits	Type	Reset	Description
15:11	RO	11001b	**PME_Support** – The PCI Express Switch supports PME assertion on behalf of SHPC when in D3hot. The PCI Express Switch does not generate PME from D3cold
10	RO	0	**D2 Support:** PCI Express Switch does not support D2 device state
9	RO	0	**D1 Support:** PCI Express Switch does not support D1 device state
8:6	RO	0	**Aux Current:** PCI Express Switch does not support Aux power
5	RO	0	**DSI** – PCI Express Switch does not require device-specific initialization when transitioned to D0 from D3hot state. So this bit is zero.
4	RO	0	Reserved
3	RO	0	**PME Clock:** Not relevant to PCI Express and hence hardwired to 0.
2:0	RO	2	**Version:** PCI Express Switch PM Implementation is compliant with 1.1 of the PCI PM Spec

13.3.1.45 Offset 74h:EXPPM_PMCSR—PCI Express* Bridge Power Management Control/Status Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 74 – 75h
Default Value: 0h
Attribute: RW, RO, RWS
Size: 16 bits

Bits	Type	Reset	Description
			Upstream Port
15:0	RO	0h	Reserved
			Downstream Port
15	RWCS	0h	**PME Status:** This bit is sticky. When set, the PCI Express port generates a PME internally independent of the PMEEN bit defined below. Software clears this bit by writing a 1 when it has been completed.
14:13	RO	0h	**Data Scale:** PCI Express Switch does not implement Data register and hence these two bits are 0
12:09	RO	0h	**Data Select:** Reserved since data register is not implemented
8	RWS	0h	**PME En:** Gates assertion of the PME message.
7:2	RO	0h	Reserved
1:0	RW	0h	**PowerState** – This 2-bit field is used both to determine the current power state of a function and to set the function into a new power state. PCI Express Switch supported field values are given below. 00b – D0 01b – Reserved 10b – Reserved 11b – D3 If software attempts to write an unsupported, optional state to this field, the write operation must complete normally on the bus; however, the data is discarded and no state change occurs.

13.3.1.46 Offset 76h:EXPPM_BSE—PCI Express* Bridge Power Management Bridge Support Extension Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 76h
Default Value: 00h
Attribute: RO
Size: 8 bits

Bits	Type	Reset	Description
7	RO	0h	**PCC_En (Bus Power/Clock Control Enable):** PCI Express Switch* does not provide either bus or clock control of PCI when in D3hot state. This bit is hardwired to 0.
6	RO	0h	**B2/B3#:** This bit has no meaning in PCI Express Switch since BPCC_En bit is a 0.
5:0	RO	0h	Reserved

13.3.1.47 Offset 77h:PCIEPM_DATA—PCI Express* Bridge Power Management Data Field Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 77h
Default Value: 00h
Attribute: RO
Size: 8 bits

Bits	Type	Reset	Description
07:00	RO	0h	**Data:** PCI Express Switch* does not report the data register

13.3.1.48 Offset 80h:SVID_CAPID — Subsystem and Vendor ID Capabilities Identifier Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 80h
Default Value: 0Dh
Attribute: RO
Size: 8 bits

Identifies this item in the Capabilities list as the PCI bridge subsystem vendor capability. It returns 0Dh when read.

Bits	Type	Reset	Description
07:00	RO	0D	**Identifier (ID):** Indicates this is the PCI bridge subsystem vendor capability.

13.3.1.49 Offset 81h:SVID_NXTP — Next Item Pointer Register (Bm:D0:F0, Bp:D0:F0, Bp:D1:F0, Bp:D2:F0)

Offset: 81h
Default Value: 00h
Attribute: RO
Size: 8 bits

Note: Indicates where the next item in the capabilities list resides. This is the last item in the list.

Bits	Type	Reset	Description
07:00	RO	00	**Next Pointer:** SVID is the last capability list item and hence these bits are all 0s.

13.3.1.50 Offset 84h:SVID — Subsystem Vendor ID Register (Bm:D0:F0, Bp:D0:F0, Bp:D1:F0, Bp:D2:F0)

Offset: 84h
Default Value: 0000h
Attribute: RO
Size: 16 bits

Bits	Type	Reset	Description
07:00	RWOS	0000	**Subsystem Vendor Identifier:** Indicates the manufacturer of the subsystem. This field is write once and is locked down until a power good reset occurs.

13.3.1.51 Offset 86h:SID — Subsystem ID Register (Bm:D0:F0, Bp:D0:F0, Bp:D1:F0, Bp:D2:F0)

Offset: 86h
Default Value: 0000h
Attribute: RO
Size: 16 bits

Bits	Type	Reset	Description
07:00	RWOS	0000	**Subsystem Identifier:** Indicates the subsystem as identified by the vendor. This field is write once and is locked down until a bridge reset occurs (not the PCI Express link reset).

13.3.1.52 Offset FCh: EXP_PHC — PCI Express* Port Hide Control(Bp:D1:F0, Bp:D2:F0)

Offset: FCh Attribute: RWS
Default Value: 0003h Size: 16 bits

Bits	Type	Reset	Description
15:8	RWS	0h	Reserved
7	RWS	0h	Hide PCI Express downstream Integrated LAN port 0: configuration space visible 1: configuration space hidden
6	RWS	0h	Hide PCI Express downstream port 2 0: configuration space visible 1: configuration space hidden
5:2	RWS	0h	Reserved
1	RWS	1h	Reserved
0	RWS	1h	Reserved

13.4 PCI Express* Switch, Upstream/Downstream Port (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0) Enhanced

The enhanced PCI Express configuration access mechanism utilizes a flat memory-mapped address space to access device configuration registers. In this case, the memory address determines the configuration register accessed and the memory data returns the contents of the addressed register. Refer to the Section 7.9 in the *PCI Express* Base Specification, Revision 1.0a* for details.

13.4.1 Configuration Registers

13.4.1.1 Offset 100h: EXP_CAPID– PCI Express* Advanced Error Capability Identifier Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 100 – 103h Attribute: RO
Default Value: 00010001h Size: 32 bits

Note: This register stores the PCI Express extended capability ID value.

Bits	Type	Reset	Description
31:20	RO	000h	**Next PCI Express Extended Capability Pointer:** This is the last capability
19:16	RO	1h	**Capability Version Number:** PCI Express Advanced Error Reporting Extended Capability Version Number.
15:0	RO	0001h	**PCI Express Extended Capability ID (EXP_XCAPID):** PCI Express Extended Capability ID indicating Advanced Error Reporting Capability.

13.4.1.2 Offset 104h: ERRUNC_STS– PCI Express* Uncorrectable Error Status Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 104 – 107h
Default Value: 0000h
Attribute: RWCS, RO
Size: 32 bits

This register reports error status of individual errors generated on the PCI-X bus interface. An individual error status bit that is set to a 1 indicates that a particular error occurred; software may clear an error status by writing a 1 to the respective bit. Refer to Section 10 of the *PCI Express* to PCI/PCI-X* Bridge Specification Revision* 1.0 for more details.

Bits	Type	Reset	Description
31:21	RO	0	Reserved.
20	RWCS	0	**Unsupported Request Error Status:** Set by PCI Express Switch whenever an unsupported request is detected on PCI Express including those that master abort on the switch or signaled by the SHPC (on write data parity errors – config and mem)
19	RO	0	**ECRC Check:** PCI Express Switch does not do ECRC check and this bit is never set.
18	RWCS	0	**Malformed TLP:** PCI Express Switch sets this bit when it receives a malformed TLP. Header logging is done.
17	RWCS	0	**Receiver Overflow:** PCI Express Switch would set this if receive buffers overflow
16	RWCS	0	**Unexpected Completion:** PCI Express Switch sets this bit whenever it receives a completion with a requestor id that does not match or when it receives a completion with a matching requestor id but an unexpected tag field. PCI Express Switch logs the header of the unexpected completion
15	RWCS	0	**Completer Abort:** PCI Express Switch sets this bit and logs the header associated with the request when SHPC signals a completer abort. PCI Express Switch logs the header.
14	RWCS	0	**Completion Timeout:** PCI Express Switch sets this bit when inbound memory / config / I/O reads do not receive completions within 16-32ms.
13	RWCS	0	**Flow Control Protocol Error Status:** PCI Express Switch sets this bit when there is a flow control protocol error detected
12	RWCS	0	**Poisoned TLP Received:** PCI Express Switch sets this bit when a poisoned TLP is received from PCI Express. Note that internal queue errors in the J and B unit s are not covered by this bit. PCI Express Switch logs the header of the poisoned TLP packet.
11:5	RO	0	Reserved.
4	RWCS	0	**Data Link Protocol Error:** PCI Express Switch sets this bit when there is a data link protocol error detected.
3:1	RO	0	Reserved.
0	Undefined	Undefined	**Undefined –** The value read from this bit is undefined. In previous versions of this specification, this bit was used to indicate a Link Training Error. System software must ignore the value read from this bit. System software is permitted to write any value to this bit.

13.4.1.3 Offset 108h: ERRUNC_MSK– PCI Express* Uncorrectable Error Mask Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 108 – 10Bh
Default Value: 0000h
Attribute: RWCS, RO
Size: 32 bits

Bits	Type	Reset	Description
31:21	RO	0	Reserved.
20	RWS	0	Unsupported request Error Mask
19	RO	0	ECRC Check N/A to PCI Express Switch Mask

Bits	Type	Reset	Description
18	RWS	0	Malformed TLP Mask
17	RWS	0	Receiver overflow Mask
16	RWS	0	Unexpected completion Mask
15	RWS	0	Completer aborted Mask
14	RWS	0	Completion timeout mask
13	RWS	0	Flow control protocol error status mask
12	RWS	0	Poisoned TLP received mask
11:5	RO	0	Reserved.
4	RWS	0	Data Link Protocol Error Mask.
3:1	RO	0	Reserved
0	Undefined	Undefined	**Undefined –** The value read from this bit is undefined. In previous versions of this specification, this bit was used to indicate a Link Training Error. System software must ignore the value read from this bit. System software is permitted to write any value to this bit.

13.4.1.4 Offset 10Ch: ERRUNC_SEV– PCI Express* Uncorrectable Error Severity Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 10C – 10Fh Attribute: RWCS, RO
Default Value: 00061010h Size: 32 bits

Bits	Type	Reset	Description
31:21	RO	0	Reserved.
20	RWS	0	Unsupported Request Error Severity
19	RO	0	ECRC Check: N/A to PCI Express Switch Severity
18	RWS	1	Malformed TLP Severity
17	RWS	1	Receiver Overflow Severity
16	RWS	0	Unexpected Completion Severity
15	RWS	0	Completer Abort Severity
14	RWS	0	Completion Timeout Severity
13	RWS	1	Flow Control Protocol Error Severity
12	RWS	0	Poisoned TLP Received Severity
11:5	RO	0	Reserved.
4	RWS	1	Data link protocol error severity
3:1	RO	0	Reserved
0	Undefined	Undefined	**Undefined –** The value read from this bit is undefined. In previous versions of this specification, this bit was used to indicate a Link Training Error. System software must ignore the value read from this bit. System software is permitted to write any value to this bit.

13.4.1.5 Offset 110h: ERRCOR_STS– PCI Express* Correctable Error Status Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 110 – 113h
Default Value: 00000000h
Attribute: RWCS, RO
Size: 32 bits

Bits	Type	Reset	Description
31:13	RO	0	Reserved.
12	RWCS	0	Replay Timer Timeout Status:
11:9	RO	0	Reserved.
8	RWCS	0	**Replay Number Rollover Status:** The PCI Express Switch sets this bit when the replay number rolls over from 11 to 00.
7	RWCS	0	**Bad DLLP Status:** The PCI Express Switch sets this bit on CRC errors on DLLP.
6	RWCS	0	**Bad TLP Status:** The PCI Express Switch sets this bit on CRC errors on TLP.
5:1	RO	0	Reserved.
0	RWCS	0	**Receiver Error:** The PCI Express Switch sets this bit when the physical layer detects a receiver error.

13.4.1.6 Offset 114h: PCI ExpressERRUNC_MSK– PCI Express* Correctable Error Mask Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 114 – 117h
Default Value: 00000000h
Attribute: RWS, RO
Size: 32 bits

This register masks the reporting of individual PCI Express correctable errors via a PCI Express error message. There is one mask bit per error. Note that the status bits are set in the status register irrespective of whether the mask bit is on or off. The mask bit also affects the header log for the PCI Express transaction. If the mask bit is on, the header is not logged and no error message is generated on the PCI Express bus.

Bits	Type	Reset	Description
31:13	RO	0	Reserved.
12	RWS	0	**Replay Timer Timeout Mask:** The PCI Express Switch sets this bit if replay timer timeout happened.
11:9	RO	0	Reserved.
8	RWS	0	**Replay Number Rollover Mask:** The PCI Express Switch sets this bit when the replay number rolls over from 11 to 00.
7	RWS	0	**Bad DLLP Mask:** The PCI Express Switch sets this bit on CRC errors on DLLP.
6	RWS	0	**Bad TLP Mask:** The PCI Express Switch sets this bit on CRC errors on TLP.
5:1	RO	0	Reserved.
0	RWS	0	**Receiver Error Mask: PCI Express Switch sets this bit when the physical layer detects a receiver error.**

13.4.1.7 Offset 118h: ADVERR_CTL– Advanced Error Control and Capabilities Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 118 – 11Bh
Default Value: 00000000h
Attribute: RWS, RO
Size: 32 bits

This register masks the reporting of individual PCI Express correctable errors via a PCI Express error message. There is one mask bit per error. Note that the status bits are set in the status register irrespective of whether the mask bit is on or off. The mask bit also affects the header log for the PCI Express transaction. If the mask bit is on, the header is not logged and no error message is generated on the PCI Express bus.

Bits	Type	Reset	Description
31:9	RO	0	Reserved.
8	RO	0	**ECRC Check Enable:** The PCI Express Switch does not support ECRC check and this bit is Reserved.
7	RO	0	**ECRC Check Capable:** The PCI Express Switch is not ECRC check capable.
6	RO	0	**ECRC Check Enable:** The PCI Express Switch is not ECRC check capable.
5	RO	0	**ECRC Generation Capable:** The PCI Express Switch cannot generate ECRC.
4:0	ROS	0	The First Error Pointer – Identifies the bit position of the first error reported in the Uncorrectable Error Status register. This register rearms itself (which does not change its current value) once the error status bit pointed to by the pointer is cleared by software by writing a 1 to that status bit.

13.4.1.8 Offset 11Ch: EXPHDRLOG– PCI Express* Transaction Header Log Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 11C – 12Bh Attribute: RWCS, RO
Default Value: 0000h Size: 128 bits.

Bits	Type	Reset	Description
127:0	ROS	0	Header of the PCI Express packet in error. Once an error is logged in this register, it remains locked for further error loggings until the time the software clears the status bit that cause the header log, that is, the error pointer is rearmed to log again.

13.4.1.9 Offset 170h: PEXH_STS – Intel® 631xESB/632xESB I/O Controller Hub PCI Express* to PCI-X Bridge Strap Status Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset: 170 – 171h Attribute: RO
Default Value: xxxxh Size: 16 bits

This register indicates the status of various Power-On straps on Intel® 631xESB/ 632xESB I/O Controller Hub PCI Express Switch and Bridge.

Bits	Type	Reset	Description
15	RO	0	Reserved.
14	RO	Strap	Reserved.
13:12	RO	0	Reserved.
11:8	RO	Strap	**PCI Slot Count (PSC):** Reflects the value of the HPxSLOT[3:0]# pins sampled at the rising edge of PWROK.
7:1	RO	Strap	**Manageability Address (MA):** These 7 bits represent the address the SMBus slave port will respond to when an access is attempted. This register will have the following value: Bit Value 7 '1' 6 '1' 5 SMBUS[5] 4 '0' 3 SMBUS[3] 2 SMBUS[2] 1 SMBUS[1]
0	RO	Strap	**P133EN Status (133EN_STS):** Reflects the status of the Px133EN pin sampled at rising edge of PWROK. This serves as a dashboard for the BIOS.

13.4.1.10 Offset 172h: PXB_STRAP – Intel® 631xESB/632xESB I/O Controller Hub PCI Express* Upstream and Downstream Strap Status Register (Bm:D0:F0,Bp:D0:F0,Bp:D1:F0,Bp:D2:F0)

Offset:	172h	Attribute:	RO
Default Value:	xxh	Size:	8 bits

THIS REGISTER RESIDES IN THE UPSTREAM PORT ONLY. For the downstream ports these bits are disabled.

This register stores the switch port strap values captured at power-up-reset from the SMBUS pins.

Bits	Type	Reset	Description
7:3	RO	0	Reserved.
2	RO	Strap	**South Strap -** SMBUS[2] 0: One PCI Express South x8 port (Option may not exist, depending on SKU). 1: Two PCI Express South x4 ports (port E1 and E2, where port E2 could be fused off depending on the SKU). When the PCI Express to PCI-X Bridge south ports are put in x8 mode, PE1 lanes 3:0 stay the same, and PE2 lanes 3:0 become PE1 lanes 7:4.
1:0	RO	Strap	**North Straps -** SMBUS[1:0] 00: One PCI Express North x8 port 01: Reserved 10: Two PCI Express North x4 ports Relative to the single x8 port, -- Lanes 3:0 no change. -- Lanes 7:4 become new x4 port, direct-connect to LAN. 11: Reserved

13.5 I/OxAPIC Interrupt Controller Registers (Bm:D0:F1)

The Intel® 631xESB/632xESB I/O Controller Hub contains one I/OxAPIC controllers which resides on the Bus m: Device 0: Function 1. This integrated I/OxAPIC supports only FSB interrupt delivery. Interrupts are delivered as interrupt message transactions on the processor system bus.

13.5.1 PCI Configuration Space Registers

Table 13-2. Configuration Register Summary (Sheet 1 of 2)

Address Offset	Symbol	Register Name	Default	Access
00–01h	VID	Vendor ID Register	8086h	RO
02–03h	DID	Device ID Register	3504h -3507h	RO
04–05h	PCICMD	Command Register	0000h	RW, RO
06–07h	PCISTS	Status Register	0030h	RWC, RO
08h	RID	Revision ID Register	00h	RO
09–0Bh	CC	Class Code Register	080020h	RO
0Ch	CLS	Cache Line Size Register	00h	RW
0Dh	PLT	Primary Latency Timer Register	00h	RW
0Eh	HTYPE	Header Type Register	00h	RO

Table 13-2. Configuration Register Summary (Sheet 2 of 2)

Address Offset	Symbol	Register Name	Default	Access
10–13h	MBAR	Memory Base Address Register	see register desc.	RW, RO
2C-2Fh	SSID	Subsystem Identifier Register	00h	RWO
34h	CAPP	Capabilities Pointer Register	44h	RWO
40-41h	ABAR	Alternate Base Address Register	00h	RW,RO
44h	EXP_CAPID	PCI Express Capability Identifier Register	10h	RO
45h	EXP_NXTP	Next Item Pointer Register	5Ch	RO
46-47h	EXP_CAP	PCI Express Capability Register	0001h	RO
48-4Bh	EXP_DEVCAP	PCI Express Device Capabilities Register	00000001h	RO
4C-4Dh	EXP_DEVCNTL	PCI Express Device Control Register	0020h	RW, RO
4E-4F	EXP_DEVSTS	PCI Express Device Status Register	0000	RWC, RO
50-53h	EXP_LCAP	PCI Express Link Capabilities Register	0003E081h	RO
54-55h	EXP_LCNTL	PCI Express Link Control Register	0000h	RW, RO
56-57h	EXP_LSTS	PCI Express Link Status Register	0000	RO
6Ch	PM_CAPID	Power Management Capability Identifier Register	00x0oh	RO
6Dh	PM_NXTPTR	Power Management Next Pointer	00	RO
6E-6Fh	PM_CAP	Power Management Capabilities Register	0002h	RO
70-71h	PM_CNTLSTS	Power Management Control and Status Register	0000h	RW,RO

13.5.1.1 Offset 00h: VID-Vendor ID Register (Bm:D0: F1)

Offset: 00-01h Attribute: RO
Default Value: 8086h Size: 16 bits

This register contains the Vendor Identifiers.

Bits	Type	Reset	Description
15:0	RO	8086h	**Vendor ID (VID):** 16-bit field which indicates that Intel is the vendor

13.5.1.2 Offset 02h: DID—Device ID Register (Bm:D0:F1)

Offset: 02–03h Attribute: RO
Default Value: 3504h - 3507h (Function 1) Size: 16 bits

Bits	Type	Reset	Description
15:0	RO	3504h – 3507h depending on SKU.	**Device ID (DID):** Device number of the Intel Intel® 631xESB/632xESB I/O Controller Hub IOxAPIC (Bm:D0:F1).

13.5.1.3 Offset 04h: PCICMD—PCI Command Register (Bm:D0:F1)

Offset: 04–05h
Default Value: 0000h
Attribute: RW, RO
Size: 16 bits

Bits	Type	Reset	Description
15:9	RO	0	Reserved.
8	RW	0	**SERR Enable (SEE):** Controls the enable for PCI-compatible SERR reporting on the PCI Express interface (along with the Status Register (STS REG, offset 06h, bit 14). 0 = Disable SERR reporting 1 = Enable SERR reporting Note that this bit does not affect the setting of the PCI Express error bits in the PCI Express Capability Structure.
7	RO	0	**Wait Cycle Control (WCC):** Reserved.
6	RW	0	**Parity Error Response (PER):** Controls the response to data parity errors forwarded from the PCI Express interface and peer PCI on read completions. 0 = Disable. Ignore errors on the PCI Express interface and the peer-PCI interface. 1 = Enable. Report read completion data parity errors on the PCI E interface and set the Master Data Parity Detected (MDPD) bit in the status register. Note that this bit does not affect the setting of the PCI Express error bits in the PCI Express Capability Structure.
5	RO	0	**VGA Palette Snoop (VGA_PS):** Reserved.
4	RO	0	**Memory Write and Invalidate (MWIE):** The Intel® 631xESB/632xESB I/O Controller Hub does not generate memory write and invalidate transactions, as the PCI Express interface does not have a corresponding transfer type.
3	RO	0	**Special Cycle Enable (SCE):** Reserved.
2	RW	0	**Bus Master Enable (BME):** Controls the I/OxAPIC's ability to act as a master on PCI Express when forwarding system bus interrupt. Note that this bit does not stop the Intel® 631xESB/632xESB I/O Controller Hub IOxAPIC (Bm:D0:F1) from issuing completions on PCI Express 0 = Disable. Don't respond to any memory transactions on the PCI interface that target the PCI Express interface. 1 = Enable.Requests other than memory or I/O requests are not controlled by this bit.
1	RW	0	**Memory Space Enable (MSE):** Controls the I/OxAPIC's response as a target to memory accesses on the PCI Express interface that address the I/OxAPIC. 0 = These transactions are master aborted on the PCI Express interface. 1 = To allowed memory transaction from PCI to be passed to the PCI Express.
0	RO	0	**I/O Space Enable (IOSE):** Reserved

13.5.1.4 Offset 06h: PCISTS—Status Register (Bm:D0:F1)

Offset: 06–07h
Default Value: 0010h
Attribute: RWC, RO
Size: 16 bits

Bits	Type	Reset	Description
15	RWC	0	Detected Parity Error (DPE): 0 = Software clears this bit by writing a 1 to it. 1 = Data parity error on the PCI Express bus interface or peer PCI segment is detected. This bit gets set even if the Parity Error Response (bit 6 of the command register) is not set. Indicates that a parity error was detected on cycles targeting the I/OxAPIC.
14	RWC	0	**Signaled System Error (SSE):** Set whenever an ERR_FATAL or ERR_NONFATAL message is sent on PCI Express for data parity errors to I/OxAPIC configuration or memory space and the SERR enable bit (bit 8 in PCICMD) is set. This bit is also set on error messages generated on PCI Express for errors not specific to a function. 0 = These transactions are master aborted on the PCI Express interface. 1 = The Intel® 631xESB/632xESB I/O Controller Hub IOxAPIC (Bm:D0:F1) is allowed to accept cycles from PCI to be passed to the PCI Express interface.
13	RO	0	Received Master-Abort (RMA): Reserved
12	RO	0	Received Target-Abort (RTA): Reserved
11	RWC	0	1 = Signaled Target Abort (STA): This bit reports the signaling of a Target-Abort termination by the Intel® 631xESB/632xESB I/O Controller Hub IOxAPIC (Bm:D0:F1) when it responds as the target of a transaction on the PCI/PCI-X interface or when the PCI Express to PCI-X bridge signals a PCI-X Split Completion Message with Target Abort. 0 = Target Abort not signaled on the PCI/PCI-X interface. 1 = Target Abort signaled on the PCI/PCI-X interface. Software clears this bit by writing a 1 to it.
10:9	RO	0	**DEVSEL# Timing (DVT):** A value of 0 indicates that fast decode is performed by the I/OxAPIC.
8	RO	0	Master Data Parity Error (MDP): Reserved
7	RO	0	**Fast Back-to-Back Transactions Capable (FBC):** Reserved as not fast back-to-back capable.
6	RO	0	Reserved.
5	RO	0	**66 MHz Enable (66EN):** A value of 1 indicates that the I/OxAPIC is 66 MHz capable
4	RO	1	**Capabilities List (CAPL):** Indicates that the PCI Express to PCI-X bridge contains the capabilities pointer in the bridge. Offset 34h (Capabilities List Pointer - CAPP) indicates the offset for the first entry in the linked list of capabilities. Default = 1.
3:0	RO	0	Reserved.

13.5.1.5 Offset 08h: RID—Revision ID Register (Bm:D0:F1)

Offset: 08h
Default Value: 00h
Attribute: RO
Size: 8 bits

Bits	Type	Reset	Description
7:0	RO	A0-00h A1-00h	**Revision ID (REVID):** This indicates the stepping of the IOxAPIC of the PCI Express-to-PCI-X bridge. “00/04/08” indicate the A-0/B-0/C-0 steppings

13.5.1.6 Offset 09h: CC—Class Code Register (Bm:D0:F1)

Offset: 09–0Bh Attribute: RO
Default Value: 080020h Size: 24 bits

This contains the class code, sub class code, and programming interface for the device.

Bits	Type	Reset	Description
23:16	RO	08h	**Base Class Code (BCC):** The value of '08h' indicates that this is a generic system peripheral.
15:8	ROS	0h	**Sub Class Code (SCC):** The value of '00h' indicates that this generic peripheral is an interrupt controller.
7:0	RO	20h	**Programming Interface (PIF):** The value of '20h' indicates that this interrupt peripheral is an I/OxAPIC.

13.5.1.7 Offset 0Ch: CLS—Cache Line Size Register (Bm:D0:F1)

Offset: 0Ch Attribute: RW
Default Value: 00h Size: 8 bits

This indicates the cache line size of the system.

Bits	Type	Reset	Description
7:0	RO	0	Cache Line Size (CLS): Reserved.

13.5.1.8 Offset 0Dh: MLAT—Master Latency Timer Register (Bm:D0:F1)

Offset: 0Dh Attribute: RW
Default Value: 00h Size: 8 bits

This register does not apply to the PCI Express interface.

Bits	Type	Reset	Description
7:0	RO	0	**Latency Time:** Reserved.

13.5.1.9 Offset 0Eh: HTYP—Header Type Register (Bm:D0:F1)

Offset: 0Eh Attribute: RW
Default Value: 81h Size: 8 bits

This register is used to indicate the layout for bytes 10h through 3Fh of the device's configuration space.

Bits	Type	Reset	Description
7:0	RO	00h	**Header Type (HTYPE):** This indicates that it is a type "00" header (normal PCI device) and that it is part of a multi-function device.

13.5.1.10 Offset 0Fh: BIST—Built-in Self-Test Register (Bm:D0:F1)

Offset: 0Fh Attribute: RW
Default Value: 81h Size: 8 bits

This register is used to indicate the layout for bytes 10h through 3Fh of the device's configuration space.

Bits	Type	Reset	Description
7:0	RO	00h	Built-In Self-Test (BIST): Reserved.

13.5.1.11 Offset 10h: MBAR—Memory Base Register (Bm:D0:F1)

Offset: 10-13h Attribute: RW, RO
Default Value: 00000000h Size: 32 bits

This register contains the I/OxAPIC Base Address for the I/OxAPIC memory space.

Bits	Type	Reset	Description
31:12	RW	0	**Address (ADDR):** These bits determine the base address of the I/OxAPIC.
11:4	RO	0	Reserved.
3	RO	0	Prefetchable (PF): Indicates that the BAR is not pre-fetchable.
2:1	RO	10b	**Location (LOC):** '00' indicates that the address can be located anywhere in the 32-bit address space
0	RO	0	Memory Space Indicator (MEMSI): This bit is a read-only 0 indicating that this Base Address Register maps into memory space.

13.5.1.12 Offset 2Ch: SS—Subsystem Identifier Register (Bm:D0:F1)

Offset: 2C-2Fh Attribute: RW
Default Value: 00000000h Size: 32 bits

This register is initialized to logic 0 by the assertion of PxPCIRST#. This register can be written only once after PxPCIRST# deassertion.

Bits	Type	Reset	Description
31:16	RWOS	0	**Subsystem ID (SSID):** Write once register for sub-system ID.
15:0	RWOS	0	**Subsystem Vendor ID (SSVID):** Write once register for holding the subsystem vendor ID.

13.5.1.13 Offset 34h: CAPP—Capabilities Pointer Register (Bm:D0:F1)

Offset: 34h Attribute: RO
Default Value: 44h Size: 8 bits

Bits	Type	Reset	Description
7:0	RO	44	**Capabilities Pointer (CAPP):** Indicates the presence of the PCI Express capability list item.

13.5.1.14 Offset 40h: ABAR—Alternate Base Address Register (Bm:D0:F1)

Offset: 40-41h Attribute: RW,RO
Default Value: 0000h Size: 16 bits

This register contains an alternate base address in the legacy I/OxAPIC range. This range can co-exist with the BAR register range. This range is needed for Operating Systems that support the legacy I/OxAPIC mapping, but do not yet support remapping the I/OxAPIC anywhere in the 4GB address space.

Bits	Type	Reset	Description
15	RW	0	**Enable (EN):** When set, the range FECX_YZ00 to FECX_YZFF is enabled as an alternate access method to the I/OxAPIC registers. Bits 'XYZ' are defined below.
14:12	RO	0	Reserved

Bits	Type	Reset	Description
11:8	RW	0	**Base Address [19:16] (XBAD)**: These bits determine the high order bits of the I/O APIC address map. When a memory address is recognized and matches FECX_YZ00 to FECX_YZFF, it will respond to the cycle and access the internal I/O APIC.
7:4	RW	0	**Base Address [15:12] (YBAD):** These bits determine the low order bits of the I/O APIC address map. When a memory address is recognized and matches FECX_YZ00 to FECX_YZFF, it will respond to the cycle and access the internal I/O APIC.
3:0	RW	0	**Base Address [11:8] (ZBAD):** These bits determine the low order bits of the I/O APIC address map. When a memory address is recognized and matches FECX_YZ00 to FECX_YZFF, it respond to the cycle and access the internal I/O APIC.

13.5.1.15 Offset 44h: EXP_CAPID—PCI Express* Capability Identifier Register (Bm:D0:F1)

Offset: 44h
Default Value: 10h
Attribute: RO
Size: 8 bits

Bits	Type	Reset	Description
7:0	RO	10h	**PCI Express Capability ID (PECID):** Indicates PCI Express capability

13.5.1.16 Offset 45h: EXP_NXTP—PCI Express* Next Pointer Register (Bm:D0:F1)

Offset: 45h
Default Value: 6Ch
Attribute: RO
Size: 8 bits

Bits	Type	Reset	Description
7:0	RW	6Ch	**Next Pointer (MNPTR):** Points to the next capabilities list pointer, which is the MSI capability.

13.5.1.17 Offset 46: EXP_CAP—PCI Express* Capability Register (Bm:D0:F1)

Offset: 46-47h
Default Value: 0001h
Attribute: RO
Size: 16 bits

This register carries the version number of the capability item and other base information contained in the PCI Express capability structure.

Bits	Type	Reset	Description
15:14	RO	0	Reserved.
13:9	RO	0	Interrupt Message Number (IMN): Not relevant for I/OxAPIC.
11:8	RO	0	Slot Implemented (SLOTI): Not relevant for I/OxAPIC.
7:4	RO	0	**Device/Port Type (DPT):** Indicated PCI Express end-point device.
3:0	RO	01h	**Version Number (VN):** Indicates PCI Express capability structure version number.

13.5.1.18 Offset 48h: EXP_DCAP—PCI Express* Device Capability Register (Bm:D0:F1)

Offset: 48-4Bh
Attribute: RO
Default Value: 00000001h
Size: 32 bits

This register identifies PCI Express device specific capabilities.

Bits	Type	Reset	Description
31:28	RO	0	Reserved.
27:26	RO	0	**Captured Slot Power Limit Scale (CSPLS):** Specifies the scale used for the Slot Power Limit Value.Range of Values: 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x This value is set by the Set_Slot_Power_Limit message. In combination with the Slot Power Limit value, specifies the upper limit on power supplied by slot. Power limit (in Watts) calculated by multiplying the value in this field by the value in the Slot Power Limit Value field. Hard wired to 0.
25:18	RO	0	**Captured Slot Power Limit Value (CSPLV):** In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot. Power limit (in Watts) calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field. This value is set by the Set_Slot_Power_Limit message. Hard wired to 0.
17:12	RO	0	Reserved.
11:9	RO	0	**Endpoint L1s Acceptable Latency (EL1AL):** Intel® 6700PXH 64-bit PCI Hub does not support L1 Link State Power Management (LSPM).
8:6	RO	0	**Endpoint L0s Acceptable Latency (EL0AL):** Intel® 6700PXH 64-bit PCI Hub wants the least latency possible out of L0s
5	RO	0	**Extended Tag Field Supported (ETFS):** Intel® 6700PXH 64-bit PCI Hub supports only a 5-bit tag.
4:3	RO	0	**Phantom Functions Supported (PFS):** Intel® 6700PXH 64-bit PCI Hub does not support phantom functions.
2:0	RO	001b	**MaX_ Payload_Size Supported (MPSS):** This field is set to a value of 001b, signifying that Intel® 6700PXH 64-bit PCI Hub supports a maximum payload size of 256 byte packets.

13.5.1.19 Offset 4Ch: DEVCNTL—Device Control Register (Bm:D0:F1)

Offset: 4C-4Dh
Attribute: RW, RO
Default Value: 0020h
Size: 16 bits

This register controls PCI Express device specific (Intel® 631xESB/632xESB I/O Controller Hub IOxAPIC (Bm:D0:F1)) parameters

Bits	Type	Reset	Description
15	RO	0	Reserved.
14:12	RO	0	MaX_Read_Request_Size (MRRS): Does not apply to the I/OxAPIC.
11	RO	0	Enable No Snoop (ENS): This does not apply to Intel® 6700PXH 64-bit PCI Hub since it does not set the NS bit on MSI Transactions it generates.
10	RO	0	Auxiliary (AUX) Power PM Enable (AUXPPME): Intel® 6700PXH 64-bit PCI Hub ignores this bit since it does not support auxiliary power.
9	RO	0	Phantom Function Enable (PFE): Intel® 6700PXH 64-bit PCI Hub ignores this bit since it does not support phantom functions.
8	RO	0	Extended Tag Field Enable (ETFE): Intel® 6700PXH 64-bit PCI Hub ignores this bit since it supports only 5-bit tag.

Bits	Type	Reset	Description
7:5	RW	001b	MaX_ Payload_Size (MPS): Does not affect the I/OxAPIC since it does not do writes greater than a DWORD.
4	RO	0	Enable Relaxed Ordering (ERO): Not applicable or used by the I/OxAPIC.
3	RW	0	Unsupported Request Reporting Enable (URRE): This bit enables reporting of Unsupported Requests when set to a 1. It is used by the I/OxAPIC to enable reporting of ERR_FATAL or ERR_NONFATAL messages on the PCI Express interface for reporting Unsupported Requests errors, such as data parity errors on writes to the I/OxAPIC (configuration or memory space). Refer to Section 6.2 of the *PCI Express Base Specification Revision 1.0a* for further details.
2	RW	0	Fatal Error Reporting Enable (FERE): This bit controls reporting of fatal errors. Used by the I/OxAPIC to gate the generation of the ERR_FATAL message on data parity errors to it: 0 = Disable. 1 = Report fatal errors. Refer to Section 6.2 of the *PCI Express Base Specification, Revision 1.0a* for further details.
1	RW	0	Non-Fatal Error Reporting Enable (NFERE): This bit controls reporting of non-fatal errors. Used by I/OxAPIC to gate the generation of the ERR_NONFATAL message on data parity errors to it. 0 = Disable. 1 = Report non-fatal errors. Refer to Section 6.2 of the *PCI Express Base Specification, Revision 1.0a* for further details.
0	RW	0	Correctable Error Reporting Enable (CERE): This bit controls reporting of correctable errors. When set to “1”, the Intel® 631xESB/632xESB I/O Controller Hub IOxAPIC (Bm:D0:F1) is enabled to generate ERR_CORR message on PCI Express. Not used by I/OxAPIC in normal operation. 0 = Disable. 1 = Report correctable errors.

13.5.1.20 Offset 4Eh: DSTS—Device Status Register (Bm:D0:F1)

Offset: 4E-4Fh Attribute: RWC, RWO
Default Value: 00h Size: 16 bits

This register provides information on specific parameters of a PCI Express device.

Bits	Type	Reset	Description
15:6	RO	0	Reserved.
5	RO	0	Transactions Pending (TP): Reserved.
4	RO	0	Aux Power Detected (AUXPD): Intel® 631xESB/632xESB I/O Controller Hub IOxAPIC (Bm:D0:F1) does not support aux power and hence this bit is reserved.
3	RO	0	**Unsupported Request Detected (URD):** This bit indicates that Intel® 6700PXH 64-bit PCI Hub received an Unsupported request. The I/OxAPIC will set this bit whenever it receives a configuration or memory write with bad parity. It is also set on link unsupported request errors that are not specific to any function within Intel® 6700PXH 64-bit PCI Hub.
2	RWC	0	**Fatal Error Detected (FED):** The I/OxAPIC does not set this bit on its own, but rather it is set on link fatal errors.
1	RWC	0	**Non-Fatal Error Detected (NFED):** The I/OxAPIC sets this bit whenever it detects a write to I/OxAPIC (configuration or memory space) with bad data parity. This bit is also set on link uncorrectable errors that are not specific to any functions.
0	RWC	0	**Correctable Error Detected (CED):** The I/OxAPIC does not set this bit on its own, but rather it is set on link correctable errors.

13.5.1.21 Offset 50h: LCAP—Link Capabilities Register (Bm:D0:F1)

Offset: 50-53h Attribute: RO
Default Value: 0003E081h Size: 32 bits

This register identifies PCI Express link specific capabilities.

Bits	Type	Reset	Description
31:24	RO	0	Port Number (PNUM): Not applicable, reserved to zero.
23:18	RO	0	Reserved.
17:15	RO	0	**L1 Exit Latency (L1XL)**: L1 transition is not supported.
14:12	RO	0	**L0 Exit Latency (L0XL):** L0s Exit Latency: The value in these bits is influenced by the PCI reference clock configuration in Intel® 631xESB/ 632xESB I/O Controller Hub IOxAPIC (Bm:D0:F1), since the reference clock is configured as a common clock. Because it is a common clock configuration, the Common Clock Configuration bit (CCC, bit 6) in the Link Control register (LCTL, offset 54h) is set to a 1. The mapping is shown below: Bit 6 PCI Express Link Control Link Capabilities Bits 14:12 0 110b = 2-4µs. 1 010b = 128ms to less than 256ms
11:10	RO	01	**Active State Link PM Support (ASLPMS):** Indicates the level of active state power management supported on the given PCI Express link. The PCI-SIG defined encodings are as follows: 01 Enters L0s per the specified requirements for L0s entry.
9:4	RO	8h	**Maximum Link Width (MLW):** Intel® 631xESB/632xESB I/O Controller Hub IOxAPIC (Bm:D0:F1) supports a maximum PCI Express link width of x8, so this field is set to the PCI-SIG defined value for x8, which is 001000 b, or 8h.
3:0	RO	0001	**Maximum Link Speed (MLS):** Intel® 631xESB/632xESB I/O Controller Hub IOxAPIC (Bm:D0:F1) supports a PCI Express link speed of 2.5 Gbps only, so this field is set to the PCI-SIG defined value for 2.5 Gbps, which is 0001b, or 1h.

13.5.1.22 Offset 54h: LCTL—Link Control Register (Bm:D0:F1)

Offset: 54-55h Attribute: RW; RO
Default Value: 0000h Size: 16 bits

This register controls PCI Express link specific parameters.

Bits	Type	Reset	Description
15:7	RO	0	Reserved.
6	RW	0	**Common Clock Configuration (CCC):** This bit when set indicates that IOxAPIC (Bm:D0:F1) and the component it is connected to via the PCI Express link (located at the opposite end of this link) are operating with a distributed common reference clock. A value of 0 indicates that this component and the component at the opposite end of this Link are operating with an asynchronous reference clock. 0 = Intel® 631xESB/632xESB I/O Controller Hub IOxAPIC (Bm:D0:F1) and the other PCI Express component have an asynchronous reference clock. 1 = Intel® 631xESB/632xESB I/O Controller Hub IOxAPIC (Bm:D0:F1) and the other PCI Express component share a common clock. Note that this bit is used to reflect the proper L0s exit latency value in the EXP_LSTS register.
5:4	RO	0	Reserved.

Bits	Type	Reset	Description
3	RO	0	Read Request Return Parameter Control (RRRPC): Not used by the I/OxAPIC.
2	RO	0	Reserved.
1:0	RW	0	**Active State Link PM Control (ASLPMC):** Controls the level of active state Power Management supported on the given PCI Express link. The PCI-SIG defined encodings are as follows: 00bDisabled 01bL0s entry supported 10bReserved 11bL0s and L1s entry supported These bits enable Intel® 631xESB/632xESB I/O Controller Hub IOxAPIC (Bm:D0:F1) to enter L0s. Not used by I/OxAPIC in normal operation.

13.5.1.23 Offset 56h LSTS—Link Status Register (Bm:D0:F1)

Offset: 56-57h
Default Value: 0041h(X4 Link 0081h(X8 Link)
Attribute: RO
Size: 16 bits

This register provides information about PCI Express link specific parameters.

Bits	Type	Reset	Description
15:10	RO	0	Reserved.
9:4	RO	4h or 8h	**Negotiated Link Width (NLW):** Indicates the negotiated width of PCI Express Link. Defined encodings are: 000100b X4 width 001000b X8 width
3:0	RO	1h	**Link Speed (LS):** Supports a PCI Express link speed of 2.5 Gbps only, so this field is set to the PCI-SIG defined value for 2.5 Gbps, which is 0001b, or 1h.

13.5.1.24 Offset 6Ch: PM_CAPID – Power Management Capability Identifier Register

Offset: 6Ch
Default Value: 00h
Attribute: RW
Size: 8 bits

This register provides information about PCI Express link specific parameters.

Bits	Type	Reset	Description
7:0	RO	01h	**Capability ID (CAP_ID):** Capability ID indicates PCI compatible Power Management.

13.5.1.25 Offset 6Dh: PM_NXTPTR – Power Management Next Pointer

Offset: 6Dh
Default Value: 00h
Attribute: RW
Size: 8 bits

This register provides information about PCI Express link specific parameters.

Bits	Type	Reset	Description
7:0	RO	0	**Next Pointer (NXTPTR):** Next Pointer if non-zero.

13.5.1.26 Offset 6Eh: PM_CAP – Power Management Capabilities Register

Offset: 6E-6Fh
Default Value: 0002h
Attribute: RO
Size: 16 bits

This register provides information about PCI Express link specific parameters.

Bits	Type	Reset	Description
15:3	RO	0	Reserved.
2:0	RO	10b	**Version (VERS):** I/OxAPIC Power Management implementation is compliant with the *PCI Power Management Specification Revision 1.1*.

13.5.1.27 Offset 70h: PM_CNTLSTS – Power Management Control and Status Register

Offset: 70-71h
Default Value: 00h
Attribute: RW
Size: 16 bits

This register provides information about PCI Express link specific parameters.

Bits	Type	Reset	Description
15:2	RO	0	Reserved.
1:0	RW	0	**PowerState (PWR_ST):** This 2-bit field is used both to determine the current power state of a function and to set the function into a new power state. The I/OxAPIC supported field values are given below. 00b – D0 01b – Reserved 10b – Reserved 11b – D3hot If software attempts to write an unsupported, optional state to this field, the write operation must complete normally on the bus; however, the data is discarded and no state change occurs. When in D3hot state, the I/OxAPIC responds to configuration transactions only and a transition from D3hot to D0 does not reset the I/OxAPIC's registers. Also, in D3hot state, the I/OxAPIC cannot generate any MSI. Virtual wire interrupts generated by the I/OxAPIC on behalf of PCI agents/SHPC are not masked by the D3hot state.

13.5.2 I/OxAPIC Direct Memory Space Registers

13.5.2.1 Register Summary

Offset Address	Symbol	Full Name	Default	Attribute
00h	IDX	Index Register	00h	RW
10–13h	WND	Window Register	00000000h	RW
20h	PAR	IRQ Pin Assertion Register	000000xxh	RW, RO
40h	EOI	EOI Register	00h	RW

13.5.2.2 Offset 00h: IDX—Index Register

Offset: 00h Attribute: RW
Default Value: 00h Size: 8 bits

The Index Register will select which indirect register appears in the window register to be manipulated by software. Software will program this register to select the desired I/OxAPIC internal register.

Bits	Type	Reset	Description
7:0	RW	0	**Index (IDX):** Indirect register to access.

13.5.2.3 Offset 10h: WND—Window Register

Offset: 10–13h Attribute: RW
Default Value: 00000000h Size: 32 bits

This is a 32-bit register specifying the data to be read or written to the register pointed to by the Register Select register. This register can be accessed in byte quantities.

Bits	Type	Reset	Description
31:0	RW	0	**Window (WND):** Data to be written to the indirect register on writes, and location of register data from the indirect register on reads.

13.5.2.4 Offset 20h: PAR—IRQ Pin Assertion Register

Offset: 20h Attribute: RW, RO
Default Value: 000000xxh Size: 32 bits

The IRQ Pin Assertion Register is present to provide a mechanism to scale the number of interrupt inputs into the I/Ox APIC without increasing the number of dedicated input pins. When a device that supports this interrupt assertion protocol requires interrupt service, that device will issue a write to this register. Bits [4:0] written to this register contain the IRQ number for this interrupt. The only valid values are 0–23.

Bits	Type	Reset	Description
31:5	RO	0	Reserved.
4:0	RW	xx	**Assertion (PAR):** Virtual pin to be asserted (active high). Writes to this register are treated with edge triggered semantics regardless of what is programmed in the RDL DWord, though the interrupt message is generated directly from the contents of the RDL and RDH DWords.

13.5.2.5 Offset 40h: EOI—EOI Register

Offset: 40h Attribute: RW
Default Value: 00h Size: 8 bits

The EOI register is present to provide a mechanism to maintain the level triggered semantics for level-triggered interrupts issued on the parallel bus.

When a write is issued to this register, the I/Ox APIC will check the lower 8 bits written to this register, and compare it with the vector field for each entry in the I/O Redirection Table. When a match is found, the Remote_IRR bit for that I/O Redirection Entry will be cleared.

Note that if multiple I/O Redirection entries, for any reason, assign the same vector for more than one interrupt input, each of those entries will have the Remote_IRR bit reset to '0'.

Bits	Type	Reset	Description
7:0	RW	0h	**End of Interrupt (EOI):** Vector to be cleared by the EOI.

13.5.3 Indirect Memory Space Registers

13.5.3.1 Register Summary

To access the indirect memory space, an 8-bit value must be written to the index register, which is a "pointer" (indirect) to a 32-bit memory location. The 32-bit value in the Window Register can then be read.

Table 13-3. Indirect Memory Space Registers Summary

Address Offset	Symbol	Full Name	Default	Attribute
00h	ID	APIC ID Register	00000000h	RW, RO
01h	VS	Version Register	00170020h	RO
03h	BCFG	Boot Configuration Register	00000001h	RW, RO
10h	RDL[0]	Redirection Table Low DWord 0 Register	00010000h	RW, RO
11h	RDH[0]	Redirection Table High DWord 0 Register	00000000h	RW, RO
3E	RDL[23]	Redirection Table Low DWord 23 Register	00010000h	RW, RO
3F	RDH[23]	Redirection Table High DWord 23 Register	00000000h	RW, RO
40-FF	Reserved	Reserved.	00000000h	RO

13.5.3.2 Offset 00h: ID—APIC ID Register

Offset: 00h Attribute: RW, RO
Default Value: 00000000h Size: 32 bits

The APIC ID serves as a physical name of the APIC. The APIC bus arbitration ID for the APIC is derived from its I/OxAPIC ID. This register is reset to zero on power up reset.

Bits	Type	Reset	Description
31:28	RO	0	Reserved.
27:24	RW	0	**I/OxAPIC ID (APICID):** Software must program this value before using the I/OxAPIC.
23:0	RO	0	Reserved.

13.5.3.3 Offset 01h: VS—Version Register

Offset: 01h Attribute: RO
Default Value: 00178020h Size: 32 bits

Contains information related to this I/OxAPIC for driver/OS/software.

Bits	Type	Reset	Description
31:24	RO	0	Reserved.
23:16	RO	17h	**Maximum Redirection Entries (MAX):** This is the entry number of the highest entry in the redirection table. It is equal to the number of interrupt inputs minus one. This field is hardwired to 17h to indicate 24 interrupts.
15	RO	1	**IRQ Assertion Register Supported (PRQ):** This bit is set to 1 to indicate that this version of the I/OxAPIC implements the IRQ Assertion register and allows PCI devices to write to it to cause interrupts.
14:8	RO	0	Reserved.
7:0	RO	20h	**Version (VS):** This identifies the implementation version. This field is hardwired to "20h" to indicate this is an I/OxAPIC.

13.5.3.4 Offset 03h: BCFG—Boot Configuration Register

Offset: 03h Attribute: RW, RO
Default Value: 00000000h Size: 32 bits

The Boot Configuration contains information that is only supposed to be accessed by BIOS and is not for OS use. It contains bits that must be programmed before the OS takes control of interrupts.

Bits	Type	Reset	Description
31:1	RO	0	Reserved.
0	RW	1	**Delivery Type (DT):** Software sets this bit to 1 to indicate that the delivery mechanism is as a system bus message and not the I/OxAPIC serial bus.

13.5.3.5 Offset 10h, 12h,..., 3Eh: RDL—Redirection Table Low DWord Register

Offset: 10h,12h,...,3Eh Attribute: RW, RO
Default Value: 00010000h Size: 32 bits

The information in this register is sent on the system bus to address a local APIC. There is one of these registers for every interrupt. The 1st interrupt (pin 0) has this entry at offset 10h. The 2nd interrupt at 12h, 3rd at 14h, and so forth, until the final interrupt (interrupt 23) at 3Eh.

Bits	Type	Reset	Description
31:18	RO	0	Reserved.
17	RW	0	**Disable Flushing Bit (DFLUSH):** This bit is maintained for any potential software compatibility, but the Intel® 631xESB/632xESB I/O Controller Hub IOxAPIC (Bm:D0:F1) will perform no flushing action, regardless of the setting of this bit.
16	RW	1	Mask (MSK): 0 = An edge or level on this interrupt pin results in the delivery of the interrupt to the destination. 1 = Interrupts are not delivered nor held pending. Setting this bit after the interrupt is accepted by a local APIC has no effect on that interrupt.
15	RW	0	**Trigger Mode (TM):** This field indicates the type of signal on the interrupt pin that triggers an interrupt. 0 = Edge sensitive. 1 = Level sensitive.

Bits	Type	Reset	Description
14	RO	0	**Remote IRR (RIRR):** This bit is used for level-triggered interrupts; its meaning is undefined for edge triggered interrupts. 0 = EOI message is received from a local APIC. 1 = For level triggered interrupts, this bit is set when Local APICs accept the level interrupt sent by the I/OxAPIC. It is reset when an EOI message is received from a local APIC.
13	RW	0	**Interrupt Input Pin Polarity (IP):** This bit specifies the polarity of each interrupt signal connected to the interrupt pins. 0 = Active high. 1 = Active low.
12	RO	0	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. It is read only. Writes to this bit have no effect. 0 = Idle; no activity for this interrupt. 1 = Pending - interrupt has been injected, but delivery is held up due the inability of the receiving APIC unit to accept the interrupt at this time.
11	RW	0	**Destination Mode (DSTM):** This field determines the interpretation of the Destination field. 0 = Physical; Destination APIC ID is identified by RDH bits [59:56]. 1 = Logical; Destination is identified by matching bits [63:56] with the Logical Destination in the Destination Format Register and Logical Destination Register in each local APIC.
10:8	RW	0	**Delivery Mode (DELM):** This field specifies how the APICs listed in the destination field should act upon reception of the interrupt. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are described in more detail in each serial message. The encodings are: 000 = Fixed: Trigger Mode can be edge or level. 001 = Lowest Priority: Trigger Mode can be edge or level. 010 = SMI/PMI: Not supported. 011 = Reserved. 100 = NMI: Not supported. 101 = INIT: Not supported. 110 = Reserved. 111 = ExtINT: Not supported.
7:0	RW	0	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

13.5.3.6 Offset 11h, 13h,..., 3Fh: RDH—Redirection Table High Register

Offset: 11h,13h,..,3Fh Attribute: RW, RO
Default Value: 00000000h Size: 32 bits

The information in this register is sent on the system bus to address a local APIC. There is one of these registers for every interrupt. The 1st interrupt (pin 0) has this entry at offset 11h. The 2nd interrupt at 13h, 3rd at 15h, and so forth, until the final interrupt (interrupt 23) at 3Fh.

Bits	Type	Reset	Description
31:24	RW	0	**Destination ID (DID):** This information is transferred in bits [19:12] of the address.
23:16	RW	0	**Extended Destination ID (EDID):** These bits are sent to a local APIC in system bus delivery mode. These are bits [11:4] of the address.
15:0	RO	0	Reserved.

13.6 PCI Express* to PCI-X* Bridges (Bm:D0:F3)

13.6.1 Configuration Registers

The bridge configuration space follows the standard PCI-to-PCI bridge configuration space format. Table 13-4 shows the PCI Express to PCI-X bridge configuration registers and their address byte offset values.

Note: Registers that are not shown should be treated as Reserved.

Table 13-4. Configuration Register Summary (Sheet 1 of 3)

Address Offset	Symbol	Register Name	Default	Access
00–01h	VID	Vendor ID Register	8086h	RO
02–03h	DID	Device ID Register	0320h	RO
04–05h	PCICMD	Command Register	0000h	RW, RO
06–07h	PCISTS	Status Register	0010h	RWC, RO
08h	RID	Revision ID Register	04h	RO
09–0Bh	CC	Class Code Register	060400h	RO
0Ch	CLS	Cache Line Size Register	00h	RW
0Dh	PLT	Primary Latency Timer Register	00h	RW
0Eh	HTYPE	Header Type Register	81h	RO
10–17h	SHPC_BAR	SHPC Base Address Register	see register desc.	RW, RO
18h	PBN	Primary Bus Number Register	00h	RW
19h	SCBN	Secondary Bus Number Register	00h	RW
1Ah	SBBN	Subordinate Bus Number Register	00h	RW
1Bh	SLT	Secondary Latency Timer Register	00h (PCI) 40h (PCI-X)	RW
1Ch	IOB	I/O Base Register	00h	RW, RO
1Dh	IOL	I/O Limit Register	00h	RW, RO
1E–1Fh	SECSTS	Secondary Status Register	02A0h	RWC,RO
20–21h	MB	Memory Base Register	0000h	RW
22-23h	ML	Memory Limit Register	0000h	RW
24–25h	PMB	Prefetchable Memory Base Register	0001h	RW, RO
26–27h	PML	Prefetchable Memory Limit Register	0001h	RW, RO
28–2Bh	PB_UPPER	Prefetchable Base Upper 32 Bits Register	00000000h	RW
2C–2Fh	PL_UPPER	Prefetchable Limit Upper 32 Bits Register	00000000h	RW
30–31h	IOBU16	I/O Base Upper 16 Bits Register	0000h	RO
32–33h	IOLU16	I/O Limit Upper 16 Bits Register	0000h	RO
34h	CAPP	Capabilities Pointer Register	44h	RO
3Ch	INTRL	Interrupt Line Information Register	00h	RW
3Dh	INTRP	Interrupt Pin Information Register	0100h	RO
3E–3Fh	BRIDGE_CNT	Bridge Control Register	0000h	RW, RWC, RO

Table 13-4. Configuration Register Summary (Sheet 2 of 3)

Address Offset	Symbol	Register Name	Default	Access
40–41h	CNF	PCI Express to PCI-X bridge Configuration Register	check register desc	RW, RO
42h	MTT	Multi-Transaction Timer Register	00h	RW, RO
43h	PCLKC	PCI Clock Control Register	FFh	RW, RO
44h	PCI Express_CAPID	PCI Express Capability Identifier Register	10h	RO
45h	PCI Express_NXTP	PCI Express Next Item Pointer Register	5Ch	RO
46–47h	PCI Express_CAP	PCI Express Capability Designator Register	0071h	RO
48–4B	PCI Express_DCAP	PCI Express Device Capabilities Register	0001h	RW, RO
4C–4D	PCI Express_DCTL	PCI Express Device Control Register	2000h	RW, RO
4E-4F	PCI Express_DSTS	PCI Express Device Status Register	0	RWC, RO
50-53h	PCI Express_LCAP	PCI Express Link Capabilities Register	000B0211h	RO
54-55h	PCI Express_LCTL	PCI Express Link Control Register	0000h	RW, RO
56–57h	PCI Express_LSTS	PCI Express Link Status Register	0000h	RO
5Ch	MSI_CAPID	PCI Express MSI Capability Identifier Register	05h	RO
5Dh	MSI_NXTP	PCI Express MSI Next Item Pointer Register	6Ch	RO
5E–5Fh	MSI_MC	PCI Express MSI Message Control Register	0080h	RW, RO
60–67h	MSI_MA	PCI Express MSI Message Address Register	00000000h	RW, RO
68–69h	MSI_MD	PCI Express MSI Message Data Register	0000h	RW
6Ch	PCIXPM_CAPID	Power Management Capability Register	01h	RO
6Dh	PCIXPM_NXTP	Power Management Next Item Pointer Register	D8h (HP) 00h (Non-HP)	RO
6E–6Fh	PCIXPM_PMC	Power Management Capabilities Register	402Ah (HP) 002Ah (Non-Hot-Plug)	RO
70–71h	PCIXPM_PMCSR	Power Management Control and Status Register	0000h	RWC, RO
72h	PCIXPM_BSE	Power Management Bridge Support Extensions Register	00h	RO
73h	PCIXPM_DATA	Power Management Data Register	00h	RO
78h	SHPC_CAPID	SHPC Capability Identifier Register	0Ch	RO
79h	SHPC_NXTP	SHPC Next Item Pointer Register	00h	RO
7Ah	SHPC_DWSEL	SHPC DWord Select Register	00h	RO
7Bh	SHPC_STS	SHPC Status Register	00h	RO
7C–7Fh	SHPC_DWORD	SHPC Data Register	00000000h	RW
D8h	PX_CAPID	PCI-X Capabilities Identifier Register	07h	RO
D9h	PX_NXTP	PCI-X Next Pointer Register	D0h	RO
DA–DBh	PX_SSTS	PCI-X Secondary Status Register	0003h	RWC, RO

Table 13-4. Configuration Register Summary (Sheet 3 of 3)

Address Offset	Symbol	Register Name	Default	Access
DC-DFh	PX_BSTS	PCI-X Bridge Status Register	00030000h (Function 0) 00030002h (Function 2)	RO
E0–E3h	PX_USTC	PCI-X Upstream Split Transaction Control Register	0000FFFFh	RW, RO
E4–E7h	PX_DSTC	PCI-X Downstream Split Transaction Control Register	0000FFFFh	RW, RO
E8–E9h	RAS_STS	RAS Status Register	0000h	RWC
EA–EBh	RAS_CMD	RAS Command Register	0000h	RW
EC–EDh	ARB_CNTRL	Arbiter Control Register	0180h	RW
F4–F5h	PXB_STS	PCI Express to PCI-X bridge Status Register	strap	RO
100-103h	PCI Express_CAPID	PCI Express Capability Identifier Register	30000000	RO
12C-12Dh	PCIXERRUNC_STS	PCI Express Uncorrectable Error Status Register	0000h	RWC
130-133h	PCIXERRUNC_MSK	Uncorrectable PCI-X Error Mask Register	000017A8h	RWS,RO
134-135h	SEC_UNC_ERRSEV	Secondary Uncorrectable Error Severity Register	2340h	RWS,RO
138-13Bh	PcIXERRUNC_PTR	Uncorrectable Error Pointer Register	00000000h	ROS,RO
13C-143h	PCIXHDLOG	PCI-X Uncorrectable Transaction Header Log Register	0000h	ROS
14C-153h	PCIXDLOG	PCI-X Uncorrectable/Correctable Data Error Log Register	0000000000000000h	ROS
154-155h	PCIXERRLOGCTL	Other PCI-X Error Logs and Control Register	00000000h	RWCS,ROS,RO
300-303h	PWRBUDGTCAP	Power Budgeting Enhanced Capability Header Register	00010004h	RO
304h	PWRBUDGTDSEL	Power Budgeting Data Select Register	00h	RW
308-30Bh	PWRBUDGTDATA	Power Budgeting Data Register	00000000h	RO
30Ch	PWRBUDGT	Power Budgeting Register	0h	RO,RWO
314h	PWRBUDGTINFO0	Power Budgeting Register 0	00000000h	RO,RW

13.6.1.1 Offset 00h: VID—Vendor ID Register (Bm:D0:F3)

Offset: 00–01h
Default Value: 8086h
Attribute: RO
Size: 16 bits

Bits	Type	Reset	Description
15:00	RO	8086h	**Vendor ID (VID):** 16-bit vendor ID assigned to Intel VID=8086h.

13.6.1.2 Offset 02h: DID—Device ID Register (Bm:D0:F3)

Offset: 02–03h
Default Value: 0320h (Function 0)
0321h (Function 2)
Attribute: RO
Size: 16 bits

Bits	Type	Reset	Description
15:0	RO	350Ch – 350Fh depending on SKU.	**Device ID (DID):** Device number of the Intel® 631xESB/632xESB I/O Controller Hub PCI Express to PCI-X bridge.

13.6.1.3 Offset 04h: PCICMD—PCI Command Register (Bm:D0:F3)

Offset: 04–05h
Default Value: 0000h
Attribute: RW, RO
Size: 16 bits

Bits	Type	Reset	Description
15:11	RO	0	Reserved.
10	RW	0	**Interrupt Mask (INTMASK):** This bit disables the SHPC from asserting IRQ[23]# wired to the I/OxAPIC. This bit is valid only when the MSI is disabled; that is, the MSI enable bit (bit 0) in the MSC_MC register (offset 5Eh) is a zero. A value of 0 for this bit enables the assertion of its IRQ[23]# signal to the I/OxAPIC. A value of 1 disables the assertion of its IRQ[23]# signal. If IRQ[23]# is already asserted when this bit is set, it must be de-asserted.
9	RO	0	**Fast Back-to-Back Transactions Enable (FBTE):** This bit has no meaning on the PCI Express interface. It is hardwired to '0'.
8	RW	0	**SERR Enable (SEE):** Controls the enable for PCI-compatible SERR reporting on the PCI Express interface (along with the Status Register (STS REG, offset 06h, bit 14). 0 = Disable SERR reporting 1 = Enable SERR reporting Note that this bit does not affect the setting of the PCI Express error bits in the PCI Express Capability Structure.
7	RO	0	Wait Cycle Control (WCC): Reserved.
6	RW	0	**Parity Error Response (PER):** Controls the response to data parity errors forwarded from the PCI Express interface and peer PCI on read completions. 0 = Disable. Ignore errors on the PCI Express interface and the peer-PCI interface. 1 = Enable. Report read completion data parity errors on the PCI E interface and set the Master Data Parity Detected (MDPD) bit in the status register. Note that this bit does not affect the setting of the PCI Express error bits in the PCI Express Capability Structure.
5	RO	0	VGA Palette Snoop (VGA_PS): Reserved.
4	RO	0	**Memory Write and Invalidate (MWIE):** The Intel® 631xESB/632xESB I/O Controller Hub does not generate memory write and invalidate transactions, as the PCI Express interface does not have a corresponding transfer type.
3	RO	0	Special Cycle Enable (SCE): Reserved.

Bits	Type	Reset	Description
2	RW	0	**Bus Master Enable (BME):** Controls the ability to act as a master on PCI Express when forwarding memory transactions from PCI (memory, I/O, and configuration) or when generating MSI transaction on behalf of the SHPC. 0 = Disable. 1 = Enable. Note that this bit does not stop Intel® 631xESB/632xESB I/O Controller Hub from issuing completions on PCI Express. Software must guarantee that when this bit is set, all inbound posted transactions are flushed in the bridge segment. Otherwise, delayed completions (for example, configuration read completions) could be stuck behind a posted write and cannot proceed from PCI to PCI Express.
1	RW	0	**Memory Space Enable (MSE):** Controls the response as a target to memory accesses on the PCI Express interface that address a device behind the PCI Express to PCI-X bridge or the SHPC memory space. 0 = These transactions are master aborted on the PCI Express interface. 1 = To allowed memory transaction from PCI to be passed to the PCI Express.
0	RW	0	**I/O Space Enable (IOSE):** Controls the PCI Express to PCI-X bridge's response as a target to I/O transactions on the PCI Express interface that addresses a device that resides behind the PCI Express to PCI-X bridge. 0 = These transactions are master aborted on the PCI Express interface. 1 = Enables response to I/O transaction initiated on the PCI Express interface.

13.6.1.4 Offset 06h: PCISTS—Status Register (Bm:D0:F3)

Offset: 06–07h
Default Value: 0010h
Attribute: RWC, RO
Size: 16 bits

Bits	Type	Reset	Description
15	RWC	0	**Detected Parity Error (DPE):** 0 = Software clears this bit by writing a 1 to it. 1 = Data parity error on the PCI Express bus interface or peer PCI segment is detected. This bit gets set even if the Parity Error Response (bit 6 of the command register) is not set. Indicates that a parity error was detected on cycles targeting the I/OxAPIC.
14	RWC	0	**Signaled System Error (SSE):** This bit is used for PCI-compatible error signaling on the PCI Express bus. 0 = Software clears this bit by writing a 1 to it. 1 = SERR# is reported to the PCI Express interface.
13	RWC	0	Received Master-Abort (RMA): 0 = Software clears this bit by writing a 1 to it. 1 = Intel® 631xESB/632xESB I/O Controller Hub is acting as master on the PCI Express interface and receives a completion packet with master abort status.
12	RWC	0	**Received Target-Abort (RTA):** 0 = Software clears this bit by writing a 1 to it. 1 = Intel® 631xESB/632xESB I/O Controller Hub is acting as master on the PCI Express interface and receives a completion packet with target abort status.
11	RWC	0	**Signaled Target Abort (STA):** This bit is set whenever the PCI Express to PCI-X bridge generates a completion packet with CA status on PCI Express (either forwarded from PCI interface or internally signaled by SHPC) 0 = Target Abort not signaled on the PCI/PCI-X interface. 1 = Target Abort signaled on the PCI/PCI-X interface. Software clears this bit by writing a 1 to it.
10:9	RO	0	**DEVSEL# Timing (DVT):** These bits have no meaning on the PCI Express interface. Hardwired to 0.

Bits	Type	Reset	Description
8	RWC	0	**Master Data Parity Error (MDP):** 0 = Software clears this bit by writing a 1 to it. 1 = PCI Express to PCI-X bridge receives a completion packet from the PCI Express interface from a previous request, and detects a data parity error, and the Parity Error Response (PER) bit in the Command Register (offset 04h, bit 6) is set.
7	RO	0	**Fast Back-to-Back Transactions Capable (FBC):** Does not apply to PCI Express. Hardwired to 0.
6	RO	0	Reserved.
5	RO	0	**66 MHz Enable (66EN):** Does not apply to PCI Express. Hardwired to 0.
4	RO	1	**Capabilities List (CAPL):** Indicates that the PCI Express to PCI-X bridge contains the capabilities pointer in the bridge. Offset 34h (Capabilities List Pointer - CAPP) indicates the offset for the first entry in the linked list of capabilities. Default = 1.
3	RO	0	**Interrupt Status (INTSTS):** This bit reflects the state of the SHPC interrupt, when the interrupt is generated via the IRQ[23]# wire (not via MSI). Only when the INTx mask bit in the command register is a 0 and this Interrupt Status bit is a 1, and MSI is disabled will the SHPC assert the IRQ[23]# signal to the I/OxAPIC. Setting the INTx mask bit to a 1 has no effect on the setting of this bit.
2:0	RO	0	Reserved.

13.6.1.5 Offset 08h: RID—Revision ID Register (Bm:D0:F3)

Offset: 08h Attribute: RO
Default Value: 00h Size: 8 bits

Bits	Type	Reset	Description
7:0	RO	04h	**Revision ID (REVID):** This indicates the stepping of the PCI Express to PCI-X bridge. 00 = A0 stepping.

13.6.1.6 Offset 09h: CC—Class Code Register (Bm:D0:F3)

Offset: 09–0Bh Attribute: RO
Default Value: 060400h Size: 24 bits

This contains the class code, sub class code, and programming interface for the device.

Bits	Type	Reset	Description
23:16	RO	06h	**Base Class Code (BCC):** The value of "06h" indicates that this is a bridge device.
15:8	ROS	04h	**Sub Class Code (SCC):** 8-bit value that indicates this is of type PCI-to-PCI bridge.
7:0	RO	0	**Programming Interface (PIF):** Indicates that this is standard (non-subtractive) PCI-to-PCI bridge.

13.6.1.7 Offset 0Ch: CLS—Cache Line Size Register (Bm:D0:F3)

Offset: 0Ch Attribute: RW
Default Value: 00h Size: 8 bits

This indicates the cache line size of the system.

Bits	Type	Reset	Description
7:0	RW	0	**Cache Line Size (CLS):** This field is implemented by PCI Express devices as a RW field for legacy compatibility purposes but has no impact on any PCI Express device functionality.

13.6.1.8 Offset 0Dh: PLT—Primary Latency Timer Register (Bm:D0:F3)

Offset: 0Dh
Default Value: 00h
Attribute: RW
Size: 8 bits

This register does not apply to the PCI Express interface.

Bits	Type	Reset	Description
7:3	RO	0	**Time Value (TV):** Read only register since PCI Express does not have an equivalent functionality.
2:0	RO	0	Reserved.

13.6.1.9 Offset 0Eh: HTYP—Header Type Register (Bm:D0:F3)

Offset: 0Eh
Default Value: 81h
Attribute: RW
Size: 8 bits

This register is used to indicate the layout for bytes 10h through 3Fh of the device's configuration space.

Bits	Type	Reset	Description
7	RO	1	**Multi-Function Device (MFD):** Reserved as '1' to indicate the bridge is a multi-function device.
6:0	RO	01h	**Header Type (HTYPE):** Defines the layout of addresses 10h through 3Fh in configuration space. Reads as 01h to indicate that the register layout conforms to the standard PCI Express-to-PCI/PCI-X bridge layout.

13.6.1.10 Offset 10h: SHPC_BAR—SHPC 64-bit Base Address Register (Bm:D0:F3)

Offset: 10-17h
Default Value: 00000008h
Attribute: RW, RO
Size: 64 bits

This register is used to access the SHPC working register set.

Note: When Hot-Plug is disabled (HPX_SLOT[3] = 0), this register is RESERVED and set to 0h.

Bits	Type	Reset	Description
63:12	RW	0	**Base Address (BA):** These bits are used by BIOS to understand that SHPC needs 4 Kbytes of memory space and then write a valid 4 Kbyte aligned base address.
11:4	RO	0	Reserved.
3	RO	0	**Prefetchable (PF_SHPC):** This bit is a read-only 0 to indicate that this register needs to be mapped into the non-prefetchable space.
2:1	RO	10b	**Type (TYP_SHPC):** These bits are read-only with a reset default of 10b, indicating that this register can map anywhere in the 64-bit memory space.
0	RO	0	**Memory Space Indicator (MEMSI):** This bit is a read-only 0 indicating that this Base Address Register maps into memory space.

13.6.1.11 Offset 18h: PBN— Primary Bus Number Register (Bm:D0:F3)

Offset: 18h
Default Value: 00h
Attribute: RW
Size: 8 bits

This register is used to record the bus number of the logical PCI bus segment to which the primary interface of the bridge is connected.

Bits	Type	Reset	Description
7:0	RW	0	**Primary Bus Number (PBN):** This field indicates the bus number of the PCI Express interface. Configuration software programs the value in this register. Any type 1 configuration cycle with a bus number less than this number will not be accepted by this portion of the Intel® 631xESB/632xESB I/O Controller Hub.

13.6.1.12 Offset 19h: SCBN—Secondary Bus Number Register (Bm:D0:F3)

Offset: 19h
Default Value: 00h
Attribute: RW
Size: 8 bits

This register is used to record the bus number of the PCI bus segment to which the secondary interface of the bridge is connected.

Bits	Type	Reset	Description
7:0	RW	0	**Secondary Bus Number (SCBN):** This field indicates the bus number of PCI to which the secondary interface is connected. Any type 1 configuration cycle matching this bus number will be translated to a type 0 configuration cycle and run on the PCI bus.

13.6.1.13 Offset 1Ah: SBBN—Subordinate Bus Number Register (Bm:D0:F3)

Offset: 1Ah
Default Value: 00h
Attribute: RW
Size: 8 bits

This register is used to record the bus number of the highest numbered PCI bus segment which is downstream of (or subordinate to) the bridge (PCI Express to PCI-X bridge).

Bits	Type	Reset	Description
7:0	RW	0	**Subordinate Bus Number (SBBN):** This field indicates the highest PCI bus number below this bridge. Any type 1 configuration cycle on the PCI Express interface whose bus number is greater than the secondary bus number and less than or equal to the subordinate bus number will be run as a type 1 configuration cycle on the PCI bus.

13.6.1.14 Offset 1Bh: SLT—Secondary Latency Timer (Bm:D0:F3)

Offset: 1Bh
Default Value: 00h (PCI)
40h (PCI-X)
Attribute: RW, RO
Size: 8 bits

This timer controls the amount of time that the PCI Express to PCI-X bridge will continue to burst data on its secondary interface. The counter starts counting down from the assertion of PxFRAME#. If the grant is removed, the expiration of this counter will result in the de-assertion of PxFRAME#. If the grant has not been removed, then

the PCI Express to PCI-X bridge may continue ownership of the bus. Secondary latency timer's default value should be 64 in PCI-X mode (Refer to Section 1.12.2 of the *PCI-X* Protocol Addendum to the PCI Local Bus Specification*, *Revision 2.0a*, Rule 11).

Bits	Type	Reset	Description
7:3	RW	PCI – 00h PCI-X – 08h	**Secondary Latency Timer (TV):** 5-bit value that indicates the number of PCI clocks, in 8-clock increments, that the PCI Express Bridge/Switch will remain as a master of the PCI bus if another master is requesting use of the PCI bus. ***Note:*** In scenarios like Hot-Plug when SW changes the mode of the PCI bus from conventional to PCI-X or vice-versa, this register changes its default value also appropriately.
2:0	RO	0	Reserved.

13.6.1.15 Offset 1Ch: IOB—I/O Base Register (Bm:D0:F3)

Offset: 1Ch Attribute: RW, RO
Default Value: 00h Size: 8 bits

This register defines the base and limit (aligned to a 4-Kbyte boundary) of the I/O area of the bridge. Accesses from the PCI Express interface that are within the ranges specified in this register will be sent to PCI if the I/O space enable bit is set. Accesses from PCI that are outside the ranges specified will master abort.

Bits	Type	Reset	Description
7:4	RW	0	**I/O Base Address Bits [15:12] (IOBA):** This field defines the bottom address of an address range to determine when to forward I/O transactions from one interface to the other. These bits correspond to address lines 15:12 for 4 KB alignment. Bits 11:0 are assumed to be 000h.
3:2	RO	0	**I/O Base Address Bits [11:10] (IOBA1K):** When the EN1K bit is set in the Intel® 631xESB/632xESB I/O Controller Hub Configuration register (CNF), these bits become read/write and are compared with I/O address bits [11:10] to determine the 1 KB base address. When the EN1K bit is cleared, this field becomes Read Only.
1:0	RO	0	**I/O Base Addressing Capability (IOBC):** These are hardwired to '0', indicating support for only 16-bit I/O addressing.

13.6.1.16 Offset 1Dh: IOL—I/O Limit Register (Bm:D0:F3)

Offset: 1Dh Attribute: RW, RO
Default Value: 00h Size: 8 bits

This register defines the limit (aligned to a 4-Kbyte boundary) of the I/O area of the bridge. Accesses from the PCI Express interface that are within the ranges specified in this register will be sent to PCI if the I/O space enable bit is set. Accesses from PCI that are outside the ranges specified will master abort.

Bits	Type	Reset	Description
7:4	RW	0	**I/O Limit Address Bits [15:12] (IOLA):** Defines the top address of an address range to determine when to forward I/O transactions from PCI Express to PCI. These bits correspond to address lines 15:12 for 4 KB alignment. Bits [11:0] are assumed to be FFFh.
3:2	RO	0	**I/O Limit Address Bits [11:10] (IOLA1K):** When the EN1K bit is set in the Intel® 631xESB/632xESB I/O Controller Hub Configuration register (CNF), these bits become read/write and are compared with I/O address bits [11:10] to determine the 1 KB limit address. When the EN1K bit is cleared, this field becomes Read Only.
1:0	RO	0	**I/O Limit Addressing Capability (IOLC):** These bits are hardwired to '0', indicating support for only 16-bit I/O addressing.

13.6.1.17 Offset 1Eh: SSTS—Secondary Status Register (Bm:D0:F3)

Offset: 1E–1Fh
Default Value: 02A0h
Attribute: RWC, RO
Size: 16 bits

Bits	Type	Reset	Description
15	RWC	0	Detected Parity Error (DPE): This bit reports the detection of an uncorrectable address, attribute or data error by the Intel® 631xESB/632xESB I/O Controller Hub's PCI/PCI-X interface. This bit is set when any one of the following three conditions are true: • An uncorrectable address or attribute error as a potential target is detected. • An uncorrectable data error when the target of a write transaction or a PCI-X Split Completion is detected. • An uncorrectable data error when the master of a read transaction (immediate read data or PCI-X Split Response) is detected. This bit gets set even if the Parity Error Response Enable bit (bit 0 of offset 3E–3Fh) of the Bridge Control Register. 0 = Uncorrectable address, attribute or data error not detected on the PCI/PCI-X interface. 1 = Uncorrectable address, attribute or data error detected on the PCI/PCI-X interface. Software clears this bit by writing a 1 to it.
14	RWC	0	Received System Error (RSE): This bit reports the detection of a SERR# assertion on the PCI/PCI-X interface. 0 = SERR# assertion on the PCI/PCI-X interface has not been detected. 1 = SERR# assertion on the PCI/PCI-X interface has been detected. Software clears this bit by writing a 1 to it.
13	RWC	0	Received Master Abort (RMA): This bit reports the detection of a Master-Abort termination when the PCI Express to PCI-X bridge is acting as a PCI/PCI-X master or when the PCI Express to PCI-X bridge receives a PCI-X Split Completion Message indicating Master Abort. 0 = Master-Abort not detected on the PCI/PCI-X interface. 1 = Master-Abort detected on the PCI/PCI-X interface Software clears this bit by writing a 1 to it.
12	RWC	0	Received Target Abort (RTA): This bit reports the detection of a Target-Abort termination when the PCI Express to PCI-X bridge is acting as a PCI/PCI-X master or when the PCI Express to PCI-X bridge signals a PCI-X Split Completion Message indicating Target Abort. 0 = Target-Abort not detected on the PCI/PCI-X interface. 1 = Target-Abort detected on the PCI/PCI-X interface Software clears this bit by writing a 1 to it.
11	RWC	0	Signaled Target Abort (STA): This bit reports the signaling of a Target-Abort termination by the PCI Express to PCI-X bridge when it responds as the target of a transaction on the PCI/PCI-X interface or when the PCI Express to PCI-X bridge signals a PCI-X Split Completion Message with Target Abort. 0 = Target-Abort not signaled on the PCI/PCI-X interface. 1 = Target-Abort signaled on the PCI/PCI-X interface. Software clears this bit by writing a 1 to it.
10:9	RO	01b	**DEVSEL# Timing (DVT):** This field indicates that the PCI Express to PCI-X bridge responds in medium decode time to all cycles targeting the PCI Express interface.

Bits	Type	Reset	Description
8	RWC	0	**Master Data Parity Error (MDP):** This bit is used to report the detection of an uncorrectable data error. This Bit is set if the PCI Express to PCI-X bridge is the bus master of the transaction on the PCI/PCI-X interface, the Parity Error Response bit in the Bridge Control register is set, and either of the following two conditions occur: • The PCI Express to PCI-X bridge asserts PERR# on a read transaction • The PCI Express to PCI-X bridge detects PERR# asserted on a write transaction In addition, when in PCI-X mode, this bit is set if either of the following occur: • The PCI Express to PCI-X bridge detects an uncorrectable data error in a Split Completion or Split Completion Message. • The PCI Express to PCI-X bridge receives a Split Completion Message for a non-posted write indicating an Uncorrectable (Split) Write Data Error. 0 = No uncorrectable data error detected on the PCI/PCI-X interface. 1 = Uncorrectable data error detected on the PCI/PCI-X interface. Once set, this bit remains set until it is reset by writing a 1 to this bit location. If the Parity Error Response bit is cleared, this bit is never set.
7	RO	1	**Fast Back-to-Back Transactions Capable (FBTC):** Indicates that the secondary interface can receive fast back-to-back cycles.
6	RO	0	Reserved.
5	RO	1	**66 MHz Capable (C66):** Indicates the secondary interface of the bridge is 66 MHz capable.
4:0	RO	0	Reserved.

13.6.1.18 Offset 20h: MB—Memory Base Register (Bm:D0:F3)

Offset: 20–21h Attribute: RW, RO
Default Value: 0000h Size: 16 bits

This register defines the base (aligned to a 1-Mbyte boundary) of the prefetchable memory area of the bridge. Accesses from the PCI Express interface that are within the range specified in this register will be sent to PCI if the memory space enable bit is set.

Accesses from PCI that are outside the range specified will be forwarded to the PCI Express interface if the bus master enable bit is set.

Bits	Type	Reset	Description
15:4	RW	0	**Memory Base (MB):** These bits are compared with bits [31:20] of the incoming address to determine the lower 1 MB aligned value (inclusive) of the range. The incoming address must be greater than or equal to this value.
3:0	RO	0	Reserved.

13.6.1.19 Offset 22h: ML—Memory Limit Register (Bm:D0:F3)

Offset: 22–24h Attribute: RW, RO
Default Value: 0000h Size: 16 bits

This register defines the limit (aligned to a 1 MByte boundary) of the prefetchable memory area of the bridge. Accesses from the PCI Express interface that are within the range specified in this register will be sent to PCI if the memory space enable bit is set.

Accesses from PCI that are outside the range specified will be forwarded to the PCI Express interface if the bus master enable bit is set.

Bits	Type	Reset	Description
15:4	RW	0	**Memory Limit (ML):** These bits are compared with bits [31:20] of the incoming address to determine the upper 1MByte aligned value (exclusive) of the range. The incoming address must be less than this value.
3:0	RO	0	Reserved.

13.6.1.20 Offset 24h: PMB—Prefetchable Memory Base Register (Bm:D0:F3)

Offset: 24–25h
Default Value: 0001h
Attribute: RW, RO
Size: 16 bits

Defines the base (aligned to a 1MByte boundary) of the prefetchable memory area of the bridge. Accesses from the PCI Express interface that are within the ranges specified in this register will be sent to PCI if the memory space enable bit is set.

Accesses from PCI that are outside the ranges specified will be forwarded to the PCI Express interface if the bus master enable bit is set.

Note that even though this register specifies a valid prefetchable memory window, the PCI Express to PCI-X bridge never prefetches through this window in the outbound direction (reads from PCI Express to PCI). In the inbound direction, prefetchability through this window is controlled through the PCI Express to PCI-X bridge configuration register bits 4:3, at offset 40h.

Bits	Type	Reset	Description
15:4	RW	0	**Prefetchable Memory Base (PMB):** These bits are compared with bits [31:20] of the incoming address to determine the lower 1 MB aligned value (inclusive) of the range. The incoming address must be greater than or equal to this value.
3:0	RO	1	**64-bit Indicator (IS64B):** Indicates that 64-bit addressing is supported for the limit. This value must be in agreement with the IS64L field.

13.6.1.21 Offset 26h: PML—Prefetchable Memory Limit Register (Bm:D0:F3)

Offset: 26–27h
Default Value: 0001h
Attribute: RW, RO
Size: 16 bits

Defines the limit (aligned to a 1 MByte boundary) of the prefetchable memory area of the bridge. Accesses from the PCI Express interface that are within the ranges specified in this register will be sent to PCI if the memory space enable bit is set.

Accesses from PCI that are outside the ranges specified will be forwarded to the PCI Express interface if the bus master enable bit is set.

Note that even though this register specifies a valid prefetchable memory window, the PCI Express to PCI-X bridge never prefetches through this window in the outbound direction (reads from PCI Express to PCI). In the inbound direction, prefetchability through this window is controlled through the PCI Express to PCI-X bridge configuration register bits 4:3, at offset 40h.

Bits	Type	Reset	Description
15:4	RW	0	**Prefetchable Memory Limit (PML):** These bits are compared with bits [31:20] of the incoming address to determine the upper 1 MByte aligned value (exclusive) of the range. The incoming address must be less than this value.
3:0	RO	1	**64-bit Indicator (IS64L):** Indicates that 64-bit addressing is supported for the limit. This value must be in agreement with the IS64B field.

13.6.1.22 Offset 28h: PMBU32—Prefetchable Base Upper 32 Bits Register (Bm:D0:F3)

Offset: 28–2Bh
Default Value: 00000000h
Attribute: RW, RO
Size: 32 bits

This defines the upper 32 bits of the prefetchable address base register.

Bits	Type	Reset	Description
31:0	RW	0	**Prefetchable Memory Base Upper Portion (PMBU):** All bits are read/ writeable; full 64-bit addressing supported.

13.6.1.23 Offset 2Ch: PMLU32—Prefetchable Limit Upper 32 Bits Register (Bm:D0:F3)

Offset: 2C–2Fh
Default Value: 00000000h
Attribute: RW
Size: 32 bits

This defines the upper 32 bits of the prefetchable address limit register.

Bits	Type	Reset	Description
31:0	RW	0	**Prefetchable Memory Limit Upper Portion (PMLU):** All bits are read/ writeable; full 64-bit addressing supported.

13.6.1.24 Offset 30h: IOLU16—I/O Limit Upper 16 Bits Register (Bm:D0:F3)

Offset: 30–31h
Default Value: 0000h
Attribute: RO
Size: 16 bits

Since I/O is limited to 64 Kbytes, this register is reserved and not used.

Bits	Type	Reset	Description
15:0	RO	0	**I/O Limit High 16 Bits (IOLH):** Reserved.

13.6.1.25 Offset 32h: IOBU16—I/O Base Upper 16 Bits Register (Bm:D0:F3)

Offset: 32–33h
Default Value: 0000h
Attribute: RO
Size: 16 bits

Since I/O is limited to 64 Kbytes, this register is reserved and not used.

Bits	Type	Reset	Description
15:0	RO	0	**I/O Base High 16 Bits (IOBH):** Reserved.

13.6.1.26 Offset 34h: CAPP—Capabilities Pointer Register (Bm:D0:F3)

Offset: 34h
Default Value: 44h
Attribute: RO
Size: 8 bits

This register is used to point to a linked list of additional capabilities.

Bits	Type	Reset	Description
7:0	RO	44h	**Capabilities Pointer (PTR):** This field indicates that the pointer for the first entry in the PCI Express Capability List is at offset 44h in configuration space.

13.6.1.27 Offset 3Ch: INTR — Interrupt Information Register (Bm:D0:F3)

Offset: 3Ch
Default Value: 00h
Attribute: RW
Size: 16 bits

This register contains information on interrupts on the bridge.

Bits	Type	Reset	Description
SHPC Disabled (HXSLOT[3]=0 at PWROK asserting edge)			
15:08	RO	00h	**Interrupt Pin (PIN):** Indicates no interrupt is used by the bridge segment
SHPC Enabled (HXSLOT[3]=1 at PWROK asserting edge)			
15:08	RO	01h	**Interrupt Pin (PIN):** Intel® 631xESB/632xESB I/O Controller Hub has an integrated SHPC, which is a source of interrupt. The logical PCI-X bus interrupt pin is INTA# with a corresponding register value of 01h. Note that the Hot-Plug interrupt is routed internally to IRQ[23]# of the APIC.
7:0	RW	00h	**Interrupt Line (INTRL):** This register is used to convey the interrupt line routing information between the initialization code and the device driver. This is not used by Intel® 631xESB/632xESB I/O Controller Hub. This is a read/write register with a reset default of 0.

13.6.1.28 Offset 3Eh: BCTRL—Bridge Control Register (Bm:D0:F3)

Offset: 3E–3Fh
Default Value: 0000h
Attribute: RW, RWC; RO
Size: 16 bits

This register provides extensions to the Command register that are specific to a bridge. The Bridge Control register provides many of the same controls for the secondary interface that are provided by the Command register for the primary interface. Some bits affect operation of both interfaces of the bridge.

Bits	Type	Reset	Description
15:12	RO	0	Reserved.
11	RW	0	**Discard Timer SERR Enable (DTSE):** Controls the generation of ERR_UNC on the primary interface in response to a timer discard on the secondary interface. 0 = Do not generate ERR_UNC on a secondary timer discard 1 = Generate ERR_UNC in response to a secondary timer discard
10	RWC	0	**Discard Timer Status (DTS):** Software clears this bit by writing a 1 to it. 1 = Secondary discard timer expires (there is no discard timer for the primary interface)
9	RW	0	**Secondary Discard Timer (SDT):** Sets the maximum number of PCI clock cycles that the PCI Express to PCI-X bridge waits for an initiator on the PCI bus to repeat a delayed transaction request. The counter starts once the delayed transaction completion is at the head of the queue. If the master has not repeated the transaction at least once before the counter expires, the PCI Express to PCI-X bridge discards the transaction from its queues. 0 = The PCI master timeout value is between 2^{15} and 2^{16} PCI clocks. 1 = The PCI master timeout value is between 2^{10} and 2^{11} PCI clocks.

Bits	Type	Reset	Description
8	RO	0	**Primary Discard Timer (PDT):** Not relevant to the PCI Express interface. This bit is RW for software compatibility only.
7	RO	0	**Fast Back-to-Back Enable (FBE):** The PCI Express to PCI-X bridge cannot generate fast back-to-back cycles on the PCI bus from PCI Express interface initiated transactions.
6	RW	0	**Secondary** Bus Reset (SBR): Controls PxPCIRST# assertion on the PCI bus. 0 =PxPCIRST# is deasserted. 1 = PxPCIRST# is asserted. When PxPCIRST# is asserted, the data buffers between the PCI Express interface and PCI and the PCI bus interface logic are initialized back to reset conditions. The PCI Express interface logic and the PCI Express to PCI-X bridge configuration registers are not affected. SHPC interface logic, SHPC working space registers, I/OxAPIC interface logic and I/OxAPIC registers are not reset on this bit being set. Note that once this bit is set, the currently running transaction on the PCI bus will be completed and then the bus will be reset. It is the responsibility of software to make sure that all pending transactions with the bus segment are complete before setting this bit.
5	RW	0	**Master Abort Mode (MAM):** Controls the behavior when a master abort occurs on either interface. Master Abort on the PCI Express interface (Memory reads only): 0 = The PCI Express to PCI-X bridge asserts PxTRDY# on the PCI/PCI-X bus. It drives all '1's for reads. 1 = The PCI Express to PCI-X bridge returns a target abort on the PCI/PCI-X bus. Master Abort PCI (Completion required packets only): 0 = Normal completion status will be returned on the PCI Express interface. 1 = Target abort completion status will be returned on the PCI Express interface.
4	RW	0	**VGA 16-bit Decode (V16D):** This bit enables the bridge to provide 16-bit decoding of the VGA I/O address precluding the decode of VGA alias addresses every 1 KB. This bit requires the VGA enable bit (bit 3 of this register) to be set to 1. 0 = Disable 1 = Enable
3	RW	0	**VGA Enable (VGAE):** Modifies the response to VGA compatible address. 1 = the following transactions from the PCI Express interface to PCI regardless of the value of the I/O base and I/O limit registers is forwarded. The transactions are qualified by the memory enable and I/O enable in the command register. Memory addresses: 000A0000h–000BFFFFh I/O addresses: 3B0h–3BBh and 3C0h-3DFh. For the I/O addresses, bits [63:16] of the address must be '0', and bits [15:10] of the address are ignored (that is, aliased). 0 = The same holds true from secondary accesses to the primary interface in reverse. That is, when the bit is 0, memory and I/O addresses on the secondary interface between the above ranges will be forwarded to the PCI Express interface.

Bits	Type	Reset	Description
2	RW	0	**ISA Enable (IE):** Modifies the response by the bridge to ISA I/O addresses. This only applies to I/O addresses that are enabled by the I/O Base and I/O Limit registers and are in the first 64 KB of PCI I/O space. 0 = Disable. 1 = Enable. The bridge will block any forwarding from primary to secondary of I/O transactions addressing the last 768 bytes in each 1 KB block (offsets 100h to 3FFh). This bit has no effect on transfers originating on the secondary bus as the Intel® 631xESB/632xESB I/O Controller Hub does not forward I/O transactions across the bridge.
1	RW	0	**SERR Enable (SE):** Controls the forwarding of secondary interface SERR# assertions on the primary interface. 0 = Disable. 1 = Enable. The Intel® 631xESB/632xESB I/O Controller Hub will send a PCI Express interface SERR cycle when all of the following are true: • SERR# is asserted on the secondary interface. • This bit is set. • The SERR Enable bit in the Command Register is set.
0	RW	0	**Parity Error Response Enable (PERE):** Controls the response to address and data parity errors on the secondary interface. 0 = The bridge must ignore any parity errors that it detects and continue normal operation. The Intel® 631xESB/632xESB I/O Controller Hub must generate parity even if parity error reporting is disabled. 1 = Report parity errors.

13.6.1.29 Offset 40h: CNF—PCI Express* to PCI-X* Bridge Configuration Register (Bm:D0:F3)

Offset: 40–41h Attribute: RW, RO
Default Value: See Register Description Size: 16 bits

This register contains PCI Express to PCI-X bridge specific control bits.

Bits	Type	Reset	Description
15:14	RW	x	**PCI Mode (PMODE):** Determines the mode of operation of the PCI bus. These bits both reflect the status of the current PCI bus mode at power up and also lets software change the mode by writing to these bits. Bits Mode 00 Conventional PCI Mode 01 PCI-X Mode 1 10/11 Reserved
13	RO	1	Reserved
12	RW	0	Enable I/O Space to 1 KB Granularity (EN1K): 0 = Disable. 1 = Enable. I/O space is decoded to 1 KB instead of the 4 KB limit that currently exists in the I/O base and I/O limit registers. It does this by redefining bits [11:10] and bits [3:2] of the IOB and IOL registers at offset 1Ch and 1Dh to be read/write, and enables them to be compared with I/O address bits [11:10] to determine if they are within the bridge's I/O range.
11	RO	0	Reserved.
10:9	RW	0	**PCI Frequency (PFREQ):** Determines the frequency at which the PCI bus operates. After software determines the bus' capabilities, it sets this value and the PMODE (bits 14 and 15 of this register) to the desired frequency and resets the PCI bus. The values are encoded as follows: 00 = 33 MHz 01 = 66 MHz 10 = 100 MHz 11 = 133 MHz Invalid combinations should not be written by software. Results will be indeterminate.

Bits	Type	Reset	Description
8:6	RO	0	Reserved.
5	RW	0	**SHPC GPE Message Enable (SGME):** Enable Redirection of Hot-Plug interrupts to Assert/Deassert_GPE Messages on the PCI Express bus.
4:0	RO	0	Reserved.

13.6.1.30 Offset 42h: MTT—Multi-Transaction Timer Register (Bm:D0:F3)

Offset: 42h Attribute: RW, RO
Default Value: 00h Size: 8 bits

This register controls the amount of time that the PCI Express to PCI-X bridge's arbiter allows a PCI initiator to perform multiple back-to-back transactions on the PCI bus. The number of clocks programmed in the Multi-Transition Timer represents the guaranteed time slice (measured in PCI clocks) allotted to the current agent, after which the arbiter will grant another agent that is requesting the bus.

Bits	Type	Reset	Description
7:3	RW	0	**Timer Count Value (MTC):** This field specifies the amount of time that grant remains asserted to a master continuously asserting its request for multiple transfers. This field specifies the count in an 8-clock (PCI clock) granularity.
2:0	RO	0	Reserved.

13.6.1.31 Offset 43h: PCLKC—PCI Clock Control Register (Bm:D0:F3)

Offset: 43h Attribute: RW, RO
Default Value: FFh Size: 8 bits

This register controls the enable or disable of the PCI Express to PCI-X bridge PCI clock outputs PxPCLKO[6:0].

Bits	Type	Reset	Description
7	RO	1b	Reserved
6:0	RW	1111111 b	**PCI Clock Control (PCLKC):** These bits enable the PCI clock output buffers, when 1. Otherwise the buffers are tri-stated. Bit 6 corresponds to PxPCLKO[6], bit 5 corresponds to PxPCLKO[5], and so forth.

13.6.1.32 Offset 44h: PCI Express_CAPID—PCI Express* Capability Identifier Register (Bm:D0:F3)

Offset: 44h Attribute: RO
Default Value: 10h Size: 8 bits

Bits	Type	Reset	Description
7:0	RO	10h	**PCI Express Capability Identifier (PCI ExpressCAPI):** Indicates PCI Express capability.

13.6.1.33 Offset 45h: PCI Express_NXTP—PCI Express* Next Pointer Register (Bm:D0:F3)

Offset: 45h Attribute: RO
Default Value: 5Ch Size: 8 bits

Bits	Type	Reset	Description
7:0	RO	5Ch or 6Ch	**Next Pointer (MNPTR):** Points to the next capabilities list pointer, which is the MSI capability. When SHPC is enabled, the register value is 5Ch; When SHPC is disabled, the register value is 6Ch.

13.6.1.34 Offset 46h: PCI Express_CAP—PCI Express* Capability Register (Bm:D0:F3)

Offset: 46 - 47h
Default Value: 0030h
Attribute: RO
Size: 16 bits

Bits	Type	Reset	Description
15:8	RO	0	Reserved.
7:4	RO	7h	**Device/Port Type(DEVPORT):** Indicates the type of PCI Express logical device. Value of 7h indicates that this is a PCI/PCI-X to PCI Express Bridge.
3:0	RO	1h	**Capability Version (CAPVER):** Indicates PCI-SIG defined PCI Express capability structure version number. Must be 1h for this version.

13.6.1.35 Offset 48h: PCI Express_DCAP—PCI Express* Device Capabilities Register (Bm:D0:F3)

Offset: 48 – 4Bh
Default Value: 00000001h
Attribute: RO
Size: 32 bits

This register contains information about the PCI Express link capabilities.

Bits	Type	Reset	Description
31:12	RO	0	Reserved.
11:9	RO	0	**Endpoint L1 Acceptable Latency (L1AL):** The PCI Express to PCI-X bridge does not support L1 Link State Power Management (LSPM).
8:6	RO	0	**Endpoint L0s Acceptable Latency (L0AL):** The PCI Express to PCI-X bridge wants the least possible latency out of L0s.
5	RO	0	**Extended Tag Field Supported (ETFS):** This field indicates the maximum supported size of the Tag Field. Defined encodings are: 0 = 5-bit Tag field supported 1 = 8-bit Tag field supported The PCI Express to PCI-X bridge only supports a 5-bit tag.
4:3	RO	0	Reserved.
2:0	RO	1	**Supported Maximum Payload Size (SMPS):** The PCI Express to PCI-X bridge supports a max payload size of 256 byte packets.

13.6.1.36 Offset 4Ch: PCI Express_DCTL—PCI Express* Device Control Register (Bm:D0:F3)

Offset: 4C – 4Dh
Default Value: 0000h
Attribute: RW, RO
Size: 16 bits

This register contains command bits that control the PCI Express to PCI-X bridge behavior on the PCI Express bus.

Bits	Type	Reset	Description
15	RW	0	**Bridge Configuration Retry Enable (BCRE):** When set, the PCI Express to PCI-X bridge is enabled to return a configuration retry response on the PCI Express* bus for a configuration transaction to PCI/PCI-X.
14:12	RW	2h	**MaX_Read_Request Size (MRRS):** Applies to the bridge segment when the segment is in the PCI mode only. When in PCI-X mode, this does not apply (branch predict). The PCI Express to PCI-X bridge cannot send requests greater than the size indicated by this field. Encodings are: Value Request Size 000b 128 bytes 001b 256 bytes 010b 512 bytes 011b 1024 bytes 100b 2048 bytes 101b 4096 bytes 110b Alias 101b 111b Alias 101b
11	RO	0	**Enable No Snoop (ENS):** This does not apply to the PCI Express to PCI-X bridge since it does not set the No Snoop bit on MSI transactions it generates.
10	RO	0	**Auxiliary (AUX) Power PM Enable (AUXPWRPM_EN):** The PCI Express to PCI-X bridge ignores this since it does not support Aux Power.
9	RO	0	**Phantom Function Enable (PFE):** The PCI Express to PCI-X bridge ignores this since it does not support Phantom functions.
8	RO	0	**Extended Tag Field Enable (ETFE):** Always a 0 since the PCI Express to PCI-X bridge only supports a 5-bit tag.
7:5	RW	0	**Maximum Payload Size (MPS):** For PCI Express to PCI-X bridge this must be programmed to either 000 (128B) or 001(256B). Any other value will default to a behavior of 128B.
4	RO	0	Reserved.
3	RW	0	**Unsupported Request Reporting Enable (URRE):** Enables reporting of unsupported requests.
2	RW	0	**Fatal Error Reporting Enabled (FERE):** Controls reporting of fatal errors. 0 = Disable. 1 = PCI Express to PCI-X bridge will report fatal errors.
1	RW	0	**Non-Fatal Error Reporting Enabled (NFERE):** Controls reporting of non-fatal errors. 0 = Disable. 1 = PCI Express to PCI-X bridge will report uncorrectable errors.
0	RW	0	**Correctable Error Reporting Enable (CERE):** Controls reporting of correctable errors. 0 = Disable. 1 = Report correctable errors.

13.6.1.37 Offset 4Eh: EXP_DSTS—PCI Express* Device Status Register (Bm:D0:F3)

Offset: 4E – 4Fh
Attribute: RWC; RO
Default Value: 0000h
Size: 16 bits

This register contains information on the PCI Express device status.

Bits	Type	Reset	Description
15:6	RO	0	Reserved.
5	RO	0	**Transactions Pending (TP):** When this bit is set, the PCI Express to PCI-X bridge has issued Non-Posted Requests which have not been completed. The PCI Express to PCI-X bridge reports this bit cleared only when all completions for any outstanding Non-Posted Request have been received. Note that this is a dynamic bit; that is, this bit could go on and off based on traffic through the PCI Express to PCI-X bridge.
4	RO	0	**Aux Power Detected (APD):** The PCI Express to PCI-X bridge does not support aux power and hence this bit is reserved.
3	RWC	0	**Unsupported Request Detected URD):** The PCI Express to PCI-X bridge sets this bit when any unsupported request from PCI Express is received. This includes requests that are not claimed by any functions within the PCI Express-to-PCI-X bridge, but does NOT include any request that is forwarded to the PCI interface with completions returned with an unsupported request status.
2	RWC	0	**Fatal Error Detected (FERRD):** When set, a fatal error has been detected (regardless of whether an error message was generated or not). This bit remains set until software writes a 1 to clear it.
1	RWC	0	**Non-Fatal Error Detected (NFERRD):** When set, a nonfatal error has been detected (regardless of whether the mask bit was set in advanced error capability or not). This bit remains set until software writes a 1 to clear it.
0	RWC	0	**Correctable Error Detected (CERRD):** When set, a correctable error has been detected (regardless of whether an error message was generated). This bit remains set until software writes a 1 to clear it.

13.6.1.38 Offset 50h: PCI Express_LCAP—PCI Express* Link Capabilities Register (Bm:D0:F3)

Offset: 50 – 53h
Attribute: RO
Default Value: 000B0211h
Size: 32 bits

This register identifies PCI Express Link specific capabilities.

Bits	Type	Reset	Description
31:18	RO	0	Reserved.
17:15	RO	111b	**L1 Exit Latency (L1EL):** L1 transition is not supported.
14:12	RO	111b	**L0s Exit Latency (L0EL):** The value in these bits is influenced by bit 6 in the link control register. Note that software could write the bit 6 in link control register to either a 1 or 0 and these bits should change accordingly. The mapping is shown below: Bit 6 PCI Express Link Control Link Capabilities Bits 14:12 0 110b = 2-4 us 1 010b = 128 ms to less than 256 ms
11:10	RO	1h	**Active State Link PM Support (ASLPMS):** Only Active State L0s supported.
9:4	RO	08h	**Maximum Link Width (MLW):** Support a X8 link maximum.
3:0	RO	1h	**Maximum Link Speed (MLS):** Support 2.5 Gbps.

13.6.1.39 Offset 54h: PCI Express_LCTL– PCI Express* Link Control Register (Bm:D0:F3)

Offset: 54 – 55h
Default Value: 0000h
Attribute: RW, RO
Size: 16 bits

This register controls PCI Express Link specific parameters.

Bits	Type	Reset	Description
15:8	RO	0	Reserved.
7	RW	0	**Extended Synch (EXTS):** This bit when set forces extended transmission of 4096 fast training sequence (FTS) ordered sets in FTS and an extra 1024 training sequence one (TS1) at exit from L1 prior to entering L0. This mode provides external devices monitoring the link time to achieve bit and symbol lock before the link enters L0 state and resumes communication. Default value for this bit is 0.
6	RW	0	**Common Clock Configuration (CCC):** This bit when set indicates that PCI Express to PCI-X bridge and the component at the opposite end of this Link are operating with a distributed common reference clock. A value of 0 indicates that this component and the component at the opposite end of this Link are operating with asynchronous reference clock. Note that this bit is used to reflect the proper L0s exit latency value in the EXP_LSTS register. Components utilize this common clock configuration information.
5:2	RO	0	Reserved.
1:0	RW	0	**Active State Link PM Control (ASLPMC):** Enables PCI Express to PCI-X bridge to enter L0s, not used by I/OxAPIC in normal operation. 00 = L0s entry disabled. 01 = The PCI Express to PCI-X bridge enters L0s per the specification requirements for L0s entry. 10 = L0s entry disabled. 11 = PCI Express to PCI-X bridge enters L0s per the specification requirements for L0s entry.

13.6.1.40 Offset 56h: PCI Express_LSTS – PCI Express* Link Status Register (Bm:D0:F3)

Offset: 56 – 57h
Default Value: 0040h (X4 link)
0080h (X8 link)
Attribute: RO
Size: 16 bits

This register provides information about PCI Express Link specific parameters.

Bits	Type	Reset	Description
15:13	RO	0	Reserved.
12	ROS	0	**Slot Clock Configuration:** This bit indicates that when PCI Express Bridge/ Switch is on a PCI Express connector, that it is using the same reference clock as is provided at the connector. A value of 0 indicates independent reference clock and a value of 1 indicates same reference clock. Note that this bit becomes RWS when ACNF[2] is set.
11	RO	0	**Link Training –** This read-only bit indicates the Physical Layer LTSSM is in the Configuration or Recovery state, or that 1b was written to the Retrain Link bit but Link training has not yet begun. Hardware clears this bit when the LTSSM exits the Configuration/Recovery state. This field is not applicable and reserved for Endpoint devices and Upstream Ports of Switches, and must be hardwired to 0b.

Bits	Type	Reset	Description
10	RO	0	**Undefined –** The value read from this bit is undefined. In previous versions of this specification, this bit was used to indicate a Link Training Error. System software must ignore the value read from this bit. System software is permitted to write any value to this bit.
9:4	RO	4h (X4) 8h (X8)	**Negotiated Link Width (NLW):** This field indicates the negotiated width of PCI Express Link. Defined encodings are: 000100b X4 001000b X8
3:0	RO	0001b	**Link Speed (LS):** This field indicates the negotiated Link speed of the PCI Express Link. The Intel® 631xESB/632xESB I/O Controller Hub supports only 2.5 Gbps.

13.6.1.41 Offset 5Ch: MSI_CAPID— PCI Express* MSI Capability Identifier Register (Bm:D0:F3)

Offset: 5Ch Attribute: RO
Default Value: 05h Size: 8 bits

This register identifies whether the function is MSI capable.

Bits	Type	Reset	Description
7:0	RO	05h	**Capability ID (MCID):** The value of 05h in this field identifies the function as Message Signaled Interrupt capable.

13.6.1.42 Offset 5Dh: MSI_NXTP—PCI Express* MSI Next Pointer Register (Bm:D0:F3)

Offset: 5Dh Attribute: RO
Default Value: 6Ch Size: 8 bits

Bits	Type	Reset	Description
7:0	RO	6Ch	**Next Pointer (MNPTR):** Pointer to the next item in the capabilities list. Must be NULL for the final item in the list.

13.6.1.43 Offset 5Eh: MSI_MC—PCI Express* MSI Message Control Register (Bm:D0:F3)

Offset: 5E – 5Fh Attribute: RW; RO
Default Value: 0080h Size: 16 bits

Bits	Type	Reset	Description
15:8	RO	0	Reserved.
7	RO	1	**64Bit Address Capable (64CAP):** The Intel® 631xESB/632xESB I/O Controller Hub is capable of generating a 64-bit message address.
6:4	RW	0	**Multiple Message Enable (MMEN):** These bits are RW for software compatibility, but only one message is ever sent by the PCI Express to PCI-X Bridge.
3:1	RO	0	**Multiple Message Capable (MMCAP):** Supports only single message.
0	RW	0	**MSI Enable (MSIEN):** If set to a 1, the Intel® 631xESB/632xESB I/O Controller Hub is permitted to use MSI to request service and is prohibited from using its INTx# pin. Thus MSI would be enabled and SHPC would not use the IRQ[23]# wired to the internal I/OxAPIC to generate interrupts. If set to a 0, the Intel® 631xESB/632xESB I/O Controller Hub is prohibited from using MSI to request service.

13.6.1.44 Offset 60h: MSI_MA—PCI Express* MSI Message Address Register (Bm:D0:F3)

Offset: 60 – 67h
Default Value: 00000000h
Attribute: RW, RO
Size: 64 bits

Bits	Type	Reset	Description
63:2	RW	0	**Address (ADDR):** Lower 32 bits of the system specified message address, always DWord aligned.
1:0	RO	0	Reserved.

13.6.1.45 Offset 68h: MSI_MD—PCI Express* MSI Message Data Register (Bm:D0:F3)

Offset: 68 – 69h
Default Value: 0000h
Attribute: RW
Size: 16 bits

Bits	Type	Reset	Description
15:0	RW	0	**Data (DATA):** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (D[15:0]) of the MSI memory write transaction.

13.6.1.46 Offset 6Ch: PCI ExpressPM_CAPID – PCI Express* PM Capability Structure Register (Bm:D0:F3)

Offset: 6Ch
Default Value: 01h
Attribute: RO
Size: 8 bits

This register identifies specific PCI Express Power Management capabilities.

Bits	Type	Reset	Description
7:0	RO	01h	**Capability ID (CAPID):** Capability ID indicates PCI compatible Power Management.

13.6.1.47 Offset 6Dh: PCI ExpressPM_NXTP – PCI Express* Bridge Power Management Capabilities Register (Bm:D0:F3)

Offset: 6Dh
Default Value: 78h or D8h
Attribute: RO
Size: 8 bits

Bits	Type	Reset	Description
7:0	RO	78h or 80h	**Next Capability Pointer (NCPTR):** Points to the next capability item. Default is 78h when SHPC is enabled (HPX_SLOT[3] = 1), and 80h when SHPC is disabled (HPX_SLOT[3] = 0).

13.6.1.48 Offset 6Eh: PCI ExpressPM_PMC – PCI Express* Bridge Power Management Capabilities Register (Bm:D0:F3)

Offset: 6Eh
Default Value: 01h
Attribute: RO
Size: 8 bits

Bits	Type	Reset	Description
15:11	RO	19h	**PME_Support (PMES):** Supports PME assertion on behalf of the SHPC when in the **D3**hot state. The PCI Express to PCI-X bridge does not generate PME from the **D3**cold state.
10	RO	0	**D2 Support (D2S):** Does not support the **D2** device state.
9	RO	0	**D1 Support (D1S):** Does not support the **D1** device state.
8:6	RO	0	**Aux Current (AUXC):** Does not support Aux power.
5	RO	0	**Device Specific Initialization (DSI):** The PCI Express to PCI-X bridge does not require device specific initialization when transitioned to D0 from D3hot state, so this bit is zero.
4	RO	0	Reserved.
3	RO	0	**PME Clock (PMECLK):** This is not applicable to PCI Express and hence hardwired to 0.
2:0	RO	02h	**Version (VERS):** The PCI Express to PCI-X bridge PM Implementation is compliant with the *PCI Power Management Specification Revision 1.1*.

13.6.1.49 Offset 70h: PCI Express_PMCSR – PCI Express* Bridge Power Management Control/Status Register (Bm:D0:F3)

Offset: 70– 71h
Default Value: xx000000h
Attribute: RWCS, RWS, RW, RO
Size: 16 bits

Bits	Type	Reset	Description
15	RWCS	0	**PME Status (PMEST):** This bit is set when the PCI Express to PCI-X bridge would have normally sent a PME request on behalf of SHPC, independent of the state of the **PME_En** bit. The SHPC requests a PME message when the PCI Express to PCI-X bridge is in the **D3**hot state and a Hot-Plug operation is requested. Refer to the SHPC specification for the details of PME generation.
14:13	RO	0	**Data Scale (DATS):** Data register is not implemented and hence these two bits are “0.”
12:9	RO	0	**Data Select (DATSEL):** Reserved since the Data register is not implemented.
8	RWS	0	**PME Enable (PME_EN):** Gates assertion of the PME message on behalf of the SHPC.
7:2	RO	0	Reserved.
1:0	RW	00b	**Power State (PWR_ST):** This 2-bit field is used both to determine the current power state of a function and to set the function into a new power state. The PCI Express to PCI-X bridge supported field values are given below: 00b – **D0** 01b – Reserved 10b – Reserved 11b – **D3**hot If software attempts to write an unsupported reserved state to this field, the write operation must complete normally on the bus; however, the data is discarded and no state change occurs.

13.6.1.50 Offset 72h: PCI ExpressPM_BSE—PCI Express* Bridge Power Management Bridge Support extensions (Bm:D0:F3)

Offset: 72h Attribute: RO
Default Value: 00h Size: 8 bits

Bits	Type	Reset	Description
7	RO	0	**BPCC_En (Bus Power/Clock Control Enable):** PCI Express to PCI-X bridge does not provide either bus or clock control of PCI when in D3hot state. This bit is wired to a 0.
6	RO	0	**B2/B3#:** This bit has no meaning since BPCC_En bit is a 0.
5:0	RO	0	Reserved.

13.6.1.51 Offset 73h:PCI ExpressM_DATA—PCI Express* Bridge Power Management Data Field Register (Bm:D0:F3)

Bits	Type	Reset	Description
7:0	RO	0Ch	**Data:** Does not report the data register.

13.6.1.52 Offset 78h: SHPC_CAPID—SHPC Capability Identifier Register (Bm:D0:F3)

Offset: 78h Attribute: RO
Default Value: 0Ch Size: 8 bits

Note: When Hot-Plug is disabled (HPX_SLOT[3] = 0), this register is RESERVED.

Bits	Type	Reset	Description
7:0	RO	0Ch	**SHPC Capability ID (CAPID):** Used to detect the presence of an SHPC integrated with a PCI-to-PCI bridge. The SHPC Capability ID must be set to 0Ch.

13.6.1.53 Offset 79h: SHPC_NXTP—SHPC Next Item Pointer Register (Bm:D0:F3)

Offset: 79h Attribute: RO
Default Value: 80h Size: 8 bits

Note: When Hot-Plug is disabled (HPX_SLOT[3] = 0), this register is RESERVED, and default is 00h.

Bits	Type	Reset	Description
7:0	RO	80h	**Next Capability Pointer**: Points to the PCI bridge subsystem vendor capability

13.6.1.54 Offset 7Ah: SHPC_DWSEL—SHPC DWORD Select Register (Bm:D0:F3)

Offset: 7Ah Attribute: RW/RO
Default Value: 00h Size: 8 bits

This register is used to select the DWORD offset in the SHPC working register set for read and write by the SHPC software.

Note: When Hot-Plug is disabled (HPX_SLOT[3] = 0), this register is RESERVED.

Bits	Type	Reset	Description
7:0	RW	0	**DWORD Select (DWS):** Selects the DWORD from the SHPC Working Register set that is accessible through the DWORD Data register. Accesses to the DWORD Data register have no effect on the DWORD Select field. A value of 0 selects the first DWORD of the SHPC Working set. A value of 1 selects the second DWORD, and so on. This field has a default value of 0.

13.6.1.55 Offset 7Bh: SHPC_STS—SHPC Status Register (Bm:D0:F3)

Offset: 7Bh Attribute: RO
Default Value: x0h Size: 8 bits

Note: When Hot-Plug is disabled (HPX_SLOT[3] = 0), this register is RESERVED.

Bits	Type	Reset	Description
7	RO	x	**Controller Interrupt Pending (CIP):** This bit is set when one or more bits are set in the Interrupt Locator register in the SHPC working register set. This bit is cleared when no bits are set in the Interrupt Locator register.
6	RO	x	**Controller System Error Pending (CSP):** This bit is set when one or more bits are set in the SERR Locator register in the SHPC working register set. This bit is cleared when no bits are set in the SERR Locator register.
5:0	RO	0	Reserved.

13.6.1.56 Offset 7Ch: SHPC_DWORD—SHPC Data Register (Bm:D0:F3)

Offset: 7C – 7Fh Attribute: RW/RO
Default Value: 00000000h Size: 32 bits

Note: When Hot-Plug is disabled (HPX_SLOT[3] = 0), this register is RESERVED.

Bits	Type	Reset	Description
31:0	RW	0	**DWORD Data (DWD):** This field allows software to access the SHPC Working Register set via the Capabilities List Item in Configuration Space. The DWORD Select field selects the SHPC Working Register set DWORD that is accessed by reads and writes to this register. Accessing SHPC Working Register set registers through this field behaves the same as accessing them through memory-mapped accesses. Multiple accesses to the DWORD Data register continue to affect the same DWORD if the DWORD Select field is unchanged. If the PCI-to-PCI bridge integrated with the SHPC is not in the D0 power management state, reads from this register must complete successfully but the returned value is undefined and the behavior of writes is undefined.

13.6.1.57 Offset 80h: SVID_CAPID — Subsystem and Vendor ID Capabilities Identifier Register (Bm:D0:F3)

Offset: 80h Attribute: RO
Default Value: 0Dh Size: 8 bits

Note: Identifies this item in the Capabilities list as the PCI bridge subsystem vendor capability. It returns 0Dh when read.

Bits	Type	Reset	Description
7:0	RO	0D	Identifier (ID): Indicates this is the PCI bridge subsystem vendor capability.

13.6.1.58 Offset 81h: SVID_NXTP — Next Item Pointer Register (Bm:D0:F3)

Offset: 81h
Default Value: D8h
Attribute: RO
Size: 8 bits

Note: Indicates where the next item in the capabilities list resides. Points to the PCI-X Capabilities Identifier.

Bits	Type	Reset	Description
7:0	RO	D8	Next Pointer: Points to the PCI-X capability as the next capability.

13.6.1.59 Offset 84h: SVID — Subsystem Vendor ID Register (Bm:D0:F3)

Offset: 84h
Default Value: 0000h
Attribute: RWOS
Size: 16 bits.

Bits	Type	Reset	Description
15:0	RWOS	0000	Subsystem Vendor Identifier: Indicates the manufacturer of the subsystem. This field is write once and is locked down until a power good reset occurs.

13.6.1.60 Offset 86h: SID - Subsystem Identifier Register (Bm:D0:F3)

Offset: 86h
Default Value: 0000h
Attribute: RW/RO
Size: 16 bits.

Bits	Type	Reset	Description
15:0	RWOS	0000	Subsystem Identifier: Indicates the subsystem as identified by the vendor. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).

13.6.1.61 Offset D8h: PX_CAPID—PCI-X* Capability Identifier Register (Bm:D0:F3)

Offset: D8h
Default Value: 07h
Attribute: RO
Size: 8 bits

This register identifies this item in the Capabilities list as a PCI-X register set. It returns 07h when read.

Bits	Type	Reset	Description
7:0	RO	07h	**Capability Identifier (CAPID):** A value of 07h in this field indicates this is a PCI-X capabilities list.

13.6.1.62 Offset D9h: PX_NXTCP—PCI-X* Next Capabilities Pointer Register (Bm:D0:F3)

Offset: D9h
Default Value: 0h
Attribute: RO
Size: 8 bits

This register points to the next item in the Capabilities List, as required by the PCI 2.3 Specification.

Bits	Type	Reset	Description
7:0	RO	0h	**Next Capabilities Pointer (NCPTR):** Last capability structure in the link, so it is hardwired to 0.

13.6.1.63 Offset DAh: PX_SSTS—PCI-X* Secondary Status Register (Bm:D0:F3)

Offset: DA–DBh
Default Value: 0003h
Attribute: RWC, RO
Size: 16 bits

This register controls various modes and features of the PCI-X device.

Bits	Type	Reset	Description
15:9	RO	0	Reserved.
8:6	RO	x	**Secondary Clock Frequency (SCF):** This field is set with the frequency of the secondary bus. The values are: BitsMax FrequencyClock Period 000PCI ModeN/A 00166 PCI-X Mode 115 010100 PCI-X Mode 110 011133 PCI-X Mode 17.5 1xxReservedReserved
5	RO	0	**Split Request Delayed. (SRD):** The PCI Express to PCI-X bridge will never set this bit.
4	RO	0	**Split Completion Overrun (SCO):** The PCI Express to PCI-X bridge will never set this bit.
3	RWC	0	**Unexpected Split Completion (USC):** 0 = This bit is cleared by writing a 1 to it. 1 = This bit is set if an unexpected split completion with a requester ID equal to the PCI Express to PCI-X bridge's PCI/PCI-X secondary bus number is received on the PCI/PCI-X interface.
2	RWC	0	**Split Completion Discarded (SCD):** 0 = This bit is cleared by writing a 1 to it. 1 = PCI Express to PCI-X bridge discarded a split completion moving toward the secondary bus because the requester would not accept it.
1	RO	1	**133 MHz Capable (C133):** Hardwired to 1; indicates that the PCI Express to PCI-X bridge's PCI/PCI-X interface is capable of 133 MHz operation in PCI-X mode.
0	RO	1	**64-bit Device (D64):** Hardwired to 1; indicates the width of the secondary bus as 64 bits.

13.6.1.64 Offset DCh: PX_BSTS—PCI-X* Bridge Status Register (Bm:D0:F3)

Offset: DC – DFh
Default Value: 00030000h (PCI Bus A)
00030002h (PCI Bus B)
Attribute: RWC, RO
Size: 32 bits

Bits	Type	Reset	Description
31:22	RO	0	*Reserved*. Note: Bit[31] is set to 0 as PCI-X 533 is not supported Bit[30] is set to 0 as PCI-X 266 is not supported Bit[29] is set to 0 as ECC for secondary interface is not supported Bit[28:23] is reserved per PCI-X Spec 2.0 Bit[22] is set to 0 as ECC for primary interface is not supported
21	RO	0	**Split Request Delayed (SRD):** Hardwired to 0. This bit is not supported by the PCI Express to PCI-X bridge, because it will never be in a position where it cannot issue a request.
20	RO	0	**Split Completion Overrun (SCO):** Hardwired to 0. This bit is not set by the PCI Express to PCI-X bridge because the PCI Express to PCI-X bridge never requests on the PCI Express interface more data than it has room to receive.
19	RWC	0	**Unexpected Split Completion (USC):** The PCI Express to PCI-X bridge sets this field when a completion on the PCI Express bus is destined to one of the PCI bus segment (either A or B) but the tag does not match.

Bits	Type	Reset	Description
18	RO	0	**Split Completion Discarded (SCD):** Hardwired to 0. This does not apply to the PCI Express interface.
17	RO	0	**133 MHz Capable (C133):** Hardwired to 1. This field does not apply to PCI Express.
16	RO	0	**64-bit Device (D64):** This field really does not apply to the PCI Express interface, but is set to '1' to be software-compatible.
15:8	RW	0	Reserved.
7:3	RO	0	Reserved.
2:0	RO	03h	Function Number (FNUM): The function number is 03h.

13.6.1.65 Offset E8h: BG_ECCSTS – Bridge ECC Control and Status Register (Bm:D0:F3)

Offset: E8 – EB
Default Value: 00000001h (Parity Mode)
Attribute: RWC, ROS, RO
Size: 32 bits

Bits	Type	Reset	Description
31	RO	0-PCI/PCI-X Mode1	**Mode (MODE):** Writes to this register do not affect this bit unless the ECC Control Update Enable bit is a 1 in the data pattern being written. Bit Value — Mode of Operation 0b — PCI Interface is in Parity Mode. 1b — Reserved
30	RWT	0	**Disable Single-Bit-Error Correction (DSBEC):** If the bus is in parity mode, this bit has no meaning and is ignored by the PCI Express-to-PCI-X bridge. Writes to this register do not affect this bit unless the ECC Control Update Enable bit is a 1 in the data pattern being written.
29	RO	0	Reserved.
28	WT	0	Reserved.
27:24	ROS	0	Reserved.
23:20	ROS	0	Reserved.
19:16	ROS	0	Reserved.
15:8	ROS	0	**Syndrome (SYND):** The syndrome indicates information about the bit or bits that are in error. Refer to the *PCI-X Protocol Addendum to the PCI Local Bus Specification Revision 2.0*, Section 5.
7	ROS	0	Reserved.
6:4	RWC	0	Reserved.
3	RWC	0	Reserved.
2	RWC	0	Reserved.
1	RO	0	Reserved.
0	RO	1	Reserved.

13.6.1.66 Offset ECh: PX_ECCFA – Bridge ECC Error First Address Register (Bm:D0:F3)

Offset: EC – EFh
Attribute: ROS
Default Value: 00000000h
Size: 32 bits

Least significant address bits of the failing transaction.

Bits	Type	Reset	Description
31:0	ROS	0	**ECC First Address (ECC_FA):** If the ECC Error Phase register is non-zero (indicating that an error has been captured), this register indicates the contents of the AD[31::00] bus for the address phase of the transaction that included the error. If the ECC Error Phase is zero, the contents of this register are undefined. This register always records the least significant 32 bits of the address, regardless of the type or length of the transaction, or the phase in which the error occurred. The PCI Express to PCI-X bridge stores information from the failing transaction directly from the bus (***uncorrected***), even if correction of the error is possible.

13.6.1.67 Offset F0h: PX_ECCSA – Bridge ECC Error Second Address Register (Bm:D0:F3)

Offset: F0 – F3h
Attribute: ROS
Default Value: 00000000h
Size: 32 *bits

Most significant address bits of the failing transaction.

Bits	Type	Reset	Description
31:0	ROS	0	**ECC Second Address (ECC_SA):** If the ECC Error Phase register is non-zero (indicating that an error has been captured), this register indicates the contents of the AD[63::32] bus for the address phase of the transaction that included the error. If the ECC Error Phase is zero, the contents of this register are undefined. This register always records the most significant 32 bits of the address, regardless of the type or length of the transaction, or the phase in which the error occurred. The PCI Express to PCI-X bridge stores information from the failing transaction directly from the bus (uncorrected), even if correction of the error is possible.

13.6.1.68 Offset F4h: PX_ECCATTR — Bridge ECC Attribute Register (Bm:D0:F3)

Offset: F4 – F7h
Attribute: ROS
Default Value: 00000000h
Size: 32 bits

Describes the attributes of the ECC.

Bits	Type	Reset	Description
31:0	ROS	0	**ECC Attribute (ECC_AT):** If the ECC Error Phase register bits are non-zero (indicating that an error has been captured), the ECC Attribute register indicates the contents of the AD[31::00] bus for the attribute phase of the transaction that included the error. If the ECC Error Phase registers is zero, the contents of this register are undefined. This register records the contents of the bus during the attribute phase, regardless of the type or length of the transaction, or the phase in which the error occurred. The PCI Express-to-PCI-X bridge stores information in this register from the failing transaction directly from the bus (uncorrected), even if correction of the error is possible.

13.7 PCI Express* to PCI-X* Bridges (Bm:D0:F3) Enhanced

The enhanced PCI Express configuration access mechanism utilizes a flat memory-mapped address space to access device configuration registers. In this case, the memory address determines the configuration register accessed and the memory data returns the contents of the addressed register. Refer to the Section 7.9 in the *PCI Express* Base Specification*, Revision 1.0 for details.

13.7.1 Configuration Registers

13.7.1.1 Offset 100h: PCI Express_CAPID – PCI Express* Capability Identifier Register (Bm:D0:F3)

Offset: 100 – 103h
Default Value: 30000000h
Attribute: RO
Size: 32 bits

This register stores the PCI Express extended capability ID value.

Bits	Type	Reset	Description
31:20	RO	000h	**Next PCI Express Extended Capability Pointer:** Next is the power budgeting capability.
19:16	RO	1h	**Capability Version Number:** PCI Express Advanced Error Reporting Extended Capability Version Number.
15:0	RO	0001h	**PCI Express Extended Capability ID (EXP_XCAPID):** PCI Express Extended Capability ID indicating Advanced Error Reporting Capability.

13.7.1.2 Offset 104h: PEX_ERRUNC_STS – PCI Express Uncorrectable Error Status Register (Bm:D0:F3)

Offset: 104h
Default Value: 0000000h
Attribute: RW
Size: 32 bits

The uncorrectable error status register reports error status of individual uncorrectable error sources. An individual error status bit that is set to ì1î indicates that a particular error occurred; software may clear an error status by writing a 1 to the respective bit.

Bits	Type	Reset	Description
31:21	RO	0	Reserved
20	RW	0	Unsupported Request Error Status: Set by PCI Express Bridge/Switch whenever an unsupported request is detected on PCI Express including those that master abort on the switch or signaled by the SHPC (on write data parity errors ñ config and mem)
19	RO	0	ECRC Check: PCI Express Bridge/Switch does not do ECRC check and this bit is never set.
18	RW	0	Malformed TLP: PCI Express Bridge/Switch sets this bit when it receives a malformed TLP. Header logging is done.
17	RW	0	Receiver Overflow: PCI Express Bridge/Switch would set this if receive buffers overflow
16	RW	0	Unexpected Completion: PCI Express Bridge/Switch sets this bit whenever it receives a completion with a requestor id that does not match or when it receives a completion with a matching requestor id but an unexpected tag field. PCI Express Bridge/Switch logs the header of the unexpected completion
15	RW	0	Completer Abort: PCI Express Bridge/Switch sets this bit and logs the header associated with the request when SHPC signals a completer abort. PCI Express Bridge/Switch logs the header.

Bits	Type	Reset	Description
14	RW	0	Completion Timeout: PCI Express Bridge/Switch sets this bit when inbound memory/config/IO reads do not receive completions within 16-32ms.
13	RW	0	Flow Control Protocol Error Status: PCI Express Bridge/Switch sets this bit when there is a flow control protocol error detected
12	RW	0	Poisoned TLP Received: PCI Express Bridge/Switch sets this bit when a poisoned TLP is received from PCI Express. Note that internal queue errors in the J and B unit s are not covered by this bit. PCI Express Bridge/Switch logs the header of the poisoned TLP packet
11:5	RO	0	Reserved
4	RW	0	Data Link Protocol Error: PCI Express Bridge/Switch sets this bit when there is a data link protocol error detected.
3:1	RO	0	Reserved
0	Undefined	Undefined	**Undefined –** The value read from this bit is undefined. In previous versions of this specification, this bit was used to indicate a Link Training Error. System software must ignore the value read from this bit. System software is permitted to write any value to this bit.

13.7.1.3 Offset 108h: PEX_ERRUNC_MSK - PCI Express Uncorrectable Error Mask Register

Offset: 108h Attribute: RW
Default Value: 0000000h Size: 32 bits

The Uncorrectable Error Mask register controls reporting of individual uncorrectable errors by device to the host bridge via a PCI Express error message and also the logging of the header. Refer to PCI Express spec for details of how the mask bits function. A masked error (respective bit set in mask register) is not reported to the host bridge by PCI Express Bridge/Switch, nor is the header logged (status bits unaffected by the mask bit) or the pointer updated. There is a mask bit per bit of the Uncorrectable Error Status register.

Bits	Type	Reset	Description
31:21	RO	0	Reserved
20	RW	0	Unsupported Request Error Mask
19	RO	0	ECRC Check: N/A to PCI Express Bridge/Switch Mask
18	RW	0	Malformed TLP Mask
17	RW	0	Receiver Overflow Mask
16	RW	0	Unexpected Completion Mask
15	RW	0	Completer Abort Mask
14	RW	0	Completion Timeout Mask
13	RW	0	Flow Control Protocol Error Status Mask
12	RW	0	Poisoned TLP Received Mask
11:5	RO	0	Reserved
4	RW	0	Data Link Protocol Error Mask
3:1	RO	0	Reserved
0	Undefined	Undefined	**Undefined –** The value read from this bit is undefined. In previous versions of this specification, this bit was used to indicate a Link Training Error. System software must ignore the value read from this bit. System software is permitted to write any value to this bit.

13.7.1.4 Offset 10Ch: PEX_ERRUNC_SEV - PCI Express Uncorrectable Error Severity (Bm:D0:F3)

Offset: 10Ch Attribute: RW
Default Value: See Description Size: 32 bits

The Uncorrectable Error Severity register controls whether an individual uncorrectable error is reported as a fatal error. An uncorrectable error is reported as fatal (ERR_FATAL) when the corresponding error bit in the severity register is set. If the bit is cleared, the corresponding error is considered non-fatal (ERR_NONFATAL).

Bits	Type	Reset	Description
31:21	RO	0	Reserved
20	RW	0	Unsupported Request Error Severity
19	RO	0	ECRC Check: N/A to Intel® 631xESB/632xESB I/O Controller Hub Severity
18	RW	1	Malformed TLP Severity
17	RW	1	Receiver Overflow Severity
16	RW	0	Unexpected Completion Severity
15	RW	0	Completer Abort Severity
14	RW	0	Completion Timeout Severity
13	RW	1	Flow Control Protocol Error Severity
12	RW	0	Poisoned TLP Received Severity
11:5	RO	0	Reserved
4	RW	1	Data Link Protocol Error Severity
3:1	RO	0	Reserved
0	Undefined	Undefined	**Undefined –** The value read from this bit is undefined. In previous versions of this specification, this bit was used to indicate a Link Training Error. System software must ignore the value read from this bit. System software is permitted to write any value to this bit.

13.7.1.5 Offset 110h: PEX_ERRCOR_STS - PCI Express Correctable Error Status (Bm:D0:F3)

Offset: 110h Attribute: RW
Default Value: 0000h Size: 32 bits

The Correctable error status register reports error status of individual correctable error sources on a PCI Express device. When an individual error status bit is set to ì1î it indicates that a particular error occurred; software may clear an error status by writing a 1 to the respective bit.

Bits	Type	Reset	Description
31:13	RO	0	Reserved
12	RW	0	Replay Timer Timeout Status: PCI Express Bridge/Switch sets this bit if replay timer timeout happened.
11:9	RO	0	Reserved
8	RW	0	Replay Number Rollover Status: PCI Express Bridge/Switch sets this bit when the replay number rolls over from 11 to 00.
7	RW	0	Bad DLLP Status: PCI Express Bridge/Switch sets this bit on CRC errors on DLLP

Bits	Type	Reset	Description
6	RW	0	Bad TLP Status: PCI Express Bridge/Switch sets this bit on CRC errors on TLP
5:1	RO	0	Reserved
0	RW	0	Receiver Error: PCI Express Bridge/Switch sets this bit when the physical layer detects a receiver error.

13.7.1.6 Offset 114h: PEX_ERRCOR_MSK - PCI Express Correctable Error Mask (Bm:D0:F3)

Offset: 114h Attribute: RW
Default Value: See Description Size: 32 bits

The Correctable error mask register controls reporting of individual correctable errors via ERR_COR message. A masked error (respective bit set in mask register) is not reported to the host bridge by PCI Express Bridge/Switch. There is a mask bit per error in the Correctable Error Status register.

Bits	Type	Reset	Description
31:13	RO	0	Reserved
12	RW	0	Replay Timer Timeout Mask: PCI Express Bridge/Switch sets this bit if replay timer timeout happened.
11:9	RO	0	Reserved
8	RW	0	Replay Number Rollover Mask: PCI Express Bridge/Switch sets this bit when the replay number rolls over from 11 to 00.
7	RW	0	Bad DLLP Mask: PCI Express Bridge/Switch sets this bit on CRC errors on DLLP
6	RW	0	Bad TLP Mask: PCI Express Bridge/Switch sets this bit on CRC errors on TLP
5:1	RO	0	Reserved
0	RW	0	Receiver Error Mask: PCI Express Bridge/Switch sets this bit when the physical layer detects a receiver error.

13.7.1.7 Offset 118h: PEX_ADVERR_CTL - Advanced Error Control and Capabilities Register (Bm:D0:F3)

Offset: 118h Attribute: RW
Default Value: 0000h Size: 32 bits

The register gives the status and control for ECRC checks and also the pointer to the first uncorrectable error that happened.

Bits	Type	Reset	Description
31:9	RO	0	Reserved
8	Ro	0	ECRC Check Enable: Intel® 631xESB/632xESB I/O Controller Hub does not support ECRC check and this bit is reserved
7	RO	0	ECRC Check Capable: Intel® 631xESB/632xESB I/O Controller Hub is not ECRC check capable
6	RO	0	ECRC Generation Enable: Intel® 631xESB/632xESB I/O Controller Hub cannot generated ECRC and this bit is ignored by Intel® 631xESB/632xESB I/O Controller Hub
5	RO	0	ECRC Generation Capable: Intel® 631xESB/632xESB I/O Controller Hub cannot generated ECRC
4:0	RO	0	The First Error Pointer: Identifies the bit position of the first error reported in the Uncorrectable Error Status register. This register rearms itself (which does not change its current value) once the error status bit pointed to by the pointer is cleared by software by writing a 1 to that status bit.

13.7.1.8 Offset 11Ch: PEX_HDRLOG - PCI Express Transaction Header Log Register (Bm:D0:F3)

Offset: 118h
Default Value: 0
Attribute: RW
Size: 128 bits

Transaction header log for PCI Express error.

Bits	Type	Reset	Description
127:0	RO	0	Header of the PCI Express packet in error. Once an error is logged in this register, it remains locked for further error loggings until the time the software clears the status bit that cause the header log that is, the error pointer is rearmed to log again.

13.7.1.9 Offset 12Ch: PCIXERRUNC_STS - Uncorrectable PCI/X Error Status Register (Bm:D0:F3)

Offset: 12C – 12Dh
Default Value: 0000h
Attribute: RWCS, RO
Size: 16 bits

This register reports error status of individual errors generated on the PCI-X bus interface. An individual error status bit that is set to a 1 indicates that a particular error occurred; software may clear an error status by writing a 1 to the respective bit. Refer to Section 10 of the *PCI Express* to PCI/PCI-X* Bridge Specification* Revision 1.0 for more details.

Bits	Type	Reset	Description
15:14	RO	0	Reserved.
13	RWCS	0	**Internal Bridge Error (IBERR):** Accounts for internal data errors in the PCI Express to PCI-X bridge's data queues in either direction. The PCI Express to PCI-X bridge does NOT log any headers for this error.
12	RWCS	0	**PCI-X SERR# Assertion Detected (SERRAD):** The PCI Express to PCI-X bridge sets this bit whenever it detects the PCI SERR# pin is asserted. There is no header logging associated with the setting of this bit.
11	RWCS	0	**PCI-X PERR# Assertion Detected (PERRAD):** The PCI Express to PCI-X bridge sets this bit whenever it detects the PCI bus PERR# pin asserted when it is mastering a write (memory, I/O or configuration) or a split/delayed read completion on the PCI bus. The PCI Express to PCI-X bridge logs the header of the transaction in which the PERR# was detected (regardless of the data phase in which it is detected), in the PCI-X header log register. Note that this status bit and also the associated header log are always done irrespective of whether the PERR# detected was because of a PCI bus error or because of a forwarded poisoned data. But error message escalation to PCI Express is done only if the PERR# detected and was a NOT because of forwarded poisoned data.
10	RWCS	0	**PCI Delayed Transaction Timer Expired (DTTE):** This bit is set by the PCI Express to PCI-X bridge if it detects that a DT timeout has happened on a hard DT read stream or on an inbound I/O or configuration transaction. No header is logged.
9	RWCS	0	**PCI-X Uncorrectable Address Error Detected (UADED):** The PCI Express to PCI-X bridge sets this bit when it is the target of an inbound transaction and an address parity error was detected by the PCI Express to PCI-X bridge (regardless of whether the bus mode is PCI or PCI-X Mode 1). The PCI Express to PCI-X bridge logs the header of the transaction in which it detected the address/attribute parity error in the PCI/X header log register.
8	RWCS	0	**PCI-X Uncorrectable Attribute Error Detected (UATED):** The PCI Express to PCI-X bridge sets this bit when it is the target of an inbound transaction and an attribute parity error was detected by the PCI Express to PCI-X bridge. The PCI Express to PCI-X bridge logs the header of the transaction in which it detected the address/attribute parity error in the PCI-X header log register.

Bits	Type	Reset	Description
7	RWCS	0	**PCI-X Uncorrectable Data Error Detected (UDED):** The PCI Express-to-PCI-X bridge sets this bit in all PCI modes (PCI and PCI-X Mode 1) when it is the target of an inbound transaction or when it is mastering a PCI delayed read with target sourcing data to the PCI Express to PCI-X bridge, and a data parity error was detected by the PCI Express to PCI-X bridge. The PCI Express to PCI-X bridge logs the header of the transaction in which it detected the data parity error in the PCI-X header log register.
6	RWCS	0	**Uncorrectable Split Completion Message Data Error (USCMDE):** This bit is set when a split completion message is received with an uncorrectable data parity error.
5	RWCS	0	**Unexpected Split Completion Error (USCE):** This bit is set when a completion is received from PCI-X that matches the bus number range on the primary side of the PCI Express to PCI-X bridge, but the RequestorID:tag combination does not match one of the non-posted transactions that PCI Express to PCI-X bridge has outstanding on the PCI-X bus.
4	RO	0	Reserved.
3	RWCS	0	**PCI-X Detected Master Abort Status:** The PCI Express to PCI-X bridge sets this bit when it is the master of a request transaction on the PCI bus and it received a master abort. The header is logged for that transaction.
2	RWCS	0	**PCI-X Detected Target-Abort (optional in spec):** The PCI Express to PCI-X bridge sets this bit when it is the master of a request transaction on the PCI-X bus and it received a target abort. The header is logged for that transaction.
1	RWCS	0	**PCI-X Detected Split Completion Master Abort:** The PCI Express to PCI-X bridge sets this bit when a split completion it sends on the PCI-X bus (Mode 1) master aborts. The PCI Express to PCI-X bridge logs the header of the split completion.
0	RWCS	0	**PCI-X Detected Split Completion Target Abort (optional in spec):** The PCI Express-to-PCI-X bridge sets this bit when a split completion it sends on the PCI-X bus (Mode 1) target aborts. The PCI Express to PCI-X bridge logs the header.

13.7.1.10 Offset 130h: PCIXERRUNC_MSK– Uncorrectable PCI-X* Error Mask Register (Bm:D0:F3)

Offset: 130 – 133h Attribute: RWS, RO
Default Value: 000017A8h Size: 32 bits

This register masks the reporting of individual PCI-X uncorrectable errors via a PCI Express error message. There is one mask bit per error. Note that the status bits are set in the status register irrespective of whether the mask bit is on or off. The mask bit also affects the header log for the PCI-X transaction. If the mask bit is on, the header is not logged and no error message is generated on the PCI Express bus.

Bits	Type	Reset	Description
31:14	RO	0	Reserved.
13	RWS	0	**Internal Bridge Error (IBE)**
12	RWS	1	**PCI-X SERR# Assertion Mask (SEAM)**
11	RWS	0	**PCI-X PERR# Assertion Mask (PEAM)**
10	RWS	1	**PCI Delayed Transaction Timer Expired Mask (DTTEM)**
9	RWS	1	**PCI-X Uncorrectable Address Parity Error Mask (UADDEM)**
8	RWS	1	**PCI-X Uncorrectable Attribute Parity Error Mask (UATTEM)**
7	RWS	1	**Uncorrectable Data Parity Error Mask (UDEM)**
6	RWS	0	**Uncorrectable Split Completion Message Data Error Mask (USCMDE)**
5	RWS	1	**Unexpected Split Completion Error (USCE)**
4	RO	0	Reserved.
3	RWS	1	**PCI-X Master-Abort Mask (MAM)**

Bits	Type	Reset	Description
2	RWS	0	**PCI-X Received Target-Abort Mask (RTAM)**
1	RWS	0	**Master-Abort on Split Completion Mask (MASCM)**
0	RWS	0	**Target-Abort on Split Completion Mask (TASCM)**

13.7.1.11 Offset 134h: SEC_UNC_ERRSEV – Secondary Uncorrectable Error Severity Register (Bm:D0:F3)

Offset: 134 – 135h
Default Value: 2340h
Attribute: RWS, RO
Size: 16 bits

This register controls whether an individual PCI-X uncorrectable error is reported as a fatal or non-fatal error. A PCI-X uncorrectable error, if enabled, is reported as fatal (an ERR_FATAL message will be generated on the PCI Express bus) when the corresponding error bit in the severity register is set to a 1. If a bit is set to 0, then the corresponding error, if enabled, is considered non-fatal (and thus a ERR_NONFATAL message will be generated on the PCI Express bus). There is one mask bit per error.

Bits	Type	Reset	Description
15:14	RO	0	Reserved.
13	RWS	0	**Internal Bridge Error Severity (IBES)**
12	RWS	1	**PCI-X SERR# Assertion Severity (SEAS)**
11	RWS	0	**PCI-X PERR# Assertion Severity (PEAS)**
10	RWS	0	**Delayed Transaction Timer Expired Severity (DTTES)**
9	RWS	1	**PCI-X Uncorrectable Address Error Severity (UADDES)**
8	RWS	1	**PCI-X Uncorrectable Attribute Error Severity (UATTES)**
7	RWS	0	**PCI-X Uncorrectable Data Error Severity (UDES)**
6	RWS	1	**Uncorrectable Split Completion Message Data Error Severity (USCMDES)**
5	RWS	0	**Unexpected Split Completion Error Severity (USCES)**
4	Ro	0	Reserved.
3	RWS	0	**PCI-X Master-Abort Severity (MAS)**
2	RWS	0	**PCI-X Received Target-Abort Severity (RTAS)**
1	RWS	0	**PCI-X Master-Abort on Split Completion Severity (MASCS)**
0	RWS	0	**PCI-X Target-Abort on Split Completion Severity (TASCS)**

13.7.1.12 Offset 138h: PCIXERRUNC_PTR – Uncorrectable Error Pointer Register (Bm:D0:F3)

Offset:	138 – 13Bh	Attribute:	ROS, RO
Default Value:	00000000h	Size:	32 bits

This register points to the bit position of the first error reported in the Uncorrectable PCI/PCI-X Error Status register (offset 12Ch). This register is rearmed when the bit position pointed to is cleared in the associated status register. The pointer value is not updated when this register is rearmed.

Bits	Type	Reset	Description
31:4	RO	0	Reserved.
3:0	ROS	0	**Uncorrectable PCI/PCI-X First Error Pointer (UPFEP):** This register points to the first error that was logged in the Uncorrectable PCI/PCI-X Error Status register (offset 12Ch). This register rearms itself when the status bit corresponding to the error which this register is pointing to is cleared by software writing a 1 to the bit.

13.7.1.13 Offset 13Ch: PCIXHDLOG – PCI-X* Uncorrectable Transaction Header Log Register (Bm:D0:F3)

Offset:	13C – 143h	Attribute:	ROS
Default Value:	0h	Size:	128 bits

The log in this register captures the header for the transaction that generated an error. Once an error is logged in this register, this register is locked from further error loggings, until software clears the status bit corresponding to the 1st uncorrectable error that occurred. When this bit is cleared by software, this register is rearmed for further header logs.

Bits	Type	Reset	Description
127:64	ROS	0	**Transaction Address (TXNAD):** These bits capture the 64-bit value transferred on PxAD[31:0] during the 1st and 2nd address phase of the transaction in which an error was detected. The 1st address phase is logged to bits 95:64 and the 2nd address phase is logged to bits 127:96. In case of a 32-bit address, bits 127:96 will be set to all zeros. The address is logged on all error conditions.
63:44	RO	0	Reserved.
43:40	ROS	0	**Transaction Command Upper (TXNCU):** This captures the value of PxC/BE[3:0]# during the 2nd address phase of a DAC transaction Contains the 4-bit value transferred on PxC/BE[3:0]# during the 2nd attribute phase of the transaction.
39:36	ROS	0	**Transaction Command Lower (TXNCL):** This captures the value of PxC/BE[3:0]# during the 1st address phase of the transaction. Contains the 4-bit value transferred on PxC/BE[3:0]# during the 1st attribute phase of the transaction.
35:0	ROS	0	**Transaction Attribute (TXNAT):** This carries the attribute of the transaction. Contains the 36-bit value transferred on PxC/BE[3:0]# and PxAD[31:0]) during the attribute phase of the transaction. When the bus is in PCI mode, these bits are all zeros.

13.7.1.14 Offset 14Ch: PCIXDLOG – PCI-X* Uncorrectable/Correctable Data Error Log Register (Bm:D0:F3)

Offset: 14C – 153h Attribute: ROS
Default Value: 0000000000000000h Size: 64 bits

This register is logged for all correctable or uncorrectable data parity errors.

Bits	Type	Reset	Description
63:0	ROS	0	**PCI-X Data Log (PDL):** This register is logged with the PCI data bus value whenever the PCI Express to PCI-X bridge is the target of a data transfer and it detects a data parity error (correctable or uncorrectable). This register is not defined if the log valid bit in the error log and control register is not set. This register re-arms itself for loading again when software clears the log valid bit by writing a 1 to that bit. For 32-bit data transfers, only the lower 32 bits are logged.

13.7.1.15 Offset 154h: PCIXERRLOGCTL – Other PCI-X* Error Logs and Control Register (Bm:D0:F3)

Offset: 154 – 155h Attribute: RWCS, ROS, RO
Default Value: 0000000000000000h Size: 32 bits

This register contains bits logged for uncorrectable data parity errors (in PCI or PCI-X Mode 1), uncorrectable address/attribute parity errors and PCI REQ# line of failure.

Bits	Type	Reset	Description
31:19	RO	0	Reserved.
18	ROS	0	**Data Log (DATA_LOG):** A “1” indicates the data log is from a correctable ECC data error. A 0 indicates the data log is from an uncorrectable ECC/parity error. This bit is logged along with the DLOG register and is rearmed when the log valid bit is cleared. This is also only valid when the log valid bit is set by the PCI Express to PCI-X bridge.
17	ROS	0	**PCI-X Attribute Parity (PP)**: This bit indicates that parity was detected in the attribute phase of a request and completion. When the PCI Express to PCI-X bridge is driving, it is the value driven. When the PCI Express to PCI-X bridge is receiving, it is the value captured. This bit is only valid in PCI-X Mode 1 operation. This bit is logged along with the Secondary Header Log register (SEC_HDLOG, offset 13Ch) when there is an attribute parity error. This bit is not loaded for any other error conditions. This bit remains set until software clears the corresponding status bit in the Secondary Uncorrectable Error Status register (SEC_UNC_ERRSTS, offset 12Ch).
16	ROS	0	**PCI Address High (PAH):** This bit represents the parity detected in the 2nd phase (upper 32-bits) of a dual address cycle. This bit is forced to ‘0’ if the address was a single address cycle. When the PCI Express to PCI-X bridge is driving, this bit contains the value driven. When the PCI Express to PCI-X bridge is receiving, this bit contains the value captured. This is only valid in PCI-X Mode 1 operation. This bit is logged along with the Secondary Header Log register (SEC_HDLOG, offset 13Ch) when there is an address parity error (this bit is never loaded independently of the Secondary Header Log register). This bit is not loaded for any other error conditions. This bit remains set until software clears the corresponding status bit in the Secondary Uncorrectable Error Status register (SEC_UNC_ERRSTS, offset 12Ch).

Bits	Type	Reset	Description
15	ROS	0	**PCI Address Low (PAL):** For PCI-X requests and all PCI cycles, this bit represents the parity detected in the 1st phase (lower 32-bits) of a dual address cycle, or just the address of a regular address cycle. For PCI-X completions, this bit represents the 1st clock (requester attributes) driven in the completion cycle. When the PCI Express to PCI-X bridge is driving, this bit contains the value driven. When the PCI Express to PCI-X bridge is receiving, this bit contains the value captured. This is only valid in PCI-X Mode 1 operation. This bit is logged along with the Secondary Header Log register (SEC_HDLOG, offset 13Ch) when there is an address parity error (this bit is never loaded independently of the PCI-X Header Log register). This bit is not loaded for any other error conditions. This bit remains set until software clears the corresponding status bit in the Secondary Uncorrectable Error Status register (SEC_UNC_ERRSTS, offset 12Ch).
14	RWCS	0	**REQ# Log Valid (RLV):** This bit is set when REQ# log bits (bits 13:11 of this register) are valid. Clearing this bit will re-enable logging into the REQ# log register bits.
13:11	ROS	0	**REQ# Log (RL):** These bits capture the REQ# of the PCI agent mastering the transaction when the PCI Express to PCI-X bridge detected a correctable or uncorrectable address, attribute or data parity error. That is, the REQ# log is valid when either of the three error conditions occur that cause either of bits 9:7 to be set or any errors occur that cause the error phase register bits in the Bridge ECC Control and Status register (BG_ECCSTS, offset E8h) to be non-zero. Once a log is made in the REQ# log, further logging of the REQ# log bits is stopped till the REQ# log valid bit (bit 14 of this register) is cleared. Note that this register is not dependent on the clearing of status bits in the Secondary Uncorrectable Error Status register (SEC_UNC_ERRSTS, offset 12Ch) or the Bridge ECC Attribute register (BG_ECCATTR, offset F4h), to rearm itself. 000 = REQ0 001 = REQ1 010 = REQ2 011 = REQ3 100 = REQ4 101 = REQ5 110 = REQ6 111 = Reserved
10	RO	0	Reserved.
9	RWCS	0	**Log Valid (LOGV):** This is set by the PCI Express to PCI-X bridge whenever it logs a value in the Data Log register (offset 14Ch) and also the byte enable log bits in this register (offset 154h, bits 7:0). Software clears this register by writing a 1, which will rearm the Data Log register (offset 14Ch) and enable the byte enable log register bits (bits 7:0 of this register) to start loading again.
8	ROS	0	**Data Bus Width (DBW):** This bit is set if the data logged in the Data Log register is 64 bits. Otherwise this bit is clear. When clear the upper 32 bits of the Data Log registers are invalid.
7:0	ROS	0	**PCI-X Byte Enable Log (PXBEL):** This error is logged whenever the PCI Express to PCI-X bridge is the target of a data transfer and it detects a data parity/ECC error (correctable or uncorrectable). This register is logged along with the Data Log register. This register is not defined if the log valid bit (bit 9 above) is not set. This register re-arms itself for loading again when software clears the log valid bit by writing a one to that bit.

13.8 Hot-Plug Controller Registers

The Standard Hot-Plug Controller allows PCI card removal, replacement and addition without powering down the system.

13.8.1 Memory-Mapped Registers

Table 13-5. Hot-Plug Controller Register Summary

Address Offset	Symbol	Register Name	Default	Access
00-03h	SHPC_BASEOFF	SHPC Base Offset Register	00000000h	RO
04-07h	SLOTS_AVAIL1	Slots Available I Register	00000000h	RWO
08-0Bh	SLOTS_AVAIL2	Slots Available II Register	00000000h	RWO
0C-0Fh	SLOT_CONFIG	Slot Configuration Register	00000000h	RWO
10-11h	SBUS_CONFIG	Secondary Bus Configuration Register	0000h	RO
12h	SHPC_MSI_CNTL	SHPC MSI Control Register	00h	RO
13h	SHPC_PROG_IF	SHPC Programming Interface Register	01h	RO
14-15h	CONT_COMMAND	Controller Command Register	0000h	RW
16-17h	CONT_COMMAND_STS	Controller Command Status Register	0000h	RO
18-1Bh	INT_LOC	Interrupt Locator Register	00000000h	RO
1C-1Fh	SERR_LOC	SERR Locator Register	00000000h	RO
20-23h	SERR_INT	Controller SERR-INT Enable Register	0000000Fh	RW, RWC
24-3Bh	1_LSR	1st Logical Slot Register	8F00xxxxh	RW
	2_LSR	2nd Logical Slot Register		RW
	3_LSR	3rd Logical Slot Register		RW
	4_LSR	4th Logical Slot Register		RW
	5_LSR	5th Logical Slot Register		RW
	6_LSR	6th Logical Slot Register		RW

13.8.1.1 Offset 00h: SHPC_BASEOFF—SHPC Base Offset Register

Offset: 00–03h Attribute: RO
Default Value: 00000000h Size: 32 bits

This register is used by software and/or BIOS (in conjunction with the SHPC Base Address Register, SHPC_BAR) to determine the memory base address of the SHPC Working Register set. This register must be accessed initially via Configuration Space.

Bits	Type	Reset	Description
31:0	RO	0	**SHPC Base Offset (SHPCBO):** This field contains the byte offset that must be added to the 64-bit Base Address register SHPC_BAR in the PCI Express to PCI-X bridge's configuration space to access the SHPC Working Register set using memory-mapped accesses. The PCI Express to PCI-X bridge has the working register set starting at offset 0.

13.8.1.2 Offset 04h: SLOTS_AVAIL1—Slots Available I Register

Offset: 04–07h
Default Value: 00000000h
Attribute: RWO, RO
Size: 32 bits

The SHPC uses five Number of Slots Available fields organized into two Slots Available registers, this register (SLOTS_AVAIL1) being the first and SLOTS_AVAIL2 (offset 08h) being the second. Each Number of Slots Available field specifies the maximum number of Hot-Plug slots that are permitted to be enabled at the given BnPCI/PCI-X mode and frequency on the associated PCI/PCI-X bus segment. If a BnPCI/PCI-X bus segment does not support any Hot-Plug slots at a given BnPCI/PCI-X mode and frequency, then the corresponding Number of Slots Available field must be 0. This register is initialized by BIOS with platform specific loading information to be later used by OS/driver.

Bits	Type	Reset	Description
31:29	RO	0	Reserved.
28:24	RWO	0	**Number of Slots Available (133 MHz PCI-X):** Maximum number of Hot-Plug slots available to be enabled when the bus is running at 133 MHz PCI-X mode.
23:21	RO	0	Reserved.
20:16	RWO	0	**Number of Slots Available (100 MHz PCI-X):** Maximum number of Hot-Plug slots available to be enabled when the bus is running at 100 MHz PCI-X mode.
15:13	RO	0	Reserved.
12:8	RWO	0	**Number of Slots Available (66 MHz PCI-X):** Maximum number of Hot-Plug slots available to be enabled when the bus is running at 66 MHz PCI-X mode.
7:5	RO	0	Reserved.
4:0	RWO	0	**Number of Slots Available (33 MHz Conventional PCI):** Maximum number of Hot-Plug slots available to be enabled when the bus is running at 33 MHz conventional PCI mode.

13.8.1.3 Offset 08h: SLOTS_AVAIL2—Slots Available II Register

Offset: 08–0Bh
Default Value: 00000000h
Attribute: RWO, RO
Size: 32 bits

The SHPC uses five Number of Slots Available fields organized into two Slots Available registers, SLOTS_AVAIL1 (offset 04h) being the first and this register, SLOTS_AVAIL2, being the second. Each Number of Slots Available field specifies the maximum number of Hot-Plug slots that are permitted to be enabled at the given BnPCI/PCI-X mode and frequency on the associated PCI/PCI-X bus segment. If a BnPCI/PCI-X bus segment does not support any Hot-Plug slots at a given BnPCI/PCI-X mode and frequency, then the corresponding Number of Slots Available field must be 0. This register is initialized by BIOS with platform specific loading information to be later used by OS/driver.

Bits	Type	Reset	Description
31:5	RWO	0	Reserved.
4:0	RWO	0	**Number of Slots Available (66 MHz Conventional PCI):** Maximum number of Hot-Plug slots available to be enabled when the bus is running at 66 MHz conventional PCI mode.

13.8.1.4 Offset 0Ch: SLOT_CONFIG—Slot Configuration Register

Offset: 0C–0Fh
Default Value: 00000000h
Attribute: RWO, RO
Size: 32 bits

This register describes the configuration of the slots controlled by the SHPC.

Bits	Type	Reset	Description
31	RWO	0	**Attention Button Implemented (ABI):** This bit specifies whether the Hot-Plug slots controlled by this SHPC implement the optional Attention Button. If this bit is set, Attention Buttons are implemented on every PCI slot controlled by this SHPC.
30	RWO	0	**MRL Sensor Implemented (MRLSI):** This bit specifies whether MRL Sensors are implemented on the Hot-Plug slots controlled by the SHPC. If this bit is set, the platform provides an MRL Sensor for each slot controlled by this SHPC.
29	RWO	0	**Physical Slot Number Up/Down (PSNUD):** This bit specifies the direction of enumeration of external slot labels, beginning with the value in the Physical Slot Number field (PSN) of this register (offset 0C-0Fh, bits 26:6). If this bit is set, each external slot label increments by 1 from the value in the Physical Slot Number field. If this bit is cleared, each external slot label decrements by 1 from the value in the Physical Slot Number field.
28:27	RO	0	Reserved.
26:16	RWO	0	**Physical Slot Number (PSN):** This field specifies the physical slot number of the device addressed by the First Device Number (FDN) at bits 12:8 of this register. This field must be hardware initialized to a value that assigns all slots (controlled by this SHPC) a slot number that is globally unique within the chassis.
15:13	RO	0	Reserved.
12:8	RWO	0	**First Device Number (FDN):** This field contains the device number assigned to the first Hot-Plug slot on this bus segment.
7:5	RO	0	Reserved.
4:0	RO	0	**Number of Slots Implemented (NSI):** This field contains the number of Hot-Plug slots connected to the SHPC (that is, the number of slots controlled by the SHPC). This field must not return a value of 0. (If the controller does not control any slots in the system, the SHPC Capabilities List Item must not appear in the Capabilities List).

13.8.1.5 Offset 10h: SBUS_CONFIG—Secondary Bus Configuration Register

Offset: 10 - 11h
Default Value: 0000h
Attribute: RO
Size: 16 bits

This register describes the configuration of the secondary bus segment that contains the Hot-Plug slots controlled by the SHPC.

Bits	Type	Reset	Description
15:4	RO	0	Reserved.
3:0	RO	0	**Current Bus Segment Speed/Mode (CBSS):** Indicates the current speed and mode at which the PCI bus segment is operating. 0000b = 33 MHz Conventional PCI Mode 0001b = 66 MHz Conventional PCI Mode 0010b = 66 MHz PCI-X Mode 1 0011b = 100 MHz PCI-X Mode 1 0100b = 133 MHz PCI-X Mode 1 0101b = Reserved 0110b = Reserved 0111b = Reserved

13.8.1.6 Offset 12h: SHPC_MSI_CNTL—SHPC MSI Control Register

Offset: 12h
Default Value: 00h
Attribute: RO
Size: 8 bits

This register indicates the specific message number that will be used by the SHPC to signal an interrupt when using Message Signaled Interrupts (MSI).

Bits	Type	Reset	Description
7:5	RO	0	Reserved.
4:0	RO	0	**SHPC Interrupt Message Number (SHPC_IMN):** Reflects the Multiple Message Enable field (MMEN, bits 6:4) of the MSI Capability Control register (MSI_MCNTL, offset 5Eh).

13.8.1.7 Offset 13h: SHPC_PROG_IF—SHPC Programming Interface Register

Offset: 13h
Default Value: 01h
Attribute: RO
Size: 8 bits

This register identifies the format of the working register set.

Bits	Type	Reset	Description
7:0	RO	01h	**SHPC Programming Interface (SHPC_PI):** Identifies the format of the SHPC Working Register set. A value of 01h identifies the SHPC Working Register set format defined in the *Standard Hot-Plug Controller and Subsystem Specification*, Revision 1.0.

13.8.1.8 Offset 14h: CONT_COMMAND—Controller Command Register

Offset: 14–15h
Default Value: 0000h
Attribute: RW, RO
Size: 16 bits

Bits	Type	Reset	Description
15:13	RO	0	Reserved.
12:8	RW	0	**Target Slot (TS):** This field selects the target slot for a Slot Operation command. For example, writing a 2 to this field would select the 2nd slot for the Slot Operation command. Software is permitted to write the Command Code and Target Slot fields simultaneously. However, software is not required to write these fields simultaneously. If the fields are not written simultaneously, the Slot Operation command targets the slot associated with the current value in this register. If the command is not a Slot Operation command, this field is ignored. When this field is read, it returns the value that was last written to it, even after the command has completed.
7:0	RW	0	**Command Code (CCODE):** Command to be executed by the SHPC. Writing to this field triggers the SHPC to begin executing the command. Refer to the *Standard Hot-Plug Controller and Subsystem Specification*, Rev 1.0 for command encodings. When read, this field returns the command code that was last written to it, even after the command has completed.

13.8.1.9 Offset 16h: CONT_COMMAND_STS—Controller Command Status Register

Offset: 16–17h
Default Value: 0000h
Attribute: RO
Size: 16 bits

Bits	Type	Reset	Description
15:4	RO	0	Reserved.
3:1	RO	0	**Controller Command Error Code (CCEC):** This field shows the result of the last command completed by the SHPC. This field is updated when the Controller Busy bit (offset 16-17h, bit 0) transitions from 1 to 0 (indicating a command completion). If the command failed, the appropriate bit is set. If none of the bits in this field are set, the command completed successfully.
0	RO	0	**Controller Busy (CB):** This bit changes from 0 to 1 when a command code is written to the Controller Command register (CONT_COMMAND, offset 14h). It stays set until the SHPC has completed executing the command. The SHPC ignores writes to the Controller Command register (CONT_COMMAND, offset 14h) while this bit is set. This bit changes from 1 to 0 when the SHPC finishes executing a command. The SHPC must not set this bit for any other reason. For example, this bit must not be set to 1 when the SHPC automatically powers down the slot in response to detecting a MRL open event.

13.8.1.10 Offset 18h: INT_LOC—Interrupt Locator Register

Offset: 18 – 1Bh
Default Value: 00000000h
Attribute: RO
Size: 32 bits

Interrupt locator register for software to easily identify the source of an interrupt.

Bits	Type	Reset	Description
31:7	RO	0	Reserved.
6:1	RO	0	**Slot n Interrupt Pending Bits (SNIPB):** A set bit in this field indicates an interrupt pending condition on the associated slot. An interrupt pending condition occurs when the SHPC detects a Slot Event, and the event's Command Complete Interrupt Mask bit (CCIM, bit 2) in the Slot SERR-INT Mask field (, offset h) is cleared. Multiple bits are set if multiple slots have an interrupt pending. Clearing all bits in the Slot Event Latch field (SEL, bit) of the slot's Logical Slot register (LSR_SLOT, offset 24h) clears that slot's bit in this field.
0	RO	0	**Command Complete Interrupt Pending (CCIP):** The state of this bit is 1 when the Command Completion Detected bit (CCIM, bit 2) in the Slot SERR-INT Mask field (offset 20h) is set indicating a command completion and the Command Complete Interrupt Mask bit located in the Controller SERR-INT Enable register (SERR_INT, offset 20h) is cleared.

13.8.1.11 Offset 1Ch: SERR_LOC—SERR Locator Register

Offset: 1C – 1Fh Attribute: RO
Default Value: 00000000h Size: 32 bits

System Interrupt locator register for software to easily identify the source of interrupt.

Bits	Type	Reset	Description
31:8	RO	0	Reserved.
7:1	RO	0	**Slot n SERR Pending (SNSP):** A set bit in this field indicates an SERR pending condition on the associated slot. An SERR pending condition occurs when the SHPC detects a slot event capable of generating an SERR and that event's SERR Mask bit in the Slot SERR-INT Mask field is cleared. Multiple bits are set if multiple slots have an SERR pending. Clearing all bits in the slot's Slot Event Latch field that are capable of generating an SERR clears that slot's bit in this field.
0	RO	0	**Arbiter SERR Pending (ASP):** The state of this bit is 1 when the Arbiter Timeout Detected bit (ATD, bit 17) in the Controller SERR-INT Enable register (SERR_INT, offset 20h) is set and the Arbiter SERR Mask bit (ASM, bit 3) is cleared.

13.8.1.12 Offset 20h: SERR_INT—Controller SERR_INT Enable Register

Offset: 20–23h Attribute: RW, RWC, RO
Default Value: 0000000Fh Size: 32 bits

This register enables and disables SERR and System generation and reports global controller events.

Bits	Type	Reset	Description
31:18	RO	0	Reserved.
17	RWC	0	**Arbiter Timeout Detected (ATD):** This bit is set when the SHPC detects an arbiter timeout.
16	RWC	0	**Command Completion Detected (CCD):** This bit is set when the Controller Busy bit (CB, bit 0) in the Controller Command Status register (CONT_COMMAND_STS, offset 16h) transitions from 1 to 0 (indicating a command completion).
15:4	RO	0	Reserved.
3	RW	1	**Arbiter SERR Mask (ASM):** When this bit is set, arbiter timeout SERRs are masked. This bit is a mask and does not affect whether the Arbiter Timeout Detected bit (bit 17 of this register) is set. When this mask is cleared and the global SERR mask (bit 1 below) is clear, arbiter timeout error will cause ERR_NONFATAL message on the PCI Express bus, provided the SERR enable bit is set in the PCICMD register or the nonfatal message enable bit is set in the PCI Express capability.
2	RW	1	**Command Complete Interrupt Mask (CCIM):** When this bit is set, command Completion Interrupts are masked. This bit is a mask and does not affect whether the Command Completion Detected bit (CCD, bit 16 of this register) is set.
1	RW	1	**Global SERR Mask (GSM):** When this bit is set, SERR generation from the SHPC is masked.
0	RW	1	**Global Interrupt Mask (GIM):** When this bit is set, System Interrupt generation by the SHPC is masked. This bit is a mask and does not affect any bits in the Interrupt Locator register. This bit has no effect on whether the Wakeup Signal is asserted.

13.8.2 Offset 24h – 40h: Logical Slot Registers (LSR) 1 to 6

Software uses the Logical Slot Register for the following:

- Current status of the slot

- Configure system interrupts and system errors generated by the slots
- Detect pending events on the slots

Each Logical Slot Register is formatted as follows and is described in further detail below.

31	24	23	16	15	0
Slot SERR-INT Mask		Slot Event Latch		Slot Status	

13.8.2.1 SSTS – Slot Status Field, Bits [15:0]

This field contains status information about the slot.

Bits	Type	Reset	Description
15	RO	0	Reserved.
14	RO	0	Reserved.
13:12	RO	xx	**PCI-X Capability (PCI-X_CAP):** These bits report the current PCI-X capability of the add-in card installed in the slot. These bits are not valid if the slot is empty. If the slot is occupied, these bits are valid regardless of the state of the slot or speed/mode of the bus. 00b Non PCI-X 01b 66 MHz PCI-X Mode 10b Reserved 11b 133 MHz PCI-X Mode
11:10	RO	xx	**PRSNT1#/PRSNT2# (PRSNT1_PRSNT2):** These bits report the current de-bounced state of the PRSNT1# and PRSNT2# slot pins. These bits are valid regardless of the state of the slot or speed/mode of the bus. 00b Card Present; 7.5W 01b Card Present; 25W 10b Card Present; 15W 11b Slot Empty
9	RO	x	**66 MHz Capable (HP_M66EN):** This bit reports whether the add-in card is capable of running at 66 MHz conventional mode. This bit is latched as the slot is powered up or enabled, regardless of the current speed/mode of the bus. If this bit is 1, the card is capable of running at 66 MHz conventional mode. If this bit is 0, the card is only capable of 33 MHz conventional mode operation. This bit is valid only when the slot is occupied and powered or enabled.
8	RO	x	**MRL Sensor (HP_MRL):** This bit reports the current state of the MRL as reported by the de-bounced MRL Sensor input signal. If this bit is 1, the MRL Sensor is reporting that the MRL is open. If this bit is 0, the MRL Sensor is reporting that the MRL is closed.
7	RO	x	**Attention Button (ATTBUT):** This bit reports the current state of the de-bounced Attention Button input signal for this slot. If this bit is 1, the Attention Button is being pressed. If this bit is 0, the Attention Button is not being pressed.
6	RO	x	**Power Fault (PWRFLT):** This bit reports the current state of the power fault latch in the power controller circuitry for this slot. If this bit is 1, a power fault (either isolated or connected) has been detected by the power controller circuitry.

Bits	Type	Reset	Description
5:4	RO	x	**Attention Indicator State (ATTNIND):** This field reports the current state of the Attention Indicator associated with the slot. 00b Reserved 01b On 10b Blink 11b Off
3:2	RO	x	**Power Indicator State (PWRIND):** This field reports the current state of the Power Indicator associated with the slot. 00b Reserved 01b On 10b Blink 11b Off
1:0	RO	x	**Slot State (SLOT_STATUS):** This field reports the current state of the slot. 00b Reserved 01b Powered Only 10b Enabled 11b Disabled

13.8.2.2 SEVL – Slot Event Latch Field, Bits [23:16]

The Slot Event Latch field reports all latched events detected by the SHPC.

Bits	Type	Reset	Description
23:21	RO	0	Reserved.
20	RWC	0	**Connected Power Fault Detected (CPFD):** This bit is set when a connected power fault is detected by the power control circuitry for this slot.
19	RWC	0	**MRL Sensor Change Detected (MRLSCD):** This bit is set when the MRL Sensor bit in the Slot Status field changes state indicating a change in the position of the MRL.
18	RWC	0	**Attention Button Press Detected (ABPD):** This bit is set when the Attention Button bit in the Slot Status field transitions from 0 to 1 indicating the Attention Button has been pressed.
17	RWC	0	**Isolated Power Fault Detected (IPFD):** This bit is set when an isolated power fault is detected by the power control circuitry for this slot.
16	RWC	0	**Card Presence Change Detected (CPCD):** This bit is set when a change is detected on the PRSNT1#/PRSNT2# bits defined in the Slot Status field.

13.8.2.3 SSIM – Slot SERR-INT Mask Field, Bits [31:24]

The Slot SERR-INT Mask field controls masking and unmasking of system interrupts and system errors generated from events detected by the SHPC.

Bits	Type	Reset	Description
31	RO	0	Reserved.
30	RW	1	**Connected Power Fault SERR Mask (CPFSM):** If this bit is set, SERR assertions from Connected Power Fault Detected are masked. The state of this bit has no effect on the state of the Connected Power Fault Detected bit. When this bit is clear, then connected power faults can cause ERR_FATAL message on the PCI Express bus provided the SERR enable bit in the PCICMD register is set or the ERR_FATAL enable bit is set in the PCI Express capability.
29	RW	1	**MRL Sensor SERR Mask (MSSM):** If this bit is set, SERR assertions from MRL Sensor Change Detected are masked. The state of this bit has no effect on the state of the MRL Sensor Change Detected bit. When this bit is clear, then MRL sensor error condition can cause ERR_FATAL message on the PCI Express bus provided the SERR enable bit in the PCICMD register is set or the ERR_FATAL enable bit is set in the PCI Express capability.

Bits	Type	Reset	Description
28	RW	1	**Connected Power Fault Interrupt Mask (CPFIM):** If this bit is set, system interrupts from Connected Power Fault Detected are masked. The state of this bit has no effect on the state of the Connected Power Fault Detected bit.
27	RW	1	**MRL Sensor Interrupt Mask (MSIM):** If this bit is set, system interrupts from MRL Sensor Change Detected are masked. The state of this bit has no effect on the state of the MRL Sensor Change Detected bit.
26	RW	1	**Attention Button Interrupt Mask (ABIM):** If this bit is set, system interrupts from Attention Button Press Detected are masked. The state of this bit has no effect on the state of the Attention Button Press Detected bit.
25	RW	1	**Isolated Power Fault Interrupt Mask (IPFIM):** If this bit is set, system interrupts from Isolated Power Fault Detected are masked. The state of this bit has no effect on the state of the Isolated Power Fault Detected bit.
24	RW	1	**Card Presence Interrupt Mask (CPIM):** If this bit is set, system interrupts from Card Presence Change Detected are masked. The state of this bit has no effect on the state of the Card Presence Change Detected bit.

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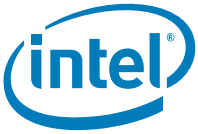


14 Intel® High Definition Audio Controller Registers (D27:F0)

The Intel High Definition Audio controller resides in PCI Device 27, Function 0 on bus 0. This function contains a set of DMA engines that are used to move samples of digitally encoded data between system memory and external codecs.

Note: All registers in this function (including memory-mapped registers) must be addressable in byte, word, and D-word quantities. The software must always make register accesses on natural boundaries (that is, D-word accesses must be on D-word boundaries; word accesses on word boundaries, and so forth). In addition, the memory-mapped register space must not be accessed with the LOCK semantic exclusive-access mechanism. If software attempts exclusive-access mechanisms to the Intel High Definition Audio memory-mapped space, the results are undefined.

14.1 Intel® High Definition Audio PCI Configuration Space (High Definition Audio— D27:F0)

Note: Address locations that are not shown should be treated as Reserved.

Table 14-1. Intel® High Definition Audio PCI Register Address Map (High Definition Audio—D27:F0) (Sheet 1 of 2)

Offset	Mnemonic	Register Name	Default	Access
00-01h	VID	Vendor Identification	8086h	RO
02-03h	DID	Device Identification	269Ah	RO
04-05h	PCICMD	PCI Command	0000h	R/W, RO
06-07h	PCISTS	PCI Status	0010h	R/WC, RO
08h	RID	Revision Identification	See register description.	RO
09h	PI	Programming Interface	00h	RO
0Ah	SCC	Sub Class Code	02h	RO
0Bh	BCC	Base Class Code	04h	RO
0Ch	CLS	Cache Line Size	00h	R/W
0Dh	LT	Latency Timer	00h	RO
0Eh	HEADTYPE	Header Type	00h	RO
10-13h	AZBARL	Intel High Definition Audio Lower Base Address (Memory)	00000004h	R/W, RO
14-17h	ALBARU	Intel High Definition Audio Upper Base Address (Memory)	00000000h	R/W
2C-2Dh	SVID	Subsystem Vendor Identification	0000h	R/WO
2E-2Fh	SID	Subsystem Identification	0000h	R/WO
34h	CAPP	Capability List Pointer	50h	RO
3Ch	INTLN	Interrupt Line	00h	R/W
3Dh	INTPN	Interrupt Pin	See Register Description	RO
40h	AZCTL	Intel High Definition Audio Control	00h	R/W, RO

Table 14-1. Intel® High Definition Audio PCI Register Address Map (High Definition Audio—D27:F0) (Sheet 2 of 2)

Offset	Mnemonic	Register Name	Default	Access
44h	TCSEL	Traffic Class Select	00h	R/W
50-51h	PID	PCI Power Management Capability ID	6001h	RO
52-53h	PC	Power Management Capabilities	C842	RO
54-57h	PCS	Power Management Control and Status	00000000h	R/W, RO, R/WC
60-61h	MID	MSI Capability ID	7005h	RO
62-63h	MMC	MSI Message Control	0080h	R/W, RO
64-67h	MMLA	MSI Message Lower Address	00000000h	R/W, RO
68-6Bh	MMUA	SMI Message Upper Address	00000000h	R/W
6C-6Dh	MMD	MSI Message Data	0000h	R/W
70-71h	PXID	PCI Express Capability Identifiers	0010h	RO
72-73h	PXC	PCI Express Capabilities	0001h	RO
74-77h	DEVCAP	Device Capabilities	00000000h	RO
78-79h	DEVC	Device Control	0800h	R/W, RO
7A-7Bh	DEVS	Device Status	0010h	RO
100-103h	VCCAP	Virtual Channel Enhanced Capability Header	13010002h	RO
104-107h	PVCCAP1	Port VC Capability Register 1	00000001h	RO
108-10Bh	PVCCAP2	Port VC Capability Register 2	00000000h	RO
10C-10D	PVCCTL	Port VC Control	0000h	RO
10E-10Fh	PVCSTS	Port VC Status	0000h	RO
110-103h	VC0CAP	VC0 Resource Capability	00000000h	RO
114-117h	VC0CTL	VC0 Resource Control	800000FFh	R/W, RO
11A-11Bh	VC0STS	VC0 Resource Status	0000h	RO
11C-11Fh	VCiCAP	VCi Resource Capability	00000000h	RO
120-123h	VCiCLT	VCi Resource Control	00000000h	R/W, RO
126-127h	VCiSTS	VCi Resource Status	0000h	RO
130-133h	RCCAP	Root Complex Link Declaration Enhanced Capability Header	00010005h	RO
134-137h	ESD	Element Self Description	05000100h	RO
140-143h	L1DESC	Link 1 Description	00000001h	RO
148-14Bh	L1ADDL	Link 1 Lower Address	See Register Description	RO
14C-14Fh	L1ADDU	Link 1 Upper Address	See Register Description	RO

14.1.1 VID—Vendor Identification Register (High Definition Audio Controller—D27:F0)

Offset: 00-01h
Default Value: 8086h
Attribute: RO
Size: 16 bits

Bit	Description
15:0	**Vendor ID** — RO. This is a 16-bit value assigned to Intel. Intel VID = 8086h

14.1.2 DID—Device Identification Register (High Definition Audio Controller—D27:F0)

Offset Address: 02–03h
Default Value: 269Ah
Attribute: RO
Size: 16 bits

Bit	Description
15:0	Device ID — RO. This is a 16-bit value assigned to the Intel High Definition Audio Controller.

14.1.3 PCICMD—PCI Command Register (High Definition Audio Controller—D27:F0)

Offset Address: 04–05h
Default Value: 0000h
Attribute: R/W, RO
Size: 16 bits

Bit	Description
15:11	Reserved
10	**Interrupt Disable (ID)** — R/W. 0= The INTx# signals may be asserted. 1= The Intel High Definition Audio controller's INTx# signal will be de-asserted Note that this bit does not affect the generation of MSIs.
9	Fast Back to Back Enable (FBE) — RO. Not implemented. Hardwired to 0.
8	SERR# Enable (SERR_EN) — RO. Not implemented. Hardwired to 0.
7	Wait Cycle Control (WCC) — RO. Not implemented. Hardwired to 0.
6	Parity Error Response (PER) — RO. Not implemented. Hardwired to 0.
5	VGA Palette Snoop (VPS). Not implemented. Hardwired to 0.
4	Memory Write and Invalidate Enable (MWIE) — RO. Not implemented. Hardwired to 0.
3	Special Cycle Enable (SCE). Not implemented. Hardwired to 0.
2	**Bus Master Enable (BME)** — R/W. Controls standard PCI Express bus mastering capabilities for Memory and I/O, reads and writes. Note that this bit also controls MSI generation since MSIs are essentially Memory writes. 0 = Disable 1 = Enable
1	**Memory Space Enable (MSE)** — R/W. Enables memory space addresses to the Intel High Definition Audio controller. 0 = Disable 1 = Enable
0	I/O Space Enable (IOSE)—RO. Hardwired to 0 since the Intel High Definition Audio controller does not implement I/O space.

14.1.4 PCISTS—PCI Status Register (High Definition Audio Controller—D27:F0)

Offset Address: 06–07h
Default Value: 0010h
Attribute: RO, R/WC
Size: 16 bits

Bit	Description
15	Detected Parity Error (DPE) —RO. Not implemented. Hardwired to 0.
14	SERR# Status (SERRS) — RO. Not implemented. Hardwired to 0.
13	Received Master Abort (RMA) — R/WC. Software clears this bit by writing a 1 to it. 0 = No master abort received. 1 = The Intel High Definition Audio controller sets this bit when, as a bus master, it receives a master abort. When set, the Intel High Definition Audio controller clears the run bit for the channel that received the abort.
12	Received Target Abort (RTA) — RO. Not implemented. Hardwired to 0.
11	Signaled Target Abort (STA) — RO. Not implemented. Hardwired to 0.
10:9	DEVSEL# Timing Status (DEV_STS) — RO. Does not apply. Hardwired to 0.
8	Data Parity Error Detected (DPED) — RO. Not implemented. Hardwired to 0.
7	Fast Back to Back Capable (FB2BC) — RO. Does not apply. Hardwired to 0.
6	Reserved.
5	66 MHz Capable (66MHZ_CAP) — RO. Does not apply. Hardwired to 0.
4	Capabilities List (CAP_LIST) — RO. Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h.
3	Interrupt Status (IS) — RO. 0 = This bit is 0 after the interrupt is cleared. 1 = This bit is 1 when the INTx# is asserted. Note that this bit is not set by an MSI.
2:0	Reserved.

14.1.5 RID—Revision Identification Register (High Definition Audio Controller—D27:F0)

Offset: 08h
Default Value: See bit description
Attribute: RO
Size: 8 Bits

Bit	Description
7:0	**Revision ID** — RO. Refer to Table 2-33 or the *Intel® 631xESB/632xESB I/O Controller Hub EDS Specification Update* for the value of the Revision ID Register

14.1.6 PI—Programming Interface Register (High Definition Audio Controller—D27:F0)

Offset: 09h
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	Programming Interface — RO.

14.1.7 SCC—Sub Class Code Register (High Definition Audio Controller—D27:F0)

Address Offset: 0Ah Attribute: RO
Default Value: 02h Size: 8 bits

Bit	Description
7:0	Sub Class Code (SCC) — RO. 02h = Audio Device

14.1.8 BCC—Base Class Code Register (High Definition Audio Controller—D27:F0)

Address Offset: 0Bh Attribute: RO
Default Value: 04h Size: 8 bits

Bit	Description
7:0	Base Class Code (BCC) — RO. 04h = Multimedia device

14.1.9 CLS—Cache Line Size Register (High Definition Audio Controller—D27:F0)

Address Offset: 0Ch Attribute: R/W
Default Value: 00h Size: 8 bits

Bit	Description
7:0	Cache Line Size— R/W. Implemented as R/W register, but has no functional impact

14.1.10 LT—Latency Timer Register (High Definition Audio Controller—D27:F0)

Address Offset: 0Dh Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Description
7:0	Latency Timer— RO. Hardwired to 00

14.1.11 HEADTYP—Header Type Register (High Definition Audio Controller—D27:F0)

Address Offset: 0Eh Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Description
7:0	Header Type— RO. Hardwired to 00.

14.1.12 AZBARL—High Definition Audio Lower Base Address Register (High Definition Audio Controller—D27:F0)

Address Offset: 10h Attribute: R/W, RO
Default Value: 00000004h Size: 32 bits

Bit	Description
31:14	**Lower Base Address (LBA)**— R/W. Base address for the Intel High Definition Audio controller's memory mapped configuration registers. 16 KBytes are requested by hardwiring bits 13:4 to 0's.
13:4	RO. Hardwired to 0's
3	Prefetchable (PREF)—RO. Hardwired to 0 to indicate that this BAR is NOT prefetchable
2:1	Address Range (ADDRNG)—RO. Hardwired to 10b, indicating that this BAR can be located anywhere in 64-bit address space.
0	Space Type (SPTYP)—RO. Hardwired to 0. Indicates this BAR is located in memory space.

14.1.13 AZBARU—Intel® High Definition Audio Upper Base Address Register (High Definition Audio Controller—D27:F0)

Address Offset: 14h Attribute: R/W
Default Value: 00000000h Size: 32 bits

Bit	Description
31:0	**Upper Base Address (UBA)**— R/W. Upper 32 bits of the Base address for the Intel High Definition Audio controller's memory mapped configuration registers.

14.1.14 SVID—Subsystem Vendor Identification Register (High Definition Audio Controller—D27:F0)

Address Offset: 2C–2Dh Attribute: R/WO
Default Value: 0000h Size: 16 bits

The SVID register, in combination with the Subsystem ID register (D27:F0:2Eh), enable the operating environment to distinguish one audio subsystem from the other(s).

This register is implemented as write-once register. Once a value is written to it, the value can be read back. Any subsequent writes will have no effect.

This register is not affected by the $D3_{HOT}$ to D0 transition.

Bit	Description
15:0	Subsystem Vendor ID — R/WO.

14.1.15 SID—Subsystem Identification Register (High Definition Audio Controller—D27:F0)

Address Offset: 2E–2Fh Attribute: R/WO
Default Value: 0000h Size: 16 bits

The SID register, in combination with the Subsystem Vendor ID register (D27:F0:2Ch) make it possible for the operating environment to distinguish one audio subsystem from the other(s).

This register is implemented as write-once register. Once a value is written to it, the value can be read back. Any subsequent writes will have no effect.

This register is not affected by the $D3_{HOT}$ to D0 transition.

Bit	Description
15:0	**Subsystem ID** — R/WO.

14.1.16 CAPPTR—Capabilities Pointer Register (Audio—D27:F0)

Address Offset: 34h
Default Value: 50h
Attribute: RO
Size: 8 bits

This register indicates the offset for the capability pointer.

Bit	Description
7:0	Capabilities Pointer (CAP_PTR) — RO. This field indicates that the first capability pointer offset is offset 50h (Power Management Capability)

14.1.17 INTLN—Interrupt Line Register (High Definition Audio Controller—D27:F0)

Address Offset: 3Ch
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	**Interrupt Line (INT_LN)** — R/W. This data is not used by the Intel® 631xESB/632xESB I/O Controller Hub. It is used to communicate to software the interrupt line that the interrupt pin is connected to.

14.1.18 INTPN—Interrupt Pin Register (High Definition Audio Controller—D27:F0)

Address Offset: 3Dh
Default Value: See Description
Attribute: RO
Size: 8 bits

Bit	Description
7:4	Reserved.
3:0	Interrupt Pin— RO. This reflects the value of D27IP.ZIP (Chipset Config Registers:Offset 3110h:bits 3:0).

14.1.19 AZCTL—Intel® High Definition Audio Control Register (High Definition Audio Controller—D27:F0)

Address Offset: 40h
Default Value: 00h
Attribute: R/W, RO
Size: 8 bits

Bit	Description
7:4	Reserved.
3	**BITCLK Detect Clear (CLKDETCLR)**— R/W. 0 = When a 0 is written to this bit, the clock detect circuit is operational and maybe enabled. 1 = Writing a 1 to this bit clears bit 1 (CLKDET#) in this register. CLKDET# bit remains clear when this bit is set to 1. ***Note:*** This bit is not affected by the $D3_{HOT}$ to D0 transition.
2	**BITCLK Detect Enable (CLKDETEN)**— R/W. 0 = Latches the current state of bit 1 (CLKDET#) in this register 1 = Enables the clock detection circuit ***Note:*** This bit is not affected by the $D3_{HOT}$ to D0 transition.
1	BITCLK Detected Inverted (CLKDET#)— RO. This bit is modified by hardware. It is set to 0 when the BITCLK toggling is detected, indicating the presence of an AC'97 codec on the link ***Note:*** Bit 2 (CLKDETEN) and bit 3 (CLKDETCLR) in this register control the operation of this bit and must be manipulated correctly in order to get a valid CLKDET# indicator.
0	**High Definition Audio/AC'97 Signal Mode**— R/W. This bit selects the shared Intel High Definition Audio/AC'97 signals. 0 = AC'97 mode is selected (Default) 1 = Intel High Definition Audio mode is selected ***Notes:*** 1. This bit has no affect on the visibility of the Intel High Definition Audio and AC'97 function configuration space. 2. This bit is in the resume well and only clear on a power-on reset. Software must not makes assumptions about the reset state of this bit and must set it appropriately.

14.1.20 TCSEL—Traffic Class Select Register (High Definition Audio Controller—D27:F0)

Address Offset: 44h
Default Value: 00h
Attribute: R/W
Size: 8 bits

This register assigned the value to be placed in the TC field for transactions over the Intel® 631xESB/632xESB I/O Controller Hub backbone. CORB and RIRB data will always be assigned TC0.

Bit	Description
7:3	Reserved.
2:0	**High Definition Audio Traffic Class Assignment (TCSEL)**— R/W. This register assigns the value to be placed in the Traffic Class field for input data, output data, and buffer descriptor transactions sent to the Intel® 631xESB/632xESB I/O Controller Hub backbone. 000 = TC0 001 = TC1 010 = TC2 011 = TC3 100 = TC4 101 = TC5 110 = TC6 111 = TC7 Note: These bits are not reset on $D3_{HOT}$ to D0 transition; however, they are reset by PLTRST#.

14.1.21 PID—PCI Power Management Capability ID Register (High Definition Audio Controller—D27:F0)

Address Offset: 50h
Default Value: 6001h
Attribute: RO
Size: 16 bits

Bit	Description
15:8	Next Capability (Next)— RO. Hardwired to 60h. Points to the next capability structure (MSI)
7:0	Cap ID (CAP)— RO. Hardwired to 01h. Indicates that this pointer is a PCI power management capability.

14.1.22 PC—Power Management Capabilities Register (High Definition Audio Controller—D27:F0)

Address Offset: 52h
Default Value: C842h
Attribute: RO
Size: 16 bits

Bit	Description
15:11	PME Support— RO. Hardwired to 11001b. Indicates PME# can be generated from D3 and D0 states.
10	D2 Support— RO. Hardwired to 0. Indicates that D2 state is not supported.
9	D1 Support—RO. Hardwired to 0. Indicates that D1 state is not supported.
8:6	Aux Current—RO. Hardwired to 001b. Reports 55mA maximum suspend well current required when in the $D3_{COLD}$ state.
5	Device Specific Initialization (DSI)—RO. Hardwired to 0. Indicates that no device specific initialization is required.
4	Reserved
3	PME Clock (PMEC)—RO. Does not apply. Hardwired to 0.
2:0	Version—RO. Hardwired to 010b. Indicates support for version 1.1 of the PCI Power Management Specification.

14.1.23 PCS—Power Management Control and Status Register (High Definition Audio Controller—D27:F0)

Address Offset: 54h
Default Value: 00000000h
Attribute: RO, R/W, R/WC
Size: 32 bits

Bit	Description
31:24	Data—RO. Does not apply. Hardwired to 0.
23	Bus Power/Clock Control Enable— RO. Does not apply. Hardwired to 0.
22	B2/B3 Support—RO. Does not apply. Hardwired to 0.
21:16	Reserved.
15	**PME Status (PMES)**—R/WC. 0 = Software clears the bit by writing a 1 to it. 1 = This bit is set when the Intel **High Definition Audio** controller would normally assert the PME# signal independent of the state of the PME_EN bit (bit 8 in this register) This bit in the resume well and only cleared on a power-on reset. Software must not make assumptions about the reset state of this bit and must set it appropriately
14:9	Reserved

Bit	Description
8	**PME Enable (PMEE)**—R/W. 0 = Disable 1 = when set and if corresponding PMES also set, the Intel High Definition Audio controller sets the AC97_STS bit in the GPE0_STS register (PMBASE +28h). The AC97_STS bit is shared by AC'97 and Intel High Definition Audio functions since they are mutually exclusive. This bit in the resume well and only cleared on a power-on reset. Software must not make assumptions about the reset state of this bit and must set it appropriately
7:2	Reserved
1:0	**Power State (PS)**—R/W. This field is used both to determine the current power state of the Intel High Definition Audio controller and to set a new power state. 00 = D0 state 11 = $D3_{HOT}$ state Others = reserved **Notes:** • If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. • When in the $D3_{HOT}$ states, the Intel High Definition Audio controller's configuration space is available, but the IO and memory space are not. Additionally, interrupts are blocked. • When software changes this value from $D3_{HOT}$ state to the D0 state, an internal warm (soft) reset is generated, and software must re-initialize the function.

14.1.24 MID—MSI Capability ID Register (High Definition Audio Controller—D27:F0)

Address Offset: 60h Attribute: RO
Default Value: 7005h Size: 16 bits

Bit	Description
15:8	Next Capability (Next)— RO. Hardwired to 70h. Points to the PCI Express capability structure.
7:0	Cap ID (CAP)— RO. Hardwired to 05h. Indicates that this pointer is a MSI capability

14.1.25 MMC—MSI Message Control Register (High Definition Audio Controller—D27:F0)

Address Offset: 62h Attribute: RO, R/W
Default Value: 0080h Size: 16 bits

Bit	Description
15:8	Reserved
7	64b Address Capability (64ADD)— RO. Hardwired to 1. Indicates the ability to generate a 64-bit message address
6:4	Multiple Message Enable (MME)—RO. Normally this is a R/W register. However since only 1 message is supported, these bits are hardwired to 000 = 1 message.
3:1	Multiple Message Capable (MMC)—RO. Hardwired to 0 indicating request for 1 message.
0	**MSI Enable (ME)**—R/W. 0 = an MSI may not be generated 1 = an MSI will be generated instead of an INTx signal.

14.1.26 MMLA—MSI Message Lower Address Register (High Definition Audio Controller—D27:F0)

Address Offset: 64h Attribute: RO, R/W
Default Value: 00000000h Size: 32 bits

Bit	Description
31:2	**Message Lower Address (MLA)**— R/W. Lower address used for MSI message.
1:0	Reserved.

14.1.27 MMUA—MSI Message Upper Address Register (High Definition Audio Controller—D27:F0)

Address Offset: 68h Attribute: R/W
Default Value: 00000000h Size: 32 bits

Bit	Description
31:0	**Message Upper Address (MUA)**— R/W. Upper 32-bits of address used for MSI message.

14.1.28 MMD—MSI Message Data Register (High Definition Audio Controller—D27:F0)

Address Offset: 6Ch Attribute: R/W
Default Value: 0000h Size: 16 bits

Bit	Description
15:0	**Message Data (MD)**— R/W. Data used for MSI message.

14.1.29 PXID—PCI Express Capability ID Register (High Definition Audio Controller—D27:F0)

Address Offset: 70h Attribute: RO
Default Value: 0010h Size: 16 bits

Bit	Description
15:8	Next Capability (Next)— RO. Hardwired to 0. Indicates that this is the last capability structure in the list.
7:0	Cap ID (CAP)—RO. Hardwired to 10h. Indicates that this pointer is a PCI Express capability structure

14.1.30 PXC—PCI Express Capabilities Register (High Definition Audio Controller—D27:F0)

Address Offset: 72h Attribute: RO
Default Value: 0001h Size: 16 bits

Bit	Description
15:14	Reserved
13:9	Interrupt Message Number (IMN)—RO. Hardwired to 0.
8	Slot Implemented (SI)—RO. Hardwired to 0.
7:4	Device/Port Type (DPT)—RO. Hardwired to 0. Indicates that this is a PCI Express Endpoint device.
3:0	Capability Version (CV)—RO. Hardwired to 0001b. Indicates version #1 PCI Express capability

14.1.31 DEVCAP—Device Capabilities Register (High Definition Audio Controller—D27:F0)

Address Offset: 74h
Default Value: 00000000h
Attribute: RWO, RO
Size: 32 bits

Bit	Description
31:28	Reserved
27:26	Captured Slot Power Limit Scale (SPLS)—RO. Hardwired to 0.
25:18	Captured Slot Power Limit Value (SPLV)—RO. Hardwired to 0.
17:15	Reserved
14	Power Indicator Present —RO. Hardwired to 0.
13	Attention Indicator Present—RO. Hardwired to 0.
12	Attention Button Present—RO. Hardwired to 0.
11:9	Endpoint L1 Acceptable Latency—RWO.
8:6	Endpoint L0s Acceptable Latency—RWO.
5	Extended Tag Field Support—RO. Hardwired to 0. Indicates 5-bit tag field support
4:3	Phantom Functions Supported—RO. Hardwired to 0. Indicates that phantom functions not supported
2:0	Max Payload Size Supported—RO. Hardwired to 0. Indicates 128B maximum payload size capability

14.1.32 DEVC—Device Control Register (High Definition Audio Controller—D27:F0)

Address Offset: 78h
Default Value: 0800h
Attribute: R/W, RO
Size: 16 bits

Bit	Description
15	Reserved
14:12	Max Read Request Size—RO. Hardwired to 0 enabling 128B maximum read request size.
11	**No Snoop Enable (NSNPEN)**—R/W. 0 = The Intel High Definition Audio controller will not set the No Snoop bit. In this case, isochronous transfers will not use VC1 (VCi) even if it is enabled since VC1 is never snooped. Isochronous transfers will use VC0. 1 = The Intel High Definition Audio controller is permitted to set the No Snoop bit in the Requester Attributes of a bus master transaction. In this case, VC0 or VC1 may be used for isochronous transfers. Note: This bit is not reset on $D3_{HOT}$ to D0 transition; however, it is reset by PLTRST#.
10	Auxiliary Power Enable—RO. Hardwired to 0, indicating that Intel High Definition Audio device does not draw AUX power
9	Phantom Function Enable—RO. Hardwired to 0 disabling phantom functions.
8	Extended Tag Field Enable—RO. Hardwired to 0 enabling 5-bit tag.
7:5	Max Payload Size—RO. Hardwired to 0 indicating 128B.
4	Enable Relaxed Ordering—RO. Hardwired to 0 disabling relaxed ordering.
3	Unsupported Request Reporting Enable—RO. Not implemented. Hardwired to 0.
2	Fatal Error Reporting Enable—RO. Not implemented. Hardwired to 0.
1	Non-Fatal Error Reporting Enable—RO. Not implemented. Hardwired to 0.
0	Correctable Error Reporting Enable—RO. Not implemented. Hardwired to 0.

14.1.33 DEVS—Device Status Register (High Definition Audio Controller—D27:F0)

Address Offset: 7Ah
Default Value: 0010h
Attribute: RO
Size: 16 bits

Bit	Description
15:6	Reserved
5	Transactions Pending—RO. 0 = Indicates that completions for all non-posted requests have been received 1 = Indicates that Intel High Definition Audio controller has issued non-posted requests which have not been completed.
4	AUX Power Detected—RO. Hardwired to 1 indicating the device is connected to resume power
3	Unsupported Request Detected—RO. Not implemented. Hardwired to 0.
2	Fatal Error Detected—RO. Not implemented. Hardwired to 0.
1	Non-Fatal Error Detected—RO. Not implemented. Hardwired to 0.
0	Correctable Error Detected—RO. Not implemented. Hardwired to 0.

14.1.34 VCCAP—Virtual Channel Enhanced Capability Header (High Definition Audio Controller—D27:F0)

Address Offset: 100h
Default Value: 13010002h
Attribute: RO
Size: 32 bits

Bit	Description
31:20	Next Capability Offset—RO. Hardwired to 130h. Points to the next capability header, which is the Root Complex Link Declaration Enhanced Capability Header.
19:16	Capability Version—RO. Hardwired to 1h.
15:0	PCI Express Extended Capability—RO. Hardwired to 0002h.

14.1.35 PVCCAP1—Port VC Capability Register 1 (High Definition Audio Controller—D27:F0)

Address Offset: 104h
Default Value: 00000001h
Attribute: RO
Size: 32 bits

Bit	Description
31:12	Reserved.
11:10	Port Arbitration Table Entry Size—RO. Hardwired to 0 since this is an endpoint device.
9:8	Reference Clock—RO. Hardwired to 0 since this is an endpoint device.
7	Reserved.
6:4	Low Priority Extended VC Count—RO. Hardwired to 0. Indicates that only VC0 belongs to the low priority VC group
3	Reserved.
2:0	Extended VC Count—RO. Hardwired to 001b. Indicates that 1 extended VC (in addition to VC0) is supported by Intel High Definition Audio controller.

14.1.36 PVCCAP2—Port VC Capability Register 2 (High Definition Audio Controller—D27:F0)

Address Offset: 108h Attribute: RO
Default Value: 00000000h Size: 32 bits

Bit	Description
31:24	VC Arbitration Table Offset—RO. Hardwired to 0 indicating that a VC arbitration table is not present.
23:8	Reserved.
7:0	VC Arbitration Capability—RO. Hardwired to 0. These bits are not applicable since the Intel High Definition Audio controller reports a 0 in the Low Priority Extended VC Count bits in the PVCCAP1 register.

14.1.37 PVCCLT—Port VC Control Register (High Definition Audio Controller—D27:F0)

Address Offset: 10Ch Attribute: RO
Default Value: 0000h Size: 16 bits

Bit	Description
15:4	Reserved.
3:1	VC Arbitration Select—RO. Hardwired to 0. Normally these bits are R/W. However, these bits are not applicable since the Intel High Definition Audio controller reports a 0 in the Low Priority Extended VC Count bits in the PVCCAP1 register
0	Load VC Arbitration Table—RO. Hardwired to 0 since an arbitration table is not present.

14.1.38 PVCSTS—Port VC Status Register (High Definition Audio Controller—D27:F0)

Address Offset: 10Eh Attribute: RO
Default Value: 0000h Size: 16 bits

Bit	Description
15:1	Reserved.
0	VC Arbitration Table Status—RO. Hardwired to 0 since an arbitration table is not present.

14.1.39 VC0CAP—VC0 Resource Capability Register (High Definition Audio Controller—D27:F0)

Address Offset: 110h Attribute: RO
Default Value: 00000000h Size: 32 bits

Bit	Description
31:24	Port Arbitration Table Offset—RO. Hardwired to 0 since this field is not valid for endpoint devices
23	Reserved.
22:16	Maximum Time Slots—RO. Hardwired to 0 since this field is not valid for endpoint devices
15	Reject Snoop Transactions—RO. Hardwired to 0 since this field is not valid for endpoint devices.
14	Advanced Packet Switching—RO. Hardwired to 0 since this field is not valid for endpoint devices
13:8	Reserved.
7:0	Port Arbitration Capability—RO. Hardwired to 0 since this field is not valid for endpoint devices

14.1.40 VC0CTL—VC0 Resource Control Register (High Definition Audio Controller—D27:F0)

Address Offset: 114h
Default Value: 800000FFh
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31	VC0 Enable—RO. Hardwired to 1 for VC0.
30:27	Reserved.
26:24	VC0 ID—RO. Hardwired to 0 since the first VC is always assigned as VC0
23:20	Reserved.
19:17	Port Arbitration Select—RO. Hardwired to 0 since this field is not valid for endpoint devices
16	Load Port Arbitration Table—RO. Hardwired to 0 since this field is not valid for endpoint devices
15:8	Reserved.
7:0	**TC/VC0 Map**—R/W, RO. Bit 0 is hardwired to 1 since TC0 is always mapped VC0. Bits [7:1] are implemented as R/W bits.

14.1.41 VC0STS—VC0 Resource Status Register (High Definition Audio Controller—D27:F0)

Address Offset: 11Ah
Default Value: 0000h
Attribute: RO
Size: 16 bits

Bit	Description
15:2	Reserved.
1	VC0 Negotiation Pending—RO. Hardwired to 0 since this bit does not apply to the integrated Intel High Definition Audio device
0	Port Arbitration Table Status—RO. Hardwired to 0 since this field is not valid for endpoint devices

14.1.42 VCiCAP—VCi Resource Capability Register (High Definition Audio Controller—D27:F0)

Address Offset: 11Ch
Default Value: 00000000h
Attribute: RO
Size: 32 bits

Bit	Description
31:24	Port Arbitration Table Offset—RO. Hardwired to 0 since this field is not valid for endpoint devices.
23	Reserved.
22:16	Maximum Time Slots—RO. Hardwired to 0 since this field is not valid for endpoint devices
15	Reject Snoop Transactions—RO. Hardwired to 0 since this field is not valid for endpoint devices
14	Advanced Packet Switching—RO. Hardwired to 0 since this field is not valid for endpoint devices
13:8	Reserved
7:0	Port Arbitration Capability—RO. Hardwired to 0 since this field is not valid for endpoint devices

14.1.43 VCiCTL—VCi Resource Control Register (High Definition Audio Controller—D27:F0)

Address Offset: 120h Attribute: R/W, RO
Default Value: 00000000h Size: 32 bits

Bit	Description
31	**VCi Enable**—R/W. 0 = VCi is disabled 1 = VCi is enabled Note: This bit is not reset on $D3_{HOT}$ to D0 transition; however, it is reset by PLTRST#.
30:27	Reserved.
26:24	**VCi ID**—R/W. This field assigns a VC ID to the VCi resource. This field is not used by the hardware, but it is R/W to avoid confusing software.
23:20	Reserved.
19:17	Port Arbitration Select—RO. Hardwired to 0 since this field is not valid for endpoint devices
16	Load Port Arbitration Table—RO. Hardwired to 0 since this field is not valid for endpoint devices
15:8	Reserved.
7:0	TC/VCi Map—RO, R/W. This field indicates the TCs that are mapped to the VCi resource. Bit 0 is hardwired to 0 indicating that it cannot be mapped to VCi. Bits [7:1] are implemented as R/W bits. This field is not used by the hardware, but it is R/W to avoid confusing software.

14.1.44 VCiSTS—VCi Resource Status Register (High Definition Audio Controller—D27:F0)

Address Offset: 126h Attribute: RO
Default Value: 0000h Size: 16 bits

Bit	Description
15:2	Reserved.
1	VCi Negotiation Pending—RO. Does not apply. Hardwired to 0.
0	Port Arbitration Table Status—RO. Hardwired to 0 since this field is not valid for endpoint devices.

14.1.45 RCCAP—Root Complex Link Declaration Enhanced Capability Header Register (High Definition Audio Controller—D27:F0)

Address Offset: 130h Attribute: RO
Default Value: 00010005h Size: 32 bits

Bit	Description
31:20	Next Capability Offset—RO. Hardwired to 0 indicating this is the last capability.
19:16	Capability Version—RO. Hardwired to 1h.
15:0	PCI Express Extended Capability ID—RO. Hardwired to 0005h.

14.1.46 ESD—Element Self Description Register (High Definition Audio Controller—D27:F0)

Address Offset: 134h Attribute: RO
Default Value: 05000100h Size: 32 bits

Bit	Description
31:24	Port Number—RO. Hardwired to 05h indicating that Intel High Definition Audio controller is assigned as Port #5.
23:16	Component ID—RO. This field returns the value of the ESD.CID field of the chip configuration section. ESD.CID is programmed by BIOS.
15:8	Number of Link Entries—RO. The Intel High Definition Audio only connects to one device, the egress port. Therefore this field reports a value of 1h.
7:4	Reserved.
3:0	Element Type (ELTYP)—RO. The Intel High Definition Audio controller is an integrated Root Complex Device. Therefore, the field reports a value of 0h.

14.1.47 L1DESC—Link 1 Description Register (High Definition Audio Controller—D27:F0)

Address Offset: 140h Attribute: RO
Default Value: 00000001h Size: 32 bits

Bit	Description
31:24	Target Port Number—RO. The Intel High Definition Audio controller targets the RCRB Egress port, which is Port #0.
23:16	Target Component ID—RO. This field returns the value of the ESD.CID field of the chip configuration section. ESD.CID is programmed by BIOS.
15:2	Reserved.
1	Link Type—RO. Hardwired to 0 indicating Type 0.
0	Link Valid—RO. Hardwired to 1.

14.1.48 L1ADDL—Link 1 Lower Address Register (High Definition Audio Controller—D27:F0)

Address Offset: 148h Attribute: RO
Default Value: See Register Description Size: 32 bits

Bit	Description
31:14	Link 1 Lower Address—RO. Hardwired to match the RCBA register value in the PCI-LPC bridge (D31:F0:F0h).
13:0	Reserved.

14.1.49 L1ADDU—Link 1 Upper Address Register (High Definition Audio Controller—D27:F0)

Address Offset: 14Ch Attribute: RO
Default Value: See Register Description Size: 32 bits

Bit	Description
31:0	Link 1 Upper Address—RO. Hardwired to match the RCBA register value in the PCI-LPC bridge (D31:F0:F0h).

14.2 Intel® High Definition Audio Memory Mapped Configuration Registers (High Definition Audio—D27:F0)

The base memory location for these memory mapped configuration registers is specified in the AZBAR register (D27:F0:offset 10h and D27:F0:offset 14h). The individual registers are then accessible at AZBAR + Offset as indicated in the following table.

These memory mapped registers must be accessed in Byte, Word, or Dword quantities.

Table 14-2. Intel® High Definition Audio PCI Register Address Map (High Definition Audio—D27:F0) (Sheet 1 of 4)

AZBAR + Offset	Mnemonic	Register Name	Default	Access
00-01h	GCAP	Global Capabilities	4401h	RO
02h	VMIN	Minor Version	00h	RO
03h	VMAJ	Major Version	01h	RO
04-05h	OUTPAY	Output Payload Capability	003Ch	RO
06-07h	INPAY	Input Payload Capability	001Dh	RO
08-0Bh	GCTL	Global Control	00000000h	R/W
0C-0Dh	WAKEEN	Wake Enable	0000h	R/W
0E-0Fh	STATESTS	State Change Status	0000h	R/WC
10-11h	GSTS	Global Status	0000h	R/WC
20-23h	INTCTL	Interrupt Control	00000000h	R/W
24-27h	INTSTS	Interrupt Status	00000000h	RO
30-33h	WALCLK	Wall Clock Counter	00000000h	RO
34-37h	SYNC	Stream Synchronization	00000000h	R/W
40-43h	CORBLBASE	CORB Lower Base Address	00000000h	R/W, RO
44-47h	CORBUBASE	CORB Upper Base Address	00000000h	R/W
4A-4Bh	CORBRP	CORB Read Pointer	0000h	R/W
4Ch	CORBCTL	CORB Control	00h	R/W
4Dh	CORBST	CORB Status	00h	R/WC
4Eh	CORBSIZE	CORB Size	42h	RO
50-53h	RIRBLBASE	RIRB Lower Base Address	00000000h	R/W, RO
54-57h	RIRBUBASE	RIRB Upper Base Address	00000000h	R/W
58-59h	RIRBWP	RIRB Write Pointer	0000h	R/W, RO
5A-5Bh	RINTCNT	Response Interrupt Count	0000h	R/W
5Ch	RIRBCTL	RIRB Control	00h	R/W
5Dh	RIRBSTS	RIRB Status	00h	R/WC
5Eh	RIRBSIZE	RIRB Size	42h	RO
60-63h	IC	Immediate Command	00000000h	R/W
64-67h	IR	Immediate Response	00000000h	RO
68-69h	IRS	Immediate Command Status	0000h	R/W, R/WC
70-73h	DPLBASE	DMA Position Lower Base Address	00000000h	R/W, RO
74-77h	DPUBASE	DMA Position Upper Base Address	00000000h	R/W

Table 14-2. Intel® High Definition Audio PCI Register Address Map (High Definition Audio—D27:F0) (Sheet 2 of 4)

AZBAR + Offset	Mnemonic	Register Name	Default	Access
80-82h	ISD0CTL	Input Stream Descriptor 0 (ISD0) Control	040000h	R/W, RO
83h	ISD0STS	ISD0 Status	00h	R/WC, RO
84-87h	ISD0LPIB	ISD0 Link Position in Buffer	00000000h	RO
88-8Bh	ISD0CBL	ISD0 Cyclic Buffer Length	00000000h	R/W
8C-8Dh	ISD0LVI	ISD0 Last Valid Index	0000h	R/W
8E-8F	ISD0FIFOW	ISD0 FIFO Watermark	0004h	R/W
90-91h	ISD0FIFOS	ISD0 FIFO Size	005Fh	RO
92-93h	ISD0FMT	ISD0 Format	0000h	R/W
98-9Bh	ISD0BDPL	ISD0 Buffer Descriptor List Pointer-Lower Base Address	00000000h	R/W, RO
9C-9Fh	ISD0BDPU	ISD0 Buffer Description List Pointer-Upper Base Address	00000000h	R/W
A0-A2h	ISD1CTL	Input Stream Descriptor 1(ISD01) Control	040000h	R/W, RO
A3h	ISD1STS	ISD1 Status	00h	R/WC, RO
A4-A7h	ISD1LPIB	ISD1 Link Position in Buffer	00000000h	RO
A8-ABh	ISD1CBL	ISD1 Cyclic Buffer Length	00000000h	R/W
AC-ADh	ISD1LVI	ISD1 Last Valid Index	0000h	R/W
AE-AFh	ISD1FIFOW	ISD1 FIFO Watermark	0004h	R/W
B0-B1h	ISD1FIFOS	ISD1 FIFO Size	005Fh	RO
B2-B3h	ISD1FMT	ISD1 Format	0000h	R/W
B8-BBh	ISD1BDPL	ISD1 Buffer Descriptor List Pointer-Lower Base Address	00000000h	R/W, RO
BC-BFh	ISD1BDPU	ISD1 Buffer Description List Pointer-Upper Base Address	00000000h	R/W
C0-C2h	ISD2CTL	Input Stream Descriptor 2 (ISD2) Control	040000h	R/W, RO
C3h	ISD2STS	ISD2 Status	00h	R/WC, RO
C4-C7h	ISD2LPIB	ISD2 Link Position in Buffer	00000000h	RO
C8-CBh	ISD2CBL	ISD2 Cyclic Buffer Length	00000000h	R/W
CC-CDh	ISD2LVI	ISD2 Last Valid Index	0000h	R/W
CE-CFh	ISD1FIFOW	ISD1 FIFO Watermark	0004h	R/W
D0-D1h	ISD2FIFOS	ISD2 FIFO Size	005Fh	RO
D2-D3h	ISD2FMT	ISD2 Format	0000h	R/W
D8-DBh	ISD2BDPL	ISD2 Buffer Descriptor List Pointer-Lower Base Address	00000000h	R/W, RO
DC-DFh	ISD2BDPU	ISD2 Buffer Description List Pointer-Upper Base Address	00000000h	R/W
E0-E2h	ISD3CTL	Input Stream Descriptor 3 (ISD3) Control	040000h	R/W, RO
E3h	ISD3STS	ISD3 Status	00h	R/WC, RO
E4-E7h	ISD3LPIB	ISD3 Link Position in Buffer	00000000h	RO
E8-EBh	ISD3CBL	ISD3 Cyclic Buffer Length	00000000h	R/W
EC-EDh	ISD3LVI	ISD3 Last Valid Index	0000h	R/W
EE-EFh	ISD3FIFOW	ISD3 FIFO Watermark	0004h	R/W
F0-F1h	ISD3FIFOS	ISD3 FIFO Size	005Fh	RO

Table 14-2. Intel® High Definition Audio PCI Register Address Map (High Definition Audio—D27:F0) (Sheet 3 of 4)

AZBAR + Offset	Mnemonic	Register Name	Default	Access
F2-F3h	ISD3FMT	ISD3 Format	0000h	R/W
F8-FBh	ISD3BDPL	ISD3 Buffer Descriptor List Pointer-Lower Base Address	00000000h	R/W, RO
FC-FFh	ISD3BDPU	ISD3 Buffer Description List Pointer-Upper Base Address	00000000h	R/W
100-102h	OSD0CTL	Output Stream Descriptor 0 (OSD0) Control	040000h	R/W, RO
103h	OSD0STS	OSD0 Status	00h	R/WC, RO
104-107h	OSD0LPIB	OSD0 Link Position in Buffer	00000000h	RO
108-10Bh	OSD0CBL	OSD0 Cyclic Buffer Length	00000000h	R/W
10C-10Dh	OSD0LVI	OSD0 Last Valid Index	0000h	R/W
10E-10Fh	OSD0FIFOW	OSD0 FIFO Watermark	0004h	R/W
110-111h	OSD0FIFOS	OSD0 FIFO Size	00BFh	R/W
112-113h	OSD0FMT	OSD0 Format	0000h	R/W
118-11Bh	OSD0BDPL	OSD0 Buffer Descriptor List Pointer-Lower Base Address	00000000h	R/W, RO
11C-11Fh	OSD0BDPU	OSD0 Buffer Description List Pointer-Upper Base Address	00000000h	R/W
120-122h	OSD1CTL	Output Stream Descriptor 1 (OSD1) Control	040000h	R/W, RO
123h	OSD1STS	OSD1 Status	00h	R/WC, RO
124-127h	OSD1LPIB	OSD1 Link Position in Buffer	00000000h	RO
128-12Bh	OSD1CBL	OSD1 Cyclic Buffer Length	00000000h	R/W
12C-12Dh	OSD1LVI	OSD1 Last Valid Index	0000h	R/W
12E-12Fh	OSD1FIFOW	OSD1 FIFO Watermark	0004h	R/W
130-131h	OSD1FIFOS	OSD1 FIFO Size	00BFh	R/W
132-133h	OSD1FMT	OSD1 Format	0000h	R/W
138-13Bh	OSD1BDPL	OSD1 Buffer Descriptor List Pointer-Lower Base Address	00000000h	R/W, RO
13C-13Fh	OSD1BDPU	OSD1 Buffer Description List Pointer-Upper Base Address	00000000h	R/W
140-142h	OSD2CTL	Output Stream Descriptor 2 (OSD2) Control	040000h	R/W, RO
143h	OSD2STS	OSD2 Status	00h	R/WC, RO
144-147h	OSD2LPIB	OSD2 Link Position in Buffer	00000000h	RO
148-14Bh	OSD2CBL	OSD2 Cyclic Buffer Length	00000000h	R/W
14C-14Dh	OSD2LVI	OSD2 Last Valid Index	0000h	R/W
14E-14Fh	OSD2FIFOW	OSD2 FIFO Watermark	0004h	R/W
150-151h	OSD2FIFOS	OSD2 FIFO Size	00BFh	R/W
152-153h	OSD2FMT	OSD2 Format	0000h	R/W
158-15Bh	OSD2BDPL	OSD2 Buffer Descriptor List Pointer-Lower Base Address	00000000h	R/W, RO
15C-15Fh	OSD2BDPU	OSD2 Buffer Description List Pointer-Upper Base Address	00000000h	R/W
160-162h	OSD3CTL	Output Stream Descriptor 3 (OSD3) Control	040000h	R/W, RO
163h	OSD3STS	OSD3 Status	00h	R/WC, RO
164-167h	OSD3LPIB	OSD3 Link Position in Buffer	00000000h	RO

Table 14-2. Intel® High Definition Audio PCI Register Address Map (High Definition Audio—D27:F0) (Sheet 4 of 4)

AZBAR + Offset	Mnemonic	Register Name	Default	Access
168-16Bh	OSD3CBL	OSD3 Cyclic Buffer Length	00000000h	R/W
16C-16Dh	OSD3LVI	OSD3 Last Valid Index	0000h	R/W
16E-16Fh	OSD3FIFOW	OSD3 FIFO Watermark	0004h	R/W
170-171h	OSD3FIFOS	OSD3 FIFO Size	00BFh	R/W
172-173h	OSD3FMT	OSD3 Format	0000h	R/W
178-17Bh	OSD3BDPL	OSD3 Buffer Descriptor List Pointer-Lower Base Address	00000000h	R/W, RO
17C-17Fh	OSD3BDPU	OSD3 Buffer Description List Pointer-Upper Base Address	00000000h	R/W

14.2.1 GCAP—Global Capabilities Register (High Definition Audio Controller—D27:F0)

Memory Address: AZBAR + 00h Attribute: RO
Default Value: 4401h Size: 16 bits

Bit	Description
15:12	Number of Output Stream Supported— RO. Hardwired to 0100b indicating that the Intel High Definition Audio controller supports 4 output streams.
11:8	Number of Input Stream Supported— RO. Hardwired to 0100b indicating that the Intel High Definition Audio controller supports 4 input streams.
7:3	Number of Bidirectional Stream Supported— RO. Hardwired to 0 indicating that the Intel High Definition Audio controller supports 0 bidirectional stream.
2	Reserved.
1	Number of Serial Data Out Signals— RO. Hardwired to 0 indicating that the Intel High Definition Audio controller supports 1 serial data output signal.
0	64-bit Address Supported— RO. Hardwired to 1b indicating that the Intel High Definition Audio controller supports 64-bit addressing for BDL addresses, data buffer addressees, and command buffer addresses.

14.2.2 VMIN—Minor Version Register (High Definition Audio Controller—D27:F0)

Memory Address: AZBAR + 02h Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Description
7:0	Minor Version— RO. Hardwired to 0 indicating that the minor revision number 00h of the Intel High Definition Audio specification is supported

14.2.3 VMAJ—Major Version Register (High Definition Audio Controller—D27:F0)

Memory Address: AZBAR + 03h Attribute: RO
Default Value: 01h Size: 8 bits

Bit	Description
7:0	Major Version— RO. Hardwired to 01h indicating that major revision number 1 of the Intel High Definition Audio specification is supported.

14.2.4 OUTPAY—Output Payload Capability Register (High Definition Audio Controller—D27:F0)

Memory Address: AZBAR + 04h Attribute: RO
Default Value: 003Ch Size: 16 bits

Bit	Description
15:7	Reserved.
6:0	Output Payload Capability— RO. Hardwired to 3Ch indicating 60 word payload. This field indicates the total output payload available on the link. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48Mhz frame. The default link clock of 24.000MHz (the data is double pumped) provides 1000 bits per frame, or 62.5 words in total. 40 bits are used for command and control, leaving 60 words available for data payload. 00h = 0 word 01h = 1 word payload. ..... FFh = 256 word payload.

14.2.5 INPAY—Input Payload Capability Register (High Definition Audio Controller—D27:F0)

Memory Address: AZBAR + 06h Attribute: RO
Default Value: 001Dh Size: 16 bits

Bit	Description
15:7	Reserved.
6:0	Input Payload Capability— RO. Hardwired to 1Dh indicating 29 word payload. This field indicates the total output payload available on the link. This does not include bandwidth used for response. This measurement is in 16-bit word quantities per 48Mhz frame. The default link clock of 24.000MHz provides 500 bits per frame, or 31.25 words in total. 36 bits are used for response, leaving 29 words available for data payload. 00h = 0 word 01h = 1 word payload. ..... FFh = 256 word payload.

14.2.6 GCTL—Global Control Register (High Definition Audio Controller—D27:F0)

Memory Address: AZBAR + 08h Attribute: R/W
Default Value: 00000000h Size: 32 bits

Bit	Description
31:9	Reserved.
8	**Accept Unsolicited Response Enable**— R/W. 0 = Unsolicited responses from the codecs are not accepted. 1 = Unsolicited response from the codecs are accepted by the controller and placed into the Response Input Ring Buffer.

Bit	Description
7:2	Reserved.
1	**Flush Control** — R/W. Writing a 1 to this bit initiates a flush. When the flush completion is received by the controller, hardware sets the Flush Status bit and clears this Flush Control bit. Before a flush cycle is initiated, the DMA Position Buffer must be programmed with a valid memory address by software, but the DMA Position Buffer bit 0 needs not be set to enable the position reporting mechanism. Also, all streams must be stopped (the associated RUN bit must be 0). When the flush is initiated, the controller will flush the pipelines to memory to guarantee that the hardware is ready to transition to a D3 state. Setting this bit is not a critical step in the power state transition if the content of the FIFIOs is not critical.
0	**Controller Reset #**— R/W. 0 = Writing a 0 to this bit causes the Intel High Definition Audio controller to be reset. All state machines, FIFOs and non-resume well memory mapped configuration registers (not PCI configuration registers) in the controller will be reset. The Intel High Definition Audio link RESET# signal will be asserted, and all other link signals will be driven to their default values. After the hardware has completed sequencing into the reset state, it will report a 0 in this bit. Software must read a 0 from this bit to verify the controller is in reset. 1 = Writing a 1 to this bit causes the controller to exit its reset state and deassert the Intel High Definition Audio link RESET# signal. Software is responsible for setting/clearing this bit such that the minimum Intel High Definition Audio link RESET# signal assertion pulse width specification is met. When the controller hardware is ready to begin operation, it will report a 1 in this bit. Software must read a 1 from this bit before accessing any controller registers. This bit defaults to a 0 after Hardware reset, therefore, software needs to write a 1 to this bit to begin operation. Note: The CORB/RIRB RUN bits and all stream RUN bits must be verified cleared to 0 before writing a 0 to this bit in order to assure a clean re-start. When setting or clearing this bit, software must ensure that minimum link timing requirements (minimum RESET# assertion time, and so forth) are met. When this bit is 0 indicating that the controller is in reset, all Intel High Definition Audio memory mapped registers are ignored as if the device is not present. The only exception is this bit itself, which will cause the controller to leave the reset state when a 1 is written to it.

14.2.7 WAKEEN—Wake Enable Register (High Definition Audio Controller—D27:F0)

Memory Address: AZBAR + 0Ch Attribute: R/W
Default Value: 0000h Size: 16 bits

Bit	Description
15:3	Reserved.
2:0	**SDIN Wake Enable Flags**— R/W. These bits control which SDI signal(s) may generate a wake event. A 1b in the bit mask indicates that the associated SDIN signal is enabled to generate a wake. Bit 0 is used for SDI[0] Bit 1 is used for SDI[1] Bit 2 is used for SDI[2] Note: These bits are in the resume well and only cleared on a power on reset. Software must not make assumptions about the reset state of these bits and must set them appropriately.

14.2.8 STATESTS—State Change Status Register (High Definition Audio Controller—D27:F0)

Memory Address: AZBAR + 0Eh
Default Value: 0000h
Attribute: R/WC
Size: 16 bits

Bit	Description
15:3	Reserved.
2:0	**SDIN State Change Status Flags**— R/WC. Flag bits that indicate which SDI signal(s) received a state change event. The bits are cleared by writing 1's to them. Bit 0 = SDI[0] Bit 1 = SDI[1] Bit 2 = SDI[2] Note: These bits are in the resume well and only cleared on a power on reset. Software must not make assumptions about the reset state of these bits and must set them appropriately.

14.2.9 GSTS—Global Status Register (High Definition Audio Controller—D27:F0)

Memory Address: AZBAR + 10h
Default Value: 0000h
Attribute: R/WC
Size: 16 bits

Bit	Description
15:2	Reserved.
1	**Flush Status**— R/WC. This bit is set to 1 by hardware to indicate that the flush cycle initiated when the Flush Control bit (AZBAR + 08h, bit 1) was set has completed. Software must write a 1 to clear this bit before the next time the Flush Control bit is set to clear the bit.
0	Reserved.

14.2.10 INTCTL—Interrupt Control Register (High Definition Audio Controller—D27:F0)

Memory Address: AZBAR + 20h
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

Bit	Description
31	**Global Interrupt Enable (GIE)**—R/W. Global bit to enable device interrupt generation. When set to 1, the Intel High Definition Audio function is enabled to generate an interrupt. This control is in addition to any bits in the bus specific address space, such as the Interrupt Enable bit in the PCI configuration space. ***Note:*** This bit is not affected by the $D3_{HOT}$ to D0 transition.

Bit	Description
30	**Controller Interrupt Enable (CIE)**— R/W. Enables the general interrupt for controller functions. When set to 1, the controller generates an interrupt when the corresponding status bit gets set due to a Response Interrupt, a Response Buffer Overrun, and State Change events. ***Note:*** This bit is not affected by the $D3_{HOT}$ to D0 transition.
29:8	Reserved
7:0	**Stream Interrupt Enable (SIE)**—R/W. When set to 1, the individual streams are enabled to generate an interrupt when the corresponding status bits get set. A stream interrupt will be caused as a result of a buffer with IOC = 1in the BDL entry being completed, or as a result of a FIFO error (underrun or overrun) occurring. Control over the generation of each of these sources is in the associated Stream Descriptor. The streams are numbered and the SIE bits assigned sequentially, based on their order in the register set. Bit 0: input stream 1 Bit 1: input stream 2 Bit 2: input stream 3 Bit 3: input stream 4 Bit 4: output stream 1 Bit 5: output stream 2 Bit 6: output stream 3 Bit 7: output stream 4

14.2.11 INTSTS—Interrupt Status Register (High Definition Audio Controller—D27:F0)

Memory Address: AZBAR + 24h
Default Value: 00000000h
Attribute: RO
Size: 32 bits

Bit	Description
31	Global Interrupt Status (GIS)—RO. This bit is an OR of all the interrupt status bits in this register. ***Note:*** This bit is not affected by the $D3_{HOT}$ to D0 transition.
30	**Controller Interrupt Status (CIS)**— RO. Status of general controller interrupt. 1 = indicates that an interrupt condition occurred due to a Response Interrupt, a Response Buffer Overrun Interrupt, or a SDIN state change event. The exact cause can be determined by interrogating other registers. This bit is an OR of all of the stated interrupt status bits for this register. ***Notes:*** 1. This bit is set regardless of the state of the corresponding interrupt enable bit, but a hardware interrupt will not be generated unless the corresponding enable bit is set. 2. This bit is not affected by the $D3_{HOT}$ to D0 transition.
29:8	Reserved
7:0	**Stream Interrupt Status (SIS)**—RO. 1 = indicates that an interrupt condition occurred on the corresponding stream. This bit is an OR of all of the stream's interrupt status bits. ***Note:*** These bits are set regardless of the state of the corresponding interrupt enable bits. The streams are numbered and the SIE bits assigned sequentially, based on their order in the register set. Bit 0: input stream 1 Bit 1: input stream 2 Bit 2: input stream 3 Bit 3: input stream 4 Bit 4: output stream 1 Bit 5: output stream 2 Bit 6: output stream 3 Bit 7: output stream 4

14.2.12 WALCLK—Wall Clock Counter Register (High Definition Audio Controller—D27:F0)

Memory Address: AZBAR + 30h
Default Value: 00000000h
Attribute: RO
Size: 32 bits

Bit	Description
31:0	Wall Clock Counter— RO. 32 bit counter that is incremented on each link BCLK period and rolls over from FFFF FFFFh to 0000 0000h. This counter will roll over to 0 with a period of approximately 179 seconds. This counter is enabled while the BCLK bit is set to 1. Software uses this counter to synchronize between multiple controllers. Will be reset on controller reset.

14.2.13 SSYNC—Stream Synchronization Register (High Definition Audio Controller—D27:F0)

Memory Address: AZBAR + 34h
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

Bit	Description
31:8	Reserved
7:0	**Stream Synchronization (SSYNC)**— R/W. When set to 1, these bits block data from being sent on or received from the link. Each bit controls the associated stream descriptor (that is, bit 0 corresponds to the first stream descriptor, and so forth). To synchronously start a set of DMA engines, these bits are first set to 1. The RUN bits for the associated stream descriptors are then set to 1 to start the DMA engines. When all streams are ready (FIFORDY =1), the associated SSYNC bits can all be set to 0 at the same time, and transmission or reception of bits to or from the link will begin together at the start of the next full link frame. To synchronously stop the streams, fist these bits are set, and then the individual RUN bits in the stream descriptor are cleared by software. If synchronization is not desired, these bits may be left as 0, and the stream will simply begin running normally when the stream's RUN bit is set. The streams are numbered and the SIE bits assigned sequentially, based on their order in the register set. Bit 0: input stream 1 Bit 1: input stream 2 Bit 2: input stream 3 Bit 3: input stream 4 Bit 4: output stream 1 Bit 5: output stream 2 Bit 6: output stream 3 Bit 7: output stream 4

14.2.14 CORBLBASE—CORB Lower Base Address Register (High Definition Audio Controller—D27:F0)

Memory Address: AZBAR + 40h
Default Value: 00000000h
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31:7	**CORB Lower Base Address**— R/W. Lower address of the Command Output Ring Buffer, allowing the CORB base address to be assigned on any 128B boundary. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.
6:0	CORB Lower Base Unimplemented Bits— RO. Hardwired to 0. This required the CORB to be allocated with 128B granularity to allow for cache line fetch optimizations.

14.2.15 CORBUBASE—CORB Upper Base Address Register (High Definition Audio Controller—D27:F0)

Memory Address: AZBAR + 44h Attribute: R/W
Default Value: 00000000h Size: 32 bits

Bit	Description
31:0	**CORB Upper Base Address**— R/W. Upper 32 bits of the address of the Command Output Ring buffer. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.

14.2.16 CORBRP—CORB Read Pointer Register (High Definition Audio Controller—D27:F0)

Memory Address: AZBAR + 4Ah Attribute: R/W
Default Value: 0000h Size: 16 bits

Bit	Description
15	**CORB Read Pointer Reset**—R/W. Software writes a 1 to this bit to reset the CORB Read Pointer to 0. The CORB DMA engine must be stopped prior to resetting the Read Pointer or else DMA transfer may be corrupted. This bit is always read as 0.
14:8	Reserved.
7:0	**CORB Read Pointer**— R/W. Software writes the last valid CORB entry offset into this field in Dword granularity. The DMA engine fetches commands from the CORB until the Read pointer matches the Write pointer. Supports 256 CORB entries (256x4B = 1KB). This register field may be written when the DMA engine is running.

14.2.17 CORBCTL—CORB Control Register (High Definition Audio Controller—D27:F0)

Memory Address: AZBAR + 4Ch Attribute: R/W
Default Value: 00h Size: 8 bits

Bit	Description
7:2	Reserved.
1	**Enable CORB DMA Engine**— R/W. 0 = DMA stop 1 = DMA run After software writes a 0 to this bit, the hardware may not stop immediately. The hardware will physically update the bit to 0 when the DMA engine is truly stopped. Software must read a 0 from this bit to verify that the DMA engine is truly stopped.
0	**CORB Memory Error Interrupt Enable**— R/W. If this bit is set the controller will generate an interrupt if the CMEI status bit (AZBAR + 4Dh: bit 0) is set.

14.2.18 CORBST—CORB Status Register (High Definition Audio Controller—D27:F0)

Memory Address: AZBAR + 4Dh Attribute: R/WC
Default Value: 00h Size: 8 bits

Bit	Description
7:1	Reserved.
0	**CORB Memory Error Indication (CMEI)**— R/WC. If this bit is set, the controller has detected an error in the path way between the controller and memory. This may be an ECC bit error or any other type of detectable data error which renders the command data fetched invalid. Software can clear this bit by writing a 1 to it. However, this type of error leaves the audio subsystem in an unviable state and typically required a controller reset by writing a 0 to the Controller Reset # bit (AZBAR + 08h: bit 0).

14.2.19 CORBSIZE—CORB Size Register (High Definition Audio Controller—D27:F0)

Memory Address: AZBAR + 4Eh Attribute: RO
Default Value: 42h Size: 8 bits

Bit	Description
7:4	CORB Size Capability—RO. Hardwired to 0100b indicating that CORB size of 256 CORB entries (1024B) is supported
3:2	Reserved.
1:0	CORB Size— RO. Hardwired to 10b which sets the CORB size to 256 entries (1024B)

14.2.20 RIRBLBASE—RIRB Lower Base Address Register (High Definition Audio Controller—D27:F0)

Memory Address: AZBAR + 50h Attribute: R/W, RO
Default Value: 00000000h Size: 32 bits

Bit	Description
31:7	**RIRB Lower Base Address**— R/W. Lower address of the Response Input Ring Buffer, allowing the RIRB base address to be assigned on any 128B boundary. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.
6:0	RIRB Lower Base Unimplemented Bits— RO. Hardwired to 0. This required the RIRB to be allocated with 128B granularity to allow for cache line fetch optimizations.

14.2.21 RIRBUBASE—RIRB Upper Base Address Register (High Definition Audio Controller—D27:F0)

Memory Address: AZBAR + 54h Attribute: R/W
Default Value: 00000000h Size: 32 bits

Bit	Description
31:0	**RIRB Upper Base Address**— R/W. Upper 32 bits of the address of the Response Input Ring Buffer. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.

14.2.22 RIRBWP—RIRB Write Pointer Register (High Definition Audio Controller—D27:F0)

Memory Address: AZBAR + 58h
Default Value: 0000h
Attribute: R/W, RO
Size: 16 bits

Bit	Description
15	**RIRB Write Pointer Reset**—R/W. Software writes a 1 to this bit to reset the RIRB Write Pointer to 0. The RIRB DMA engine must be stopped prior to resetting the Write Pointer or else DMA transfer may be corrupted. This bit is always read as 0.
14:8	Reserved.
7:0	RIRB Write Pointer (RIRBWP) — RO. Indicates the last valid RIRB entry written by the DMA controller. Software reads this field to determine how many responses it can read from the RIRB. The value read indicates the RIRB Write Pointer offset in 2 Dword RIRB entry units (since each RIRB entry is 2 Dwords long). Supports up to 256 RIRB entries (256 x 8 B = 2 KB). This register field may be written when the DMA engine is running.

14.2.23 RINTCNT—Response Interrupt Count Register (High Definition Audio Controller—D27:F0)

Memory Address: AZBAR + 5Ah
Default Value: 0000h
Attribute: R/W
Size: 16 bits

Bit	Description
15:8	Reserved.
7:0	**N Response Interrupt Count**— R/W. 0000 0001b = 1 response sent to RIRB ..... 1111 1111b = 255 responses sent to RIRB 0000 0000b = 256 responses sent to RIRB The DMA engine should be stopped when changing this field or else an interrupt may be lost. Note that each response occupies 2 Dwords in the RIRB. This is compared to the total number of responses that have been returned, as opposed to the number of frames in which there were responses. If more than one codecs responds in one frame, then the count is increased by the number of responses received in the frame.

14.2.24 RIRBCTL—RIRB Control Register (High Definition Audio Controller—D27:F0)

Memory Address: AZBAR + 5Ch
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:3	Reserved.
2	**Response overrun Interrupt Control**—R/W. If this bit is set, the hardware will generate an interrupt when the Response Overrun Interrupt Status bit (AZBAR + 5Dh: bit 2) is set.
1	**Enable RIRB DMA Engine**— R/W. 0 = DMA stop 1 = DMA run After software writes a 0 to this bit, the hardware may not stop immediately. The hardware will physically update the bit to 0 when the DMA engine is truly stopped. Software must read a 0 from this bit to verify that the DMA engine is truly stopped.
0	**Response Interrupt Control**— R/W. 0 = Disable Interrupt 1 = Generate an interrupt after N number of responses are sent to the RIRB buffer OR when an empty Response slot is encountered on all SDI[x] inputs (whichever occurs first). The N counter is reset when the interrupt is generated.

14.2.25 RIRBSTS—RIRB Status Register (High Definition Audio Controller—D27:F0)

Memory Address: AZBAR + 5Dh
Default Value: 00h
Attribute: R/WC
Size: 8 bits

Bit	Description
7:3	Reserved.
2	**Response Overrun Interrupt Status**— R/WC. Software sets this bit to 1 when the RIRB DMA engine is not able to write the incoming responses to memory before additional incoming responses overrun the internal FIFO. When the overrun occurs, the hardware will drop the responses which overrun the buffer. An interrupt may be generated if the Response Overrun Interrupt Control bit is set. Note that this status bit is set even if an interrupt is not enabled for this event. Software clears this bit by writing a 1 to it.
1	Reserved.
0	Response Interrupt— R/WC. Hardware sets this bit to 1 when an interrupt has been generated after N number of Responses are sent to the RIRB buffer OR when an empty Response slot is encountered on all SDI[x] inputs (whichever occurs first). Note that this status bit is set even if an interrupt is not enabled for this event. Software clears this bit by writing a 1 to it.

14.2.26 RIRBSIZE—RIRB Size Register (High Definition Audio Controller—D27:F0)

Memory Address: AZBAR + 5Eh
Default Value: 42h
Attribute: RO
Size: 8 bits

Bit	Description
7:4	RIRB Size Capability—RO. Hardwired to 0100b indicating that RIRB size of 256 RIRB entries (2048B) is supported
3:2	Reserved.
1:0	RIRB Size— RO. Hardwired to 10b which sets the CORB size to 256 entries (2048B)

14.2.27 IC—Immediate Command Register (High Definition Audio Controller—D27:F0)

Memory Address: AZBAR + 60h
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

Bit	Description
31:0	**Immediate Command Write—R/W**. The command to be sent to the codec via the Immediate Command mechanism is written to this register. The command stored in this register is sent out over the link during the next available frame after a 1 is written to the ICB bit (AZBAR + 68h: bit 0)

14.2.28 IR—Immediate Response Register (High Definition Audio Controller—D27:F0)

Memory Address: AZBAR + 64h
Default Value: 00000000h
Attribute: RO
Size: 32 bits

Bit	Description
31:0	Immediate Response Read (IRR)—RO. This register contains the response received from a codec resulting from a command sent via the Immediate Command mechanism. If multiple codecs responded in the same time, there is no guarantee as to which response will be latched. Therefore, broadcast-type commands must not be issued via the Immediate Command mechanism.

14.2.29 IRS—Immediate Command Status Register (High Definition Audio Controller—D27:F0)

Memory Address: AZBAR + 68h
Default Value: 0000h
Attribute: R/W, R/WC
Size: 16 bits

Bit	Description
15:2	Reserved.
1	**Immediate Result Valid (IRV)**—R/WC. This bit is set to 1 by hardware when a new response is latched into the Immediate Response register (AZBAR + 64). This is a status flag indicating that software may read the response from the Immediate Response register. Software must clear this bit by writing a 1 to it before issuing a new command so that the software may determine when a new response has arrived.
0	**Immediate Command Busy (ICB)** —R/W. When this bit is read as 0, it indicates that a new command may be issued using the Immediate Command mechanism. When this bit transitions from a 0 to a 1 (via software writing a 1), the controller issues the command currently stored in the Immediate Command register to the codec over the link. When the corresponding response is latched into the Immediate Response register, the controller hardware sets the IRV flag and clears the ICB bit back to 0. ***Note:*** An Immediate Command must not be issued while the CORB/RIRB mechanism is operating, otherwise the responses conflict. This must be enforced by software.

14.2.30 DPLBASE—DMA Position Lower Base Address Register (High Definition Audio Controller—D27:F0)

Memory Address: AZBAR + 70h
Default Value: 00000000h
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31:7	**DMA Position Lower Base Address**—R/W. Lower 32 bits of the DMA Position Buffer Base Address. This register field must not be written when any DMA engine is running or the DMA transfer may be corrupted. This same address is used by the Flush Control and must be programmed with a valid value before the Flush Control bit (AZBAR+08h:bit 1) is set.
6:1	DMA Position Lower Base Unimplemented bits—RO. Hardwired to 0 to force the 128 byte buffer alignment for cache line write optimizations.
0	**DMA Position Buffer Enable**—R/W. When this bit is set to 1, the controller will write the DMA positions of each of the DMA engines to the buffer in the main memory periodically (typically once per frame). Software can use this value to know what data in memory is valid data.

14.2.31 DPUBASE—DMA Position Upper Base Address Register (High Definition Audio Controller—D27:F0)

Memory Address: AZBAR + 74h
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

Bit	Description
31:0	**DMA Position Upper Base Address**—R/W. Upper 32 bits of the DMA Position Buffer Base Address. This register field must not be written when any DMA engine is running or the DMA transfer may be corrupted.

14.2.32 SDCTL—Stream Descriptor Control Register (High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: AZBAR + 80hAttribute: R/W, RO
Input Stream[1]: AZBAR + A0h
Input Stream[2]: AZBAR + C0h
Input Stream[3]: AZBAR + E0h
Output Stream[0]: AZBAR + 100h
Output Stream[1]: AZBAR + 120h
Output Stream[2]: AZBAR + 140h
Output Stream[3]: AZBAR + 160h

Default Value: 040000h Size: 24 bits

Bit	Description
23:20	**Stream Number**—R/W. This value reflect the Tag associated with the data being transferred on the link. When data controlled by this descriptor is sent out over the link, it will have its stream number encoded on the SYNC signal. When an input stream is detected on any of the SDI signals that match this value, the data samples are loaded into FIFO associated with this descriptor. Note that while a single SDI input may contain data from more than one stream number, two different SDI inputs may not be configured with the same stream number. 0000 = Reserved 0001 = Stream 1 …….. 1110 = Stream 14 1111 = Stream 15
19	Bidirectional Direction Control—RO. This bit is only meaningful for bidirectional streams; therefore, this bit is hardwired to 0.
18	Traffic Priority—RO. Hardwired to 1 indicating that all streams will use VC1 if it is enabled through the PCI Express registers.
17:16	Stripe Control—RO. This bit is only meaningful for input streams; therefore, this bit is hardwired to 0.
15:5	Reserved
4	**Descriptor Error Interrupt Enable**—R/W. 0 = Disable 1 = An interrupt is generated when the Descriptor Error Status bit is set.
3	**FIFO Error Interrupt Enable**—R/W. This bit controls whether the occurrence of a FIFO error (overrun for input or underrun for output) will cause an interrupt or not. If this bit is not set, bit 3in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.

Bit	Description
2	**Interrupt on Completion Enable**—R/W. This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set, bit 2 in the Status register will be set, but the interrupt will not occur.
1	**Stream Run (RUN)**—R/W. 0 = When cleared to 0, the DMA engine associated with this input stream will be disabled. The hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine. 1 = When set to 1, the DMA engine associated with this input stream will be enabled to transfer data from the FIFO to the main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set.
0	**Stream Reset (SRST)**—R/W. 0 = Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. 1 = Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. The RUN bit must be cleared before SRST is asserted.

14.2.33 SDSTS—Stream Descriptor Status Register (High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: AZBAR + 83h
Input Stream[1]: AZBAR + A3h
Input Stream[2]: AZBAR + C3h
Input Stream[3]: AZBAR + E3h
Output Stream[0]: AZBAR + 103h
Output Stream[1]: AZBAR + 123h
Output Stream[2]: AZBAR + 143h
Output Stream[3]: AZBAR + 163h

Attribute:R/WC, RO

Default Value: 00h

Size: 8 bits

Bit	Description
7:6	Reserved.
5	FIFO Ready (FIFORDY)—RO. For output streams, the controller hardware will set this bit to 1 while the output DMA FIFO contains enough data to maintain the stream on the link. This bit defaults to 0 on reset because the FIFO is cleared on a reset. For input streams, the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set.
4	**Descriptor Error**—R/WC. When set, this bit indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort, a parity or ECC error on the bus, or any other error which renders the current Buffer Descriptor or Buffer Descriptor list useless. This error is treated as a fatal stream error, as the stream cannot continue running. The RUN bit will be cleared and the stream will stopped. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.

Bit	Description
3	**FIFO Error**—R/WC. This bit is set when a FIFO error occurs. This bit is set even if an interrupt is not enabled. The bit is cleared by writing a 1 to it. For an input stream, this indicates a FIFO overrun occurring while the RUN bit is set. When this happens, the FIFO pointers do not increment and the incoming data is not written into the FIFO, thereby being lost. For an output stream, this indicates a FIFO underrun when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
2	**Buffer Completion Interrupt Status**—R/WC. This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to it.
1:0	Reserved.

14.2.34 SDLPIB—Stream Descriptor Link Position in Buffer Register (High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: AZBAR + 84h — Attribute:RO
Input Stream[1]: AZBAR + A4h
Input Stream[2]: AZBAR + C4h
Input Stream[3]: AZBAR + E4h
Output Stream[0]: AZBAR + 104h
Output Stream[1]: AZBAR + 124h
Output Stream[2]: AZBAR + 144h
Output Stream[3]: AZBAR + 164h

Default Value: 00000000h — Size: 32 bits

Bit	Description
31:0	Link Position in Buffer—RO. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

14.2.35 SDCBL—Stream Descriptor Cyclic Buffer Length Register (High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: AZBAR + 88h — Attribute:R/W
Input Stream[1]: AZBAR + A8h
Input Stream[2]: AZBAR + C8h
Input Stream[3]: AZBAR + E8h
Output Stream[0]: AZBAR + 108h
Output Stream[1]: AZBAR + 128h
Output Stream[2]: AZBAR + 148h
Output Stream[3]: AZBAR + 168h

Default Value: 00000000h — Size: 32 bits

Bit	Description
31:0	**Cyclic Buffer Length**—R/W. Indicates the number of bytes in the complete cyclic buffer. This register represents an integer number of samples. Link Position in Buffer will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should be only modified when the RUN bit is 0. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfer may be corrupted.

14.2.36 SDLVI—Stream Descriptor Last Valid Index Register (High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: AZBAR + 8Ch — Attribute:R/W
Input Stream[1]: AZBAR + ACh
Input Stream[2]: AZBAR + CCh
Input Stream[3]: AZBAR + ECh
Output Stream[0]: AZBAR + 10Ch
Output Stream[1]: AZBAR + 12Ch
Output Stream[2]: AZBAR + 14Ch
Output Stream[3]: AZBAR + 16Ch

Default Value: 0000h — Size: 16 bits

Bit	Description
15:8	Reserved.
7:0	**Last Valid Index**—R/W. The value written to this register indicates the index for the last valid Buffer Descriptor in BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. This field must be at least 1, that is, there must be at least 2 valid entries in the buffer descriptor list before DMA operations can begin. This value should only modified when the RUN bit is 0.

14.2.37 SDFIFOW—Stream Descriptor FIFO Watermark Register (High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: AZBAR + 8Eh — Attribute:R/W
Input Stream[1]: AZBAR + AEh
Input Stream[2]: AZBAR + CEh
Input Stream[3]: AZBAR + EEh
Output Stream[0]: AZBAR + 10Eh
Output Stream[1]: AZBAR + 12Eh
Output Stream[2]: AZBAR + 14Eh
Output Stream[3]: AZBAR + 16Eh

Default Value: 0004h — Size: 16 bits

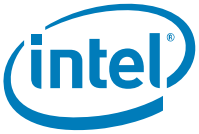
Bit	Description
15:3	Reserved.
2:0	**FIFO Watermark (FIFOW)**—R/W. Indicates the minimum number of bytes accumulated/free in the FIFO before the controller will start a fetch/eviction of data. 010 = 8B 011 = 16B 100 = 32B (Default) Others = Unsupported Note: When the bit field is programmed to an unsupported size, the hardware sets itself to the default value. Software must read the bit field to test if the value is supported after setting the bit field.

14.2.38 SDFIFOS—Stream Descriptor FIFO Size Register (High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: AZBAR + 90h
Input Stream[1]: AZBAR + B0h
Input Stream[2]: AZBAR + D0h
Input Stream[3]: AZBAR + F0h
Output Stream[0]: AZBAR + 110h
Output Stream[1]: AZBAR + 130h
Output Stream[2]: AZBAR + 150h
Output Stream[3]: AZBAR + 170h
Attribute: Input: RO, Output: R/W

Default Value: Input Stream: 0077h, Output Stream: 00BFh
Size: 16 bits

Bit	Description
15:8	Reserved.
7:0	**FIFO Size**—RO (Input stream), R/W (Output stream). Indicates the maximum number of bytes that could be fetched by the controller at one time. This is the maximum number of bytes that may have been DMA'd into memory but not yet transmitted on the link, and is also the maximum possible value that the PICB count will increase by at one time. The value in this field is different for input and output streams. It is also dependent on the Bits per Samples setting for the corresponding stream. Following are the values read/written from/to this register for input and output streams, and for non-padded and padded bit formats: *Output Stream R/W value*: 0Fh = 16B8, 16, 20, 24, or 32 bit Output Streams 1Fh = 32B8, 16, 20, 24, or 32 bit Output Streams 3Fh = 64B8, 16, 20, 24, or 32 bit Output Streams 7Fh = 128B8, 16, 20, 24, or 32 bit Output Streams BFh = 192B8, 16, or 32 bit Output Streams FFh = 256B20, 24 bit Output Streams ***Notes:*** 1. All other values not listed are not supported. 2. When the output stream is programmed to an unsupported size, the hardware sets itself to the default value (BFh). 3. Software must read the bit field to test if the value is supported after setting the bit field. *Input Stream RO value*: 77h = 120B8, 16, 32 bit Input Streams 9Fh = 160B20, 24 bit Input Streams ***Note:*** The default value is different for input and output streams, and reflects the default state of the BITS fields (in Stream Descriptor Format registers) for the corresponding stream.



14.2.39 SDFMT—Stream Descriptor Format Register (High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: AZBAR + 92h
Input Stream[1]: AZBAR + B2h
Input Stream[2]: AZBAR + D2h
Input Stream[3]: AZBAR + F2h
Output Stream[0]: AZBAR + 112h
Output Stream[1]: AZBAR + 132h
Output Stream[2]: AZBAR + 152h
Output Stream[3]: AZBAR + 172h

Attribute:R/W

Default Value: 0000h

Size: 16 bits

Bit	Description
15	Reserved.
14	**Sample Base Rate**—R/W 0 = 48 kHz 1 = 44.1 kHz
13:11	**Sample Base Rate Multiple**—R/W 000 = 48 kHz, 44.1 kHz or less 001 = x2 (96 kHz, 88.2 kHz, 32 kHz) 010 = x3 (144 kHz) 011 = x4 (192 kHz, 176.4 kHz) Others = Reserved.
10:8	**Sample Base Rate Devisor**—R/W. 000 = Divide by 1(48 kHz, 44.1 kHz) 001 = Divide by 2 (24 kHz, 22.05 kHz) 010 = Divide by 3 (16 kHz, 32 kHz) 011 = Divide by 4 (11.025 kHz) 100 = Divide by 5 (9.6 kHz) 101 = Divide by 6 (8 kHz) 110 = Divide by 7 111 = Divide by 8 (6 kHz)
7	Reserved.
6:4	**Bits per Sample (BITS)**—R/W. 000 = 8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001 = 16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010 = 20 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries 011 = 24 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries 100 = 32 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries Others = Reserved.
3:0	Number of channels (CHAN)—R/W. Indicates number of channels in each frame of the stream. 0000 =1 0001 =2 ..... 1111 =16

14.2.40 SDBDPL—Stream Descriptor Buffer Descriptor List Pointer Lower Base Address Register (High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: AZBAR + 98h — Attribute:R/W,RO
Input Stream[1]: AZBAR + B8h
Input Stream[2]: AZBAR + D8h
Input Stream[3]: AZBAR + F8h
Output Stream[0]: AZBAR + 118h
Output Stream[1]: AZBAR + 138h
Output Stream[2]: AZBAR + 158h
Output Stream[3]: AZBAR + 178h

Default Value: 00000000h — Size: 32 bits

Bit	Description
31:7	**Buffer Descriptor List Pointer Lower Base Address**—R/W. Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0, or DMA transfer may be corrupted.
6:0	Hardwired to 0 forcing alignment on 128-B boundaries.

14.2.41 SDBDPU—Stream Descriptor Buffer Descriptor List Pointer Upper Base Address Register (High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: AZBAR + 9Ch — Attribute:R/W
Input Stream[1]: AZBAR + BCh
Input Stream[2]: AZBAR + DCh
Input Stream[3]: AZBAR + FCh
Output Stream[0]: AZBAR + 11Ch
Output Stream[1]: AZBAR + 13Ch
Output Stream[2]: AZBAR + 15Ch
Output Stream[3]: AZBAR + 17Ch

Default Value: 00000000h — Size: 32 bits

Bit	Description
31:0	**Buffer Descriptor List Pointer Upper Base Address**—R/W. Upper 32-bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0, or DMA transfer may be corrupted.

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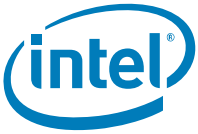


15 PCI Express* Configuration Registers

15.1 PCI Express* Configuration Registers (PCI Express – D28:F0/F1/F2/F3)

Note: Register address locations that are not shown in Table 15-1 and should be treated as Reserved.

Table 15-1. PCI Express* Configuration Registers Address Map (PCI Express – D28:F0/F1/F2/F3) (Sheet 1 of 3)

Offset	Mnemonic	Register Name	Function 0 Default	Function 1 Default	Function 2 Default	Function 3 Default	Type
00–01h	VID	Vendor Identification	8086h	8086h	8086h	8086h	RO
02–03h	DID	Device Identification	See register description	See register description	See register description	See register description	RO
04–05h	PCICMD	PCI Command	0000h	0000h	0000h	0000h	R/W, RO
06–07h	PCISTS	PCI Status	0010h	0010h	0010h	0010h	R/WC, RO
08h	RID	Revision Identification	See register description.	See register description.	See register description.	See register description.	RO
09h	PI	Programming Interface	00h	00h	00h	00h	RO
0Ah	SCC	Sub Class Code	04h	04h	04h	04h	RO
0Bh	BCC	Base Class Code	06h	06h	06h	06h	RO
0Ch	CLS	Cache Line Size	00h	00h	00h	00h	R/W
0Dh	PLT	Primary Latency Timer	00h	00h	00h	00h	RO
0Eh	HEADTYP	Header Type	81h	81h	81h	81h	RO
18–1Ah	BNUM	Bus Number	000000h	000000h	000000h	000000h	R/W
1C–1Dh	IOBL	I/O Base and Limit	0000h	0000h	0000h	0000h	R/W, RO
1E–1Fh	SSTS	Secondary Status Register	0000h	0000h	0000h	0000h	R/WC
20–23h	MBL	Memory Base and Limit	00000000h	00000000h	00000000h	00000000h	R/W
24–27h	PMBL	Prefetchable Memory Base and Limit	00010001h	00010001h	00010001h	00010001h	R/W, RO
28–2Bh	PMBU32	Prefetchable Memory Base Upper 32 Bits	00000000h	00000000h	00000000h	00000000h	R/W
2C–2Fh	PMLU32	Prefetchable Memory Limit Upper 32 Bits	00000000h	00000000h	00000000h	00000000h	R/W
34h	CAPP	Capabilities List Pointer	40h	40h	40h	40h	RO
3C–3Dh	INTR	Interrupt Information	See bit description	See bit description	See bit description	See bit description	R/W, RO
3E–3Fh	BCTRL	Bridge Control Register	0000h	0000h	0000h	0000h	R/W
40–41h	CLIST	Capabilities List	8010	8010	8010	8010	RO
42–43h	XCAP	PCI Express Capabilities	0041	0041	0041	0041	R/WO, RO
44–47h	DCAP	Device Capabilities	00000FE0h	00000FE0h	00000FE0h	00000FE0h	RO

Table 15-1. PCI Express* Configuration Registers Address Map (PCI Express – D28:F0/F1/F2/F3) (Sheet 2 of 3)

Offset	Mnemonic	Register Name	Function 0 Default	Function 1 Default	Function 2 Default	Function 3 Default	Type
48–49h	DCTL	Device Control	0000h	0000h	0000h	0000h	R/W, RO
4A–4Bh	DSTS	Device Status	0010h	0010h	0010h	0010h	R/WC, RO
4C–4Fh	LCAP	Link Capabilities	See bit description	See bit description	See bit description	See bit description	R/W, RO
50–51h	LCTL	Link Control	0000h	0000h	0000h	0000h	R/W, R/W (special), RO
52–53h	LSTS	Link Status	See bit description	See bit description	See bit description	See bit description	RO
54–57h	SLCAP	Slot Capabilities Register	00000060h	00000060h	00000060h	00000060h	R/WO, RO
58–59h	SLCTL	Slot Control	0000h	0000h	0000h	0000h	R/W, RO
5A–5Bh	SLSTS	Slot Status	0000h	0000h	0000h	0000h	R/WC, RO
5C–5Dh	RCTL	Root Control	0000h	0000h	0000h	0000h	R/W
60–63h	RSTS	Root Status	00000000h	00000000h	00000000h	00000000h	R/WC, RO
80–81h	MID	Message Signaled Interrupt Identifiers	9005h	9005h	9005h	9005h	RO
82–83h	MC	Message Signaled Interrupt Message Control	0000h	0000h	0000h	0000h	R/W, RO
84–87h	MA	Message Signaled Interrupt Message Address	0000h	0000h	0000h	0000h	R/W
88–89h	MD	Message Signaled Interrupt Message Data	0000h	0000h	0000h	0000h	R/W
90–91h	SVCAP	Subsystem Vendor Capability	A00Dh	A00Dh	A00Dh	A00Dh	RO
94–97h	SVID	Subsystem Vendor Identification	00000000h	00000000h	00000000h	00000000h	R/WO
A0–A1h	PMCAP	Power Management Capability	0001h	0001h	0001h	0001h	RO
A2–A3h	PMC	PCI Power Management Capability	C802h	C802h	C802h	C802h	RO
A4–A7h	PMCS	PCI Power Management Control and Status	00000000h	00000000h	00000000h	00000000h	R/W, RO
D8–DBh	MPC	Miscellaneous Port Configuration	00110000h	00110000h	00110000h	00110000h	R/W
DC–DFh	SMSCS	SMI/SCI Status Register	00000000h	00000000h	00000000h	00000000h	R/WC
E0h	RWC	Resume Well Control	00	00	00	00	R/W
100–103h	VCH	Virtual Channel Capability Header	18010002h	18010002h	18010002h	18010002h	RO
104–107h	VCAP1	Virtual Channel Capability 1	See bit description	See bit description	See bit description	See bit description	RO
108–10Bh	VCAP2	Virtual Channel Capability 2	00000001h	00000001h	00000001h	00000001h	RO
10C–10Dh	PVC	Port Virtual Channel Control	0000h	0000h	0000h	0000h	R/W, RO
10E–10Fh	PVS	Port Virtual Channel Status	0000h	0000h	0000h	0000h	RO

Table 15-1. PCI Express* Configuration Registers Address Map (PCI Express – D28:F0/F1/F2/F3) (Sheet 3 of 3)

Offset	Mnemonic	Register Name	Function 0 Default	Function 1 Default	Function 2 Default	Function 3 Default	Type
110–113h	V0CAP	Virtual Channel 0 Resource Capability	00000001h	00000001h	00000001h	00000001h	RO
114–117h	V0CTL	Virtual Channel 0 Resource Control	800000FFh	800000FFh	800000FFh	800000FFh	R/W, RO
11A–11Bh	V0STS	Virtual Channel 0 Resource Status	0000h	0000h	0000h	0000h	RO
11C–11Fh	V1CAP	Virtual Channel 1 Resource Capability	See bit description	See bit description	See bit description	See bit description	RO
120–123h	V1CTL	Virtual Channel 1 Resource Control	00000000h	00000000h	00000000h	00000000h	R/W, RO
126–127h	V1STS	Virtual Channel 1 Resource Status	0000h	0000h	0000h	0000h	RO
144–147h	UES	Uncorrectable Error Status	See bit description	See bit description	See bit description	See bit description	R/WC, RO
148–14Bh	UEM	Uncorrectable Error Mask	00000000h	00000000h	00000000h	00000000h	R/WO, RO
14C–14Fh	UEV	Uncorrectable Error Severity	00060011h	00060011h	00060011h	00060011h	RO
150–153h	CES	Correctable Error Status	00000000h	00000000h	00000000h	00000000h	R/WC
154–157h	CEM	Correctable Error Mask	00000000h	00000000h	00000000h	00000000h	R/WO
158–15Bh	AECC	Advanced Error Capabilities and Control	00000000h	00000000h	00000000h	00000000h	RO
170–173h	RES	Root Error Status	00000000h	00000000h	00000000h	00000000h	R/WC, RO
180–183h	RCTCL	Root Complex Topology Capability List	00010005h	00010005h	00010005h	00010005h	RO
184–187h	ESD	Element Self Description	See bit description	See bit description	See bit description	See bit description	RO
18C–18Fh	ULD	Upstream Link Description	00000001h	00000001h	00000001h	00000001h	RO
190–197h	ULBA	Upstream Link Base Address	See bit description	See bit description	See bit description	See bit description	RO

15.1.1 VID – Vendor Identification Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 00–01h
Default Value: 8086h
Attribute: RO
Size: 16 bits

Bit	Description
15:0	Vendor ID – RO. This is a 16-bit value assigned to Intel

15.1.2 DID – Device Identification Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 02–03h
Default Value: See description
Attribute: RO
Size: 16 bits

Bit	Description
15:0	Device ID – RO. Bit 0 of this field reflects the state of fuses FDPCIE. Por# Device ID **(FDPCIE=0)** Device ID **(FDPCIE=1)** 1. 2690 2691 2. 2692 2693 3. 2694 2695 4. 2696 2697

15.1.3 PCICMD – PCI Command Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 04–05h
Default Value: 0000h
Attribute: R/W, RO
Size: 16 bits

Bit	Description
15:11	Reserved
10	**Interrupt Disable –** R/W. This disables pin-based INTx# interrupts on enabled Hot-Plug and power management events. This bit has no effect on MSI operation. 0 = bInternal INTx# messages are generated if there is an interrupt for Hot-Plug or power management and MSI is not enabled. 1 = Internal INTx# messages will not be generated. This bit does not affect interrupt forwarding from devices connected to the root port. Assert_INTx and Deassert_INTx messages will still be forwarded to the internal interrupt controllers if this bit is set.
9	Fast Back to Back Enable (FBE) – Reserved per the PCI Express Base Specification.
8	**SERR# Enable (SEE)** – R/W. 0 = Disable. 1 = Enables the root port to generate an SERR# message when PSTS.SSE is set.
7	Wait Cycle Control (WCC) – Reserved per the PCI Express Base Specification.
6	**Parity Error Response (PER)** – R/W. 0 = Disable. 1 = Indicates that the device is capable of reporting parity errors as a master on the backbone.
5	VGA Palette Snoop (VPS) – Reserved per the PCI Express Base Specification.
4	Postable Memory Write Enable (PMWE) – Reserved per the PCI Express Base Specification.
3	Special Cycle Enable (SCE) – Reserved per the PCI Express Base Specification.
2	**Bus Master Enable (BME)** – R/W. 0 = Disable. All cycles from the device are master aborted 1 = Enable. Allows the root port to forward cycles onto the backbone from a PCI Express device.
1	**Memory Space Enable (MSE)** – R/W. 0 = Disable. Memory cycles within the range specified by the memory base and limit registers are master aborted on the backbone. 1 = Enable. Allows memory cycles within the range specified by the memory base and limit registers can be forwarded to the PCI Express device.
0	**I/O Space Enable (IOSE)** – R/W. This bit controls access to the I/O space registers. 0 = Disable. I/O cycles within the range specified by the I/O base and limit registers are master aborted on the backbone. 1 = Enable. Allows I/O cycles within the range specified by the I/O base and limit registers can be forwarded to the PCI Express device.

15.1.4 PCISTS – PCI Status Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 06–07h
Default Value: 0010h
Attribute: R/WC, RO
Size: 16 bits

Bit	Description
15	**DPE – Detected Parity Error (DPE) –** R/WC. 0 = No parity error detected. 1 = Set when the root port receives a command or data from the backbone with a parity error. This is set even if PCIMD.PER (D28:F0/F1/F2/F3:04, bit 6) is not set.
14	**Signaled System Error (SSE) –** R/WC. 0 = No system error signaled. 1 = Set when the root port signals a system error to the internal SERR# logic.
13	**Received Master Abort (RMA) –** R/WC. 0 = Root port has not received a completion with unsupported request status from the backbone. 1 = Set when the root port receives a completion with unsupported request status from the backbone.
12	**Received Target Abort (RTA) –** R/WC. 0 = Root port has not received a completion with completer abort from the backbone. 1 = Set when the root port receives a completion with completer abort from the backbone.
11	**Signaled Target Abort (STA) –** R/WC. 0 = No target abort received. 1 = Set whenever the root port forwards a target abort received from the downstream device onto the backbone.
10:9	DEVSEL# Timing Status (DEV_STS) – Reserved per the PCI Express Base Specification.
8	**Master Data Parity Error Detected (DPED)** – R/WC. 0 = No data parity error received. 1 = Set when the root port receives a completion with a data parity error on the backbone and PCIMD.PER (D28:F0/F1/F2/F3:04, bit 6) is set.
7	Fast Back to Back Capable (FB2BC) – Reserved per the PCI Express Base Specification.
6	Reserved
5	66 MHz Capable – Reserved per the PCI Express Base Specification.
4	Capabilities List – RO. Hardwired to 1. Indicates the presence of a capabilities list.
3	**Interrupt Status –** RO. Indicates status of Hot-Plug and power management interrupts on the root port that result in INTx# message generation. 0 = Interrupt is deasserted. 1 = Interrupt is asserted. This bit is not set if MSI is enabled. If MSI is not enabled, this bit is set regardless of the state of PCICMD.Interrupt Disable bit (D28:F0/F1/F2/F3:04h:bit 10).
2:0	Reserved

15.1.5 RID – Revision Identification Register (PCI Express – D28:F0/F1/F2/F3)

Offset Address: 08h
Default Value: See bit description
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Revision ID –** RO. Refer to Table 2-33 or the *Intel® 631xESB/632xESB I/O Controller Hub EDS Specification Update* for the value of the Revision ID Register

15.1.6 PI – Programming Interface Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 09h
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	Programming Interface – RO. 00h = No specific register level programming interface defined.

15.1.7 SCC – Sub Class Code Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 0Ah
Default Value: 04h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	Sub Class Code (SCC) – RO. 04h = PCI-to-PCI bridge.

15.1.8 BCC – Base Class Code Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 0Bh
Default Value: 06h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	Base Class Code (BCC) – RO. 06h = Indicates the device is a bridge device.

15.1.9 CLS – Cache Line Size Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 0Ch
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	Base Class Code (BCC) – R/W. This is read/write but contains no functionality, per the PCI Express base specification.

15.1.10 PLT – Primary Latency Timer Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 0Dh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:3	Latency Count. Reserved per the PCI Express Base Specification.
2:0	Reserved

15.1.11 HEADTYP – Header Type Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 0Eh
Default Value: 81h
Attribute: RO
Size: 8 bits

Bit	Description
7	Multi-Function Device – RO. 0 = Single-function device. 1 = Multi-function device.
6:0	Configuration Layout. Hardwired to 01h, which indicates a PCI-to-PCI bridge.

15.1.12 BNUM – Bus Number Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 18–1Ah
Default Value: 000000h
Attribute: R/W
Size: 24 bits

Bit	Description
23:16	Subordinate Bus Number (SBBN) – R/W. Indicates the highest PCI bus number below the bridge.
15:8	Secondary Bus Number (SCBN) – R/W. Indicates the bus number the port.
7:0	Primary Bus Number (PBN) – R/W. Indicates the bus number of the backbone.

15.1.13 IOBL – I/O Base and Limit Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 1C–1Dh
Default Value: 0000h
Attribute: R/W, RO
Size: 16 bits

Bit	Description
15:12	**I/O Limit Address (IOLA) –** R/W. I/O Base bits corresponding to address lines 15:12 for 4-KB alignment. Bits 11:0 are assumed to be padded to FFFh.
11:8	**I/O Limit Address Capability (IOLC)** – R/O. Indicates that the bridge does not support 32-bit I/O addressing.
7:4	**I/O Base Address (IOBA)** – R/W. I/O Base bits corresponding to address lines 15:12 for 4-KB alignment. Bits 11:0 are assumed to be padded to 000h.
3:0	**I/O Base Address Capability (IOBC)** – R/O. Indicates that the bridge does not support 32-bit I/O addressing.

15.1.14 SSTS – Secondary Status Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 1E–1Fh
Default Value: 0000h
Attribute: R/WC
Size: 16 bits

Bit	Description
15	**Detected Parity Error (DPE)** – R/WC. 0 = No error. 1 = The port received a poisoned TLP.
14	**Received System Error (RSE)** – R/WC. 0 = No error. 1 = The port received an ERR_FATAL or ERR_NONFATAL message from the device.
13	**Received Master Abort (RMA)** – R/WC. 0 = Unsupported Request not received. 1 = The port received a completion with “Unsupported Request” status from the device.
12	**Received Target Abort (RTA)** – R/WC. 0 = Completion Abort not received. 1 = The port received a completion with “Completion Abort” status from the device.
11	**Signaled Target Abort (STA)** – R/WC. 0 = Completion Abort not sent. 1 = The port generated a completion with “Completion Abort” status to the device.
10:9	Secondary DEVSEL# Timing Status (SDTS): Reserved per PCI Express Base spec.
8	**Data Parity Error Detected (DPD)** – R/WC. 0 = Conditions below did not occur. 1 = Set when the BCTRL.PERE (D28:FO/F1/F2/F3:3E: bit 0) is set, and either of the following two conditions occurs: • Port receives completion marked poisoned. • Port poisons a write request to the secondary side.
7	Secondary Fast Back to Back Capable (SFBC): Reserved per PCI Express spec.
6	Reserved
5	Secondary 66 MHz Capable (SC66): Reserved per PCI Express spec.
4:0	Reserved

15.1.15 MBL – Memory Base and Limit Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 20–23h
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

Accesses that are within the ranges specified in this register will be sent to the attached device if CMD.MSE (D28:F0/F1/F2/F3:04:bit 1) is set. Accesses from the attached device that are outside the ranges specified will be forwarded to the backbone if CMD.BME (D28:F0/F1/F2/F3:04:bit 2) is set. The comparison performed is MB >= AD[31:20] <= ML.

Bit	Description
31:20	**Memory Limit (ML) –** R/W. These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range.
19:16	Reserved
15:4	**Memory Base (MB)** – R/W. These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range.
3:0	Reserved

15.1.16 PMBL – Prefetchable Memory Base and Limit Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 24–27h
Default Value: 00010001h
Attribute: R/W, RO
Size: 32 bits

Accesses that are within the ranges specified in this register will be sent to the device if CMD.MSE (D28:F0/F1/F2/F3;04, bit 1) is set. Accesses from the device that are outside the ranges specified will be forwarded to the backbone if CMD.BME (D28:F0/F1/F2/F3;04, bit 2) is set. The comparison performed is PMBU32:PMB >= AD[63:32]:AD[31:20] <= PMLU32:PML.

Bit	Description
31:20	**Prefetchable Memory Limit (PML) –** R/W. These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range.
19:16	**64-bit Indicator (I64L)** – RO. Indicates support for 64-bit addressing
15:4	**Prefetchable Memory Base (PMB)** – R/W. These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range.
3:0	**64-bit Indicator (I64B)** – RO. Indicates support for 64-bit addressing

15.1.17 PMBU32 – Prefetchable Memory Base Upper 32 Bits Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 28–2Bh
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

Bit	Description
31:0	**Prefetchable Memory Base Upper Portion (PMBU) –** R/W. Upper 32-bits of the prefetchable address base.

15.1.18 PMLU32 – Prefetchable Memory Limit Upper 32 Bits Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 2C–2Fh
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

Bit	Description
31:0	**Prefetchable Memory Limit Upper Portion (PMLU) –** R/W. Upper 32-bits of the prefetchable address limit.

15.1.19 CAPP – Capabilities List Pointer Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 34h
Default Value: 40h
Attribute: R0
Size: 8 bits

Bit	Description
7:0	**Capabilities Pointer (PTR) –** RO. Indicates that the pointer for the first entry in the capabilities list is at 40h in configuration space.

15.1.20 INTR – Interrupt Information Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 3C–3Dh
Default Value: See bit description
Attribute: R/W, RO
Size: 16 bits

Bit	Description
15:8	**Interrupt Pin (IPIN) –** RO. Indicates the interrupt pin driven by the root port. At reset, this register takes on the following values, which reflect the reset state of the D28IP register in chipset config space: Port Bits[15:12] Bits[11:08] 1 0h D28IP.P1IP 2 0h D28IP.P2IP 3 0h D28IP.P3IP 4 0h D28IP.P4IP ***Note:*** The value that is programmed into D28IP is always reflected in this register.
7:0	**Interrupt Line (ILINE) –** R/W. Default = 00h. Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register.

15.1.21 BCTRL – Bridge Control Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 3E–3Fh
Default Value: 0000h
Attribute: R/W
Size: 16 bits

Bit	Description
15:12	Reserved
11	Discard Timer SERR# Enable (DTSE): Reserved per PCI Express spec.
10	Discard Timer Status (DTS): Reserved per PCI Express spec.
9	Secondary Discard Timer (SDT): Reserved per PCI Express spec.
8	Primary Discard Timer (PDT): Reserved per PCI Express spec.
7	Fast Back to Back Enable (FBE): Reserved per PCI Express spec.
6	**Secondary Bus Reset (SBR)** – R/W. Triggers a hot reset on the PCI Express port.
5	Master Abort Mode (MAM): Reserved per Express spec.
4	**VGA 16-Bit Decode (V16) –** R/W. 0 = VGA range is enabled. 1 = The I/O aliases of the VGA range (see BCTRL:VE definition below), are not enabled, and only the base I/O ranges can be decoded
3	**VGA Enable (VE)** – R/W. 0 = The ranges below will not be claimed off the backbone by the root port. 1 = The following ranges will be claimed off the backbone by the root port: • Memory ranges A0000h-BFFFFh • I/O ranges 3B0h – 3BBh and 3C0h – 3DFh, and all aliases of bits 15:10 in any combination of 1's

Bit	Description
2	**ISA Enable (IE)** – R/W. This bit only applies to I/O addresses that are enabled by the I/O Base and I/O Limit registers and are in the first 64KB of PCI I/O space. 0 = The root port will not block any forwarding from the backbone as described below. 1 = The root port will block any forwarding from the backbone to the device of I/O transactions addressing the last 768 bytes in each 1KB block (offsets 100h to 3FFh).
1	**SERR# Enable (SE)** – R/W. 0 = The messages described below are not forwarded to the backbone. 1 = ERR_COR, ERR_NONFATAL, and ERR_FATAL messages received are forwarded to the backbone.
0	**Parity Error Response Enable (PERE)** – R/W. When set, 0 = Poisoned write TLPs and completions indicating poisoned TLPs will not set the SSTS.DPD (D28:F0/F1/F2/F3:1E, bit 8). 1 = Poisoned write TLPs and completions indicating poisoned TLPs will set the SSTS.DPD (D28:F0/F1/F2/F3:1E, bit 8).

15.1.22 CLIST – Capabilities List Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 40–41h
Default Value: 8010h
Attribute: RO
Size: 16 bits

Bit	Description
15:8	**Next Capability (NEXT) –** RO. Value of 80h indicates the location of the next pointer.
7:0	**Capability ID (CID) –** RO. Indicates this is a PCI Express capability.

15.1.23 XCAP – PCI Express Capabilities Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 42–43h
Default Value: 0041h
Attribute: R/WO, RO
Size: 16 bits

Bit	Description
15:14	Reserved
13:9	**Interrupt Message Number (IMN)** – RO. The Intel® 631xESB/632xESB I/O Controller Hub does not have multiple MSI interrupt numbers.
8	**Slot Implemented (SI) –** R/WO. Indicates whether the root port is connected to a slot. Slot support is platform specific. BIOS programs this field, and it is maintained until a platform reset.
7:4	**Device / Port Type (DT)** – RO. Indicates this is a PCI Express root port.
3:0	**Capability Version (CV)** – RO. Indicates PCI Express 1.0.

15.1.24 DCAP – Device Capabilities Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 44–47h
Default Value: 00000FE0h
Attribute: RO
Size: 32 bits

Bit	Description
31:28	Reserved
27:26	**Captured Slot Power Limit Scale (CSPS)** – RO. Not supported.
25:18	**Captured Slot Power Limit Value (CSPV) –** RO. Not supported.
17:15	Reserved
14	**Power Indicator Present (PIP)** – RO. Indicates no power indicator is present on the root port.

Bit	Description
13	**Attention Indicator Present (AIP)** – RO. Indicates no attention indicator is present on the root port.
12	**Attention Button Present (ABP)** – RO. Indicates no attention button is present on the root port.
11:9	**Endpoint L1 Acceptable Latency (E1AL)** – RO. Indicates more than 4 µs. This field essentially has no meaning for root ports since root ports are not endpoints.
8:6	**Endpoint L0 Acceptable Latency (E0AL)** – RO. Indicates more than 64 µs. This field essentially has no meaning for root ports since root ports are not endpoints.
5	**Extended Tag Field Supported (ETFS)** – RO. Indicates that 8-bit tag fields are supported.
4:3	**Phantom Functions Supported (PFS)** – RO. No phantom functions supported.
2:0	**Max Payload Size Supported (MPS)** – RO. Indicates the maximum payload size supported is 128B.

15.1.25 DCTL – Device Control Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 48–49h
Default Value: 0000h
Attribute: R/W, RO
Size: 16 bits

Bit	Description
15	Reserved
14:12	Max Read Request Size (MRRS) – RO. Hardwired to 0.
11	**Enable No Snoop (ENS) –** RO. Not supported. The root port will never issue non-snoop requests.
10	**Aux Power PM Enable (APME)** – R/W. The OS will set this bit to 1 if the device connected has detected aux power. It has no effect on the root port otherwise.
9	**Phantom Functions Enable (PFE)** – RO. Not supported.
8	**Extended Tag Field Enable (ETFE)** – RO. Not supported.
7:5	**Max Payload Size (MPS)** – R/W. The root port only supports 128B payloads, regardless of the programming of this field.
4	**Enable Relaxed Ordering (ERO)** – RO. Not supported.
3	**Unsupported Request Reporting Enable (URE)** – R/W. 0 = The root port will ignore unsupported request errors. 1 = The root port will generate errors when detecting an unsupported request.
2	**Fatal Error Reporting Enable (FEE)** – R/W. 0 = The root port will ignore fatal errors. 1 = The root port will generate errors when detecting a fatal error.
1	**Non-Fatal Error Reporting Enable (NFE)** – R/W. 0 = The root port will ignore non-fatal errors. 1 = The root port will generate errors when detecting a non-fatal error.
0	**Correctable Error Reporting Enable (CEE)** – R/W. 0 = The root port will ignore correctable errors. 1 = The root port will generate errors when detecting a correctable error.

15.1.26 DSTS – Device Status Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 4A–4Bh
Default Value: 0010h
Attribute: R/WC, RO
Size: 16 bits

Bit	Description
15:6	Reserved
5	**Transactions Pending (TDP)** – RO. This bit has no meaning for the root port since only one transaction may be pending to the Intel® 631xESB/632xESB I/O Controller Hub, so a read of this bit cannot occur until it has already returned to 0.
4	**AUX Power Detected (APD) –** RO. The root port contains AUX power for wakeup.
3	**Unsupported Request Detected (URD)** – R/WC. Indicates an unsupported request was detected.
2	**Fatal Error Detected (FED)** – R/WC. Indicates a fatal error was detected. 0 = Fatal has not occurred. 1 = A fatal error occurred from a data link protocol error, link training error, buffer overflow, or malformed TLP.
1	**Non-Fatal Error Detected (NFED)** – R/WC. Indicates a non-fatal error was detected. 0 = Non-fatal has not occurred. 1 = A non-fatal error occurred from a poisoned TLP, unexpected completions, unsupported requests, completer abort, or completer timeout.
0	**Correctable Error Detected (CED)** – R/WC. Indicates a correctable error was detected. 0 = Correctable has not occurred. 1 = The port received an internal correctable error from receiver errors / framing errors, TLP CRC error, DLLP CRC error, replay num rollover, replay timeout.

15.1.27 LCAP – Link Capabilities Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 4C–4Fh
Default Value: See bit description
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31:24	**Port Number (PN)** – RO. Indicates the port number for the root port. This value is different for each implemented port: Function # / Port # / Value of PN field D28:F0 / 1 / 01h D28:F1 / 2 / 02h D28:F2 / 3 / 03h D28:F3 / 4 / 04h
23:18	Reserved
17:15	**L1 Exit Latency (EL1) –** RO. Set to 010b to indicate an exit latency of 2 µs to 4 µs.
14:12	**L0s Exit Latency (EL0)** – RO. Indicates as exit latency based upon common-clock configuration. LCLT.CCC / Value of EL0 (these bits) 0 / MPC.UCEL (D28:F0/F1/F2/F3:D8h:bits20:18) 1 / MPC.CCEL (D28:F0/F1/F2/F3:D8h:bits17:15) ***Note:*** LCLT.CCC is at D28:F0/F1/F2/F3:50h:bit 6

Bit	Description
11:10	**Active State Link PM Support (APMS)** – R/O. Indicates what level of active state link power management is supported on the root port. Bits — Definition 00 — Neither L0s nor L1 are supported 01 — L0s Entry Supported 10 — L1 Entry Supported 11 — Both L0s and L1 Entry Supported
9:4	**Maximum Link Width (MLW)** – RO. For the root ports, several values can be taken, based upon the value of the chipset config register field RPC.PC (Chipset Config Registers:Offset 0224h:bits1:0): Value of MLW field Port # — RPC.PC=00b — RPC.PC=01bPRC.PC=11b 1 — 01h — 02h04h 2 — 01h — 01h01h 3 — 01h — 01h01h 4 — 01h — 01h01h
3:0	**Maximum Link Speed (MLS)** – RO. Set to 1h to indicate the link speed is 2.5 Gb/s.

15.1.28 LCTL – Link Control Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 50–51h
Default Value: 0000h
Attribute: R/W, R/W (special), RO
Size: 16 bits

Bit	Description
15:8	Reserved
7	**Extended Synch (ES)** – R/W. 0 = Extended synch disabled. 1 = Forces extended transmission of FTS ordered sets in FTS and extra TS2 at exit from L1 prior to entering L0.
6	**Common Clock Configuration (CCC) –** R/W. 0 = The Intel® 631xESB/632xESB I/O Controller Hub and device are not using a common reference clock. 1 = The Intel® 631xESB/632xESB I/O Controller Hub and device are operating with a distributed common reference clock.
5	**Retrain Link (RL)** – RO/W. 0 = This bit always returns 0 when read. 1 = The root port will train its downstream link. ***Note:*** Software uses LSTS.LT (D28:F0/F1/F2/F3:52, bit 11) and LSTS.LTE (D28:F0/F1/F2/F3:52, bit 10) to check the status of training.
4	**Link Disable (LD)** – R/W. 0 = Link enabled. 1 = The root port will disable the link.
3	**Read Completion Boundary Control (RCBC)** – RO. Indicates the read completion boundary is 64 bytes.
2	Reserved
1:0	**Active State Link PM Control (APMC)** – R/W. Indicates whether the root port should enter L0s or L1 or both. Bits — Definition 00 — Disabled 01 — L0s Entry is Enabled 10 — L1 Entry is Enabled 11 — L0s and L1 Entry Enabled

15.1.29 LSTS – Link Status Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 52–53h
Default Value: See bit description
Attribute: RO
Size: 16 bits

Bit	Description
15:13	Reserved
12	**Slot Clock Configuration (SCC)** – RO. Set to 1b to indicate that the Intel® 631xESB/632xESB I/O Controller Hub uses the same reference clock as on the platform and does not generate its own clock.
11	**Link Training (LT) –** RO. Default value is 0b. 0 = Link training completed. 1 = Link training is occurring.
10	Link Training Error (LTE**)** – RO. Not supported. Set value is 0b.
9:4	**Negotiated Link Width (NLW)** – RO. This field indicates the negotiated width of the given PCI Express Link. Port # — Possible Values 1 — 000000b, 000001b, 000100b,001000b 2 — 000000b, 000001b, 000100b 3 — 000001b 4 — 000000b, 000001b, 000100b,001000b ***Note:*** 000000b =link failure, 000001b = x1 link width, 0000100 = x4 link width, 0001000 = x8 link width
3:0	**Link Speed (LS)** – RO. This field indicates the negotiated Link speed of the given PCI Express Link. 01h = Link is 2.5 Gb/s.

15.1.30 SLCAP – Slot Capabilities Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 54–57h
Default Value: 00000060h
Attribute: R/WO, RO
Size: 32 bits

Bit	Description
31:19	**Physical Slot Number (PSN)** – R/WO. This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset.
18:17	Reserved
16:15	**Slot Power Limit Scale (SLS) –** R/WO. Specifies the scale used for the slot power limit value. BIOS sets this field and it remains set until a platform reset.
14:7	**Slot Power Limit Value (SLV)** – R/WO. Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset.
6	**Hot-Plug Capable (HPC)** – RO. 1b = Indicates that Hot-Plug is supported.
5	**Hot-Plug Surprise (HPS)** – RO. 1b = Indicates the device may be removed from the slot without prior notification.
4	**Power Indicator Present (PIP)** – RO. 0b = Indicates that a power indicator LED is not present for this slot.
3	**Attention Indicator Present (AIP)** – RO. 0b = Indicates that an attention indicator LED is not present for this slot.

Bit	Description
2	**MRL Sensor Present (MSP)** – RO. 0b = Indicates that an MRL sensor is not present.
1	**Power Controller Present (PCP)** – RO. 0b = Indicates that a power controller is not implemented for this slot.
0	**Attention Button Present (ABP)** – RO. 0b = Indicates that an attention button is not implemented for this slot.

15.1.31 SLCTL – Slot Control Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 58–59h
Default Value: 0000h
Attribute: R/W, RO
Size: 16 bits

Bit	Description
15:11	Reserved
10	**Power Controller Control (PCC) –** RO.This bit has no meaning for module based Hot-Plug.
9:8	**Power Indicator Control (PIC) –** R/W. When read, the current state of the power indicator is returned. When written, the appropriate POWER_INDICATOR_* messages are sent. Defined encodings are: Bits Definition 11 Off 10 Blink 01 On 00 Reserved
7:6	**Attention Indicator Control (AIC)** – R/W. When read, the current state of the attention indicator is returned. When written, the appropriate ATTENTION_INDICATOR_* messages are sent. Defined encodings are: Bits Definition 11 Off 10 Blink 01 On 00 Reserved
5	**Hot-Plug Interrupt Enable (HPE)** – R/W. 0 = Hot-Plug interrupts based on Hot-Plug events is disabled. 1 = Enables generation of a Hot-Plug interrupt on enabled Hot-Plug events.
4	**Command Completed Interrupt Enable (CCE)** – R/W. 0 = Hot-Plug interrupts based on command completions is disabled. 1 = Enables the generation of a Hot-Plug interrupt when a command is completed by the Hot-Plug controller.
3	**Presence Detect Changed Enable (PDE)** – R/W. 0 = Hot-Plug interrupts based on presence detect logic changes is disabled. 1 = Enables the generation of a Hot-Plug interrupt or wake message when the presence detect logic changes state.
2	**MRL Sensor Changed Enable (MSE)** – R/W. MSE not supported.
1	**Power Fault Detected Enable (PFE)** – R/W. PFE not supported.
0	**Attention Button Pressed Enable (ABE)** – R/W. When set, enables the generation of a Hot-Plug interrupt when the attention button is pressed. 0 = Hot-Plug interrupts based on the attention button being pressed is disabled. 1 = Enables the generation of a Hot-Plug interrupt when the attention button is pressed.

15.1.32 SLSTS – Slot Status Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 5A–5Bh
Default Value: 0000h
Attribute: R/WC, RO
Size: 16 bits

Bit	Description
15:7	Reserved
6	**Presence Detect State (PDS)** – RO. If XCAP.SI (D28:F0/F1/F2/F3:42h:bit 8) is set (indicating that this root port spawns a slot), then this bit: 0 = Indicates the slot is empty. 1 = Indicates the slot has a device connected. Otherwise, if XCAP.SI is cleared, this bit is always set (1).
5	MRL Sensor State (MS) – Reserved as the MRL sensor is not implemented.
4	**Command Completed (CC)** – R/WC. 0 = Issued command not completed. 1 = The Hot-Plug controller completed an issued command.
3	**Presence Detect Changed (PDC)** – R/WC. 0 = No change in the PDS bit. 1 = The PDS bit changed states.
2	MRL Sensor Changed (MSC) – Reserved as the MRL sensor is not implemented.
1	Power Fault Detected (PFD) – Reserved as a power controller is not implemented.
0	**Attention Button Pressed (ABP)** – R/WC. 1 = The attention button has not been pressed. 1 = The attention button is pressed.

15.1.33 RCTL – Root Control Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 5C–5Dh
Default Value: 0000h
Attribute: R/W
Size: 16 bits

Bit	Description
15:4	Reserved
3	**PME Interrupt Enable (PIE)** – R/W. 0 = Interrupt generation disabled. 1 = Interrupt generation enabled when RSTS.IS (D28:F0/F1/F2/F3:06, bit 3) is in a set state (either due to a 0 to 1 transition, or due to this bit being set with RSTS.IS already set).
2	**System Error on Fatal Error Enable (SFE) –** R/W. 0 = An SERR# will not be generated. 1 = An SERR# will be generated, assuming CMD.SEE (D28:F0/F1/F2/F3:04, bit 8) is set, if a fatal error is reported by any of the devices in the hierarchy of this root port, including fatal errors in this root port.
1	**System Error on Non-Fatal Error Enable (SNE)** – R/W. 0 = An SERR# will not be generated. 1 = An SERR# will be generated, assuming CMD.SEE (D28:F0/F1/F2/F3:04, bit 8) is set, if a non-fatal error is reported by any of the devices in the hierarchy of this root port, including non-fatal errors in this root port.
0	**System Error on Correctable Error Enable (SCE)** – R/W. 0 = An SERR# will not be generated. 1 = An SERR# will be generated, assuming CMD.SEE (D28:F0/F1/F2/F3:04, bit 8) if a correctable error is reported by any of the devices in the hierarchy of this root port, including correctable errors in this root port.

15.1.34 RSTS – Root Status Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 60–63h
Default Value: 00000000h
Attribute: R/WC, RO
Size: 32 bits

Bit	Description
31:18	Reserved
17	**PME Pending (PP)** – RO. 0 = When the original PME is cleared by software, it will be set again, the requestor ID will be updated, and this bit will be cleared. 1 = Indicates another PME is pending when the PME status bit is set.
16	**PME Status (PS) –** R/WC. 0 = PME was not asserted. 1 = Indicates that PME was asserted by the requestor ID in RID. Subsequent PMEs are kept pending until this bit is cleared.
15:0	**PME Requestor ID (RID)** – RO. Indicates the PCI requestor ID of the last PME requestor. Valid only when PS is set.

15.1.35 MID – Message Signaled Interrupt Identifiers Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 80–81h
Default Value: 9005h
Attribute: RO
Size: 16 bits

Bit	Description
15:8	**Next Pointer (NEXT)** – RO. Indicates the location of the next pointer in the list.
7:0	**Capability ID (CID) –** RO. Capabilities ID indicates MSI.

15.1.36 MC – Message Signaled Interrupt Message Control Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 82–83h
Default Value: 0000h
Attribute: R/W, RO
Size: 16 bits

Bit	Description
15:8	Reserved
7	**64 Bit Address Capable (C64) –** RO. Capable of generating a 32-bit message only.
6:4	**Multiple Message Enable (MME) –** R/W. These bits are R/W for software compatibility, but only one message is ever sent by the root port.
3:1	**Multiple Message Capable (MMC) –** RO. Only one message is required.
0	**MSI Enable (MSIE) –** R/W. 0 = MSI is disabled. 1 = MSI is enabled and traditional interrupt pins are not used to generate interrupts. ***Note:*** CMD.BME (D28:F0/F1/F2/F3:04h:bit 2) must be set for an MSI to be generated. If CMD.BME is cleared, and this bit is set, no interrupts (not even pin based) are generated.

15.1.37 MA – Message Signaled Interrupt Message Address Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 84–87h
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

Bit	Description
31:2	**Address (ADDR)** – R/W. Lower 32 bits of the system specified message address, always DW aligned.
1:0	Reserved

15.1.38 MD – Message Signaled Interrupt Message Data Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 88–89h
Default Value: 0000h
Attribute: R/W
Size: 16 bits

Bit	Description
15:0	**Data (DATA)** – R/W. This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD[15:0]) during the data phase of the MSI memory write transaction.

15.1.39 SVCAP – Subsystem Vendor Capability Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 90–91h
Default Value: AOODh
Attribute: RO
Size: 16 bits

Bit	Description
15:8	**Next Capability (NEXT)** – RO. Indicates the location of the next pointer in the list.
7:0	**Capability Identifier (CID)** – RO. Value of 0Dh indicates this is a PCI bridge subsystem vendor capability.

15.1.40 SVID – Subsystem Vendor Identification Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 94–97h
Default Value: 00000000h
Attribute: R/WO
Size: 32 bits

Bit	Description
31:16	**Subsystem Identifier (SID)** – R/WO. Indicates the subsystem as identified by the vendor. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).
15:0	**Subsystem Vendor Identifier (SVID)** – R/WO. Indicates the manufacturer of the subsystem. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).

15.1.41 PMCAP – Power Management Capability Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: A0–A1h
Default Value: 0001h
Attribute: RO
Size: 16 bits

Bit	Description
15:8	**Next Capability (NEXT)** – RO. Indicates this is the last item in the list.
7:0	**Capability Identifier (CID)** – RO. Value of 01h indicates this is a PCI power management capability.

15.1.42 PMC – PCI Power Management Capabilities Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: A2–A3h
Default Value: C802h
Attribute: RO
Size: 16 bits

Bit	Description
15:11	**PME_Support (PMES) –** RO. Indicates PME# is supported for states D0, $D3_{HOT}$ and $D3_{COLD}$. The root port does not generate PME#, but reporting that it does is necessary for some legacy operating systems to enable PME# in devices connected behind this root port.
10	**D2_Support (D2S) –** RO. The D2 state is not supported.
9	**D1_Support (D1S) –** RO The D1 state is not supported.
8:6	**AuX_Current (AC) –** RO. Reports 375 mA maximum suspend well current required when in the $D3_{COLD}$ state.
5	**Device Specific Initialization (DSI) –** RO. Indicates that no device-specific initialization is required.
4	Reserved
3	**PME Clock (PMEC) –** RO. Indicates that PCI clock is not required to generate PME#.
2:0	**Version (VS) –** RO. Indicates support for Revision 1.1 of the PCI Power Management Specification.

15.1.43 PMCS – PCI Power Management Control and Status Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: A4–A7h
Default Value: 00000000h
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31:24	Reserved
23	Bus Power / Clock Control Enable (BPCE) – Reserved per PCI Express specification.
22	B2/B3 Support (B23S) – Reserved per PCI Express specification.
21:16	Reserved
15	**PME Status (PMES) –** RO. Indicates a PME was received on the downstream link.
14:9	Reserved

Bit	Description
8	**PME Enable (PMEE) –** R/W. Indicates PME is enabled. The root port takes no action on this bit, but it must be R/W for some legacy operating systems to enable PME# on devices connected to this root port.
7:2	Reserved
1:0	**Power State (PS) –** RO. This field is used both to determine the current power state of the SATA controller and to set a new power state. The values are: • 00 – D0 state • 11 – $D3_{HOT}$ state ***Note:*** When in the $D3_{HOT}$ state, the controller's configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked. If software attempts to write a '10' or '01' to these bits, the write will be ignored.

15.1.44 MPC – Miscellaneous Port Configuration Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: D8–DBh
Default Value: 00110000h
Attribute: R/W
Size: 32 bits

Bit	Description
31	**Power Management SCI Enable (PMCE) –** R/W. 0 = SCI generation based on a power management event is disabled. 1 = Enables the root port to generate SCI whenever a power management event is detected.
30	**Hot-Plug SCI Enable (HPCE)** – R/W. 0 = SCI generation based on a Hot-Plug event is disabled. 1 = Enables the root port to generate SCI whenever a Hot-Plug event is detected.
29:21	Reserved
20:18	**Unique Clock Exit Latency (UCEL) –** R/W. This value represents the L0s Exit Latency for unique-clock configurations (LCTL.CCC = 0) (D28:F0/F1/F2/F3:Offset 50h:bit 6). It defaults to 512 ns to less than 1 µs, but may be overridden by BIOS.
17:15	**Common Clock Exit Latency (CCEL) –** R/W. This value represents the L0s Exit Latency for common-clock configurations (LCTL.CCC = 1) (D28:F0/F1/F2/F3:Offset 50h:bit 6). It defaults to 128 ns to less than 256 ns, but may be overridden by BIOS.
14:8	Reserved
7	**Port I/OxApic Enable (PAE) –** R/W. 0 = Hole is disabled. 1 = A range is opened through the bridge for the following memory addresses: Port # Address 1 FEC1_0000h – FEC1_7FFFh 2 FEC1_8000h – FEC1_FFFFh 3 FEC2_0000h – FEC2_7FFFh 4 FEC2_8000h – FEC2_FFFFh
6:2	Reserved
1	**Hot-Plug SMI Enable (HPME) –** R/W. 0 = SMI generation based on a Hot-Plug event is disabled. 1 = Enables the root port to generate SMI whenever a Hot-Plug event is detected.
0	**Power Management SMI Enable (PMME) –** R/W. 0 = SMI generation based on a power management event is disabled. 1 = Enables the root port to generate SMI whenever a power management event is detected.

15.1.45 SMSCS – SMI/SCI Status Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: DC–DFh
Default Value: 00000000h
Attribute: R/WC
Size: 32 bits

Bit	Description
31	**Power Management SCI Status (PMCS) –** R/WC. This bit is set if the Hot-Plug controller needs to generate an interrupt, and this interrupt has been routed to generate an SCI.
30	**Hot-Plug SCI Status (HPCS)** – R/WC. This bit is set if the Hot-Plug controller needs to generate an interrupt, and has this interrupt been routed to generate an SCI.
29:4	Reserved
3	**Hot-Plug Command Completed SMI Status (HPCCM)** – R/WC. This bit is set when SLSTS.CC (D28:F0/F1/F2/F3:5A, bit 4) transitions from 0 to 1, and MPC.HPME (D28:F0/F1/F2/F3:D8, bit 1) is set. When this bit is set, an SMI# will be generated.
2	**Hot-Plug Attention Button SMI Status (HPABM)** – R/WC. This bit is set when SLSTS.ABP (D28:F0/F1/F2/F3:5A, bit 0) transitions from 0 to 1, and MPC.HPME (D28:F0/F1/F2/F3:D8, bit 1) is set. When this bit is set, an SMI# will be generated.
1	**Hot-Plug Presence Detect SMI Status (HPPDM)** – R/WC. This bit is set when SLSTS.PDC (D28:F0/F1/F2/F3:5A, bit 3) transitions from 0 to 1, and MPC.HPME (D28:F0/F1/F2/F3:D8, bit 1) is set. When this bit is set, an SMI# will be generated.
0	**Power Management SMI Status (PMMS)** – R/WC. This bit is set when RSTS.PS (D28:F0/F1/F2/F3:60, bit 16) transitions from 0 to', and MPC.PMME (D28:F0/F1/F2/F3:D8, bit 1) is set.

15.1.46 RWC – Resume Well Control Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: E0h
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:1	Reserved
0	**Beacon Enable (BE)** – R/W. 0 = Resuming from a beacon is disabled. 1 = Enables receiving beacon signaling and resuming the port (more power will be consumed when in S3).

15.1.47 VCH – Virtual Channel Capability Header Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 100–103h
Default Value: 18010002h
Attribute: RO
Size: 32 bits

Bit	Description
31:20	**Next Capability Offset (NCO) –** RO. Indicates the next item in the list.
19:16	**Capability Version (CV)** – RO. Indicates this is version 1 of the capability structure by the PCI SIG.
15:0	**Capability ID (CID)** – RO. Indicates this is the Virtual Channel capability item.

15.1.48 VCAP1 – Virtual Channel Capability 1 Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 104–107h
Default Value: 00000001h
Attribute: RO
Size: 32 bits

Bit	Description
31:12	Reserved
11:10	**Port Arbitration Table Entry Size (PATS)** – RO. Must be set to 00 for root ports are per PCI Express specification.
9:8	**Reference Clock (RC)** – RO. Fixed at 100ns for this version of the PCI Express specification.
7	Reserved.
6:4	**Low Priority Extended VC Count (LPEVC)** – RO. Indicates that there are no additional VCs of low priority with extended capabilities.
3	Reserved.
2:0	**Extended VC Count (EVC)** – RO. When FFPCI Express2 is cleared, this field is '001', to indicate that there is one additional VC (VC1) that exists with extended capabilities. When FPCI Express2 is set, this field is '000' to indicate that there are no additional VCs with extended capabilities.

15.1.49 VCAP2 – Virtual Channel Capability 2 Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 108–10Bh
Default Value: 00000001h
Attribute: RO
Size: 32 bits

Bit	Description
31:24	**VC Arbitration Table Offset (ATO)** – RO. Indicates that no table is present for VC arbitration since it is fixed.
23:8	Reserved.
7:0	**VC Arbitration Capability (AC)** – RO. Indicates that the VC arbitration is fixed in the root port. VC1 is highest priority, and VC0 is lowest priority.

15.1.50 PVC – Port Virtual Channel Control Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 10C–10Dh
Default Value: 0000h
Attribute: R/W, RO
Size: 16 bits

Bit	Description
15:4	Reserved.
3:1	**VC Arbitration Select (AS)** – R/W. Indicates which VC should be programmed in the VC arbitration table. The root port takes no action on the setting of this field since there is no arbitration table.
0	**Load VC Arbitration Table (LAT) –** RO. Indicates that the table programmed should be loaded into the VC arbitration table. This bit is defined as read/write with always returning 0 on reads. Since there is no VC arbitration table in the root port, this bit can be built as RO.

15.1.51 PVS – Port Virtual Channel Status Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 10E–10Fh
Default Value: 0000h
Attribute: RO
Size: 16 bits

Bit	Description
15:1	Reserved.
0	**VC Arbitration Table Status (VAS)** – RO. Indicates the coherency status of the VC Arbitration table when it is being updated. This field is always 0 in the root port since there is no VC arbitration table.

15.1.52 V0CAP – Virtual Channel 0 Resource Capability Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 110–113h
Default Value: 00000001h
Attribute: RO
Size: 32 bits

Bit	Description
31:24	**Port Arbitration Table Offset (AT)** – RO. This VC implements no port arbitration table since the arbitration is fixed.
23	Reserved.
22:16	**Maximum Time Slots (MTS)** – RO. This VC implements fixed arbitration, and therefore this field is not used.
15	**Reject Snoop Transactions (RTS)** – RO. This VC must be able to take snoopable transactions.
14	**Advanced Packet Switching (APS)** – RO. This VC is capable of all transactions, not just advanced packet switching transactions.
13:8	Reserved.
7:0	**Port Arbitration Capability (PAC)** – RO. Indicates that this VC uses fixed port arbitration.

15.1.53 V0CTL – Virtual Channel 0 Resource Control Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 114–117h
Default Value: 800000FFh
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31	**Virtual Channel Enable (EN)** – RO. 0 = Virtual Channel 0 cannot be disabled. 1 = Enables the VC.
30:27	Reserved.
26:24	**Virtual Channel Identifier (VCID)** – RO. Indicates the ID to use for this virtual channel.
23:20	Reserved.
19:17	**Port Arbitration Select (PAS)** – R/W. Indicates which port table is being programmed. The root complex takes no action on this setting since the arbitration is fixed and there is no arbitration table.
16	**Load Port Arbitration Table (LAT)** – RO. The root port does not implement an arbitration table for this virtual channel.

Bit	Description
15:8	Reserved.
7:1	**Transaction Class / Virtual Channel Map (TVM)** – R/W. Indicates which transaction classes are mapped to this virtual channel. When a bit is set, this transaction class is mapped to the virtual channel. Bit Transaction Class 7 Transaction Class 7 6 Transaction Class 6 5 Transaction Class 5 4 Transaction Class 4 3 Transaction Class 3 2 Transaction Class 2 1 Transaction Class 1
0	Reserved. Transaction class 0 must always mapped to VC0.

15.1.54 V0STS – Virtual Channel 0 Resource Status Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 11A–11Bh
Default Value: 0000h
Attribute: RO
Size: 16 bits

Bit	Description
15:2	Reserved.
1	**VC Negotiation Pending (NP)** – RO. 0 = Negotiation is not pending. 1 = Indicates the Virtual Channel is still being negotiated with ingress ports.
0	Port Arbitration Tables Status (ATS). There is no port arbitration table for this VC, so this bit is reserved as 0.

15.1.55 V1CAP – Virtual Channel 1 Resource Capability Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 11C–11Fh
Default Value: 00000001h
Attribute: RO
Size: 32 bits

Bit	Description
31:24	**Port Arbitration Table Offset (AT)** – RO. This VC implements no port arbitration table since the arbitration is fixed.
23	Reserved.
22:16	**Maximum Time Slots (MTS)** – RO. This VC implements fixed arbitration, and therefore this field is not used.
15	**Reject Snoop Transactions (RTS)** – RO. This VC must be able to take snoopable transactions.
14	**Advanced Packet Switching (APS)** – RO. This VC is capable of all transactions, not just advanced packet switching transactions.
13:8	Reserved.
7:0	**Port Arbitration Capability (PAC)** – RO. Indicates that this VC uses fixed port arbitration.

15.1.56 V1CTL – Virtual Channel 1 Resource Control Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 120–123h
Default Value: 00000000h
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31	**Virtual Channel Enable (EN)** – RW. 0 = Disable the VC. 1 = Enables the VC.
30:27	Reserved.
26:24	**Virtual Channel Identifier (VCID)** – RW. Indicates the ID to use for this virtual channel.
23:20	Reserved.
19:17	**Port Arbitration Select (PAS)** – R/W. Indicates which port table is being programmed. The root complex takes no action on this setting since the arbitration is fixed and there is no arbitration table.
16	**Load Port Arbitration Table (LAT)** – RO. The root port does not implement an arbitration table for this virtual channel.
15:8	Reserved.
7:1	**Transaction Class / Virtual Channel Map (TVM)** – R/W. Indicates which transaction classes are mapped to this virtual channel. When a bit is set, this transaction class is mapped to the virtual channel. Bit Transaction Class 7 Transaction Class 7 6 Transaction Class 6 5 Transaction Class 5 4 Transaction Class 4 3 Transaction Class 3 2 Transaction Class 2 1 Transaction Class 1
0	Reserved. Transaction class 0 cannot be mapped to VC1.

15.1.57 V1STS – Virtual Channel 1 Resource Status Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 126–127h
Default Value: 00000000h
Attribute: RO
Size: 16 bits

Bit	Description
15:2	Reserved.
1	**VC Negotiation Pending (NP)** – RO. 0 = Negotiation is not pending. 1 = Indicates the Virtual Channel is still being negotiated with ingress ports.
0	**Port Arbitration Tables Status (ATS) –** RO. Indicates the coherency status of the port arbitration table. This bit is set during a table update, and cleared after the table has been updated.

15.1.58 UES – Uncorrectable Error Status Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 144–147h
Default Value: 00000000000x0xxx0x0x0000000x0000b
Attribute: R/WC, RO
Size: 32 bits

This register maintains its state through a platform reset. It loses its state upon suspend.

Bit	Description
31:21	Reserved
20	**Unsupported Request Error Status (URE)** – R/WC. Indicates an unsupported request was received.
19	ECRC Error Status (EE) – RO. ECRC is not supported.
18	**Malformed TLP Status (MT)** – R/WC. Indicates a malformed TLP was received.
17	**Receiver Overflow Status (RO)** – R/WC. Indicates a receiver overflow occurred.
16	**Unexpected Completion Status (UC)** – R/WC. Indicates an unexpected completion was received.
15	**Completion Abort Status (CA)** – R/WC. Indicates a completer abort was received.
14	**Completion Timeout Status (CT)** – R/WC. Indicates a completion timed out.
13	Flow Control Protocol Error Status (FCPE) – RO. Flow Control Protocol Errors not supported.
12	**Poisoned TLP Status (PT)** – R/WC. Indicates a poisoned TLP was received.
11:5	Reserved
4	**Data Link Protocol Error Status (DLPE)** – R/WC. Indicates a data link protocol error occurred.
3:1	Reserved
0	Training Error Status (TE) – RO. Training Errors not supported.

15.1.59 UEM – Uncorrectable Error Mask (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 148–14Bh
Default Value: 00000000h
Attribute: R/WO, RO
Size: 32 bits

When set, the corresponding error in the UES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled.

Bit	Description
31:21	Reserved
20	**Unsupported Request Error Mask (URE)** – R/WO. 0 = The corresponding error in the UES register (D28:F0/F1/F2/F3:144) is enabled. 1 = The corresponding error in the UES register (D28:F0/F1/F2/F3:144) is masked.
19	ECRC Error Mask (EE) – RO. ECRC is not supported.
18	**Malformed TLP Mask (MT)** – R/WO. 0 = The corresponding error in the UES register (D28:F0/F1/F2/F3:144) is enabled. 1 = The corresponding error in the UES register (D28:F0/F1/F2/F3:144) is masked.
17	**Receiver Overflow Mask (RO)** – R/WO. 0 = The corresponding error in the UES register (D28:F0/F1/F2/F3:144) is enabled. 1 = The corresponding error in the UES register (D28:F0/F1/F2/F3:144) is masked.
16	**Unexpected Completion Mask (UC)** – R/WO. 0 = The corresponding error in the UES register (D28:F0/F1/F2/F3:144) is enabled. 1 = The corresponding error in the UES register (D28:F0/F1/F2/F3:144) is masked.
15	Completion Abort Mask (CA) – R/WO. 0 = The corresponding error in the UES register (D28:F0/F1/F2/F3:144) is enabled. 1 = The corresponding error in the UES register (D28:F0/F1/F2/F3:144) is masked.
14	**Completion Timeout Mask (CT)** – R/WO. 0 = The corresponding error in the UES register (D28:F0/F1/F2/F3:144) is enabled. 1 = The corresponding error in the UES register (D28:F0/F1/F2/F3:144) is masked.
13	Flow Control Protocol Error Mask (FCPE) – RO. Flow Control Protocol Errors not supported.

Bit	Description
12	**Poisoned TLP Mask (PT)** – R/WO. 0 = The corresponding error in the UES register (D28:F0/F1/F2/F3:144) is enabled. 1 = The corresponding error in the UES register (D28:F0/F1/F2/F3:144) is masked.
11:5	Reserved
4	**Data Link Protocol Error Mask (DLPE)** – R/WO. 0 = The corresponding error in the UES register (D28:F0/F1/F2/F3:144) is enabled. 1 = The corresponding error in the UES register (D28:F0/F1/F2/F3:144) is masked.
3:1	Reserved
0	Training Error Mask (TE) – RO. Training Errors not supported

15.1.60 UEV – Uncorrectable Error Severity (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 14C–14Fh
Default Value: 00060011h
Attribute: RO
Size: 32 bits

Bit	Description
31:21	Reserved
20	**Unsupported Request Error Severity (URE)** – RO. 0 = Error considered non-fatal. (Default) 1 = Error is fatal.
19	ECRC Error Severity (EE) – RO. ECRC is not supported.
18	**Malformed TLP Severity (MT)** – RO. 0 = Error considered non-fatal. 1 = Error is fatal. (Default)
17	**Receiver Overflow Severity (RO)** – RO. 0 = Error considered non-fatal. 1 = Error is fatal. (Default)
16	**Unexpected Completion Severity (UC)** – RO. 0 = Error considered non-fatal. (Default) 1 = Error is fatal.
15	**Completion Abort Severity (CA) –** RO. 0 = Error considered non-fatal. (Default) 1 = Error is fatal.
14	**Completion Timeout Severity (CT)** – RO. 0 = Error considered non-fatal. (Default) 1 = Error is fatal.
13	Flow Control Protocol Error Severity (FCPE) – RO. Flow Control Protocol Errors not supported.
12	**Poisoned TLP Severity (PT)** – RO. 0 = Error considered non-fatal. (Default) 1 = Error is fatal.
11:5	Reserved
4	**Data Link Protocol Error Severity (DLPE)** – RO. 0 = Error considered non-fatal. 1 = Error is fatal. (Default)
3:1	Reserved
0	Training Error Severity (TE) – RO. TE is not supported.

15.1.61 CES – Correctable Error Status Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 150–153h
Default Value: 00000000h
Attribute: R/WC
Size: 32 bits

Bit	Description
31:13	Reserved
12	**Replay Timer Timeout Status (RTT)** – R/WC. Indicates the replay timer timed out.
11:9	Reserved
8	**Replay Number Rollover Status (RNR) –** R/WC. Indicates the replay number rolled over.
7	**Bad DLLP Status (BD)** – R/WC. Indicates a bad DLLP was received.
6	**Bad TLP Status (BT) –** R/WC. Indicates a bad TLP was received.
5:1	Reserved
0	**Receiver Error Status (RE) –** R/WC. Indicates a receiver error occurred.

15.1.62 CEM – Correctable Error Mask Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 154–157h
Default Value: 00000000h
Attribute: R/WO
Size: 32 bits

When set, the corresponding error in the CES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled.

Bit	Description
31:13	Reserved
12	**Replay Timer Timeout Mask (RTT)** – R/WO. Mask for replay timer timeout.
11:9	Reserved
8	**Replay Number Rollover Mask (RNR) –** R/WO. Mask for replay number rollover.
7	**Bad DLLP Mask (BD)** – R/WO. Mask for bad DLLP reception.
6	**Bad TLP Mask (BT) –** R/WO. Mask for bad TLP reception.
5:1	Reserved
0	**Receiver Error Mask (RE) –** R/WO. Mask for receiver errors.

15.1.63 AECC – Advanced Error Capabilities and Control Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 158–15Bh
Default Value: 00000000h
Attribute: RO
Size: 32 bits

Bit	Description
31:9	Reserved
8	ECRC Check Enable (ECE) – RO. ECRC is not supported.
7	ECRC Check Capable (ECC) – RO. ECRC is not supported.
6	ECRC Generation Enable (EGE) – RO. ECRC is not supported.
5	ECRC Generation Capable (EGC) – RO. ECRC is not supported.
4:0	First Error Pointer (FEP) – RO.

15.1.64 RES – Root Error Status Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 170–173h
Default Value: 00000000h
Attribute: R/WC, RO
Size: 32 bits

Bit	Description
31:27	**Advanced Error Interrupt Message Number (AEMN)** – RO. There is only one error interrupt allocated.
26:4	Reserved
3	**Multiple ERR_FATAL/NONFATAL Received (MENR)** – RO. Only one error will be captured.
2	**ERR_FATAL/NONFATAL Received (ENR)** – R/WC. 0 = No error message received. 1 = Either a fatal or a non-fatal error message is received.
1	**Multiple ERR_COR Received (MCR)** – RO. Only one error will be captured.
0	**ERR_COR Received (CR)** – R/WC. 0 = No error message received. 1 = A correctable error message is received.

15.1.65 RCTCL – Root Complex Topology Capability List Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 180–183h
Default Value: 00010005h
Attribute: RO
Size: 32 bits

Bit	Description
31:20	**Next Capability (NEXT)** – RO. Indicates the next item in the list, in this case, end of list.
19:16	**Capability Version (CV)** – RO. Indicates the version of the capability structure.
15:0	**Capability ID (CID) –** RO. Indicates this is a root complex topology capability.

15.1.66 ESD – Element Self Description Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 184–187h
Default Value: See Description
Attribute: RO
Size: 32 bits

Bit	Description
31:24	**Port Number (PN)** – RO. Indicate the ingress port number for the root port. There is a different value per port: Port #Value 1 01h 2 02h 3 03h 4 04h
23:16	**Component ID (CID)** – RO. This field returns the value of the ESD.CID field of the chip configuration section, that is programmed by platform BIOS, since the root port is in the same component as the RCRB.
15:8	**Number of Link Entries (NLE) –** RO. (Default value is 01h) Indicates one link entry (corresponding to the RCRB).
7:4	Reserved.
3:0	**Element Type (ET) –** RO. (Default value is 0h) Indicates that the element type is a root port.

15.1.67 ULD – Upstream Link Description Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 18C–18Fh
Default Value: 00000001h
Attribute: RO
Size: 32 bits

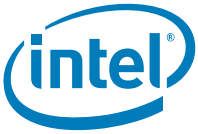
Bit	Description
31:24	**Target Port Number (PN)** – RO. Indicates the port number of the RCRB.
23:16	**Target Component ID (TCID)** – RO. This field returns the value of the ESD.CID field of the chip configuration section, that is programmed by platform BIOS, since the root port is in the same component as the RCRB.
15:2	Reserved.
1	**Link Type (LT) –** RO. Indicates that the link points to the RCRB.
0	**Link Valid (LV) –** RO. Indicates that this link entry is valid.

15.1.68 ULBA – Upstream Link Base Address Register (PCI Express – D28:F0/F1/F2/F3)

Address Offset: 190–197h
Default Value: See Description
Attribute: RO
Size: 64 bits

Bit	Description
63:32	**Base Address Upper (BAU)** – RO. The RCRB of the Intel® 631xESB/632xESB I/O Controller Hub lives in 32-bit space.
31:0	**Base Address Lower (BAL)** – RO. This field matches the RCBA register (D31:F0:Offset F0h) value in the LPC bridge.

§§



16 UHCI Controllers Registers

16.1 PCI Configuration Registers (USB – D29:F0/F1/F2/F3)

Note: Register address locations that are not shown in Table 16-1 and should be treated as Reserved
(see Section 11.1 for details).

Table 16-1. UHCI Controller PCI Register Address Map (USB – D29:F0/F1/F2/F3)

Offset	Mnemonic	Register Name	Function 0 Default	Function 1 Default	Function 2 Default	Function 3 Default	Type
00–01h	VID	Vendor Identification	8086h	8086h	8086h	8086h	RO
02–03h	DID	Device Identification	2658h	2659h	265Ah	265Bh	RO
04–05h	PCICMD	PCI Command	0000h	0000h	0000h	0000h	R/W, RO
06–07h	PCISTS	PCI Status	0280h	0280h	0280h	0280h	R/WC, RO
08h	RID	Revision Identification	See register description.	See register description.	See register description.	See register description.	RO
09h	PI	Programming Interface	00h	00h	00h	00h	RO
0Ah	SCC	Sub Class Code	03h	03h	03h	03h	RO
0Bh	BCC	Base Class Code	0Ch	0Ch	0Ch	0Ch	RO
0Dh	MLT	Master Latency Timer	00h	00h	00h	00h	RO
0Eh	HEADTYP	Header Type	80h	00h	00h	00h	RO
20–23h	Base	Base Address	00000001h	00000001h	00000001h	00000001h	R/W, RO
2C–2Dh	SVID	Subsystem Vendor Identification	0000h	0000h	0000h	0000h	R/WO
2E–2Fh	SID	Subsystem Identification	0000h	0000h	0000h	0000h	R/WO
3Ch	INT_LN	Interrupt Line	00h	00h	00h	00h	R/W
3Dh	INT_PN	Interrupt Pin	See register description.	See register description.	See register description.	See register description.	RO
60h	USB_RELNUM	Serial Bus Release Number	10h	10h	10h	10h	RO
C0–C1h	USB_LEGKEY	USB Legacy Keyboard/ Mouse Control	2000h	2000h	2000h	2000h	R/W, RO R/WC
C4h	USB_RES	USB Resume Enable	00h	00h	00h	00h	R/W
C8h	CWP	Core Well Policy	00h	00h	00h	00h	R/W

Note: Refer to the *Intel® 631xESB/632xESB I/O Controller Hub EDS Specification Update* for the value of the Revision ID Register

16.1.1 VID – Vendor Identification Register (USB – D29:F0/F1/F2/F3)

Address Offset: 00–01h
Default Value: 8086h
Attribute: RO
Size: 16 bits

Bit	Description
15:0	Vendor ID – RO. This is a 16-bit value assigned to Intel

16.1.2 DID – Device Identification Register (USB – D29:F0/F1/F2/F3)

Address Offset: 02–03h
Default Value: UHCI #1 = 2688h
UHCI #2 = 2689h
UHCI #3 = 268Ah
UHCI #4 = 268Bh
Attribute: RO
Size: 16 bits

Bit	Description
15:0	Device ID – RO. This is a 16-bit value assigned to the Intel® 631xESB/632xESB I/O Controller Hub USB host controllers

16.1.3 PCICMD – PCI Command Register (USB – D29:F0/F1/F2/F3)

Address Offset: 04–05h
Default Value: 0000h
Attribute: R/W, RO
Size: 16 bits

Bit	Description
15:11	Reserved
10	**Interrupt Disable –** R/W. 0 = Enable. The function is able to generate its interrupt to the interrupt controller. 1 = Disable. The function is not capable of generating interrupts. ***Note:*** The corresponding Interrupt Status bit is not affected by the interrupt enable.
9	Fast Back to Back Enable (FBE) – RO. Hardwired to 0.
8	SERR# Enable – RO. Reserved as 0.
7	Wait Cycle Control (WCC) – RO. Hardwired to 0.
6	Parity Error Response (PER) – RO. Hardwired to 0.
5	VGA Palette Snoop (VPS) – RO. Hardwired to 0.
4	Postable Memory Write Enable (PMWE) – RO. Hardwired to 0.
3	Special Cycle Enable (SCE) – RO. Hardwired to 0.
2	**Bus Master Enable (BME)** – R/W. 0 = Disable 1 = Enable. Act as a master on the PCI bus for USB transfers.
1	Memory Space Enable (MSE) – RO. Hardwired to 0.
0	**I/O Space Enable (IOSE)** – R/W. This bit controls access to the I/O space registers. 0 = Disable 1 = Enable accesses to the USB I/O registers. The Base Address register for USB should be programmed before this bit is set.

16.1.4 PCISTS – PCI Status Register (USB – D29:F0/F1/F2/F3)

Address Offset:	06–07h	Attribute:	R/WC, RO
Default Value:	0280h	Size:	16 bits

Note: For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 to the bit has no effect.

Bit	Description
15	**DPE – Detected Parity Error (DPE) –** R/WC. 0 = No parity error detected. 1 = Set when a data parity error data parity error is detected on writes to the UHCI register space or on read completions returned to the host controller.
14	Reserved as 0b. Read Only.
13	Received Master Abort (RMA) – R/WC. 0 = No master abort generated by USB. 1 = USB, as a master, generated a master abort.
12	Reserved. Always read as 0.
11	Signaled Target Abort (STA) – R/WC. 0 = Intel® 631xESB/632xESB I/O Controller Hub did Not terminate transaction for USB function with a target abort. 1 = USB function is targeted with a transaction that the Intel® 631xESB/632xESB I/O Controller Hub terminates with a target abort.
10:9	**DEVSEL# Timing Status (DEV_STS) –** RO. This 2-bit field defines the timing for DEVSEL# assertion. These read only bits indicate the Intel® 631xESB/632xESB I/O Controller Hub's DEVSEL# timing when performing a positive decode. Intel® 631xESB/632xESB I/O Controller Hub generates DEVSEL# with medium timing for USB.
8	Data Parity Error Detected (DPED) – RO. Hardwired to 0.
7	Fast Back to Back Capable (FB2BC) – RO. Hardwired to 1.
6	User Definable Features (UDF) – RO. Hardwired to 0.
5	66 MHz Capable – RO. Hardwired to 0.
4	Capabilities List – RO. Hardwired to 0.
3	**Interrupt Status –** RO. This bit reflects the state of this function's interrupt at the input of the enable/disable logic. 0 = Interrupt is deasserted. 1 = Interrupt is asserted. The value reported in this bit is independent of the value in the Interrupt Enable bit.
2:0	Reserved

16.1.5 RID – Revision Identification Register (USB – D29:F0/F1/F2/F3)

Offset Address:	08h	Attribute:	RO
Default Value:	See bit description	Size:	8 bits

Bit	Description
7:0	**Revision ID –** RO. Refer to Table 2-33 or the *Intel® 631xESB/632xESB I/O Controller Hub EDS Specification Update* for the value of the Revision ID Register

16.1.6 PI – Programming Interface Register (USB – D29:F0/F1/F2/F3)

Address Offset: 09h
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	Programming Interface – RO. 00h = No specific register level programming interface defined.

16.1.7 SCC – Sub Class Code Register (USB – D29:F0/F1/F2/F3)

Address Offset: 0Ah
Default Value: 03h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	Sub Class Code (SCC) – RO. 03h = USB host controller.

16.1.8 BCC – Base Class Code Register (USB – D29:F0/F1/F2/F3)

Address Offset: 0Bh
Default Value: 0Ch
Attribute: RO
Size: 8 bits

Bit	Description
7:0	Base Class Code (BCC) – RO. 0Ch = Serial Bus controller.

16.1.9 MLT – Master Latency Timer Register (USB – D29:F0/F1/F2/F3)

Address Offset: 0Dh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	Master Latency Timer (MLT) – RO. The USB controller is implemented internal to the Intel® 631xESB/632xESB I/O Controller Hub and not arbitrated as a PCI device. Therefore the device does not require a Master Latency Timer.

16.1.10 HEADTYP – Header Type Register (USB – D29:F0/F1/F2/F3)

Address Offset: 0Eh
Default Value: FN 0: 80h
FN 1: 00h
FN 2: 00h
FN 3: 00h
Attribute: RO
Size: 8 bits

For functions 1, 2, and 3, this register is hardwired to 00h. For function 0, bit 7 is determined by the values in the USB Function Disable bits (11:8 of the Function Disable register Chipset Config Registers:Offset 3418h).

Bit	Description
7	Multi-Function Device – RO. 0 = Single-function device. 1 = Multi-function device. Since the upper functions in this device can be individually hidden, this bit is based on the function-disable bits in Device 31:F0:F2h as follows: D29:F7_Disable D29:F3_Disable D29:F2_Disable D29:F1_Disable Multi-Function Bit (bit 15) (bit 11) (bit 10) (bit 9) 0 X X X 1 X 0 X X 1 X X 0 X 1 X X X 0 1 1 1 1 1 0
6:0	Configuration Layout. Hardwired to 00h, which indicates the standard PCI configuration layout.

16.1.11 BASE – Base Address Register (USB – D29:F0/F1/F2/F3)

Address Offset: 20–23h
Default Value: 00000001h
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31:16	Reserved
15:5	**Base Address** – R/W. Bits [15:5] correspond to I/O address signals AD [15:5], respectively. This gives 32 bytes of relocatable I/O space.
4:1	Reserved
0	Resource Type Indicator (RTE) – RO. Hardwired to 1 to indicate that the base address field in this register maps to I/O space.

16.1.12 SVID – Subsystem Vendor Identification Register (USB – D29:F0/F1/F2/F3)

Address Offset: 2Ch–2Dh
Default Value: 0000h
Lockable: No
Attribute: R/WO
Size: 16 bits
Power Well: Core

Bit	Description
15:0	Subsystem Vendor ID (SVID) – R/WO. BIOS sets the value in this register to identify the Subsystem Vendor ID. The USB_SVID register, in combination with the USB Subsystem ID register, enables the operating system to distinguish each subsystem from the others. ***Note:*** The software can write to this register only once per core well reset. Writes should be done as a single 16-bit cycle.

16.1.13 SID – Subsystem Identification Register (USB – D29:F0/F1/F2/F3)

Address Offset:	2Eh–2Fh	Attribute:	R/WO
Default Value:	0000h	Size:	16 bits
Lockable:	No	Power Well:	Core

Bit	Description
15:0	**Subsystem ID (SID) –** R/WO. BIOS sets the value in this register to identify the Subsystem ID. The SID register, in combination with the SVID register (D29:F0/F1/F2/F3:2C), enables the operating system to distinguish each subsystem from other(s). The value read in this register is the same as what was written to the IDE_SID register. ***Note:*** The software can write to this register only once per core well reset. Writes should be done as a single 16-bit cycle.

16.1.14 INT_LN – Interrupt Line Register (USB – D29:F0/F1/F2/F3)

Address Offset:	3Ch	Attribute:	R/W
Default Value:	00h	Size:	8 bits

Bit	Description
7:0	**Interrupt Line (INT_LN)** – RO. This data is not used by the Intel® 631xESB/632xESB I/O Controller Hub. It is to communicate to software the interrupt line that the interrupt pin is connected to.

16.1.15 INT_PN – Interrupt Pin Register (USB – D29:F0/F1/F2/F3)

Address Offset:	3Dh	Attribute:	RO
Default Value:	Function 0: See Description Function 1: See Description Function 2: See Description Function 3: See Description	Size:	8 bits

Bit	Description
7:0	**Interrupt Line (INT_LN)** – RO. This value tells the software which interrupt pin each USB host controller uses. The upper 4 bits are hardwired to 0000b; the lower 4 bits are determine by the Interrupt Pin default values that are programmed in the memory-mapped configuration space as follows: Function 0 D29IP.U0P (Chipset Config Registers:Offset 3108:bits 3:0) Function 1 D29IP.U1P (Chipset Config Registers:Offset 3108:bits 7:4) Function 2 D29IP.U2P (Chipset Config Registers:Offset 3108:bits 11:8) Function 3 D29IP.U3P (Chipset Config Registers:Offset 3108:bits 15:12) ***Note:*** This does not determine the mapping to the PIRQ pins.

16.1.16 USB_RELNUM – Serial Bus Release Number Register USB – D29:F0/F1/F2/F3)

Address Offset:	60h	Attribute:	RO
Default Value:	10h	Size:	8 bits

Bit	Description
7:0	Serial Bus Release Number – RO. 10h = USB controller is compliant with the USB Specification, Release 1.0.

16.1.17 USB_LEGKEY – USB Legacy Keyboard/Mouse Control Register (USB – D29:F0/F1/F2/F3)

Address Offset: C0–C1h
Default Value: 2000h
Attribute: R/W, R/WC, RO
Size: 16 bits

This register is implemented separately in each of the USB UHCI functions. However, the enable and status bits for the trapping logic are OR'd and shared, respectively, since their functionality is not specific to any one host controller.

Bit	Description
15	**SMI Caused by End of Pass-Through (SMIBYENDPS) –** R/WC. This bit indicates if the event occurred. Note that even if the corresponding enable bit is not set in bit 7, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. 0 = Software clears this bit by writing a 1 to the bit location in any of the controllers. 1 = Event Occurred
14	Reserved
13	**PCI Interrupt Enable (USBPIRQEN) –** R/W. This bit is used to prevent the USB controller from generating an interrupt due to transactions on its ports. Note that, when disabled, it will probably be configured to generate an SMI using bit 4 of this register. Default to 1 for compatibility with older USB software. 0 = Disable 1 = Enable
12	**SMI Caused by USB Interrupt (SMIBYUSB) –** RO. This bit indicates if an interrupt event occurred from this controller. The interrupt from the controller is taken before the enable in bit 13 has any effect to create this read-only bit. Note that even if the corresponding enable bit is not set in Bit 4, this bit may still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. 0 = Software should clear the interrupts via the USB controllers. Writing a 1 to this bit will have no effect. 1 = Event Occurred.
11	**SMI Caused by Port 64 Write (TRAPBY64W) –** R/WC. This bit indicates if the event occurred. Note that even if the corresponding enable bit is not set in bit 3, this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Note that the A20Gate Pass-Through Logic allows specific port 64h writes to complete without setting this bit. 0 = Software clears this bit by writing a 1 to the bit location in any of the controllers. 1 = Event Occurred.
10	**SMI Caused by Port 64 Read (TRAPBY64R) –** R/WC. This bit indicates if the event occurred. Note that even if the corresponding enable bit is not set in bit 2, this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. 0 = Software clears this bit by writing a 1 to the bit location in any of the controllers. 1 = Event Occurred.
9	**SMI Caused by Port 60 Write (TRAPBY60W) –** R/WC. This bit indicates if the event occurred. Note that even if the corresponding enable bit is not set in bit 1, this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Note that the A20Gate Pass-Through Logic allows specific port 64h writes to complete without setting this bit. 0 = Software clears this bit by writing a 1 to the bit location in any of the controllers. 1 = Event Occurred.
8	**SMI Caused by Port 60 Read (TRAPBY60R) –** R/WC. This bit indicates if the event occurred. Note that even if the corresponding enable bit is not set in the bit 0, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. 0 = Software clears this bit by writing a 1 to the bit location in any of the controllers. 1 = Event Occurred.
7	**SMI at End of Pass-Through Enable (SMIATENDPS) –** R/W. This bit enables SMI at the end of a pass-through. This can occur if an SMI is generated in the middle of a pass-through, and needs to be serviced later. 0 = Disable 1 = Enable
6	Pass Through State (PSTATE) – RO. 0 = If software needs to reset this bit, it should set bit 5 in all of the host controllers to 0. 1 = Indicates that the state machine is in the middle of an A20GATE pass-through sequence.

Bit	Description
5	**A20Gate Pass-Through Enable (A20PASSEN) –** R/W. 0 = Disable. 1 = Enable. Allows A20GATE sequence Pass-Through function. A specific cycle sequence involving writes to port 60h and 64h does not result in the setting of the SMI status bits.
4	**SMI on USB IRQ Enable (USBSMIEN) –** R/W. 0 = Disable 1 = Enable. USB interrupt will cause an SMI event.
3	**SMI on Port 64 Writes Enable (64WEN) –** R/W. 0 = Disable 1 = Enable. A 1 in bit 11 will cause an SMI event.
2	**SMI on Port 64 Reads Enable (64REN) –** R/W. 0 = Disable 1 = Enable. A 1 in bit 10 will cause an SMI event.
1	**SMI on Port 60 Writes Enable (60WEN) –** R/W. 0 = Disable 1 = Enable. A 1 in bit 9 will cause an SMI event.
0	**SMI on Port 60 Reads Enable (60REN) –** R/W. 0 = Disable 1 = Enable. A 1 in bit 8 will cause an SMI event.

16.1.18 USB_RES – USB Resume Enable Register (USB – D29:F0/F1/F2/F3)

Address Offset: C4h Attribute: R/W
Default Value: 00h Size: 8 bits

Bit	Description
7:2	Reserved
1	**PORT1EN** – R/W. Enable port 1 of the USB controller to respond to wakeup events. 0 = The USB controller will not look at this port for a wakeup event. 1 = The USB controller will monitor this port for remote wakeup and connect/disconnect events.
0	**PORT0EN** – R/W. Enable port 0 of the USB controller to respond to wakeup events. 0 = The USB controller will not look at this port for a wakeup event. 1 = The USB controller will monitor this port for remote wakeup and connect/disconnect events.

16.1.19 CWP – Core Well Policy Register (USB – D29:F0/F1/F2/F3)

Address Offset: C8h Attribute: R/W
Default Value: 00h Size: 8 bits

Bit	Description
7:1	Reserved
0	**Static Bus Master Status Policy Enable** (SBMSPE) – R/W. 0 = The UHCI host controller dynamically sets the Bus Master status bit (Power Management 1 Status Register,[PMBASE+00h], bit 4) based on the memory accesses that are scheduled. The default setting provides a more accurate indication of snoopable memory accesses in order to help with software-invoked entry to C3 and C4 power states 1 = The UHCI host controller statically forces the Bus Master Status bit in power management space to 1 whenever the HCHalted bit (USB Status Register, Base+02h, bit 5) is cleared. ***Note:*** The PCI Power Management registers are enabled in the PCI Device 31: Function 0 space (PM_IO_EN), and can be moved to any I/O location (128-byte aligned).

16.2 USB I/O Registers

Some of the read/write register bits that deal with changing the state of the USB hub ports function such that on read back they reflect the current state of the port, and not necessarily the state of the last write to the register. This allows the software to poll the state of the port and wait until it is in the proper state before proceeding. A host controller reset, global reset, or port reset will immediately terminate a transfer on the affected ports and disable the port. This affects the USBCMD register, bit 4 and the PORTSC registers, bits [12,6,2]. See individual bit descriptions for more detail.

Table 16-2. USB I/O Registers

BASE + Offset	Mnemonic	Register Name	Default	Type
00–01	USBCMD	USB Command	0000h	R/W
02–03	USBSTS	USB Status	0020h	R/WC
04–05	USBINTR	USB Interrupt Enable	0000h	R/W
06–07	FRNUM	Frame Number	0000h	R/W (see Note 1)
08–0B	FRBASEADD	Frame List Base Address	Undefined	R/W
0C	SOFMOD	Start of Frame Modify	40h	R/W
0D–0F	–	Reserved	–	–
10–11	PORTSC0	Port 0 Status/Control	0080h	R/WC, RO, R/W (see Note 1)
12–13	PORTSC1	Port 1 Status/Control	0080h	R/WC, RO, R/W (see Note 1)

Note: These registers are WORD writable only. Byte writes to these registers have unpredictable effects.

16.2.1 USBCMD – USB Command Register

I/O Offset: Base + (00–01h) Attribute: R/W
Default Value: 0000h Size: 16 bits

The Command Register indicates the command to be executed by the serial bus host controller. Writing to the register causes a command to be executed. The table following the bit description provides additional information on the operation of the Run/Stop and Debug bits.

Bit	Description
15:7	Reserved
8	**Loop Back Test Mode** – R/W. 0 = Disable loop back test mode. 1 = In loop back test mode. When both ports are connected together, a write to one port will be seen on the other port and the data will be stored in I/O offset 18h.
7	**Max Packet (MAXP)** – R/W. This bit selects the maximum packet size that can be used for full speed bandwidth reclamation at the end of a frame. This value is used by the host controller to determine whether it should initiate another transaction based on the time remaining in the SOF counter. Use of reclamation packets larger than the programmed size will cause a Babble error if executed during the critical window at frame end. The Babble error results in the offending endpoint being stalled. Software is responsible for ensuring that any packet which could be executed under bandwidth reclamation be within this size limit. 0 = 32 bytes 1 = 64 bytes
6	**Configure Flag (CF)** – R/W. This bit has no effect on the hardware. It is provided only as a semaphore service for software. 0 = Indicates that software has not completed host controller configuration. 1 = HCD software sets this bit as the last action in its process of configuring the host controller.

Bit	Description
5	**Software Debug (SWDBG)** – R/W. The SWDBG bit must only be manipulated when the controller is in the stopped state. This can be determined by checking the HCHalted bit in the USBSTS register. 0 = Normal Mode. 1 = Debug mode. In SW Debug mode, the host controller clears the Run/Stop bit after the completion of each USB transaction. The next transaction is executed when software sets the Run/Stop bit back to 1.
4	**Force Global Resume (FGR)** – R/W. 0 = Software resets this bit to 0 after 20 ms has elapsed to stop sending the Global Resume signal. At that time all USB devices should be ready for bus activity. The 1 to 0 transition causes the port to send a low speed EOP signal. This bit will remain a 1 until the EOP has completed. 1 = Host controller sends the Global Resume signal on the USB, and sets this bit to 1 when a resume event (connect, disconnect, or K-state) is detected while in global suspend mode.
3	**Enter Global Suspend Mode (EGSM)** – R/W. 0 = Software resets this bit to 0 to come out of Global Suspend mode. Software writes this bit to 0 at the same time that Force Global Resume (bit 4) is written to 0 or after writing bit 4 to 0. 1 = Host controller enters the Global Suspend mode. No USB transactions occur during this time. The Host controller is able to receive resume signals from USB and interrupt the system. Software must ensure that the Run/Stop bit (bit 0) is cleared prior to setting this bit.
2	**Global Reset (GRESET)** – R/W. 0 = This bit is reset by the software after a minimum of 10 ms has elapsed as specified in Section 7 of the USB Specification. 1 = Global Reset. The host controller sends the global reset signal on the USB and then resets all its logic, including the internal hub registers. The hub registers are reset to their power on state. Chip Hardware Reset has the same effect as Global Reset (bit 2), except that the host controller does not send the Global Reset on USB.
1	**Host Controller Reset (HCRESET)** – R/W. The effects of HCRESET on Hub registers are slightly different from Chip Hardware Reset and Global USB Reset. The HCRESET affects bits [8,3:0] of the Port Status and Control Register (PORTSC) of each port. HCRESET resets the state machines of the host controller including the Connect/Disconnect state machine (one for each port). When the Connect/Disconnect state machine is reset, the output that signals connect/disconnect are negated to 0, effectively signaling a disconnect, even if a device is attached to the port. This virtual disconnect causes the port to be disabled. This disconnect and disabling of the port causes bit 1 (connect status change) and bit 3 (port enable/disable change) of the PORTSC (D29:F0/F1/F2/F3:BASE + 10h) to get set. The disconnect also causes bit 8 of PORTSC to reset. About 64 bit times after HCRESET goes to 0, the connect and low-speed detect will take place, and bits 0 and 8 of the PORTSC will change accordingly. 0 = Reset by the host controller when the reset process is complete. 1 = Reset. When this bit is set, the host controller module resets its internal timers, counters, state machines, and so forth, to their initial value. Any transaction currently in progress on USB is immediately terminated.
0	**Run/Stop (RS)** – R/W. When set to 1, the Intel® 631xESB/632xESB I/O Controller Hub proceeds with execution of the schedule. It continues execution as long as this bit is set. When this bit is cleared, it completes the current transaction on the USB and then halts. The HC Halted bit in the status register indicates when the host controller has finished the transaction and has entered the stopped state. The host controller clears this bit when the following fatal errors occur: consistency check failure, PCI Bus errors. 0 = Stop 1 = Run ***Note:*** This bit should only be cleared if there are no active Transaction Descriptors in the executable schedule or software will reset the host controller prior to setting this bit again.

Table 16-3. Run/Stop, Debug Bit Interaction SWDBG (Bit 5), Run/Stop (Bit 0) Operation

SWDBG (Bit 5)	Run/Stop (Bit 0)	Description
0	0	If executing a command, the host controller completes the command and then stops. The 1.0 ms frame counter is reset and command list execution resumes from start of frame using the frame list pointer selected by the current value in the FRNUM register. (While Run/Stop=0, the FRNUM register (D29:F0/F1/F2/F3:BASE + 06h) can be reprogrammed).
0	1	Execution of the command list resumes from Start Of Frame using the frame list pointer selected by the current value in the FRNUM register. The host controller remains running until the Run/Stop bit is cleared (by software or hardware).
1	0	If executing a command, the host controller completes the command and then stops and the 1.0 ms frame counter is frozen at its current value. All status are preserved. The host controller begins execution of the command list from where it left off when the Run/Stop bit is set.
1	1	Execution of the command list resumes from where the previous execution stopped. The Run/Stop bit is set to 0 by the host controller when a TD is being fetched. This causes the host controller to stop again after the execution of the TD (single step). When the host controller has completed execution, the HC Halted bit in the Status Register is set.

When the USB host controller is in Software Debug Mode (USBCMD Register bit 5=1), the single stepping software debug operation is as follows:

To Enter Software Debug Mode:

1. HCD puts host controller in Stop state by setting the Run/Stop bit to 0.
2. HCD puts host controller in Debug Mode by setting the SWDBG bit to 1.
3. HCD sets up the correct command list and Start Of Frame value for starting point in the Frame List Single Step Loop.
4. HCD sets Run/Stop bit to 1.
5. Host controller executes next active TD, sets Run/Stop bit to 0, and stops.
6. HCD reads the USBCMD register to check if the single step execution is completed (HCHalted=1).
7. HCD checks results of TD execution. Go to step 4 to execute next TD or step 8 to end Software Debug mode.
8. HCD ends Software Debug mode by setting SWDBG bit to 0.
9. HCD sets up normal command list and Frame List table.
10. HCD sets Run/Stop bit to 1 to resume normal schedule execution.

In Software Debug mode, when the Run/Stop bit is set, the host controller starts. When a valid TD is found, the Run/Stop bit is reset. When the TD is finished, the HCHalted bit in the USBSTS register (bit 5) is set.

The SW Debug mode skips over inactive TDs and only halts after an active TD has been executed. When the last active TD in a frame has been executed, the host controller waits until the next SOF is sent and then fetches the first TD of the next frame before halting.

This HCHalted bit can also be used outside of Software Debug mode to indicate when the host controller has detected the Run/Stop bit and has completed the current transaction. Outside of the Software Debug mode, setting the Run/Stop bit to 0 always

resets the SOF counter so that when the Run/Stop bit is set the host controller starts over again from the frame list location pointed to by the Frame List Index (see FRNUM Register description) rather than continuing where it stopped.

16.2.2 USBSTS – USB Status Register

I/O Offset: Base + (02–03h) Attribute: R/WC
Default Value: 0020h Size: 16 bits

This register indicates pending interrupts and various states of the host controller. The status resulting from a transaction on the serial bus is not indicated in this register.

Bit	Description
15:6	Reserved
5	**HCHalted** – R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = The host controller has stopped executing as a result of the Run/Stop bit being set to 0, either by software or by the host controller hardware (debug mode or an internal error). Default.
4	**Host Controller Process Error** – R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = The host controller has detected a fatal error. This indicates that the host controller suffered a consistency check failure while processing a Transfer Descriptor. An example of a consistency check failure would be finding an illegal PID field while processing the packet header portion of the TD. When this error occurs, the host controller clears the Run/Stop bit in the Command register (D29:F0/F1/F2/F3:BASE + 00h, bit 0) to prevent further schedule execution. A hardware interrupt is generated to the system.
3	**Host System Error** – R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = A serious error occurred during a host system access involving the host controller module. In a PCI system, conditions that set this bit to 1 include PCI Parity error, PCI Master Abort, and PCI Target Abort. When this error occurs, the host controller clears the Run/Stop bit in the Command register to prevent further execution of the scheduled TDs. A hardware interrupt is generated to the system.
2	**Resume Detect (RSM_DET)** – R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = The host controller received a “RESUME” signal from a USB device. This is only valid if the Host controller is in a global suspend state (Command register, D29:F0/F1/F2/F3:BASE + 00h, bit 3 = 1).
1	**USB Error Interrupt** – R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = Completion of a USB transaction resulted in an error condition (for example, error counter underflow). If the TD on which the error interrupt occurred also had its IOC bit (D29:F0/F1/F2/F3:BASE + 04h, bit 2) set, both this bit and Bit 0 are set.
0	**USB Interrupt (USBINT)** – R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = The host controller sets this bit when the cause of an interrupt is a completion of a USB transaction whose Transfer Descriptor had its IOC bit set. Also set when a short packet is detected (actual length field in TD is less than maximum length field in TD), and short packet detection is enabled in that TD.

16.2.3 USBINTR – USB Interrupt Enable Register

I/O Offset: Base + (04–05h) Attribute: R/W
Default Value: 0000h Size: 16 bits

This register enables and disables reporting of the corresponding interrupt to the software. When a bit is set and the corresponding interrupt is active, an interrupt is generated to the host. Fatal errors (host controller processor error, (D29:F0/F1/F2/F3:BASE + 02h, bit 4, USBSTS Register) cannot be disabled by the host controller. Interrupt sources that are disabled in this register still appear in the Status Register to allow the software to poll for events.

Bit	Description
15:5	Reserved
4	**Scratchpad (SP) –** R/W.
3	**Short Packet Interrupt Enable** – R/W. 0 = Disabled. 1 = Enabled.
2	**Interrupt on Complete Enable (IOC)** – R/W. 0 = Disabled. 1 = Enabled.
1	**Resume Interrupt Enable –** R/W. 0 = Disabled. 1 = Enabled.
0	**Timeout/CRC Interrupt Enable** – R/W. 0 = Disabled. 1 = Enabled.

16.2.4 FRNUM – Frame Number Register

I/O Offset: Base + (06–07h) Attribute: R/W
(Writes must be Word Writes)
Default Value: 0000h Size: 16 bits

Bits [10:0] of this register contain the current frame number that is included in the frame SOF packet. This register reflects the count value of the internal frame number counter. Bits [9:0] are used to select a particular entry in the Frame List during scheduled execution. This register is updated at the end of each frame time.

This register must be written as a word. Byte writes are not supported. This register cannot be written unless the host controller is in the STOPPED state as indicated by the HCHalted bit (D29:F0/F1/F2/F3:BASE + 02h, bit 5). A write to this register while the Run/Stop bit is set (D29:F0/F1/F2/F3:BASE + 00h, bit 0) is ignored.

Bit	Description
15:11	Reserved
10:0	**Frame List Current Index/Frame Number** – R/W. This field provides the frame number in the SOF Frame. The value in this register increments at the end of each time frame (approximately every 1 ms). In addition, bits [9:0] are used for the Frame List current index and correspond to memory address signals [11:2].

16.2.5 FRBASEADD – Frame List Base Address Register

I/O Offset: Base + (08–0Bh) Attribute: R/W
Default Value: Undefined Size: 32 bits

This 32-bit register contains the beginning address of the Frame List in the system memory. HCD loads this register prior to starting the schedule execution by the host controller. When written, only the upper 20 bits are used. The lower 12 bits are written as 0's (4-KB alignment). The contents of this register are combined with the frame number counter to enable the host controller to step through the Frame List in sequence. The two least significant bits are always 00. This requires DWord alignment for all list entries. This configuration supports 1024 Frame List entries.

Bit	Description
31:12	**Base Address** – R/W. These bits correspond to memory address signals [31:12], respectively.
11:0	Reserved

16.2.6 SOFMOD – Start of Frame Modify Register

I/O Offset: Base + (0Ch) Attribute: R/W
Default Value: 40h Size: 8 bits

This 1-byte register is used to modify the value used in the generation of SOF timing on the USB. Only the 7 least significant bits are used. When a new value is written into these 7 bits, the SOF timing of the next frame will be adjusted. This feature can be used to adjust out any offset from the clock source that generates the clock that drives the SOF counter. This register can also be used to maintain real time synchronization with the rest of the system so that all devices have the same sense of real time. Using this register, the frame length can be adjusted across the full range required by the USB specification. Its initial programmed value is system dependent based on the accuracy of hardware USB clock and is initialized by system BIOS. It may be reprogrammed by USB system software at any time. Its value will take effect from the beginning of the next frame. This register is reset upon a host controller reset or global reset. Software must maintain a copy of its value for reprogramming if necessary.

Bit	Description
7	Reserved
6:0	**SOF Timing Value** – R/W. Guidelines for the modification of frame time are contained in Section 7 of the USB Specification. The SOF cycle time (number of SOF counter clock periods to generate a SOF frame length) is equal to 11936 + value in this field. The default value is decimal 64 which gives a SOF cycle time of 12000. For a 12 MHz SOF counter clock input, this produces a 1 ms Frame period. The following table indicates what SOF Timing Value to program into this field for a certain frame period. **Frame Length (# 12 MHz Clocks) (decimal)** / **SOF Reg. Value (decimal)** 11936 / 0 11937 / 1 . / . . / . 11999 / 63 12000 / 64 12001 / 65 . / . . / . 12062 / 126 12063 / 127

16.2.7 PORTSC[0,1] – Port Status and Control Register

I/O Offset: Port 0/2/4/6: Base + (10–11h) Attribute: R/WC, RO,
Port 1/3/5/7: Base + (12–13h) R/W (Word writes only)
Default Value: 0080h Size: 16 bits

Note: For Function 0, this applies to Intel® 631xESB/632xESB I/O Controller Hub USB ports 0 and 1; for Function 1, this applies to Intel® 631xESB/632xESB I/O Controller Hub USB ports 2 and 3; for Function 2, this applies to Intel® 631xESB/632xESB I/O Controller Hub USB ports 4 and 5; and for Function 3, this applies to Intel® 631xESB/632xESB I/O Controller Hub USB ports 6 and 7.

After a power-up reset, global reset, or host controller reset, the initial conditions of a port are: no device connected, Port disabled, and the bus line status is 00 (single-ended zero).

Bit	Description
15:13	Reserved – RO.
12	**Suspend –** R/W. This bit should not be written to a 1 if global suspend is active (bit 3=1 in the USBCMD register). Bit 2 and bit 12 of this register define the hub states as follows: **Bits [12,2] Hub State** X0 Disable 01 Enable 11 Suspend When in suspend state, downstream propagation of data is blocked on this port, except for single-ended 0 resets (global reset and port reset). The blocking occurs at the end of the current transaction, if a transaction was in progress when this bit was written to 1. In the suspend state, the port is sensitive to resume detection. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB. 1 = Port in suspend state. 0 = Port not in suspend state. ***Note:*** Normally, if a transaction is in progress when this bit is set, the port will be suspended when the current transaction completes. However, in the case of a specific error condition (out transaction with babble), the Intel® 631xESB/632xESB I/O Controller Hub may issue a start-of-frame, and then suspend the port.
11	**Overcurrent Indicator –** R/WC. Set by hardware. 0 = Software clears this bit by writing a 1 to it. 1 = Overcurrent pin has gone from inactive to active on this port.
10	**Overcurrent Active –** RO. This bit is set and cleared by hardware. 0 = Indicates that the overcurrent pin is inactive (high). 1 = Indicates that the overcurrent pin is active (low).
9	**Port Reset –** R/W. 0 = Port is not in Reset. 1 = Port is in Reset. When set, the port is disabled and sends the USB Reset signaling.
8	**Low Speed Device Attached (LS)** – RO. 0 = Full speed device is attached. 1 = Low speed device is attached to this port.
7	Reserved – RO. Always read as 1.
6	**Resume Detect (RSM_DET) –** R/W. Software sets this bit to a 1 to drive resume signaling. The host controller sets this bit to a 1 if a J-to-K transition is detected for at least 32 microseconds while the port is in the Suspend state. The Intel® 631xESB/632xESB I/O Controller Hub will then reflect the K-state back onto the bus as long as the bit remains a 1, and the port is still in the suspend state (bit 12,2 are '11'). Writing a 0 (from 1) causes the port to send a low speed EOP. This bit will remain a 1 until the EOP has completed. 0 = No resume (K-state) detected/driven on port. 1 = Resume detected/driven on port.
5:4	**Line Status –** RO. These bits reflect the D+ (bit 4) and D– (bit 5) signals lines' logical levels. These bits are used for fault detect and recovery as well as for USB diagnostics. This field is updated at EOF2 time (See Section 11 of the USB Specification).
3	**Port Enable/Disable Change –** R/WC. For the root hub, this bit gets set only when a port is disabled due to disconnect on that port or due to the appropriate conditions existing at the EOF2 point (See Section 11 of the USB Specification). 0 = No change. Software clears this bit by writing a 1 to the bit location. 1 = Port enabled/disabled status has changed.

Bit	Description
2	**Port Enabled/Disabled (PORT_EN) –** R/W. Ports can be enabled by host software only. Ports can be disabled by either a fault condition (disconnect event or other fault condition) or by host software. Note that the bit status does not change until the port state actually changes and that there may be a delay in disabling or enabling a port if there is a transaction currently in progress on the USB. 0 = Disable 1 = Enable
1	**Connect Status Change –** R/WC. This bit indicates that a change has occurred in the port's Current Connect Status (see bit 0). The hub device sets this bit for any changes to the port device connect status, even if system software has not cleared a connect status change. If, for example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be setting" an already-set bit (that is, the bit will remain set). However, the hub transfers the change bit only once when the host controller requests a data transfer to the Status Change endpoint. System software is responsible for determining state change history in such a case. 0 = No change. Software clears this bit by writing a 1 to it. 1 = Change in Current Connect Status.
0	**Current Connect Status –** RO. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change bit (Bit 1) to be set. 0 = No device is present. 1 = Device is present on port.

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17 EHCI Controller Registers (D29:F7)

17.1 USB EHCI Configuration Registers (USB EHCI – D29:F7)

Note: Register address locations that are not shown in Table 17-1 should be treated as Reserved (see Section 11.1 for details).

Note: All configuration registers in this section are in the core well and reset by a core well reset and the D3-to-D0 warm reset, except as noted.

Table 17-1. USB EHCI PCI Register Address Map (USB EHCI – D29:F7) (Sheet 1 of 2)

Offset	Mnemonic	Register Name	Default Value	Type
00–01h	VID	Vendor Identification	8086h	RO
02–03h	DID	Device Identification	See register description	RO
04–05h	PCICMD	PCI Command	0000h	R/W, RO
06–07h	PCISTS	PCI Status	0290h	R/W, RO
08h	RID	Revision Identification	See register description	RO
09h	PI	Programming Interface	20h	RO
0Ah	SCC	Sub Class Code	03h	RO
0Bh	BCC	Base Class Code	0Ch	RO
0Dh	PMLT	Primary Master Latency Timer	00h	RO
10–13h	MEM_BASE	Memory Base Address	00000000h	R/W, RO
2C–2Dh	SVID	USB EHCI Subsystem Vendor Identification	XXXXh	R/W (special)
2E–2Fh	SID	USB EHCI Subsystem Identification	XXXXh	R/W (special)
34h	CAP_PTR	Capabilities Pointer	50h	RO
3Ch	INT_LN	Interrupt Line	00h	R/W
3Dh	INT_PN	Interrupt Pin	See register description	RO
50h	PWR_CAPID	PCI Power Management Capability ID	01h	RO
51h	NXT_PTR1	Next Item Pointer	58h	R/W (special)
52–53h	PWR_CAP	Power Management Capabilities	C9C2h	R/W (special)
54–55h	PWR_CNTL_STS	Power Management Control/Status	0000h	R/W, R/WC, RO
58h	DEBUG_CAPID	Debug Port Capability ID	0Ah	RO
59h	NXT_PTR2	Next Item Pointer #2	00h	RO
5A–5Bh	DEBUG_BASE	Debug Port Base Offset	20A0h	RO
60h	USB_RELNUM	USB Release Number	20h	RO
61h	FL_ADJ	Frame Length Adjustment	20h	R/W
62–63h	PWAKE_CAP	Port Wake Capabilities	01FFh	R/W
64–67h	–	Reserved	–	–

Table 17-1. USB EHCI PCI Register Address Map (USB EHCI – D29:F7) (Sheet 2 of 2)

Offset	Mnemonic	Register Name	Default Value	Type
68–6Bh	LEG_EXT_CAP	USB EHCI Legacy Support Extended Capability	00000001h	R/W, RO
6C–6Fh	LEG_EXT_CS	USB EHCI Legacy Extended Support Control/Status	00000000h	R/W, R/WC, RO
70–73h	SPECIAL_SMI	Intel Specific USB 2.0 SMI	00000000h	R/W, R/WC
74–7Fh	–	Reserved	–	–
80h	ACCESS_CNTL	Access Control	00h	R/W

17.1.1 VID – Vendor Identification Register (USB EHCI – D29:F7)

Offset Address: 00–01h Attribute: RO
Default Value: 8086h Size: 16 bits

Bit	Description
15:0	Vendor ID – RO. This is a 16-bit value assigned to Intel.

17.1.2 DID – Device Identification Register (USB EHCI – D29:F7)

Offset Address: 02–03h Attribute: RO
Default Value: See bits description Size: 16 bits

Bit	Description
15:0	Device ID – RO. This is a 16-bit value assigned to the Intel® 631xESB/632xESB I/O Controller Hub USB EHCI controller. Default value: 268Ch-268Fh, varies by SKU, and lower 2 bits are determined by fuses. Refer to Table 2-33.

17.1.3 PCICMD – PCI Command Register (USB EHCI – D29:F7)

Address Offset: 04–05h Attribute: R/W, RO
Default Value: 0000h Size: 16 bits

Bit	Description
15:11	Reserved
10	**Interrupt Disable –** R/W. 0 = The function is capable of generating interrupts. 1 = The function can not generate its interrupt to the interrupt controller. Note that the corresponding Interrupt Status bit (D29:F7:06h, bit 3) is not affected by the interrupt enable.
9	Fast Back to Back Enable (FBE) – RO. Hardwired to 0.
8	SERR# Enable (SERR_EN) – R/W. 0 = Disables EHC's capability to generate an SERR#. 1 = The Enhanced Host controller (EHC) is capable of generating (internally) SERR# when it receive a completion status other than "successful" for one of its DMA-initiated memory reads on ESI (and subsequently on its internal interface).
7	Wait Cycle Control (WCC) – RO. Hardwired to 0.

Bit	Description
6	Parity Error Response (PER) – RO. Hardwired to 0.
5	VGA Palette Snoop (VPS) – RO. Hardwired to 0.
4	Postable Memory Write Enable (PMWE) – RO. Hardwired to 0.
3	Special Cycle Enable (SCE) – RO. Hardwired to 0.
2	Bus Master Enable (BME) – R/W. 0 = Disables this functionality. 1 = Enables the Intel® 631xESB/632xESB I/O Controller Hub to act as a master on the PCI bus for USB transfers.
1	**Memory Space Enable (MSE) –** R/W. This bit controls access to the USB 2.0 Memory Space registers. 0 = Disables this functionality. 1 = Enables accesses to the USB 2.0 registers. The Base Address register (D29:F7:10h) for USB 2.0 should be programmed before this bit is set.
0	I/O Space Enable (IOSE) – RO. Hardwired to 0.

17.1.4 PCISTS – PCI Status Register (USB EHCI – D29:F7)

Address Offset: 06–07h
Default Value: 0290h
Attribute: R/W, RO
Size: 16 bits

Note: For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 to the bit has no effect.

Bit	Description
15	Detected Parity Error (DPE) – RO. Hardwired to 0.
14	**Signaled System Error (SSE) –** R/W. 0 = No SERR# signaled. 1 = This bit is set when it signals SERR# (internally). The SER_EN bit (bit 8 of the Command Register) must be 1 for this bit to be set.
13	**Received Master Abort (RMA) –** R/W. 0 = No master abort received by EHC on a memory access. 1 = This bit is set when EHC, as a master, receives a master abort status on a memory access. This is treated as a Host Error and halts the DMA engines. This event can optionally generate an SERR# by setting the SERR# Enable bit.
12	**Received Target Abort (RTA) –** R/W. 0 = No target abort received by EHC on memory access. 1 = This bit is set when EHC, as a master, receives a target abort status on a memory access. This is treated as a Host Error and halts the DMA engines. This event can optionally generate an SERR# by setting the SERR# Enable bit (D29:F7:04h, bit 8).
11	Signaled Target Abort (STA) – RO. This bit is used to indicate when the EHCI function responds to a cycle with a target abort. There is no reason for this to happen, so this bit will be hardwired to 0.
10:9	DEVSEL# Timing Status (DEVT_STS) – RO. This 2-bit field defines the timing for DEVSEL# assertion.
8	**Master Data Parity Error Detected (DPED) –** R/W. 0 = No data parity error detected on USB2.0 read completion packet. 1 = This bit is set when a data parity error is detected on a USB 2.0 read completion packet on the internal interface to the EHCI host controller and bit 6 of the Command register is set to 1.
7	Fast Back to Back Capable (FB2BC) – RO. Hardwired to 1.
6	User Definable Features (UDF) – RO. Hardwired to 0.
5	66 MHz Capable (66 MHz _CAP) – RO. Hardwired to 0.

Bit	Description
4	Capabilities List (CAP_LIST) – RO. Hardwired to 1 indicating that offset 34h contains a valid capabilities pointer.
3	**Interrupt Status –** RO. This bit reflects the state of this function's interrupt at the input of the enable/disable logic. 0 = This bit will be 0 when the interrupt is deasserted. 1 = This bit is a 1 when the interrupt is asserted. The value reported in this bit is independent of the value in the Interrupt Enable bit.
2:0	Reserved

17.1.5 RID – Revision Identification Register (USB EHCI – D29:F7)

Offset Address: 08h Attribute: RO
Default Value: See bit description Size: 8 bits

Bit	Description
7:0	**Revision ID –** RO. Refer to Table 2-33 or the *Intel® 631xESB/632xESB I/O Controller Hub EDS Specification Update* for the value of the Revision ID Register

17.1.6 PI – Programming Interface Register (USB EHCI – D29:F7)

Address Offset: 09h Attribute: RO
Default Value: 20h Size: 8 bits

Bit	Description
7:0	Programming Interface – RO. A value of 20h indicates that this USB 2.0 host controller conforms to the EHCI Specification.

17.1.7 SCC – Sub Class Code Register (USB EHCI – D29:F7)

Address Offset: 0Ah Attribute: RO
Default Value: 03h Size: 8 bits

Bit	Description
7:0	Sub Class Code (SCC) – RO. 03h = Universal serial bus host controller.

17.1.8 BCC – Base Class Code Register (USB EHCI – D29:F7)

Address Offset: 0Bh Attribute: RO
Default Value: 0Ch Size: 8 bits

Bit	Description
7:0	Base Class Code (BCC) – RO. 0Ch = Serial bus controller.

17.1.9 PMLT – Primary Master Latency Timer Register (USB EHCI – D29:F7)

Address Offset: 0Dh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	Master Latency Timer Count (MLTC) – RO. Hardwired to 00h. Because the EHCI controller is internally implemented with arbitration on an interface (and not PCI), it does not need a master latency timer.

17.1.10 MEM_BASE – Memory Base Address Register (USB EHCI – D29:F7)

Address Offset: 10–13h
Default Value: 00000000h
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31:10	**Base Address** – R/W. Bits [31:10] correspond to memory address signals [31:10], respectively. This gives 1-KB of locatable memory space aligned to 1-KB boundaries.
9:4	Reserved
3	Prefetchable – RO. Hardwired to 0 indicating that this range should not be prefetched.
2:1	Type – RO. Hardwired to 00b indicating that this range can be mapped anywhere within 32-bit address space.
0	Resource Type Indicator (RTE) – RO. Hardwired to 0 indicating that the base address field in this register maps to memory space.

17.1.11 SVID – USB EHCI Subsystem Vendor ID Register (USB EHCI – D29:F7)

Address Offset: 2C–2Dh
Default Value: **XXXX**h
Reset: None
Attribute: R/W (special)
Size: 16 bits

Bit	Description
15:0	**Subsystem Vendor ID (SVID)** – R/W (special). This register, in combination with the USB 2.0 Subsystem ID register, enables the operating system to distinguish each subsystem from the others. ***Note:*** Writes to this register are enabled when the WRT_RDONLY bit (D29:F7:80h, bit 0) is set to 1.

17.1.12 SID – USB EHCI Subsystem ID Register (USB EHCI – D29:F7)

Address Offset: 2E–2Fh
Default Value: XXXXh
Reset: None
Attribute: R/W (special)
Size: 16 bits

Bit	Description
15:0	**Subsystem ID (SID)** – R/W (special). BIOS sets the value in this register to identify the Subsystem ID. This register, in combination with the Subsystem Vendor ID register, enables the operating system to distinguish each subsystem from other(s). ***Note:*** Writes to this register are enabled when the WRT_RDONLY bit (D29:F7:80h, bit 0) is set to 1.

17.1.13 CAP_PTR – Capabilities Pointer Register (USB EHCI – D29:F7)

Address Offset: 34h
Default Value: 50h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	Capabilities Pointer (CAP_PTR) – RO. This register points to the starting offset of the USB 2.0 capabilities ranges.

17.1.14 INT_LN – Interrupt Line Register (USB EHCI – D29:F7)

Address Offset: 3Ch
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	**Interrupt Line (INT_LN) –** R/W. This data is not used. It is used as a scratchpad register to communicate to software the interrupt line that the interrupt pin is connected to.

17.1.15 INT_PN – Interrupt Pin Register (USB EHCI – D29:F7)

Address Offset: 3Dh
Default Value: See Description
Attribute: RO
Size: 8 bits

Bit	Description
7:0	Interrupt Pin – RO. This reflects the value of D29IP.EIP (Chipset Config Registers:Offset 3108:bits 31:28). ***Note:*** Bits 7:4 are always 0h

17.1.16 PWR_CAPID – PCI Power Management Capability ID Register (USB EHCI – D29:F7)

Address Offset: 50h
Default Value: 01h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	Power Management Capability ID – RO. A value of 01h indicates that this is a PCI Power Management capabilities field.

17.1.17 NXT_PTR1 – Next Item Pointer #1 Register (USB EHCI – D29:F7)

Address Offset: 51h
Default Value: 58h
Attribute: R/W (special)
Size: 8 bits

Bit	Description
7:0	**Next Item Pointer 1 Value** – R/W (special). This register defaults to 58h, which indicates that the next capability registers begin at configuration offset 58h. This register is writable when the WRT_RDONLY bit (D29:F7:80h, bit 0) is set. This allows BIOS to effectively hide the Debug Port capability registers, if necessary. This register should only be written during system initialization before the plug-and-play software has enabled any master-initiated traffic. Only values of 58h (Debug Port visible) and 00h (Debug Port invisible) are expected to be programmed in this register. ***Note:*** Register not reset by D3-to-D0 warm reset.

17.1.18 PWR_CAP – Power Management Capabilities Register (USB EHCI – D29:F7)

Address Offset: 52–53h
Default Value: C9C2h
Attribute: R/W (special)
Size: 16 bits

Bit	Description
15:11	**PME Support (PME_SUP)** – R/W (special). This 5-bit field indicates the power states in which the function may assert PME#. The Intel® 631xESB/632xESB I/O Controller Hub EHC does not support the D1 or D2 states. For all other states, the Intel® 631xESB/632xESB I/O Controller Hub EHC is capable of generating PME#. Software should never need to modify this field.
10	D2 Support **(D2_SUP)** – R/W (special). 0 = D2 State is not supported 1 = D2 State is supported
9	D1 Support **(D1_SUP)** – R/W (special). 0 = D1 State is not supported 1 = D1 State is supported
8:6	**Auxiliary Current (AUX_CUR)** – R/W (special). The Intel® 631xESB/632xESB I/O Controller Hub EHC reports 375 mA maximum Suspend well current required when in the $D3_{COLD}$ state. This value can be written by BIOS when a more accurate value is known.
5	**Device Specific Initialization (DSI**) – R/W (special). The Intel® 631xESB/632xESB I/O Controller Hub reports 0, indicating that no device-specific initialization is required.
4	Reserved
3	**PME Clock (PME_CLK)** – R/W (special). The Intel® 631xESB/632xESB I/O Controller Hub reports 0, indicating that no PCI clock is required to generate PME#.
2:0	**Version (VER)** – R/W (special). The Intel® 631xESB/632xESB I/O Controller Hub reports 010b, indicating that it complies with Revision 1.1 of the PCI Power Management Specification.

Notes:
1. Normally, this register is read-only to report capabilities to the power management software. To report different power management capabilities, depending on the system in which the Intel® 631xESB/632xESB I/O Controller Hub is used, bits 15:11 and 8:6 in this register are writable when the WRT_RDONLY bit (D29:F7:80h, bit 0) is set. The value written to this register does not affect the hardware other than changing the value returned during a read.
2. Reset: core well, but not D3-to-D0 warm reset.

17.1.19 PWR_CNTL_STS – Power Management Control/Status Register (USB EHCI – D29:F7)

Address Offset: 54–55h
Default Value: 0000h
Attribute: R/W, R/WC, RO
Size: 16 bits

Bit	Description
15	**PME Status –** R/WC. 0 = Writing a 1 to this bit will clear it and cause the internal PME to deassert (if enabled). 1 = This bit is set when the EHC would normally assert the PME# signal independent of the state of the PME_En bit. ***Note:*** This bit must be explicitly cleared by the operating system each time the operating system is loaded.
14:13	Data Scale – RO. Hardwired to 00b indicating it does not support the associated Data register.
12:9	Data Select – RO. Hardwired to 0000b indicating it does not support the associated Data register.
8	**PME Enable –** R/W. 0 = Disable. 1 = Enable. Enables EHC to generate an internal PME signal when PME_Status is 1. ***Note:*** This bit must be explicitly cleared by the operating system each time it is initially loaded.
7:2	Reserved
1:0	**Power State –** R/W. This 2-bit field is used both to determine the current power state of EHC function and to set a new power state. The definition of the field values are: 00 = D0 state 11 = $D3_{HOT}$ state If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the $D3_{HOT}$ state, the must not accept accesses to the EHC memory range; but the configuration space must still be accessible. When not in the D0 state, the generation of the interrupt output is blocked. Specifically, the PIRQH is not asserted when not in the D0 state. When software changes this value from the $D3_{HOT}$ state to the D0 state, an internal warm (soft) reset is generated, and software must re-initialize the function.

Note: Reset (bits 15, 8): suspend well, and not D3-to-D0 warm reset nor core well reset.

17.1.20 DEBUG_CAPID – Debug Port Capability ID Register (USB EHCI – D29:F7)

Address Offset: 58h
Default Value: 0Ah
Attribute: RO
Size: 8 bits

Bit	Description
7:0	Debug Port Capability ID – RO. Hardwired to 0Ah indicating that this is the start of a Debug Port Capability structure.

17.1.21 NXT_PTR2 – Next Item Pointer #2 Register (USB EHCI – D29:F7)

Address Offset: 59h
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	Next Item Pointer 2 Capability – RO. Hardwired to 00h to indicate there are no more capability structures in this function.

17.1.22 DEBUG_BASE – Debug Port Base Offset Register (USB EHCI – D29:F7)

Address Offset: 5Ah–5Bh
Default Value: 20A0h
Attribute: RO
Size: 16 bits

Bit	Description
15:13	**BAR Number –** RO. Hardwired to 001b to indicate the memory BAR begins at offset 10h in the EHCI configuration space.
12:0	**Debug Port Offset –** RO. Hardwired to 0A0h to indicate that the Debug Port registers begin at offset A0h in the EHCI memory range.

17.1.23 USB_RELNUM – USB Release Number Register (USB EHCI – D29:F7)

Address Offset: 60h
Default Value: 20h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	USB Release Number – RO. A value of 20h indicates that this controller follows *Universal Serial Bus (USB) Specification*, Revision 2.0.

17.1.24 FL_ADJ – Frame Length Adjustment Register (USB EHCI – D29:F7)

Address Offset: 61h
Default Value: 20h
Attribute: R/W
Size: 8 bits

This feature is used to adjust any offset from the clock source that generates the clock that drives the SOF counter. When a new value is written into these six bits, the length of the frame is adjusted. Its initial programmed value is system dependent based on the accuracy of hardware USB clock and is initialized by system BIOS. This register should only be modified when the HChalted bit (D29:F7:CAPLENGTH + 24h, bit 12) in the USB2.0_STS register is a 1. Changing value of this register while the host controller is operating yields undefined results. It should not be reprogrammed by USB system software unless the default or BIOS programmed values are incorrect, or the system is restoring the register while returning from a suspended state.

These bits in suspend well and not reset by a D3-to-D0 warm rest or a core well reset.

Bit	Description
7:6	Reserved – RO. These bits are reserved for future use and should read as 00b.
5:0	**Frame Length Timing Value –** R/W. Each decimal value change to this register corresponds to 16 high-speed bit times. The SOF cycle time (number of SOF counter clock periods to generate a SOF micro-frame length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000. Frame Length FLADJ Value (# 480 MHz Clocks) decimal (hex) 594880 (00h) 595041 (01h) 595202 (02h) … 59984 31 (1Fh) 60000 32 (20h) … 60480 62 (3Eh) 60496 63 (3Fh)

17.1.25 PWAKE_CAP – Port Wake Capability Register (USB EHCI – D29:F7)

Address Offset: 62–63h
Default Value: 01FFh
Attribute: R/W
Size: 16 bits

This register is in the suspend power well. The intended use of this register is to establish a policy about which ports are to be used for wake events. Bit positions 1–8 in the mask correspond to a physical port implemented on the current EHCI controller. A 1 in a bit position indicates that a device connected below the port can be enabled as a wake-up device and the port may be enabled for disconnect/connect or overcurrent events as wake-up events. This is an information-only mask register. The bits in this register **do not** affect the actual operation of the EHCI host controller. The system-specific policy can be established by BIOS initializing this register to a system-specific value. System software uses the information in this register when enabling devices and ports for remote wake-up.

These bits are not reset by a D3-to-D0 warm rest or a core well reset.

Bit	Description
15:9	Reserved – RO.
8:1	**Port Wake Up Capability Mask –** R/W. Bit positions 1 through 8 correspond to a physical port implemented on this host controller. For example, bit position 1 corresponds to port 1, bit position 2 corresponds to port 2, and so forth.
0	**Port Wake Implemented –** R/W. A 1 in this bit indicates that this register is implemented to software.

17.1.26 LEG_EXT_CAP – USB EHCI Legacy Support Extended Capability Register (USB EHCI – D29:F7)

Address Offset: 68–6Bh
Default Value: 00000001h
Power Well: Suspend
Attribute: R/W, RO
Size: 32 bits
Note: These bits are not reset by a D3-to-D0 warm rest or a core well reset.

Bit	Description
31:25	Reserved – RO. Hardwired to 00h
24	**HC OS Owned Semaphore** – R/W. System software sets this bit to request ownership of the EHCI controller. Ownership is obtained when this bit reads as 1 and the HC BIOS Owned Semaphore bit reads as clear.
23:17	Reserved – RO. Hardwired to 00h
16	**HC BIOS Owned Semaphore –** R/W. The BIOS sets this bit to establish ownership of the EHCI controller. System BIOS will clear this bit in response to a request for ownership of the EHCI controller by system software.
15:8	**Next EHCI Capability Pointer** – RO. Hardwired to 00h to indicate that there are no EHCI Extended Capability structures in this device.
7:0	**Capability ID** – RO. Hardwired to 01h to indicate that this EHCI Extended Capability is the Legacy Support Capability.

17.1.27 LEG_EXT_CS – USB EHCI Legacy Support Extended Control / Status Register (USB EHCI – D29:F7)

Address Offset: 6C–6Fh
Default Value: 00000000h
Power Well: Suspend
Attribute: R/W, R/WC, RO
Size: 32 bits
Note: These bits are not reset by a D3-to-D0 warm rest or a core well reset.

Bit	Description
31	**SMI on BAR** – R/WC. Software clears this bit by writing a 1 to it. 0 = Base Address Register (BAR) not written. 1 = This bit is set to 1 when the Base Address Register (BAR) is written.
30	**SMI on PCI Command** – R/WC. Software clears this bit by writing a 1 to it. 0 = PCI Command (PCICMD) Register Not written. 1 = This bit is set to 1 when the PCI Command (PCICMD) Register is written.
29	**SMI on OS Ownership Change** – R/WC. Software clears this bit by writing a 1 to it. 0 = No HC OS Owned Semaphore bit change. 1 = This bit is set to 1 when the HC OS Owned Semaphore bit in the LEG_EXT_CAP register (D29:F7:68h, bit 24) transitions from 1 to 0 or 0 to 1.
28:22	Reserved – RO. Hardwired to 00h
21	**SMI on Async Advance** – RO. This bit is a shadow bit of the Interrupt on Async Advance bit (D29:F7:CAPLENGTH + 24h, bit 5) in the USB2.0_STS register. ***Note:*** To clear this bit system software must write a 1 to the Interrupt on Async Advance bit in the USB2.0_STS register.
20	**SMI on Host System Error** – RO. This bit is a shadow bit of Host System Error bit in the USB2.0_STS register (D29:F7:CAPLENGTH + 24h, bit 4). ***Note:*** To clear this bit system software must write a 1 to the Host System Error bit in the USB2.0_STS register.
19	**SMI on Frame List Rollover** – RO. This bit is a shadow bit of Frame List Rollover bit (D29:F7:CAPLENGTH + 24h, bit 3) in the USB2.0_STS register. ***Note:*** To clear this bit system software must write a 1 to the Frame List Rollover bit in the USB2.0_STS register.

Bit	Description
18	**SMI on Port Change Detect** – RO. This bit is a shadow bit of Port Change Detect bit (D29:F7:CAPLENGTH + 24h, bit 2) in the USB2.0_STS register. ***Note:*** To clear this bit system software must write a 1 to the Port Change Detect bit in the USB2.0_STS register.
17	**SMI on USB Error** – RO. This bit is a shadow bit of USB Error Interrupt (USBERRINT) bit (D29:F7:CAPLENGTH + 24h, bit 1) in the USB2.0_STS register. ***Note:*** To clear this bit system software must write a 1 to the USB Error Interrupt bit in the USB2.0_STS register.
16	**SMI on USB Complete –** RO. This bit is a shadow bit of USB Interrupt (USBINT) bit (D29:F7:CAPLENGTH + 24h, bit 0) in the USB2.0_STS register. ***Note:*** To clear this bit system software must write a 1 to the USB Interrupt bit in the USB2.0_STS register.
15	**SMI on BAR Enable –** R/W. 0 = Disable. 1 = Enable. When this bit is 1 and SMI on BAR (D29:F7:6Ch, bit 31) is 1, then the host controller will issue an SMI.
14	**SMI on PCI Command Enable** – R/W. 0 = Disable. 1 = Enable. When this bit is 1 and SMI on PCI Command (D29:F7:6Ch, bit 30) is 1, then the host controller will issue an SMI.
13	**SMI on OS Ownership Enable** – R/W. 0 = Disable. 1 = Enable. When this bit is a 1 AND the OS Ownership Change bit (D29:F7:6Ch, bit 29) is 1, the host controller will issue an SMI.
12:6	Reserved – RO. Hardwired to 00h
5	**SMI on Async Advance Enable** – R/W. 0 = Disable. 1 = Enable. When this bit is a 1, and the SMI on Async Advance bit (D29:F7:6Ch, bit 21) is a 1, the host controller will issue an SMI immediately.
4	**SMI on Host System Error Enable** – R/W. 0 = Disable. 1 = Enable. When this bit is a 1, and the SMI on Host System Error (D29:F7:6Ch, bit 20) is a 1, the host controller will issue an SMI.
3	**SMI on Frame List Rollover Enable** – R/W. 0 = Disable. 1 = Enable. When this bit is a 1, and the SMI on Frame List Rollover bit (D29:F7:6Ch, bit 19) is a 1, the host controller will issue an SMI.
2	**SMI on Port Change Enable** – R/W. 0 = Disable. 1 = Enable. When this bit is a 1, and the SMI on Port Change Detect bit (D29:F7:6Ch, bit 18) is a 1, the host controller will issue an SMI.
1	**SMI on USB Error Enable** – R/W. 0 = Disable. 1 = Enable. When this bit is a 1, and the SMI on USB Error bit (D29:F7:6Ch, bit 17) is a 1, the host controller will issue an SMI immediately.
0	**SMI on USB Complete Enable** – R/W. 0 = Disable. 1 = Enable. When this bit is a 1, and the SMI on USB Complete bit (D29:F7:6Ch, bit 16) is a 1, the host controller will issue an SMI immediately.

17.1.28 SPECIAL_SMI – Intel Specific USB 2.0 SMI Register (USB EHCI – D29:F7)

Address Offset: 70–73h
Default Value: 00000000h
Power Well: Suspend
Attribute: R/W, R/WC
Size: 32 bits

Note: These bits are not reset by a D3-to-D0 warm rest or a core well reset.

Bit	Description
31:30	Reserved – RO. Hardwired to 00h
29:22	**SMI on PortOwner –** R/WC. Software clears these bits by writing a 1 to it. 0 = No Port Owner bit change. 1 = Bits 29:22 correspond to the Port Owner bits for ports 1 (22) through 8 (29). These bits are set to 1 when the associated Port Owner bits transition from 0 to 1 or 1 to 0.
21	**SMI on PMCSR** – R/WC. Software clears these bits by writing a 1 to it. 0 = Power State bits Not modified. 1 = Software modified the Power State bits in the Power Management Control/Status (PMCSR) register (D29:F7:54h).
20	**SMI on Async** – R/WC. Software clears these bits by writing a 1 to it. 0 = No Async Schedule Enable bit change 1 = Async Schedule Enable bit transitioned from 1 to 0 or 0 to 1.
19	**SMI on Periodic** – R/WC. Software clears this bit by writing a 1 it. 0 = No Periodic Schedule Enable bit change. 1 = Periodic Schedule Enable bit transitions from 1 to 0 or 0 to 1.
18	**SMI on CF** – R/WC. Software clears this bit by writing a 1 it. 0 = No Configure Flag (CF) change. 1 = Configure Flag (CF) transitions from 1 to 0 or 0 to 1.
17	**SMI on HCHalted –** R/WC. Software clears this bit by writing a 1 it. 0 = HCHalted did Not transition to 1 (as a result of the Run/Stop bit being cleared). 1 = HCHalted transitions to 1 (as a result of the Run/Stop bit being cleared).
16	**SMI on HCReset –** R/WC. Software clears this bit by writing a 1 it. 0 = HCRESET did Not transitioned to 1. 1 = HCRESET transitioned to 1.
15:14	Reserved – RO. Hardwired to 00h
13:6	**SMI on PortOwner Enable** – R/W. 0 = Disable. 1 = Enable. When any of these bits are 1 and the corresponding SMI on PortOwner bits are 1, then the host controller will issue an SMI. Unused ports should have their corresponding bits cleared.
5	**SMI on PMSCR Enable** – R/W. 0 = Disable. 1 = Enable. When this bit is 1 and SMI on PMSCR is 1, then the host controller will issue an SMI.
4	**SMI on Async Enable** – R/W. 0 = Disable. 1 = Enable. When this bit is 1 and SMI on Async is 1, then the host controller will issue an SMI
3	**SMI on Periodic Enable** – R/W. 0 = Disable. 1 = Enable. When this bit is 1 and SMI on Periodic is 1, then the host controller will issue an SMI.
2	**SMI on CF Enable** – R/W. 0 = Disable. 1 = Enable. When this bit is 1 and SMI on CF is 1, then the host controller will issue an SMI.
1	**SMI on HCHalted Enable** – R/W. 0 = Disable. 1 = Enable. When this bit is a 1 and SMI on HCHalted is 1, then the host controller will issue an SMI.
0	**SMI on HCReset Enable** – R/W. 0 = Disable. 1 = Enable. When this bit is a 1 and SMI on HCReset is 1, then host controller will issue an SMI.

17.1.29 ACCESS_CNTL – Access Control Register (USB EHCI – D29:F7)

Address Offset: 80h
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:1	Reserved
0	**WRT_RDONLY –** R/W. When set to 1, this bit enables a select group of normally read-only registers in the EHC function to be written by software. Registers that may only be written when this mode is entered are noted in the summary tables and detailed description as “Read/Write-Special”. The registers fall into two categories: 1. System-configured parameters, and 2. Status bits

17.2 Memory-Mapped I/O Registers

The EHCI memory-mapped I/O space is composed of two sets of registers: Capability Registers and Operational Registers.

Note: The Intel® 631xESB/632xESB I/O Controller Hub EHCI controller will not accept memory transactions (neither reads nor writes) as a target that are locked transactions. The locked transactions should not be forwarded to PCI as the address space is known to be allocated to USB.

Note: When the EHCI function is in the D3 PCI power state, accesses to the USB 2.0 memory range are ignored and result a master abort. Similarly, if the Memory Space Enable (MSE) bit (D29:F7:04h, bit 1) is not set in the Command register in configuration space, the memory range will not be decoded by the Intel® 631xESB/632xESB I/O Controller Hub Enhanced Host controller (EHC). If the MSE bit is not set, then the Intel® 631xESB/632xESB I/O Controller Hub must default to allowing any memory accesses for the range specified in the BAR to go to PCI. This is because the range may not be valid and, therefore, the cycle must be made available to any other targets that may be currently using that range.

17.2.1 Host Controller Capability Registers

These registers specify the limits, restrictions and capabilities of the host controller implementation. Within the host controller capability registers, only the structural parameters register is writable. These registers are implemented in the suspend well and is only reset by the standard suspend-well hardware reset, not by HCRESET or the D3-to-D0 reset.

Table 17-2. Enhanced Host Controller Capability Registers

MEM_BASE + Offset	Mnemonic	Register	Default	Type
00h	CAPLENGTH	Capabilities Registers Length	20h	RO
02–03h	HCIVERSION	Host Controller Interface Version Number	0100h	RO
04–07h	HCSPARAMS	Host Controller Structural Parameters	00104208h	R/W (special), RO
08–0Bh	HCCPARAMS	Host Controller Capability Parameters	00006871h	RO

Note: “Read/Write Special” means that the register is normally read-only, but may be written when the WRT_RDONLY bit is set. Because these registers are expected to be programmed by BIOS during initialization, their contents must not get modified by HCRESET or D3-to-D0 internal reset.

17.2.1.1 CAPLENGTH – Capability Registers Length Register

Offset: MEM_BASE + 00h Attribute: RO
Default Value: 20h Size: 8 bits

Bit	Description
7:0	Capability Register Length Value – RO. This register is used as an offset to add to the Memory Base Register (D29:F7:10h) to find the beginning of the Operational Register Space. This field is hardwired to 20h indicating that the Operation Registers begin at offset 20h.

17.2.1.2 HCIVERSION – Host Controller Interface Version Number Register

Offset: MEM_BASE + 02–03h Attribute: RO
Default Value: 0100h Size: 16 bits

Bit	Description
15:0	Host Controller Interface Version Number – RO. This is a two-byte register containing a BCD encoding of the version number of interface that this host controller interface conforms.

17.2.1.3 HCSPARAMS – Host Controller Structural Parameters

Offset: MEM_BASE + 04–07h Attribute: R/W (special), RO
Default Value: 00104208h Size: 32 bits

Note: This register is reset by a suspend well reset and not a D3-to-D0 reset or HCRESET.

Bit	Description
31:24	Reserved – RO. Default=0h.
23:20	Debug Port Number (DP_N) – R/W (special). Hardwired to 1h indicating that the Debug Port is on the lowest numbered port.
19:16	Reserved
15:12	**Number of Companion Controllers (N_CC) –** R/W (special). This field indicates the number of companion controllers associated with this USB EHCI host controller. A 0 in this field indicates there are no companion host controllers. Port-ownership hand-off is not supported. Only high-speed devices are supported on the host controller root ports. A value larger than 1 in this field indicates there are companion USB UHCI host controller(s). Port-ownership hand-offs are supported. High, Full- and Low-speed devices are supported on the host controller root ports. The Intel® 631xESB/632xESB I/O Controller Hub allows the default value of 4h to be over-written by BIOS. When removing classic controllers, they should be disabled in the following order: Function 3, Function 2, Function 1, and Function 0, which correspond to ports 7:6, 5:4, 3:2, and 1:0, respectively.
11:8	Number of Ports per Companion Controller (N_PCC) – RO. Hardwired to 2h. This field indicates the number of ports supported per companion host controller. It is used to indicate the port routing configuration to system software.
7:4	Reserved. These bits are reserved and default to 0.
3:0	**N_PORTS –** R/W (special). This field specifies the number of physical downstream ports implemented on this host controller. The value of this field determines how many port registers are addressable in the Operational Register Space. Valid values are in the range of 1h to Fh. Reports 8h by default. However, software may write a value less than 8 for some platform configurations. A 0 in this field is undefined.

Note: This register is writable when the WRT_RDONLY bit is set.

17.2.1.4 HCCPARAMS – Host Controller Capability Parameters Register

Offset: MEM_BASE + 08–0Bh Attribute: RO
Default Value: 00006871h Size: 32 bits

Bit	Description
31:16	Reserved
15:8	EHCI Extended Capabilities Pointer (EECP) – RO. This field is hardwired to 68h, indicating that the EHCI capabilities list exists and begins at offset 68h in the PCI configuration space.
7:4	Isochronous Scheduling Threshold – RO. This field indicates, relative to the current position of the executing host controller, where software can reliably update the isochronous schedule. When bit 7 is 0, the value of the least significant 3 bits indicates the number of micro-frames a host controller hold a set of isochronous data structures (one or more) before flushing the state. When bit 7 is a 1, then host software assumes the host controller may cache an isochronous data structure for an entire frame. Refer to the EHCI specification for details on how software uses this information for scheduling isochronous transfers. This field is hardwired to 7h.
3	Reserved. These bits are reserved and should be set to 0.
2	Asynchronous Schedule Park Capability – RO. This bit is hardwired to 0 indicating that the host controller does not support this optional feature
1	Programmable Frame List Flag – RO. 0 = System software must use a frame list length of 1024 elements with this host controller. The USB2.0_CMD register (D29:F7:CAPLENGTH + 20h, bits 3:2) *Frame List Size* field is a read-only register and must be set to 0. 1 = System software can specify and use a smaller frame list and configure the host controller via the USB2.0_CMD register *Frame List Size* field. The frame list must always be aligned on a 4K page boundary. This requirement ensures that the frame list is always physically contiguous.
0	64-bit Addressing Capability – RO. This field documents the addressing range capability of this implementation. The value of this field determines whether software should use the 32-bit or 64-bit data structures. Values for this field have the following interpretation: 0 = Data structures using 32-bit address memory pointers 1 = Data structures using 64-bit address memory pointers This bit is hardwired to 1. ***Note:*** Intel® 631xESB/632xESB I/O Controller Hub only implements 44 bits of addressing. Bits 63:44 will always be 0.

17.2.2 Host Controller Operational Registers

This section defines the enhanced host controller operational registers. These registers are located after the capabilities registers. The operational register base must be DWord-aligned and is calculated by adding the value in the first capabilities register (CAPLENGTH) to the base address of the enhanced host controller register address space (MEM_BASE). Since CAPLENGTH is always 20h, Table 17-3 already accounts for this offset. All registers are 32 bits in length.

Table 17-3. Enhanced Host Controller Operational Register Address Map (Sheet 1 of 2)

MEM_BASE + Offset	Mnemonic	Register Name	Default	Special Notes	Type
20–23h	USB2.0_CMD	USB 2.0 Command	00080000h		R/W, RO
24–27h	USB2.0_STS	USB 2.0 Status	00001000h		R/WC, RO
28–2Bh	USB2.0_INTR	USB 2.0 Interrupt Enable	00000000h		R/W
2C–2Fh	FRINDEX	USB 2.0 Frame Index	00000000h		R/W,
30–33h	CTRLDSSEGMENT	Control Data Structure Segment	00000000h		R/W, RO

Table 17-3. Enhanced Host Controller Operational Register Address Map (Sheet 2 of 2)

MEM_BASE + Offset	Mnemonic	Register Name	Default	Special Notes	Type
34–37h	PERODICLISTBASE	Period Frame List Base Address	00000000h		R/W
38–3Bh	ASYNCLISTADDR	Current Asynchronous List Address	00000000h		R/W
3C–5Fh	–	Reserved	0h		RO
60–63h	CONFIGGLAG	Configure Flag	00000000h	Suspend	R/W
64–67h	PORT0SC	Port 0 Status and Control	00003000h	Suspend	R/W, R/WC, RO
68–6Bh	PORT1SC	Port 1 Status and Control	00003000h	Suspend	R/W, R/WC, RO
6C–6Fh	PORT2SC	Port 2 Status and Control	00003000h	Suspend	R/W, R/WC, RO
70–73h	PORT3SC	Port 3 Status and Control	00003000h	Suspend	R/W, R/WC, RO
74–77h	PORT4SC	Port 4 Status and Control	00003000h	Suspend	R/W, R/WC, RO
78–7Bh	PORT5SC	Port 5 Status and Control	00003000h	Suspend	R/W, R/WC, RO
7C–7Fh	PORT6SC	Port 6 Status and Control	00003000h	Suspend	R/W, R/WC, RO
80–83h	PORT7SC	Port 7 Status and Control	00003000h	Suspend	R/W, R/WC, RO
84–9Fh	–	Reserved	Undefined		RO
A0–B3h	–	Debug Port Registers	Undefined		See register description
B4–3FFh	–	Reserved	Undefined		RO

Note: Software must read and write these registers using only DWord accesses.These registers are divided into two sets. The first set at offsets MEM_BASE + 00:3Bh are implemented in the core power well. Unless otherwise noted, the core-well registers are reset by the assertion of any of the following:

- Core well hardware reset
- HCRESET
- D3-to-D0 reset

The second set at offsets MEM_BASE + 60h to the end of the implemented register space are implemented in the Suspend power well. Unless otherwise noted, the suspend-well registers are reset by the assertion of either of the following:

- Suspend well hardware reset
- HCRESET

17.2.2.1 USB2.0_CMD – USB 2.0 Command Register

Offset: MEM_BASE + 20–23h Attribute: R/W, RO
Default Value: 00080000h Size: 32 bits

Bit	Description
31:24	Reserved. These bits are reserved and should be set to 0 when writing this register.
23:16	**Interrupt Threshold Control** – R/W. System software uses this field to select the maximum rate at which the host controller will issue interrupts. The only valid values are defined below. If software writes an invalid value to this register, the results are undefined. Value Maximum Interrupt Interval 00h Reserved 01h1 micro-frame 02h2 micro-frames 04h4 micro-frames (default) 08h8 micro-frames (default, equates to 1 ms) 10h16 micro-frames (2 ms) 20h32 micro-frames (4 ms) 40h64 micro-frames (8 ms)
15:8	Reserved. These bits are reserved and should be set to 0 when writing this register.
11:8	Unimplemented Asynchronous Park Mode Bits. Hardwired to 000b indicating the host controller does not support this optional feature.
7	Light Host Controller Reset – RO. Hardwired to 0. optional reset is not implemented.
6	**Interrupt on Async Advance Doorbell** – R/W. This bit is used as a doorbell by software to tell the host controller to issue an interrupt the next time it advances asynchronous schedule. 0 = The host controller sets this bit to a 0 after it has set the Interrupt on Async Advance status bit (D29:F7:CAPLENGTH + 24h, bit 5) in the USB2.0_STS register to a 1. 1 = Software must write a 1 to this bit to ring the doorbell. When the host controller has evicted all appropriate cached schedule state, it sets the Interrupt on Async Advance status bit in the USB2.0_STS register. If the *Interrupt on Async Advance Enable* bit in the USB2.0_INTR register (D29:F7:CAPLENGTH + 28h, bit 5) is a 1 then the host controller will assert an interrupt at the next interrupt threshold. See the EHCI specification for operational details. ***Note:*** Software should not write a 1 to this bit when the asynchronous schedule is inactive. Doing so will yield undefined results.
5	**Asynchronous Schedule Enable** – R/W. Default 0b. This bit controls whether the host controller skips processing the Asynchronous Schedule. 0 = Do not process the Asynchronous Schedule 1 = Use the ASYNCLISTADDR register to access the Asynchronous Schedule.
4	**Periodic Schedule Enable** – R/W. Default 0b. This bit controls whether the host controller skips processing the Periodic Schedule. 0 = Do not process the Periodic Schedule 1 = Use the PERIODICLISTBASE register to access the Periodic Schedule.

Bit	Description
3:2	**Frame List Size** – RO. Hardwire this field to 00b because it only supports the 1024-element frame list size.
1	**Host Controller Reset (HCRESET)** – R/W. This control bit used by software to reset the host controller. The effects of this on root hub registers are similar to a Chip Hardware Reset (that is, RSMRST# assertion and PWROK deassertion on the Intel® 631xESB/632xESB I/O Controller Hub). When software writes a 1 to this bit, the host controller resets its internal pipelines, timers, counters, state machines, and so forth, to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports. ***Note:*** PCI configuration registers and Host controller capability registers are not effected by this reset. All operational registers, including port registers and port state machines are set to their initial values. Port ownership reverts to the companion host controller(s), with the side effects described in the EHCI spec. Software must re-initialize the host controller in order to return the host controller to an operational state. This bit is set to 0 by the host controller when the reset process is complete. Software cannot terminate the reset process early by writing a 0 to this register. Software should not set this bit to a 1 when the HCHalted bit (D29:F7:CAPLENGTH + 24h, bit 12) in the USB2.0_STS register is a 0. Attempting to reset an actively running host controller will result in undefined behavior. This reset me be used to leave EHCI port test modes.
0	**Run/Stop (RS)** – R/W. 0 = Stop (default) 1 = Run. When set to a 1, the Host controller proceeds with execution of the schedule. The Host controller continues execution as long as this bit is set. When this bit is set to 0, the Host controller completes the current transaction on the USB and then halts. The HCHalted bit in the USB2.0_STS register indicates when the Host controller has finished the transaction and has entered the stopped state. Software should not write a 1 to this field unless the host controller is in the Halted state (that is, HCHalted in the USBSTS register is a 1). The Halted bit is cleared immediately when the Run bit is set. The following table explains how the different combinations of Run and Halted should be interpreted: Run/StopHaltedInterpretation 0 0 Valid- in the process of halting 0 1 Valid- halted 1 0 Valid- running 1 1 Invalid- the HCHalted bit clears immediately. Memory read cycles initiated by the EHC that receive any status other than Successful will result in this bit being cleared.

Note: The Command Register indicates the command to be executed by the serial bus host controller. Writing to the register causes a command to be executed.

17.2.2.2 USB2.0_STS – USB 2.0 Status Register

Offset:	MEM_BASE + 24–27h	Attribute:	R/WC, RO
Default Value:	00001000h	Size:	32 bits

This register indicates pending interrupts and various states of the Host controller. The status resulting from a transaction on the serial bus is not indicated in this register. See the Interrupts description in section 4 of the EHCI specification for additional information concerning USB 2.0 interrupt conditions.

Note: For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 has no effect.

Bit	Description
31:16	Reserved. These bits are reserved and should be set to 0 when writing this register.
15	**Asynchronous Schedule Status** — RO. This bit reports the current real status of the Asynchronous Schedule. 0 = Status of the Asynchronous Schedule is disabled. (Default) 1 = Status of the Asynchronous Schedule is enabled. ***Note:*** The Host controller is not required to *immediately* disable or enable the Asynchronous Schedule when software transitions the *Asynchronous Schedule Enable* bit (D29:F7:CAPLENGTH + 20h, bit 5) in the USB2.0_CMD register. When this bit and the *Asynchronous Schedule Enable* bit are the same value, the Asynchronous Schedule is either enabled (1) or disabled (0).
14	**Periodic Schedule Status** — RO. This bit reports the current real status of the Periodic Schedule. 0 = Status of the Periodic Schedule is disabled. (Default) 1 = Status of the Periodic Schedule is enabled. ***Note:*** The Host controller is not required to *immediately* disable or enable the Periodic Schedule when software transitions the *Periodic Schedule Enable* bit (D29:F7:CAPLENGTH + 20h, bit 4) in the USB2.0_CMD register. When this bit and the *Periodic Schedule Enable* bit are the same value, the Periodic Schedule is either enabled (1) or disabled (0).
13	**Reclamation** — RO. 0=Default. This read-only status bit is used to detect an empty asynchronous schedule. The operational model and valid transitions for this bit are described in Section 4 of the EHCI Specification.
12	**HCHalted** — RO. 0 = This bit is a 0 when the Run/Stop bit is a 1. 1 = The Host controller sets this bit to 1 after it has stopped executing as a result of the Run/Stop bit being set to 0, either by software or by the Host controller hardware (for example, internal error). (Default)
11:6	Reserved
5	**Interrupt on Async Advance –** R/WC. 0=Default. System software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by writing a 1 to the *Interrupt on Async Advance Doorbell* bit (D29:F7:CAPLENGTH + 20h, bit 6) in the USB2.0_CMD register. This bit indicates the assertion of that interrupt source.
4	**Host System Error –** R/WC. 0 = No serious error occurred during a host system access involving the Host controller module 1 = The Host controller sets this bit to 1 when a serious error occurs during a host system access involving the Host controller module. A hardware interrupt is generated to the system. Memory read cycles initiated by the EHC that receive any status other than Successful will result in this bit being set. When this error occurs, the Host controller clears the Run/Stop bit in the USB2.0_CMDregister (D29:F7:CAPLENGTH + 20h, bit 0) to prevent further execution of the scheduled TDs. A hardware interrupt is generated to the system (if enabled in the Interrupt Enable Register).
3	**Frame List Rollover –** R/WC. 0 = No *Frame List Index* rollover from its maximum value to 0. 1 = The Host controller sets this bit to a 1 when the *Frame List Index* (see Section) rolls over from its maximum value to 0. Since the Intel® 631xESB/632xESB I/O Controller Hub only supports the 1024-entry Frame List Size, the *Frame List Index* rolls over every time FRNUM13 toggles.

Bit	Description
2	**Port Change Detect –** R/WC. This bit is allowed to be maintained in the Auxiliary power well. Alternatively, it is also acceptable that on a D3 to D0 transition of the EHCI HC device, this bit is loaded with the OR of all of the PORTSC change bits (including: Force port resume, overcurrent change, enable/disable change and connect status change). Regardless of the implementation, when this bit is readable (that is, in the D0 state), it must provide a valid view of the Port Status registers. 0 = No change bit transition from a 0 to 1 or No Force Port Resume bit transition from 0 to 1 as a result of a J-K transition detected on a suspended port. 1 = The Host controller sets this bit to 1 when any port for which the *Port Owner* bit is set to 0 has a change bit transition from a 0 to 1 or a Force Port Resume bit transition from 0 to 1 as a result of a J-K transition detected on a suspended port.
1	**USB Error Interrupt (USBERRINT) –** R/WC. 0 = No error condition. 1 = The Host controller sets this bit to 1 when completion of a USB transaction results in an error condition (for example, error counter underflow). If the TD on which the error interrupt occurred also had its IOC bit set, both this bit and Bit 0 are set. See the EHCI specification for a list of the USB errors that will result in this interrupt being asserted.
0	**USB Interrupt (USBINT) –** R/WC. 0 = No completion of a USB transaction whose Transfer Descriptor had its IOC bit set. No short packet is detected. 1 = The Host controller sets this bit to 1 when the cause of an interrupt is a completion of a USB transaction whose Transfer Descriptor had its IOC bit set. The Host controller also sets this bit to 1 when a short packet is detected (actual number of bytes received was less than the expected number of bytes).

17.2.2.3 USB2.0_INTR – USB 2.0 Interrupt Enable Register

Offset:	MEM_BASE + 28–2Bh	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

This register enables and disables reporting of the corresponding interrupt to the software. When a bit is set and the corresponding interrupt is active, an interrupt is generated to the host. Interrupt sources that are disabled in this register still appear in the USB2.0_STS Register to allow the software to poll for events. Each interrupt enable bit description indicates whether it is dependent on the interrupt threshold mechanism (see Section 4 of the EHCI specification), or not.

Bit	Description
31:6	Reserved. These bits are reserved and should be 0 when writing this register.
5	**Interrupt on Async Advance Enable –** R/W. 0 = Disable. 1 = Enable. When this bit is a 1, and the Interrupt on Async Advance bit (D29:F7:CAPLENGTH + 24h, bit 5) in the USB2.0_STS register is a 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the Interrupt on Async Advance bit.
4	**Host System Error Enable –** R/W. 0 = Disable. 1 = Enable. When this bit is a 1, and the Host System Error Status bit (D29:F7:CAPLENGTH + 24h, bit 4) in the USB2.0_STS register is a 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Host System Error bit.
3	**Frame List Rollover Enable –** R/W. 0 = Disable. 1 = Enable. When this bit is a 1, and the Frame List Rollover bit (D29:F7:CAPLENGTH + 24h, bit 3) in the USB2.0_STS register is a 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Frame List Rollover bit.

Bit	Description
2	**Port Change Interrupt Enable –** R/W. 0 = Disable. 1 = Enable. When this bit is a 1, and the Port Change Detect bit (D29:F7:CAPLENGTH + 24h, bit 2) in the USB2.0_STS register is a 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Port Change Detect bit.
1	**USB Error Interrupt Enable –** R/W. 0 = Disable. 1 = Enable. When this bit is a 1, and the USBERRINT bit (D29:F7:CAPLENGTH + 24h, bit 1) in the USB2.0_STS register is a 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software by clearing the USBERRINT bit in the USB2.0_STS register.
0	**USB Interrupt Enable –** R/W. 0 = Disable. 1 = Enable. When this bit is a 1, and the USBINT bit (D29:F7:CAPLENGTH + 24h, bit 0) in the USB2.0_STS register is a 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software by clearing the USBINT bit in the USB2.0_STS register.

17.2.2.4 FRINDEX – Frame Index Register

Offset:	MEM_BASE + 2C–2Fh	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

The SOF frame number value for the bus SOF token is derived or alternatively managed from this register. Refer to Section 4 of the EHCI specification for a detailed explanation of the SOF value management requirements on the host controller. The value of FRINDEX must be within 125 µs (1 micro-frame) ahead of the SOF token value. The SOF value may be implemented as an 11-bit shadow register. For this discussion, this shadow register is 11 bits and is named SOFV. SOFV updates every 8 micro-frames. (1 millisecond). An example implementation to achieve this behavior is to increment SOFV each time the FRINDEX[2:0] increments from 0 to 1.

Software must use the value of FRINDEX to derive the current micro-frame number, both for high-speed isochronous scheduling purposes and to provide the **get** micro-frame number function required to client drivers. Therefore, the value of FRINDEX and the value of SOFV must be kept consistent if chip is reset or software writes to FRINDEX. Writes to FRINDEX must also **write-through** FRINDEX[13:3] to SOFV[10:0]. In order to keep the update as simple as possible, software should never write a FRINDEX value where the three least significant bits are 111b or 000b.

Note: This register is used by the host controller to index into the periodic frame list. The register updates every 125 microseconds (once each micro-frame). Bits [12:3] are used to select a particular entry in the Periodic Frame List during periodic schedule execution. The number of bits used for the index is fixed at 10 for the Intel® 631xESB/632xESB I/O Controller Hub since it only supports 1024-entry frame lists. This register must be written as a DWord. Word and byte writes produce undefined results. This register cannot be written unless the Host controller is in the Halted state as indicated by the *HCHalted* bit (D29:F7:CAPLENGTH + 24h, bit 12). A write to this register while the Run/Stop bit (D29:F7:CAPLENGTH + 20h, bit 0) is set to a 1 (USB2.0_CMD register) produces undefined results. Writes to this register also effect the SOF value. See Section 4 of the EHCI specification for details.

Bit	Description
31:14	Reserved
13:0	**Frame List Current Index/Frame Number** – R/W. The value in this register increments at the end of each time frame (for example, micro-frame). Bits [12:3] are used for the Frame List current index. This means that each location of the frame list is accessed 8 times (frames or micro-frames) before moving to the next index.

17.2.2.5 CTRLDSSEGMENT – Control Data Structure Segment Register

Offset: MEM_BASE + 30–33h Attribute: R/W, RO
Default Value: 00000000h Size: 32 bits

This 32-bit register corresponds to the most significant address bits [63:32] for all EHCI data structures. Since the Intel® 631xESB/632xESB I/O Controller Hub hardwires the 64-bit Addressing Capability field in HCCPARAMS to 1, then this register is used with the link pointers to construct 64-bit addresses to EHCI control data structures. This register is concatenated with the link pointer from either the PERIODICLISTBASE, ASYNCLISTADDR, or any control data structure link field to construct a 64-bit address. This register allows the host software to locate all control data structures within the same 4 GB memory segment.

Bit	Description
31:12	Upper Address[63:44] – RO. Hardwired to 0s. The EHC is only capable of generating addresses up to 16 terabytes (44 bits of address).
11:0	Upper Address[43:32] – R/W. This 12-bit field corresponds to address bits 43:32 when forming a control data structure address.

17.2.2.6 PERIODICLISTBASE – Periodic Frame List Base Address Register

Offset: MEM_BASE + 34–37h Attribute: R/W
Default Value: 00000000h Size: 32 bits

This 32-bit register contains the beginning address of the Periodic Frame List in the system memory. Since the Intel® 631xESB/632xESB I/O Controller Hub host controller operates in 64-bit mode (as indicated by the 1 in the 64-bit Addressing Capability field in the HCCSPARAMS register) (offset 08h, bit 0), then the most significant 32 bits of every control data structure address comes from the CTRLDSSEGMENT register. HCD loads this register prior to starting the schedule execution by the Host controller. The memory structure referenced by this physical memory pointer is assumed to be 4-Kbyte aligned. The contents of this register are combined with the Frame Index Register (FRINDEX) to enable the Host controller to step through the Periodic Frame List in sequence.

Bit	Description
31:12	**Base Address (Low)** – R/W. These bits correspond to memory address signals [31:12], respectively.
11:0	Reserved. Must be written as 0's. During runtime, the value of these bits are undefined.

17.2.2.7 ASYNCLISTADDR – Current Asynchronous List Address Register

Offset:	MEM_BASE + 38–3Bh	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

This 32-bit register contains the address of the next asynchronous queue head to be executed. Since the Intel® 631xESB/632xESB I/O Controller Hub host controller operates in 64-bit mode (as indicated by a 1 in 64-bit Addressing Capability field in the HCCPARAMS register) (offset 08h, bit 0), then the most significant 32 bits of every control data structure address comes from the CTRLDSSEGMENT register (offset 08h). Bits [4:0] of this register cannot be modified by system software and will always return 0's when read. The memory structure referenced by this physical memory pointer is assumed to be 32-byte aligned.

Bit	Description
31:5	**Link Pointer Low (LPL)** – R/W. These bits correspond to memory address signals [31:5], respectively. This field may only reference a Queue Head (QH).
4:0	Reserved. These bits are reserved and their value has no effect on operation.

17.2.2.8 CONFIGFLAG – Configure Flag Register

Offset:	MEM_BASE + 60–63h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

This register is in the suspend power well. It is only reset by hardware when the suspend power is initially applied or in response to a host controller reset.

Bit	Description
31:1	Reserved. Read from this field will always return 0.
0	**Configure Flag (CF)** – R/W. Host software sets this bit as the last action in its process of configuring the Host controller. This bit controls the default port-routing control logic. Bit values and side-effects are listed below. See section 4 of the EHCI spec for operation details. 0 = Port routing control logic default-routes each port to the classic host controllers (default). 1 = Port routing control logic default-routes all ports to this host controller.

17.2.2.9 PORTSC – Port N Status and Control Register

Offset:	Port 0: MEM_BASE + 64–67h Port 1: MEM_BASE + 68–6Bh Port 2: MEM_BASE + 6C–6Fh Port 3: MEM_BASE + 70–73h Port 4: MEM_BASE + 74–77h Port 5: MEM_BASE + 78–7Bh Port 6: MEM_BASE + 7C–7Fh Port 7: MEM_BASE + 80–83h		
Attribute:	R/W, R/WC, RO		
Default Value:	00003000h	Size:	32 bits

A host controller must implement one or more port registers. Software uses the N_Port information from the Structural Parameters Register to determine how many ports need to be serviced. All ports have the structure defined below. Software must not write to unreported Port Status and Control Registers.

This register is in the suspend power well. It is only reset by hardware when the suspend power is initially applied or in response to a host controller reset. The initial conditions of a port are:

- No device connected
- Port disabled.

When a device is attached, the port state transitions to the attached state and system software will process this as with any status change notification. Refer to Section 4 of the EHCI specification for operational requirements for how change events interact with port suspend mode.

Bit	Description
31:23	Reserved. These bits are reserved for future use and will return a value of 0's when read.
22	**Wake on Overcurrent Enable (WKOC_E) –** R/W. 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1 enables the setting of the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the overcurrent Active bit (bit 4 of this register) is set.
21	**Wake on Disconnect Enable (WKDSCNNT_E) –** R/W. 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1 enables the setting of the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Current Connect Status changes from connected to disconnected (that is, bit 0 of this register changes from 1 to 0).
20	**Wake on Connect Enable (WKCNNT_E) –** R/W. 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1 enables the setting of the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Current Connect Status changes from disconnected to connected (that is, bit 0 of this register changes from 0 to 1).
19:16	**Port Test Control –** R/W. When this field is 0's, the port is NOT operating in a test mode. A non-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. The encoding of the test mode bits are (0110b – 1111b are reserved): BitsTest Mode 0000bTest mode not enabled (Default) 0001bTest J_STATE 0010bTest K_STATE 0011bTest SE0_NAK 0100bTest Packet 0101bTest FORCE_ENABLE Refer to USB Specification Revision 2.0, Section 7 for details on each test mode.
15:14	Reserved – R/W. Should be written to =00b.
13	**Port Owner –** R/W. Default = 1b. This bit unconditionally goes to a 0 when the Configured Flag bit in the USB2.0_CMD register makes a 0 to 1 transition. System software uses this field to release ownership of the port to a selected host controller (in the event that the attached device is not a high-speed device). Software writes a 1 to this bit when the attached device is not a high-speed device. A 1 in this bit means that a companion host controller owns and controls the port. See Section 4 of the EHCI Specification for operational details.
12	**Port Power (PP)** – RO. Read-only with a value of 1. This indicates that the port does have power.
11:10	**Line Status** – RO.These bits reflect the current logical levels of the D+ (bit 11) and D– (bit 10) signal lines. These bits are used for detection of low-speed USB devices prior to the port reset and enable sequence. This field is valid only when the port enable bit is 0 and the current connect status bit is set to a 1. 00 = SE0 10 = J-state 01 = K-state 11 = Undefined
9	Reserved. This bit will return a 0 when read.

Bit	Description
8	**Port Reset** – R/W. Default = 0. When software writes a 1 to this bit (from a 0), the bus reset sequence as defined in the USB Specification, Revision 2.0 is started. Software writes a 0 to this bit to terminate the bus reset sequence. Software must keep this bit at a 1 long enough to guarantee the reset sequence completes as specified in the USB Specification, Revision 2.0. 1 = Port is in Reset. 0 = Port is not in Reset. ***Note:*** When software writes a 0 to this bit, there may be a delay before the bit status changes to a 0. The bit status will not read as a 0 until after the reset has completed. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (for example, set the *Port Enable* bit to a 1). A host controller must terminate the reset and stabilize the state of the port within 2 milliseconds of software transitioning this bit from 0 to 1. For example: if the port detects that the attached device is high-speed during reset, then the host controller must have the port in the enabled state within 2 ms of software writing this bit to a 0. The HCHalted bit (D29:F7:CAPLENGTH + 24h, bit 12) in the USB2.0_STS register should be a 0 before software attempts to use this bit. The host controller may hold Port Reset asserted to a 1 when the HCHalted bit is a 1. This bit is 0 if Port Power is 0 ***Note:*** System software should not attempt to reset a port if the *HCHalted* bit in the USB2.0_STS register is a 1. Doing so will result in undefined behavior.
7	**Suspend –** R/W. 0 = Port not in suspend state.(Default) 1 = Port in suspend state. Port Enabled Bit and Suspend bit of this register define the port states as follows: Port Enabled, Suspend BitsPort State 0, XDisable 1, 0Enable 1, 1Suspend When in suspend state, downstream propagation of data is blocked on this port, except for port reset. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port depending on the activity on the port. The host controller will unconditionally set this bit to a 0 when software sets the *Force Port Resume* bit to a 0 (from a 1). A write of 0 to this bit is ignored by the host controller. If host software sets this bit to a 1 when the port is not enabled (that is, Port enabled bit is a 0) the results are undefined.
6	**Force Port Resume –** R/W. 0 = No resume (K-state) detected/driven on port. (Default) 1 = Resume detected/driven on port. Software sets this bit to a 1 to drive resume signaling. The Host controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a 1 because a J-to-K transition is detected, the Port Change Detect bit (D29:F7:CAPLENGTH + 24h, bit 2) in the USB2.0_STS register is also set to a 1. If software sets this bit to a 1, the host controller must not set the Port Change Detect bit. ***Note:*** When the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification, Revision 2.0. The resume signaling (Full-speed 'K') is driven on the port as long as this bit remains a 1. Software must appropriately time the Resume and set this bit to a 0 when the appropriate amount of time has elapsed. Writing a 0 (from 1) causes the port to return to high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a 1 until the port has switched to the high-speed idle.
5	**Overcurrent Change –** R/WC. The functionality of this bit is not dependent upon the port owner. Software clears this bit by writing a 1 to it. 0 = No change. (Default) 1 = There is a change to Overcurrent Active.
4	Overcurrent Active **–** RO. 0 = This port does not have an overcurrent condition. (Default) 1 = This port currently has an overcurrent condition. This bit will automatically transition from 1 to 0 when the over current condition is removed. The Intel® 631xESB/632xESB I/O Controller Hub automatically disables the port when the overcurrent active bit is 1.
3	**Port Enable / Disable Change** – R/WC. For the root hub, this bit gets set to a 1 only when a port is disabled due to the appropriate conditions existing at the EOF2 point (See Section 11 of the USB Specification for the definition of a port error). This bit is not set due to the Disabled-to-Enabled transition, nor due to a disconnect. Software clears this bit by writing a 1 to it. 0 = No change in status. (Default). 1 = Port enabled/disabled status has changed.

Bit	Description
2	**Port Enabled/Disabled** – R/W. Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing a 1 to this bit. Ports can be disabled by either a fault condition (disconnect event or other fault condition) or by host software. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events. 0 = Disable 1 = Enable (Default)
1	**Connect Status Change** – R/WC. This bit indicates a change has occurred in the port's Current Connect Status. Software sets this bit to 0 by writing a 1 to it. 0 = No change (Default). 1 = Change in Current Connect Status. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be "setting" an already-set bit (that is, the bit will remain set).
0	**Current Connect Status** – RO. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change bit (Bit 1) to be set. 0 = No device is present. (Default) 1 = Device is present on port.

17.2.3 USB 2.0-Based Debug Port Register

The Debug port's registers are located in the same memory area, defined by the Base Address Register (MEM_BASE), as the standard EHCI registers. The base offset for the debug port registers (A0h) is declared in the Debug Port Base Offset Capability Register at Configuration offset 5Ah (D29:F7:offset 5Ah). The specific EHCI port that supports this debug capability (port 0) is indicated by a 4-bit field (bits 20–23) in the HCSPARAMS register of the EHCI controller. The address map of the Debug Port registers is shown in Table 17-4.

Table 17-4. Debug Port Register Address Map

MEM_BASE + Offset	Mnemonic	Register Name	Default	Type
A0h	CNTL_STS	Control/Status	0000h	R/W, R/WC, RO, WO
A4h	USBPID	USB PIDs	0000h	R/W, RO
A8h	DATABUF[3:0]	Data Buffer (Bytes 3:0)	00000000h	R/W
ACh	DATABUF[7:4]	Data Buffer (Bytes 7:4)	00000000h	R/W
B0h	CONFIG	Configuration	00007F01h	R/W

Notes:
1. All of these registers are implemented in the core well and reset by PLTRST#, EHC HCRESET, and a EHC D3-to-D0 transition.
2. The hardware associated with this register provides no checks to ensure that software programs the interface correctly. How the hardware behaves when programmed illegally is undefined.

17.2.3.1 CNTL_STS – Control/Status Register

Offset: MEM_BASE + A0h Attribute: R/W, R/WC, RO, WO
Default Value: 0000h Size: 32 bits

Bit	Description
31	Reserved

Bit	Description
30	**OWNER_CNT –** R/W. 0 = Ownership of the debug port is NOT forced to the EHCI controller (Default) 1 = Ownership of the debug port is forced to the EHCI controller (that is, immediately taken away from the companion Classic USB Host controller) If the port was already owned by the EHCI controller, then setting this bit has no effect. This bit overrides all of the ownership-related bits in the standard EHCI registers.
29	Reserved
28	**ENABLED_CNT –** R/W. 0 = Software can clear this by writing a 0 to it. The hardware clears this bit for the same conditions where the Port Enable/Disable Change bit (in the PORTSC register) is set. (Default) 1 = Debug port is enabled for operation. Software can directly set this bit if the port is already enabled in the associated PORTSC register (this is enforced by the hardware).
27:17	Reserved
16	**DONE_STS –** R/WC. Software can clear this by writing a 1 to it. 0 = Request Not complete 1 = Set by hardware to indicate that the request is complete.
15:12	LINK_ID_STS – RO. This field identifies the link interface. 0h = Hardwired. Indicates that it is a USB Debug Port.
11	Reserved. This bit returns 0 when read. Writes have no effect.
10	**IN_USE_CNT –** R/W. Set by software to indicate that the port is in use. Cleared by software to indicate that the port is free and may be used by other software. This bit is cleared after reset. (This bit has no affect on hardware.)
9:7	**EXCEPTION_STS –** RO. This field indicates the exception when the ERROR_GOOD#_STS bit is set. This field should be ignored if the ERROR_GOOD#_STS bit is 0. 000 =No Error. (Default) Note: this should not be seen, since this field should only be checked if there is an error. 001 =Transaction error: indicates the USB 2.0 transaction had an error (CRC, bad PID, timeout, and so forth) 010 =Hardware error. Request was attempted (or in progress) when port was suspended or reset. All Other combinations are reserved
6	**ERROR_GOOD#_STS –** RO. 0 = Hardware clears this bit to 0 after the proper completion of a read or write. (Default) 1 = Error has occurred. Details on the nature of the error are provided in the Exception field.
5	**GO_CNT –** WO. 0 = Hardware clears this bit when hardware sets the DONE_STS bit. (Default) 1 = Causes hardware to perform a read or write request. ***Note:*** Writing a 1 to this bit when it is already set may result in undefined behavior.
4	**WRITE_READ#_CNT –** R/W. Software clears this bit to indicate that the current request is a read. Software sets this bit to indicate that the current request is a write. 0 = Read (Default) 1 = Write
3:0	**DATA_LEN_CNT –** R/W. This field is used to indicate the size of the data to be transferred. default = 0h. For write operations, this field is set by software to indicate to the hardware how many bytes of data in Data Buffer are to be transferred to the console. A value of 0h indicates that a zero-length packet should be sent. A value of 1–8 indicates 1–8 bytes are to be transferred. Values 9–Fh are illegal and how hardware behaves if used is undefined. For read operations, this field is set by hardware to indicate to software how many bytes in Data Buffer are valid in response to a read operation. A value of 0h indicates that a zero length packet was returned and the state of Data Buffer is not defined. A value of 1–8 indicates 1–8 bytes were received. Hardware is not allowed to return values 9–Fh. The transferring of data always starts with byte 0 in the data area and moves toward byte 7 until the transfer size is reached.

Notes:
1. Software should do Read-Modify-Write operations to this register to preserve the contents of bits not being modified. This include Reserved bits.
2. To preserve the usage of RESERVED bits in the future, software should always write the same value read from the bit until it is defined. Reserved bits will always return 0 when read.

17.2.3.2 USBPID – USB PIDs Register

Offset:	MEM_BASE + A4h	Attribute:	R/W, RO
Default Value:	0000h	Size:	32 bits

This DWord register is used to communicate PID information between the USB debug driver and the USB debug port. The debug port uses some of these fields to generate USB packets, and uses other fields to return PID information to the USB debug driver.

Bit	Description
31:24	Reserved: These bits will return 0 when read. Writes will have no effect.
23:16	**RECEIVED_PID_STS[23:16]** – RO. Hardware updates this field with the received PID for transactions in either direction. When the controller is writing data, this field is updated with the handshake PID that is received from the device. When the host controller is reading data, this field is updated with the data packet PID (if the device sent data), or the handshake PID (if the device NAKs the request). This field is valid when the hardware clears the GO_DONE#_CNT bit.
15:8	**SEND_PID_CNT[15:8]** – R/W. Hardware sends this PID to begin the data packet when sending data to USB (that is, WRITE_READ#_CNT is asserted). Software typically sets this field to either DATA0 or DATA1 PID values.
7:0	**TOKEN_PID_CNT[7:0]** – R/W. Hardware sends this PID as the Token PID for each USB transaction. Software typically sets this field to either IN, OUT, or SETUP PID values.

17.2.3.3 DATABUF[7:0] – Data Buffer Bytes[7:0] Register

Offset:	MEM_BASE + A8–AFh	Attribute:	R/W
Default Value:	0000000000000000h	Size:	64 bits

This register can be accessed as 8 separate 8-bit registers or 2 separate 32-bit register.

Bit	Description
63:0	**DATABUFFER[63:0]** – R/W. This field is the 8 bytes of the data buffer. Bits 7:0 correspond to least significant byte (byte 0). Bits 63:56 correspond to the most significant byte (byte 7). The bytes in the Data Buffer must be written with data before software initiates a write request. For a read request, the Data Buffer contains valid data when DONE_STS bit (offset A0, bit 16) is cleared by the hardware, ERROR_GOOD#_STS (offset A0, bit 6) is cleared by the hardware, and the DATA_LENGTH_CNT field (offset A0, bits 3:0) indicates the number of bytes that are valid.

17.2.3.4 CONFIG – Configuration Register

Offset:	MEM_BASE + B0–B3h	Attribute:	R/W
Default Value:	00007F01h	Size:	32 bits

Bit	Description
31:15	Reserved
14:8	**USB_ADDRESS_CNF** – R/W. This 7-bit field identifies the USB device address used by the controller for all Token PID generation. (Default = 7Fh)
7:4	Reserved
3:0	**USB_ENDPOINT_CNF** – R/W. This 4-bit field identifies the endpoint used by the controller for all Token PID generation. (Default = 01h)

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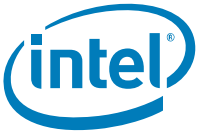


18 PCI-to-PCI Bridge Registers (D30:F0)

The Intel® 631xESB/632xESB I/O Controller Hub PCI bridge resides in PCI Device 30, Function 0 on bus #0. This implements the buffering and control logic between PCI and the backbone. The arbitration for the PCI bus is handled by this PCI device.

18.1 PCI Configuration Registers (D30:F0)

Note: Address locations that are not shown should be treated as Reserved (see Section 2.3 for details).

Table 18-1. PCI Bridge Register Address Map (PCI-PCI – D30:F0)

Offset	Mnemonic	Register Name	Default	Type
00–01h	VID	Vendor Identification	8086h	RO
02–03h	DID	Device Identification	244Eh	RO
04–05h	PCICMD	PCI Command	0000h	R/W, RO
06–07h	PSTS	PCI Status	0010h	R/WC, RO
08h	RID	Revision Identification	See register description.	RO
09-0Bh	CC	Class Code	060401h	RO
0Dh	PMLT	Primary Master Latency Timer	00h	RO
0Eh	HEADTYP	Header Type	01h	RO
18-1Ah	BNUM	Bus Number	000000h	R/W, RO
1Bh	SMLT	Secondary Master Latency Timer	00h	R/W, RO
1C-1Dh	IOBASE_LIMIT	I/O Base and Limit	0000h	R/W, RO
1E–1Fh	SECSTS	Secondary Status	0280h	R/WC, RO
20–23h	MEMBASE_LIMIT	Memory Base and Limit	00000000h	R/W, RO
24–27h	PREF_MEM_BASE_LIMIT	Prefetchable Memory Base and Limit	00010001h	R/W, RO
28–2Bh	PMBU32	Prefetchable Memory Upper 32 Bits	00000000h	R/W
2C–2Fh	PMLU32	Prefetchable Memory Limit Upper 32 Bits	00000000h	R/W
34h	CAPP	Capability List Pointer	50h	RO
3C-3Dh	INTR	Interrupt Information	0000h	R/W, RO
3E–3Fh	BCTRL	Bridge Control	0000h	R/WC, RO
40–41h	SPDH	Secondary PCI Device Hiding	00h	R/W, RO
44-47h	DTC	Delayed Transaction Control	00000000h	R/W, RO
48-4B	DTS	Bridge Proprietary Status	00000000h	R/WC, RO
4C-4F	BPC	Bridge Policy Configuration	40000000h	R/W RO
50–51h	SVCAP	Subsystem Vendor Capability Pointer	000Dh	RO
54-57	SVID	Subsystem Vendor IDs	00000000	R/WO

18.1.1 VID – Vendor Identification Register (PCI-PCI – D30:F0)

Offset Address: 00–01h
Default Value: 8086h
Attribute: RO
Size: 16 bits

Bit	Description
15:0	Vendor ID – RO. This is a 16-bit value assigned to Intel. Intel VID = 8086h.

18.1.2 DID – Device Identification Register (PCI-PCI – D30:F0)

Offset Address: 02–03h
Default Value: 244Eh
Attribute: RO
Size: 16 bits

Bit	Description
15:0	Device ID – RO.This is a 16-bit value assigned to the PCI bridge.

18.1.3 PCICMD – PCI Command (PCI-PCI – D30:F0)

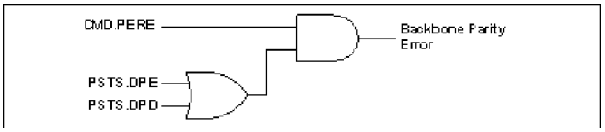
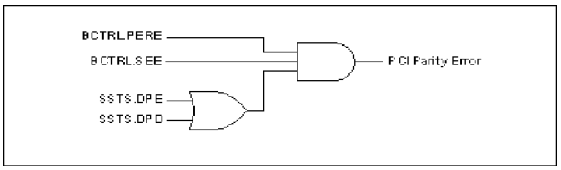
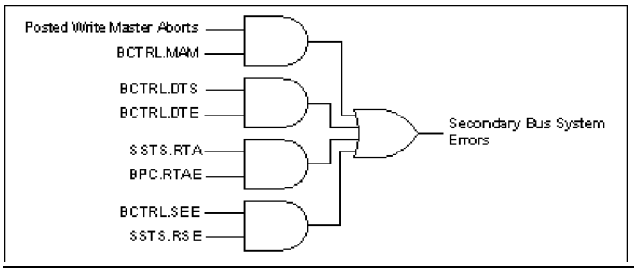
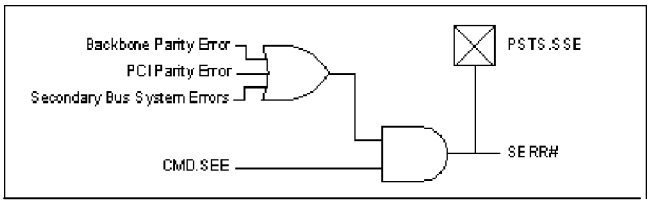
Offset Address: 04–05h
Default Value: 0000h
Attribute: R/W, RO
Size: 16 bits

Bit	Description
15:11	Reserved
10	Interrupt Disable (ID) – RO. Hardwired to 0. The PCI bridge has no interrupts to disable
9	Fast Back to Back Enable (FBE) – RO. Hardwired to 0, per the PCI Express* Specification.
8	**SERR# Enable (SERR_EN)** – R/W. 0 = Disable. 1 = Enable the Intel® 631xESB/632xESB I/O Controller Hub to generate an NMI (or SMI# if NMI routed to SMI#) when the D30:F0 SSE bit (offset 06h, bit 14) is set.
7	Wait Cycle Control (WCC) – RO. Hardwired to 0, per the PCI Express Specification.
6	Parity Error Response (PER) – R/W. 0 = The Intel® 631xESB/632xESB I/O Controller Hub ignores parity errors on the PCI bridge. 1 = The Intel® 631xESB/632xESB I/O Controller Hub will set the SSE bit (D30:F0, offset 06h, bit 14) when parity errors are detected on the PCI bridge.
5	VGA Palette Snoop (VPS) – RO. Hardwired to 0, per the PCI Express Specification.
4	Memory Write and Invalidate Enable (MWE) – RO. Hardwired to 0, per the PCI Express Specification.
3	Special Cycle Enable (SCE) – RO. Hardwired to 0, per the PCI Express Specification and the PCI-to-PCI Bridge Specification.
2	**Bus Master Enable (BME) –** R/W. 0 = Disable 1 = Enable. Allows the PCI-to-PCI bridge to accept cycles from PCI.
1	**Memory Space Enable (MSE)** – R/W. Controls the response as a target for memory cycles targeting PCI. 0 = Disable 1 = Enable
0	**I/O Space Enable (IOSE) –** R/W. Controls the response as a target for I/O cycles targeting PCI. 0 = Disable 0 = Enable

18.1.4 PSTS – PCI Status Register (PCI-PCI – D30:F0)

Offset Address:	06–07h	Attribute:	R/WC, RO
Default Value:	0010h	Size:	16 bits

Note: For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 to the bit has no effect.

Bit	Description
15	**Detected Parity Error (DPE) –** R/WC. 0 = Parity error Not detected. 1 = Indicates that the Intel® 631xESB/632xESB I/O Controller Hub detected a parity error on the internal backbone. This bit gets set even if the Parity Error Response bit (D30:F0:04 bit 6) is not set.
14	**Signaled System Error (SSE)** – R/WC. Several internal and external sources of the bridge can cause SERR#. The first class of errors is parity errors related to the backbone. The PCI bridge captures generic data parity errors (errors it finds on the backbone) as well as errors returned on backbone cycles where the bridge was the master. If either of these two conditions is met, and the primary side of the bridge is enabled for parity error response, SERR# will be captured as shown below.  As with the backbone, the PCI bus captures the same sets of errors. The PCI bridge captures generic data parity errors (errors it finds on PCI) as well as errors returned on PCI cycles where the bridge was the master. If either of these two conditions is met, and the secondary side of the bridge is enabled for parity error response, SERR# will be captured as shown below.  The final class of errors is system bus errors. There are three status bits associated with system bus errors, each with a corresponding enable. The diagram capturing this is shown below.  After checking for the three above classes of errors, an SERR# is generated, and PSTS.SSE logs the generation of SERR#, if CMD.SEE (D30:F0:04, bit 8) is set, as shown below. 
13	**Received Master Abort (RMA) –** R/WC. 0 = No master abort received. 1 = Set when the bridge receives a master abort status from the backbone.
12	**Received Target Abort (RTA)** – R/WC. 0 = No target abort received. 1 = Set when the bridge receives a target abort status from the backbone.

Bit	Description
11	**Signaled Target Abort (STA)** – R/WC. 0 = No signaled target abort 1 = Set when the bridge generates a completion packet with target abort status on the backbone.
10:9	Reserved.
8	**Data Parity Error Detected (DPD) –** R/WC. 0 = Data parity error Not detected. 1 = Set when the bridge receives a completion packet from the backbone from a previous request, and detects a parity error, and CMD.PERE is set (D30:F0:04 bit 6).
7:5	Reserved.
4	Capabilities List (CLIST) – RO. Hardwired to 1. Capability list exist on the PCI bridge.
3	Interrupt Status (IS) – RO. Hardwired to 0. The PCI bridge does not generate interrupts.
2:0	Reserved

18.1.5 RID – Revision Identification Register (PCI-PCI – D30:F0)

Offset Address: 08h Attribute: RO
Default Value: See bit description Size: 8 bits

Bit	Description
7:0	**Revision ID –** RO. Refer to Table 2-33 or the *Intel® 631xESB/632xESB I/O Controller Hub EDS Specification Update - NDA* for the value of the Revision ID Register

18.1.6 CC – Class Code Register (PCI-PCI – D30:F0)

Offset Address: 09-0Bh Attribute: RO
Default Value: 060401h Size: 32 bits

Bit	Description
23:16	Base Class Code (BCC) – RO. Hardwired to 06h. Indicates this is a bridge device.
15:8	Sub Class Code (SCC) – RO. Hardwired to 04h. Indicates this device is a PCI-to-PCI bridge.
7:0	Programming Interface (PI) – RO. Hardwired to 01h. Indicates the bridge is subtractive decode

18.1.7 PMLT – Primary Master Latency Timer Register (PCI-PCI – D30:F0)

Offset Address: 0Dh Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Description
7:3	Master Latency Timer Count (MLTC) – RO. Reserved per the PCI Express specification.
2:0	Reserved

18.1.8 HEADTYP – Header Type Register (PCI-PCI – D30:F0)

Offset Address: 0Eh
Default Value: 81h
Attribute: RO
Size: 8 bits

Bit	Description
7	Multi-Function Device (MFD) – RO. The value reported here depends upon the state of the AC '97 function hide (FD) register (Chipset Config Registers:Offset 3418h), per the following table: FD.AADFD.AMDMFD 0 0 1 0 1 1 1 0 1 1 1 0
6:0	Header Type (HTYPE) – RO. This 7-bit field identifies the header layout of the configuration space, which is a PCI-to-PCI bridge in this case.

18.1.9 BNUM – Bus Number Register (PCI-PCI – D30:F0)

Offset Address: 18-1Ah
Default Value: 000000h
Attribute: R/W, RO
Size: 24 bits

Bit	Description
23:16	Subordinate Bus Number (SBBN) – R/W. Indicates the highest PCI bus number below the bridge.
15:8	Secondary Bus Number (SCBN) – R/W. Indicates the bus number of PCI.
7:0	Primary Bus Number (PBN) – RO. Hardwired to 00h for legacy software compatibility.

18.1.10 SMLT – Secondary Master Latency Timer Register (PCI-PCI – D30:F0)

Offset Address: 1Bh
Default Value: 00h
Attribute: R/W, RO
Size: 8 bits

This timer controls the amount of time the Intel® 631xESB/632xESB I/O Controller Hub PCI-to-PCI bridge will burst data on its secondary interface. The counter starts counting down from the assertion of FRAME#. If the grant is removed, then the expiration of this counter will result in the de-assertion of FRAME#. If the grant has not been removed, then the Intel® 631xESB/632xESB I/O Controller Hub PCI-to-PCI bridge may continue ownership of the bus.

Bit	Description
7:3	**Master Latency Timer Count (MLTC) –** R/W. This 5-bit field indicates the number of PCI clocks, in 8-clock increments, that the Intel® 631xESB/632xESB I/O Controller Hub remains as master of the bus.
2:0	Reserved

18.1.11 IOBASE_LIMIT – I/O Base and Limit Register (PCI-PCI – D30:F0)

Offset Address: 1C-1Dh
Default Value: 0000h
Attribute: R/W, RO
Size: 16 bits

Bit	Description
15:12	**I/O Limit Address Limit bits**[15:12] – R/W. I/O Base bits corresponding to address lines 15:12 for 4-KB alignment. Bits 11:0 are assumed to be padded to FFFh.
11:8	II/O Limit Address Capability (IOLC) – RO. Indicates that the bridge does not support 32-bit I/O addressing.
7:4	**II/O Base Address (IOBA)** – R/W. I/O Base bits corresponding to address lines 15:12 for 4-KB alignment. Bits 11:0 are assumed to be padded to 000h.
3:0	II/O Base Address Capability (IOBC) – RO. Indicates that the bridge does not support 32-bit I/O addressing.

18.1.12 SECSTS – Secondary Status Register (PCI-PCI – D30:F0)

Offset Address: 1E–1Fh
Default Value: 0280h
Attribute: R/WC, RO
Size: 16 bits

Note: For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 to the bit has no effect.

Bit	Description
15	**Detected Parity Error (DPE)** – R/WC. 0 = Parity error **not** detected. 1 = Intel® 631xESB/632xESB I/O Controller Hub PCI bridge detected an address or data parity error on the PCI bus
14	**Received System Error** (R**SE) –** R/WC. 0 = SERR# assertion **not** received 1 = SERR# assertion is received on PCI.
13	**Received Master Abort (RMA) –** R/WC. 0 = No master abort. 1 = This bit is set whenever the bridge is acting as an initiator on the PCI bus and the cycle is master-aborted. For (G)MCH/Intel® 631xESB/632xESB I/O Controller Hub interface packets that have completion required, this must also cause a target abort to be returned and sets PSTS.STA. (D30:F0:06 bit 11)
12	**Received Target Abort (RTA)** – R/WC. 0 = No target abort. 1 = This bit is set whenever the bridge is acting as an initiator on PCI and a cycle is target-aborted on PCI. For (G)MCH/Intel® 631xESB/632xESB I/O Controller Hub interface packets that have completion required, this event must also cause a target abort to be returned, and sets PSTS.STA. (D30:F0:06 bit 11).
11	**Signaled Target Abort (STA) –** R/WC. 0 = No target abort. 1 = This bit is set when the bridge is acting as a target on the PCI Bus and signals a target abort.
10:9	DEVSEL# Timing (DEVT) – RO. 01h = Medium decode timing.
8	**Data Parity Error Detected (DPD)** – R/WC. 0 = Conditions described below **not** met. 1 = The Intel® 631xESB/632xESB I/O Controller Hub sets this bit when all of the following three conditions are met: • The bridge is the initiator on PCI. • PERR# is detected asserted or a parity error is detected internally • BCTRL.PERE (D30:F0:3E bit 0) is set.
7	Fast Back to Back Capable (FBC) – RO. Hardwired to 1 to indicate that the PCI to PCI target logic is capable of receiving fast back-to-back cycles.

Bit	Description
6	Reserved
5	66 MHz Capable (66MHZ_CAP) – RO. Hardwired to 0. This bridge is 33 MHz capable only.
4:0	Reserved

18.1.13 MEMBASE_LIMIT – Memory Base and Limit Register (PCI-PCI – D30:F0)

Offset Address: 20–23h Attribute: R/W, RO
Default Value: 00000000h Size: 32 bits

This register defines the base and limit, aligned to a 1-MB boundary, of the non-prefetchable memory area of the bridge. Accesses that are within the ranges specified in this register will be sent to PCI if CMD.MSE is set. Accesses from PCI that are outside the ranges specified will be accepted by the bridge if CMD.BME is set.

Bit	Description
31-20	**Memory Limit** (ML) – R/W. These bits are compared with bits 31:20 of the incoming address to determine the upper 1-MB aligned value (exclusive) of the range. The incoming address must be less than this value.
19-16	Reserved
15:4	**Memory Base** (MB) – R/W. These bits are compared with bits 31:20 of the incoming address to determine the lower 1-MB aligned value (inclusive) of the range. The incoming address must be greater than or equal to this value.
3:0	Reserved

18.1.14 PREF_MEM_BASE_LIMIT – Prefetchable Memory Base and Limit Register (PCI-PCI – D30:F0)

Offset Address: 24–27h Attribute: R/W, RO
Default Value: 00010001h Size: 32-bit

Defines the base and limit, aligned to a 1-MB boundary, of the prefetchable memory area of the bridge. Accesses that are within the ranges specified in this register will be sent to PCI if CMD.MSE is set. Accesses from PCI that are outside the ranges specified will be accepted by the bridge if CMD.BME is set.

Bit	Description
31-20	**Prefetchable Memory Limit (PML) –** R/W. These bits are compared with bits 31:20 of the incoming address to determine the upper 1-MB aligned value (exclusive) of the range. The incoming address must be less than this value.
19-16	64-bit Indicator (I64L) – RO. Indicates support for 64-bit addressing.
15:4	**Prefetchable Memory Base (PMB) –** R/W. These bits are compared with bits 31:20 of the incoming address to determine the lower 1-MB aligned value (inclusive) of the range. The incoming address must be greater than or equal to this value.
3:0	**64-bit Indicator (I64B) –** RO. Indicates support for 64-bit addressing.

18.1.15 PMBU32 – Prefetchable Memory Base Upper 32 Bits Register (PCI-PCI – D30:F0)

Offset Address: 28–2Bh
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

Bit	Description
31:0	**Prefetchable Memory Base Upper Portion (PMBU)** – R/W. Upper 32-bits of the prefetchable address base.

18.1.16 PMLU32 – Prefetchable Memory Limit Upper 32 Bits Register (PCI-PCI – D30:F0)

Offset Address: 2C–2Fh
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

Bit	Description
31:0	**Prefetchable Memory Limit Upper Portion (PMLU)** – R/W. Upper 32-bits of the prefetchable address limit.

18.1.17 CAPP – Capability List Pointer Register (PCI-PCI – D30:F0)

Offset Address: 34h
Default Value: 50h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Capabilities Pointer (PTR)** – RO. Indicates that the pointer for the first entry in the capabilities list is at 50h in configuration space.

18.1.18 INTR – Interrupt Information Register (PCI-PCI – D30:F0)

Offset Address: 3C–3Dh
Default Value: 0000h
Attribute: R/W, RO
Size: 16 bits

Bit	Description
15:8	**Interrupt Pin (IPIN)** – RO. The PCI bridge does not assert an interrupt.
7:0	**Interrupt Line (ILINE)** – R/W. Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register. Since the bridge does not generate an interrupt, BIOS should program this value to FFh as per the PCI bridge specification.

18.1.19 BCTRL – Bridge Control Register (PCI-PCI – D30:F0)

Offset Address: 3E–3Fh
Default Value: 0000h
Attribute: R/WC, RO
Size: 16 bits

Bit	Description
15:12	Reserved
11	**Discard Timer SERR# Enable (DTE**) – R/W. Controls the generation of SERR# on the primary interface in response to the DTS bit being set: 0 = Do not generate SERR# on a secondary timer discard 1 = Generate SERR# in response to a secondary timer discard
10	**Discard Timer Status (DTS) –** R/WC. This bit is set to 1 when the secondary discard timer (see the SDT bit below) expires for a delayed transaction in the hard state.

Bit	Description
9	**Secondary Discard Timer (SDT)** – R/W. This bit sets the maximum number of PCI clock cycles that the Intel® 631xESB/632xESB I/O Controller Hub waits for an initiator on PCI to repeat a delayed transaction request. The counter starts once the delayed transaction data is has been returned by the system and is in a buffer in the Intel® 631xESB/632xESB I/O Controller Hub PCI bridge. If the master has not repeated the transaction at least once before the counter expires, the Intel® 631xESB/632xESB I/O Controller Hub PCI bridge discards the transaction from its queue. 0 = The PCI master timeout value is between 2^{15} and 2^{16} PCI clocks 1 = The PCI master timeout value is between 2^{10} and 2^{11} PCI clocks
8	**Primary Discard Timer (PDT**) – R/W. This bit is R/W for software compatibility only.
7	Fast Back to Back Enable (FBE) – RO. Hardwired to 0. The PCI logic will not generate fast back-to-back cycles on the PCI bus.
6	**Secondary Bus Reset (SBR) –** R/W. Controls PCIRST# assertion on PCI. 0 = Bridge de-asserts PCIRST# 1 = Bridge asserts PCIRST#. When PCIRST# is asserted, the delayed transaction buffers, posting buffers, and the PCI bus are initialized back to reset conditions. The rest of the part and the configuration registers are not affected.
5	**Master Abort Mode (MAM**) – R/W. Controls the Intel® 631xESB/632xESB I/O Controller Hub PCI bridge's behavior when a master abort occurs: Master Abort on (G)MCH/Intel® 631xESB/632xESB I/O Controller Hub Interconnect (ESI): 0 = Bridge asserts TRDY# on PCI. It drives all 1's for reads, and discards data on writes. 1 = Bridge returns a target abort on PCI. Master Abort PCI (non-locked cycles): 0 = Normal completion status will be returned on the (G)MCH/Intel® 631xESB/632xESB I/O Controller Hub interconnect. 1 = Target abort completion status will be returned on the (G)MCH/Intel® 631xESB/632xESB I/O Controller Hub interconnect. ***Note:*** All locked reads will return a completer abort completion status on the (G)MCH/ Intel® 631xESB/632xESB I/O Controller Hub interconnect.
4	**VGA 16-Bit Decode (V16D) –** R/W. Enables the Intel® 631xESB/632xESB I/O Controller Hub PCI bridge to provide 16-bits decoding of VGA I/O address precluding the decode of VGA alias addresses every 1 KB. This bit requires the VGAE bit in this register be set.
3	**VGA Enable (VGAE)** – R/W. When set to a 1, the Intel® 631xESB/632xESB I/O Controller Hub PCI bridge forwards the following transactions to PCI regardless of the value of the I/O base and limit registers. The transactions are qualified by CMD.MSE (D30:F0:04 bit 1) and CMD.IOSE (D30:F0:04 bit 0) being set. • Memory addresses: 000A0000h-000BFFFFh • I/O addresses: 3B0h-3BBh and 3C0h-3DFh. For the I/O addresses, bits [63:16] of the address must be 0, and bits [15:10] of the address are ignored (that is, aliased). The same holds true from secondary accesses to the primary interface in reverse. That is, when the bit is 0, memory and I/O addresses on the secondary interface between the above ranges will be claimed.
2	**ISA Enable (IE)** – R/W. This bit only applies to I/O addresses that are enabled by the I/O Base and I/O Limit registers and are in the first 64 KB of PCI I/O space. If this bit is set, the Intel® 631xESB/ 632xESB I/O Controller Hub PCI bridge will block any forwarding from primary to secondary of I/O transactions addressing the last 768 bytes in each 1-KB block (offsets 100h to 3FFh).
1	**SERR# Enable (SEE) –** R/W. Controls the forwarding of secondary interface SERR# assertions on the primary interface. When set, the PCI bridge will forward SERR# pin. • SERR# is asserted on the secondary interface. • This bit is set. • CMD.SEE (D30:F0:04 bit 8) is set.
0	Parity Error Response Enable (PERE) – R/W. 0 = Disable 1 = The Intel® 631xESB/632xESB I/O Controller Hub PCI bridge is enabled for parity error reporting based on parity errors on the PCI bus.

18.1.20 SPDH – Secondary PCI Device Hiding Register (PCI-PCI – D30:F0)

Offset Address: 40–41h
Default Value: 00h
Attribute: R/W, RO
Size: 16 bits

This register allows software to hide the PCI devices, either plugged into slots or on the motherboard.

Bit	Description
15:8	Reserved
7	**Hide Device 7 (HD7)** – R/W, RO. Same as bit 0 of this register, except for device 7 (AD[23])
6	**Hide Device 6 (HD6) –** R/W, RO. Same as bit 0 of this register, except for device 6 (AD[22])
5	**Hide Device 5** (HD5) – R/W, RO. Same as bit 0 of this register, except for device 5 (AD[21])
4	**Hide Device 4 (**HD4) – R/W, RO. Same as bit 0 of this register, except for device 4 (AD[20])
3	Hide Device 3 (HD3) – R/W, RO. Same as bit 0 of this register, except for device 3 (AD[19])
2	**Hide Device 2 (HD2) –** R/W, RO. Same as bit 0 of this register, except for device 2 (AD[18])
1	**Hide Device 1 (HD1)** – R/W, RO. Same as bit 0 of this register, except for device 1 (AD[17])
0	**Hide Device 0 (HD0) –** R/W, RO. 0 = The PCI configuration cycles for this slot are not affected. 1 = Intel® 631xESB/632xESB I/O Controller Hub hides device 0 on the PCI bus. This is done by masking the IDSEL (keeping it low) for configuration cycles to that device. Since the device will not see its IDSEL go active, it will not respond to PCI configuration cycles and the processor will think the device is not present. AD[16] is used as IDSEL for device 0.

18.1.21 DTC – Delayed Transaction Control Register (PCI-PCI – D30:F0)

Offset Address: 44–47h
Default Value: 00000000h
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31	Discard Delayed Transactions (DDT) – R/W. 0 = Logged delayed transactions are kept. 1 = The Intel® 631xESB/632xESB I/O Controller Hub PCI bridge will discard any delayed transactions it has logged. This includes transactions in the pending queue, and any transactions in the active queue, whether in the hard or soft DT state. The prefetchers will be disabled and return to an idle state. ***Notes:*** If a transaction is running on PCI at the time this bit is set, that transaction will continue until either the PCI master disconnects (by de-asserting FRAME#) or the PCI bridge disconnects (by asserting STOP#). This bit is cleared by the PCI bridge when the delayed transaction queues are empty and have returned to an idle state. Software sets this bit and polls for its completion
30	Block Delayed Transactions (BDT) – R/W. 0 = Delayed transactions accepted 1 = The Intel® 631xESB/632xESB I/O Controller Hub PCI bridge will not accept incoming transactions which will result in delayed transactions. It will blindly retry these cycles by asserting STOP#. All postable cycles (memory writes) will still be accepted.
29: 8	Reserved
7: 6	Maximum Delayed Transactions (MDT) – R/W. Controls the maximum number of delayed transactions that the Intel® 631xESB/632xESB I/O Controller Hub PCI bridge will run. Encodings are: 00 =) 2 Active, 5 pending 01 =) 2 active, no pending 10 =) 1 active, no pending 11 =) Reserved

Bit	Description
5	Reserved
4	**Auto Flush After Disconnect Enable (AFADE)** – R/W. 0 = The PCI bridge will retain any fetched data until required to discard by producer/consumer rules. 1 = The PCI bridge will flush any prefetched data after either the PCI master (by de-asserting FRAME#) or the PCI bridge (by asserting STOP#) disconnects the PCI transfer.
3	**Never Prefetch (NP)** – R/W. 0 = Prefetch enabled 1 = The Intel® 631xESB/632xESB I/O Controller Hub will only fetch a single DW and will not enable prefetching, regardless of the command being an Memory read (MR), Memory read line (MRL), or Memory read multiple (MRM).
2	**Memory Read Multiple Prefetch Disable (MRMPD): –** R/W. 0 = MRM commands will fetch multiple cache lines as defined by the prefetch algorithm. 1 = Memory read multiple (MRM) commands will fetch only up to a single, 64-byte aligned cache line.
1	**Memory Read Line Prefetch Disable (MRLPD): –** R/W. 0 = MRL commands will fetch multiple cache lines as defined by the prefetch algorithm. 1 = Memory read line (MRL) commands will fetch only up to a single, 64-byte aligned cache line.
0	**Memory Read Prefetch Disable (MRPD): –** R/W. 0 = MR commands will fetch up to a 64-byte aligned cache line. 1 = Memory read (MR) commands will fetch only a single DW.

18.1.22 BPS – Bridge Proprietary Status Register (PCI-PCI – D30:F0)

Offset Address: 48–4Bh
Default Value: 00000000h
Attribute: R/WC, RO
Size: 32 bits

Bit	Description
31:17	Reserved
16	**PERR# Assertion Detected (PAD)** – R/WC. This bit is set by hardware whenever the PERR# pin is asserted on the rising edge of PCI clock. This includes cases in which the chipset is the agent driving PERR#. It remains asserted until cleared by software writing a 1 to this location. When enabled by the PERR#-to-SERR# Enable bit (in the Bridge Policy Configuration register), a 1 in this bit can generate an internal SERR# and be a source for the NMI logic. This bit can be used by software to determine the source of a system problem.
15:7	Reserved
6:4	**Number of Pending Transactions (NPT) –** RO. This read-only indicator tells debug software how many transactions are in the pending queue. Possible values are: 000 = No pending transaction 001 = 1 pending transaction 010 = 2 pending transactions 011 = 3 pending transactions 100 = 4 pending transactions 101 = 5 pending transactions 110 - 111 = Reserved ***Note:*** This field is not valid if DTC.MDT (offset 44h:bits 7:6) is any value other than '00'.
3:2	Reserved
1:0	**Number of Active Transactions (NAT) –** RO. This read-only indicator tells debug software how many transactions are in the active queue. Possible values are: 00 = No active transactions 01 = 1 active transaction 10 = 2 active transactions 11 = Reserved

18.1.23 BPC – Bridge Policy Configuration Register (PCI-PCI – D30:F0)

Offset Address: 4C–4Fh
Default Value: 00000000h
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31:7	Reserved
6	**PERR#-to-SERR# Enable (PSE)** – R/W. When this bit is set, a 1 in the PERR# Assertion status bit (in the Bridge Proprietary Status register) will result in an internal SERR# assertion on the primary side of the bridge (if also enabled by the SERR# Enable bit in the primary Command register). SERR# is a source of NMI.
5	**Secondary Discard Timer Testmode (SDTT) –** R/W. 0 = The secondary discard timer expiration will be defined in BCTRL.SDT (D30:F0:3E, bit 9) 1 = The secondary discard timer will expire after 128 PCI clocks.
4:3	Reserved
2:1	Reserved
0	**Received Target Abort SERR# Enable (RTAE)** – R/W. When set, the PCI bridge will report SERR# when PSTS.RTA (D30:F0:06 bit 12) or SSTS.RTA (D30:F0:1E bit 12) are set, and CMD.SEE (D30:F0:04 bit 8) is set.

18.1.24 SVCAP – Subsystem Vendor Capability Register (PCI-PCI – D30:F0)

Offset Address: 50–51h
Default Value: 000Dh
Attribute: RO
Size: 16 bits

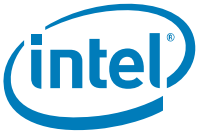
Bit	Description
15:8	**Next Capability (NEXT) –** RO. Value of 00h indicates this is the last item in the list.
7:0	**Capability Identifier (CID) –** RO. Value of 0Dh indicates this is a PCI bridge subsystem vendor capability.

18.1.25 SVID – Subsystem Vendor IDs Register (PCI-PCI – D30:F0)

Offset Address: 54–57h
Default Value: 00000000h
Attribute: R/WO
Size: 32 bits

Bit	Description
31:16	**Subsystem Identifier (SID) –** R/WO. Indicates the subsystem as identified by the vendor. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).
15:0	**Subsystem Vendor Identifier (SVID) –** R/WO. Indicates the manufacturer of the subsystem. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).

§



19 AC'97 Audio Controller Registers (D30:F2)

19.1 AC'97 Audio PCI Configuration Space (Audio – D30:F2)

Note: Registers that are not shown should be treated as Reserved.

Table 19-1. AC '97 Audio PCI Register Address Map (Audio – D30:F2)

Offset	Mnemonic	Register Name	Default	Access
00–01h	VID	Vendor Identification	8086h	RO
02–03h	DID	Device Identification	2698h	RO
04–05h	PCICMD	PCI Command	0000	R/W, RO
06–07h	PCISTS	PCI Status	0280h	R/WC, RO
08h	RID	Revision Identification	See register description	RO
09h	PI	Programming Interface	00	RO
0Ah	SCC	Sub Class Code	01h	RO
0Bh	BCC	Base Class Code	04h	RO
0Eh	HEADTYP	Header Type	00h	RO
10–13h	NAMBBAR	Native Audio Mixer Base Address	00000001h	R/W, RO
14–17h	NAMMBAR	Native Audio Bus Mastering Base Address	00000001h	R/W, RO
18–1Bh	MMBAR	Mixer Base Address (Mem)	00000000h	R/W, RO
1C–1Fh	MBBAR	Bus Master Base Address (Mem)	00000000h	R/W, RO
2C–2Dh	SVID	Subsystem Vendor Identification	0000h	R/WO
2E–2Fh	SID	Subsystem Identification	0000h	R/WO
34h	CAP_PTR	Capabilities Pointer	50h	RO
3Ch	INT_LN	Interrupt Line	00h	R/W
3Dh	INT_PN	Interrupt Pin	See register description	RO
40h	PCID	Programmable Codec ID	09h	R/W
41h	CFG	Configuration	00h	R/W
50–51h	PID	PCI Power Management Capability ID	0001h	RO
52–53h	PC	PC -Power Management Capabilities	C9C2h	RO
54–55h	PCS	Power Management Control and Status	0000h	R/W, R/WC

Note: Internal reset as a result of $D3_{HOT}$ to D0 transition will reset all the core well registers except the following BIOS programmed registers as BIOS may not be invoked following the D3-to-D0 transition. All resume well registers will not be reset by the $D3_{HOT}$ to D0 transition.

Core well registers **not** reset by the $D3_{HOT}$ to D0 transition:

- offset 2Ch–2Dh – Subsystem Vendor ID (SVID)
- offset 2Eh–2Fh – Subsystem ID (SID)
- offset 40h – Programmable Codec ID (PCID)
- offset 41h – Configuration (CFG)

Resume well registers **will not** be reset by the $D3_{HOT}$ to D0 transition:

- offset 54h–55h – Power Management Control and Status (PCS)
- Bus Mastering Register: Global Status Register, bits 17:16
- Bus Mastering Register: SDATA_IN MAP register, bits 7:3

19.1.1 VID – Vendor Identification Register (Audio – D30:F2)

Offset:	00–01h	Attribute:	RO
Default Value:	8086h	Size:	16 Bits
Lockable:	No	Power Well:	Core

Bit	Description
15:0	Vendor ID. This is a 16-bit value assigned to Intel.

19.1.2 DID – Device Identification Register (Audio – D30:F2)

Offset:	02–03h	Attribute:	RO
Default Value:	2698h	Size:	16 Bits
Lockable:	No	Power Well:	Core

Bit	Description
15:0	Device ID.

19.1.3 PCICMD – PCI Command Register (Audio – D30:F2)

Address Offset:	04–05h	Attribute:	R/W, RO
Default Value:	0000h	Size:	16 bits
Lockable:	No	Power Well:	Core

PCICMD is a 16-bit control register. Refer to the PCI 2.3 specification for complete details on each bit.

Bit	Description
15:11	Reserved. Read 0.
10	**Interrupt Disable (ID) –** R/W. 0 = The INTx# signals may be asserted and MSIs may be generated. 1 = The AC '97 controller's INTx# signal will be de-asserted and it may not generate MSIs.
9	Fast Back to Back Enable (FBE) – RO. Not implemented. Hardwired to 0.
8	SERR# Enable (SERR_EN) – RO. Not implemented. Hardwired to 0.
7	Wait Cycle Control (WCC) – RO. Not implemented. Hardwired to 0.
6	Parity Error Response (PER) – RO. Not implemented. Hardwired to 0.
5	VGA Palette Snoop (VPS). Not implemented. Hardwired to 0.
4	Memory Write and Invalidate Enable (MWIE) – RO. Not implemented. Hardwired to 0.
3	Special Cycle Enable (SCE). Not implemented. Hardwired to 0.

2	**Bus Master Enable (BME)** – R/W. Controls standard PCI bus mastering capabilities. 0 = Disable 1 = Enable
1	**Memory Space Enable (MSE) –** R/W. Enables memory space addresses to the AC'97 Audio controller. 0 = Disable 1 = Enable
0	**I/O Space Enable (IOSE)** – R/W. This bit controls access to the AC'97 Audio controller I/O space registers. 0 = Disable (Default). 1 = Enable access to I/O space. The Native PCI Mode Base Address register should be programmed prior to setting this bit. ***Note:*** This bit becomes writable when the IOSE bit in offset 41h is set. If at any point software decides to clear the IOSE bit, software must first clear the IOS bit.

19.1.4 PCISTS – PCI Status Register (Audio – D30:F2)

Offset:	06–07h	Attribute:	RO, R/WC
Default Value	0280h	Size:	16 bits
Lockable:	No	Power Well:	Core

PCISTA is a 16-bit status register. Refer to the PCI 2.3 specification for complete details on each bit.

Bit	Description
15	Detected Parity Error (DPE). Not implemented. Hardwired to 0.
14	Signaled System Error (SSE) – RO. Not implemented. Hardwired to 0.
13	Master Abort Status (MAS) – R/WC. Software clears this bit by writing a 1 to it. 0 = No master abort generated. 1 = Bus Master AC '97 2.3 interface function, as a master, generates a master abort.
12	Reserved – RO. Will always read as 0.
11	Signaled Target Abort (STA) – RO. Not implemented. Hardwired to 0.
10:9	DEVSEL# Timing Status (DEV_STS) – RO. This 2-bit field reflects the Intel® 631xESB/632xESB I/O Controller Hub's DEVSEL# timing when performing a positive decode. 01b = Medium timing.
8	Data Parity Error Detected (DPED) – RO. Not implemented. Hardwired to 0.
7	Fast Back to Back Capable (FB2BC) – RO. Hardwired to 1. This bit indicates that the Intel® 631xESB/632xESB I/O Controller Hub as a target is capable of fast back-to-back transactions.
6	UDF Supported – RO. Not implemented. Hardwired to 0.
5	66 MHz Capable (66MHZ_CAP) – RO. Hardwired to 0.
4	Capabilities List (CAP_LIST) **–** RO. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h.
3	**Interrupt Status (IS)** – RO. 0 = This bit is 0 after the interrupt is cleared. 1 = This bit is 1 when the INTx# is asserted.
2:0	Reserved.

19.1.5 RID – Revision Identification Register (Audio – D30:F2)

Offset:	08h	Attribute:	RO
Default Value:	See bit description	Size:	8 Bits
Lockable:	No	Power Well:	Core

Bit	Description
7:0	**Revision ID –** RO. Refer to Table 2-33 or the *Intel® 631xESB/632xESB I/O Controller Hub EDS Specification Update* for the value of the Revision ID Register

19.1.6 PI – Programming Interface Register (Audio – D30:F2)

Offset:	09h	Attribute:	RO
Default Value:	00h	Size:	8 bits
Lockable:	No	Power Well:	Core

Bit	Description
7:0	Programming Interface – RO.

19.1.7 SCC – Sub Class Code Register (Audio – D30:F2)

Address Offset:	0Ah	Attribute:	RO
Default Value:	01h	Size:	8 bits
Lockable:	No	Power Well:	Core

Bit	Description
7:0	Sub Class Code (SCC) – RO. 01h = Audio Device

19.1.8 BCC – Base Class Code Register (Audio – D30:F2)

Address Offset:	0Bh	Attribute:	RO
Default Value:	04h	Size:	8 bits
Lockable:	No	Power Well:	Core

Bit	Description
7:0	Base Class Code (BCC) – RO. 04h = Multimedia device

19.1.9 HEADTYP – Header Type Register (Audio – D30:F2)

Address Offset:	0Eh	Attribute:	RO
Default Value:	00h	Size:	8 bits
Lockable:	No	Power Well:	Core

Bit	Description
7:0	Header Type – RO. Hardwired to 00h.

19.1.10 NAMBAR – Native Audio Mixer Base Address Register (Audio – D30:F2)

Address Offset:	10–13h	Attribute:	R/W, RO
Default Value:	00000000h	Size:	32 bits
Lockable:	No	Power Well:	Core

The Native PCI Mode Audio function uses PCI Base Address register #1 to request a contiguous block of I/O space that is to be used for the Native Audio Mixer software interface. The mixer requires 256 bytes of I/O space. Native Audio Mixer and Modem codec I/O registers are located from 00h to 7Fh and reside in the codec. Access to these registers will be decoded by the AC '97 controller and forwarded over the AC-link to the codec. The codec will then respond with the register value.

In the case of the split codec implementation, accesses to the different codecs are differentiated by the controller by using address offsets 00h–7Fh for the primary codec and address offsets 80h–FEh for the secondary codec.

Note: The tertiary codec cannot be addressed via this address space. The tertiary space is only available from the new MMBAR register. This register powers up as read only and only becomes write-able when the IOSE bit in offset 41h is set.

For description of these I/O registers, refer to the *Audio Codec '97 Component Specification, Version 2.3*.

Bit	Description
31:16	Hardwired to 0's.
15:8	**Base Address –** R/W. These bits are used in the I/O space decode of the Native Audio Mixer interface registers. The number of upper bits that a device actually implements depends on how much of the address space the device will respond to. For the AC '97 mixer, the upper 16 bits are hardwired to 0, while bits 15:8 are programmable. This configuration yields a maximum I/O block size of 256 bytes for this base address.
7:1	Reserved. Read as 0's.
0	**Resource Type Indicator (RTE) –** RO. This bit defaults to 0 and changes to 1 if the IOSE bit is set (D30:F2:Offset 41h, bit 0). When 1, this bit indicates a request for I/O space.

19.1.11 NABMBAR – Native Audio Bus Mastering Base Address Register (Audio – D30:F2)

Address Offset:	14–17h	Attribute:	R/W, RO
Default Value:	00000001h	Size:	32 bits
Lockable:	No	Power Well:	Core

The Native PCI Mode Audio function uses PCI Base Address register #1 to request a contiguous block of I/O space that is to be used for the Native Mode Audio software interface.

Note: The DMA registers for S/PDIF* and Microphone In 2 cannot be addressed via this address space. These DMA functions are only available from the new MBBAR register. This register powers up as read only and only becomes write-able when the IOSE bit in offset 41h is set.

Bit	Description
31:16	Hardwired to 0's
15:6	**Base Address –** R/W. These bits are used in the I/O space decode of the Native Audio Bus Mastering interface registers. The number of upper bits that a device actually implements depends on how much of the address space the device will respond to. For AC '97 bus mastering, the upper 16 bits are hardwired to 0, while bits 15:6 are programmable. This configuration yields a maximum I/O block size of 64 bytes for this base address.
5:1	Reserved. Read as 0's.
0	**Resource Type Indicator (RTE) –** RO. This bit defaults to 0 and changes to 1 if the IOSE bit is set (D30:F2:Offset 41h, bit 0). When 1, this bit indicates a request for I/O space.

19.1.12 MMBAR – Mixer Base Address Register (Audio – D30:F2)

Address Offset:	18–1Bh	Attribute:	R/W, RO
Default Value:	00000000h	Size:	32 bits
Lockable:	No	Power Well:	Core

This BAR creates 512 bytes of memory space to signify the base address of the register space. The lower 256 bytes of this space map to the same registers as the 256-byte I/O space pointed to by NAMBAR. The lower 384 bytes are divided as follows:

- 128 bytes for the primary codec (offsets 00–7Fh)
- 128 bytes for the secondary codec (offsets 80–FFh)
- 128 bytes for the tertiary codec (offsets 100h–17Fh).
- 128 bytes of reserved space (offsets 180h–1FFh), returning all 0.

Bit	Description
31:9	**Base Address –** R/W. This field provides the lower 32-bits of the 512-byte memory offset to use for decoding the primary, secondary, and tertiary codec's mixer spaces.
8:3	Reserved. Read as 0's.
2:1	Type – RO. Hardwired to 00b to Indicate the base address exists in 32-bit address space
0	Resource Type Indicator (RTE) – RO. Hardwired to 0 to indicate a request for memory space.

19.1.13 MBBAR – Bus Master Base Address Register (Audio – D30:F2)

Address Offset:	1C–1Fh	Attribute:	R/W, RO
Default Value:	00000000h	Size:	32 bits
Lockable:	No	Power Well:	Core

This BAR creates 256-bytes of memory space to signify the base address of the bus master memory space. The lower 64-bytes of the space pointed to by this register point to the same registers as the MBBAR.

Bit	Description
31:8	**Base Address** – R/W. This field provides the I/O offset to use for decoding the PCM In, PCM Out, and Microphone 1 DMA engines.
7:3	Reserved. Read as 0's.
2:1	Type – RO. Hardwired to 00b to indicate the base address exists in 32-bit address space
0	Resource Type Indicator (RTE) – RO. Hardwired to 0 to indicate a request for memory space.

19.1.14 SVID – Subsystem Vendor Identification Register (Audio – D30:F2)

Address Offset:	2C–2Dh	Attribute:	R/WO
Default Value:	0000h	Size:	16 bits
Lockable:	No	Power Well:	Core

The SVID register, in combination with the Subsystem ID register (D30:F2:2Eh), enable the operating environment to distinguish one audio subsystem from the other(s).

This register is implemented as write-once register. Once a value is written to it, the value can be read back. Any subsequent writes will have no effect.

This register is not affected by the $D3_{HOT}$ to D0 transition.

Bit	Description
15:0	**Subsystem Vendor ID** – R/WO.

19.1.15 SID – Subsystem Identification Register (Audio – D30:F2)

Address Offset:	2E–2Fh	Attribute:	R/WO
Default Value:	0000h	Size:	16 bits
Lockable:	No	Power Well:	Core

The SID register, in combination with the Subsystem Vendor ID register (D30:F2:2Ch) make it possible for the operating environment to distinguish one audio subsystem from the other(s).

This register is implemented as write-once register. Once a value is written to it, the value can be read back. Any subsequent writes will have no effect.

This register is not affected by the $D3_{HOT}$ to D0 transition.

Bit	Description
15:0	**Subsystem ID –** R/WO.

19.1.16 CAP_PTR – Capabilities Pointer Register (Audio – D30:F2)

Address Offset:	34h	Attribute:	RO
Default Value:	50h	Size:	8 bits
Lockable:	No	Power Well:	Core

This register indicates the offset for the capability pointer.

Bit	Description
7:0	Capabilities Pointer (CAP_PTR) – RO. This field indicates that the first capability pointer offset is offset 50h

19.1.17 INT_LN – Interrupt Line Register (Audio – D30:F2)

Address Offset:	3Ch	Attribute:	R/W
Default Value:	00h	Size:	8 bits
Lockable:	No	Power Well:	Core

This register indicates which PCI interrupt line is used for the AC'97 module interrupt.

Bit	Description
7:0	**Interrupt Line (INT_LN) –** R/W. This data is not used by the Intel® 631xESB/632xESB I/O Controller Hub. It is used to communicate to software the interrupt line that the interrupt pin is connected to.

19.1.18 INT_PN – Interrupt Pin Register (Audio – D30:F2)

Address Offset:	3Dh	Attribute:	RO
Default Value:	See Description	Size:	8 bits
Lockable:	No	Power Well:	Core

This register indicates which PCI interrupt pin is used for the AC '97 module interrupt. The AC '97 interrupt is internally OR'd to the interrupt controller with the PIRQB# signal.

Bit	Description
7:0	AC '97 Interrupt Routing – RO. This reflects the value of D30IP.AAIP in chipset configuration space.

19.1.19 PCID – Programmable Codec Identification Register (Audio – D30:F2)

Address Offset:	40h	Attribute:	R/W
Default Value:	09h	Size:	8 bits
Lockable:	No	Power Well:	Core

This register is used to specify the ID for the secondary and tertiary codecs for I/O accesses. This register is not affected by the D3HOT to D0 transition. The value in this register must be modified only before any AC'97 codec accesses.

Bit	Description
7:4	Reserved.
3:2	**Tertiary Codec ID (TID**) – R/W. These bits define the encoded ID that is used to address the tertiary codec I/O space. Bit 1 is the first bit sent and Bit 0 is the second bit sent on ACZ_SDOUT during slot 0.
1:0	**Secondary Codec ID (SCID) –** R/W. These two bits define the encoded ID that is used to address the secondary codec I/O space. The two bits are the ID that will be placed on slot 0, bits 0 and 1, upon an I/O access to the secondary codec. Bit 1 is the first bit sent and bit 0 is the second bit sent on ACZ_SDOUT during slot 0.

19.1.20 CFG – Configuration Register (Audio – D30:F2)

Address Offset:	41h	Attribute:	R/W
Default Value:	00h	Size:	8 bits
Lockable:	No	Power Well:	Core

This register is used to specify the ID for the secondary and tertiary codecs for I/O accesses. This register is not affected by the D3HOT to D0 transition.

Bit	Description
7:1	Reserved – RO.
0	**I/O Space Enable (IOSE) –** R/W. 0 = Disable. The IOS bit at offset 04h and the I/O space BARs at offset 10h and 14h become read only registers. Additionally, bit 0 of the I/O BARs at offsets 10h and 14h are hardwired to 0 when this bit is 0. This is the default state for the I/O BARs. BIOS must explicitly set this bit to allow a legacy driver to work. 1 = Enable.

19.1.21 PID – PCI Power Management Capability Identification Register (Audio – D30:F2)

Address Offset:	50–51h	Attribute:	RO
Default Value:	0001h	Size:	16 bits
Lockable:	No	Power Well:	Core

Bit	Description
15:8	Next Capability (NEXT) – RO. This field indicates that the next item in the list is at offset 00h.
7:0	Capability ID (CAP) – RO.This field indicates that this pointer is a message signaled interrupt capability

19.1.22 PC – Power Management Capabilities Register (Audio – D30:F2)

Address Offset:	52–53h	Attribute:	RO
Default Value:	C9C2h	Size:	16 bits
Lockable:	No	Power Well:	Core

This register is not affected by the $D3_{HOT}$ to D0 transition.

Bit	Description
15:11	PME Support – RO. This field indicates PME# can be generated from all D states.
10:9	Reserved.
8:6	Auxiliary Current – RO. This field reports 375 mA maximum Suspend well current required when in the $D3_{COLD}$ state.
5	Device Specific Initialization (DSI) – RO. This field indicates that no device-specific initialization is required.
4	Reserved – RO.
3	PME Clock (PMEC) – RO. This field indicates that PCI clock is not required to generate PME#.
2:0	Version (VER) – RO. This field indicates support for Revision 1.1 of the PCI Power Management Specification.

19.1.23 PCS – Power Management Control and Status Register (Audio – D30:F2)

Address Offset:	54–55h	Attribute:	R/W, R/WC
Default Value:	0000h	Size:	16 bits
Lockable:	No	Power Well:	Resume

Bit	Description
15	**PME Status (PMES) –** R/WC. This bit resides in the resume well. Software clears this bit by writing a 1 to it. 0 = PME# signal Not asserted by AC '97 controller. 1 = This bit is set when the AC'97 controller would normally assert the PME# signal independent of the state of the PME_En bit.
14:9	Reserved – RO.
8	**Power Management Event Enable (PMEE) –** R/W. 0 = Disable. 1 = Enable. When set, and if corresponding PMES is also set, the AC '97 controller sets the AC97_STS bit in the GPE0_STS register
7:2	Reserved – RO.
1:0	**Power State (PS) –** R/W. This field is used both to determine the current power state of the AC'97 controller and to set a new power state. The values are: 00 = D0 state 01 = not supported 10 = not supported 11 = $D3_{HOT}$ state When in the $D3_{HOT}$ state, the AC'97 controller's configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked. If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs.

19.2 AC'97 Audio I/O Space (D30:F2)

The AC'97 I/O space includes Native Audio Bus Master Registers and Native Mixer Registers. For the Intel® 631xESB/632xESB I/O Controller Hub, the offsets are important as they will determine bits 1:0 of the TAG field (codec ID).

Audio Mixer I/O space can be accessed as a 16-bit field only since the data packet length on AC-link is a word. Any S/W access to the codec will be done as a 16-bit access starting from the first active byte. In case no byte enables are active, the access will be done at the first word of the qWord that contains the address of this request.

Table 19-2. Intel® 631xESB/632xESB I/O Controller Hub Audio Mixer Register Configuration (Sheet 1 of 2)

Primary Offset (Codec ID =00)	Secondary Offset (Codec ID =01)	Tertiary Offset (Codec ID =10)	NAMBAR Exposed Registers (D30:F2)
00h	80h	100h	Reset
02h	82h	102h	Master Volume
04h	84h	104h	Aux Out Volume
06h	86h	106h	Mono Volume
08h	88h	108h	Master Tone (R & L)
0Ah	8Ah	10Ah	PC_BEEP Volume
0Ch	8Ch	10Ch	Phone Volume
0Eh	8Eh	10Eh	Mic Volume
10h	90h	110h	Line In Volume

Table 19-2. Intel® 631xESB/632xESB I/O Controller Hub Audio Mixer Register Configuration (Sheet 2 of 2)

Primary Offset (Codec ID =00)	Secondary Offset (Codec ID =01)	Tertiary Offset (Codec ID =10)	NAMBAR Exposed Registers (D30:F2)
12h	92h	112h	CD Volume
14h	94h	114h	Video Volume
16h	96h	116h	Aux In Volume
18h	98h	118h	PCM Out Volume
1Ah	9Ah	11Ah	Record Select
1Ch	9Ch	11Ch	Record Gain
1Eh	9Eh	11Eh	Record Gain Mic
20h	A0h	120h	General Purpose
22h	A2h	122h	3D Control
24h	A4h	124h	AC'97 RESERVED
26h	A6h	126h	Powerdown Ctrl/Stat
28h	A8h	128h	Extended Audio
2Ah	AAh	12Ah	Extended Audio Ctrl/Stat
2Ch	ACh	12Ch	PCM Front DAC Rate
2Eh	AEh	12Eh	PCM Surround DAC Rate
30h	B0h	130h	PCM LFE DAC Rate
32h	B2h	132h	PCM LR ADC Rate
34h	B4h	134h	MIC ADC Rate
36h	B6h	136h	6Ch Vol: C, LFE
38h	B8h	138h	6Ch Vol: L, R Surround
3Ah	BAh	13Ah	S/PDIF Control
3C–56h	BC–D6h	13C–156h	Intel RESERVED
58h	D8h	158h	AC'97 Reserved
5Ah	DAh	15Ah	Vendor Reserved
7Ch	FCh	17Ch	Vendor ID1
7Eh	FEh	17Eh	Vendor ID2

Note:
1. Software should not try to access reserved registers
2. Primary Codec ID cannot be changed. Secondary codec ID can be changed via bits 1:0 of configuration register 40h. Tertiary codec ID can be changed via bits 3:2 of configuration register 40h.
3. The tertiary offset is only available through the memory space defined by the MMBAR register.

The Bus Master registers are located from offset + 00h to offset + 51h and reside in the AC'97 controller. Accesses to these registers do not cause the cycle to be forwarded over the AC-link to the codec. S/W could access these registers as bytes, word, DWord or qWord quantities, but reads must not cross DWord boundaries.

In the case of the split codec implementation accesses to the different codecs are differentiated by the controller by using address offsets 00h–7Fh for the primary codec, address offsets 80h–FFh for the secondary codec and address offsets 100h–17Fh for the tertiary codec.

The Global Control (GLOB_CNT) (D30:F2:2Ch) and Global Status (GLOB_STA) (D30:F2:30h) registers are aliased to the same global registers in the audio and modem I/O space. Therefore a read/write to these registers in either audio or modem I/O space affects the same physical register.

Bus Mastering registers exist in I/O space and reside in the AC'97 controller. The six channels, PCM in, PCM in 2, PCM out, Mic in, Mic 2, and S/PDIF out, each have their own set of Bus Mastering registers. The following register descriptions apply to all six channels. The register definition section titles use a generic "X_" in front of the register to indicate that the register applies to all six channels. The naming prefix convention used in Table 19-3 and in the register description I/O address is as follows:

PI = PCM in channel
PO = PCM out channel
MC = Mic in channel
MC2 = Mic 2 channel
PI2 = PCM in 2 channel
SP = S/PDIF out channel.

Table 19-3. Native Audio Bus Master Control Registers (Sheet 1 of 2)

Offset	Mnemonic	Name	Default	Access
00h	PI_BDBAR	PCM In Buffer Descriptor list Base Address	00000000h	R/W
04h	PI_CIV	PCM In Current Index Value	00h	RO
05h	PI_LVI	PCM In Last Valid Index	00h	R/W
06h	PI_SR	PCM In Status	0001h	R/WC, RO
08h	PI_PICB	PCM In Position in Current Buffer	0000h	RO
0Ah	PI_PIV	PCM In Prefetched Index Value	00h	RO
0Bh	PI_CR	PCM In Control	00h	R/W, R/W (special)
10h	PO_BDBAR	PCM Out Buffer Descriptor list Base Address	00000000h	R/W
14h	PO_CIV	PCM Out Current Index Value	00h	RO
15h	PO_LVI	PCM Out Last Valid Index	00h	R/W
16h	PO_SR	PCM Out Status	0001h	R/WC, RO
18h	PO_PICB	PCM In Position In Current Buffer	0000h	RO
1Ah	PO_PIV	PCM Out Prefetched Index Value	00h	RO
1Bh	PO_CR	PCM Out Control	00h	R/W, R/W (special)
20h	MC_BDBAR	Mic. In Buffer Descriptor List Base Address	00000000h	R/W
24h	MC_CIV	Mic. In Current Index Value	00h	RO
25h	MC_LVI	Mic. In Last Valid Index	00h	R/W
26h	MC_SR	Mic. In Status	0001h	R/WC, RO
28h	MC_PICB	Mic. In Position In Current Buffer	0000h	RO
2Ah	MC_PIV	Mic. In Prefetched Index Value	00h	RO
2Bh	MC_CR	Mic. In Control	00h	R/W, R/W (special)
2Ch	GLOB_CNT	Global Control	00000000h	R/W, R/W (special)
30h	GLOB_STA	Global Status	See register description	R/W, R/WC, RO
34h	CAS	Codec Access Semaphore	00h	R/W (special)
40h	MC2_BDBAR	Mic. 2 Buffer Descriptor List Base Address	00000000h	R/W
44h	MC2_CIV	Mic. 2 Current Index Value	00h	RO
45h	MC2_LVI	Mic. 2 Last Valid Index	00h	R/W
46h	MC2_SR	Mic. 2 Status	0001h	RO, R/WC
48h	MC2_PICB	Mic 2 Position In Current Buffer	0000h	RO
4Ah	MC2_PIV	Mic. 2 Prefetched Index Value	00h	RO

Table 19-3. Native Audio Bus Master Control Registers (Sheet 2 of 2)

Offset	Mnemonic	Name	Default	Access
4Bh	MC2_CR	Mic. 2 Control	00h	R/W, R/W (special)
50h	PI2_BDBAR	PCM In 2 Buffer Descriptor List Base Address	00000000h	R/W
54h	PI2_CIV	PCM In 2 Current Index Value	00h	RO
55h	PI2_LVI	PCM In 2 Last Valid Index	00h	R/W
56h	PI2_SR	PCM In 2 Status	0001h	R/WC, RO
58h	PI2_PICB	PCM In 2 Position in Current Buffer	0000h	RO
5Ah	PI2_PIV	PCM In 2 Prefetched Index Value	00h	RO
5Bh	PI2_CR	PCM In 2 Control	00h	R/W, R/W (special)
60h	SPBAR	S/PDIF Buffer Descriptor List Base Address	00000000h	R/W
64h	SPCIV	S/PDIF Current Index Value	00h	RO
65h	SPLVI	S/PDIF Last Valid Index	00h	R/W
66h	SPSR	S/PDIF Status	0001h	R/WC, RO
68h	SPPICB	S/PDIF Position In Current Buffer	0000h	RO
6Ah	SPPIV	S/PDIF Prefetched Index Value	00h	RO
6Bh	SPCR	S/PDIF Control	00h	R/W, R/W (special)
80h	SDM	SData_IN Map	00h	R/W, RO

Note: Internal reset as a result of $D3_{HOT}$ to D0 transition will reset all the core well registers except the registers shared with the AC'97 Modem (GCR, GSR, CASR). All resume well registers will not be reset by the $D3_{HOT}$ to D0 transition.

Core well registers and bits **not** reset by the $D3_{HOT}$ to D0 transition:

- offset 2Ch–2Fh – bits 6:0 Global Control (GLOB_CNT)
- offset 30h–33h – bits [29,15,11:10,0] Global Status (GLOB_STA)
- offset 34h – Codec Access Semaphore Register (CAS)

Resume well registers and bits **will not** be reset by the $D3_{HOT}$ to D0 transition:

- offset 30h–33h – bits [17:16] Global Status (GLOB_STA)

19.2.1 *X*_BDBAR – Buffer Descriptor Base Address Register (Audio – D30:F2)

I/O Address:	NABMBAR + 00h (PIBDBAR), NABMBAR + 10h (POBDBAR), NABMBAR + 20h (MCBDBAR) MBBAR + 40h (MC2BDBAR) MBBAR + 50h (PI2BDBAR) MBBAR + 60h (SPBAR)	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits
Lockable:	No	Power Well:	Core

Software can read the register at offset 00h by performing a single 32-bit read from address offset 00h. Reads across DWord boundaries are not supported.

Bit	Description
31:3	**Buffer Descriptor Base Address[31:3] –** R/W. These bits represent address bits 31:3. The data should be aligned on 8-byte boundaries. Each buffer descriptor is 8 bytes long and the list can contain a maximum of 32 entries.
2:0	Hardwired to 0.

19.2.2 *X*_CIV – Current Index Value Register (Audio – D30:F2)

I/O Address:	NABMBAR + 04h (PICIV), NABMBAR + 14h (POCIV), NABMBAR + 24h (MCCIV) MBBAR + 44h (MC2CIV) MBBAR + 54h (PI2CIV) MBBAR + 64h (SPCIV)	Attribute:	RO
Default Value:	00h	Size:	8 bits
Lockable:	No	Power Well:	Core

Software can read the registers at offsets 04h, 05h and 06h simultaneously by performing a single, 32-bit read from address offset 04h. Software can also read this register individually by doing a single, 8-bit read to offset 04h.

Bit	Description
7:5	Hardwired to 0
4:0	**Current Index Value [4:0] –** RO. These bits represent which buffer descriptor within the list of 32 descriptors is currently being processed. As each descriptor is processed, this value is incremented. The value rolls over after it reaches 31.

Note: Reads across DWord boundaries are not supported.

19.2.3 *X*_LVI – Last Valid Index Register (Audio – D30:F2)

I/O Address:	NABMBAR + 05h (PILVI), NABMBAR + 15h (POLVI), NABMBAR + 25h (MCLVI) MBBAR + 45h (MC2LVI) MBBAR + 55h (PI2LVI) MBBAR + 65h (SPLVI)	Attribute:	R/W
Default Value:	00h	Size:	8 bits
Lockable:	No	Power Well:	Core

Software can read the registers at offsets 04h, 05h and 06h simultaneously by performing a single, 32-bit read from address offset 04h. Software can also read this register individually by doing a single, 8-bit read to offset 05h.

Bit	Description
7:5	Hardwired to 0.
4:0	**Last Valid Index [4:0] –** R/W. This value represents the last valid descriptor in the list. This value is updated by the software each time it prepares a new buffer and adds it to the list.

Note: Reads across DWord boundaries are not supported.

19.2.4 *X*_SR – Status Register (Audio – D30:F2)

I/O Address:	NABMBAR + 06h (PISR), NABMBAR + 16h (POSR), NABMBAR + 26h (MCSR) MBBAR + 46h (MC2SR) MBBAR + 56h (PI2SR) MBBAR + 66h (SPSR)	Attribute:	R/WC, RO
Default Value:	0001h	Size:	16 bits
Lockable:	No	Power Well:	Core

Software can read the registers at offsets 04h, 05h and 06h simultaneously by performing a single, 32-bit read from address offset 04h. Software can also read this register individually by doing a single, 16-bit read to offset 06h. Reads across DWord boundaries are not supported.

Bit	Description
15:5	Reserved.
4	FIFO Error (FIFOE) – R/WC. Software clears this bit by writing a 1 to it. 0 = No FIFO error. 1 = FIFO error occurs. **PISR Register:** FIFO error indicates a FIFO overrun. The FIFO pointers don't increment, the incoming data is not written into the FIFO, thus is lost. **POSR Register:** FIFO error indicates a FIFO underrun. The sample transmitted in this case should be the last valid sample. The Intel® 631xESB/632xESB I/O Controller Hub will set the FIFOE bit if the under-run or overrun occurs when there are more valid buffers to process.
3	**Buffer Completion Interrupt Status (BCIS) –** R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = Set by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. It remains active until cleared by software.
2	**Last Valid Buffer Completion Interrupt (LVBCI) –** R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = Last valid buffer has been processed. It remains active until cleared by software. This bit indicates the occurrence of the event signified by the last valid buffer being processed. Thus this is an event status bit that can be cleared by software once this event has been recognized. This event will cause an interrupt if the enable bit (D30:F2:NABMBAR + 0Bh, bit 2) in the Control Register is set. The interrupt is cleared when the software clears this bit. In the case of *Transmits* (PCM out, Modem out) this bit is set, after the last valid buffer has been fetched (not after transmitting it). While in the case of *Receives*, this bit is set after the data for the last buffer has been written to memory.
1	**Current Equals Last Valid (CELV) –** RO. 0 = Cleared by hardware when controller exists state (that is, until a new value is written to the LVI register.) 1 = Current Index is equal to the value in the Last Valid Index Register (D30:F2:NABMBAR + 05h), and the buffer pointed to by the CIV has been processed (that is, after the last valid buffer has been processed). This bit is very similar to bit 2, except this bit reflects the state rather than the event. This bit reflects the state of the controller, and remains set until the controller exits this state.
0	**DMA Controller Halted (DCH) –** RO. 0 = Running. 1 = Halted. This could happen because of the Start/Stop bit being cleared and the DMA engines are idle, or it could happen once the controller has processed the last valid buffer.

19.2.5 *X*_PICB – Position In Current Buffer Register (Audio – D30:F2)

I/O Address:	NABMBAR + 08h (PIPICB), NABMBAR + 18h (POPICB), NABMBAR + 28h (MCPICB) MBBAR + 48h (MC2PICB) MBBAR + 58h (PI2PICB) MBBAR + 68h (SPPICB)	Attribute:	RO
Default Value:	0000h	Size:	16 bits
Lockable:	No	Power Well:	Core

Software can read the registers at the offsets 08h, 0Ah, and 0Bh by performing a 32-bit read from the address offset 08h. Software can also read this register individually by doing a single, 16-bit read to offset 08h. Reads across DWord boundaries are not supported.

Bit	Description
15:0	**Position In Current Buffer [15:0] –** RO. These bits represent the number of samples left to be processed in the current buffer. Once again, this means, the number of samples not yet read from memory (in the case of reads from memory) or not yet written to memory (in the case of writes to memory), irrespective of the number of samples that have been transmitted/received across AC-link.

19.2.6 *X*_PIV – Prefetched Index Value Register (Audio – D30:F2)

I/O Address:	NABMBAR + 0Ah (PIPIV), NABMBAR + 1Ah (POPIV), NABMBAR + 2Ah (MCPIV) MBBAR + 4Ah (MC2PIV) MBBAR + 5Ah (PI2PIV) MBBAR + 6Ah (SPPIV)	Attribute:	RO
Default Value:	00h	Size:	8 bits
Lockable:	No	Power Well:	Core

Software can read the registers at the offsets 08h, 0Ah, and 0Bh by performing a 32-bit read from the address offset 08h. Software can also read this register individually by doing a single, 8-bit read to offset 0Ah. Reads across DWord boundaries are not supported

Bit	Description
7:5	Hardwired to 0.
4:0	**Prefetched Index Value [4:0] –** RO. These bits represent which buffer descriptor in the list has been prefetched. The bits in this register are also modulo 32 and roll over after they reach 31.

19.2.7 *X*_CR – Control Register (Audio – D30:F2)

I/O Address:	NABMBAR + 0Bh (PICR), NABMBAR + 1Bh (POCR), NABMBAR + 2Bh (MCCR) MBBAR + 4Bh (MC2CR) MBBAR + 5Bh (PI2CR) MBBAR + 6Bh (SPCR)	Attribute:	R/W, R/W (special)
Default Value:	00h	Size:	8 bits
Lockable:	No	Power Well:	Core

Software can read the registers at the offsets 08h, 0Ah, and 0Bh by performing a 32-bit read from the address offset 08h. Software can also read this register individually by doing a single, 8-bit read to offset 0Bh. Reads across DWord boundaries are not supported.

Bit	Description
7:5	Reserved.
4	**Interrupt on Completion Enable (IOCE) –** R/W. This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. 0 = Disable. Interrupt will not occur. 1 = Enable.
3	**FIFO Error Interrupt Enable (FEIE) –** R/W. This bit controls whether the occurrence of a FIFO error will cause an interrupt or not. 0 = Disable. Bit 4 in the Status Register will be set, but the interrupt will not occur. 1 = Enable. Interrupt will occur.
2	**Last Valid Buffer Interrupt Enable (LVBIE) –** R/W. This bit controls whether the completion of the last valid buffer will cause an interrupt or not. 0 = Disable. Bit 2 in the Status register will still be set, but the interrupt will not occur. 1 = Enable.
1	**Reset Registers (RR) –** R/W (special). 0 = Removes reset condition. 1 = Contents of all Bus master related registers to be reset, except the interrupt enable bits (bit 4,3,2 of this register). Software needs to set this bit but need not clear it since the bit is self clearing. This bit must be set only when the Run/Pause bit (D30:F2:2Bh, bit 0) is cleared. Setting it when the Run bit is set will cause undefined consequences.
0	**Run/Pause Bus Master (RPBM) –** R/W. 0 = Pause bus master operation. This results in all state information being retained (that is, master mode operation can be stopped and then resumed). 1 = Run. Bus master operation starts.

19.2.8 GLOB_CNT – Global Control Register (Audio – D30:F2)

I/O Address:	NABMBAR + 2Ch	Attribute:	R/W, R/W (special)
Default Value:	00000000h	Size:	32 bits
Lockable:	No	Power Well:	Core

Bit	Description
31:30	**S/PDIF Slot Map (SSM) –** R/W. If the run/pause bus master bit (bit 0 of offset 2Bh) is set, then the value in these bits indicate which slots S/PDIF data is transmitted on. Software must ensure that the programming here does not conflict with the PCM channels being used. If there is a conflict, unpredictable behavior will result – the hardware will not check for a conflict. 00 = Reserved 01 = Slots 7 and 8 10 = Slots 6 and 9 11 = Slots 10 and 11
29:24	Reserved.
23:22	**PCM Out Mode (POM) –** R/W. Enables the PCM out channel to use 16 or 20-bit audio on PCM out. This does not affect the microphone of S/PDIF DMA. When greater than 16 bit audio is used, the data structures are aligned as 32-bits per sample, with the highest order bits representing the data, and the lower order bits as don't care. 00 = 16 bit audio (default) 01 = 20 bit audio 10 = Reserved. If set, indeterminate behavior will result. 11 = Reserved. If set, indeterminate behavior will result.
21:20	**PCM 4/6 Enable –** R/W. This field configures PCM Output for 2, 4 or 6 channel mode. 00 = 2-channel mode (default) 01 = 4-channel mode 10 = 6-channel mode 11 = Reserved
19:7	Reserved.
6	**ACZ_SDIN2 Interrupt Enable –** R/W. 0 = Disable. 1 = Enable an interrupt to occur when the codec on the ACZ_SDIN2 causes a resume event on the AC-link. ***Note:*** This bit is not affected by AC '97 Audio Function $D3_{HOT}$ to D0 reset.
5	**ACZ_SDIN1 Interrupt Enable** – R/W. 0 = Disable. 1 = Enable an interrupt to occur when the codec on the ACZ_SDIN1 causes a resume event on the AC-link. ***Note:*** This bit is not affected by AC '97 Audio Function $D3_{HOT}$ to D0 reset.
4	**ACZ_SDIN0 Interrupt Enable** – R/W. 0 = Disable. 1 = Enable an interrupt to occur when the codec on ACZ_SDIN0 causes a resume event on the AC-link. ***Note:*** This bit is not affected by AC '97 Audio Function $D3_{HOT}$ to D0 reset.
3	AC-LINK Shut Off (LSO) – R/W. 0 = Normal operation. 1 = Controller disables all outputs which will be pulled low by internal pull down resistors. ***Note:*** This bit is not affected by AC '97 Audio Function $D3_{HOT}$ to D0 reset.

Bit	Description
2	**AC'97 Warm Reset** – R/W (special). 0 = Normal operation. 1 = Writing a 1 to this bit causes a warm reset to occur on the AC-link. The warm reset will awaken a suspended codec without clearing its internal registers. If software attempts to perform a warm reset while bit_clk is running, the write will be ignored and the bit will not change. This bit is self-clearing (it remains set until the reset completes and bit_clk is seen on the AC-link, after which it clears itself). ***Note:*** This bit is not affected by AC '97 Audio Function $D3_{HOT}$ to D0 reset.
1	**AC'97 Cold Reset# –** R/W. 0 = Writing a 0 to this bit causes a cold reset to occur throughout the AC '97 circuitry. All data in the controller and the codec will be lost. Software needs to clear this bit no sooner than the minimum number of ms have elapsed. 1 = This bit defaults to 0 and hence after reset, the driver needs to set this bit to a 1. The value of this bit is retained after suspends; hence, if this bit is set to a 1 prior to suspending, a cold reset is not generated automatically upon resuming. Note: This bit is in the Core well and is not affected by AC '97 Audio Function $D3_{HOT}$ to D0 reset.
0	**GPI Interrupt Enable (GIE) –** R/W. This bit controls whether the change in status of any GPI causes an interrupt. 0 = Bit 0 of the Global Status Register is set, but no interrupt is generated. 1 = The change on value of a GPI causes an interrupt and sets bit 0 of the Global Status Register. ***Note:*** This bit is not affected by AC '97 Audio Function $D3_{HOT}$ to D0 reset.

Note: Reads across DWord boundaries are not supported.

19.2.9 GLOB_STA – Global Status Register (Audio – D30:F2)

I/O Address: NABMBAR + 30h
Default Value: 00x0xxx01110000000000xxxxx00xxxb
Lockable: No
Attribute: RO, R/W, R/WC
Size: 32 bits
Power Well: Core

Bit	Description
31:30	Reserved.
29	**ACZ_SDIN2 Resume Interrupt (S2RI) –** R/WC. This bit indicates a resume event occurred on ACZ_SDIN2. Software clears this bit by writing a 1 to it. 0 = Resume event did Not occur. 1 = Resume event occurred. This bit is not affected by $D3_{HOT}$ to D0 Reset.
28	**ACZ_SDIN2 Codec Ready (S2CR)** – RO. Reflects the state of the codec ready bit on ACZ_SDIN2. Bus masters ignore the condition of the codec ready bits, so software must check this bit before starting the bus masters. Once the codec is "ready", it must never go "not ready" spontaneously. 0 = Not Ready. 1 = Ready.
27	**Bit Clock Stopped (BCS)** – RO. This bit indicates that the bit clock is not running. 0 = Transition is found on BIT_CLK. 1 = Intel® 631xESB/632xESB I/O Controller Hub detected that there has been no transition on BIT_CLK for four consecutive PCI clocks.
26	**S/PDIF Interrupt (SPINT)** – RO. 0 = When the specific status bit is cleared, this bit will be cleared. 1 = S/PDIF out channel interrupt status bits have been set.
25	**PCM In 2 Interrupt (P2INT)** – RO. 0 = When the specific status bit is cleared, this bit will be cleared. 1 = One of the PCM In 2 channel status bits have been set.
24	**Microphone 2 In Interrupt (M2INT)** – RO. 0 = When the specific status bit is cleared, this bit will be cleared. 1 = One of the Mic in channel interrupts status bits has been set.

Bit	Description
23:22	**Sample Capabilities** – RO. This field indicates the capability to support more greater than 16-bit audio. 00 = Reserved 01 = 16 and 20-bit Audio supported (Intel® 631xESB/632xESB I/O Controller Hub value) 10 = Reserved 11 = Reserved
21:20	**Multichannel Capabilities** — RO. This field indicates the capability to support more 4 and 6 channels on PCM Out.
19:18	Reserved.
17	**MD3 –** R/W. Power down semaphore for Modem. This bit exists in the suspend well and maintains context across power states (except G3). The bit has no hardware function. It is used by software in conjunction with the AD3 bit to coordinate the entry of the two codecs into D3 state. This bit is not affected by $D3_{HOT}$ to D0 Reset.
16	**AD3 –** R/W. Power down semaphore for Audio. This bit exists in the suspend well and maintains context across power states (except G3). The bit has no hardware function. It is used by software in conjunction with the MD3 bit to coordinate the entry of the two codecs into D3 state. This bit is not affected by $D3_{HOT}$ to D0 Reset.
15	**Read Completion Status (RCS) –** R/WC. This bit indicates the status of codec read completions. 0 = A codec read completes normally. 1 = A codec read results in a time-out. The bit remains set until being cleared by software writing a 1 to the bit location. This bit is not affected by $D3_{HOT}$ to D0 Reset.
14	**Bit 3 of Slot 12 –** RO. Display bit 3 of the most recent slot 12.
13	**Bit 2 of Slot 12** – RO. Display bit 2 of the most recent slot 12.
12	**Bit 1 of slot 12** – RO. Display bit 1 of the most recent slot 12.
11	**ACZ_SDIN1 Resume Interrupt (S1R1) –** R/WC. This bit indicates that a resume event occurred on ACZ_SDIN1. Software clears this bit by writing a 1 to it. 0 = Resume event did Not occur 1 = Resume event occurred. This bit is not affected by $D3_{HOT}$ to D0 Reset.
10	**ACZ_SDIN0 Resume Interrupt (S0R1)** – R/WC. This bit indicates that a resume event occurred on ACZ_SDIN0. Software clears this bit by writing a 1 to it. 0 = Resume event did Not occur 1 = Resume event occurred. This bit is not affected by $D3_{HOT}$ to D0 Reset.
9	**ACZ_SDIN1 Codec Ready (S1CR) –** RO. Reflects the state of the codec ready bit in ACZ_SDIN1. Bus masters ignore the condition of the codec ready bits, so software must check this bit before starting the bus masters. Once the codec is "ready", it must never go "not ready" spontaneously. 0 = Not Ready. 1 = Ready.
8	**ACZ_SDIN0 Codec Ready (S0CR) –** RO. Reflects the state of the codec ready bit in ACZ_SDIN0. Bus masters ignore the condition of the codec ready bits, so software must check this bit before starting the bus masters. Once the codec is "ready", it must never go "not ready" spontaneously. 0 = Not Ready. 1 = Ready.
7	**Microphone In Interrupt (MINT) –** RO. 0 = When the specific status bit is cleared, this bit will be cleared. 1 = One of the Mic in channel interrupts status bits has been set.
6	**PCM Out Interrupt (POINT)** – RO. 0 = When the specific status bit is cleared, this bit will be cleared. 1 = One of the PCM out channel interrupts status bits has been set.
5	**PCM In Interrupt (PIINT) –** RO. 0 = When the specific status bit is cleared, this bit will be cleared. 1 = One of the PCM in channel interrupts status bits has been set.
4:3	Reserved

Bit	Description
2	**Modem Out Interrupt (MOINT**) – RO. 0 = When the specific status bit is cleared, this bit will be cleared. 1 = One of the modem out channel interrupts status bits has been set.
1	**Modem In Interrupt (MIINT)** – RO. 0 = When the specific status bit is cleared, this bit will be cleared. 1 = One of the modem in channel interrupts status bits has been set.
0	**GPI Status Change Interrupt (GSCI) –** R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = This bit reflects the state of bit 0 in slot 12, and is set when bit 0 of slot 12 is set. This indicates that one of the GPI's changed state, and that the new values are available in slot 12. This bit is not affected by AC '97 Audio Function $D3_{HOT}$ to D0 Reset.

Note: Reads across DWord boundaries are not supported.

19.2.10 CAS – Codec Access Semaphore Register (Audio – D30:F2)

I/O Address:	NABMBAR + 34h	Attribute:	R/W (special)
Default Value:	00h	Size:	8 bits
Lockable:	No	Power Well:	Core

Bit	Description
7:1	Reserved.
0	**Codec Access Semaphore (CAS) –** R/W (special). This bit is read by software to check whether a codec access is currently in progress. 0 = No access in progress. 1 = The act of reading this register sets this bit to 1. The driver that read this bit can then perform an I/O access. Once the access is completed, hardware automatically clears this bit.

Note: Reads across DWord boundaries are not supported.

19.2.11 SDM – SDATA_IN Map Register (Audio – D30:F2)

I/O Address:	NABMBAR + 80h	Attribute:	R/W, RO
Default Value:	00h	Size:	8 bits
Lockable:	No	Power Well:	Core

Bit	Description
7:6	**PCM In 2, Microphone In 2 Data In Line (DI2L)** – R/W. When the SE bit is set, these bits indicates which ACZ_SDIN line should be used by the hardware for decoding the input slots for PCM In 2 and Microphone In 2. When the SE bit is cleared, the value of these bits are irrelevant, and PCM In 2 and Mic In 2 DMA engines are not available. 00 = ACZ_SDIN0 01 = ACZ_SDIN1 10 = ACZ_SDIN2 11 = Reserved
5:4	**PCM In 1, Microphone In 1 Data In Line (DI1L)** – R/W. When the SE bit is set, these bits indicates which ACZ_SDIN line should be used by the hardware for decoding the input slots for PCM In 1 and Microphone In 1. When the SE bit is cleared, the value of these bits are irrelevant, and the PCM In 1 and Mic In 1 engines use the OR'd ACZ_SDIN lines. 00 = ACZ_SDIN0 01 = ACZ_SDIN1 10 = ACZ_SDIN2 11 = Reserved

3	**Steer Enable (SE) –** R/W. When set, the ACZ_SDIN lines are treated separately and not OR'd together before being sent to the DMA engines. When cleared, the ACZ_SDIN lines are OR'd together, and the "Microphone In 2" and "PCM In 2" DMA engines are not available.
2	Reserved **–** RO.
1:0	**Last Codec Read Data Input (LDI) –** RO. When a codec register is read, this indicates which ACZ_SDIN the read data returned on. Software can use this to determine how the codecs are mapped. The values are: 00 = ACZ_SDIN0 01 = ACZ_SDIN1 10 = ACZ_SDIN2 11 = Reserved

Note: Reads across DWord boundaries are not supported.

§§

20 AC'97 Modem Controller Registers (D30:F3)

20.1 AC'97 Modem PCI Configuration Space (D30:F3)

Note: Registers that are not shown should be treated as Reserved.

Table 20-1. AC '97 Modem PCI Register Address Map (Modem – D30:F3)

Offset	Mnemonic	Register	Default	Access
00–01h	VID	Vendor Identification	8086	RO
02–03h	DID	Device Identification	2699h	RO
04–05h	PCICMD	PCI Command	0000h	R/W, RO
06–07h	PCISTS	PCI Status	0290h	R/WC, RO
08h	RID	Revision Identification	See register description	RO
09h	PI	Programming Interface	00h	RO
0Ah	SCC	Sub Class Code	03h	RO
0Bh	BCC	Base Class Code	07h	RO
0Eh	HEADTYP	Header Type	00h	RO
10–13h	MMBAR	Modem Mixer Base Address	00000001h	R/W, RO
14–17h	MBAR	Modem Base Address	00000001h	R/W, RO
2C–2Dh	SVID	Subsystem Vendor Identification	0000h	R/WO
2E–2Fh	SID	Subsystem Identification	0000h	R/WO
34h	CAP_PTR	Capabilities Pointer	50h	RO
3Ch	INT_LN	Interrupt Line	00h	R/W
3Dh	INT_PN	Interrupt Pin	See register description	RO
50–51h	PID	PCI Power Management Capability ID	0001h	RO
52–53h	PC	Power Management Capabilities	C9C2h	RO
54–55h	PCS	Power Management Control and Status	0000h	R/W, R/WC

Note: Internal reset as a result of $D3_{HOT}$ to D0 transition will reset all the core well registers except the following BIOS programmed registers as BIOS may not be invoked following the D3-to-D0 transition. All resume well registers will not be reset by the $D3_{HOT}$ to D0 transition.

Core well registers **not** reset by the $D3_{HOT}$ to D0 transition:

- offset 2Ch–2Dh – Subsystem Vendor ID (SVID)
- offset 2Eh–2Fh – Subsystem ID (SID)

Resume well registers **will not** be reset by the $D3_{HOT}$ to D0 transition:

- offset 54h–55h – Power Management Control and Status (PCS)

20.1.1 VID – Vendor Identification Register (Modem – D30:F3)

Address Offset:	00–01h	Attribute:	RO
Default Value:	8086	Size:	16 Bits
Lockable:	No	Power Well:	Core

Bit	Description
15:0	Vendor ID – RO

20.1.2 DID – Device Identification Register (Modem – D30:F3)

Address Offset:	02–03h	Attribute:	RO
Default Value:	2699h	Size:	16 Bits
Lockable:	No	Power Well:	Core

Bit	Description
15:0	Device ID – RO

20.1.3 PCICMD – PCI Command Register (Modem – D30:F3)

Address Offset:	04–05h	Attribute:	R/W, RO
Default Value:	0000h	Size:	16 bits
Lockable:	No	Power Well:	Core

PCICMD is a 16-bit control register. Refer to the *PCI Local Bus Specification* for complete details on each bit.

Bit	Description
15:11	Reserved. Read 0.
10	**Interrupt Disable (ID) –** R/W. 0 = The INTx# signals may be asserted and MSIs may be generated. 1 = The AC '97 controller's INTx# signal will be de-asserted and it may not generate MSIs.
9	Fast Back to Back Enable (FBE) – RO. Not implemented. Hardwired to 0.
8	SERR# Enable (SERR_EN) – RO. Not implemented. Hardwired to 0.
7	Wait Cycle Control (WCC) – RO. Not implemented. Hardwired to 0.
6	Parity Error Response (PER) – RO. Not implemented. Hardwired to 0.
5	VGA Palette Snoop (VPS) – RO. Not implemented. Hardwired to 0.
4	Memory Write and Invalidate Enable (MWIE) – RO. Not implemented. Hardwired to 0.
3	Special Cycle Enable (SCE) – RO. Not implemented. Hardwired to 0.
2	**Bus Master Enable (BME) –** R/W. This bit controls standard PCI bus mastering capabilities. 0 = Disable 1 = Enable
1	Memory Space Enable (MSE) – RO. Hardwired to 0, AC '97 does not respond to memory accesses.
0	**I/O Space Enable (IOSE) –** R/W. This bit controls access to the I/O space registers. 0 = Disable access. (default = 0). 1 = Enable access to I/O space. The Native PCI Mode Base Address register should be programmed prior to setting this bit.

20.1.4 PCISTS – PCI Status Register (Modem – D30:F3)

Address Offset:	06–07h	Attribute:	R/WC, RO
Default Value:	0290h	Size:	16 bits
Lockable:	No	Power Well:	Core

PCISTA is a 16-bit status register. Refer to the *PCI Local Bus Specification* for complete details on each bit.

Note: For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 to the bit has no effect.

Bit	Description
15	Detected Parity Error (DPE) – RO. Not implemented. Hardwired to 0.
14	Signaled System Error (SSE) – RO. Not implemented. Hardwired to 0.
13	**Master Abort Status (MAS) –** R/WC. 0 = Master abort Not generated by bus master AC '97 function. 1 = Bus Master AC '97 interface function, as a master, generates a master abort.
12	Reserved. Read as 0.
11	Signaled Target Abort (STA) – RO. Not implemented. Hardwired to 0.
10:9	DEVSEL# Timing Status (DEV_STS) – RO. This 2-bit field reflects the Intel® 631xESB/632xESB I/O Controller Hub's DEVSEL# timing parameter. These read only bits indicate the Intel® 631xESB/ 632xESB I/O Controller Hub's DEVSEL# timing when performing a positive decode.
8	Data Parity Error Detected (DPED) – RO. Not implemented. Hardwired to 0.
7	Fast Back to Back Capable (FB2BC) – RO. Hardwired to 1. This bit indicates that the Intel® 631xESB/632xESB I/O Controller Hub as a target is capable of fast back-to-back transactions.
6	User Definable Features (UDF) – RO. Not implemented. Hardwired to 0.
5	66 MHz Capable (66MHZ_CAP) – RO. Hardwired to 0.
4	Capabilities List (CAP_LIST) – RO. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h.
3	**Interrupt Status (INTS) –** RO. 0 = This bit is 0 after the interrupt is cleared. 1 = This bit is 1 when the INTx# is asserted.
2:0	Reserved

20.1.5 RID – Revision Identification Register (Modem – D30:F3)

Address Offset:	08h	Attribute:	RO
Default Value:	See bit description	Size:	8 Bits
Lockable:	No	Power Well:	Core

Bit	Description
7:0	**Revision ID –** RO. Refer to Table 2-33 or the *Intel® 631xESB/632xESB I/O Controller Hub EDS Specification Update* for the value of the Revision ID Register

20.1.6 PI – Programming Interface Register (Modem – D30:F3)

Address Offset: 09h
Default Value: 00h
Lockable: No
Attribute: RO
Size: 8 bits
Power Well: Core

Bit	Description
7:0	Programming Interface – RO.

20.1.7 SCC – Sub Class Code Register (Modem – D30:F3)

Address Offset: 0Ah
Default Value: 03h
Lockable: No
Attribute: RO
Size: 8 bits
Power Well: Core

Bit	Description
7:0	Sub Class Code – RO. 03h = Generic Modem.

20.1.8 BCC – Base Class Code Register (Modem – D30:F3)

Address Offset: 0Bh
Default Value: 07h
Lockable: No
Attribute: RO
Size: 8 bits
Power Well: Core

Bit	Description
7:0	Base Class Code – RO. 07h = Simple Communications controller.

20.1.9 HEADTYP – Header Type Register (Modem – D30:F3)

Address Offset: 0Eh
Default Value: 00h
Lockable: No
Attribute: RO
Size: 8 bits
Power Well: Core

Bit	Description
7:0	Header Type – RO.

20.1.10 MMBAR – Modem Mixer Base Address Register (Modem – D30:F3)

Address Offset: 10–13h
Default Value: 00000001h
Attribute: R/W, RO
Size: 32 bits

The Native PCI Mode Modem uses PCI Base Address register #1 to request a contiguous block of I/O space that is to be used for the Modem Mixer software interface. The mixer requires 256 bytes of I/O space. All accesses to the mixer registers are forwarded over the AC-link to the codec where the registers reside.

In the case of the split codec implementation accesses to the different codecs are differentiated by the controller by using address offsets 00h–7Fh for the primary codec and address offsets 80h–FEh for the secondary codec.

Bit	Description
31:16	Hardwired to 0's.
15:8	**Base Address –** R/W. These bits are used in the I/O space decode of the Modem interface registers. The number of upper bits that a device actually implements depends on how much of the address space the device will respond to. For the AC '97 Modem, the upper 16 bits are hardwired to 0, while bits 15:8 are programmable. This configuration yields a maximum I/O block size of 256 bytes for this base address.
7:1	Reserved. Read as 0
0	Resource Type Indicator (RTE) – RO. Hardwired to 1indicating a request for I/O space.

20.1.11 MBAR – Modem Base Address Register (Modem – D30:F3)

Address Offset:	14–17h	Attribute:	R/W, RO
Default Value:	00000001h	Size:	32 bits

The Modem function uses PCI Base Address register #1 to request a contiguous block of I/O space that is to be used for the Modem software interface. The Modem Bus Mastering register space requires 128 bytes of I/O space. All Modem registers reside in the controller, therefore cycles are **not** forwarded over the AC-link to the codec.

Bit	Description
31:16	Hardwired to 0's.
15:7	**Base Address –** R/W. These bits are used in the I/O space decode of the Modem interface registers. The number of upper bits that a device actually implements depends on how much of the address space the device will respond to. For the AC '97 Modem, the upper 16 bits are hardwired to 0, while bits 15:7 are programmable. This configuration yields a maximum I/O block size of 128 bytes for this base address.
6:1	Reserved. Read as 0
0	Resource Type Indicator (RTE) **–** RO. Hardwired to 1 indicating a request for I/O space.

20.1.12 SVID – Subsystem Vendor Identification Register (Modem – D30:F3)

Address Offset:	2C–2Dh	Attribute:	R/WO
Default Value:	0000h	Size:	16 bits
Lockable:	No	Power Well:	Core

The SVID register, in combination with the Subsystem ID register, enable the operating environment to distinguish one audio subsystem from the other(s). This register is implemented as write-once register. Once a value is written to it, the value can be read back. Any subsequent writes will have no effect.

This register is not affected by the $D3_{HOT}$ to D0 transition.

Bit	Description
15:0	**Subsystem Vendor ID** – R/WO.

20.1.13 SID – Subsystem Identification Register (Modem – D30:F3)

Address Offset:	2E–2Fh	Attribute:	R/WO
Default Value:	0000h	Size:	16 bits
Lockable:	No	Power Well:	Core

The SID register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one audio subsystem from another. This register is implemented as write-once register. Once a value is written to it, the value can be read back. Any subsequent writes will have no effect.

This register is not affected by the $D3_{HOT}$ to D0 transition.

Bit	Description
15:0	**Subsystem ID** – R/WO.

20.1.14 CAP_PTR – Capabilities Pointer Register (Modem – D30:F3)

Address Offset:	34h	Attribute:	RO
Default Value:	50h	Size:	8 bits
Lockable:	No	Power Well:	Core

This register indicates the offset for the capability pointer.

Bit	Description
7:0	Capabilities Pointer (CAP_PTR) – RO. This field indicates that the first capability pointer offset is offset 50h

20.1.15 INT_LN – Interrupt Line Register (Modem – D30:F3)

Address Offset:	3Ch	Attribute:	R/W
Default Value:	00h	Size:	8 bits
Lockable:	No	Power Well:	Core

This register indicates which PCI interrupt line is used for the AC'97 module interrupt.

Bit	Description
7:0	Interrupt Line (INT_LN) – R/W. This data is not used by the Intel® 631xESB/632xESB I/O Controller Hub. It is used to communicate to software the interrupt line that the interrupt pin is connected to.

20.1.16 INT_PIN – Interrupt Pin Register (Modem – D30:F3)

Address Offset:	3Dh	Attribute:	RO
Default Value:	See description	Size:	8 bits
Lockable:	No	Power Well:	Core

This register indicates which PCI interrupt pin is used for the AC'97 modem interrupt. The AC'97 interrupt is internally OR'd to the interrupt controller with the PIRQB# signal.

Bit	Description
7:3	Reserved
2:0	Interrupt Pin (INT_PN) – RO. This reflects the value of D30IP.AMIP in chipset configuration space.

20.1.17 PID – PCI Power Management Capability Identification Register (Modem – D30:F3)

Address Offset:	50h	Attribute:	RO
Default Value:	0001h	Size:	16 bits
Lockable:	No	Power Well:	Core

Bit	Description
15:8	Next Capability (NEXT) – RO. This field indicates that this is the last item in the list.
7:0	Capability ID (CAP) – RO. This field indicates that this pointer is a message signaled interrupt capability.

20.1.18 PC – Power Management Capabilities Register (Modem – D30:F3)

Address Offset:	52h	Attribute:	RO
Default Value:	C9C2h	Size:	16 bits
Lockable:	No	Power Well:	Core

Bit	Description
15:11	PME Support – RO. This field indicates PME# can be generated from all D states.
10:9	Reserved.
8:6	Auxiliary Current – RO. This field reports 375 mA maximum Suspend well current required when in the $D3_{COLD}$ state.
5	Device Specific Initialization (DSI) – RO. This bit indicates that no device-specific initialization is required.
4	Reserved – RO.
3	PME Clock (PMEC) – RO. This bit indicates that PCI clock is not required to generate PME#.
2:0	Version (VS) – RO. This field indicates support for Revision 1.1 of the PCI Power Management Specification.

20.1.19 PCS – Power Management Control and Status Register (Modem – D30:F3)

Address Offset:	54h	Attribute:	R/W, R/WC
Default Value:	0000h	Size:	16 bits
Lockable:	No	Power Well:	Resume

This register is not affected by the $D3_{HOT}$ to D0 transition.

Bit	Description
15	**PME Status (PMES) –** R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = This bit is set when the AC'97 controller would normally assert the PME# signal independent of the state of the PME_En bit. This bit resides in the resume well.
14:9	Reserved – RO.

Bit	Description
8	**PME Enable (PMEE) –** R/W. 0 = Disable. 1 = Enable. When set, and if corresponding PMES is also set, the AC '97 controller sets the AC97_STS bit in the GPE0_STS register
7:2	Reserved – RO.
1:0	**Power State (PS) –** R/W. This field is used both to determine the current power state of the AC'97 controller and to set a new power state. The values are: 00 = D0 state 01 = not supported 10 = not supported 11 = $D3_{HOT}$ state When in the $D3_{HOT}$ state, the AC'97 controller's configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked. If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs.

20.2 AC'97 Modem I/O Space (D30:F3)

In the case of the split codec implementation accesses to the modem mixer registers in different codecs are differentiated by the controller by using address offsets 00h–7Fh for the primary codec and address offsets 80h–FEh for the secondary codec. Table 20-2 shows the register addresses for the modem mixer registers.

Table 20-2. Intel® 631xESB/632xESB I/O Controller Hub Modem Mixer Register Configuration

Register		MMBAR Exposed Registers (D30:F3)
Primary	Secondary	Name
00h:38h	80h:B8h	Intel RESERVED
3Ch	BCh	Extended Modem ID
3Eh	BEh	Extended Modem Stat/Ctrl
40h	C0h	Line 1 DAC/ADC Rate
42h	C2h	Line 2 DAC/ADC Rate
44h	C4h	Handset DAC/ADC Rate
46h	C6h	Line 1 DAC/ADC Level Mute
48h	C8h	Line 2 DAC/ADC Level Mute
4Ah	CAh	Handset DAC/ADC Level Mute
4Ch	CCh	GPIO Pin Config
4Eh	CEh	GPIO Polarity/Type
50h	D0h	GPIO Pin Sticky
52h	D2h	GPIO Pin wakeup
54h	D4h	GPIO Pin Status
56h	D6h	Misc. Modem AFE Stat/Ctrl
58h	D8h	AC'97 Reserved
5Ah	DAh	Vendor Reserved
7Ch	FCh	Vendor ID1
7Eh	FEh	Vendor ID2

Notes:
1. Registers in italics are for functions not supported by the Intel® 631xESB/632xESB I/O Controller Hub

2. Software should not try to access reserved registers
3. The Intel® 631xESB/632xESB I/O Controller Hub supports a modem codec connected to ACZ_SDIN[2:0], as long as the Codec ID is 00 or 01. However, the Intel® 631xESB/632xESB I/O Controller Hub does not support more than one modem codec. For a complete list of topologies, see your Intel® 631xESB/632xESB I/O Controller Hub enabled Platform Design Guide.

The Global Control (GLOB_CNT) and Global Status (GLOB_STA) registers are aliased to the same global registers in the audio and modem I/O space. Therefore a read/write to these registers in either audio or modem I/O space affects the same physical register. Software could access these registers as bytes, word, DWord quantities, but reads must not cross DWord boundaries.

These registers exist in I/O space and reside in the AC'97 controller. The two channels, Modem in and Modem out, each have their own set of Bus Mastering registers. The following register descriptions apply to both channels. The naming prefix convention used is as follows:
MI = Modem in channel
MO = Modem out channel

Table 20-3. Modem Registers

Offset	Mnemonic	Name	Default	Access
00h–03h	MI_BDBAR	Modem In Buffer Descriptor List Base Address	00000000h	R/W
04h	MI_CIV	Modem In Current Index Value	00h	RO
05h	MI_LVI	Modem In Last Valid Index	00h	R/W
06h–07h	MI_SR	Modem In Status	0001h	R/WC, RO
08h–09h	MI_PICB	Modem In Position In Current Buffer	0000h	RO
0Ah	MI_PIV	Modem In Prefetch Index Value	00h	RO
0Bh	MI_CR	Modem In Control	00h	R/W, R/W (special)
10h–13h	MO_BDBAR	Modem Out Buffer Descriptor List Base Address	00000000h	R/W
14h	MO_CIV	Modem Out Current Index Value	00h	RO
15h	MO_LVI	Modem Out Last Valid	00h	R/W
16h–17h	MO_SR	Modem Out Status	0001h	R/WC, RO
18h–19h	MI_PICB	Modem In Position In Current Buffer	0000h	RO
1Ah	MO_PIV	Modem Out Prefetched Index	00h	RO
1Bh	MO_CR	Modem Out Control	00h	R/W, R/W (special)
3Ch–3Fh	GLOB_CNT	Global Control	00000000h	R/W, R/W (special)
40h–43h	GLOB_STA	Global Status	00300000h	RO, R/W, R/WC
44h	CAS	Codec Access Semaphore	00h	R/W (special)

Note: MI = Modem in channel; MO = Modem out channel

Note: Internal reset as a result of $D3_{HOT}$ to D0 transition will reset all the core well registers except the registers shared with the AC'97 audio controller (GCR, GSR, CASR). All resume well registers will not be reset by the $D3_{HOT}$ to D0 transition.

Core well registers and bits **not** reset by the $D3_{HOT}$ to D0 transition:

- offset 3Ch–3Fh – bits [6:0] Global Control (GLOB_CNT)
- offset 40h–43h – bits [29,15,11:10] Global Status (GLOB_STA)

- offset 44h – Codec Access Semaphore Register (CAS)

Resume well registers and bits **will not** be reset by the $D3_{HOT}$ to D0 transition:

- offset 40h–43h – bits [17:16] Global Status (GLOB_STA)

20.2.1 *X*_BDBAR – Buffer Descriptor List Base Address Register (Modem – D30:F3)

I/O Address:	MBAR + 00h (MIBDBAR), MBAR + 10h (MOBDBAR)	Attribute:	R/W
Default Value:	00000000h	Size:	32bits
Lockable:	No	Power Well:	Core

Software can read the register at offset 00h by performing a single 32-bit read from address offset 00h. Reads across DWord boundaries are not supported.

Bit	Description
31:3	**Buffer Descriptor List Base Address [31:3] –** R/W. These bits represent address bits 31:3. The entries should be aligned on 8-byte boundaries.
2:0	Hardwired to 0.

20.2.2 *X*_CIV – Current Index Value Register (Modem – D30:F3)

I/O Address:	MBAR + 04h (MICIV), MBAR + 14h (MOCIV),	Attribute:	RO
Default Value:	00h	Size:	8bits
Lockable:	No	Power Well:	Core

Software can read the registers at offsets 04h, 05h and 06h simultaneously by performing a single, 32-bit read from address offset 04h. Software can also read this register individually by doing a single, 8-bit read to offset 04h. Reads across DWord boundaries are not supported.

Bit	Description
7:5	Hardwired to 0.
4:0	**Current Index Value [4:0] –** RO. These bits represent which buffer descriptor within the list of 16 descriptors is being processed currently. As each descriptor is processed, this value is incremented.

20.2.3 *X*_LVI – Last Valid Index Register (Modem – D30:F3)

I/O Address:	MBAR + 05h (MILVI), MBAR + 15h (MOLVI)	Attribute:	R/W
Default Value:	00h	Power Well:	Core

Software can read the registers at offsets 04h, 05h and 06h simultaneously by performing a single, 32-bit read from address offset 04h. Software can also read this register individually by doing a single, 8-bit read to offset 05h. Reads across DWord boundaries are not supported.

Bit	Description
7:5	Hardwired to 0
4:0	**Last Valid Index [4:0] –** R/W. These bits indicate the last valid descriptor in the list. This value is updated by the software as it prepares new buffers and adds to the list.

20.2.4 *X*_SR – Status Register (Modem – D30:F3)

I/O Address:	MBAR + 06h (MISR), MBAR + 16h (MOSR)	Attribute:	R/WC, RO
Default Value:	0001h	Size:	16 bits
Lockable:	No	Power Well:	Core

Software can read the registers at offsets 04h, 05h and 06h simultaneously by performing a single, 32-bit read from address offset 04h. Software can also read this register individually by doing a single, 16-bit read to offset 06h. Reads across DWord boundaries are not supported.

Bit	Description
15:5	Reserved
4	**FIFO Error (FIFOE) –** R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = FIFO error occurs. **Modem in:** FIFO error indicates a FIFO overrun. The FIFO pointers don't increment, the incoming data is not written into the FIFO, thereby being lost. **Modem out:** FIFO error indicates a FIFO underrun. The sample transmitted in this case should be the last valid sample. The Intel® 631xESB/632xESB I/O Controller Hub will set the FIFOE bit if the under-run or overrun occurs when there are more valid buffers to process.
3	**Buffer Completion Interrupt Status (BCIS) –** R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = Set by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. Remains active until software clears bit.
2	**Last Valid Buffer Completion Interrupt (LVBCI) –** R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = Set by hardware when last valid buffer has been processed. It remains active until cleared by software. This bit indicates the occurrence of the event signified by the last valid buffer being processed. Thus, this is an event status bit that can be cleared by software once this event has been recognized. This event will cause an interrupt if the enable bit in the Control Register is set. The interrupt is cleared when the software clears this bit. In the case of transmits (PCM out, Modem out) this bit is set, after the last valid buffer has been fetched (not after transmitting it). While in the case of Receives, this bit is set after the data for the last buffer has been written to memory.
1	**Current Equals Last Valid (CELV)** – RO. 0 = Hardware clears when controller exists state (that is, until a new value is written to the LVI register). 1 = Current Index is equal to the value in the Last Valid Index Register, AND the buffer pointed to by the CIV has been processed (that is, after the last valid buffer has been processed). This bit is very similar to bit 2, except, this bit reflects the state rather than the event. This bit reflects the state of the controller, and remains set until the controller exits this state.
0	**DMA Controller Halted (DCH)** – RO. 0 = Running. 1 = Halted. This could happen because of the Start/Stop bit being cleared and the DMA engines are idle, or it could happen once the controller has processed the last valid buffer.

20.2.5 *X*_PICB – Position in Current Buffer Register (Modem – D30:F3)

I/O Address:	MBAR + 08h (MIPICB), MBAR + 18h (MOPICB),	Attribute:	RO
Default Value:	0000h	Size:	16 bits
Lockable:	No	Power Well:	Core

Software can read the registers at the offsets 08h, 0Ah, and 0Bh by performing a 32-bit read from the address offset 08h. Software can also read this register individually by doing a single, 16-bit read to offset 08h. Reads across DWord boundaries are not supported.

Bit	Description
15:0	**Position In Current Buffer[15:0]** – RO. These bits represent the number of samples left to be processed in the current buffer.

20.2.6 *X*_PIV – Prefetch Index Value Register (Modem – D30:F3)

I/O Address:	MBAR + 0Ah (MIPIV), MBAR + 1Ah (MOPIV)	Attribute:	RO
Default Value:	00h	Size:	8 bits
Lockable:	No	Power Well:	Core

Software can read the registers at the offsets 08h, 0Ah, and 0Bh by performing a 32-bit read from the address offset 08h. Software can also read this register individually by doing a single, 8-bit read to offset 0Ah. Reads across DWord boundaries are not supported.

Bit	Description
7:5	Hardwired to 0
4:0	**Prefetched Index Value [4:0] –** RO. These bits represent which buffer descriptor in the list has been prefetched.

20.2.7 *X*_CR – Control Register (Modem – D30:F3)

I/O Address:	MBAR + 0Bh (MICR), MBAR + 1Bh (MOCR)	Attribute:	R/W, R/W (special)
Default Value:	00h	Size:	8 bits
Lockable:	No	Power Well:	Core

Software can read the registers at the offsets 08h, 0Ah, and 0Bh by performing a 32-bit read from the address offset 08h. Software can also read this register individually by doing a single, 8-bit read to offset 0Bh. Reads across DWord boundaries are not supported.

Bit	Description
7:5	Reserved
4	**Interrupt on Completion Enable (IOCE) –** R/W. This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. 0 = Disable 1 = Enable
3	**FIFO Error Interrupt Enable (FEIE) –** R/W. This bit controls whether the occurrence of a FIFO error will cause an interrupt or not. 0 = Disable. Bit 4 in the Status Register will be set, but the interrupt will not occur. 1 = Enable. Interrupt will occur
2	**Last Valid Buffer Interrupt Enable (LVBIE) –** R/W. This bit controls whether the completion of the last valid buffer will cause an interrupt or not. 0 = Disable. Bit 2 in the Status register will still be set, but the interrupt will not occur. 1 = Enable
1	**Reset Registers (RR) –** R/W (special). 0 = Removes reset condition. 1 = Contents of all registers to be reset, except the interrupt enable bits (bit 4,3,2 of this register). Software needs to set this bit. It must be set only when the Run/Pause bit is cleared. Setting it when the Run bit is set will cause undefined consequences. This bit is self-clearing (software needs not clear it).
0	**Run/Pause Bus Master (RPBM) –** R/W. 0 = Pause bus master operation. This results in all state information being retained (that is, master mode operation can be stopped and then resumed). 1 = Run. Bus master operation starts.

20.2.8 GLOB_CNT – Global Control Register (Modem – D30:F3)

I/O Address:	MBAR + 3Ch	Attribute:	R/W, R/W (special)
Default Value:	00000000h	Size:	32 bits
Lockable:	No	Power Well:	Core

Bit	Description
31:6	Reserved.
6	**ACZ_SDIN2 Interrupt Enable (S2RE) –** R/W. 0 = Disable. 1 = Enable an interrupt to occur when the codec on the ACZ_SDIN2 causes a resume event on the AC-link.
5	ACZ_SDIN1 Resume Interrupt Enable (S1RE) – R/W. 0 = Disable. 1 = Enable an interrupt to occur when the codec on the ACZ_SDIN1 causes a resume event on the AC-link.
4	ACZ_SDIN0 Resume Interrupt Enable (S0RE) – R/W. 0 = Disable. 1 = Enable an interrupt to occur when the codec on ACZ_SDIN0 causes a resume event on the AC-link.
3	AC-LINK Shut Off (LSO) – R/W. 0 = Normal operation. 1 = Controller disables all outputs which will be pulled low by internal pull down resistors.

Bit	Description
2	AC'97 Warm Reset – R/W (special). 0 = Normal operation. 1 = Writing a 1 to this bit causes a warm reset to occur on the AC-link. The warm reset will awaken a suspended codec without clearing its internal registers. If software attempts to perform a warm reset while bit_clk is running, the write will be ignored and the bit will not change. This bit is self-clearing (it remains set until the reset completes and bit_clk is seen on the AC-link, after which it clears itself).
1	**AC'97 Cold Reset# –** R/W. 0 = Writing a 0 to this bit causes a cold reset to occur throughout the AC '97 circuitry. All data in the controller and the codec will be lost. Software needs to clear this bit no sooner than the minimum number of ms have elapsed. 1 = This bit defaults to 0 and hence after reset, the driver needs to set this bit to a 1. The value of this bit is retained after suspends; hence, if this bit is set to a 1 prior to suspending, a cold reset is not generated automatically upon resuming. Note: This bit is in the Core well.
0	**GPI Interrupt Enable (GIE) –** R/W. This bit controls whether the change in status of any GPI causes an interrupt. 0 = Bit 0 of the Global Status Register is set, but no interrupt is generated. 1 = The change on value of a GPI causes an interrupt and sets bit 0 of the Global Status Register. ***Note:*** This bit is cleared by the AC '97 Modem function $D3_{HOT}$ to D0 reset.

Note: Reads across DWord boundaries are not supported.

20.2.9 GLOB_STA – Global Status Register (Modem – D30:F3)

I/O Address:	MBAR + 40h	Attribute:	RO, R/W, R/WC
Default Value:	00300000h	Size:	32 bits
Lockable:	No	Power Well:	Core

Bit	Description
31:30	Reserved.
29	**ACZ_SDIN2 Resume Interrupt (S2RI)** – R/WC. This bit indicates a resume event occurred on ACZ_SDIN2. 0 = Software clears this bit by writing a 1 to it. 1 = Resume event occurred. This bit is not affected by $D3_{HOT}$ to D0 Reset.
28	**ACZ_SDIN2 Codec Ready (S2CR)** – RO. This bit reflects the state of the codec ready bit on ACZ_SDIN2. Bus masters ignore the condition of the codec ready bits, so software must check this bit before starting the bus masters. Once the codec is "ready", it must never go "not ready" spontaneously. 0 = Not Ready. 1 = Ready.
27	**Bit Clock Stopped (BCS)** – RO. This bit indicates that the bit clock is not running. 0 = Transition is found on BIT_CLK. 1 = Intel® 631xESB/632xESB I/O Controller Hub detects that there has been no transition on BIT_CLK for four consecutive PCI clocks.
26	**S/PDIF* Interrupt (SPINT)** – RO. 0 = When the specific status bit is cleared, this bit will be cleared. 1 = S/PDIF out channel interrupt status bits have been set.
25	**PCM In 2 Interrupt (P2INT) –** RO. 0 = When the specific status bit is cleared, this bit will be cleared. 1 = One of the PCM In 2 channel status bits have been set.
24	**Microphone 2 In Interrupt (M2INT) –** RO. 0 = When the specific status bit is cleared, this bit will be cleared. 1 = One of the Mic in channel interrupts status bits has been set.

Bit	Description
23:22	**Sample Capabilities** – RO. This field indicates the capability to support more greater than 16-bit audio. 00 = Reserved 01 = 16 and 20-bit Audio supported (Intel® 631xESB/632xESB I/O Controller Hub value) 10 = Reserved 11 = Reserved
21:20	**Multichannel Capabilities** – RO. This field indicates the capability to support 4 and 6 channels on PCM Out.
19:18	Reserved.
17	**MD3 –** R/W. Power down semaphore for Modem. This bit exists in the suspend well and maintains context across power states (except G3). The bit has no hardware function. It is used by software in conjunction with the AD3 bit to coordinate the entry of the two codecs into D3 state. This bit is not affected by $D3_{HOT}$ to D0 Reset.
16	**AD3 –** R/W. Power down semaphore for Audio. This bit exists in the suspend well and maintains context across power states (except G3). The bit has no hardware function. It is used by software in conjunction with the MD3 bit to coordinate the entry of the two codecs into D3 state. This bit is not affected by $D3_{HOT}$ to D0 Reset.
15	**Read Completion Status (RCS) –** R/WC. This bit indicates the status of codec read completions. Software clears this bit by writing a 1 to it. 0 = A codec read completes normally. 1 = A codec read results in a time-out. This bit is not affected by $D3_{HOT}$ to D0 Reset.
14	**Bit 3 of Slot 12** – RO. Display bit 3 of the most recent slot 12.
13	**Bit 2 of Slot 12** – RO. Display bit 2 of the most recent slot 12.
12	**Bit 1 of Slot 12** – RO. Display bit 1 of the most recent slot 12.
11	**ACZ_SDIN1 Resume Interrupt (S1RI) –** R/WC. This bit indicates that a resume event occurred on ACZ_SDIN1. Software clears this bit by writing a 1 to it. 0 = Resume event did Not occur. 1 = Resume event occurred. This bit is not affected by $D3_{HOT}$ to D0 Reset.
10	**ACZ_SDIN0 Resume Interrupt (S0RI) –** R/WC. This bit indicates that a resume event occurred on ACZ_SDIN0. Software clears this bit by writing a 1 to it. 0 = Resume event did Not occur. 1 = Resume event occurred. This bit is not affected by $D3_{HOT}$ to D0 Reset.
9	**ACZ_SDIN1 Codec Ready (S1CR)** – RO. This bit reflects the state of the codec ready bit in ACZ_SDIN1. Bus masters ignore the condition of the codec ready bits, so software must check this bit before starting the bus masters. Once the codec is "ready", it must never go "not ready" spontaneously. 0 = Not Ready. 1 = Ready.
8	**ACZ_SDIN0 Codec Ready (S0CR)** – RO. This bit reflects the state of the codec ready bit in ACZ_SDIN 0. Bus masters ignore the condition of the codec ready bits, so software must check this bit before starting the bus masters. Once the codec is "ready", it must never go "not ready" spontaneously. 0 = Not Ready. 1 = Ready.
7	**Microphone In Interrupt (MINT)** – RO. 0 = When the specific status bit is cleared, this bit will be cleared. 1 = One of the Mic in channel interrupts status bits has been set.
6	**PCM Out Interrupt (POINT)** – RO. 0 = When the specific status bit is cleared, this bit will be cleared. 1 = One of the PCM out channel interrupts status bits has been set.
5	**PCM In Interrupt (PIINT)** – RO. 0 = When the specific status bit is cleared, this bit will be cleared. 1 = One of the PCM in channel interrupts status bits has been set.
4:3	Reserved

Bit	Description
2	**Modem Out Interrupt (MOINT)** – RO. 0 = When the specific status bit is cleared, this bit will be cleared. 1 = One of the modem out channel interrupts status bits has been set.
1	**Modem In Interrupt (MIINT)** – RO. 0 = When the specific status bit is cleared, this bit will be cleared. 1 = One of the modem in channel interrupts status bits has been set.
0	**GPI Status Change Interrupt (GSCI) –** R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = This bit reflects the state of bit 0 in slot 12, and is set when bit 0 of slot 12 is set. This indicates that one of the GPI's changed state, and that the new values are available in slot 12. This bit is not affected by AC '97 Audio Modem function $D3_{HOT}$ to D0 Reset.

Note: On reads from a codec, the controller will give the codec a maximum of four frames to respond, after which if no response is received, it will return a dummy read completion to the processor (with all F's on the data) and also set the Read Completion Status bit in the Global Status Register.

Note: Reads across DWord boundaries are not supported.

20.2.10 CAS – Codec Access Semaphore Register (Modem – D30:F3)

I/O Address:	NABMBAR + 44h	Attribute:	R/W (special)
Default Value:	00h	Size:	8 bits
Lockable:	No	Power Well:	Core

Bit	Description
7:1	Reserved
0	**Codec Access Semaphore (CAS) –** R/W (special). This bit is read by software to check whether a codec access is currently in progress. 0 = No access in progress. 1 = The act of reading this register sets this bit to 1. The driver that read this bit can then perform an I/O access. Once the access is completed, hardware automatically clears this bit.

Note: Reads across DWord boundaries are not supported.

§§

21 LPC Interface Bridge Registers (D31:F0)

The LPC bridge function of the Intel® 631xESB/632xESB I/O Controller Hub resides in PCI Device 31:Function 0. This function contains many other functional units, such as DMA and Interrupt controllers, Timers, Power Management, System Management, GPIO, RTC, and LPC Configuration Registers.

Registers and functions associated with other functional units (EHCI, UHCI, IDE, and so forth) are described in their respective sections.

21.1 PCI Configuration Registers (LPC I/F – D31:F0)

Note: Address locations that are not shown should be treated as Reserved.

Table 21-1. LPC Interface PCI Register Address Map (LPC I/F – D31:F0) (Sheet 1 of 2)

Offset	Mnemonic	Register Name	Default	Type
00–01h	VID	Vendor Identification	8086h	RO
02–03h	DID	Device Identification	See register description	RO
04–05h	PCICMD	PCI Command	0007h	R/W, RO
06–07h	PCISTS	PCI Status	0200h	R/WC, RO
08h	RID	Revision Identification	See register description.	R/WO
09h	PI	Programming Interface	00h	RO
0Ah	SCC	Sub Class Code	01h	RO
0Bh	BCC	Base Class Code	06h	RO
0D	PLT	Primary Latency Timer	00h	RO
0Eh	HEADTYP	Header Type	80h	RO
2C–2Fh	SS	Sub System Identifiers	00000000h	R/WO
40–43h	PMBASE	ACPI Base Address	00000001h	R/W, RO
44h	ACPI_CNTL	ACPI Control	00h	R/W
48–4Bh	GPIOBASE	GPIO Base Address	00000001h	R/W, RO
4C	GC	GPIO Control	00h	R/W
60–63h	PIRQ[*n*]_ROUT	PIRQ[A–D] Routing Control	80h	R/W
64h	SIRQ_CNTL	Serial IRQ Control	10h	R/W
68–6Bh	PIRQ[*n*]_ROUT	PIRQ[E–H] Routing Control	80h	R/W
80h	LPC_I/O_DEC	I/O Decode Ranges	0000h	R/W
82–83h	LPC_EN	LPC I/F Enables	0000h	R/W
84–85h	GEN1_DEC	LPC I/F Generic Decode Range 1	0000h	R/W
88–89h	GEN2_DEC	LPC I/F Generic Decode Range 2	0000h	R/W
A0–CFh		Power Management (See Section 21.8.1)		
D0–D3h	FWH_SEL1	Firmware Hub Select 1	00112233h	R/W, RO

Table 21-1. LPC Interface PCI Register Address Map (LPC I/F – D31:F0) (Sheet 2 of 2)

Offset	Mnemonic	Register Name	Default	Type
D4–D5h	FWH_SEL2	Firmware Hub Select 2	4567h	R/W
D8–D9h	FWH_DEC_EN1	Firmware Hub Decode Enable 1	FFCFh	R/W, RO
DCh	BIOS_CNTL	BIOS Control	00h	R/WLO, R/W
F0h	RCBA	Root Complex Base Address	00h	R/W

21.1.1 VID – Vendor Identification Register (LPC I/F – D31:F0)

Offset Address: 00–01h
Default Value: 8086h
Lockable: No
Attribute: RO
Size: 16-bit
Power Well: Core

Bit	Description
15:0	Vendor ID – RO. This is a 16-bit value assigned to Intel. Intel VID = 8086h

21.1.2 DID – Device Identification Register (LPC I/F – D31:F0)

Offset Address: 02–03h
Default Value: See bits description
Lockable: No
Attribute: RO
Size: 16-bit
Power Well: Core

Bit	Description
15:0	Device ID – RO. This is a 16-bit value assigned to the Intel® 631xESB/632xESB I/O Controller Hub LPC bridge. The upper 12-bits of this register are hardwired to 267h. The lower 4 bits are controlled by the FDCOMP fuse. Refer to Table 2-33

21.1.3 PCICMD – PCI COMMAND Register (LPC I/F – D31:F0)

Offset Address: 04–05h
Default Value: 0007h
Lockable: No
Attribute: R/W, RO
Size: 16-bit
Power Well: Core

Bit	Description
15:10	Reserved
9	Fast Back to Back Enable (FBE) – RO. Hardwired to 0.
8	**SERR# Enable (SERR_EN) –** R/W. The LPC bridge generates SERR# if this bit is set.
7	Wait Cycle Control (WCC) – RO. Hardwired to 0.
6	**Parity Error Response Enable (PERE) –** R/W. 0 = No action is taken when detecting a parity error. 1 = Enables the Intel® 631xESB/632xESB I/O Controller Hub LPC bridge to respond to parity errors detected on backbone interface.
5	VGA Palette Snoop (VPS) – RO. Hardwired to 0.
4	Memory Write and Invalidate Enable (MWIE) – RO. Hardwired to 0.
3	Special Cycle Enable (SCE) – RO. Hardwired to 0.
2	Bus Master Enable (BME) – RO. Bus Masters cannot be disabled.
1	Memory Space Enable (MSE) – RO. Memory space cannot be disabled on LPC.
0	I/O Space Enable (IOSE) – RO. I/O space cannot be disabled on LPC.

21.1.4 PCISTS – PCI Status Register (LPC I/F – D31:F0)

Offset Address:	06–07h	Attribute:	RO, R/WC
Default Value:	0200h	Size:	16-bit
Lockable:	No	Power Well:	Core

Note: For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 to the bit has no effect.

Bit	Description
15	**Detected Parity Error (DPE) –** R/WC. Set when the LPC bridge detects a parity error on the internal backbone. Set even if the PCICMD.PERE bit (D31:F0:04, bit 6) is 0 0 = Parity Error Not detected. 1 = Parity Error detected.
14	**Signaled System Error (SSE)** – R/WC. Set when the LPC bridge signals a system error to the internal SERR# logic.
13	**Master Abort Status (RMA) –** R/WC. 0 = Unsupported request status not received. 1 = The bridge received a completion with unsupported request status from the backbone.
12	**Received Target Abort (RTA) –** R/WC. 0 = Completion abort not received. 1 = Completion with completion abort received from the backbone.
11	**Signaled Target Abort (STA) –** R/WC. 0 = Target abort Not generated on the backbone. 1 = LPC bridge generated a completion packet with target abort status on the backbone.
10:9	**DEVSEL# Timing Status (DEV_STS) –** RO. 01 = Medium Timing.
8	**Data Parity Error Detected (DPED) –** R/WC. 0 = All conditions listed below Not met. 1 = Set when all three of the following conditions are met: • LPC bridge receives a completion packet from the backbone from a previous request, • Parity error has been detected (D31:F0:06, bit 15) • PCICMD.PERE bit (D31:F0:04, bit 6) is set.
7	Fast Back to Back Capable (FBC): Reserved – bit has no meaning on the internal backbone.
6	Reserved.
5	66 MHz Capable (66MHZ_CAP) – Reserved – bit has no meaning on internal backbone.
4	Capabilities List (CLIST) – RO. No capability list exist on the LPC bridge.
3	Interrupt Status (IS) – RO. The LPC bridge does not generate interrupts.
2:0	Reserved.

21.1.5 RID – Revision Identification Register (LPC I/F – D31:F0)

Offset Address:	08h	Attribute:	R/WO
Default Value:	See bit description	Size:	8 bits

BIOS must always read this register and write the value back before passing control to the OS. Once written, additional writes to this register will not have any affect until a core-well reset occurs.

Bit	Description
7:0	**Revision ID –** RO. Refer to Table 2-33 or the *Intel® 631xESB/632xESB I/O Controller Hub EDS Specification Update* for the value of the Revision ID Register

21.1.6 PI – Programming Interface Register (LPC I/F – D31:F0)

Offset Address: 09h Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Description
7:0	**Programming Interface** – RO.

21.1.7 SCC – Sub Class Code Register (LPC I/F – D31:F0)

Offset Address: 0Ah Attribute: RO
Default Value: 01h Size: 8 bits

Bit	Description
7:0	**Sub Class Code** – RO. 8-bit value that indicates the category of bridge for the LPC bridge. 01h = PCI-to-ISA bridge.

21.1.8 BCC – Base Class Code Register (LPC I/F – D31:F0)

Offset Address: 0Bh Attribute: RO
Default Value: 06h Size: 8 bits

Bit	Description
7:0	**Base Class Code** – RO. 8-bit value that indicates the type of device for the LPC bridge. 06h = Bridge device.

21.1.9 PLT – Primary Latency Timer Register (LPC I/F – D31:F0)

Offset Address: 0Dh Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Description
7:3	Master Latency Count (MLC) – Reserved.
2:0	Reserved.

21.1.10 HEADTYP – Header Type Register (LPC I/F – D31:F0)

Offset Address: 0Eh Attribute: RO
Default Value: 80h Size: 8 bits

Bit	Description
7	**Multi-Function Device –** RO. This bit is 1 to indicate a multi-function device.
6:0	**Header Type –** RO. This 7-bit field identifies the header layout of the configuration space.

21.1.11 SS – Sub System Identifiers Register (LPC I/F – D31:F0)

Offset Address: 2C–2Fh Attribute: R/WO
Default Value: 00000000h Size: 32 bits

This register is initialized to logic 0 by the assertion of PLTRST#. This register can be written only once after PLTRST# de-assertion.

Bit	Description
31:16	**Subsystem ID (SSID) –** R/WO This is written by BIOS. No hardware action taken on this value.
15:0	**Subsystem Vendor ID (SSVID) –** R/WO This is written by BIOS. No hardware action taken on this value.

21.1.12 PMBASE – ACPI Base Address Register (LPC I/F – D31:F0)

Offset Address:	40–43h	Attribute:	R/W, RO
Default Value:	00000001h	Size:	32 bit
Lockable:	No	Usage:	ACPI, Legacy
		Power Well:	Core

Sets base address for ACPI I/O registers, GPIO registers and TCO I/O registers. These registers can be mapped anywhere in the 64-K I/O space on 128-byte boundaries.

Bit	Description
31:16	Reserved
15:7	**Base Address** – R/W. This field provides 128 bytes of I/O space for ACPI, GPIO, and TCO logic. This is placed on a 128-byte boundary.
6:1	Reserved
0	Resource Type Indicator (RTE) – RO. Hardwired to 1 to indicate I/O space.

21.1.13 ACPI_CNTL – ACPI Control Register (LPC I/F – D31:F0)

Offset Address:	44h	Attribute:	R/W
Default Value:	00h	Size:	8 bit
Lockable:	No	Usage:	ACPI, Legacy
		Power Well:	Core

Bit	Description
7	**ACPI Enable (ACPI_EN) –** R/W. 0 = Disable. 1 = Decode of the I/O range pointed to by the ACPI base register is enabled, and the ACPI power management function is enabled.
6:3	Reserved
2:0	**SCI IRQ Select (SCI_IRQ_SEL) –** R/W. Specifies on which IRQ the SCI will internally appear. If not using the APIC, the SCI must be routed to IRQ9–11, and that interrupt is not sharable with the SERIRQ stream, but is shareable with other PCI interrupts. If using the APIC, the SCI can also be mapped to IRQ20–23, and can be shared with other interrupts. **BitsSCI Map** 000IRQ9 001IRQ10 010 IRQ11 011Reserved 100IRQ20 (Only available if APIC enabled) 101IRQ21 (Only available if APIC enabled) 110IRQ22 (Only available if APIC enabled) 111IRQ23 (Only available if APIC enabled) ***Note:*** When the TCO interrupt is mapped to APIC interrupts 9, 10 or 11, the signal is in fact active high. When the TCO interrupt is mapped to IRQ 20, 21, 22, or 23, the signal is active low and can be shared with PCI interrupts that may be mapped to those same signals (IRQs).

21.1.14 GPIOBASE – GPIO Base Address Register (LPC I/F – D31:F0)

Offset Address: 48–4Bh
Default Value: 00000001h
Attribute: R/W, RO
Size: 32 bit

Bit	Description
31:16	Reserved. Always 0.
15:6	**Base Address (BA) –** R/W. Provides the 64 bytes of I/O space for GPIO.
5:1	Reserved. Always 0.
0	RO. Hardwired to 1 to indicate I/O space.

21.1.15 GC – GPIO Control Register (LPC I/F – D31:F0)

Offset Address: 4Ch
Default Value: 00h
Attribute: R/W
Size: 8 bit

Bit	Description
7:5	Reserved.
4	**GPIO Enable (EN) –** R/W. This bit enables/disables decode of the I/O range pointed to by the GPIO Base Address register (D31:F0:48h) and enables the GPIO function. 0 = Disable. 1 = Enable.
3:0	Reserved.

21.1.16 PIRQ[n]_ROUT – PIRQ[A,B,C,D] Routing Control Register (LPC I/F – D31:F0)

Offset Address: PIRQA – 60h, PIRQB – 61h, PIRQC – 62h, PIRQD – 63h
Default Value: 80h
Lockable: No
Attribute: R/W
Size: 8 bit
Power Well: Core

Bit	Description
7	**Interrupt Routing Enable (IRQEN) –** R/W. 0 = The corresponding PIRQ is routed to one of the ISA-compatible interrupts specified in bits[3:0]. 1 = The PIRQ is not routed to the 8259. ***Note:*** BIOS must program this bit to 0 during POST for any of the PIRQs that are being used. The value of this bit may subsequently be changed by the OS when setting up for I/O APIC interrupt delivery mode.
6:4	Reserved
3:0	**IRQ Routing** – R/W. (ISA compatible.) 0000 = Reserved 1000 = Reserved 0001 = Reserved 1001 = IRQ9 0010 = Reserved 1010 = IRQ10 0011 = IRQ3 1011 = IRQ11 0100 = IRQ4 1100 = IRQ12 0101 = IRQ5 1101 = Reserved 0110 = IRQ6 1110 = IRQ14 0111 = IRQ7 1111 = IRQ15

21.1.17 SIRQ_CNTL – Serial IRQ Control Register (LPC I/F – D31:F0)

Offset Address:	64h	Attribute:	R/W, RO
Default Value:	10h	Size:	8 bit
Lockable:	No	Power Well:	Core

Bit	Description
7	**Serial IRQ Enable (SIRQEN) –** R/W. 0 = The buffer is input only and internally SERIRQ will be a 1. 1 = Serial IRQs will be recognized. The SERIRQ pin will be configured as SERIRQ.
6	**Serial IRQ Mode Select (SIRQMD) –** R/W. 0 = The serial IRQ machine will be in quiet mode. 1 = The serial IRQ machine will be in continuous mode. ***Note:*** For systems using Quiet Mode, this bit should be set to 1 (Continuous Mode) for at least one frame after coming out of reset before switching back to Quiet Mode. Failure to do so will result in the Intel® 631xESB/632xESB I/O Controller Hub not recognizing SERIRQ interrupts.
5:2	**Serial IRQ Frame Size (SIRQSZ) –** RO. Fixed field that indicates the size of the SERIRQ frame as 21 frames.
1:0	**Start Frame Pulse Width (SFPW) –** R/W. This is the number of PCI clocks that the SERIRQ pin will be driven low by the serial IRQ machine to signal a start frame. In continuous mode, the Intel® 631xESB/632xESB I/O Controller Hub will drive the start frame for the number of clocks specified. In quiet mode, the Intel® 631xESB/632xESB I/O Controller Hub will drive the start frame for the number of clocks specified minus one, as the first clock was driven by the peripheral. 00 = 4 clocks 01 = 6 clocks 10 = 8 clocks 11 = Reserved

21.1.18 PIRQ[n]_ROUT – PIRQ[E,F,G,H] Routing Control Register (LPC I/F – D31:F0)

Offset Address:	PIRQE – 68h, PIRQF – 69h, PIRQG – 6Ah, PIRQH – 6Bh	Attribute:	R/W
Default Value:	80h	Size:	8 bit
Lockable:	No	Power Well:	Core

Bit	Description
7	**Interrupt Routing Enable (IRQEN) –** R/W. 0 = The corresponding PIRQ is routed to one of the ISA-compatible interrupts specified in bits[3:0]. 1 = The PIRQ is not routed to the 8259. ***Note:*** BIOS must program this bit to 0 during POST for any of the PIRQs that are being used. The value of this bit may subsequently be changed by the OS when setting up for I/O APIC interrupt delivery mode.
6:4	Reserved
3:0	**IRQ Routing** – R/W. (ISA compatible.) 0000 = Reserved 1000 = Reserved 0001 = Reserved 1001 = IRQ9 0010 = Reserved 1010 = IRQ10 0011 = IRQ3 1011 = IRQ11 0100 = IRQ4 1100 = IRQ12 0101 = IRQ5 1101 = Reserved 0110 = IRQ6 1110 = IRQ14 0111 = IRQ7 1111 = IRQ15

21.1.19 LPC_I/O_DEC – I/O Decode Ranges Register (LPC I/F – D31:F0)

Offset Address: 80h
Default Value: 0000h
Attribute: R/W
Size: 16 bit

Bit	Description
15:13	Reserved
12	FDD Decode Range – R/W. Determines which range to decode for the FDD Port 0 = 3F0h – 3F5h, 3F7h (Primary) 1 = 370h – 375h, 377h (Secondary)
11:10	Reserved
9:8	**LPT Decode Range** – R/W. This field determines which range to decode for the LPT Port. 00 = 378h – 37Fh and 778h – 77Fh 01 = 278h – 27Fh (port 279h is read only) and 678h – 67Fh 10 = 3BCh –3BEh and 7BCh – 7BEh 11 = Reserved
7	Reserved
6:4	**COMB Decode Range** – R/W. This field determines which range to decode for the COMB Port. 000 = 3F8h – 3FFh (COM1) 001 = 2F8h – 2FFh (COM2) 010 = 220h – 227h 011 = 228h – 22Fh 100 = 238h – 23Fh 101 = 2E8h – 2EFh (COM4) 110 = 338h – 33Fh 111 = 3E8h – 3EFh (COM3)
3	Reserved
2:0	**COMA Decode Range** – R/W. This field determines which range to decode for the COMA Port. 000 = 3F8h – 3FFh (COM1) 001 = 2F8h – 2FFh (COM2) 010 = 220h – 227h 011 = 228h – 22Fh 100 = 238h – 23Fh 101 = 2E8h – 2EFh (COM4) 110 = 338h – 33Fh 111 = 3E8h – 3EFh (COM3)

21.1.20 LPC_EN – LPC I/F Enables Register (LPC I/F – D31:F0)

Offset Address: 82h – 83h
Default Value: 0000h
Attribute: R/W
Size: 16 bit
Power Well: Core

Bit	Description
15:14	Reserved
13	**CNF2_LPC_EN** – R/W. Microcontroller Enable # 2. 0 = Disable. 1 = Enables the decoding of the I/O locations 4Eh and 4Fh to the LPC interface. This range is used for a microcontroller.
12	**CNF1_LPC_EN** – R/W. Super I/O Enable. 0 = Disable. 1 = Enables the decoding of the I/O locations 2Eh and 2Fh to the LPC interface. This range is used for Super I/O devices.

Bit	Description
11	**MC_LPC_EN** – R/W. Microcontroller Enable # 1. 0 = Disable. 1 = Enables the decoding of the I/O locations 62h and 66h to the LPC interface. This range is used for a microcontroller.
10	**KBC_LPC_EN** – R/W. Keyboard Enable. 0 = Disable. 1 = Enables the decoding of the I/O locations 60h and 64h to the LPC interface. This range is used for a microcontroller.
9	**GAMEH_LPC_EN** – R/W. High Gameport Enable 0 = Disable. 1 = Enables the decoding of the I/O locations 208h to 20Fh to the LPC interface. This range is used for a gameport.
8	**GAMEL_LPC_EN** – R/W. Low Gameport Enable 0 = Disable. 1 = Enables the decoding of the I/O locations 200h to 207h to the LPC interface. This range is used for a gameport.
7:4	Reserved
3	**FDD_LPC_EN** – R/W. Floppy Drive Enable 0 = Disable. 1 = Enables the decoding of the FDD range to the LPC interface. This range is selected in the LPC_FDD/LPT Decode Range Register (D31:F0:80h, bit 12).
2	**LPT_LPC_EN** – R/W. Parallel Port Enable 0 = Disable. 1 = Enables the decoding of the LPTrange to the LPC interface. This range is selected in the LPC_FDD/LPT Decode Range Register (D31:F0:80h, bit 9:8).
1	**COMB_LPC_EN** – R/W. Com Port B Enable 0 = Disable. 1 = Enables the decoding of the COMB range to the LPC interface. This range is selected in the LPC_COM Decode Range Register (D31:F0:80h, bits 6:4).
0	**COMA_LPC_EN** – R/W. Com Port A Enable 0 = Disable. 1 = Enables the decoding of the COMA range to the LPC interface. This range is selected in the LPC_COM Decode Range Register (D31:F0:80h, bits 3:2).

21.1.21 GEN1_DEC – LPC I/F Generic Decode Range 1 Register (LPC I/F – D31:F0)

Offset Address: 84h – 85h
Default Value: 0000h
Attribute: R/W
Size: 16 bit
Power Well: Core

Bit	Description
15:7	**Generic I/O Decode Range 1 Base Address (GEN1_BASE) –** R/W. This address is aligned on a 128-byte boundary, and must have address lines 31:16 as 0. ***Note:*** This generic decode is for I/O addresses only, not memory addresses. The size of this range is 128 bytes.
6:1	Reserved
0	**Generic Decode Range 1 Enable (GEN1_EN) –** R/W. 0 = Disable. 1 = Enable the GEN1 I/O range to be forwarded to the LPC I/F

21.1.22 GEN2_DEC – LPC I/F Generic Decode Range 2 Register (LPC I/F – D31:F0)

Offset Address: 88h – 89h
Default Value: 0000h
Attribute: R/W
Size: 16 bit
Power Well: Core

Bit	Description
15:4	**Generic I/O Decode Range 2 Base Address (GEN2_BASE) –** R/W. This address is aligned on a 16-byte boundary, and must have address lines 31:16 as 0. ***Note:*** This generic decode is for I/O addresses only, not memory addresses. The size of this range is 16 bytes.
3:1	Reserved. Read as 0.
0	**Generic I/O Decode Range 2 Enable (GEN2_EN) –** R/W. 0 = Disable. 1 = Accesses to the GEN2 I/O range will be forwarded to the LPC I/F

21.1.23 FWH_SEL1 – Firmware Hub Select 1 Register (LPC I/F – D31:F0)

Offset Address: D0h–D3h
Default Value: 00112233h
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31:28	**FWH_F8_IDSEL** – RO. IDSEL for two 512-KB Firmware Hub memory ranges and one 128-KB memory range. This field is fixed at 0000. The IDSEL programmed in this field addresses the following memory ranges: FFF8 0000h – FFFF FFFFh FFB8 0000h – FFBF FFFFh 000E 0000h – 000F FFFFh
27:24	**FWH_F0_IDSEL** – R/W. IDSEL for two 512-KB Firmware Hub memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFF0 0000h – FFF7 FFFFh FFB0 0000h – FFB7 FFFFh
23:20	**FWH_E8_IDSEL** – R/W. IDSEL for two 512-KB Firmware Hub memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFE8 0000h – FFEF FFFFh FFA8 0000h – FFAF FFFFh
19:16	**FWH_E0_IDSEL** – R/W. IDSEL for two 512-KB Firmware Hub memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFE0 0000h – FFE7 FFFFh FFA0 0000h – FFA7 FFFFh
15:12	**FWH_D8_IDSEL** – R/W. IDSEL for two 512-KB Firmware Hub memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFD8 0000h – FFDF FFFFh FF98 0000h – FF9F FFFFh
11:8	**FWH_D0_IDSEL** – R/W. IDSEL for two 512-KB Firmware Hub memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFD0 0000h – FFD7 FFFFh FF90 0000h – FF97 FFFFh
7:4	**FWH_C8_IDSEL** – R/W. IDSEL for two 512-KB Firmware Hub memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFC8 0000h – FFCF FFFFh FF88 0000h – FF8F FFFFh
3:0	**FWH_C0_IDSEL** – R/W. IDSEL for two 512-KB Firmware Hub memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFC0 0000h – FFC7 FFFFh FF80 0000h – FF87 FFFFh

21.1.24 FWH_SEL2 – Firmware Hub Select 2 Register (LPC I/F – D31:F0)

Offset Address: D4h–D5h
Default Value: 4567h
Attribute: R/W
Size: 16 bits

Bit	Description
15:12	**FWH_70_IDSEL** – R/W. IDSEL for two, 1-M Firmware Hub memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FF70 0000h – FF7F FFFFh FF30 0000h – FF3F FFFFh
11:8	**FWH_60_IDSEL** – R/W. IDSEL for two, 1-M Firmware Hub memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FF60 0000h – FF6F FFFFh FF20 0000h – FF2F FFFFh
7:4	**FWH_50_IDSEL** – R/W. IDSEL for two, 1-M Firmware Hub memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FF50 0000h – FF5F FFFFh FF10 0000h – FF1F FFFFh
3:0	**FWH_40_IDSEL** – R/W. IDSEL for two, 1-M Firmware Hub memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FF40 0000h – FF4F FFFFh FF00 0000h – FF0F FFFFh

21.1.25 FWH_DEC_EN1 – Firmware Hub Decode Enable Register (LPC I/F – D31:F0)

Offset Address: D8h–D9h
Default Value: FFCFh
Attribute: R/W, RO
Size: 16 bits

Bit	Description
15	**FWH_F8_EN** – RO. This bit enables decoding two 512-KB Firmware Hub memory ranges, and one 128-KB memory range. 0 = Disable 1 = Enable the following ranges for the Firmware Hub FFF80000h – FFFFFFFFh FFB80000h – FFBFFFFFh 000E0000h – 000FFFFFh
14	**FWH_F0_EN** – R/W. This bit enables decoding two 512-KB Firmware Hub memory ranges. 0 = Disable. 1 = Enable the following ranges for the Firmware Hub: FFF00000h – FFF7FFFFh FFB00000h – FFB7FFFFh
13	**FWH_E8_EN** – R/W. This bit enables decoding two 512-KB Firmware Hub memory ranges. 0 = Disable. 1 = Enable the following ranges for the Firmware Hub: FFE80000h – FFEFFFFh FFA80000h – FFAFFFFFh
12	**FWH_E0_EN** – R/W. This bit enables decoding two 512-KB Firmware Hub memory ranges. 0 = Disable. 1 = Enable the following ranges for the Firmware Hub: FFE00000h – FFE7FFFFh FFA00000h – FFA7FFFFh
11	**FWH_D8_EN** – R/W. This bit enables decoding two 512-KB Firmware Hub memory ranges. 0 = Disable. 1 = Enable the following ranges for the Firmware Hub FFD80000h – FFDFFFFFh FF980000h – FF9FFFFFh

Bit	Description
10	**FWH_D0_EN** – R/W. This bit enables decoding two 512-KB Firmware Hub memory ranges. 0 = Disable. 1 = Enable the following ranges for the Firmware Hub FFD00000h – FFD7FFFFh FF900000h – FF97FFFFh
9	**FWH_C8_EN** – R/W. This bit enables decoding two 512-KB Firmware Hub memory ranges. 0 = Disable. 1 = Enable the following ranges for the Firmware Hub FFC80000h – FFCFFFFFh FF880000h – FF8FFFFFh
8	**FWH_C0_EN** – R/W. This bit enables decoding two 512-KB Firmware Hub memory ranges. 0 = Disable. 1 = Enable the following ranges for the Firmware Hub FFC00000h – FFC7FFFFh FF800000h – FF87FFFFh
7	**FWH_Legacy_F_EN** – R/W. This enables the decoding of the legacy 128-K range at F0000h – FFFFFh. 0 = Disable. 1 = Enable the following legacy ranges for the Firmware Hub F0000h – FFFFFh
6	**FWH_Legacy_E_EN** – R/W. This enables the decoding of the legacy 128-K range at E0000h – EFFFFh. 0 = Disable. 1 = Enable the following legacy ranges for the Firmware Hub E0000h – EFFFFh
5:4	Reserved
3	**FWH_70_EN** – R/W. Enables decoding two 1-M Firmware Hub memory ranges. 0 = Disable. 1 = Enable the following ranges for the Firmware Hub FF70 0000h – FF7F FFFFh FF30 0000h – FF3F FFFFh
2	**FWH_60_EN** – R/W. Enables decoding two 1-M Firmware Hub memory ranges. 0 = Disable. 1 = Enable the following ranges for the Firmware Hub FF60 0000h – FF6F FFFFh FF20 0000h – FF2F FFFFh
1	**FWH_50_EN –** R/W. Enables decoding two 1-M Firmware Hub memory ranges. 0 = Disable. 1 = Enable the following ranges for the Firmware Hub FF50 0000h – FF5F FFFFh FF10 0000h – FF1F FFFFh
0	**FWH_40_EN** – R/W. Enables decoding two 1-M Firmware Hub memory ranges. 0 = Disable. 1 = Enable the following ranges for the Firmware Hub FF40 0000h – FF4F FFFFh FF00 0000h – FF0F FFFFh

21.1.26 BIOS_CNTL – BIOS Control Register (LPC I/F – D31:F0)

Offset Address:	DCh	Attribute:	R/WLO, R/W
Default Value:	00h	Size:	8 bit
Lockable:	No	Power Well:	Core

Bit	Description
7:2	Reserved
1	**BIOS Lock Enable (BLE) –** R/WLO. 0 = Setting the BIOSWE will not cause SMIs. 1 = Enables setting the BIOSWE bit to cause SMIs. Once set, this bit can only be cleared by a PLTRST#
0	**BIOS Write Enable (BIOSWE) –** R/W. 0 = Only read cycles result in Firmware Hub I/F cycles. 1 = Access to the BIOS space is enabled for both read and write cycles. When this bit is written from a 0 to a 1 and BIOS Lock Enable (BLE) is also set, an SMI# is generated. This ensures that only SMI code can update BIOS.

21.1.27 RCBA – Root Complex Base Address Register (LPC I/F – D31:F0)

Offset Address:	F0h	Attribute:	R/W
Default Value:	00h	Size:	8 bit

Bit	Description
31:14	**Base Address (BA) –** R/W. Base Address for the root complex register block decode range. This address is aligned on a 16-KB boundary.
13:1	Reserved
0	**Enable (EN) –** R/W. When set, enables the range specified in BA to be claimed as the Root Complex Register Block.

21.2 DMA I/O Registers (LPC I/F – D31:F0)

Table 21-2. DMA Registers (Sheet 1 of 2)

Port	Alias	Register Name	Default	Type
00h	10h	Channel 0 DMA Base & Current Address	Undefined	R/W
01h	11h	Channel 0 DMA Base & Current Count	Undefined	R/W
02h	12h	Channel 1 DMA Base & Current Address	Undefined	R/W
03h	13h	Channel 1 DMA Base & Current Count	Undefined	R/W
04h	14h	Channel 2 DMA Base & Current Address	Undefined	R/W
05h	15h	Channel 2 DMA Base & Current Count	Undefined	R/W
06h	16h	Channel 3 DMA Base & Current Address	Undefined	R/W
07h	17h	Channel 3 DMA Base & Current Count	Undefined	R/W
08h	18h	Channel 0–3 DMA Command	Undefined	WO
		Channel 0–3 DMA Status	Undefined	RO
0Ah	1Ah	Channel 0–3 DMA Write Single Mask	000001XXb	WO
0Bh	1Bh	Channel 0–3 DMA Channel Mode	000000XXb	WO

Table 21-2. DMA Registers (Sheet 2 of 2)

Port	Alias	Register Name	Default	Type
0Ch	1Ch	Channel 0–3 DMA Clear Byte Pointer	Undefined	WO
0Dh	1Dh	Channel 0–3 DMA Master Clear	Undefined	WO
0Eh	1Eh	Channel 0–3 DMA Clear Mask	Undefined	WO
0Fh	1Fh	Channel 0–3 DMA Write All Mask	0Fh	R/W
80h	90h	Reserved Page	Undefined	R/W
81h	91h	Channel 2 DMA Memory Low Page	Undefined	R/W
82h	–	Channel 3 DMA Memory Low Page	Undefined	R/W
83h	93h	Channel 1 DMA Memory Low Page	Undefined	R/W
84h–86h	94h–96h	Reserved Pages	Undefined	R/W
87h	97h	Channel 0 DMA Memory Low Page	Undefined	R/W
88h	98h	Reserved Page	Undefined	R/W
89h	99h	Channel 6 DMA Memory Low Page	Undefined	R/W
8Ah	9Ah	Channel 7 DMA Memory Low Page	Undefined	R/W
8Bh	9Bh	Channel 5 DMA Memory Low Page	Undefined	R/W
8Ch–8Eh	9Ch–9Eh	Reserved Page	Undefined	R/W
8Fh	9Fh	Refresh Low Page	Undefined	R/W
C0h	C1h	Channel 4 DMA Base & Current Address	Undefined	R/W
C2h	C3h	Channel 4 DMA Base & Current Count	Undefined	R/W
C4h	C5h	Channel 5 DMA Base & Current Address	Undefined	R/W
C6h	C7h	Channel 5 DMA Base & Current Count	Undefined	R/W
C8h	C9h	Channel 6 DMA Base & Current Address	Undefined	R/W
CAh	CBh	Channel 6 DMA Base & Current Count	Undefined	R/W
CCh	CDh	Channel 7 DMA Base & Current Address	Undefined	R/W
CEh	CFh	Channel 7 DMA Base & Current Count	Undefined	R/W
D0h	D1h	Channel 4–7 DMA Command	Undefined	WO
		Channel 4–7 DMA Status	Undefined	RO
D4h	D5h	Channel 4–7 DMA Write Single Mask	000001XXb	WO
D6h	D7h	Channel 4–7 DMA Channel Mode	000000XXb	WO
D8h	D9h	Channel 4–7 DMA Clear Byte Pointer	Undefined	WO
DAh	DBh	Channel 4–7 DMA Master Clear	Undefined	WO
DCh	DDh	Channel 4–7 DMA Clear Mask	Undefined	WO
DEh	DFh	Channel 4–7 DMA Write All Mask	0Fh	R/W

21.2.1 DMABASE_CA – DMA Base and Current Address Registers (LPC I/F – D31:F0)

I/O Address: Ch. #0 = 00h; Ch. #1 = 02h; Ch. #2 = 04h; Ch. #3 = 06h; Ch. #5 = C4h Ch. #6 = C8h; Ch. #7 = CCh; Attribute:R/W; Size:16 bit (per channel), but accessed in two 8-bit quantities
Default Value: Undef
Lockable: No
Power Well:Core

Bit	Description
15:0	**Base and Current Address** – R/W. This register determines the address for the transfers to be performed. The address specified points to two separate registers. On writes, the value is stored in the *Base Address* register and copied to the *Current Address* register. On reads, the value is returned from the *Current Address* register. The address increments/decrements in the Current Address register after each transfer, depending on the mode of the transfer. If the channel is in auto-initialize mode, the Current Address register will be reloaded from the Base Address register after a terminal count is generated. For transfers to/from a 16-bit slave (channel's 5-7), the address is shifted left one bit location. Bit 15 will be shifted into Bit 16. The register is accessed in 8 bit quantities. The byte is pointed to by the current byte pointer flip/flop. Before accessing an address register, the byte pointer flip/flop should be cleared to ensure that the low byte is accessed first

21.2.2 DMABASE_CC – DMA Base and Current Count Registers (LPC I/F – D31:F0)

I/O Address: Ch. #0 = 01h; Ch. #1 = 03h; Ch. #2 = 05h; Ch. #3 = 07h; Ch. #5 = C6h; Ch. #6 = CAh; Ch. #7 = CEh; Attribute:R/W; Size:16-bit (per channel), but accessed in two 8-bit quantities
Default Value: Undefined
Lockable: No
Power Well:Core

Bit	Description
15:0	**Base and Current Count** – R/W. This register determines the number of transfers to be performed. The address specified points to two separate registers. On writes, the value is stored in the *Base Count* register and copied to the *Current Count* register. On reads, the value is returned from the *Current Count* register. The actual number of transfers is one more than the number programmed in the Base Count Register (that is, programming a count of 4h results in 5 transfers). The count is decrements in the Current Count register after each transfer. When the value in the register rolls from zero to FFFFh, a terminal count is generated. If the channel is in auto-initialize mode, the Current Count register will be reloaded from the Base Count register after a terminal count is generated. For transfers to/from an 8-bit slave (channels 0–3), the count register indicates the number of bytes to be transferred. For transfers to/from a 16-bit slave (channels 5–7), the count register indicates the number of words to be transferred. The register is accessed in 8 bit quantities. The byte is pointed to by the current byte pointer flip/flop. Before accessing a count register, the byte pointer flip/flop should be cleared to ensure that the low byte is accessed first.

21.2.3 DMAMEM_LP – DMA Memory Low Page Registers (LPC I/F – D31:F0)

I/O Address: Ch. #0 = 87h; Ch. #1 = 83h
Ch. #2 = 81h; Ch. #3 = 82h
Ch. #5 = 8Bh; Ch. #6 = 89h
Ch. #7 = 8Ah; Attribute:R/W
Default Value: Undefined Size:8-bit
Lockable: No Power Well:Core

Bit	Description
7:0	**DMA Low Page** (ISA Address bits [23:16]) – R/W. This register works in conjunction with the DMA controller's Current Address Register to define the complete 24-bit address for the DMA channel. This register remains static throughout the DMA transfer. Bit 16 of this register is ignored when in 16 bit I/O count by words mode as it is replaced by the bit 15 shifted out from the current address register.

21.2.4 DMACMD – DMA Command Register (LPC I/F – D31:F0)

I/O Address: Ch. #0–3 = 08h;
Ch. #4–7 = D0h Attribute: WO
Default Value: Undefined Size: 8-bit
Lockable: No Power Well: Core

Bit	Description
7:5	Reserved. Must be 0.
4	**DMA Group Arbitration Priority** – WO. Each channel group is individually assigned either fixed or rotating arbitration priority. At part reset, each group is initialized in fixed priority. 0 = Fixed priority to the channel group 1 = Rotating priority to the group.
3	Reserved. Must be 0.
2	**DMA Channel Group Enable** – WO. Both channel groups are enabled following part reset. 0 = Enable the DMA channel group. 1 = Disable. Disabling channel group 4–7 also disables channel group 0–3, which is cascaded through channel 4.
1:0	Reserved. Must be 0.

21.2.5 DMASTA – DMA Status Register (LPC I/F – D31:F0)

I/O Address:	Ch. #0–3 = 08h; Ch. #4–7 = D0h	Attribute:	RO
Default Value:	Undefined	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7:4	**Channel Request Status** – RO. When a valid DMA request is pending for a channel, the corresponding bit is set to 1. When a DMA request is not pending for a particular channel, the corresponding bit is set to 0. The source of the DREQ may be hardware or a software request. Note that channel 4 is the cascade channel, so the request status of channel 4 is a logical OR of the request status for channels 0 through 3. 4 = Channel 0 5 = Channel 1 (5) 6 = Channel 2 (6) 7 = Channel 3 (7)
3:0	**Channel Terminal Count Status** – RO. When a channel reaches terminal count (TC), its status bit is set to 1. If TC has not been reached, the status bit is set to 0. Channel 4 is programmed for cascade, so the TC bit response for channel 4 is irrelevant: 0 = Channel 0 1 = Channel 1 (5) 2 = Channel 2 (6) 3 = Channel 3 (7)

21.2.6 DMA_WRSMSK – DMA Write Single Mask Register (LPC I/F – D31:F0)

I/O Address:	Ch. #0–3 = 0Ah; Ch. #4–7 = D4h	Attribute:	WO
Default Value:	0000 01xx	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7:3	Reserved. Must be 0.
2	Channel Mask Select – WO. 0 = Enable DREQ for the selected channel. The channel is selected through bits [1:0]. Therefore, only one channel can be masked / unmasked at a time. 1 = Disable DREQ for the selected channel.
1:0	**DMA Channel Select** – WO. These bits select the DMA Channel Mode Register to program. 00 = Channel 0 (4) 01 = Channel 1 (5) 10 = Channel 2 (6) 11 = Channel 3 (7)

21.2.7 DMACH_MODE – DMA Channel Mode Register (LPC I/F – D31:F0)

I/O Address:	Ch. #0–3 = 0Bh; Ch. #4–7 = D6h	Attribute:	WO
Default Value:	0000 00xx	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7:6	**DMA Transfer Mode** – WO. Each DMA channel can be programmed in one of four different modes: 00 = Demand mode 01 = Single mode 10 = Reserved 11 = Cascade mode
5	**Address Increment/Decrement Select** – WO. This bit controls address increment/decrement during DMA transfers. 0 = Address increment. (default after part reset or Master Clear) 1 = Address decrement.
4	**Autoinitialize Enable** – WO. 0 = Autoinitialize feature is disabled and DMA transfers terminate on a terminal count. A part reset or Master Clear disables autoinitialization. 1 = DMA restores the Base Address and Count registers to the current registers following a terminal count (TC).
3:2	**DMA Transfer Type** – WO. These bits represent the direction of the DMA transfer. When the channel is programmed for cascade mode, (bits[7:6] = 11) the transfer type is irrelevant. 00 = Verify – No I/O or memory strobes generated 01 = Write – Data transferred from the I/O devices to memory 10 = Read – Data transferred from memory to the I/O device 11 = Illegal
1:0	**DMA Channel Select** – WO. These bits select the DMA Channel Mode Register that will be written by bits [7:2]. 00 = Channel 0 (4) 01 = Channel 1 (5) 10 = Channel 2 (6) 11 = Channel 3 (7)

21.2.8 DMA Clear Byte Pointer Register (LPC I/F – D31:F0)

I/O Address:	Ch. #0–3 = 0Ch; Ch. #4–7 = D8h	Attribute:	WO
Default Value:	xxxx xxxx	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7:0	**Clear Byte Pointer** – WO. No specific pattern. Command enabled with a write to the I/O port address. Writing to this register initializes the byte pointer flip/flop to a known state. It clears the internal latch used to address the upper or lower byte of the 16-bit Address and Word Count Registers. The latch is also cleared by part reset and by the Master Clear command. This command precedes the first access to a 16-bit DMA controller register. The first access to a 16-bit register will then access the significant byte, and the second access automatically accesses the most significant byte.

21.2.9 DMA Master Clear Register (LPC I/F – D31:F0)

I/O Address: Ch. #0–3 = 0Dh; Ch. #4–7 = DAh — Attribute: WO
Default Value: xxxx xxxx — Size: 8-bit

Bit	Description
7:0	**Master Clear** – WO. No specific pattern. Enabled with a write to the port. This has the same effect as the hardware Reset. The Command, Status, Request, and Byte Pointer flip/flop registers are cleared and the Mask Register is set.

21.2.10 DMA_CLMSK – DMA Clear Mask Register (LPC I/F – D31:F0)

I/O Address: Ch. #0–3 = 0Eh; Ch. #4–7 = DCh — Attribute: WO
Default Value: xxxx xxxx — Size: 8-bit
Lockable: No — Power Well: Core

Bit	Description
7:0	**Clear Mask Register** – WO. No specific pattern. Command enabled with a write to the port.

21.2.11 DMA_WRMSK – DMA Write All Mask Register (LPC I/F – D31:F0)

I/O Address: Ch. #0–3 = 0Fh; Ch. #4–7 = DEh — Attribute: R/W
Default Value: 0000 1111 — Size: 8-bit
Lockable: No — Power Well: Core

Bit	Description
7:4	Reserved. Must be 0.
3:0	**Channel Mask Bits** – R/W. This register permits all four channels to be simultaneously enabled/disabled instead of enabling/disabling each channel individually, as is the case with the Mask Register – Write Single Mask Bit. In addition, this register has a read path to allow the status of the channel mask bits to be read. A channel's mask bit is automatically set to 1 when the Current Byte/Word Count Register reaches terminal count (unless the channel is in auto-initialization mode). Setting the bit(s) to a 1 disables the corresponding DREQ(s). Setting the bit(s) to a 0 enables the corresponding DREQ(s). Bits [3:0] are set to 1 upon part reset or Master Clear. When read, bits [3:0] indicate the DMA channel [3:0] ([7:4]) mask status. Bit 0 = Channel 0 (4)1 = Masked, 0 = Not Masked Bit 1 = Channel 1 (5)1 = Masked, 0 = Not Masked Bit 2 = Channel 2 (6)1 = Masked, 0 = Not Masked Bit 3 = Channel 3 (7)1 = Masked, 0 = Not Masked ***Note:*** Disabling channel 4 also disables channels 0–3 due to the cascade of channel's 0 – 3 through channel 4.

21.3 Timer I/O Registers (LPC I/F – D31:F0)

Port	Aliases	Register Name	Default Value	Type
40h	50h	Counter 0 Interval Time Status Byte Format	0XXXXXXXb	RO
		Counter 0 Counter Access Port	Undefined	R/W
41h	51h	Counter 1 Interval Time Status Byte Format	0XXXXXXXb	RO
		Counter 1 Counter Access Port	Undefined	R/W

Port	Aliases	Register Name	Default Value	Type
42h	52h	Counter 2 Interval Time Status Byte Format	0XXXXXXXb	RO
		Counter 2 Counter Access Port	Undefined	R/W
43h	53h	Timer Control Word	Undefined	WO
		Timer Control Word Register	XXXXXXX0b	WO
		Counter Latch Command	X0h	WO

21.3.1 TCW – Timer Control Word Register (LPC I/F – D31:F0)

I/O Address: 43h Attribute: WO
Default Value: All bits undefined Size: 8 bits

This register is programmed prior to any counter being accessed to specify counter modes. Following part reset, the control words for each register are undefined and each counter output is 0. Each timer must be programmed to bring it into a known state.

Bit	Description
7:6	**Counter Select** – WO. The Counter Selection bits select the counter the control word acts upon as shown below. The Read Back Command is selected when bits[7:6] are both 1. 00 = Counter 0 select 01 = Counter 1 select 10 = Counter 2 select 11 = Read Back Command
5:4	**Read/Write Select** – WO. These bits are the read/write control bits. The actual counter programming is done through the counter port (40h for counter 0, 41h for counter 1, and 42h for counter 2). 00 = Counter Latch Command 01 = Read/Write Least Significant Byte (LSB) 10 = Read/Write Most Significant Byte (MSB) 11 = Read/Write LSB then MSB
3:1	**Counter Mode Selection** – WO. These bits select one of six possible modes of operation for the selected counter. 000 = Mode 0Out signal on end of count (=0) 001 = Mode 1Hardware retriggerable one-shot x10 = Mode 2Rate generator (divide by n counter) x11 = Mode 3Square wave output 100 = Mode 4Software triggered strobe 101 = Mode 5Hardware triggered strobe
0	Binary/BCD Countdown Select – WO. 0 = Binary countdown is used. The largest possible binary count is 2^{16} 1 = Binary coded decimal (BCD) count is used. The largest possible BCD count is 10^4

There are two special commands that can be issued to the counters through this register, the Read Back Command and the Counter Latch Command. When these commands are chosen, several bits within this register are redefined. These register formats are described below:

RDBK_CMD – Read Back Command (LPC I/F – D31:F0)

The Read Back Command is used to determine the count value, programmed mode, and current states of the OUT pin and Null count flag of the selected counter or counters. Status and/or count may be latched in any or all of the counters by selecting the counter during the register write. The count and status remain latched until read, and further latch commands are ignored until the count is read. Both count and status of the selected counters may be latched simultaneously by setting both bit 5 and bit 4 to 0. If both are latched, the first read operation from that counter returns the latched

status. The next one or two reads, depending on whether the counter is programmed for one or two byte counts, returns the latched count. Subsequent reads return an unlatched count.

Bit	Description
7:6	**Read Back Command.** Must be 11 to select the Read Back Command
5	Latch Count of Selected Counters. 0 = Current count value of the selected counters will be latched 1 = Current count will not be latched
4	Latch Status of Selected Counters. 0 = Status of the selected counters will be latched 1 = Status will not be latched
3	Counter 2 Select. 1 = Counter 2 count and/or status will be latched
2	Counter 1 Select. 1 = Counter 1 count and/or status will be latched
1	Counter 0 Select. 1 = Counter 0 count and/or status will be latched.
0	Reserved. Must be 0.

LTCH_CMD – Counter Latch Command (LPC I/F – D31:F0)

The Counter Latch Command latches the current count value. This command is used to insure that the count read from the counter is accurate. The count value is then read from each counter's count register through the Counter Ports Access Ports Register (40h for counter 0, 41h for counter 1, and 42h for counter 2). The count must be read according to the programmed format, that is, if the counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other (read, write, or programming operations for other counters may be inserted between the reads). If a counter is latched once and then latched again before the count is read, the second Counter Latch Command is ignored.

Bit	Description
7:6	**Counter Selection.** These bits select the counter for latching. If “11” is written, then the write is interpreted as a read back command. 00 = Counter 0 01 = Counter 1 10 = Counter 2
5:4	**Counter Latch Command.** 00 = Selects the Counter Latch Command.
3:0	Reserved. Must be 0.

21.3.2 SBYTE_FMT – Interval Timer Status Byte Format Register (LPC I/F – D31:F0)

I/O Address:	Counter 0 = 40h, Counter 1 = 41h, Counter 2 = 42h	Attribute: Size:	RO 8 bits per counter
Default Value:	Bits[6:0] undefined, Bit 7=0		

Each counter's status byte can be read following a Read Back Command. If latch status is chosen (bit 4=0, Read Back Command) as a read back option for a given counter, the next read from the counter's Counter Access Ports Register (40h for counter 0, 41h for counter 1, and 42h for counter 2) returns the status byte. The status byte returns the following:

Bit	Description
7	**Counter OUT Pin State** – RO. 0 = OUT pin of the counter is also a 0 1 = OUT pin of the counter is also a 1
6	**Count Register Status** – RO. This bit indicates when the last count written to the Count Register (CR) has been loaded into the counting element (CE). The exact time this happens depends on the counter mode, but until the count is loaded into the counting element (CE), the count value will be incorrect. 0 = Count has been transferred from CR to CE and is available for reading. 1 = Null Count. Count has not been transferred from CR to CE and is not yet available for reading.
5:4	**Read / Write Selection Status** – RO. These reflect the read/write selection made through bits[5:4] of the control register. The binary codes returned during the status read match the codes used to program the counter read/write selection. 00 = Counter Latch Command 01 = Read/Write Least Significant Byte (LSB) 10 = Read/Write Most Significant Byte (MSB) 11 = Read/Write LSB then MSB
3:1	**Mode Selection Status** – RO. These bits return the counter mode programming. The binary code returned matches the code used to program the counter mode, as listed under the bit function above. 000 = Mode 0Out signal on end of count (=0) 001 = Mode 1Hardware retriggerable one-shot x10 = Mode 2Rate generator (divide by n counter) x11 = Mode 3Square wave output 100 = Mode 4Software triggered strobe 101 = Mode 5Hardware triggered strobe
0	**Countdown Type Status** – RO. This bit reflects the current countdown type. 0 = Binary countdown 1 = Binary Coded Decimal (BCD) countdown.

21.3.3 Counter Access Ports Register (LPC I/F – D31:F0)

I/O Address:	Counter 0 – 40h, Counter 1 – 41h, Counter 2 – 42h	Attribute:	R/W
Default Value:	All bits undefined	Size:	8 bit

Bit	Description
7:0	**Counter Port** – R/W. Each counter port address is used to program the 16-bit Count Register. The order of programming, either LSB only, MSB only, or LSB then MSB, is defined with the Interval Counter Control Register at port 43h. The counter port is also used to read the current count from the Count Register, and return the status of the counter programming following a Read Back Command.

21.4 8259 Interrupt Controller (PIC) Registers (LPC I/F – D31:F0)

21.4.1 Interrupt Controller I/O MAP (LPC I/F – D31:F0)

The interrupt controller registers are located at 20h and 21h for the master controller (IRQ 0–7), and at A0h and A1h for the slave controller (IRQ 8–13). These registers have multiple functions, depending upon the data written to them. Table 21-3 shows the different register possibilities for each address.

Table 21-3. PIC Registers (LPC I/F – D31:F0)

Port	Aliases	Register Name	Default Value	Type
20h	24h, 28h, 2Ch, 30h, 34h, 38h, 3Ch	Master PIC ICW1 Init. Cmd Word 1	Undefined	WO
		Master PIC OCW2 Op Ctrl Word 2	001XXXXXb	WO
		Master PIC OCW3 Op Ctrl Word 3	X01XXX10b	WO
21h	25h, 29h, 2Dh, 31h, 35h, 39h, 3Dh	Master PIC ICW2 Init. Cmd Word 2	Undefined	WO
		Master PIC ICW3 Init. Cmd Word 3	Undefined	WO
		Master PIC ICW4 Init. Cmd Word 4	01h	WO
		Master PIC OCW1 Op Ctrl Word 1	00h	R/W
A0h	A4h, A8h, ACh, B0h, B4h, B8h, BCh	Slave PIC ICW1 Init. Cmd Word 1	Undefined	WO
		Slave PIC OCW2 Op Ctrl Word 2	001XXXXXb	WO
		Slave PIC OCW3 Op Ctrl Word 3	X01XXX10b	WO
A1h	A5h, A9h, ADh, B1h, B5h, B9h, BDh	Slave PIC ICW2 Init. Cmd Word 2	Undefined	WO
		Slave PIC ICW3 Init. Cmd Word 3	Undefined	WO
		Slave PIC ICW4 Init. Cmd Word 4	01h	WO
		Slave PIC OCW1 Op Ctrl Word 1	00h	R/W
4D0h	–	Master PIC Edge/Level Triggered	00h	R/W
4D1h	–	Slave PIC Edge/Level Triggered	00h	R/W

Note: Refer to note addressing active-low interrupt sources in 8259 Interrupt Controllers section (Section 5.10).

21.4.2 ICW1 – Initialization Command Word 1 Register (LPC I/F – D31:F0)

Offset Address: Master Controller – 20h / Slave Controller – A0h
Attribute: WO
Size: 8 bit /controller
Default Value: All bits undefined

A write to Initialization Command Word 1 starts the interrupt controller initialization sequence, during which the following occurs:

1. The Interrupt Mask register is cleared.
2. IRQ7 input is assigned priority 7.
3. The slave mode address is set to 7.
4. Special mask mode is cleared and Status Read is set to IRR.

Once this write occurs, the controller expects writes to ICW2, ICW3, and ICW4 to complete the initialization sequence.

Bit	Description
7:5	**ICW/OCW Select** – WO. These bits are MCS-85 specific, and not needed. 000 = Should be programmed to "000"
4	**ICW/OCW Select** – WO. 1 = This bit must be a 1 to select ICW1 and enable the ICW2, ICW3, and ICW4 sequence.
3	**Edge/Level Bank Select (LTIM)** – WO. Disabled. Replaced by the edge/level triggered control registers (ELCR, D31:F0:4D0h, D31:F0:4D1h).

Bit	Description
2	ADI – WO. 0 = Ignored for the Intel® 631xESB/632xESB I/O Controller Hub. Should be programmed to 0.
1	**Single or Cascade (SNGL)** – WO. 0 = Must be programmed to a 0 to indicate two controllers operating in cascade mode.
0	**ICW4 Write Required (IC4)** – WO. 1 = This bit must be programmed to a 1 to indicate that ICW4 needs to be programmed.

21.4.3 ICW2 – Initialization Command Word 2 Register (LPC I/F – D31:F0)

Offset Address: Master Controller – 21h / Slave Controller – A1h
Attribute: WO
Size: 8 bit /controller
Default Value: All bits undefined

ICW2 is used to initialize the interrupt controller with the five most significant bits of the interrupt vector address. The value programmed for bits[7:3] is used by the processor to define the base address in the interrupt vector table for the interrupt routines associated with each IRQ on the controller. Typical ISA ICW2 values are 08h for the master controller and 70h for the slave controller.

Bit	Description
7:3	**Interrupt Vector Base Address** – WO. Bits [7:3] define the base address in the interrupt vector table for the interrupt routines associated with each interrupt request level input.
2:0	**Interrupt Request Level** – WO. When writing ICW2, these bits should all be 0. During an interrupt acknowledge cycle, these bits are programmed by the interrupt controller with the interrupt to be serviced. This is combined with bits [7:3] to form the interrupt vector driven onto the data bus during the second INTA# cycle. The code is a three bit binary code: Code – Master Interrupt – Slave Interrupt 000 – IRQ0 – IRQ8 001 – IRQ1 – IRQ9 010 – IRQ2 – IRQ10 011 – IRQ3 – IRQ11 100 – IRQ4 – IRQ12 101 – IRQ5 – IRQ13 110 – IRQ6 – IRQ14 111 – IRQ7 – IRQ15

21.4.4 ICW3 – Master Controller Initialization Command Word 3 Register (LPC I/F – D31:F0)

Offset Address: 21h
Attribute: WO
Default Value: All bits undefined
Size: 8 bits

Bit	Description
7:3	0 = These bits must be programmed to zero.
2	**Cascaded Interrupt Controller IRQ Connection** – WO. This bit indicates that the slave controller is cascaded on IRQ2. When IRQ8#–IRQ15 is asserted, it goes through the slave controller's priority resolver. The slave controller's INTR output onto IRQ2. IRQ2 then goes through the master controller's priority solver. If it wins, the INTR signal is asserted to the processor, and the returning interrupt acknowledge returns the interrupt vector for the slave controller. 1 = This bit must always be programmed to a 1.
1:0	0 = These bits must be programmed to 0.

21.4.5 ICW3 – Slave Controller Initialization Command Word 3 Register (LPC I/F – D31:F0)

Offset Address: A1h
Default Value: All bits undefined
Attribute: WO
Size: 8 bits

Bit	Description
7:3	0 = These bits must be programmed to zero.
2:0	**Slave Identification Code** – WO. These bits are compared against the slave identification code broadcast by the master controller from the trailing edge of the first internal INTA# pulse to the trailing edge of the second internal INTA# pulse. These bits must be programmed to 02h to match the code broadcast by the master controller. When 02h is broadcast by the master controller during the INTA# sequence, the slave controller assumes responsibility for broadcasting the interrupt vector.

21.4.6 ICW4 – Initialization Command Word 4 Register (LPC I/F – D31:F0)

Offset Address: Master Controller – 021h
Slave Controller – 0A1h
Default Value: 01h
Attribute: WO
Size: 8 bits

Bit	Description
7:5	0 = These bits must be programmed to zero.
4	**Special Fully Nested Mode (SFNM)** – WO. 0 = Should normally be disabled by writing a 0 to this bit. 1 = Special fully nested mode is programmed.
3	**Buffered Mode (BUF)** – WO. 0 = Must be programmed to 0 for the Intel® 631xESB/632xESB I/O Controller Hub. This is non-buffered mode.
2	**Master/Slave in Buffered Mode** – WO. Not used. 0 = Should always be programmed to 0.
1	**Automatic End of Interrupt (AEOI)** – WO. 0 = This bit should normally be programmed to 0. This is the normal end of interrupt. 1 = Automatic End of Interrupt (AEOI) mode is programmed.
0	**Microprocessor Mode** – WO. 1 = Must be programmed to 1 to indicate that the controller is operating in an Intel Architecture-based system.

21.4.7 OCW1 – Operational Control Word 1 (Interrupt Mask) Register (LPC I/F – D31:F0)

Offset Address: Master Controller – 021h
Slave Controller – 0A1h
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	**Interrupt Request Mask** – R/W. When a 1 is written to any bit in this register, the corresponding IRQ line is masked. When a 0 is written to any bit in this register, the corresponding IRQ mask bit is cleared, and interrupt requests will again be accepted by the controller. Masking IRQ2 on the master controller will also mask the interrupt requests from the slave controller.

21.4.8 OCW2 – Operational Control Word 2 Register (LPC I/F – D31:F0)

Offset Address: Master Controller – 020h Attribute: WO
Slave Controller – 0A0h Size: 8 bits
Default Value: Bit[4:0]=undefined, Bit[7:5]=001

Following a part reset or ICW initialization, the controller enters the fully nested mode of operation. Non-specific EOI without rotation is the default. Both rotation mode and specific EOI mode are disabled following initialization.

Bit	Description
7:5	**Rotate and EOI Codes** (R, SL, EOI) – WO. These three bits control the Rotate and End of Interrupt modes and combinations of the two. 000 = Rotate in Auto EOI Mode (Clear) 001 = Non-specific EOI command 010 = No Operation 011 = *Specific EOI Command 100 = Rotate in Auto EOI Mode (Set) 101 = Rotate on Non-Specific EOI Command 110 = *Set Priority Command 111 = *Rotate on Specific EOI Command *L0 – L2 Are Used
4:3	**OCW2 Select** – WO. When selecting OCW2, bits 4:3 = “00”
2:0	**Interrupt Level Select** (L2, L1, L0) – WO. L2, L1, and L0 determine the interrupt level acted upon when the SL bit is active. A simple binary code, outlined below, selects the channel for the command to act upon. When the SL bit is inactive, these bits do not have a defined function; programming L2, L1 and L0 to 0 is sufficient in this case. BitsInterrupt LevelBitsInterrupt Level 000IRQ0/8100IRQ4/12 001IRQ1/9101IRQ5/13 010IRQ2/10110IRQ6/14 011IRQ3/11111IRQ7/15

21.4.9 OCW3 – Operational Control Word 3 Register (LPC I/F – D31:F0)

Offset Address: Master Controller – 020h Attribute: WO
Slave Controller – 0A0h Size: 8 bits
Default Value: Bit[6,0]=0, Bit[7,4:2]=undefined, Bit[5,1]=1

Bit	Description
7	Reserved. Must be 0.
6	**Special Mask Mode (SMM)** – WO. 1 = The Special Mask Mode can be used by an interrupt service routine to dynamically alter the system priority structure while the routine is executing, through selective enabling/disabling of the other channel's mask bits. Bit 5, the ESMM bit, must be set for this bit to have any meaning.
5	**Enable Special Mask Mode (ESMM)** – WO. 0 = Disable. The SMM bit becomes a “don't care”. 1 = Enable the SMM bit to set or reset the Special Mask Mode.

Bit	Description
4:3	**OCW3 Select** – WO. When selecting OCW3, bits 4:3 = 01
2	**Poll Mode Command** – WO. 0 = Disable. Poll Command is not issued. 1 = Enable. The next I/O read to the interrupt controller is treated as an interrupt acknowledge cycle. An encoded byte is driven onto the data bus, representing the highest priority level requesting service.
1:0	**Register Read Command** – WO. These bits provide control for reading the In-Service Register (ISR) and the Interrupt Request Register (IRR). When bit 1=0, bit 0 will not affect the register read selection. When bit 1=1, bit 0 selects the register status returned following an OCW3 read. If bit 0=0, the IRR will be read. If bit 0=1, the ISR will be read. Following ICW initialization, the default OCW3 port address read will be “read IRR”. To retain the current selection (read ISR or read IRR), always write a 0 to bit 1 when programming this register. The selected register can be read repeatedly without reprogramming OCW3. To select a new status register, OCW3 must be reprogrammed prior to attempting the read. 00 = No Action 01 = No Action 10 = Read IRQ Register 11 = Read IS Register

21.4.10 ELCR1 – Master Controller Edge/Level Triggered Register (LPC I/F – D31:F0)

Offset Address: 4D0h Attribute: R/W
Default Value: 00h Size: 8 bits

In edge mode, (bit[x] = 0), the interrupt is recognized by a low to high transition. In level mode (bit[x] = 1), the interrupt is recognized by a high level. The cascade channel, IRQ2, the heart beat timer (IRQ0), and the keyboard controller (IRQ1), cannot be put into level mode.

Bit	Description
7	**IRQ7 ECL** – R/W. 0 = Edge. 1 = Level.
6	**IRQ6 ECL** – R/W. 0 = Edge. 1 = Level.
5	**IRQ5 ECL** – R/W. 0 = Edge. 1 = Level.
4	**IRQ4 ECL** – R/W. 0 = Edge. 1 = Level.
3	**IRQ3 ECL** – R/W. 0 = Edge. 1 = Level.
2:0	Reserved. Must be 0.

21.4.11 ELCR2 – Slave Controller Edge/Level Triggered Register (LPC I/F – D31:F0)

Offset Address: 4D1h
Default Value: 00h
Attribute: R/W
Size: 8 bits

In edge mode, (bit[x] = 0), the interrupt is recognized by a low to high transition. In level mode (bit[x] = 1), the interrupt is recognized by a high level. The real time clock, IRQ8#, and the floating point error interrupt, IRQ13, cannot be programmed for level mode.

Bit	Description
7	**IRQ15 ECL** – R/W. 0 = Edge 1 = Level
6	**IRQ14 ECL** – R/W. 0 = Edge 1 = Level
5	Reserved. Must be 0.
4	**IRQ12 ECL** – R/W. 0 = Edge 1 = Level
3	**IRQ11 ECL** – R/W. 0 = Edge 1 = Level
2	**IRQ10 ECL** – R/W. 0 = Edge 1 = Level
1	**IRQ9 ECL** – R/W. 0 = Edge 1 = Level
0	Reserved. Must be 0.

21.5 Advanced Programmable Interrupt Controller (APIC)(D31:F0)

21.5.1 APIC Register Map (LPC I/F – D31:F0)

The APIC is accessed via an indirect addressing scheme. Two registers are visible by software for manipulation of most of the APIC registers. These registers are mapped into memory space. The registers are shown in Table 21-4.

Table 21-4. APIC Direct Registers (LPC I/F – D31:F0)

Address	Mnemonic	Register Name	Size	Type
FEC0_0000h	IND	Index	8 bits	R/W
FEC0_0010h	WDW	Window	32 bits	R/W
FECO_0040h	EOIR	EOI	32 bits	WO

Table 21-5 lists the registers which can be accessed within the APIC via the Index Register. When accessing these registers, accesses must be done a DWord at a time. For example, software should never access byte 2 from the Data register before accessing bytes 0 and 1. The hardware will not attempt to recover from a bad programming model in this case.

Table 21-5. APIC Indirect Registers (LPC I/F – D31:F0)

Index	Mnemonic	Register Name	Size	Type
00	ID	Identification	32 bits	R/W
01	VER	Version	32 bits	RO
02–0F	–	Reserved	–	RO
10–11	REDIR_TBL0	Redirection Table 0	64 bits	R/W, RO
12–13	REDIR_TBL1	Redirection Table 1	64 bits	R/W, RO
…	…	…	…	…
3E–3F	REDIR_TBL23	Redirection Table 23	64 bits	R/W, RO
40–FF	–	Reserved	–	RO

21.5.2 IND – Index Register (LPC I/F – D31:F0)

Memory Address FEC0_0000h Attribute: R/W
Default Value: 00h Size: 8 bits

The Index Register will select which APIC indirect register to be manipulated by software. The selector values for the indirect registers are listed in Table 21-5. Software will program this register to select the desired APIC internal register

Bit	Description
7:0	**APIC Index** – R/W. This is an 8-bit pointer into the I/O APIC register table.

21.5.3 DAT – Window Register (LPC I/F – D31:F0)

Memory Address FEC0_0010h Attribute: R/W
Default Value: 00000000h Size: 32 bits

This is a 32-bit register specifying the data to be read or written to the register pointed to by the Index register. This register can only be accessed in DWord quantities.

Bit	Description
7:0	**EOIx** – R/W. This is a 32-bit register for the data to be read or written to the APIC indirect register (Figure 21-5) pointed to by the Index register (Memory Address FEC0_0000h).

21.5.4 EOIR – EOI Register (LPC I/F – D31:F0)

Memory Address FEC0_0040h Attribute: WO
Default Value: N/A Size: 32 bits

The EOI register is present to provide a mechanism to maintain the level triggered semantics for level-triggered interrupts issued on the parallel bus.

When a write is issued to this register, the I/O APIC will check the lower 8 bits written to this register, and compare it with the vector field for each entry in the I/O Redirection Table. When a match is found, the Remote_IRR bit (Index Offset 10h, bit 14) for that I/O Redirection Entry will be cleared.

Note: If multiple I/O Redirection entries, for any reason, assign the same vector for more than one interrupt input, each of those entries will have the Remote_IRR bit reset to 0. The interrupt which was prematurely reset will not be lost because if its input remained active when the Remote_IRR bit is cleared, the interrupt will be reissued and serviced

at a later time. Note: Only bits 7:0 are actually used. Bits 31:8 are ignored by the Intel® 631xESB/632xESB I/O Controller Hub.

Note: To provide for future expansion, the processor should always write a value of 0 to Bits 31:8.

Bit	Description
31:8	Reserved. To provide for future expansion, the processor should always write a value of 0 to Bits 31:8.
7:0	**Redirection Entry Clear** – WO. When a write is issued to this register, the I/O APIC will check this field, and compare it with the vector field for each entry in the I/O Redirection Table. When a match is found, the Remote_IRR bit for that I/O Redirection Entry will be cleared.

21.5.5 ID – Identification Register (LPC I/F – D31:F0)

Index Offset: 00h Attribute: R/W
Default Value: 00000000h Size: 32 bits

The APIC ID serves as a physical name of the APIC. The APIC bus arbitration ID for the APIC is derived from its I/O APIC ID. This register is reset to 0 on power-up reset.

Bit	Description
31:28	Reserved
27:24	**APIC ID** – R/W. Software must program this value before using the APIC.
23:16	Reserved
15	Scratchpad Bit.
14:0	Reserved

21.5.6 VER – Version Register (LPC I/F – D31:F0)

Index Offset: 01h Attribute: RO
Default Value: 00170020h Size: 32 bits

Each I/O APIC contains a hardwired Version Register that identifies different implementation of APIC and their versions. The maximum redirection entry information also is in this register, to let software know how many interrupt are supported by this APIC.

Bit	Description
31:24	Reserved
23:16	Maximum Redirection Entries – RO. This is the entry number (0 being the lowest entry) of the highest entry in the redirection table. It is equal to the number of interrupt input pins minus one and is in the range 0 through 239. In the Intel® 631xESB/632xESB I/O Controller Hub this field is hardwired to 17h to indicate 24 interrupts.
15	PRQ – RO. Indicate that the IOxAPIC does not implement the Pin Assertion Register.
14:8	Reserved
7:0	Version – RO. This is a version number that identifies the implementation version.

21.5.7 REDIR_TBL – Redirection Table (LPC I/F – D31:F0)

Index Offset:	10h–11h (vector 0) through 3E–3Fh (vector 23)	Attribute:	R/W, RO
Default Value:	Bit 16 = 1,. All other bits undefined	Size:	64 bits each, (accessed as two 32 bit quantities)

The Redirection Table has a dedicated entry for each interrupt input pin. The information in the Redirection Table is used to translate the interrupt manifestation on the corresponding interrupt pin into an APIC message.

The APIC will respond to an edge triggered interrupt as long as the interrupt is held until after the acknowledge cycle has begun. Once the interrupt is detected, a delivery status bit internally to the I/O APIC is set. The state machine will step ahead and wait for an acknowledgment from the APIC unit that the interrupt message was sent. Only then will the I/O APIC be able to recognize a new edge on that interrupt pin. That new edge will only result in a new invocation of the handler if its acceptance by the destination APIC causes the Interrupt Request Register bit to go from 0 to 1. (In other words, if the interrupt was not already pending at the destination.)

Bit	Description
63:56	**Destination** – R/W. If bit 11 of this entry is 0 (Physical), then bits 59:56 specifies an APIC ID. In this case, bits 63:59 should be programmed by software to 0. If bit 11 of this entry is 1 (Logical), then bits 63:56 specify the logical destination address of a set of processors.
55:48	**Extended Destination ID (EDID)** – RO. These bits are sent to a local APIC only when in Processor System Bus mode. They become bits 11:4 of the address.
47:17	Reserved
16	Mask – R/W. 0 = Not masked: An edge or level on this interrupt pin results in the delivery of the interrupt to the destination. 1 = Masked: Interrupts are not delivered nor held pending. Setting this bit after the interrupt is accepted by a local APIC has no effect on that interrupt. This behavior is identical to the device withdrawing the interrupt before it is posted to the processor. It is software's responsibility to deal with the case where the mask bit is set after the interrupt message has been accepted by a local APIC unit but before the interrupt is dispensed to the processor.
15	**Trigger Mode** – R/W. This field indicates the type of signal on the interrupt pin that triggers an interrupt. 0 = Edge triggered. 1 = Level triggered.
14	**Remote IRR** – R/W. This bit is used for level triggered interrupts; its meaning is undefined for edge triggered interrupts. 0 = Reset when an EOI message is received from a local APIC. 1 = Set when Local APIC/s accept the level interrupt sent by the I/O APIC.
13	**Interrupt Input Pin Polarity** – R/W. This bit specifies the polarity of each interrupt signal connected to the interrupt pins. 0 = Active high. 1 = Active low.
12	**Delivery Status** – RO. This field contains the current status of the delivery of this interrupt. Writes to this bit have no effect. 0 = Idle. No activity for this interrupt. 1 = Pending. Interrupt has been injected, but delivery is not complete.
11	**Destination Mode** – R/W. This field determines the interpretation of the Destination field. 0 = Physical. Destination APIC ID is identified by bits 59:56. 1 = Logical. Destinations are identified by matching bit 63:56 with the Logical Destination in the Destination Format Register and Logical Destination Register in each Local APIC.
10:8	**Delivery Mode** – R/W. This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are listed in the note below:
7:0	**Vector** – R/W. This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

Note: Delivery Mode encoding:

000 = Fixed. Deliver the signal on the INTR signal of all processor cores listed in the destination. Trigger Mode can be edge or level.

001 = Lowest Priority. Deliver the signal on the INTR signal of the processor core that is executing at the lowest priority among all the processors listed in the specified destination. Trigger Mode can be edge or level.

010 = SMI (System Management Interrupt). Requires the interrupt to be programmed as edge triggered. The vector information is ignored but must be programmed to all zeroes for future compatibility: **not supported**

011 = Reserved

100 = NMI. Deliver the signal on the NMI signal of all processor cores listed in the destination. Vector information is ignored. NMI is treated as an edge triggered interrupt even if it is programmed as level triggered. For proper operation this redirection table entry must be programmed to edge triggered. The NMI delivery mode does not set the RIRR bit. If the redirection table is incorrectly set to level, the loop count will continue counting through the redirection table addresses. Once the count for the NMI pin is reached again, the interrupt will be sent again: **not supported**

101 = INIT. Deliver the signal to all processor cores listed in the destination by asserting the INIT signal. All addressed local APICs will assume their INIT state. INIT is always treated as an edge triggered interrupt even if programmed as level triggered. For proper operation this redirection table entry must be programmed to edge triggered. The INIT delivery mode does not set the RIRR bit. If the redirection table is incorrectly set to level, the loop count will continue counting through the redirection table addresses. Once the count for the INIT pin is reached again, the interrupt will be sent again: **not supported**

110 = Reserved

111 = ExtINT. Deliver the signal to the INTR signal of all processor cores listed in the destination as an interrupt that originated in an externally connected 8259A compatible interrupt controller. The INTA cycle that corresponds to this ExtINT delivery will be routed to the external controller that is expected to supply the vector. Requires the interrupt to be programmed as edge triggered.

21.6 Real Time Clock Registers (LPC I/F – D31:F0)

21.6.1 I/O Register Address Map (LPC I/F – D31:F0)

The RTC internal registers and RAM are organized as two banks of 128 bytes each, called the standard and extended banks. The first 14 bytes of the standard bank contain the RTC time and date information along with four registers, A–D, that are used for configuration of the RTC. The extended bank contains a full 128 bytes of battery backed SRAM, and will be accessible even when the RTC module is disabled (via the RTC configuration register). Registers A–D do not physically exist in the RAM.

All data movement between the host processor and the real-time clock is done through registers mapped to the standard I/O space. The register map appears in Table 21-6.

Table 21-6. RTC I/O Registers (LPC I/F – D31:F0)

I/O Locations	If U128E bit = 0	Function
70h and 74h	Also alias to 72h and 76h	Real-Time Clock (Standard RAM) Index Register
71h and 75h	Also alias to 73h and 77h	Real-Time Clock (Standard RAM) Target Register
72h and 76h		Extended RAM Index Register (if enabled)
73h and 77h		Extended RAM Target Register (if enabled)

Notes:

1. I/O locations 70h and 71h are the standard legacy location for the real-time clock. The map for this bank is shown in Table 21-7. Locations 72h and 73h are for accessing the extended RAM. The extended RAM bank is also accessed using an indexed scheme. I/O address 72h is used as the address pointer and I/O address 73h is used as the data register. Index addresses above 127h are not valid. If the extended RAM is not needed, it may be disabled.
2. Software must preserve the value of bit 7 at I/O addresses 70h and 74h. When writing to this address, software must first read the value, and then write the same value for bit 7 during the sequential address write. Note that port 70h is not

directly readable. The only way to read this register is through Alt Access mode. Although RTC Index bits 6:0 are readable from port 74h, bit 7 will always return 0. If the NMI# enable is not changed during normal operation, software can alternatively read this bit once and then retain the value for all subsequent writes to port 70h.

21.6.2 Indexed Registers (LPC I/F – D31:F0)

The RTC contains two sets of indexed registers that are accessed using the two separate Index and Target registers (70/71h or 72/73h), as shown in Table 21-7.

Table 21-7. RTC (Standard) RAM Bank (LPC I/F – D31:F0)

Index	Name
00h	Seconds
01h	Seconds Alarm
02h	Minutes
03h	Minutes Alarm
04h	Hours
05h	Hours Alarm
06h	Day of Week
07h	Day of Month
08h	Month
09h	Year
0Ah	Register A
0Bh	Register B
0Ch	Register C
0Dh	Register D
0Eh–7Fh	114 Bytes of User RAM

21.6.2.1 RTC_REGA – Register A (LPC I/F – D31:F0)

RTC Index:	0A	Attribute:	R/W
Default Value:	Undefined	Size:	8-bit
Lockable:	No	Power Well:	RTC

This register is used for general configuration of the RTC functions. None of the bits are affected by RSMRST# or any other Intel® 631xESB/632xESB I/O Controller Hub reset signal.

Bit	Description
7	**Update In Progress (UIP) –** R/W. This bit may be monitored as a status flag. 0 = The update cycle will not start for at least 488 µs. The time, calendar, and alarm information in RAM is always available when the UIP bit is 0. 1 = The update is soon to occur or is in progress.
6:4	**Division Chain Select (DV[2:0]) –** R/W. These three bits control the divider chain for the oscillator, and are not affected by RSMRST# or any other reset signal. DV2 corresponds to bit 6. 010 = Normal Operation 11X = Divider Reset 101 = Bypass 15 stages (test mode only) 100 = Bypass 10 stages (test mode only) 011 = Bypass 5 stages (test mode only) 001 = Invalid 000 = Invalid
3:0	**Rate Select (RS[3:0]) –** R/W. Selects one of 13 taps of the 15 stage divider chain. The selected tap can generate a periodic interrupt if the PIE bit is set in Register B. Otherwise this tap will set the PF flag of Register C. If the periodic interrupt is not to be used, these bits should all be set to zero. RS3 corresponds to bit 3. 0000 = Interrupt never toggles 0001 = 3.90625 ms 0010 = 7.8125 ms 0011 = 122.070 µs 0100 = 244.141 µs 0101 = 488.281 µs 0110 = 976.5625 µs 0111 = 1.953125 ms 1000 = 3.90625 ms 1001 = 7.8125 ms 1010 = 15.625 ms 1011 = 31.25 ms 1100 = 62.5 ms 1101 = 125 ms 1110 = 250 ms 1111= 500 ms

21.6.2.2 RTC_REGB – Register B (General Configuration) (LPC I/F – D31:F0)

RTC Index:	0Bh	Attribute:	R/W
Default Value:	U0U00UUU (U: Undefined)	Size:	8-bit
Lockable:	No	Power Well:	RTC

Bit	Description
7	**Update Cycle Inhibit (SET) –** R/W. Enables/Inhibits the update cycles. This bit is not affected by RSMRST# nor any other reset signal. 0 = Update cycle occurs normally once each second. 1 = A current update cycle will abort and subsequent update cycles will not occur until SET is returned to zero. When set is one, the BIOS may initialize time and calendar bytes safely. ***Note:*** This bit should be set then cleared early in BIOS POST after each powerup directly after coin-cell battery insertion.
6	Periodic Interrupt Enable **(**PIE) – R/W. This bit is cleared by RSMRST#, but not on any other reset. 0 = Disable. 1 = Enable. Allows an interrupt to occur with a time base set with the RS bits of register A.
5	Alarm Interrupt Enable **(**AIE) – R/W. This bit is cleared by RTCRST#, but not on any other reset. 0 = Disable. 1 = Enable. Allows an interrupt to occur when the AF is set by an alarm match from the update cycle. An alarm can occur once a second, one an hour, once a day, or one a month.

Bit	Description
4	Update-Ended Interrupt Enable (UIE) – R/W. This bit is cleared by RSMRST#, but not on any other reset. 0 = Disable. 1 = Enable. Allows an interrupt to occur when the update cycle ends.
3	**Square Wave Enable (SQWE) –** R/W. This bit serves no function in the Intel® 631xESB/632xESB I/O Controller Hub. It is left in this register bank to provide compatibility with the Motorola 146818B. The Intel® 631xESB/632xESB I/O Controller Hub has no SQW pin. This bit is cleared by RSMRST#, but not on any other reset.
2	**Data Mode (DM) –** R/W. This bit specifies either binary or BCD data representation. This bit is not affected by RSMRST# nor any other reset signal. 0 = BCD 1 = Binary
1	**Hour Format (HOURFORM) –** R/W. This bit indicates the hour byte format. This bit is not affected by RSMRST# nor any other reset signal. 0 = Twelve-hour mode. In twelve-hour mode, the seventh bit represents AM as zero and PM as one. 1 = Twenty-four hour mode.
0	**Daylight Savings Enable (DSE) –** R/W. This bit triggers two special hour updates per year. The days for the hour adjustment are those specified in United States federal law as of 1987, which is different than previous years. This bit is not affected by RSMRST# nor any other reset signal. 0 = Daylight Savings Time updates do not occur. 1 = a) Update on the first Sunday in April, where time increments from 1:59:59 AM to 3:00:00 AM. b) Update on the last Sunday in October when the time first reaches 1:59:59 AM, it is changed to 1:00:00 AM. The time must increment normally for at least two update cycles (seconds) previous to these conditions for the time change to occur properly.

21.6.2.3 RTC_REGC – Register C (Flag Register) (LPC I/F – D31:F0)

RTC Index:	0Ch	Attribute:	RO
Default Value:	00U00000 (U: Undefined)	Size:	8-bit
Lockable:	No	Power Well:	RTC

Writes to Register C have no effect.

Bit	Description
7	**Interrupt Request Flag (IRQF) –** RO. IRQF = (PF * PIE) + (AF * AIE) + (UF *UFE). This bit also causes the RTC Interrupt to be asserted. This bit is cleared upon RSMRST# or a read of Register C.
6	**Periodic Interrupt Flag (PF) –** RO. This bit is cleared upon RSMRST# or a read of Register C. 0 = If no taps are specified via the RS bits in Register A, this flag will not be set. 1 = Periodic interrupt Flag will be 1 when the tap specified by the RS bits of register A is 1.
5	**Alarm Flag (AF) –** RO. 0 = This bit is cleared upon RTCRST# or a read of Register C. 1 = Alarm Flag will be set after all Alarm values match the current time.
4	**Update-Ended Flag (UF) –** RO. 0 = The bit is cleared upon RSMRST# or a read of Register C. 1 = Set immediately following an update cycle for each second.
3:0	Reserved. Will always report 0.

21.6.2.4 RTC_REGD – Register D (Flag Register) (LPC I/F – D31:F0)

RTC Index:	0Dh	Attribute:	R/W
Default Value:	10UUUUUU (U: Undefined)	Size:	8-bit
Lockable:	No	Power Well:	RTC

Bit	Description
7	**Valid RAM and Time Bit (VRT)** – R/W. 0 = This bit should always be written as a 0 for write cycle, however it will return a 1 for read cycles. 1 = This bit is hardwired to 1 in the RTC power well.
6	Reserved. This bit always returns a 0 and should be set to 0 for write cycles.
5:0	**Date Alarm** – R/W. These bits store the date of month alarm value. If set to 000000b, then a don't care state is assumed. The host must configure the date alarm for these bits to do anything, yet they can be written at any time. If the date alarm is not enabled, these bits will return 0's to mimic the functionality of the Motorola 146818B. These bits are not affected by any reset assertion.

21.7 Processor Interface Registers (LPC I/F – D31:F0)

Table 21-8 is the register address map for the processor interface registers.

Table 21-8. Processor Interface PCI Register Address Map (LPC I/F – D31:F0)

Offset	Mnemonic	Register Name	Default	Type
61h	NMI_SC	NMI Status and Control	00h	R/W, RO
70h	NMI_EN	NMI Enable	80h	R/W (special)
92h	PORT92	Fast A20 and Init	00h	R/W
F0h	COPROC_ERR	Coprocessor Error	00h	WO
CF9h	RST_CNT	Reset Control	00h	R/W

21.7.1 NMI_SC – NMI Status and Control Register (LPC I/F – D31:F0)

I/O Address:	61h	Attribute:	R/W, RO
Default Value:	00h	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7	**SERR# NMI Source Status (SERR#_NMI_STS) –** RO. 1 = Bit is set if a PCI agent detected a system error and pulses the PCI SERR# line and if bit 2 (PCI_SERR_EN) is cleared. This interrupt source is enabled by setting bit 2 to 0. To reset the interrupt, set bit 2 to 1 and then set it to 0. When writing to port 61h, this bit must be 0. ***Note:*** This bit is set by any of the Intel® 631xESB/632xESB I/O Controller Hub internal sources of SERR; this includes SERR assertions forwarded from the secondary PCI bus, errors on a PCI Express port, or other internal functions that generate SERR#.
6	**IOCHK# NMI Source Status (IOCHK_NMI_STS) –** RO. 1 = Bit is set if an LPC agent (via SERIRQ) asserted IOCHK# and if bit 3 (IOCHK_NMI_EN) is cleared. This interrupt source is enabled by setting bit 3 to 0. To reset the interrupt, set bit 3 to 1 and then set it to 0. When writing to port 61h, this bit must be a 0.
5	**Timer Counter 2 OUT Status (TMR2_OUT_STS) –** RO. This bit reflects the current state of the 8254 counter 2 output. Counter 2 must be programmed following any PCI reset for this bit to have a determinate value. When writing to port 61h, this bit must be a 0.
4	**Refresh Cycle Toggle (REF_TOGGLE) –** RO. This signal toggles from either 0 to 1 or 1 to 0 at a rate that is equivalent to when refresh cycles would occur. When writing to port 61h, this bit must be a 0.

Bit	Description
3	**IOCHK# NMI Enable (IOCHK_NMI_EN) –** R/W. 0 = Enabled. 1 = Disabled and cleared.
2	**PCI SERR# Enable (PCI_SERR_EN) –** R/W. 0 = SERR# NMIs are enabled. 1 = SERR# NMIs are disabled and cleared.
1	**Speaker Data Enable (SPKR_DAT_EN) –** R/W. 0 = SPKR output is a 0. 1 = SPKR output is equivalent to the Counter 2 OUT signal value.
0	**Timer Counter 2 Enable (TIM_CNT2_EN) –** R/W. 0 = Disable 1 = Enable

21.7.2 NMI_EN – NMI Enable (and Real Time Clock Index) Register (LPC I/F – D31:F0)

I/O Address:	70h	Attribute:	R/W (special)
Default Value:	80h	Size:	8-bit
Lockable:	No	Power Well:	Core

Note: The RTC Index field is write-only for normal operation. This field can only be read in Alt-Access Mode. Note, however, that this register is aliased to Port 74h (documented in), and all bits are readable at that address.

Bits	Description
7	**NMI Enable (NMI_EN) –** R/W (special). 0 = Enable NMI sources. 1 = Disable All NMI sources.
6:0	**Real Time Clock Index Address (RTC_INDX) –** R/W (special). This data goes to the RTC to select which register or CMOS RAM address is being accessed.

21.7.3 PORT92 – Fast A20 and Init Register (LPC I/F – D31:F0)

I/O Address:	92h	Attribute:	R/W
Default Value:	00h	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7:2	Reserved
1	**Alternate A20 Gate (ALT_A20_GATE) –** R/W. This bit is Or'd with the A20GATE input signal to generate A20M# to the processor. 0 = A20M# signal can potentially go active. 1 = This bit is set when INIT# goes active.
0	**INIT_NOW** – R/W. When this bit transitions from a 0 to a 1, the Intel® 631xESB/632xESB I/O Controller Hub will force INIT# active for 16 PCI clocks.

21.7.4 COPROC_ERR – Coprocessor Error Register (LPC I/F – D31:F0)

I/O Address:	F0h	Attribute:	WO
Default Value:	00h	Size:	8-bits
Lockable:	No	Power Well:	Core

Bits	Description
7:0	**Coprocessor Error (COPROC_ERR)** – WO. Any value written to this register will cause IGNNE# to go active, if FERR# had generated an internal IRQ13. For FERR# to generate an internal IRQ13, the COPROC_ERR_EN bit (Device 31:Function 0, Offset D0, Bit 13) must be 1.

21.7.5 RST_CNT – Reset Control Register (LPC I/F – D31:F0)

I/O Address:	CF9h	Attribute:	R/W
Default Value:	00h	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7:4	Reserved
3	**Full Reset (FULL_RST) –** R/W. This bit is used to determine the states of SLP_S3#, SLP_S4#, and SLP_S5# after a CF9 hard reset (SYS_RST =1 and RST_CPU is set to 1), after PWROK going low (with RSMRST# high), or after two TCO timeouts. 0 = Intel® 631xESB/632xESB I/O Controller Hub will keep SLP_S3#, SLP_S4# and SLP_S5# high. 1 = Intel® 631xESB/632xESB I/O Controller Hub will drive SLP_S3#, SLP_S4# and SLP_S5# low for 3 – 5 seconds. ***Note:*** When this bit is set, it also causes the full power cycle (SLP_S3/4/5# assertion) in response to SYSRESET#, PWROK#, and Watchdog timer reset sources.
2	**Reset CPU (RST_CPU)** – R/W. When this bit transitions from a 0 to a 1, it initiates a hard or soft reset, as determined by the SYS_RST bit (bit 1 of this register).
1	**System Reset (SYS_RST) –** R/W. This bit is used to determine a hard or soft reset to the processor. 0 = When RST_CPU bit goes from 0 to 1, the Intel® 631xESB/632xESB I/O Controller Hub performs a soft reset by activating INIT# for 16 PCI clocks. 1 = When RST_CPU bit goes from 0 to 1, the Intel® 631xESB/632xESB I/O Controller Hub performs a hard reset by activating PLTRST# for 1 millisecond. It also resets the resume well bits (except for those noted throughout the EDS). The SLP_S3#, SLP_S4#, and SLP_S5# signals will not go active.
0	Reserved

21.8 Power Management Registers (PM – D31:F0)

The power management registers are distributed within the PCI Device 31: Function 0 space, as well as a separate I/O range. Each register is described below. Unless otherwise indicate, bits are in the main (core) power well.

Bits not explicitly defined in each register are assumed to be reserved. When writing to a reserved bit, the value should always be 0. Software should not attempt to use the value read from a reserved bit, as it may not be consistently 1 or 0.

21.8.1 Power Management PCI Configuration Registers (PM – D31:F0)

Table 21-9 shows a small part of the configuration space for PCI Device 31: Function 0. It includes only those registers dedicated for power management. Some of the registers are only used for Legacy Power management schemes.

Table 21-9. Power Management PCI Register Address Map (PM – D31:F0)

Offset	Mnemonic	Register Name	Default	Type
A0h	GEN_PMCON_1	General Power Management Configuration 1	0000h	R/W, RO, R/WO
A2h	GEN_PMCON_2	General Power Management Configuration 2	0000h	R/W, R/WC
A4h	GEN_PMCON_3	General Power Management Configuration 3	00h	R/W, R/WC
ACh	ETR3	Extended Test Mode Register 3	00	R/W
B8–BBh	GPI_ROUT	GPI Route Control	00000000h	R/W

21.8.1.1 GEN_PMCON_1 – General PM Configuration 1 Register (PM – D31:F0)

Offset Address: A0h
Default Value: 0000h
Lockable: No
Attribute: R/W, RO, R/WO
Size: 16-bit
Usage: ACPI, Legacy
Power Well: Core

Bit	Description
15:11	Reserved
10	**BIOS_PCI_EXP_EN** – R/W. This bit acts as a global enable for the SCI associated with the PCI Express ports. 0 = The various PCI Express ports and (G)MCH cannot cause the PCI_EXP_STS bit to go active. 1 = The various PCI Express ports and (G)MCH can cause the PCI_EXP_STS bit to go active.
9	**PWRBTN_LVL** – RO. This bit indicates the current state of the PWRBTN# signal. 0 = Low. 1 = High.
8	Reserved
7	Reserved
6	**i64_EN**. Software sets this bit to indicate that the processor is an IA_64 processor, not an IA_32 processor. This may be used in various state machines where there are behavioral differences.
5	**CPU SLP# Enable (CPUSLP_EN) –** R/W. 0 = Disable. 1 = Enables the CPUSLP# signal to go active in theS1 state. This reduces the processor power. ***Note:*** CPUSLP# will go active during Intel SpeedStep technology transitions and on entry to C3, C4, S3, S4 and S5 even if this bit is not set.
4	**SMI_LOCK –** R/WO. When this bit is set, writes to the GLB_SMI_EN bit (PMBASE + 30h, bit 0) will have no effect. Once the SMI_LOCK bit is set, writes of 0 to SMI_LOCK bit will have no effect (that is, once set, this bit can only be cleared by PLTRST#).
3:2	Reserved
1:0	Periodic SMI# Rate Select **(**PER_SMI_SEL) – R/W. Set by software to control the rate at which periodic SMI# is generated. 00 = 1 minute 01 = 32 seconds 10 = 16 seconds 11 = 8 seconds

21.8.1.2 GEN_PMCON_2 – General PM Configuration 2 Register (PM – D31:F0)

Offset Address:	A2h	Attribute:	R/W, R/WC
Default Value:	00h	Size:	8-bit
Lockable:	No	Usage:	ACPI, Legacy
		Power Well:	Resume

Bit	Description
7	DRAM Initialization Bit – R/W. This bit does not effect hardware functionality in any way. BIOS is expected to set this bit prior to starting the DRAM initialization sequence and to clear this bit after completing the DRAM initialization sequence. BIOS can detect that a DRAM initialization sequence was interrupted by a reset by reading this bit during the boot sequence. • If the bit is 1, then the DRAM initialization was interrupted. • This bit is reset by the assertion of the RSMRST# pin.
6:5	Reserved
4	**System Reset Status (SRS) –** R/WC. Software clears this bit by writing a 1 to it. 0 = SYS_RESET# button Not pressed. 1 = Intel® 631xESB/632xESB I/O Controller Hub sets this bit when the SYS_RESET# button is pressed. BIOS is expected to read this bit and clear it, if it is set. ***Note:*** This bit is also reset by RSMRST# and CF9h resets.
3	**CPU Thermal Trip Status (CTS) –** R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = This bit is set when PLTRST# is inactive and THRMTRIP# goes active while the system is in an S0 or S1 state. ***Notes:*** 1. This bit is also reset by RSMRST#, and CF9h resets. It is not reset by the shutdown and reboot associated with the CPUTHRMTRIP# event. 2. The CF9h reset in the description refers to CF9h type core well reset which includes SYS_RST#, PWROK/VRMPWRGD low, SMBus hard reset, TCO Timeout. This type of reset will clear CTS bit.
2	Minimum SLP_S4# Assertion Width Violation Status – R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = Hardware sets this bit when the SLP_S4# assertion width is less than the time programmed in the SLP_S4# Minimum Assertion Width field. When exiting G3, the Intel® 631xESB/632xESB I/O Controller Hub begins the timer when the RSMRST# input deasserts. Note that this bit is functional regardless of the value in the SLP_S4# Assertion Stretch Enable. ***Note:*** This bit is reset by the assertion of the RSMRST# pin, but can be set in some cases before the default value is readable.
1	CPU Power Failure **(**CPUPWR_FLR) – R/WC. 0 = Software (typically BIOS) clears this bit by writing a 0 to it. 1 = Indicates that the VRMPWRGD signal from the processor's VRM went low.
0	**PWROK Failure (PWROK_FLR) –** R/WC. 0 = Software clears this bit by writing a 1 to it, or when the system goes into a G3 state. 1 = This bit will be set any time PWROK goes low, when the system was in S0, or S1 state. The bit will be cleared only by software by writing a 1 to this bit or when the system goes to a G3 state. ***Note:*** See Section 5.15.10.3 for more details about the PWROK pin functionality. ***Note:*** In the case of true PWROK failure, PWROK will go low first before the VRMPWRGD.

Note: VRMPWROK is sampled using the RTC clock. Therefore, low times that are less than one RTC clock period may not be detected by the Intel® 631xESB/632xESB I/O Controller Hub.

21.8.1.3 GEN_PMCON_3 – General PM Configuration 3 Register (PM – D31:F0)

Offset Address:	A4h	Attribute:	R/W, R/WC
Default Value:	00h	Size:	8-bit
Lockable:	No	Usage:	ACPI, Legacy
		Power Well:	RTC

Bit	Description
7:6	**SWSMI_RATE_SEL** – R/W. This field indicates when the SWSMI timer will time out. Valid values are: 00 = 1.5 ms ± 0.6 ms 01 = 16 ms ± 4 ms 10 = 32 ms ± 4 ms 11 = 64 ms ± 4 ms These bits are not cleared by any type of reset except RTCRST#.
5:4	SLP_S4# Minimum Assertion Width – R/W. This field indicates the minimum assertion width of the SLP_S4# signal to guarantee that the DRAMs have been safely power-cycled. Valid values are: 11 = 1 to 2 seconds 10 = 2 to 3 seconds 01 = 3 to 4 seconds 00 = 4 to 5 seconds This value is used in two ways: 1. If the SLP_S4# assertion width is ever shorter than this time, a status bit is set for BIOS to read when S0 is entered. 2. If enabled by bit 3 in this register, the hardware will prevent the SLP_S4# signal from deasserting within this minimum time period after asserting. RTCRST# forces this field to the conservative default state (00b)
3	SLP_S4# Assertion Stretch Enable – R/W. 0 = The SLP_S4# minimum assertion time is 1 to 2 RTCCLK. 1 = The SLP_S4# signal minimally assert for the time specified in bits 5:4 of this register. This bit is cleared by RTCRST#
2	**RTC Power Status (RTC_PWR_STS)** – R/W. This bit is set when RTCRST# indicates a weak or missing battery. The bit is not cleared by any type of reset. The bit will remain set until the software clears it by writing a 0 back to this bit position.
1	**Power Failure (PWR_FLR) –** R/WC. This bit is in the RTC well, and is not cleared by any type of reset except RTCRST#. 0 = Indicates that the trickle current has not failed since the last time the bit was cleared. Software clears this bit by writing a 1 to it. 1 = Indicates that the trickle current (from the main battery or trickle supply) was removed or failed. ***Note:*** Clearing CMOS in an Intel® 631xESB/632xESB I/O Controller Hub-based platform can be done by using a jumper on RTCRST# or GPI, or using SAFEMODE strap. Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low.
0	**AFTERG3_EN** – R/W. This bit determines what state to go to when power is re-applied after a power failure (G3 state). This bit is in the RTC well and is not cleared by any type of reset except writes to CF9h or RTCRST#. 0 = System will return to S0 state (boot) after power is re-applied. 1 = System will return to the S5 state (except if it was in S4, in which case it will return to S4). In the S5 state, the only enabled wake event is the Power Button or any enabled wake event that was preserved through the power failure. ***Note:*** Bit will be set when THRMTRIP#-based shutdown occurs.

Note: RSMRST# is sampled using the RTC clock. Therefore, low times that are less than one RTC clock period may not be detected by the Intel® 631xESB/632xESB I/O Controller Hub.

21.8.1.4 ETR3 – Extended Test Mode Register 3(PM – D31:F0)

Offset Address:	ACh	Attribute:	R/W
Default Value:	00h	Size:	32 bit
Power Well:	Resume		

Note: This register resides in the resume well. Bit [13:12] are reset by internal resume well reset (WrsmrstB).

Bit	Description
31:20	Reserved
19	**Second LAN PowerUp Reset Disable**: 0 = It is an indication that resume well power was applied. BIOS sets this bit every time after it carried out the additional LAN reset for system that implements LAN disable through GPIO. 1 = BIOS should not perform the additional LAN reset. This bit is only cleared when RSMRST# goes low.
18	**CF9h Without Resume Well Reset Enable**: 0 = CF9h write of 6h or Eh will also reset resume well logic. 1 = CF9h write of 6h or Eh will not cause internal Resume Well Reset (WrsmrstB) to be asserted and thus resume well logic will maintain to their states. This bit is to be used when a second reset through CF9 write is desired upon power up or after resume from low power states. This bit has to be set prior to the write to CF9 register and has to be cleared upon completing the reset. Failing to do so prevents resume well registers from being reset in the future CF9 writes.
17:14	Reserved
13	LPC Generic Range 2 Bit 5 Mask: 0 = The existing LPC Generic I/O decode range 2 decodes bit 5 as defined in D31:F0:88h register description. 1 = The LPC Generic I/O decode range 2 forces an address match on bit 5.
12	LPC Generic Range 2 Bit 4 Mask: 0 = The existing LPC Generic I/O decode range 2 decodes bit 4 as defined in D31:F0:88h register description. 1 = The LPC Generic I/O decode range 2 forces an address match on bit 4.
11:10	Reserved

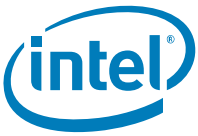
Bit	Description
9	**Digital Filter Enable**: 0 = (Default) the existing functionality is maintained (analog filtering up to 60 ns) 1 = It turns ON the digital filter circuit on the transient disconnect detect, which prevents transient disconnects less than 25 us long from being detected.
8	**Transient Disconnect Detect Enable**: 0 = (Default) this ensures that a single-ended zero on any of the USB ports will have to last at least 64 microseconds to be detected as a disconnect. 1 = It turns ON the “Transient Disconnect Detect” functionality in the Classic USB controllers and functions the same as ICH3.
7:0	**SV Probe Mode Select:** This is the select for one of the 256 possible sets of internal signals driven externally for observability. The balls used for this feature are identical to the LAN/USB 2.0 Probe Mode pins: **Bit Pin** 00 oc0# 01 oc1# 02 oc2# 03 oc3# 04 Ri# 05 Gp8 06 gp11_smbalert# 07 gp12 08 gp13 09 gp25 10 gp27 11 gp28 When this field is all ‘0’, SV Probe Mode is not selected and the probe mode pins are mapped according to the USB 2.0 EHC PROBEMODE_SEL defined in the D29:F7:offset E0h, bits[4:0]. Any other setting of these bits will select the SV Probe Mode, regardless of the Probe Mode Enable bit (Bus n: Device 8, Function 0, Offset F0h, Bit 0). See the MAS for specific internal signals selected.

21.8.1.5 GPI_ROUT – GPI Routing Control Register (PM – D31:F0)

Offset Address:	B8h – BBh	Attribute:	R/W
Default Value:	0000h	Size:	32-bit
Lockable:	No	Power Well:	Resume

Bit	Description
31:02	**GPI[15] through GPI[1]:** See bits 1:0 for description.
01:00	If the corresponding GPIO is implemented and is set to an input, a ‘1’ in the GP_LVL bit can be routed to cause an SMI# or SCI. If the GPIO is not set to an input, this field has no effect. • 00 – No effect (or GPIO unimplemented) • 01 – SMI# (if corresponding ALT_GPI_SMI_EN bit also set) • 10 – SCI (if corresponding GPE0_EN bit also set) • 11 – Reserved If the system is in an S1-S5 state and if the GPE0_EN bit is also set, then the GPI can cause a Wake event, even if the GPI is NOT routed to cause an SMI# or SCI. Exception: If the system is in S5 state due to a powerbutton override, then the GPIs will not cause wake events. **NOTE:** Core well GPIs are not capable of waking the system from sleep states where the core well is not powered.

Note: GPIOs that are not implemented will not have the corresponding bits implemented in this register.



21.8.2 Power Management I/O Registers

Table 21-10 shows the registers associated with ACPI and Legacy power management support. These registers are enabled in the PCI Device 31: Function 0 space (PM_IO_EN), and can be moved to any I/O location (128-byte aligned). The registers are defined to be compliant with the ACPI 2.0 specification, and use the same bit names.

Note: All reserved bits and registers will always return 0 when read, and will have no effect when written.

Table 21-10. ACPI and Legacy I/O Register Map

PMBASE+ Offset	Mnemonic	Register Name	ACPI Pointer	Default	Type
00–01h	PM1_STS	PM1 Status	PM1a_EVT_BLK	0000h	R/WC
02–03h	PM1_EN	PM1 Enable	PM1a_EVT_BLK+2	0000h	R/W
04–07h	PM1_CNT	PM1 Control	PM1a_CNT_BLK	00000000h	R/W, WO
08–0Bh	PM1_TMR	PM1 Timer	PMTMR_BLK	00000000h	RO
0C–0Fh	–	Reserved	–	–	–
10h–13h	PROC_CNT	Processor Control	P_BLK	00000000h	R/W, RO, WO
14h	LV2	Level 2	P_BLK+4	00h	RO
15h–16h	–	Reserved	–	–	–
17–1Fh	–	Reserved	–	–	–
20h	–	Reserved	–	–	–
28–2Bh	GPE0_STS	General Purpose Event 0 Status	GPE0_BLK	00000000h	R/W, R/WC
2C–2Fh	GPE0_EN	General Purpose Event 0 Enables	GPE0_BLK+4	00000000h	R/W
30–33h	SMI_EN	SMI# Control and Enable		0000h	R/W, WO, R/W (special)
34–37h	SMI_STS	SMI Status		0000h	R/WC, RO
38–39h	ALT_GP_SMI_EN	Alternate GPI SMI Enable		0000h	R/W
3A–3Bh	ALT_GP_SMI_STS	Alternate GPI SMI Status		0000h	R/WC
3C–43h	–	Reserved	–	–	–
44–45h	DEVACT_STS	Device Activity Status		0000h	R/WC
46h–4Fh	–	Reserved			
50h	–	Reserved			
51h–5Fh	–	Reserved	–	–	–
54h–57h	C3_RES	C3-Residency Register	–	00h	RO
60h–7Fh	–	Reserved for TCO	–	–	–

21.8.2.1 PM1_STS – Power Management 1 Status Register

I/O Address:	PMBASE + 00h (*ACPI PM1a_EVT_BLK*)	Attribute:	R/WC
Default Value:	0000h	Size:	16-bit
Lockable:	No	Usage:	ACPI or Legacy
Power Well:	Bits 0–7: Core, Bits 8–15: Resume, except Bit 11 in RTC		

If bit 10 or 8 in this register is set, and the corresponding _EN bit is set in the PM1_EN register, then the Intel® 631xESB/632xESB I/O Controller Hub will generate a Wake Event. Once back in an S0 state (or if already in an S0 state when the event occurs), the Intel® 631xESB/632xESB I/O Controller Hub will also generate an SCI if the SCI_EN bit is set, or an SMI# if the SCI_EN bit is not set.

Note: Bit 5 does not cause an SMI# or a wake event. Bit 0 does not cause a wake event but can cause an SMI# or SCI.

Bit	Description
15	**Wake Status (WAK_STS) –** R/WC. This bit is not affected by hard resets caused by a CF9 write, but is reset by RSMRST#. 0 = Software clears this bit by writing a 1 to it. 1 = Set by hardware when the system is in one of the sleep states (via the SLP_EN bit) and an enabled wake event occurs. Upon setting this bit, the Intel® 631xESB/632xESB I/O Controller Hub will transition the system to the ON state. If the AFTERG3_EN bit is not set and a power failure (such as removed batteries) occurs without the SLP_EN bit set, the system will return to an S0 state when power returns, and the WAK_STS bit will not be set. If the AFTERG3_EN bit is set and a power failure occurs without the SLP_EN bit having been set, the system will go into an S5 state when power returns, and a subsequent wake event will cause the WAK_STS bit to be set. Note that any subsequent wake event would have to be caused by either a Power Button press, or an enabled wake event that was preserved through the power failure (enable bit in the RTC well).
14	Reserved
13:12	Reserved
11	**Power Button Override Status (PRBTNOR_STS) –** R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = This bit is set any time a Power Button Override occurs (Intel® 631xESB/632xESB I/O Controller Hub, the power button is pressed for at least 4 consecutive seconds), or due to the corresponding bit in the SMBus slave message. The power button override causes an unconditional transition to the S5 state, as well as sets the AFTERG# bit. The BIOS or SCI handler clears this bit by writing a 1 to it. This bit is not affected by hard resets via CF9h writes, and is not reset by RSMRST#. Thus, this bit is preserved through power failures.
10	**RTC Status (RTC_STS) –** R/WC. This bit is not affected by hard resets caused by a CF9 write, but is reset by RSMRST#. 0 = Software clears this bit by writing a 1 to it. 1 = Set by hardware when the RTC generates an alarm (assertion of the IRQ8# signal). Additionally if the RTC_EN bit (PMBASE + 02h, bit 10) is set, the setting of the RTC_STS bit will generate a wake event.
9	Reserved
8	**Power Button Status (PWRBTN__STS) –** R/WC. This bit is not affected by hard resets caused by a CF9 write. 0 = If the PWRBTN# signal is held low for more than 4 seconds, the hardware clears the PWRBTN_STS bit, sets the PWRBTNOR_STS bit, and the system transitions to the S5 state with only PWRBTN# enabled as a wake event. This bit can be cleared by software by writing a one to the bit position. 1 = This bit is set by hardware when the PWRBTN# signal is asserted Low, independent of any other enable bit. In the S0 state, while PWRBTN_EN and PWRBTN_STS are both set, an SCI (or SMI# if SCI_EN is not set) will be generated. In any sleeping state S1–S5, while PWRBTN_EN (PMBASE + 02h, bit 8) and PWRBTN_STS are both set, a wake event is generated. ***Note:*** If the PWRBTN_STS bit is cleared by software while the PWRBTN# signal is sell asserted, this will not cause the PWRBN_STS bit to be set. The PWRBTN# signal must go inactive and active again to set the PWRBTN_STS bit.
7:6	Reserved
5	**Global Status (GBL _STS) –** R/WC. 0 = The SCI handler should then clear this bit by writing a 1 to the bit location. 1 = Set when an SCI is generated due to BIOS wanting the attention of the SCI handler. BIOS has a corresponding bit, BIOS_RLS, which will cause an SCI and set this bit.
4:1	Reserved
0	**Timer Overflow Status (TMROF_STS) –** R/WC. 0 = The SCI or SMI# handler clears this bit by writing a 1 to the bit location. 1 = This bit gets set any time bit 22 of the 24-bit timer goes high (bits are numbered from 0 to 23). This will occur every 2.3435 seconds. When the TMROF_EN bit (PMBASE + 02h, bit 0) is set, then the setting of the TMROF_STS bit will additionally generate an SCI or SMI# (depending on the SCI_EN).

21.8.2.2 PM1_EN – Power Management 1 Enable Register

I/O Address:	PMBASE + 02h (*ACPI PM1a_EVT_BLK + 2*)	Attribute:	R/W
Default Value:	0000h	Size:	16-bit
Lockable:	No	Usage:	ACPI or Legacy
Power Well:	Bits 0–7: Core, Bits 8–9, 11–15: Resume, Bit 10: RTC		

Bit	Description
15	Reserved
14	Reserved
13:11	Reserved
10	**RTC Event Enable (RTC_EN) –** R/W. This bit is in the RTC well to allow an RTC event to wake after a power failure. This bit is not cleared by any reset other than RTCRST# or a Power Button Override event. 0 = No SCI (or SMI#) or wake event is generated then RTC_STS (PMBASE + 00h, bit 10) goes active. 1 = An SCI (or SMI#) or wake event will occur when this bit is set and the RTC_STS bit goes active.
9	Reserved.
8	**Power Button Enable (PWRBTN_EN) –** R/W. This bit is used to enable the setting of the PWRBTN_STS bit to generate a power management event (SMI#, SCI). PWRBTN_EN has no effect on the PWRBTN_STS bit (PMBASE + 00h, bit 8) being set by the assertion of the power button. The Power Button is always enabled as a Wake event. 0 = Disable. 1 = Enable.
7:6	Reserved.
5	**Global Enable (GBL_EN) –** R/W. When both the GBL_EN and the GBL_STS bit (PMBASE + 00h, bit 5) are set, an SCI is raised. 0 = Disable. 1 = Enable SCI on GBL_STS going active.
4:1	Reserved.
0	**Timer Overflow Interrupt Enable (TMROF_EN) –** R/W. Works in conjunction with the SCI_EN bit (PMBASE + 04h, bit 0) as described below: TMROF_ENSCI_ENEffect when TMROF_STS is set 0 x No SMI# or SCI 1 0 SMI# 1 1 SCI

21.8.2.3 PM1_CNT – Power Management 1 Control

I/O Address: PMBASE + 04h (*ACPI PM1a_CNT_BLK*)
Default Value: 0000h
Lockable: No
Power Well: Bits 0–7: Core, Bits 8–12: RTC, Bits 13–15: Resume
Attribute: R/W, WO
Size: 32-bit
Usage: ACPI or Legacy

Bit	Description
31:14	Reserved.
13	**Sleep Enable (SLP_EN) –** WO. Setting this bit causes the system to sequence into the Sleep state defined by the SLP_TYP field.
12:10	**Sleep Type (SLP_TYP) –** R/W. This 3-bit field defines the type of Sleep the system should enter when the SLP_EN bit is set to 1. These bits are only reset by RTCRST#. 000 = ON: Typically maps to S0 state. 001 = asserts STPCLK#. Puts processor in Stop-Grant state. Optional to assert CPUSLP# to put processor in sleep state: Typically maps to S1 state. 010 = Reserved 011 = Reserved 100 = Reserved 101 = Suspend-To-RAM. Assert SLP_S3#: Typically maps to S3 state. 110 = Suspend-To-Disk. Assert SLP_S3#, and SLP_S4#: Typically maps to S4 state. 111 = Soft Off. Assert SLP_S3#, SLP_S4#, and SLP_S5#: Typically maps to S5 state.
9:3	Reserved.
2	**Global Release (GBL_RLS) –** WO. 0 = This bit always reads as 0. 1 = ACPI software writes a 1 to this bit to raise an event to the BIOS. BIOS software has a corresponding enable and status bits to control its ability to receive ACPI events.
1	Reserved
0	**SCI Enable (SCI_EN) –** R/W. Selects the SCI interrupt or the SMI# interrupt for various events including the bits in the PM1_STS register (bit 10, 8, 0), and bits in GPE0_STS. 0 = These events will generate an SMI#. 1 = These events will generate an SCI.

21.8.2.4 PM1_TMR – Power Management 1 Timer Register

I/O Address: PMBASE + 08h (*ACPI PMTMR_BLK*)
Default Value: xx000000h
Lockable: No
Power Well: Core
Attribute: RO
Size: 32-bit
Usage: ACPI

Bit	Description
31:24	Reserved
23:0	**Timer Value (TMR_VAL) –** RO. Returns the running count of the PM timer. This counter runs off a 3.579545 MHz clock (14.31818 MHz divided by 4). It is reset to 0 during a PCI reset, and then continues counting as long as the system is in the S0 state. After an S1 state, the counter will not be reset (it will continue counting from the last value in S0 state. Anytime bit 22 of the timer goes HIGH to LOW (bits referenced from 0 to 23), the TMROF_STS bit (PMBASE + 00h, bit 0) is set. The High-to-Low transition will occur every 2.3435 seconds. If the TMROF_EN bit (PMBASE + 02h, bit 0) is set, an SCI interrupt is also generated.

21.8.2.5 PROC_CNT – Processor Control Register

I/O Address: PMBASE + 10h (*ACPI P_BLK*)
Default Value: 00000000h
Lockable: No (bits 7:5 are write once)
Power Well: Core
Attribute: R/W, RO, WO
Size: 32-bit
Usage: ACPI or Legacy

Bit	Description
31:18	Reserved
17	**Throttle Status (THTL_STS) –** RO. 0 = No clock throttling is occurring (maximum processor performance). 1 = Indicates that the clock state machine is throttling the CPU performance. This could be due to the THT_EN bit or the FORCE_THTL bit being set.
16:9	Reserved
8	**Force Thermal Throttling (FORCE_THTL) –** R/W. Software can set this bit to force the thermal throttling function. 0 = No forced throttling. 1 = Throttling at the duty cycle specified in THRM_DTY starts immediately, and no SMI# is generated.
7:5	**THRM_DTY –** WO. This write-once field determines the duty cycle of the throttling when the FORCE_THTL bit is set. The duty cycle indicates the approximate percentage of time the STPCLK# signal is asserted while in the throttle mode. The STPCLK# throttle period is 1024 PCICLKs. Note that the throttling only occurs if the system is in the C0 state. If in the C2, C3, or C4 state, no throttling occurs. Once the THRM_DTY field is written, any subsequent writes will have no effect until PLTRST# goes active. THRM_DTY Throttle ModePCI Clocks 000 50% (Default)512 001 87.5%896 010 75.0%768 011 62.5%640 100 50%512 101 37.5%384 110 25%256 111 12.5%128
4	**THTL_EN –** R/W. When set and the system is in a C0 state, it enables a processor-controlled STPCLK# throttling. The duty cycle is selected in the THTL_DTY field. 0 = Disable 1 = Enable
3:1	**THTL_DTY –** R/W. This field determines the duty cycle of the throttling when the THTL_EN bit is set. The duty cycle indicates the approximate percentage of time the STPCLK# signal is asserted (low) while in the throttle mode. The STPCLK# throttle period is 1024 PCICLKs. **THTL_DTY Throttle ModePCI Clocks** 000 50% (Default)512 001 87.5%896 010 75.0%768 011 62.5%640 100 50%512 101 37.5%384 110 25%256 111 12.5%128
0	Reserved

21.8.2.6 LV2 – Level 2 Register

I/O Address:	PMBASE + 14h (*ACPI P_BLK+4*)	Attribute:	RO
Default Value:	00h	Size:	8-bit
Lockable:	No	Usage:	ACPI or Legacy
Power Well:	Core		

Bit	Description
7:0	Reads to this register return all 0's, writes to this register have no effect. Reads to this register generate a "enter a level 2 power state" (C2) to the clock control logic. This will cause the STPCLK# signal to go active, and stay active until a break event occurs. Throttling (due either to THTL_EN or FORCE_THTL) will be ignored.

Note: This register should not be used by Intel Itanium processors or systems with more than 1 logical CPU, unless appropriate semaphoring software has been put in place to ensure that all threads/CPUs are ready for the C2 state when the read to this register occurs

21.8.2.7 GPE0_STS – General Purpose Event 0 Status Register

I/O Address:	PMBASE + 28h (*ACPI GPE0_BLK*)	Attribute:	R/W, R/WC
Default Value:	00000000h	Size:	32-bit
Lockable:	No	Usage:	ACPI
Power Well:	Resume		

This register is symmetrical to the General Purpose Event 0 Enable Register. Unless indicated otherwise below, if the corresponding _EN bit is set, then when the _STS bit get set, the Intel® 631xESB/632xESB I/O Controller Hub will generate a Wake Event. Once back in an S0 state (or if already in an S0 state when the event occurs), the Intel® 631xESB/632xESB I/O Controller Hub will also generate an SCI if the SCI_EN bit is set, or an SMI# if the SCI_EN bit (PMBASE + 04h, bit 0) is not set. Bits 31:16 are reset by a CF9h write; bits 15:0 are not. All are reset by RSMRST#.

Bit	Description
31:16	**GPIn_STS –** R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = These bits are set any time the corresponding GPIO is set up as an input and the corresponding GPIO signal is high (or low if the corresponding GP_INV bit is set). If the corresponding enable bit is set in the GPE0_EN register, then when the GPI[n]_STS bit is set: • If the system is in an S1–S5 state, the event will also wake the system. • If the system is in an S0 state (or upon waking back to an S0 state), a SCI will be caused depending on the GPI_ROUT bits (D31:F0:B8h, bits 31:30) for the corresponding GPI.
15	Reserved
14	**USB4_STS –** R/W. 0 = Disable. 1 = Set by hardware and can be reset by writing a one to this bit position or a resume-well reset. This bit is set when USB UHCI controller #4 needs to cause a wake. Additionally if the USB4_EN bit is set, the setting of the USB4_STS bit will generate a wake event.
13	**PME_B0_STS** – R/W. This bit will be set to 1 by the Intel® 631xESB/632xESB I/O Controller Hub when any internal device with PCI Power Management capabilities on bus 0 asserts the equivalent of the PME# signal. Additionally, if the PME_B0_EN bit is set, and the system is in an S0 state, then the setting of the PME_B0_STS bit will generate an SCI (or SMI# if SCI_EN is not set). If the PME_B0_STS bit is set, and the system is in an S1–S4 state (or S5 state due to SLP_TYP and SLP_EN), then the setting of the PME_B0_STS bit will generate a wake event, and an SCI (or SMI# if SCI_EN is not set) will be generated. If the system is in an S5 state due to power button override, then the PME_B0_STS bit will not cause a wake event or SCI. The default for this bit is 0. Writing a 1 to this bit position clears this bit.
12	**USB3_STS –** R/W. 0 = Disable. 1 = Set by hardware and can be reset by writing a one to this bit position or a resume-well reset. This bit is set when USB UHCI controller #3 needs to cause a wake. Additionally if the USB3_EN bit is set, the setting of the USB3_STS bit will generate a wake event.

Bit	Description
11	**PME_STS** – R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = Set by hardware when the PME# signal goes active. Additionally, if the PME_EN bit is set, and the system is in an S0 state, then the setting of the PME_STS bit will generate an SCI or SMI# (if SCI_EN is not set). If the PME_EN bit is set, and the system is in an S1–S4 state (or S5 state due to setting SLP_TYP and SLP_EN), then the setting of the PME_STS bit will generate a wake event, and an SCI will be generated. If the system is in an S5 state due to power button override or a power failure, then PME_STS will not cause a wake event or SCI.
10	Reserved
9	**PCI_EXP_STS –** R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = Set by hardware to indicate that: • The PME event message was received on one or more of the PCI Express ports • An Assert PMEGPE message received from the (G)MCH via ESI ***Notes:*** 1. The PCI WAKE# pin and the PCI Express Beacons have no impact on this bit. 2. If the PCI_EXP_STS bit went active due to an Assert PMEGPE message, then a Deassert PMEGPE message must be received prior to the software write in order for the bit to be cleared. 3. If the bit is not cleared and the corresponding PCI_EXP_EN bit is set, the level-triggered SCI will remain active. 4. A race condition exists where the PCI Express device sends another PME message because the PCI Express device was not serviced within the time when it must resend the message. This may result in a spurious interrupt, and this is comprehended and approved by the PCI Express specification. The window for this race condition is approximately 95-105 milliseconds.
8	**RI_STS** – R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = Set by hardware when the RI# input signal goes active.
7	**SMBus Wake Status (SMB_WAK_STS) –** R/WC. The SMBus controller can independently cause an SMI# or SCI, so this bit does not need to do so (unlike the other bits in this register). Software clears this bit by writing a 1 to it. 0 = Wake event Not caused by the Intel® 631xESB/632xESB I/O Controller Hub's SMBus logic. 1 = Set by hardware to indicate that the wake event was caused by the Intel® 631xESB/ 632xESB I/O Controller Hub's SMBus logic.This bit will be set by the WAKE/SMI# command type, even if the system is already awake. The SMI handler should then clear this bit. NOTES: 1. This bit is set by the SMBus slave command 01h (Wake/SMI#) even when the system is in the S0 state. Therefore, to avoid an instant wake on subsequent transitions to sleep states, software must clear this bit after each reception of the Wake/SMI# command or just prior to entering the sleep state. 2. If SMB_WAK_STS is set due to SMBus slave receiving a message, it will be cleared by internal logic when a THRMTRIP# event happens or a Power Button Override event. However, THRMTRIP# or Power Button Override event will not clear SMB_WAK_STS if it is set due to SMBALERT# signal going active. 3. The SMBALERT_STS bit (D31:F3:I/O Offset 00h:Bit 5) should be cleared by software before the SMB_WAK_STS bit is cleared.
6	**TCOSCI_STS** – R/WC. Software clears this bit by writing a 1 to it. 0 = TOC logic did Not cause SCI. 1 = Set by hardware when the TCO logic causes an SCI.
5	**AC97_STS** – R/WC. This bit will be set to 1 when the codecs are attempting to wake the system and the PME events for the codecs are armed for wakeup. A PME is armed by programming the appropriate PMEE bit in the Power Management Control and Status register at bit 8 of offset 54h in each AC'97 function. 0 = Software clears this bit by writing a 1 to it. 1 = Set by hardware when the codecs are attempting to wake the system. The AC97_STS bit gets set only from the following two cases: 1. The PMEE bit for the function is set, and o The AC-link bit clock has been shut and the routed ACZ_SDIN line is high (for audio, if routing is disabled, no wake events are allowed. 2. For modem, if audio routing is disabled, then the wake event is an OR of all ACZ_SDIN lines. If routing is enabled, then the wake event for modem is the remaining non-routed ACZ_SDIN line), or o GPI Status Change Interrupt bit (NABMBAR + 30h, bit 0) is 1. ***Note:*** This bit is not affected by a hard reset caused by a CF9h write. ***Note:*** This bit is also used for Azalia when Intel® 631xESB/632xESB I/O Controller Hub is configured to use the Azalia host controller rather than the AC97 host controller.

Bit	Description
4	**USB2_STS** – R/WC. Software clears this bit by writing a 1 to it. 0 = USB UHCI controller 2 does Not need to cause a wake. 1 = Set by hardware when USB UHCI controller 2 needs to cause a wake. Wake event will be generated if the corresponding USB2_EN bit is set.
3	**USB1_STS** – R/WC. Software clears this bit by writing a 1 to it. 0 = USB UHCI controller 1 does Not need to cause a wake. 1 = Set by hardware when USB UHCI controller 1 needs to cause a wake. Wake event will be generated if the corresponding USB1_EN bit is set.
2	Reserved
1	**HOT_PLUG_STS –** R/WC. 0 = This bit is cleared by writing a 1 to this bit position. 1 = When a PCI Express Hot-Plug event occurs. This will cause an SCI if the HOT_PLUG_EN bit is set in the GEP0_EN register.
0	**Thermal Interrupt Status (THRM_STS) –** R/WC. Software clears this bit by writing a 1 to it. 0 = THRM# signal Not driven active as defined by the THRM_POL bit 1 = Set by hardware anytime the THRM# signal is driven active as defined by the THRM_POL bit. Additionally, if the THRM_EN bit is set, then the setting of the THRM_STS bit will also generate a power management event (SCI or SMI#).

21.8.2.8 GPE0_EN – General Purpose Event 0 Enables Register

I/O Address:	PMBASE + 2Ch (*ACPI GPE0_BLK + 4*)	Attribute:	R/W
Default Value:	00000000h	Size:	32-bit
Lockable:	No	Usage:	ACPI
Power Well:	Bits 0–7, 9, 12, 14–31 Resume, Bits 8, 10–11, 13 RTC		

This register is symmetrical to the General Purpose Event 0 Status Register. All the bits in this register should be cleared to 0 based on a Power Button Override or processor Thermal Trip event. The resume well bits are all cleared by RSMRST#. The RTC sell bits are cleared by RTCRST#.

Bit	Description
31:16	**GPIn_EN** – R/W. These bits enable the corresponding GPI[n]_STS bits being set to cause a SCI, and/or wake event. These bits are cleared by RSMRST#. ***Note:*** Mapping is as follows: bit 31 corresponds to GPI[15]... and bit 16 corresponds to GPI:[0]. Software should not set bits 28:29 corresponding to GPI[12:13].
15	Reserved
14	USB4_EN – R/W. 0 = Disable. 1 = Enable the setting of the USB4_STS bit to generate a wake event. The USB4_STS bit is set anytime USB UHCI controller #4 signals a wake event. Break events are handled via the USB interrupt.
13	**PME_B0_EN –** R/W. 0 = Disable 1 = Enables the setting of the PME_B0_STS bit to generate a wake event and/or an SCI or SMI#. PME_B0_STS can be a wake event from the S1–S4 states, or from S5 (if entered via SLP_TYP and SLP_EN) or power failure, but not Power Button Override. This bit defaults to 0. ***Note:*** It is only cleared by Software or RTCRST#. It is not cleared by CF9h writes.
12	USB3_EN – R/W. 0 = Disable. 1 = Enable the setting of the USB3_STS bit to generate a wake event. The USB3_STS bit is set anytime USB UHCI controller #3 signals a wake event. Break events are handled via the USB interrupt.
11	**PME_EN** – R/W. 0 = Disable. 1 = Enables the setting of the PME_STS to generate a wake event and/or an SCI. PME# can be a wake event from the S1 – S4 state or from S5 (if entered via SLP_EN, but not power button override).

Bit	Description
10	Reserved
9	**PCI_EXP_EN** – R/W. 0 = Disable SCI generation upon PCI_EXP_STS bit being set. 1 = Enables Intel® 631xESB/632xESB I/O Controller Hub to cause an SCI when PCI_EXP_STS bit is set. This is used to allow the PCI Express ports, including the link to the (G)MCH, to cause an SCI due to wake/PME events.
8	**RI_EN** – R/W. The value of this bit will be maintained through a G3 state and is not affected by a hard reset caused by a CF9h write. 0 = Disable. 1 = Enables the setting of the RI_STS to generate a wake event.
7	Reserved
6	**TCOSCI_EN** – R/W. 0 = Disable. 1 = Enables the setting of the TCOSCI_STS to generate an SCI.
5	AC97_EN – R/W. 0 = Disable. 1 = Enables the setting of the AC97_STS to generate a wake event. ***Note:*** This bit is also used for Azalia when the Azalia host controller is enabled rather than the AC97 host controller.
4	**USB2_EN** – R/W. 0 = Disable. 1 = Enables the setting of the USB2_STS to generate a wake event.
3	**USB1_EN** – R/W. 0 = Disable. 1 = Enables the setting of the USB1_STS to generate a wake event.
2	**THRM#_POL** – R/W. This bit controls the polarity of the THRM# pin needed to set the THRM_STS bit. 0 = Low value on the THRM# signal will set the THRM_STS bit. 1 = HIGH value on the THRM# signal will set the THRM_STS bit.
1	**HOT_PLUG_EN –** R/W. 0 = Disables SCI generation upon the HOT_PLUG_STS bit being set. 1 = Enables the Intel® 631xESB/632xESB I/O Controller Hub to cause an SCI when the HOT_PLUG_STS bit is set. This is used to allow the PCI Express ports to cause an SCI due to Hot-Plug events.
0	**THRM_EN** – R/W. 0 = Disable. 1 = Active assertion of the THRM# signal (as defined by the THRM_POL bit) will set the THRM_STS bit and generate a power management event (SCI or SMI).

21.8.2.9 SMI_EN – SMI Control and Enable Register

I/O Address:	PMBASE + 30h	Attribute:	R/W, R/W (special), WO
Default Value:	00000000h	Size:	32 bit
Lockable:	No	Usage:	ACPI or Legacy
Power Well:	Core		

Note: This register is symmetrical to the SMI status register.

Bit	Description
31:19	Reserved
18	**INTEL_USB2_EN** – R/W. 0 = Disable 1 = Enables Intel-Specific USB2 SMI logic to cause SMI#.
17	**LEGACY_USB2_EN** – R/W. 0 = Disable 1 = Enables legacy USB2 logic to cause SMI#.
16:15	Reserved

Bit	Description
14	PERIODIC_EN – R/W. 0 = Disable. 1 = Enables the Intel® 631xESB/632xESB I/O Controller Hub to generate an SMI# when the PERIODIC_STS bit (PMBASE + 34h, bit 14) is set in the SMI_STS register (PMBASE + 34h).
13	TCO_EN – R/W. 0 = Disables TCO logic generating an SMI#. Note that if the NMI2SMI_EN bit is set, SMIs that are caused by re-routed NMIs will not be gated by the TCO_EN bit. Even if the TCO_EN bit is 0, NMIs will still be routed to cause SMIs. 1 = Enables the TCO logic to generate SMI#. ***Note:*** This bit cannot be written once the TCO_LOCK bit is set.
12	Reserved
11	**MCSMI_ENMicrocontroller SMI Enable (MCSMI_EN) –** R/W. 0 = Disable. 1 = Enables Intel® 631xESB/632xESB I/O Controller Hub to trap accesses to the microcontroller range (62h or 66h) and generate an SMI#. Note that “trapped’ cycles will be claimed by the Intel® 631xESB/632xESB I/O Controller Hub on PCI, but not forwarded to LPC.
10:8	Reserved
7	**BIOS Release (BIOS_RLS) –** WO. 0 = This bit will always return 0 on reads. Writes of 0 to this bit have no effect. 1 = Enables the generation of an SCI interrupt for ACPI software when a one is written to this bit position by BIOS software. ***Note:*** GBL_STS being set will cause an SCI, even if the SCI_EN bit is not set. Software must take great care not to set the BIOS_RLS bit (which causes GBL_STS to be set) if the SCI handler is not in place.
6	Software SMI# Timer Enable (SWSMI_TMR_EN) – R/W. 0 = Disable. Clearing the SWSMI_TMR_EN bit before the timer expires will reset the timer and the SMI# will not be generated. 1 = Starts Software SMI# Timer. When the SWSMI timer expires (the timeout period depends upon the SWSMI_RATE_SEL bit setting), SWSMI_TMR_STS is set and an SMI# is generated. SWSMI_TMR_EN stays set until cleared by software.
5	Reserved.
4	SLP_SMI_EN – R/W. 0 = Disables the generation of SMI# on SLP_EN. Note that this bit must be 0 before the software attempts to transition the system into a sleep state by writing a 1 to the SLP_EN bit. 1 = A write of 1 to the SLP_EN bit (bit 13 in PM1_CNT register) will generate an SMI#, and the system will not transition to the sleep state based on that write to the SLP_EN bit.
3	LEGACY_USB_EN – R/W. 0 = Disable. 1 = Enables legacy USB circuit to cause SMI#.
2	BIOS_EN – R/W. 0 = Disable. 1 = Enables the generation of SMI# when ACPI software writes a 1 to the GBL_RLS bit.
1	**End of SMI (EOS) –** R/W (special). This bit controls the arbitration of the SMI signal to the processor. This bit must be set for the Intel® 631xESB/632xESB I/O Controller Hub to assert SMI# low to the processor after SMI# has been asserted previously. 0 = Once the Intel® 631xESB/632xESB I/O Controller Hub asserts SMI# low, the EOS bit is automatically cleared. 1 = When this bit is set to 1, SMI# signal will be deasserted for 4 PCI clocks before its assertion. In the SMI handler, the processor should clear all pending SMIs (by servicing them and then clearing their respective status bits), set the EOS bit, and exit SMM. This will allow the SMI arbiter to re-assert SMI upon detection of an SMI event and the setting of a SMI status bit. ***Note:*** Intel® 631xESB/632xESB I/O Controller Hub is able to generate 1st SMI after reset even though EOS bit is not set. Subsequent SMI require EOS bit is set.
0	GBL_SMI_EN – R/W. 0 = No SMI# will be generated by Intel® 631xESB/632xESB I/O Controller Hub. This bit is reset by a PCI reset event. 1 = Enables the generation of SMI# in the system upon any enabled SMI event. ***Note:*** When the SMI_LOCK bit is set, this bit cannot be changed.

21.8.2.10 SMI_STS – SMI Status Register

I/O Address:	PMBASE + 34h	Attribute:	RO, R/WC
Default Value:	00000000h	Size:	32-bit
Lockable:	No	Usage:	ACPI or Legacy
Power Well:	Core		

Note: If the corresponding _EN bit is set when the _STS bit is set, the Intel® 631xESB/632xESB I/O Controller Hub will cause an SMI# (except bits 8–10 and 12, which do not need enable bits since they are logic ORs of other registers that have enable bits). The Intel® 631xESB/632xESB I/O Controller Hub uses the same GPE0_EN register (I/O address: PMBase+2Ch) to enable/disable both SMI and ACPI SCI general purpose input events. ACPI OS assumes that it owns the entire GPE0_EN register per ACPI spec. Problems arise when some of the general-purpose inputs are enabled as SMI by BIOS, and some of the general purpose inputs are enabled for SCI. In this case ACPI OS turns off the enabled bit for any GPIx input signals that are not indicated as SCI general-purpose events at boot, and exit from sleeping states. BIOS should define a dummy control method which prevents the ACPI OS from clearing the SMI GPE0_EN bits.

Bit	Description
31:21	Reserved
20	**PCI_EXP_SMI_STS –** RO. PCI Express SMI event occurred. This could be due to a PCI Express PME event or Hot-Plug Event.
19	Reserved
18	**INTEL_USB2_STS –** RO. This non-sticky read-only bit is a logical OR of each of the SMI status bits in the Intel-Specific USB2 SMI Status Register ANDed with the corresponding enable bits. This bit will not be active if the enable bits are not set. Writes to this bit will have no effect.
17	**LEGACY_USB2_STS –** RO. This non-sticky read-only bit is a logical OR of each of the SMI status bits in the USB2 Legacy Support Register ANDed with the corresponding enable bits. This bit will not be active if the enable bits are not set. Writes to this bit will have no effect.
16	**SMBus SMI Status (SMBUS_SMI_STS) –** R/WC. Software clears this bit by writing a 1 to it. 0 = This bit is set from the 64 kHz clock domain used by the SMBus. Software must wait at least 15.63 us after the initial assertion of this bit before clearing it. 1 = Indicates that the SMI# was caused by: 1. The SMBus Slave receiving a message that an SMI# should be caused, or 2. The SMBALERT# signal goes active and the SMB_SMI_EN bit is set and the SMBALERT_DIS bit is cleared, or 3. The SMBus Slave receiving a Host Notify message and the HOST_NOTIFY_INTREN and the SMB_SMI_EN bits are set, or 4. The Intel® 631xESB/632xESB I/O Controller Hub detecting the SMLINK_SLAVE_SMI command while in the S0 state.
15	**SERIRQ_SMI_STS** – RO. 0 = SMI# was not caused by the SERIRQ decoder. 1 = Indicates that the SMI# was caused by the SERIRQ decoder. ***Note:*** This is not a sticky bit
14	PERIODIC_STS – R/WC. Software clears this bit by writing a 1 to it. 0 = Software clears this bit by writing a 1 to it. 1 = This bit is set at the rate determined by the PER_SMI_SEL bits. If the PERIODIC_EN bit (PMBASE + 30h, bit 14) is also set, the Intel® 631xESB/632xESB I/O Controller Hub generates an SMI#.
13	TCO_STS – RO. Software clears this bit by writing a 1 to it. 0 = SMI# not caused by TCO logic. 1 = Indicates the SMI# was caused by the TCO logic. Note that this is not a wake event.
12	**Device Monitor Status (DEVMON_STS) –** RO. 0 = SMI# not caused by Device Monitor. 1 = Set if bit 0 of the DEVACT_STS register (PMBASE + 44h) is set. The bit is not sticky, so writes to this bit will have no effect.

Bit	Description
11	**Microcontroller SMI# Status (MCSMI_STS) –** R/WC. Software clears this bit by writing a 1 to it. 0 = Indicates that there has been no access to the power management microcontroller range (62h or 66h). 1 = Set if there has been an access to the power management microcontroller range (62h or 66h). If this bit is set, and the MCSMI_EN bit is also set, the Intel® 631xESB/632xESB I/O Controller Hub will generate an SMI#.
10	**GPE0_STS** – RO. This bit is a logical OR of the bits in the ALT_GP_SMI_STS register that are also set up to cause an SMI# (as indicated by the GPI_ROUT registers) and have the corresponding bit set in the ALT_GP_SMI_EN register. Bits that are not routed to cause an SMI# will have no effect on this bit. 0 = SMI# was not generated by a GPI assertion. 1 = SMI# was generated by a GPI assertion.
9	**GPE0_STS** – RO. This bit is a logical OR of the bits 14:10, 8:2, and 0 in the GPE0_STS register (PMBASE + 28h) that also have the corresponding bit set in the GPE0_EN register (PMBASE + 2Ch). 0 = SMI# was not generated by a GPE0 event. 1 = SMI# was generated by a GPE0 event.
8	**PM1_STS_REG** – RO. This is an ORs of the bits in the ACPI PM1 Status Register (offset PMBASE+00h) that can cause an SMI#. 0 = SMI# was not generated by a PM1_STS event. 1 = SMI# was generated by a PM1_STS event.
7	Reserved
6	**SWSMI_TMR_STS** – R/WC. Software clears this bit by writing a 1 to it. 0 = Software SMI# Timer has Not expired. 1 = Set by the hardware when the Software SMI# Timer expires.
5	Reserved
4	SLP_SMI_STS – R/WC. Software clears this bit by writing a 1 to the bit location. 0 = No SMI# caused by write of 1 to SLP_EN bit when SLP_SMI_EN bit is also set. 1 = Indicates an SMI# was caused by a write of 1 to SLP_EN bit when SLP_SMI_EN bit is also set.
3	**LEGACY_USB_STS** – RO. This bit is a logical OR of each of the SMI status bits in the USB Legacy Keyboard/Mouse Control Registers ANDed with the corresponding enable bits. This bit will not be active if the enable bits are not set. 0 = SMI# was not generated by USB Legacy event. 1 = SMI# was generated by USB Legacy event.
2	**BIOS_STS** – R/WC. 0 = No SMI# generated due to ACPI software requesting attention. 1 = SMI# was generated due to ACPI software requesting attention (writing a 1 to the GBL_RLS bit with the BIOS_EN bit set).
1:0	Reserved

21.8.2.11 ALT_GP_SMI_EN – Alternate GPI SMI Enable Register

I/O Address:	PMBASE +38h	Attribute:	R/W
Default Value:	0000h	Size:	16-bit
Lockable:	No	Usage:	ACPI or Legacy
Power Well:	Resume		

Bit	Description
15:0	**Alternate GPI SMI Enable –** R/W. These bits are used to enable the corresponding GPIO to cause an SMI#. For these bits to have any effect, the following must be true. • The corresponding bit in the ALT_GP_SMI_EN register is set. • The corresponding GPI must be routed in the GPI_ROUT register to cause an SMI. • The corresponding GPIO must be implemented.

21.8.2.12 ALT_GP_SMI_STS – Alternate GPI SMI Status Register

I/O Address:	PMBASE +3Ah	Attribute:	R/WC
Default Value:	0000h	Size:	16-bit
Lockable:	No	Usage:	ACPI or Legacy
Power Well:	Resume		

Bit	Description
15:0	**Alternate GPI SMI Status** – R/WC. These bits report the status of the corresponding GPIs. 0 = Inactive. Software clears this bit by writing a 1 to it. 1 = Active These bits are sticky. If the following conditions are true, then an SMI# will be generated and the GPE0_STS bit set: • The corresponding bit in the ALT_GPI_SMI_EN register (PMBASE + 38h) is set • The corresponding GPI must be routed in the GPI_ROUT register to cause an SMI. • The corresponding GPIO must be implemented. All bits are in the resume well. Default for these bits is dependent on the state of the GPI pins.

21.8.2.13 DEVACT_STS – Device Activity Status Register

I/O Address:	PMBASE +44h	Attribute:	R/WC
Default Value:	0000h	Size:	16-bit
Lockable:	No	Usage:	Legacy Only
Power Well:	Core		

Each bit indicates if an access has occurred to the corresponding device's trap range, or for bits 6:9 if the corresponding PCI interrupt is active. This register is used in conjunction with the Periodic SMI# timer to detect any system activity for legacy power management. The periodic SMI# timer indicates if it is the right time to read the DEVACT_STS register (PMBASE + 44h).

Note: Software clears bits that are set in this register by writing a 1 to the bit position.

Bit	Description
15:13	Reserved
12	**KBC_ACT_STS** – R/WC. KBC (60/64h). 0 = Indicates that there has been no access to this device's I/O range. 1 = This device's I/O range has been accessed. Clear this bit by writing a 1 to the bit location.
11:10	Reserved
9	PIRQDH_ACT_STS – R/WC. PIRQ[D or H]. 0 = The corresponding PCI interrupts have not been active. 1 = At least one of the corresponding PCI interrupts has been active. Clear this bit by writing a 1 to the bit location.
8	PIRQCG_ACT_STS – R/WC. PIRQ[C or G]. 0 = The corresponding PCI interrupts have not been active. 1 = At least one of the corresponding PCI interrupts has been active. Clear this bit by writing a 1 to the bit location.
7	PIRQBF_ACT_STS – R/WC. PIRQ[B or F]. 0 = The corresponding PCI interrupts have not been active. 1 = At least one of the corresponding PCI interrupts has been active. Clear this bit by writing a 1 to the bit location.

Bit	Description
6	PIRQAE_ACT_STS – R/WC. PIRQ[A or E]. 0 = The corresponding PCI interrupts have not been active. 1 = At least one of the corresponding PCI interrupts has been active. Clear this bit by writing a 1 to the bit location.
5:1	Reserved
0	**IDE_ACT_STS –** R/WC. IDE Primary Drive 0 and Drive 1. 0 = Indicates that there has been no access to this device's I/O range. 1 = This device's I/O range has been accessed. The enable bit is in the ATC register (D31:F1:Offset C0h). Clear this bit by writing a 1 to the bit location.

21.8.2.14 C3_RES – C3 Residency Register

I/O Address:	PMBASE +54h	Attribute:	RO
Default Value	00000000h	Size:	32-bit
Lockable:	No	Usage:	ACPI/Legacy
Power Well:	Core		

Bit	Description
31:00	Reserved

21.9 System Management TCO Registers (D31:F0)

The TCO logic is accessed via registers mapped to the PCI configuration space (Device 31:Function 0) and the system I/O space. For TCO PCI Configuration registers, see LPC Device 31:Function 0 PCI Configuration registers.

21.9.1 TCO Register I/O Map

The TCO I/O registers reside in a 32-byte range pointed to by a TCOBASE value, which is, PMBASE + 60h in the PCI config space. The following table shows the mapping of the registers within that 32-byte range. Each register is described in the following sections.

Table 21-11. TCO I/O Register Address Map (Sheet 1 of 2)

TCOBASE + Offset	Mnemonic	Register Name	Default	Type
00h–01h	TCO_RLD	TCO Timer Reload and Current Value	0000h	R/W
02h	TCO_DAT_IN	TCO Data In	00h	R/W
03h	TCO_DAT_OUT	TCO Data Out	00h	R/W
04h–05h	TCO1_STS	TCO1 Status	0000h	R/WC, RO
06h–07h	TCO2_STS	TCO2 Status	0000h	R/W, R/WC
08h–09h	TCO1_CNT	TCO1 Control	0000h	R/W, R/W (special), R/WC
0Ah–0Bh	TCO2_CNT	TCO2 Control	0008h	R/W
0Ch–0Dh	TCO_MESSAGE1, TCO_MESSAGE2	TCO Message 1 and 2	00h	R/W
0Eh	TCO_WDCNT	Watchdog Control Register	00h	R/W
0Fh	–	Reserved	–	–
10h	SW_IRQ_GEN	Software IRQ Generation Register	11h	R/W

Table 21-11. TCO I/O Register Address Map (Sheet 2 of 2)

TCOBASE + Offset	Mnemonic	Register Name	Default	Type
11h	–	Reserved	–	–
12h–13h	TCO_TMR	TCO Timer Initial Value	04h	R/W
14h–1Fh	–	Reserved	–	–

21.9.2 TCO_RLD – TCO Timer Reload and Current Value Register

I/O Address: TCOBASE +00h
Default Value: 0000h
Lockable: No
Attribute: R/W
Size: 16-bit
Power Well: Core

Bit	Description
15:10	Reserved
9:0	**TCO Timer Value** – R/W. Reading this register will return the current count of the TCO timer. Writing any value to this register will reload the timer to prevent the timeout.

21.9.3 TCO_DAT_IN – TCO Data In Register

I/O Address: TCOBASE +02h
Default Value: 00h
Lockable: No
Attribute: R/W
Size: 8-bit
Power Well: Core

Bit	Description
7:0	**TCO Data In Value** – R/W. This data register field is used for passing commands from the OS to the SMI handler. Writes to this register will cause an SMI and set the SW_TCO_SMI bit in the TCO1_STS register (D31:F0:04h).

21.9.4 TCO_DAT_OUT – TCO Data Out Register

I/O Address: TCOBASE +03h
Default Value: 00h
Lockable: No
Attribute: R/W
Size: 8-bit
Power Well: Core

Bit	Description
7:0	**TCO Data Out Value** – R/W. This data register field is used for passing commands from the SMI handler to the OS. Writes to this register will set the TCO_INT_STS bit in the TCO_STS register. It will also cause an interrupt, as selected by the TCO_INT_SEL bits.

21.9.5 TCO1_STS – TCO1 Status Register

I/O Address: TCOBASE +04h
Default Value: 0000h
Lockable: No
Attribute: R/WC, RO
Size: 16-bit
Power Well: Core (Except bit 7, in RTC)

Bit	Description
15:13	Reserved
12	**ESISERR_STS** – R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = Intel® 631xESB/632xESB I/O Controller Hub received a ESI special cycle message via ESI indicating that it wants to cause an SERR#. The software must read the (G)MCH to determine the reason for the SERR#.
11	Reserved

Bit	Description
10	**ESISMI_STS** – R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = Intel® 631xESB/632xESB I/O Controller Hub received a ESI special cycle message via ESI indicating that it wants to cause an SMI. The software must read the (G)MCH to determine the reason for the SMI.
9	**ESISCI_STS** – R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = Intel® 631xESB/632xESB I/O Controller Hub received a ESI special cycle message via ESI indicating that it wants to cause an SCI. The software must read the (G)MCH to determine the reason for the SCI.
8	**BIOSWR_STS** – R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = Intel® 631xESB/632xESB I/O Controller Hub sets this bit and generates and SMI# to indicate an illegal attempt to write to the BIOS. This occurs when either: a) The BIOSWP bit is changed from 0 to 1 and the BLD bit is also set, or b) any write is attempted to the BIOS and the BIOSWP bit is also set. ***Note:*** On write cycles attempted to the 4 MB lower alias to the BIOS space, the BIOSWR_STS will not be set.
7	NEWCENTURY_STS – R/WC. This bit is in the RTC well. 0 = Cleared by writing a 1 to the bit position or by RTCRST# going active. 1 = This bit is set when the Year byte (RTC I/O space, index offset 09h) rolls over from 99 to 00. Setting this bit will cause an SMI# (but not a wake event). ***Note:*** The NEWCENTURY_STS bit is not valid when the RTC battery is first installed (or when RTC power has not been maintained). Software can determine if RTC power has not been maintained by checking the RTC_PWR_STS bit (D31:F0:A4h, bit 2), or by other means (such as a checksum on RTC RAM). If RTC power is determined to have not been maintained, BIOS should set the time to a legal value and then clear the NEWCENTURY_STS bit. The NEWCENTURY_STS bit may take up to 3 RTC clocks for the bit to be cleared after a 1 is written to the bit to clear it. After writing a 1 to this bit, software should not exit the SMI handler until verifying that the bit has actually been cleared. This will ensure that the SMI is not re-entered.
6:4	Reserved
3	**TIMEOUT** – R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = Set by Intel® 631xESB/632xESB I/O Controller Hub to indicate that the SMI was caused by the TCO timer reaching 0.
2	**TCO_INT_STS** – R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = SMI handler caused the interrupt by writing to the TCO_DAT_OUT register (TCOBASE + 03h).
1	**SW_TCO_SMI** – R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = Software caused an SMI# by writing to the TCO_DAT_IN register (TCOBASE + 02h).
0	**NMI2SMI_STS –** RO. 0 = Cleared by clearing the associated NMI status bit. 1 = Set by the Intel® 631xESB/632xESB I/O Controller Hub when an SMI# occurs because an event occurred that would otherwise have caused an NMI (because NMI2SMI_EN is set).

21.9.6 TCO2_STS – TCO2 Status Register

I/O Address:	TCOBASE +06h	Attribute:	R/W, R/WC
Default Value:	0000h	Size:	16-bit
Lockable:	No	Power Well:	Resume (Except Bit 0, in RTC)

Bit	Description
15:5	Reserved
4	**SMLink Slave SMI Status (SMLINK_SLV_SMI_STS)** – R/WC. Allow the software to go directly into pre-determined sleep state. This avoids race conditions. Software clears this bit by writing a 1 to it. 0 = The bit is reset by RSMRST#, but not due to the PCI Reset associated with exit from S3–S5 states. 1 = Intel® 631xESB/632xESB I/O Controller Hub sets this bit to 1 when it receives the SMI message on the SMLink's Slave Interface.
3	Reserved
2	**BOOT_STS – R/WC.** 0 = Cleared by Intel® 631xESB/632xESB I/O Controller Hub based on RSMRST# or by software writing a 1 to this bit. Note that software should first clear the SECOND_TO_STS bit before writing a 1 to clear the BOOT_STS bit. 1 = Set to 1 when the SECOND_TO_STS bit goes from 0 to 1 and the processor has not fetched the first instruction. If rebooting due to a second TCO timer timeout, and if the BOOT_STS bit is set, the Intel® 631xESB/632xESB I/O Controller Hub will reboot using the 'safe' multiplier (1111). This allows the system to recover from a processor frequency multiplier that is too high, and allows the BIOS to check the BOOT_STS bit at boot. If the bit is set and the frequency multiplier is 1111, then the BIOS knows that the processor has been programmed to an illegal multiplier.
1	**SECOND_TO_STS –** R/WC. 0 = Software clears this bit by writing a 1 to it, or by a RSMRST#. 1 = Intel® 631xESB/632xESB I/O Controller Hub sets this bit to 1 to indicate that the TIMEOUT bit had been (or is currently) set and a second timeout occurred before the TCO_RLD register was written. If this bit is set and the NO_REBOOT config bit is 0, then the Intel® 631xESB/632xESB I/O Controller Hub will reboot the system after the second timeout. The reboot is done by asserting PLTRST#.
0	**Intruder Detect (INTRD_DET) –** R/WC. 0 = Software clears this bit by writing a 1 to it, or by RTCRST# assertion. 1 = Set by Intel® 631xESB/632xESB I/O Controller Hub to indicate that an intrusion was detected. This bit is set even if the system is in G3 state. ***Note:*** This bit has a recovery time. After writing a 1 to this bit position (to clear it), the bit may be read back as a 1 for up 65 microseconds before it is read as a 0. Software must be aware of this recovery time when reading this bit after clearing it. ***Note:*** If the INTRUDER# signal is active when the software attempts to clear the INTRD_DET bit, the bit will remain as a 1, and the SMI# will be generated again immediately. The SMI handler can clear the INTRD_SEL bits (TCOBASE + 0Ah, bits 2:1), to avoid further SMIs. However, if the INTRUDER# signals goes inactive and then active again, there will not be further SMI's (because the INTRD_SEL bits would select that no SMI# be generated). ***Note:*** If the INTRUDER# signal goes inactive some point after the INTRD_DET bit is written as a 1, then the INTRD_DET signal will go to a 0 when INTRUDER# input signal goes inactive. Note that this is slightly different than a classic sticky bit, since most sticky bits would remain active indefinitely when the signal goes active and would immediately go inactive when a 1 is written to the bit

21.9.7 TCO1_CNT – TCO1 Control Register

I/O Address:	TCOBASE +08h	Attribute:	R/W, R/W (special), R/WC
Default Value:	0000h	Size:	16-bit
Lockable:	No	Power Well:	Core

Bit	Description
15:13	Reserved
12	**TCO_LOCK** – R/W (special). When set to 1, this bit prevents writes from changing the TCO_EN bit (in offset 30h of Power Management I/O space). Once this bit is set to 1, it can not be cleared by software writing a 0 to this bit location. A core-well reset is required to change this bit from 1 to 0. This bit defaults to 0.
11	TCO Timer Halt (TCO_TMR_HLT) – R/W. 0 = The TCO Timer is enabled to count. 1 = The TCO Timer will halt. It will not count, and thus cannot reach a value that will cause an SMI# or set the SECOND_TO_STS bit. When set, this bit will prevent rebooting and prevent Alert On LAN event messages from being transmitted on the SMLINK (but not Alert On LAN* heartbeat messages).
10	**SEND_NOW** – R/W (special). 0 = The Intel® 631xESB/632xESB I/O Controller Hub will clear this bit when it has completed sending the message. Software must not set this bit to 1 again until the Intel® 631xESB/632xESB I/O Controller Hub has set it back to 0. 1 = Writing a 1 to this bit will cause the Intel® 631xESB/632xESB I/O Controller Hub to send an Alert On LAN Event message over the SMLINK interface, with the Software Event bit set. Setting the SEND_NOW bit causes the Intel® 631xESB/632xESB I/O Controller Hub integrated LAN controller to reset, which can have unpredictable side-effects. Unless software protects against these side effects, software should not attempt to set this bit.
9	**NMI2SMI_EN** – R/W. 0 = Normal NMI functionality. 1 = Forces all NMIs to instead cause SMIs. The functionality of this bit is dependent upon the settings of the NMI_EN bit and the GBL_SMI_EN bit as detailed in the following table: NMI_EN GBL_SMI_EN Description 0 0 No SMI# at all because GBL_SMI_EN = 0 0 1 SMI# will be caused due to NMI events 1 0 No SMI# at all because GBL_SMI_EN = 0 1 1 No SMI# due to NMI because NMI_EN = 1
8	**NMI_NOW** – R/WC. 0 = Software clears this bit by writing a 1 to it. The NMI handler is expected to clear this bit. Another NMI will not be generated until the bit is cleared. 1 = Writing a 1 to this bit causes an NMI. This allows the BIOS or SMI handler to force an entry to the NMI handler.
7:0	Reserved

21.9.8 TCO2_CNT – TCO2 Control Register

I/O Address:	TCOBASE +0Ah	Attribute:	R/W
Default Value:	0008h	Size:	16-bit
Lockable:	No	Power Well:	Resume

Bit	Description
15:6	Reserved
5:4	**OS_POLICY** – R/W. OS-based software writes to these bits to select the policy that the BIOS will use after the platform resets due the WDT. The following convention is recommended for the BIOS and OS: 00 = Boot normally 01 = Shut down 10 = Don't load OS. Hold in pre-boot state and use LAN to determine next step 11 = Reserved ***Note:*** These are just scratchpad bits. They should not be reset when the TCO logic resets the platform due to Watchdog Timer.
3	**GPI11_ALERT_DISABLE** – R/W. At reset (via RSMRST# asserted) this bit is set and GPI[11] alerts are disabled. 0 = Enable. 1 = Disable GPI[11]/SMBALERT# as an alert source for the heartbeats and the SMBus slave.
2:1	**INTRD_SEL** – R/W. This field selects the action to take if the INTRUDER# signal goes active. 00 = No interrupt or SMI# 01 = Interrupt (as selected by TCO_INT_SEL). 10 = SMI 11 = Reserved
0	Reserved

21.9.9 TCO_MESSAGE1 and TCO_MESSAGE2 Registers

I/O Address:	TCOBASE +0Ch (Message 1) TCOBASE +0Dh (Message 2)	Attribute:	R/W
Default Value:	00h	Size:	8-bit
Lockable:	No	Power Well:	Resume

Bit	Description
7:0	**TCO_MESSAGE[*n*]** – R/W. The value written into this register will be sent out via the SMLINK interface in the MESSAGE field of the Alert On LAN message. BIOS can write to this register to indicate its boot progress which can be monitored externally

21.9.10 TCO_WDCNT – TCO Watchdog Control Register

Offset Address:	TCOBASE + 0Eh	Attribute:	R/W
Default Value:	00h	Size:	8 bits
Power Well:	Resume		

Bit	Description
7:0	**Watchdog Status (WDSTATUS) –** R/W. The value written to this register will be sent in the Alert On LAN message on the SMLINK interface. It can be used by the BIOS or system management software to indicate more details on the boot progress. This register will be reset to the default of 00h based on RSMRST# (but not PCI reset).

21.9.11 SW_IRQ_GEN – Software IRQ Generation Register

Offset Address: TCOBASE + 10h
Default Value: 03h
Power Well: Core
Attribute: R/W
Size: 8 bits

Bit	Description
7:2	Reserved
1	IRQ12_CAUSE – R/W. The state of this bit is logically ANDed with the IRQ12 signal as received by the Intel® 631xESB/632xESB I/O Controller Hub's SERIRQ logic. This bit must be a 1 (default) if the Intel® 631xESB/632xESB I/O Controller Hub is expected to receive IRQ12 assertions from a SERIRQ device.
0	IRQ1_CAUSE – R/W. The state of this bit is logically ANDed with the IRQ1 signal as received by the Intel® 631xESB/632xESB I/O Controller Hub's SERIRQ logic. This bit must be a 1 (default) if the Intel® 631xESB/632xESB I/O Controller Hub is expected to receive IRQ1 assertions from a SERIRQ device.

21.9.12 TCO_TMR – TCO Timer Initial Value Register

I/O Address: TCOBASE +12h
Default Value: 0004h
Lockable: No
Attribute: R/W
Size: 16-bit
Power Well: Core

Bit	Description
15:10	Reserved
9:0	**TCO Timer Initial Value** – R/W. Value that is loaded into the timer each time the TCO_RLD register is written. Values of 0000h or 0001h will be ignored and should not be attempted. The timer is clocked at approximately 0.6 seconds, and thus allows timeouts ranging from 1.2 second to 613.8 seconds. Note: The timer has an error of ± 1 tick (0.6s). The TCO Timer will only count down in the S0 state.

21.10 General Purpose I/O Registers (D31:F0)

The control for the general purpose I/O signals is handled through a separate 64-byte I/O space. The base offset for this space is selected by the GPIOBASE register.

21.10.1 GPIO Register I/O Address Map

Table 21-12. Registers to Control GPIO Address Map (Sheet 1 of 2)

GPIOBASE + Offset	Mnemonic	Register Name	Default	Access
General Registers				
00–03h	GPIO_USE_SEL	GPIO Use Select	1B0C01C0h	R/W
04–07h	GP_IO_SEL	GPIO Input/Output Select	E400 FFFFh	R/W
08–0Bh	–	Reserved	–	–
0C–0Fh	GP_LVL	GPIO Level for Input or Output	FF3F0000h	R/W
10–13h		Reserved	–	–
Output Control Registers				
14–17h	–	Reserved	–	–
18–1Bh	GPO_BLINK	GPIO Blink Enable	00040000h	R/W

Table 21-12. Registers to Control GPIO Address Map (Sheet 2 of 2)

GPIOBASE + Offset	Mnemonic	Register Name	Default	Access
1C–1Fh	–	Reserved	–	–
Input Control Registers				
20–2Bh	–	Reserved	–	–
2C–2Fh	GPI_INV	GPIO Signal Invert	00000000h	R/W
30–33h	GPIO_USE_SEL2	GPIO Use Select 2 [63:32]	00000006h	R/W
34–37h	GP_IO_SEL2	GPIO Input/Output Select 2 [63:32]	00000300h	R/W
38–3Bh	GP_LVL2	GPIO Level for Input or Output 2 [63:32]	00030207h	R/W

21.10.2 GPIO_USE_SEL – GPIO Use Select Register

Offset Address: GPIOBASE + 00h
Default Value: 1B0C01C0h
Lockable: No
Attribute:R/W
Size: 32-bit
Power Well:Core for 0:7, 12:13, 16:21,, 23, 26, 29:31
Resume for 8:11, 14:15, 24, 25, 27, 28

Bit	Description
31:29 26, 23, 21, 20 15:14, 13:9, 5:0	GPIO_USE_SEL[31:29, 26, 23, 21, 20, 15:14, 13:9, 5:0] – R/W. Each bit in this register enables the corresponding GPIO (if it exists) to be used as a GPIO, rather than for the native function. 0 = Signal used as native function. 1 = Signal used as a GPIO. ***Notes:*** 1. The following bit is not implemented because there is no corresponding GPIO: 22. 2. The following bits are always 1 because they are unmuxed: 6, 7, 8, 18, 19, 24, 25, 27, 28. 3. Bit 16 is not implemented because the GPIO selection will be controlled by Bit 0 (REQ/GNT pair) 4. Bit 17 is not implemented because the GPIO selection will be controlled by Bit 1 (REQ/GNT pair) 5. If GPIO[n] does not exist, then the bit in this register will always read as 0 and writes will have no effect. 6. After a full reset (RSMRST#) all multiplexed signals in the resume and core wells are configured as their native function rather than as a GPIO. After just a PLTRST#, the GPIO in the core well are configured as their native function. 7. When configured to GPIO mode, the muxing logic should present the inactive state to native logic that uses the pin as an input.

21.10.3 GP_IO_SEL – GPIO Input/Output Select Register

Offset Address: GPIOBASE +04h
Default Value: E400FFFFh
Lockable: No
Attribute: R/W
Size: 32-bit
Power Well: Resume

Bit	Description
31:29	Always 1. These GPIs are fixed as inputs.
28:27	**GP_IO_SEL[28:27]** – R/W. When set to a 1, the corresponding GPIO signal (if enabled in the GPIO_USE_SEL register) is programmed as an input. When set to 0, the GPIO signal is programmed as an output. 0 = Output. The corresponding GPIO signal is an output. 1 = Input. The corresponding GPIO signal is an input.
26	Always 1. This GPI is fixed as an input.

Bit	Description
25:24	**GP_IO_SEL[25:24]** – R/W. When set to a 1, the corresponding GPIO signal (if enabled in the GPIO_USE_SEL register) is programmed as an input. When set to 0, the GPIO signal is programmed as an output. 0 = Output. The corresponding GPIO signal is an output. 1 = Input. The corresponding GPIO signal is an input.
23:16	Always 0. The GPOs are fixed as outputs.
15:0	Always 1. These GPIs are fixed as inputs.

21.10.4 GP_LVL – GPIO Level for Input or Output Register

Offset Address: GPIOBASE +0Ch
Attribute: R/W
Default Value: FF3F0000h
Size: 32-bit
Lockable: No
Power Well: See bit descriptions

Bit	Description
31:29	**GP_LVL[31:29] –** R/W. These bits correspond to input-only GPI in the core well. The corresponding GP_LVL bit reflects the state of the input signal (1 = high, 0 = low). Writes to these bits will have no effect. Since these bits correspond to GPI that are in the core well, these bits will be reset by PLTRST#. 0 = Low 1 = High
28:27	**GP_LVL[28:27] –** R/W. If GPIO[n] is programmed to be an output (via the corresponding bit in the GP_IO_SEL register), then the corresponding GP_LVL[n] bit can be updated by software to drive a high or low value on the output pin. 1 = high, 0 = low. If GPIO[n] is programmed as an input, then the corresponding GP_LVL bit reflects the state of the input signal (1 = high, 0 = low.). Writes will have no effect. Since these bits correspond to GPIO that are in the Resume well, these bits will be reset by RSMRST# and also by a write to the CF9h register. 0 = Low 1 = High
26	**GP_LVL[26] –** R/W. This bit corresponds to an input-only GPI in the core well. The corresponding GP_LVL bit reflects the state of the input signal (1 = high, 0 = low). Writes to this bit will have no effect. Since this bit correspond to a GPI that is in the core well, this bit will be reset by PLTRST#. 0 = Low 1 = High
25:24	**GP_LVL[25:24] –** R/W. If GPIO[n] is programmed to be an output (via the corresponding bit in the GP_IO_SEL register), then the corresponding GP_LVL[n] bit can be updated by software to drive a high or low value on the output pin. 1 = high, 0 = low. If GPIO[n] is programmed as an input, then the corresponding GP_LVL bit reflects the state of the input signal (1 = high, 0 = low.). Writes will have no effect. Since these bits correspond to GPIO that are in the Resume well, these bits will be reset by RSMRST# and also by a write to the CF9h register. 0 = Low 1 = High
23:16	**GP_LVL[23:16] –** R/W. These bits can be updated by software to drive a high or low value on the output pin. These bits correspond to GPIO that are in the core well, and will be reset to their default values by PLTRST#. 0 = Low 1 = High
15:0	Reserved. (These bits are not needed, as the level of general purpose inputs can be read through the registers in the ACPI I/O space).

21.10.5 GPO_BLINK – GPO Blink Enable Register

Offset Address:	GPIOBASE +18h	Attribute:	R/W
Default Value:	0004 0000h	Size:	32-bit
Lockable:	No	Power Well:	See bit description

Bit	Description
28:27, 25	**GP_BLINK[28:27, 25]** – R/W. The setting of this bit has no effect if the corresponding GPIO signal is programmed as an input. 0 = The corresponding GPIO will function normally. 1 = If the corresponding GPIO is programmed as an output, the output signal will blink at a rate of approximately once per second. The high and low times have approximately 0.5 seconds each. The GP_LVL bit is not altered when this bit is set. The value of the corresponding GP_LVL bit remains unchanged during the blink process, and does not effect the blink in any way. The GP_LVL bit is not altered when programmed to blink. It will remain at its previous value. These bits correspond to GPIO in the Resume well. These bits revert to the default value based on RSMRST# or a write to the CF9h register (but not just on PLTRST#).
19:18	GP_BLINK[19:18] – R/W. These bits correspond to GPIO that are in the Core well, and will be reset to their default values by PLTRST#. 0 = The corresponding GPIO will function normally. 1 = The output signal will blink at a rate of approximately once per second. The high and low times are approximately 0.5 seconds each. The GP_LVL bit is not altered when this bit is set.

Note: GPIO18 will blink by default immediately after reset. This signal could be connected to an LED to indicate a failed boot (by programming BIOS to clear GP_BLINK18 after successful POST).

21.10.6 GPI_INV – GPIO Signal Invert Register

Offset Address:	GPIOBASE +2Ch	Attribute:	R/W
Default Value:	00000000h	Size:	32-bit
Lockable:	No	Power Well:	Core 7:0, 12, 13 Resume 15:14, 11:8

Bit	Description
31:16	Reserved
15:14	**GP_INV[n] –** R/W. These bits are used to allow both active-low and active-high inputs to cause SMI# or SCI. Note that in the S0 or S1 state, the input signal must be active for at least two PCI clocks to ensure detection by the Intel® 631xESB/632xESB I/O Controller Hub. In the S3, S4 or S5 states the input signal must be active for at least 2 RTC clocks to ensure detection. The setting of these bits has no effect if the corresponding GPIO is programmed as an output. These bits correspond to GPI that are in the resume well, and will be reset to their default values by RSMRST# or by a write to the CF9h register. 0 = The corresponding GPI_STS bit is set when the Intel® 631xESB/632xESB I/O Controller Hub detects the state of the input pin to be high. 1 = The corresponding GPI_STS bit is set when the Intel® 631xESB/632xESB I/O Controller Hub detects the state of the input pin to be low.

Bit	Description
13:12	**GP_INV[n] –** R/W. These bits are used to allow both active-low and active-high inputs to cause SMI# or SCI. Note that in the S0 or S1 state, the input signal must be active for at least two PCI clocks to ensure detection by the Intel® 631xESB/632xESB I/O Controller Hub. These bits correspond to GPI that are in the core well, and will be reset to their default values by PLTRST#. 0 = The corresponding GPI_STS bit is set when the Intel® 631xESB/632xESB I/O Controller Hub detects the state of the input pin to be high. 1 = The corresponding GPI_STS bit is set when the Intel® 631xESB/632xESB I/O Controller Hub detects the state of the input pin to be low.
11:8	**GP_INV[n] –** R/W. These bits are used to allow both active-low and active-high inputs to cause SMI# or SCI. Note that in the S0 or S1 state, the input signal must be active for at least two PCI clocks to ensure detection by the Intel® 631xESB/632xESB I/O Controller Hub. In the S3, S4 or S5 states the input signal must be active for at least 2 RTC clocks to ensure detection. The setting of these bits has no effect if the corresponding GPIO is programmed as an output. These bits correspond to GPI that are in the resume well, and will be reset to their default values by RSMRST# or by a write to the CF9h register. 0 = The corresponding GPI_STS bit is set when the Intel® 631xESB/632xESB I/O Controller Hub detects the state of the input pin to be high. 1 = The corresponding GPI_STS bit is set when the Intel® 631xESB/632xESB I/O Controller Hub detects the state of the input pin to be low.
7:0	**GP_INV[n] –** R/W. These bits are used to allow both active-low and active-high inputs to cause SMI# or SCI. Note that in the S0 or S1 state, the input signal must be active for at least two PCI clocks to ensure detection by the Intel® 631xESB/632xESB I/O Controller Hub. The setting of these bits will have no effect if the corresponding GPIO is programmed as an output. These bits correspond to GPI that are in the core well, and will be reset to their default values by PLTRST#. 0 = The corresponding GPI_STS bit is set when the Intel® 631xESB/632xESB I/O Controller Hub detects the state of the input pin to be high. 1 = The corresponding GPI_STS bit is set when the Intel® 631xESB/632xESB I/O Controller Hub detects the state of the input pin to be low.

21.10.7 GPIO_USE_SEL2 – GPIO Use Select 2 Register[63:32]

Offset Address:	GPIOBASE +30h	Attribute:	R/W
Default Value:	00000006h	Size:	32-bit
Lockable:	No	Power Well:	CPU I/O for 17, Core for 16:0

Bit	Description
17, 9:8, 0	GPIO_USE_SEL2[49, 41:40, 32] – R/W. Each bit in this register enables the corresponding GPIO (if it exists) to be used as a GPIO, rather than for the native function. 0 = Signal used as native function. 1 = Signal used as a GPIO. After a full reset (RSMRST#) all multiplexed signals in the resume and core wells are configured as a GPIO rather than as their native function. After just a PLTRST#, the GPIO in the core well are configured as GPIO. ***Notes:*** 1. The following bits are not implemented because there is no corresponding GPIO: 3:7, 10:15, 18:31. 2. The following bits are always 1 because they are unmuxed: 1:2 3. Bit 16 is not implemented because the GPIO selection will be controlled by Bit 8 (REQ/GNT pair) 4. If GPIO[n] does not exist, then the bit in this register will always read as 0 and writes will have no effect.

21.10.8 GP_IO_SEL2 – GPIO Input/Output Select 2 Register[63:32]

Offset Address:	GPIOBASE +34h	Attribute:	R/W
Default Value:	00000300h	Size:	32-bit
Lockable:	No	Power Well:	Core

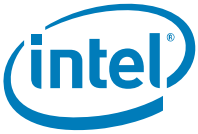
Bit	Description
31:18	Always 0. No corresponding GPIO.
17:16	Always 0. Outputs.
15:10	Always 0. No corresponding GPIO.
9:8	Always 1. Inputs.
7:3	Always 0. No corresponding GPIO.
2:0	**GP_IO_SEL2[34:32] –** R/W. 0 = GPIO signal is programmed as an output. 1 = Corresponding GPIO signal (if enabled in the GPIO_USE_SEL2 register) is programmed as an input.

21.10.9 GP_LVL2 – GPIO Level for Input or Output 2 Register[63:32]

Offset Address:	GPIOBASE +38h	Attribute:	R/W
Default Value:	00030207h	Size:	32-bit
Lockable:	No	Power Well:	See below

Bit	Description
31:18	Reserved. Read-only 0
17:16	**GP_LVL[49:48] –** R/W. The corresponding GP_LVL[n] bit can be updated by software to drive a high or low value on the output pin. Since these bits correspond to GPIO that are in the processor I/O and core well, respectively, these bits will be reset by PLTRST#. 0 = low 1 = high
15:10	Reserved. Read-only 0
9:8	**GP_LVL[41:40] –** R/W. The corresponding GP_LVL[n] bit reflects the state of the input signal. Writes will have no effect. Since these bits correspond to GPIO that are in the core well, these bits will be reset by PLTRST#. 0 = low 1 = high
7:3	Reserved. Read-only 0
2:0	**GP_LVL[34:32] –** R/W. If GPIOn is programmed to be an output (via the corresponding bit in the GP_IO_SEL register), then the corresponding GP_LVL[n] bit can be updated by software to drive a high or low value on the output pin. If GPIOn is programmed as an input, then the corresponding GP_LVL bit reflects the state of the input signal (1 = high, 0 = low). Writes will have no effect. 0 = low 1 = high Since these bits correspond to GPIO that are in the core well, these bits will be reset by PLTRST#.

§§



22 IDE Controller Registers (D31:F1)

22.1 PCI Configuration Registers (IDE – D31:F1)

Note: Address locations that are not shown should be treated as Reserved (See Section 2.3 for details). All of the IDE registers are in the core well. None of the registers can be locked.

Table 22-1. IDE Controller PCI Register Address Map (IDE-D31:F1)

Offset	Mnemonic	Register Name	Default	Type
00–01h	VID	Vendor Identification	8086h	RO
02–03h	DID	Device Identification	269Eh	RO
04–05h	PCICMD	PCI Command	00h	R/W, RO
06–07h	PCISTS	PCI Status	0280h	R/W, RO
08h	RID	Revision Identification	See register description.	RO
09h	PI	Programming Interface	8Ah	R/W, RO
0Ah	SCC	Sub Class Code	01h	RO
0Bh	BCC	Base Class Code	01h	RO
0Dh	PMLT	Primary Master Latency Timer	00h	RO
10–13h	PCMD_BAR	Primary Command Block Base Address	00000001h	R/W, RO
14–17h	PCNL_BAR	Primary Control Block Base Address	00000001h	R/W, RO
18–1Bh	SCMD_BAR	Secondary Command Block Base Address	00000001h	R/W, RO
1C–1Fh	SCNL_BAR	Secondary Control Block Base Address	00000001h	R/W, RO
20–23h	BM_BASE	Bus Master Base Address	00000001h	R/W, RO
2C–2Dh	IDE_SVID	Subsystem Vendor ID	00h	R/WO
2E–2Fh	IDE_SID	Subsystem ID	00h	R/WO
3C	INTR_LN	Interrupt Line	See register description.	R/W
3D	INTR_PN	Interrupt Pin	01h	RO
40–41h	IDE_TIMP	Primary IDE Timing	0000h	R/W
42–43h	IDE_TIMS	Secondary IDE Timing	0000h	R/W
44h	SLV_IDETIM	Slave IDE Timing	00h	R/W
48h	SDMA_CNT	Synchronous DMA Control	00h	R/W
4A–4Bh	SDMA_TIM	Synchronous DMA Timing	0000h	R/W
54h	IDE_CONFIG	IDE I/O Configuration	00h	R/W
C0h	ATC	APM Trapping Control	00h	R/W
C4h	ATS	APM Trapping Status	00h	R/WC

Note: The Intel® 631xESB/632xESB I/O Controller Hub IDE controller is not arbitrated as a PCI device; therefore, it does not need a master latency timer.

22.1.1 VID – Vendor Identification Register (IDE – D31:F1)

Offset Address:	00–01h	Attribute:	RO
Default Value:	8086h	Size:	16-bit
Lockable:	No	Power Well:	Core

Bit	Description
15:0	Vendor ID – RO. This is a 16-bit value assigned to Intel. Intel VID = 8086h

22.1.2 DID – Device Identification Register (IDE – D31:F1)

Offset Address:	02–03h	Attribute:	RO
Default Value:	269Eh	Size:	16-bit
Lockable:	No	Power Well:	Core

Bit	Description
15:0	Device ID – RO. This is a 16-bit value assigned to the Intel® 631xESB/632xESB I/O Controller Hub IDE controller.

22.1.3 PCICMD – PCI Command Register (IDE – D31:F1)

Address Offset:	04h–05h	Attribute:	RO, R/W
Default Value:	00h	Size:	16 bits

Bit	Description
15:11	Reserved
10	Interrupt Disable (ID) – R/W. 0 = Enables the IDE controller to assert INTA# (native mode) or IRQ14/15 (legacy mode). 1 = Disable. The interrupt will be deasserted.
9	Fast Back to Back Enable (FBE) – RO. Reserved as 0.
8	SERR# Enable (SERR_EN) – RO. Reserved as 0.
7	Wait Cycle Control (WCC) – RO. Reserved as 0.
6	Parity Error Response (PER) – RO. Reserved as 0.
5	VGA Palette Snoop (VPS) – RO. Reserved as 0.
4	Postable Memory Write Enable (PMWE) – RO. Reserved as 0.
3	Special Cycle Enable (SCE) – RO. Reserved as 0.
2	**Bus Master Enable (BME) –** R/W. Controls the Intel® 631xESB/632xESB I/O Controller Hub's ability to act as a PCI master for IDE Bus Master transfers.
1	**Memory Space Enable (MSE) –** R/W. 0 = Disables access. 1 = Enables access to the IDE Expansion memory range. The EXBAR register (Offset 24h) must be programmed before this bit is set. ***Note:*** BIOS should set this bit to a 1.
0	**I/O Space Enable (IOSE) –** R/W. This bit controls access to the I/O space registers. 0 = Disables access to the Legacy or Native IDE ports (both Primary and Secondary) as well as the Bus Master IO registers. 1 = Enable. Note that the Base Address register for the Bus Master registers should be programmed before this bit is set. ***Notes:*** 1. Separate bits are provided (IDE Decode Enable, in the IDE Timing register) to independently disable the Primary or Secondary I/O spaces. 2. When this bit is 0 and the IDE controller is in Native Mode, the Interrupt Pin Register (see Section 22.1.19) will be masked (the interrupt will not be asserted). If an interrupt occurs while the masking is in place and the interrupt is still active when the masking ends, the interrupt will be allowed to be asserted.

22.1.4 PCISTS – PCI Status Register (IDE – D31:F1)

Address Offset:	06–07h	Attribute:	R/WC, RO
Default Value:	0280h	Size:	16 bits

Note: For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 to the bit has no effect.

Bit	Description
15	Detected Parity Error (DPE) – RO. Reserved as 0.
14	Signaled System Error (SSE) – RO. Reserved as 0.
13	**Received Master Abort (RMA) –** R/WC. 0 = Master abort Not generated by Bus Master IDE interface function. 1 = Bus Master IDE interface function, as a master, generated a master abort.
12	Reserved as 0 **–** RO.
11	Reserved as 0 – RO.
10:9	DEVSEL# Timing Status (DEV_STS) – RO. 01 = Hardwired; however, the Intel® 631xESB/632xESB I/O Controller Hub does not have a real DEVSEL# signal associated with the IDE unit, so these bits have no effect.
8	Data Parity Error Detected (DPED) **–** RO. Reserved as 0.
7	Fast Back to Back Capable (FB2BC) **–** RO. Reserved as 1.
6	User Definable Features (UDF) **–** RO. Reserved as 0.
5	66MHz Capable (66MHZ_CAP) **–** RO. Reserved as 0.
4	Reserved
3	Interrupt Status (INTS) – RO. This bit is independent of the state of the Interrupt Disable bit in the command register. 0 = Interrupt is cleared. 1 = Interrupt/MSI is asserted.
2:0	Reserved

22.1.5 RID – Revision Identification Register (IDE – D31:F1)

Offset Address:	08h	Attribute:	RO
Default Value:	See bit description	Size:	8 bits

Bit	Description
7:0	**Revision ID –** RO. Refer to Table 2-33 or the *Intel® 631xESB/632xESB I/O Controller Hub EDS Specification Update* for the value of the Revision ID Register

22.1.6 PI – Programming Interface Register (IDE – D31:F1)

Address Offset:	09h	Attribute:	RO
Default Value:	8Ah	Size:	8 bits

Bit	Description
7	This read-only bit is a 1 to indicate that the Intel® 631xESB/632xESB I/O Controller Hub supports bus master operation
6:4	Reserved. Hardwired to 000b.
3	**SOP_MODE_CAP** – RO. This read-only bit is a 1 to indicate that the secondary controller supports both legacy and native modes.

2	**SOP_MODE_SEL** – R/W. This read/write bit determines the mode that the secondary IDE channel is operating in. 0 = Legacy-PCI mode (default) 1 = Native-PCI mode
1	**POP_MODE_CAP** – RO. This read-only bit is a 1 to indicate that the primary controller supports both legacy and native modes.
0	**POP_MODE_SEL** – R/W. This read/write bits determines the mode that the primary IDE channel is operating in. 0 = Legacy-PCI mode (default) 1 = Native-PCI mode

22.1.7 SCC – Sub Class Code Register (IDE – D31:F1)

Address Offset: 0Ah Attribute: RO
Default Value: 01h Size: 8 bits

Bit	Description
7:0	Sub Class Code (SCC) – RO. 01h = IDE device, in the context of a mass storage device.

22.1.8 BCC – Base Class Code Register (IDE – D31:F1)

Address Offset: 0Bh Attribute: RO
Default Value: 01h Size: 8 bits

Bit	Description
7:0	Base Class Code (BCC) – RO. 01 = Mass storage device

22.1.9 CLS – Cache Line Size Register (IDE – D31:F1)

Address Offset: 0Ch Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Description
7:0	Cache Line Size (CLS) – RO. 00h =Hardwired. The IDE controller is implemented internally so this register has no meaning.

22.1.10 PMLT – Primary Master Latency Timer Register (IDE – D31:F1)

Address Offset: 0Dh Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Description
7:0	Master Latency Timer Count (MLTC) – RO. 00h =Hardwired. The IDE controller is implemented internally, and is not arbitrated as a PCI device, so it does not need a Master Latency Timer.

22.1.11 PCMD_BAR – Primary Command Block Base Address Register (IDE – D31:F1)

Address Offset: 10h–13h
Default Value: 00000001h
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31:16	Reserved
15:3	**Base Address –** R/W. Base address of the I/O space (8 consecutive I/O locations).
2:1	Reserved
0	Resource Type Indicator (RTE) **–** RO. Hardwired to 1 indicating a request for I/O space.

Note: This 8-byte I/O space is used in native mode for the Primary Controller's Command Block.

22.1.12 PCNL_BAR – Primary Control Block Base Address Register (IDE – D31:F1)

Address Offset: 14h–17h
Default Value: 00000001h
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31:16	Reserved
15:2	**Base Address –** R/W. Base address of the I/O space (4 consecutive I/O locations).
1	Reserved
0	Resource Type Indicator (RTE) **–** RO. Hardwired to 1 indicating a request for I/O space.

Note: This 4-byte I/O space is used in native mode for the Primary Controller's Command Block.

22.1.13 SCMD_BAR – Secondary Command Block Base Address Register (IDE D31:F1)

Address Offset: 18h–1Bh
Default Value: 00000001h
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31:16	Reserved
15:3	**Base Address –** R/W. Base address of the I/O space (8 consecutive I/O locations).
2:1	Reserved
0	Resource Type Indicator (RTE) **–** RO. Hardwired to 1 indicating a request for I/O space.

Note: This 4-byte I/O space is used in native mode for the Secondary Controller's Command Block.

22.1.14 SCNL_BAR – Secondary Control Block Base Address Register (IDE D31:F1)

Address Offset: 1Ch–1Fh
Default Value: 00000001h
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31:16	Reserved

15:2	**Base Address –** R/W. Base address of the I/O space (4 consecutive I/O locations).
1	Reserved
0	Resource Type Indicator (RTE) **–** RO. Hardwired to 1 indicating a request for I/O space.

Note: This 4-byte I/O space is used in native mode for the Secondary Controller's Command Block.

22.1.15 BM_BASE – Bus Master Base Address Register (IDE – D31:F1)

Address Offset: 20h–23h Attribute: R/W, RO
Default Value: 00000001h Size: 32 bits

The Bus Master IDE interface function uses Base Address register 5 to request a 16-byte I/O space to provide a software interface to the Bus Master functions. Only 12 bytes are actually used (6 bytes for primary, 6 bytes for secondary). Only bits [15:4] are used to decode the address.

Bit	Description
31:16	Reserved
15:4	**Base Address –** R/W. This field provides the base address of the I/O space (16 consecutive I/O locations).
3:1	Reserved
0	Resource Type Indicator (RTE) **–** RO. Hardwired to 1 indicating a request for I/O space.

22.1.16 IDE_SVID – Subsystem Vendor Identification (IDE – D31:F1)

Address Offset: 2Ch–2Dh Attribute: R/WO
Default Value: 00h Size: 16 bits
Lockable: No Power Well: Core

Bit	Description
15:0	**Subsystem Vendor ID (SVID) –** R/WO. The SVID register, in combination with the Subsystem ID (SID) register, enables the operating system (OS) to distinguish subsystems from each other. Software (BIOS) sets the value in this register. After that, the value can be read, but subsequent writes to this register have no effect. The value written to this register will also be readable via the corresponding SVID registers for the USB#1, USB#2, and SMBus functions.

22.1.17 IDE_SID – Subsystem Identification Register (IDE – D31:F1)

Address Offset: 2Eh–2Fh Attribute: R/WO
Default Value: 00h Size: 16 bits
Lockable: No Power Well: Core

Bit	Description
15:0	**Subsystem ID (SID) –** R/WO. The SID register, in combination with the SVID register, enables the operating system (OS) to distinguish subsystems from each other. Software (BIOS) sets the value in this register. After that, the value can be read, but subsequent writes to this register have no effect. The value written to this register will also be readable via the corresponding SID registers for the USB#1, USB#2, and SMBus functions.

22.1.18 INTR_LN – Interrupt Line Register (IDE – D31:F1)

Address Offset: 3Ch
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	**Interrupt Line (INT_LN)** – R/W. This field is used to communicate to software the interrupt line that the interrupt pin is connected to.

22.1.19 INTR_PN – Interrupt Pin Register (IDE – D31:F1)

Address Offset: 3Dh
Default Value: See Register Description
Attribute: RO
Size: 8 bits

Bit	Description
7:0	Interrupt Pin – RO. This reflects the value of D31IP.PIP (Chipset Config Registers:Offset 3100h:bits 7:4).

22.1.20 IDE_TIMP – IDE Primary Timing Register (IDE – D31:F1)

Address Offset: 40–41h
Default Value: 0000h
Attribute: R/W
Size: 16 bits

This register controls the timings driven on the IDE cable for PIO and 8237 style DMA transfers. It also controls operation of the buffer for PIO transfers.

Bit	Description
15	**IDE Decode Enable (IDE) –** R/W. The IDE I/O Space Enable bit (D31:F1:04h, bit 0) in the Command register must be set in order for this bit to have any effect. 0 = Disable. 1 = Enables the Intel® 631xESB/632xESB I/O Controller Hub to decode the Command (1F0–1F7h) and Control (3F6h) Blocks. This bit also effects the memory decode range for IDE Expansion.
14	Drive 1 Timing Register Enable (SITRE) – R/W. 0 = Use bits 13:12, 9:8 for both drive 0 and drive 1. 1 = Use bits 13:12, 9:8 for drive 0, and use the Slave IDE Timing register for drive 1
13:12	**IORDY Sample Point (ISP) –** R/W. The setting of these bits determine the number of PCI clocks between IDE IOR#/IOW# assertion and the first IORDY sample point. 00 = 5 clocks 01 = 4 clocks 10 = 3 clocks 11 = Reserved
11:10	Reserved
9:8	**Recovery Time (RCT) –** R/W. The setting of these bits determines the minimum number of PCI clocks between the last IORDY sample point and the IOR#/IOW# strobe of the next cycle. 00 = 4 clocks 01 = 3 clocks 10 = 2 clocks 11 = 1 clock
7	**Drive 1 DMA Timing Enable (DTE1) –** R/W. 0 = Disable. 1 = Enable the fast timing mode for DMA transfers only for this drive. PIO transfers to the IDE data port will run in compatible timing.
6	**Drive 1 Prefetch/Posting Enable (PPE1) –** R/W. 0 = Disable. 1 = Enable Prefetch and posting to the IDE data port for this drive.

Bit	Description
5	**Drive 1 IORDY Sample Point Enable (IE1) –** R/W. 0 = Disable IORDY sampling for this drive. 1 = Enable IORDY sampling for this drive.
4	**Drive 1 Fast Timing Bank (TIME1) –** R/W. 0 = Accesses to the data port will use compatible timings for this drive. 1 = When this bit = 1 and bit 14 = 0, accesses to the data port will use bits 13:12 for the IORDY sample point, and bits 9:8 for the recovery time. When this bit = 1 and bit 14 = 1, accesses to the data port will use the IORDY sample point and recover time specified in the slave IDE timing register.
3	**Drive 0 DMA Timing Enable (DTE0) –** R/W. 0 = Disable 1 = Enable fast timing mode for DMA transfers only for this drive. PIO transfers to the IDE data port will run in compatible timing.
2	**Drive 0 Prefetch/Posting Enable (PPE0) –** R/W. 0 = Disable prefetch and posting to the IDE data port for this drive. 1 = Enable prefetch and posting to the IDE data port for this drive.
1	**Drive 0 IORDY Sample Point Enable (IE0) –** R/W. 0 = Disable IORDY sampling is disabled for this drive. 1 = Enable IORDY sampling for this drive.
0	**Drive 0 Fast Timing Bank (TIME0) –** R/W. 0 = Accesses to the data port will use compatible timings for this drive. 1 = Accesses to the data port will use bits 13:12 for the IORDY sample point, and bits 9:8 for the recovery time

22.1.21 IDE_TIMS – IDE Secondary Timing Register (IDE – D31:F1)

Address Offset: 42–43h
Default Value: 0000h
Attribute: R/W
Size: 16 bits

Bit	Description
15	**IDE Decode Enable (IDE)** – R/W. This bit enables/disables the Secondary decode. The IDE I/O Space Enable bit (D31:F1:04h, bit 0) in the Command register must be set in order for this bit to have any effect. Additionally, separate configuration bits are provided (in the IDE I/O Configuration register) to individually disable the secondary IDE interface signals, even if the IDE Decode Enable bit is set. 0 = Disable. 1 = Enables the Intel® 631xESB/632xESB I/O Controller Hub to decode the associated Command Blocks (170–177h) and Control Block (376h). Accesses to these ranges return 00h, as the secondary channel is not implemented.
14:12	No Operation (NOP) – R/W. These bits are read/write for legacy software compatibility, but have no functionality in the Intel® 631xESB/632xESB I/O Controller Hub since a secondary channel does not exist.
11	Reserved
10:0	No Operation (NOP) – R/W. These bits are read/write for legacy software compatibility, but have no functionality in the Intel® 631xESB/632xESB I/O Controller Hub since a secondary channel does not exist.

22.1.22 SLV_IDETIM – Slave (Drive 1) IDE Timing Register (IDE – D31:F1)

Address Offset: 44h
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:4	No Operation (NOP) – R/W. These bits are read/write for legacy software compatibility, but have no functionality in the Intel® 631xESB/632xESB I/O Controller Hub.
3:2	**Primary Drive 1 IORDY Sample Point (PISP1) –** R/W. This field determines the number of PCI clocks between IOR#/IOW# assertion and the first IORDY sample point, if the access is to drive 1 data port and bit 14 of the IDE timing register for primary is set. 00 = 5 clocks 01 = 4 clocks 10 = 3 clocks 11 = Reserved
1:0	**Primary Drive 1 Recovery Time (PRCT1) –** R/W. This field determines the minimum number of PCI clocks between the last IORDY sample point and the IOR#/IOW# strobe of the next cycle, if the access is to drive 1 data port and bit 14 of the IDE timing register for primary is set. 00 = 4 clocks 01 = 3 clocks 10 = 2 clocks 11 = 1 clocks

22.1.23 SDMA_CNT – Synchronous DMA Control Register (IDE – D31:F1)

Address Offset: 48h
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:4	Reserved
3:2	No Operation (NOP) – R/W. These bits are read/write for legacy software compatibility, but have no functionality in the Intel® 631xESB/632xESB I/O Controller Hub.
1	Primary Drive 1 Synchronous DMA Mode Enable (PSDE1) – R/W. 0 = Disable (default) 1 = Enable Synchronous DMA mode for primary channel drive 1.
0	Primary Drive 0 Synchronous DMA Mode Enable (PSDE0) – R/W. 0 = Disable (default) 1 = Enable Synchronous DMA mode for primary channel drive 0.

22.1.24 SDMA_TIM – Synchronous DMA Timing Register (IDE – D31:F1)

Address Offset: 4A–4Bh
Default Value: 0000h
Attribute: R/W
Size: 16 bits

Note: For FAST_PCB1 = 1 (133 MHz clk) in bits [13:12, 9:8, 5:4, 1:0], refer to Section 5.20.4 for details.

Bit	Description
15:14	Reserved
13:12	No Operation (NOP) – R/W. These bits are read/write for legacy software compatibility, but have no functionality in the Intel® 631xESB/632xESB I/O Controller Hub.
11:10	Reserved
9:8	No Operation (NOP) – R/W. These bits are read/write for legacy software compatibility, but have no functionality in the Intel® 631xESB/632xESB I/O Controller Hub.

<table>
<tr><th>Bit</th><th>Description</th></tr>
<tr><td>7:6</td><td>Reserved</td></tr>
<tr><td>5:4</td><td>Primary Drive 1 Cycle Time (PCT1) – R/W. For Ultra ATA mode, the setting of these bits determines the minimum write strobe cycle time (CT). The DMARDY#-to-STOP (RP) time is also determined by the setting of these bits.
<table>
<tr><th rowspan="2">Bits</th><th colspan="2">SBC[1] = 0</th><th colspan="2">SBC[1] = 1</th><th colspan="2">FSBCE[1] = 1</th></tr>
<tr><th>CT</th><th>RP</th><th>CT</th><th>RP</th><th>CT</th><th>RP</th></tr>
<tr><td>00</td><td>4</td><td>6</td><td colspan="2">Reserved</td><td colspan="2">Reserved</td></tr>
<tr><td>01</td><td>3</td><td>5</td><td>3</td><td>8</td><td>3</td><td>16</td></tr>
<tr><td>10</td><td>2</td><td>4</td><td>2</td><td>8</td><td colspan="2">Reserved</td></tr>
<tr><td>11</td><td colspan="2">Reserved</td><td colspan="2">Reserved</td><td colspan="2">Reserved</td></tr>
</table></td></tr>
<tr><td>3:2</td><td>Reserved</td></tr>
<tr><td>1:0</td><td>Primary Drive 0 Cycle Time (PCT0) – R/W. For Ultra ATA mode, the setting of these bits determines the minimum write strobe cycle time (CT). The DMARDY#-to-STOP (RP) time is also determined by the setting of these bits.
<table>
<tr><th rowspan="2">Bits</th><th colspan="2">SBC[1] = 0</th><th colspan="2">SBC[1] = 1</th><th colspan="2">FSBCE[1] = 1</th></tr>
<tr><th>CT</th><th>RP</th><th>CT</th><th>RP</th><th>CT</th><th>RP</th></tr>
<tr><td>00</td><td>4</td><td>6</td><td colspan="2">Reserved</td><td colspan="2">Reserved</td></tr>
<tr><td>01</td><td>3</td><td>5</td><td>3</td><td>8</td><td>3</td><td>16</td></tr>
<tr><td>10</td><td>2</td><td>4</td><td>2</td><td>8</td><td colspan="2">Reserved</td></tr>
<tr><td>11</td><td colspan="2">Reserved</td><td colspan="2">Reserved</td><td colspan="2">Reserved</td></tr>
</table></td></tr>
</table>

22.1.25 IDE_CONFIG – IDE I/O Configuration Register (IDE – D31:F1)

Address Offset: 54h
Default Value: 00h
Attribute: R/W
Size: 32 bits

Bit	Description
31:24	Reserved
23:20	**Miscellaneous Scratchpad (MS) –** R/W. Previously defined as a scratchpad bit to indicate to a driver that ATA-100 is supported. This is not used by software as all they needed to know was located in bits 7:4. See the definition of those bits.
19:18	**No Operation (NOP) –** R/W. These bits are read/write for legacy software compatibility, but have no functionality in the Intel® 631xESB/632xESB I/O Controller Hub.
17:16	**Primary Signal Mode (PSM): –** R/W. These bits are used to control mode of the IDE signal pins for swap bay support. If the PRS bit (Chipset Config Registers:Offset 3414h:bit 1) is '1', the reset states of bits 17:16 will be '01'(tri-state) instead of '00' (normal). 00 = Normal (Enabled) 01 = Tri-state (Disabled) 10 = Drive Low (Disabled) 11 = Reserved
15:14	**No Operation (NOP) –** R/W. These bits are read/write for legacy software compatibility, but have no functionality in the Intel® 631xESB/632xESB I/O Controller Hub.
13:12	**Fast Synchronous Base Clock Enable (FSBCE): –** R/W 0 = Disables fast ATA modes. 1 = Enables fast ATA modes. This overrides the state of the SCB[1:0]bits in this register.

Bit	Description
11:8	Reserved
7:4	**Ultra-DMA Cable Connected (UCC):** – R/W. These are scratchpad bits to indicate that an 80-pin connector is attached to the ATA device, and ATA-66, ATA-100, or ATA-133 timings may be used. The previous definition of these bits were to indicate support for ATA-66, but all they really indicate is that a GPIO elsewhere in the Intel® 631xESB/632xESB I/O Controller Hub determined that an 80-pin connector is attached. Since driver software cannot read that GPIO directly, BIOS copies it here. BIOS must set these bits properly or drivers will not allow ATA-66, ATA-100, or ATA-133 timings. Bit 7 controls the secondary device, 1, bit 6 secondary device 0, bit 5 primary device 1, and bit 4 primary device 0.
3:2	**No Operation (NOP) –** R/W. These bits are read/write for legacy software compatibility, but have no functionality in the Intel® 631xESB/632xESB I/O Controller Hub.
1:0	**Synchronous Base Clock (SBC)**: Clock used to determine CT and RP timings for synchronous DMA timings. '0' = 33 MHz clock used, '1' = 66 MHz clock used. Bit 1 controls the primary slave device, and bit 0 controls the primary master device.

22.1.26 ATC – APM Trapping Control Register (IDE – D31:F1)

Address Offset: C0h Attribute: R/W
Default Value: 00h Size: 8 bits

Bit	Description
7:2	Reserved.
1	**Slave Trap (PST) –** R/W. Enables trapping and SMI# assertion on legacy I/O accesses to 1F0h-1F7h and 3F6h. The active device must be the slave device for the trap and/or SMI# to occur.
0	**Master Trap (PMT) –** R/W. Enables trapping and SMI# assertion on legacy I/O accesses to 1F0h-1F7h and 3F6h. The active device must be the master device for the trap and/or SMI# to occur.

22.1.27 ATS – APM Trapping Register (IDE – D31:F1)

Address Offset: C4h Attribute: R/WC
Default Value: 00h Size: 8 bits

Bit	Description
7:2	Reserved.
1	**Slave Trap Status (PSTS) –** R/W. Indicates that a trap occured to the slave device.
0	**Master Trap Status (PMTS) –** R/W. Indicates that a trap occured to the master device.

22.2 Bus Master IDE I/O Registers (IDE – D31:F1)

The bus master IDE function uses 16 bytes of I/O space, allocated via the BMIBA register, located in Device 31:Function 1 Configuration space, offset 20h. All bus master IDE I/O space registers can be accessed as byte, word, or DWord quantities. Reading reserved bits returns an indeterminate, inconsistent value, and writes to reserved bits have no affect (but should not be attempted). The description of the I/O registers is shown in Table 22-2.

Table 22-2. Bus Master IDE I/O Registers (Sheet 1 of 2)

BMIBASE + Offset	Mnemonic	Register Name	Default	Type
00	BMICP	Bus Master IDE Command Primary	00h	R/W
01	–	Reserved	00h	RO

Table 22-2. Bus Master IDE I/O Registers (Sheet 2 of 2)

BMIBASE + Offset	Mnemonic	Register Name	Default	Type
02	BMISP	Bus Master IDE Status Primary	00h	R/WC
03	–	Reserved	00h	RO
04–07	BMIDP	Bus Master IDE Descriptor Table Pointer Primary	xxxxxxxxh	R/W

22.2.1 BMICP – Bus Master IDE Command Register (IDE – D31:F1)

Address Offset: BMIBASE + 00h
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:4	Reserved. Returns 0.
3	**Read / Write Control (RWC) –** R/W. This bit sets the direction of the bus master transfer: This bit must NOT be changed when the bus master function is active. 0 = Memory reads 1 = Memory writes
2:1	Reserved. Returns 0.
0	**Start/Stop Bus Master (START) –** R/W. 0 = All state information is lost when this bit is cleared. Master mode operation cannot be stopped and then resumed. If this bit is reset while bus master operation is still active (that is, the Bus Master IDE Active bit (BMIBASE + 02h, bit 0) of the Bus Master IDE Status register for that IDE channel is set) and the drive has not yet finished its data transfer (the Interrupt bit (BMIBASE + 02h, bit 2) in the Bus Master IDE Status register for that IDE channel is not set), the bus master command is said to be aborted and data transferred from the drive may be discarded instead of being written to system memory. 1 = Enables bus master operation of the controller. Bus master operation does not actually start unless the Bus Master Enable bit (D31:F1:04h, bit 2) in PCI configuration space is also set. Bus master operation begins when this bit is detected changing from 0 to 1. The controller will transfer data between the IDE device and memory only when this bit is set. Master operation can be halted by writing a 0 to this bit. ***Note:*** This bit is intended to be cleared by software after the data transfer is completed, as indicated by either the Bus Master IDE Active bit being cleared or the Interrupt bit of the Bus Master IDE Status register for that IDE channel being set, or both. Hardware does not clear this bit automatically.

22.2.2 BMISP – Bus Master IDE Status Register (IDE – D31:F1)

Address Offset: BMIBASE + 02h Attribute: R/WC
Default Value: 00h Size: 8 bits

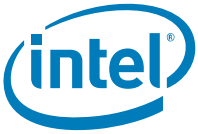
Bit	Description
7	**PRD Interrupt Status (PRDIS) –** R/WC. 0 = When this bit is cleared by software, the interrupt is cleared. 1 = Set when the host controller completes execution of a PRD that has its Interrupt bit (bit 2 of this register) set.
6	**Drive 1 DMA Capable –** R/W. 0 = Not Capable. 1 = Capable. Set by device dependent code (BIOS or device driver) to indicate that drive 1 for this channel is capable of DMA transfers, and that the controller has been initialized for optimum performance. The Intel® 631xESB/632xESB I/O Controller Hub does not use this bit. It is intended for systems that do not attach BMIDE to the PCI bus.
5	**Drive 0 DMA Capable –** R/W. 0 = Not Capable 1 = Capable. Set by device dependent code (BIOS or device driver) to indicate that drive 0 for this channel is capable of DMA transfers, and that the controller has been initialized for optimum performance. The Intel® 631xESB/632xESB I/O Controller Hub does not use this bit. It is intended for systems that do not attach BMIDE to the PCI bus.
4:3	Reserved. Returns 0.
2	**Interrupt –** R/WC. Software can use this bit to determine if an IDE device has asserted its interrupt line (IDEIRQ). 0 = Software clears this bit by writing a 1 to it. If this bit is cleared while the interrupt is still active, this bit will remain clear until another assertion edge is detected on the interrupt line. 1 = Set by the rising edge of the IDE interrupt line, regardless of whether or not the interrupt is masked in the 8259 or the internal I/O APIC. When this bit is read as 1, all data transferred from the drive is visible in system memory.
1	**Error –** R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = This bit is set when the controller encounters a target abort or master abort when transferring data on PCI.
0	**Bus Master IDE Active (ACT)** – RO. 0 = This bit is cleared by the Intel® 631xESB/632xESB I/O Controller Hub when the last transfer for a region is performed, where EOT for that region is set in the region descriptor. It is also cleared by the Intel® 631xESB/632xESB I/O Controller Hub when the Start bit is cleared in the Command register. When this bit is read as 0, all data transferred from the drive during the previous bus master command is visible in system memory, unless the bus master command was aborted. 1 = Set by the Intel® 631xESB/632xESB I/O Controller Hub when the Start bit is written to the Command register.

22.2.3 BMIDP – Bus Master IDE Descriptor Table Pointer Register (IDE – D31:F1)

Address Offset: BMIBASE + 04h Attribute: R/W
Default Value: All bits undefined Size: 32 bits

Bit	Description
31:2	**Address of Descriptor Table (ADDR)** – R/W. Corresponds to A[31:2]. The Descriptor Table must be DWord-aligned. The Descriptor Table must not cross a 64-K boundary in memory.
1:0	Reserved

§§



23 SATA Controller Registers (D31:F2)

23.1 PCI Configuration Registers (SATA–D31:F2)

Note: Address locations that are not shown should be treated as Reserved.

All of the SATA registers are in the core well. None of the registers can be locked.

Table 23-1. SATA Controller PCI Register Address Map (SATA–D31:F2) (Sheet 1 of 2)

Offset	Mnemonic	Register Name	Default	Type
00–01h	VID	Vendor Identification	8086h	RO
02–03h	DID	Device Identification	See register description	RO
04–05h	PCICMD	PCI Command	0000h	R/W, RO
06–07h	PCISTS	PCI Status	02B0h	R/WC, RO
08h	RID	Revision Identification	See register description.	RO
09h	PI	Programming Interface	See register description.	See register description
0Ah	SCC	Sub Class Code	See register description	See register description
0Bh	BCC	Base Class Code	01h	RO
0Dh	PMLT	Primary Master Latency Timer	00h	RO
10–13h	PCMD_BAR	Primary Command Block Base Address	00000001h	R/W, RO
14–17h	PCNL_BAR	Primary Control Block Base Address	00000001h	R/W, RO
18–1Bh	SCMD_BAR	Secondary Command Block Base Address	00000001h	R/W, RO
1C–1Fh	SCNL_BAR	Secondary Control Block Base Address	00000001h	R/W, RO
20–23h	BAR	Legacy Bus Master Base Address	00000001h	R/W, RO
24–27h	ABAR	AHCI Base Address	00000000h	See register description
2C–2Dh	SVID	Subsystem Vendor Identification	0000h	R/WO
2E–2Fh	SID	Subsystem Identification	0000h	R/WO
34h	CAP	Capabilities Pointer	80h	RO
3C	INT_LN	Interrupt Line	00h	R/W
3D	INT_PN	Interrupt Pin	See register description.	RO
40–41h	IDE_TIMP	Primary IDE Timing	0000h	R/W
42–43h	IDE_TIMS	Secondary IDE Timing	0000h	R/W
44h	SIDETIM	Slave IDE Timing	00h	R/W
48h	SDMA_CNT	Synchronous DMA Control	00h	R/W
4A–4Bh	SDMA_TIM	Synchronous DMA Timing	0000h	R/W
54–57h	IDE_CONFIG	IDE I/O Configuration	00000000h	R/W

Table 23-1. SATA Controller PCI Register Address Map (SATA–D31:F2) (Sheet 2 of 2)

Offset	Mnemonic	Register Name	Default	Type
70–71h	PID	PCI Power Management Capability ID	0001h	RO
72–73h	PC	PCI Power Management Capabilities	4002h	RO
74–75h	PMCS	PCI Power Management Control and Status	0000h	R/W, RO, R/WC
80–81h	MID	Message Signaled Interrupt ID	7005h	RO
82–83h	MC	Message Signaled Interrupt Message Control	0000h	R/W, RO
84–87h	MA	Message Signaled Interrupt Message Address	00000000h	R/W
88–89h	MD	Message Signaled Interrupt Message Data	0000h	R/W
90h	MAP	Address Map	00h	R/W
91h–93h	PCS	Port Control and Status	0000h	R/W, RO, R/WC
A8h-ABh	SATACR0	Capability Register 0	00100012h	RO
ACh-AFh	SATACR1	Capability Register 1	00000048h	RO
C0h	ATC	APM Tapping Control Register	00h	R/W
C4h	ATS	APM Tapping Status Register	00h	R/WC
D0–D3h	SP	Scratch Pad	00000000h	R/W
E0h–E3h	BFCS	BIST FIS Control/Status	00000000h	R/W, R/WC
E4h–E7h	BFTD1	BIST FIS Transmit Data, DW1	00000000h	R/W
E8h–EBh	BFTD2	BIST FIS Transmit Data, DW2	00000000h	R/W

Note: The Intel® 631xESB/632xESB I/O Controller Hub SATA controller is not arbitrated as a PCI device, therefore it does not need a master latency timer.

23.1.1 VID – Vendor Identification Register (SATA – D31:F2)

Offset Address: 00–01h
Default Value: 8086h
Lockable: No
Attribute: RO
Size: 16 bit
Power Well: Core

Bit	Description
15:0	Vendor ID – RO. This is a 16-bit value assigned to Intel. Intel VID = 8086h

23.1.2 DID – Device Identification Register (SATA – D31:F2)

Offset Address: 02–03h
Default Value: See bits description
Lockable: No
Attribute: RO
Size: 16 bit
Power Well: Core

Bit	Description
15:0	**Device ID –** RO. This is a 16-bit value assigned to the Intel® 631xESB/632xESB I/O Controller Hub SATA controller, and this field is defined by the following: Bits Value: Bit[15:4] = 268h; Bit[3] = '0' ; Bit[2:0] = FDSATA fuse Refer to Table 2-33

23.1.3 PCICMD – PCI Command Register (SATA–D31:F2)

Address Offset: 04h–05h
Default Value: 0000h
Attribute: RO, R/W
Size: 16 bits

Bit	Description
15:11	Reserved
10	**Interrupt Disable** – R/W. This disables pin-based INTx# interrupts. This bit has no effect on MSI operation. 0 = Internal INTx# messages are generated if there is an interrupt and MSI is not enabled. 1 = Internal INTx# messages will not be generated.
9	Fast Back to Back Enable (FBE) – RO. Reserved as 0.
8	SERR# Enable **(SERR_EN) –** RO. Reserved as 0.
7	Wait Cycle Control (WCC) – RO. Reserved as 0.
6	**Parity Error Response (PER) –** R/W. 0 = Disabled. SATA controller will not generate PERR# when a data parity error is detected. 1 = Enabled. SATA controller will generate PERR# when a data parity error is detected.
5	VGA Palette Snoop (VPS) – RO. Reserved as 0.
4	Postable Memory Write Enable (PMWE) – RO. Reserved as 0.
3	Special Cycle Enable (SCE) – RO. Reserved as 0.
2	**Bus Master Enable (BME) –** R/W. This bit controls the ability to act as a PCI master for IDE Bus Master transfers. This bit does not impact the generation of completions for split transaction commands.
1	**Memory Space Enable (MSE) –** R/W / RO. Controls access to the SATA controller's target memory space (for AHCI). ***Note:*** When MAP.MV (offset 90:bits 1:0) is not 00h, this register is Read Only (RO). For Intel® 631xESB/632xESB I/O Controller Hub, this bit is RO '0'.
0	**I/O Space Enable (IOSE) –** R/W. This bit controls access to the I/O space registers. 0 = Disables access to the Legacy or Native IDE ports (both Primary and Secondary) as well as the Bus Master I/O registers. 1 = Enable. Note that the Base Address register for the Bus Master registers should be programmed before this bit is set.

23.1.4 PCISTS – PCI Status Register (SATA–D31:F2)

Address Offset: 06–07h
Default Value: 02B0h
Attribute: R/WC, RO
Size: 16 bits

Note: For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 to the bit has no effect.

Bit	Description
15	**Detected Parity Error (DPE)** – R/WC. 0 = No parity error detected by SATA controller. 1 = SATA controller detects a parity error on its interface.
14	**Signaled System Error (SSE)** – RO. Reserved as 0.
13	**Received Master Abort (RMA) –** R/WC. 0 = Master abort Not generated. 1 = SATA controller, as a master, generated a master abort.
12	Reserved as 0 **–** RO.
11	**Signaled Target Abort (STA)** – RO. Reserved as 0.
10:9	DEVSEL# Timing Status (DEV_STS) – RO. 01 = Hardwired; Controls the device select time for the SATA controller's PCI interface.

Bit	Description
8	**Data Parity Error Detected (DPED) –** RO. This bit can only be set on read completions received from SiBUS where there is a parity error. 1 = SATA controller, as a master, either detects a parity error or sees the parity error line asserted, and the parity error response bit (bit 6 of the command register) is set.
7	**Fast Back to Back Capable (FB2BC)** – RO. Reserved as 1.
6	**User Definable Features (UDF) –** RO. Reserved as 0.
5	**66MHz Capable (66MHZ_CAP) –** RO. Reserved as 1.
4	**Capabilities List (CAP_LIST) –** RO. This bit indicates the presence of a capabilities list. The minimum requirement for the capabilities list must be PCI power management for the SATA controller.
3	**Interrupt Status (INTS)** – RO. Reflects the state of INTx# messages. 0 = Interrupt is cleared (independent of the state of Interrupt Disable bit in the command register [offset 04h]). 1 = Interrupt is to be asserted
2:0	Reserved

23.1.5 RID – Revision Identification Register (SATA – D31:F2)

Offset Address: 08h Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Description
7:0	**Revision ID –** RO. Refer to Table 2-33 or the *Intel® 631xESB/632xESB I/O Controller Hub EDS Specification Update - NDA* for the value of the Revision ID Register

23.1.6 PI – Programming Interface Register (SATA–D31:F2)

23.1.6.1 When Sub Class Code Register (D31:F2:Offset 0Ah) = 01h

Address Offset: 09h Attribute: R/W, RO
Default Value: See bit description Size: 8 bits

Bit	Description
7	This read-only bit is a 1 to indicate that bus master operation is supported
6:4	Reserved. Will always return 0.
3	**Secondary Mode Native Capable (SNC)** – RO. 0 = Secondary controller only supports legacy mode. 1 = Secondary controller supports both legacy and native modes. When MAP.MV (D31:F2:Offset 90:bits 1:0) is any value other than 00b, this bit reports as a 0. When MAP.MV is 00b, this bit reports as a 1.

Bit	Description
2	**Secondary Mode Native Enable (SNE)** – R/W / RO. Determines the mode that the secondary channel is operating in. 0 = Secondary controller operating in legacy (compatibility) mode 1 = Secondary controller operating in native PCI mode. When MAP.MV (D31:F2:Offset 90:bits 1:0) is any value other than 00b, this bit is read-only (RO). When MAP.MV is 00b, this bit is read/write (R/W). If this bit is set by software, then the PNE bit (bit 0 of this register) must also be set by software. While in theory these bits can be programmed separately, such a configuration is not supported by hardware.
1	**Primary Mode Native Capable (PNC) –** RO. 0 = Primary controller only supports legacy mode. 1 = Primary controller supports both legacy and native modes. When MAP.MV (D31:F2:Offset 90:bits 1:0) is any value other than 00b, this bit reports as a 0. When MAP.MV is 00b, this bit reports as a 1
0	**Primary Mode Native Enable (PNE)** – R/W / RO. Determines the mode that the primary channel is operating in. 0 = Primary controller operating in legacy (compatibility) mode. 1 = Primary controller operating in native PCI mode. When MAP.MV (D31:F2:Offset 90:bits 1:0) is any value other than 00b, this bit is read-only (RO). When MAP.MV is 00b, this bit is read/write (R/W). If this bit is set by software, then the SNE bit (bit 2 of this register) must also be set by software. While in theory these bits can be programmed separately, such a configuration is not supported by hardware.

23.1.6.2 When Sub Class Code Register (D31:F2:Offset 0Ah) = 04h

Address Offset: 09h Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Description
7:0	Interface (IF) – RO. When configured as RAID, this register becomes read only '0'.

23.1.6.3 When Sub Class Code Register (D31:F2:Offset 0Ah) = 06h

Address Offset: 09h Attribute: RO
Default Value: 01h Size: 8 bits

Bit	Description
7:0	Interface (IF) – RO. Indicates the SATA Controller supports AHCI, rev 1.0.

23.1.7 SCC – Sub Class Code Register (SATA–D31:F2)

Address Offset: 0Ah Attribute: See bit description
Default Value: See bit description Size: 8 bits

Bit	Description
7:0	Sub Class Code (SCC) This field takes on one of several values, per the table below: SCC Register AttributeSCC Register Value RO 01h (IDE Controller)

23.1.8 BCC – Base Class Code Register (SATA–D31:F2)

Address Offset: 0Bh
Default Value: 01h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	Base Class Code (BCC) – RO. 01h = Mass storage device

23.1.9 PMLT – Primary Master Latency Timer Register (SATA–D31:F2)

Address Offset: 0Dh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	Master Latency Timer Count (MLTC) – RO. 00h = Hardwired. The SATA controller is implemented internally, and is not arbitrated as a PCI device, so it does not need a Master Latency Timer.

23.1.10 PCMD_BAR – Primary Command Block Base Address Register (SATA–D31:F2)

Address Offset: 10h–13h
Default Value: 00000001h
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31:16	Reserved
15:3	**Base Address –** R/W. This field provides the base address of the I/O space (8 consecutive I/O locations).
2:1	Reserved
0	Resource Type Indicator (RTE) **–** RO. Hardwired to 1 to indicate a request for I/O space.

Note: This 8-byte I/O space is used in native mode for the Primary Controller's Command Block.

23.1.11 PCNL_BAR – Primary Control Block Base Address Register (SATA–D31:F2)

Address Offset: 14h–17h
Default Value: 00000001h
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31:16	Reserved
15:2	**Base Address –** R/W. This field provides the base address of the I/O space (4 consecutive I/O locations).
1	Reserved
0	Resource Type Indicator (RTE) – RO. Hardwired to 1 to indicate a request for I/O space.

Note: This 4-byte I/O space is used in native mode for the Primary Controller's Command Block.

23.1.12 SCMD_BAR – Secondary Command Block Base Address Register (IDE D31:F1)

Address Offset: 18h–1Bh
Default Value: 00000001h
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31:16	Reserved
15:3	**Base Address –** R/W. This field provides the base address of the I/O space (8 consecutive I/O locations).
2:1	Reserved
0	Resource Type Indicator (RTE) – RO. Hardwired to 1 to indicate a request for I/O space.

Note: This 4-byte I/O space is used in native mode for the Secondary Controller's Command Block.

23.1.13 SCNL_BAR – Secondary Control Block Base Address Register (IDE D31:F1)

Address Offset: 1Ch–1Fh
Default Value: 00000001h
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31:16	Reserved
15:2	**Base Address –** R/W. This field provides the base address of the I/O space (4 consecutive I/O locations).
1	Reserved
0	Resource Type Indicator (RTE) – RO. Hardwired to 1 to indicate a request for I/O space.

Note: This 4-byte I/O space is used in native mode for the Secondary Controller's Command Block.

23.1.14 BAR – Legacy Bus Master Base Address Register (SATA–D31:F2)

Address Offset: 20h–23h
Default Value: 00000001h
Attribute: R/W, RO
Size: 32 bits

The Bus Master IDE interface function uses Base Address register 5 to request a 16-byte I/O space to provide a software interface to the Bus Master functions. Only 12 bytes are actually used (6 bytes for primary, 6 bytes for secondary). Only bits [15:4] are used to decode the address.

Bit	Description
31:16	Reserved
15:4	**Base Address –** R/W. This field provides the base address of the I/O space (16 consecutive I/O locations).
3:1	Reserved
0	Resource Type Indicator (RTE) **–** RO. Hardwired to 1 to indicate a request for I/O space.

23.1.15 ABAR – AHCI Base Address Register (SATA–D31:F2)

Address Offset: 24h–27h
Default Value: 00000000h
Attribute: RO
Size: 32 bits

Bit	Description
31:0	Reserved

23.1.16 SVID – Subsystem Vendor Identification Register (SATA–D31:F2)

Address Offset: 2Ch–2Dh
Default Value: 0000h
Lockable: No
Attribute: R/WO
Size: 16 bits
Power Well: Core

Bit	Description
15:0	**Subsystem Vendor ID (SVID) –** R/WO. Value is written by BIOS. No hardware action taken on this value.

23.1.17 SID – Subsystem Identification Register (SATA–D31:F2)

Address Offset: 2Eh–2Fh
Default Value: 0000h
Lockable: No
Attribute: R/WO
Size: 16 bits
Power Well: Core

Bit	Description
15:0	**Subsystem ID (SID)** – R/WO. Value is written by BIOS. No hardware action taken on this value.

23.1.18 CAP – Capabilities Pointer Register (SATA–D31:F2)

Address Offset: 34h
Default Value: 80h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	Capabilities Pointer (CAP_PTR) – RO. This bit indicates that the first capability pointer offset is 80h, the MSI capability.

23.1.19 INT_LN – Interrupt Line Register (SATA–D31:F2)

Address Offset: 3Ch
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	**Interrupt Line –** R/W. This field is used to communicate to software the interrupt line that the interrupt pin is connected to.

23.1.20 INT_PN – Interrupt Pin Register (SATA–D31:F2)

Address Offset:	3Dh	Attribute:	RO
Default Value:	See Register Description	Size:	8 bits

Bit	Description
7:0	Interrupt Pin – RO. This reflects the value of D31IP.SIP (Chipset Config Registers:Offset 3100h:bits 11:8).

23.1.21 IDE_TIM – IDE Timing Register (SATA–D31:F2)

Address Offset:	Primary: 40–41h Secondary: 42–43h	Attribute:	R/W
Default Value:	0000h	Size:	16 bits

This register controls the timings driven on the IDE cable for PIO and 8237 style DMA transfers. It also controls operation of the buffer for PIO transfers.

Note: This register is R/W to maintain software compatibility and enable parallel ATA functionality when the PCI functions are combined. These bits have no effect on SATA operation unless otherwise noted.

Bit	Description
15	**IDE Decode Enable (IDE) –** R/W. Individually enable/disable the Primary or Secondary decode. 0 = Disable. 1 = Enables the Intel® 631xESB/632xESB I/O Controller Hub to decode the associated Command Blocks (1F0–1F7h for primary, 170–177h for secondary) and Control Block (3F6h for primary and 376h for secondary). This bit effects the IDE decode ranges for both legacy and native-Mode decoding. ***Note:*** This bit affects SATA operation in both combined and non-combined ATA modes. See Section 5.22.1 for more on ATA modes of operation.
14	**Drive 1 Timing Register Enable (SITRE)** – R/W. 0 = Use bits 13:12, 9:8 for both drive 0 and drive 1. 1 = Use bits 13:12, 9:8 for drive 0, and use the Slave IDE Timing register for drive 1
13:12	**IORDY Sample Point (ISP) –** R/W. The setting of these bits determines the number of PCI clocks between IDE IOR#/IOW# assertion and the first IORDY sample point. 00 = 5 clocks 01 = 4 clocks 10 = 3 clocks 11 = Reserved
11:10	Reserved
9:8	**Recovery Time (RCT) –** R/W. The setting of these bits determines the minimum number of PCI clocks between the last IORDY sample point and the IOR#/IOW# strobe of the next cycle. 00 = 4 clocks 01 = 3 clocks 10 = 2 clocks 11 = 1 clock
7	**Drive 1 DMA Timing Enable (DTE1) –** R/W. 0 = Disable. 1 = Enable the fast timing mode for DMA transfers only for this drive. PIO transfers to the IDE data port will run in compatible timing.
6	**Drive 1 Prefetch/Posting Enable (PPE1) –** R/W. 0 = Disable. 1 = Enable Prefetch and posting to the IDE data port for this drive.
5	**Drive 1 IORDY Sample Point Enable (IE1) –** R/W. 0 = Disable IORDY sampling for this drive. 1 = Enable IORDY sampling for this drive.

Bit	Description
4	**Drive 1 Fast Timing Bank (TIME1) –** R/W. 0 = Accesses to the data port will use compatible timings for this drive. 1 = When this bit =1 and bit 14 = 0, accesses to the data port will use bits 13:12 for the IORDY sample point, and bits 9:8 for the recovery time. When this bit = 1 and bit 14 = 1, accesses to the data port will use the IORDY sample point and recover time specified in the slave IDE timing register.
3	**Drive 0 DMA Timing Enable (DTE0) –** R/W. 0 = Disable 1 = Enable fast timing mode for DMA transfers only for this drive. PIO transfers to the IDE data port will run in compatible timing.
2	**Drive 0 Prefetch/Posting Enable (PPE0) –** R/W. 0 = Disable prefetch and posting to the IDE data port for this drive. 1 = Enable prefetch and posting to the IDE data port for this drive.
1	**Drive 0 IORDY Sample Point Enable (IE0) –** R/W. 0 = Disable IORDY sampling is disabled for this drive. 1 = Enable IORDY sampling for this drive.
0	**Drive 0 Fast Timing Bank (TIME0) –** R/W. 0 = Accesses to the data port will use compatible timings for this drive. 1 = Accesses to the data port will use bits 13:12 for the IORDY sample point, and bits 9:8 for the recovery time

23.1.22 SIDETIM – Slave IDE Timing Register (SATA–D31:F2)

Address Offset: 44h
Default Value: 00h
Attribute: R/W
Size: 8 bits

Note: This register is R/W to maintain software compatibility and enable parallel ATA functionality when the PCI functions are combined. These bits have no effect on SATA operation unless otherwise noted.

Bit	Description
7:6	**Secondary Drive 1 IORDY Sample Point (SISP1) –** R/W. This field determines the number of PCI clocks between IDE IOR#/IOW# assertion and the first IORDY sample point, if the access is to drive 1 data port and bit 14 of the IDE timing register for secondary is set. 00 = 5 clocks 01 = 4 clocks 10 = 3 clocks 11 = Reserved
5:4	**Secondary Drive 1 Recovery Time (SRCT1) –** R/W. This field determines the minimum number of PCI clocks between the last IORDY sample point and the IOR#/IOW# strobe of the next cycle, if the access is to drive 1 data port and bit 14 of the IDE timing register for secondary is set. 00 = 4 clocks 01 = 3 clocks 10 = 2 clocks 11 = 1 clocks
3:2	**Primary Drive 1 IORDY Sample Point (PISP1) –** R/W. This field determines the number of PCI clocks between IOR#/IOW# assertion and the first IORDY sample point, if the access is to drive 1 data port and bit 14 of the IDE timing register for primary is set. 00 = 5 clocks 01 = 4 clocks 10 = 3 clocks 11 = Reserved
1:0	**Primary Drive 1 Recovery Time (PRCT1) –** R/W. This field determines the minimum number of PCI clocks between the last IORDY sample point and the IOR#/IOW# strobe of the next cycle, if the access is to drive 1 data port and bit 14 of the IDE timing register for primary is set. 00 = 4 clocks 01 = 3 clocks 10 = 2 clocks 11 = 1 clocks

23.1.23 SDMA_CNT – Synchronous DMA Control Register (SATA–D31:F2)

Address Offset:	48h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

Note: This register is R/W to maintain software compatibility and enable parallel ATA functionality when the PCI functions are combined. These bits have no effect on SATA operation unless otherwise noted.

Bit	Description
7:4	Reserved
3	**Secondary Device 1 ATAxx Enable: (SDAE1) –** R/W. 0 = Disables ATA33/66/100/133 timing modes for the secondary slave device. (default) 1 = Enables ATA33/66/100/133 timing modes for the secondary slave device.
2	**Secondary Device 0 ATAxx Enable: (SDAE0)** – R/W. 0 = Disables ATA33/66/100/133 timing modes for the secondary master device. (default) 1 = Enables ATA33/66/100/133 timing modes for the secondary master device.
1	**Primary Device 1 ATAxx Enable: (PDAE1)** – R/W. 0 = Disables ATA33/66/100/133 timing modes for the primary slave device. (default) 1 = Enables ATA33/66/100/133 timing modes for the primary slave device.
0	**Primary Device 0 ATAxx Enable: (PDAE0)** – R/W. 0 = Disables ATA33/66/100/133 timing modes for the primary master device. (default) 1 = Enables ATA33/66/100/133 timing modes for the primary master device.

23.1.24 SDMA_TIM – Synchronous DMA Timing Register (SATA–D31:F2)

Address Offset:	4A–4Bh	Attribute:	R/W
Default Value:	0000h	Size:	16 bits

Note: This register is R/W to maintain software compatibility and enable parallel ATA functionality when the PCI functions are combined. These bits have no effect on SATA operation, unless otherwise noted.

Bit	Description
15:14	Reserved
13:12	**Secondary Drive 1 Cycle Time (SCT1) –** R/W. For Ultra ATA mode. The setting of these bits determines the minimum write strobe cycle time (CT). The DMARDY#-to-STOP (RP) time is also determined by the setting of these bits. SBC[3] = 0 (33 MHz clk)SCB[3] = 1 (66 MHz clk)FAST_SCB[3] = 1 (133 MHz clk) 00 = CT 4 clocks, RP 6 clocks00 = Reserved00 = Reserved 01 = CT 3 clocks, RP 5 clocks01 = CT 3 clocks, RP 8 clocks01 = CT 3 clks, RP 16 clks 10 = CT 2 clocks, RP 4 clocks10 = CT 2 clocks, RP 8 clocks10 = Reserved 11 = Reserved 11 = Reserved11 = Reserved
11:10	Reserved
9:8	**Secondary Drive 0 Cycle Time (SCT0) –** R/W. Same definition as bits 13:12, except for device 0.
7:6	Reserved
5:4	**Primary Drive 1 Cycle Time (PCT1) –** R/W. Same definition as bits 13:12, except for primary device 1.
3:2	Reserved
1:0	**Primary Drive 0 Cycle Time (PCT0) –** R/W. Same definition as bits 13:12, except for primary device 0.

23.1.25 IDE_CONFIG – IDE I/O Configuration Register (SATA–D31:F2)

Address Offset: 54h–57h
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

Note: This register is R/W to maintain software compatibility and enable parallel ATA functionality when the PCI functions are combined. These bits have no effect on SATA operation, unless otherwise noted.

Bit	Description
31:24	Reserved
23:20	**Scratchpad (SP2).** Intel® 631xESB/632xESB I/O Controller Hub does not perform any actions on these bits.
19:18	**Secondary Signals Mode (SSM): –** R/W. These bits are used to control mode of the Secondary IDE signal pins for swap bay support. If the SRS bit (Chipset Config Registers:Offset 3414h:bit 1) is 1, the reset states of bits 19:18 will be 01 (tri-state) instead of 00 (normal). 00 = Normal (Enabled) 01 = Tri-state (Disabled) 10 = Drive low (Disabled) 11 = Reserved
17:16	**Primary Signals Mode (PSM): –** R/W. These bits are used to control mode of the Primary IDE signal pins for swap bay support. If the PRS bit (Chipset Config Registers:Offset 3414h:bit 1) is 1, the reset states of bits 17:16 will be 01 (tri-state) instead of 00 (normal). 00 = Normal (Enabled) 01 = Tri-state (Disabled) 10 = Drive low (Disabled) 11 = Reserved
15:12	Fast Synchronous Base Clock Enable (FSBCE): 0 = Disables fast ATA modes. 1 = Enables fast ATA modes. This overrides the state of the SCB[3:0] bits in this register.
11:8	Reserved
7:4	Scratchpad (SP1). Intel® 631xESB/632xESB I/O Controller Hub does not perform any action on these bits.
3:0	**Synchronous Base Clock (SBC):** Clock used to determine CT and RP timings for synchronous DMA timings. 0 = 33 MHz clock used, 1 = 66 MHz clock used. Bit 3 controls the secondary slave device, bit 2 controls the secondary master device, bit 1 controls the primary slave device, and bit 0 controls the primary master device.

23.1.26 PID – PCI Power Management Capability Identification Register (SATA–D31:F2)

Address Offset: 70–71h
Default Value: 0001h
Attribute: RO
Size: 16 bits

Bits	Description
15:8	Next Capability (NEXT) – RO. Indicates that this is the last item in the list.
7:0	Capability ID (CID) – RO. Indicates that this pointer is a PCI power management.

23.1.27 PC – PCI Power Management Capabilities Register (SATA–D31:F2)

Address Offset: 72–73h
Default Value: 4002h
Attribute: RO
Size: 16 bits

Bits	Description
15:11	PME Support (PME_SUP) – RO. Indicates PME# can be generated from the $D3_{HOT}$ state in the SATA host controller.
10	D2 Support (D2_SUP) – RO. Hardwired to 0. The D2 state is not supported
9	D1 Support (D1_SUP) – RO. Hardwired to 0. The D1 state is not supported
8:6	Auxiliary Current (AUX_CUR) – RO. Hardwired to 000 to indicate 375 mA maximum Suspend well current required when in the $D3_{COLD}$ state.
5	Device Specific Initialization (DSI) – RO. Hardwired to 0 to indicate that no device-specific initialization is required.
4	Reserved
3	PME Clock (PME_CLK) – RO. Hardwired to 0 to indicate that PCI clock is not required to generate PME#.
2:0	Version (VER) – RO. Hardwired to 010 to indicates support for Revision 1.1 of the *PCI Power Management Specification*.

23.1.28 PMCS – PCI Power Management Control and Status Register (SATA–D31:F2)

Address Offset: 74–75h
Default Value: 0000h
Attribute: RO, R/W, R/WC
Size: 16 bits

Bits	Description
15	**PME Status (PMES)** – R/WC. Bit is set when a PME event is to be requested, and if this bit and PMEE is set, a PME# will be generated from the SATA controller
14:9	Reserved
8	**PME Enable (PMEE)** – R/W. When set, the SATA controller generates PME# form $D3_{HOT}$ on a wake event.
7:2	Reserved
1:0	**Power State (PS)** – R/W. These bits are used both to determine the current power state of the SATA controller and to set a new power state. 00 = D0 state 11 = $D3_{HOT}$ state When in the $D3_{HOT}$ state, the controller's configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked.

23.1.29 MID – Message Signaled Interrupt Identifiers Register (SATA–D31:F2)

Address Offset: 80–81h
Default Value: 7005h
Attribute: RO
Size: 16 bits

Bits	Description
15:8	**Next Pointer (NEXT) –** RO. This field indicates that the next item in the list the PCI power management pointer.
7:0	**Capability ID (CID) –** RO. The Capabilities ID indicates MSI.

23.1.30 MC – Message Signaled Interrupt Message Control Register (SATA–D31:F2)

Address Offset: 82–83h
Default Value: 0000h
Attribute: RO, R/W
Size: 16 bits

Bits	Description
15:8	Reserved
7	**64 Bit Address Capable (C64)** – RO. Capability of generating 32-bit messages only.
6:4	**Multiple Message Enable (MME)** – R/W. These bits are R/W for software compatibility, but only one message is ever sent by Intel® 631xESB/632xESB I/O Controller Hub.
3:1	**Multiple Message Capable (MMC) –** RO. Only one message is required.
0	**MSI Enable (MSIE) –** R/W. 0 = Disabled. 1 = MSI is enabled and traditional interrupt pins are not used to generate interrupts.

23.1.31 MA – Message Signaled Interrupt Message Address Register (SATA–D31:F2)

Address Offset: 84–87h
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

Bits	Description
31:2	**Address (ADDR)** – R/W. Lower 32 bits of the system specified message address, always DWord aligned.
1:0	Reserved

23.1.32 MD – Message Signaled Interrupt Message Data Register (SATA–D31:F2)

Address Offset: 88–89h
Default Value: 0000h
Attribute: R/W
Size: 16 bits

Bits	Description
15:0	**Data (DATA)** – R/W. This field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD[15:0]) during the data phase of the MSI memory write transaction.

23.1.33 MAP – Port Mapping Register (SATA–D31:F2)

Address Offset: 90h
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bits	Description
7:6	**SATA Mode Select:** Software programs these bits to control the mode in which the SATA HBA should operate: 00 IDE mode 01 AHCI Mode 10 RAID mode 11 Reserved NOTES: 1. When combined mode is used (non-zero MV), only IDE mode is allowed. IDE mode can be selected when RAID is enabled. 2. AHCI mode may only be selected when MV=0. AHCI mode may be selected when RAID is enabled. 3. RAID mode may only be selected when MV=0. Note that RAID5 mode may not be supported in certain SKUs of Intel® 631xESB/632xESB I/O Controller Hub. Programming these bits with values that are illegal (for example, selecting RAID when in combined mode) will result in-deterministic behavior by the hardware.
5:2	Reserved.
1:0	**Map Value –** R/W. Map Value (MV): The value in the bits below indicate the address range the SATA ports responds to, and whether or not the PATA and SATA functions are combined. When in combined mode, the AHCI memory space is not available and AHCI may not be used. 00 = Non-combined. P0 is primary master, P2 is the primary slave, P1 is secondary master, P3 is the secondary slave. 01 = Combined. IDE is primary. P1 is secondary master, P3 is the secondary slave. 10 = Combined. P0 is primary master. P2 is primary slave. IDE is secondary 11 = Reserved

23.1.34 PCS – Port Control and Status Register (SATA–D31:F2)

Address Offset: 91h–93h
Default Value: 0000h
Attribute: R/W, R/WC, RO
Size: 24 bits

Bits	Description
23:21	Reserved.
20	**OOB Retry Mode**: 0 = The SATA controller will not retry after an OOB failure. 1 = The SATA controller will continue to retry after an OOB failure until successful (infinite retry).
19:16	Reserved.
15	**Port 3 Present (P3P) –** RO. Same as P0P, except for port 3.
14	**Port 2 Present (P2P) –** RO. Same as P0P, except for port 2.
13	**Port 1 Present (P1P) –** RO. Same as P0P, except for port 1.
12	**Port 0 Present (P0P) –** RO. When set, the SATA controller has detected the presence of a device on port 0. It may change at any time. This bit is cleared when the port is disabled via P0E. This bit is not cleared upon surprise removal of a device.
11	**Port 3 Enabled (P3E)** – R/W. 0 = Disabled. The port is in the 'off' state and cannot detect any devices. 1 = Enabled. The port can transition between the on, partial, and slumber states and can detect devices. ***Note:*** This bit takes precedence over P2CMD.SUD (offset ABAR+298h:bit 1)

Bits	Description
10	**Port 2 Enabled (P2E)** – R/W. 0 = Disabled. The port is in the 'off' state and cannot detect any devices. 1 = Enabled. The port can transition between the on, partial, and slumber states and can detect devices. ***Note:*** This bit takes precedence over P2CMD.SUD (offset ABAR+218h:bit 1)
9	**Port 1 Enabled (P1E)** – R/W. 0 = Disabled. The port is in the 'off' state and cannot detect any devices. 1 = Enabled. The port can transition between the on, partial, and slumber states and can detect devices. ***Note:*** This bit takes precedence over P1CMD.SUD (offset ABAR+198h:bit 1)
8	**Port 0 Enabled (P0E)** – R/W. 0 = Disabled. The port is in the 'off' state and cannot detect any devices. 1 = Enabled. The port can transition between the on, partial, and slumber states and can detect devices. ***Note:*** This bit takes precedence over P0CMD.SUD (offset ABAR+118h:bit 1)
7:4	Reserved
3	**Port 5Present (**P5P**) –** RO. When set, the SATA controller has detected the presence of a device on port 5. It may change at any time. This bit is cleared when the port is disabled via P5E. This bit is not cleared upon surprise removal of a device.
2	**Port 4Present (P4P) –** RO. When set, the SATA controller has detected the presence of a device on port 4. It may change at any time. This bit is cleared when the port is disabled via P4E. This bit is not cleared upon surprise removal of a device.
1	**Port 5Enabled (P5E)** – R/W. The definition of this bit is the same as P0E, except for port 5. This bit takes precedence over P5CMD.SUD.
0	**Port 4 Enabled (P4E)** – R/W. The definition of this bit is the same as P0E, except for port 4. This bit takes precedence over P4CMD.SUD.

23.1.35 SATACR0 – Capability Register 0 (SATA–D31:F2)

Address Offset: A8h–ABh
Default Value: 00100012h

Attribute: RO
Size: 32 bits

Bit	Description
31:24	Reserved
23:20	**MAJOR Revision (MAJREV) –** RO: Specifies the major revision level to which the SATA HBA has been built.
19:16	**Minor Revision (MINREV) –** RO: Specifies the minor revision level to which the SATA HBA has been built.
15:08	**Next Capability Pointer (NEXT) –** RO: Pints to the next capability structure. 00h indicates this is the last capability pointer.
7:0	**Capability ID (CAP) –** RO: This value of 12h has been assigned by the PCI SIG to designate the SATA Capability Structure.

23.1.36 SATACR1 – Capability Register 1 (SATA–D31:F2)

Address Offset: ACh–AFh
Default Value: 00000048h
Attribute: RO
Size: 32 bits

Bit	Description
31:16	Reserved
15:04	**BAR Offset (BAROFST) –** RO: Indicates the offset into the BAR where the Index/Data pair are located (in Dword granularity). The Index and Data registers are located at offset 10h within the I/O space defined by LBAR. A value of 004h indicates offset 10h.
03:00	**BAR Location (BARLOC) –** RO: Indicates the offset of the BAR containing the Index/Data pair (in Dword granularity). The index and Data I/O registers reside within the space defined by LBAR in the SATA controller. A value of 8h indicates offset 20h which is LBAR. LBAR is the BAR location for Index/Data registers.

23.1.37 ATC – APM Trapping Control Register (SATA–D31:F2)

Address Offset: C0h
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:4	Reserved
3	**Secondary Slave Trap (SST) –** R/W. Enables trapping and SMI# assertion on legacy I/O accesses to 170h-177h and 376h. The active device on the secondary interface must be device 1 for the trap and/or SMI# to occur.
2	**Secondary Master Trap (SPT) –** R/W. Enables trapping and SMI# assertion on legacy I/O accesses to 170h-177h and 376h. The active device on the secondary interface must be device 0 for the trap and/or SMI# to occur.
1	**Primary Slave Trap (PST) –** R/W. Enables trapping and SMI# assertion on legacy I/O accesses to 1F0h-1F7h and 3F6h. The active device on the primary interface must be device 1 for the trap and/or SMI# to occur.
0	**Primary Master Trap (PMT) –** R/W. Enables trapping and SMI# assertion on legacy I/O accesses to 1F0h-1F7h and 3F6h. The active device on the primary interface must be device 0 for the trap and/or SMI# to occur.

23.1.38 ATS – APM Trapping Status Register (SATA–D31:F2)

Address Offset: C4h
Default Value: 00h
Attribute: R/WC
Size: 8 bits

Bit	Description
7:4	Reserved
3	**Secondary Slave Trap (SST) –** R/WC. Indicates that a trap occurred to the secondary slave device.
2	**Secondary Master Trap (SPT) –** R/WC. Indicates that a trap occurred to the secondary master device.
1	**Primary Slave Trap (PST) –** R/WC. Indicates that a trap occurred to the primary slave device.
0	**Primary Master Trap (PMT) –** R/WC. Indicates that a trap occurred to the primary master device.

23.1.39 SP Scratch Pad Register (SATA–D31:F2)

Address Offset: D0h
Default Value: 00h
Attribute: R/W
Size: 32 bits

Bit	Description
31:0	**Data (DT) –** R/W. This is a read/write register that is available for software to use. No hardware action is taken on this register.

23.1.40 BFCS – BIST FIS Control/Status Register (SATA–D31:F2)

Address Offset: E0h–E3h
Default Value: 00000000h
Attribute: R/W, R/WC
Size: 32 bits

Bits	Description
31:16	Reserved
15	**Port 5 BIST FIS Initiate (P5BFI)** – R/W. When a rising edge is detected on this bit field, the Intel® 631xESB/632xESB I/O Controller Hub initiates a BIST FIS to the device on Port 5, using the parameters specified in this register and the data specified in BFTD1 and BFTD2. The BIST FIS will only be initiated if a device on Port 5 is present and ready (not partial/slumber state). After a BIST FIS is successfully completed, software must disable and re-enable the port using the PxE bits at offset 92h prior to attempting additional BIST FISes or to return the Intel® 631xESB/632xESB I/O Controller Hub to a normal operational mode. If the BIST FIS fails to complete, as indicated by the BFF bit in the register, then software can clear then set the P5BFI bit to initiate another BIST FIS. This can be retried until the BIST FIS eventually completes successfully
14	**Port 4 BIST FIS Initiate (P4BFI)** – R/W. When a rising edge is detected on this bit field, the Intel® 631xESB/632xESB I/O Controller Hub initiates a BIST FIS to the device on Port 4, using the parameters specified in this register and the data specified in BFTD1 and BFTD2. The BIST FIS will only be initiated if a device on Port 4 is present and ready (not partial/slumber state). After a BIST FIS is successfully completed, software must disable and re-enable the port using the PxE bits at offset 92h prior to attempting additional BIST FISes or to return the Intel® 631xESB/632xESB I/O Controller Hub to a normal operational mode. If the BIST FIS fails to complete, as indicated by the BFF bit in the register, then software can clear then set the P4BFI bit to initiate another BIST FIS. This can be retried until the BIST FIS eventually completes successfully
13	**Port 3 BIST FIS Initiate (P3BFI)** – R/W. When a rising edge is detected on this bit field, the Intel® 631xESB/632xESB I/O Controller Hub initiates a BIST FIS to the device on Port 3, using the parameters specified in this register and the data specified in BFTD1 and BFTD2. The BIST FIS will only be initiated if a device on Port 3 is present and ready (not partial/slumber state). After a BIST FIS is successfully completed, software must disable and re-enable the port using the PxE bits at offset 92h prior to attempting additional BIST FISes or to return the Intel® 631xESB/632xESB I/O Controller Hub to a normal operational mode. If the BIST FIS fails to complete, as indicated by the BFF bit in the register, then software can clear then set the P3BFI bit to initiate another BIST FIS. This can be retried until the BIST FIS eventually completes successfully
12	**Port 2 BIST FIS Initiate (P2BFI)** – R/W. When a rising edge is detected on this bit field, the Intel® 631xESB/632xESB I/O Controller Hub initiates a BIST FIS to the device on Port 2, using the parameters specified in this register and the data specified in BFTD1 and BFTD2. The BIST FIS will only be initiated if a device on Port 2 is present and ready (not partial/slumber state). After a BIST FIS is successfully completed, software must disable and re-enable the port using the PxE bits at offset 92h prior to attempting additional BIST FISes or to return the Intel® 631xESB/632xESB I/O Controller Hub to a normal operational mode. If the BIST FIS fails to complete, as indicated by the BFF bit in the register, then software can clear then set the P2BFI bit to initiate another BIST FIS. This can be retried until the BIST FIS eventually completes successfully
11	**BIST FIS Successful (BFS)** – R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = This bit is set any time a BIST FIS transmitted by Intel® 631xESB/632xESB I/O Controller Hub receives an R_OK completion status from the device. ***Note:*** This bit must be cleared by software prior to initiating a BIST FIS.
10	**BIST FIS Failed (BFF)** – R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = This bit is set any time a BIST FIS transmitted by Intel® 631xESB/632xESB I/O Controller Hub receives an R_ERR completion status from the device. ***Note:*** This bit must be cleared by software prior to initiating a BIST FIS.

Bits	Description
9	**Port 1 BIST FIS Initiate (P1BFI)** – R/W. When a rising edge is detected on this bit field, the Intel® 631xESB/632xESB I/O Controller Hub initiates a BIST FIS to the device on Port 1, using the parameters specified in this register and the data specified in BFTD1 and BFTD2. The BIST FIS will only be initiated if a device on Port 1 is present and ready (not partial/slumber state). After a BIST FIS is successfully completed, software must disable and re-enable the port using the PxE bits at offset 92h prior to attempting additional BIST FISes or to return the Intel® 631xESB/632xESB I/O Controller Hub to a normal operational mode. If the BIST FIS fails to complete, as indicated by the BFF bit in the register, then software can clear then set the P1BFI bit to initiate another BIST FIS. This can be retried until the BIST FIS eventually completes successfully
8	**Port 0 BIST FIS Initiate (P0BFI)** – R/W. When a rising edge is detected on this bit field, the Intel® 631xESB/632xESB I/O Controller Hub initiates a BIST FIS to the device on Port 0, using the parameters specified in this register and the data specified in BFTD1 and BFTD2. The BIST FIS will only be initiated if a device on Port 0 is present and ready (not partial/slumber state). After a BIST FIS is successfully completed, software must disable and re-enable the port using the PxE bits at offset 92h prior to attempting additional BIST FISes or to return the Intel® 631xESB/632xESB I/O Controller Hub to a normal operational mode. If the BIST FIS fails to complete, as indicated by the BFF bit in the register, then software can clear then set the P0BFI bit to initiate another BIST FIS. This can be retried until the BIST FIS eventually completes successfully
7:2	**BIST FIS Parameters**. These 6 bits form the contents of the upper 6 bits of the BIST FIS Pattern Definition in any BIST FIS transmitted by the Intel® 631xESB/632xESB I/O Controller Hub. This field is not port specific – its contents will be used for any BIST FIS initiated on port 0, port 1, port 2 or port 3. The specific bit definitions are: Bit 7: T – Far End Transmit mode Bit 6: A – Align Bypass mode Bit 5: S – Bypass Scrambling Bit 4: L – Far End Retimed Loopback Bit 3: F – Far End Analog Loopback Bit 2: P – Primitive bit for use with Transmit mode
1:0	Reserved

23.1.41 BFTD1 – BIST FIS Transmit Data1 Register (SATA–D31:F2)

Address Offset: E4h–E7h Attribute: R/W
Default Value: 00000000h Size: 32 bits

Bits	Description
31:0	**BIST FIS Transmit Data 1** – R/W. The data programmed into this register will form the contents of the second DWord of any BIST FIS initiated by the Intel® 631xESB/632xESB I/O Controller Hub. This register is not port specific – its contents will be used for BIST FIS initiated on any port. Although the 2nd and 3rd DWs of the BIST FIS are only meaningful when the “T” bit of the BIST FIS is set to indicate “Far-End Transmit mode”, this register’s contents will be transmitted as the BIST FIS 2nd DW regardless of whether or not the “T” bit is indicated in the BFCS register (D31:F2:E0h).

23.1.42 BFTD2 – BIST FIS Transmit Data2 Register (SATA–D31:F2)

Address Offset: E8h–EBh Attribute: R/W
Default Value: 00000000h Size: 32 bits

Bits	Description
31:0	**BIST FIS Transmit Data 2 –** R/W. The data programmed into this register will form the contents of the third DWord of any BIST FIS initiated by the Intel® 631xESB/632xESB I/O Controller Hub. This register is not port specific – its contents will be used for BIST FIS initiated on any port. Although the 2nd and 3rd DWs of the BIST FIS are only meaningful when the “T” bit of the BIST FIS is set to indicate “Far-End Transmit mode”, this register’s contents will be transmitted as the BIST FIS 3rd DW regardless of whether or not the “T” bit is indicated in the BFCS register (D31:F2:E0h).

23.2 Bus Master IDE I/O Registers (D31:F2)

The bus master IDE function uses 16 bytes of I/O space, allocated via the BAR register, located in Device 31:Function 2 Configuration space, offset 20h. All bus master IDE I/O space registers can be accessed as byte, word, or DWord quantities. Reading reserved bits returns an indeterminate, inconsistent value, and writes to reserved bits have no affect (but should not be attempted). These registers are only used for legacy operation. Software must not use these registers when running AHCI. The description of the I/O registers is shown in Table 23-2.

Table 23-2. Bus Master IDE I/O Register Address Map

BAR+ Offset	Mnemonic	Register	Default	Type
00	BMICP	Command Register Primary	00h	R/W
01	–	Reserved	–	RO
02	BMISP	Bus Master IDE Status Register Primary	00h	R/W, R/WC, RO
03	–	Reserved	–	RO
04–07	BMIDP	Bus Master IDE Descriptor Table Pointer Primary	xxxxxxxx	R/W
08	BMICS	Command Register Secondary	00h	R/W
09	–	Reserved	–	RO
0Ah	BMISS	Bus Master IDE Status Register Secondary	00h	R/W, R/WC, RO
0Bh	–	Reserved	–	RO
0Ch–0Fh	BMIDS	Bus Master IDE Descriptor Table Pointer Secondary	xx	R/W
10h-13h	BMINDEX	Bus Master AHCI Index	00000000h	RO,RW
14h-17h	BMDATA	Bus Master AHCI Data	See register description	RW

23.2.1 BMIC[P,S] – Bus Master IDE Command Register (D31:F2)

Address Offset: Primary: BAR + 00h, Secondary: BAR + 08h
Attribute: R/W
Default Value: 00h
Size: 8 bits

Bit	Description
7:4	Reserved. Returns 0.

Bit	Description
3	**Read / Write Control (RWC) –** R/W. This bit sets the direction of the bus master transfer: This bit must NOT be changed when the bus master function is active. 0 = Memory reads 1 = Memory writes
2:1	Reserved. Returns 0.
0	**Start/Stop Bus Master (START) –** R/W. 0 = All state information is lost when this bit is cleared. Master mode operation cannot be stopped and then resumed. If this bit is reset while bus master operation is still active (that is, the Bus Master IDE Active bit (D31:F2:BAR + 02h, bit 0) of the Bus Master IDE Status register for that IDE channel is set) and the drive has not yet finished its data transfer (the Interrupt bit in the Bus Master IDE Status register for that IDE channel is not set), the bus master command is said to be aborted and data transferred from the drive may be discarded instead of being written to system memory. 1 = Enables bus master operation of the controller. Bus master operation does not actually start unless the Bus Master Enable bit (D31:F1:04h, bit 2) in PCI configuration space is also set. Bus master operation begins when this bit is detected changing from 0 to 1. The controller will transfer data between the IDE device and memory only when this bit is set. Master operation can be halted by writing a 0 to this bit. ***Note:*** This bit is intended to be cleared by software after the data transfer is completed, as indicated by either the Bus Master IDE Active bit being cleared or the Interrupt bit of the Bus Master IDE Status register for that IDE channel being set, or both. Hardware does not clear this bit automatically. If this bit is cleared to '0' prior to the DMA data transfer being initiated by the drive in a device to memory data transfer, then the Intel® 631xESB/ 632xESB I/O Controller Hub will not send DMAT to terminate the data transfer. SW intervention (for example, sending SRST) is required to reset the interface in this condition.

23.2.2 BMIS[P,S] – Bus Master IDE Status Register (D31:F2)

Address Offset:	Primary: BAR + 02h Secondary: BAR + 0Ah	Attribute:	R/W, R/WC, RO
Default Value:	00h	Size:	8 bits

Bit	Description
7	**PRD Interrupt Status (PRDIS)** – R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = This bit is set when the host controller execution of a PRD that has its PRD_INT bit set.
6	**Drive 1 DMA Capable –** R/W. 0 = Not Capable. 1 = Capable. Set by device dependent code (BIOS or device driver) to indicate that drive 1 for this channel is capable of DMA transfers, and that the controller has been initialized for optimum performance. This bit is not used. It is intended for systems that do not attach BMIDE to the PCI bus.
5	**Drive 0 DMA Capable –** R/W. 0 = Not Capable 1 = Capable. Set by device dependent code (BIOS or device driver) to indicate that drive 0 for this channel is capable of DMA transfers, and that the controller has been initialized for optimum performance. This bit is not used. It is intended for systems that do not attach BMIDE to the PCI bus.
4:3	Reserved. Returns 0.

Bit	Description
2	**Interrupt –** R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = Set when a device FIS is received with the 'I' bit set, provided that software has not disabled interrupts via the nIEN bit of the Device Control Register (see chapter 5 of the *Serial ATA Specification*, Revision 1.0a).
1	**Error –** R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = This bit is set when the controller encounters a target abort or master abort when transferring data on PCI.
0	**Bus Master IDE Active (ACT)** – RO. 0 = This bit is cleared by the Intel® 631xESB/632xESB I/O Controller Hub when the last transfer for a region is performed, where EOT for that region is set in the region descriptor. It is also cleared by the Intel® 631xESB/632xESB I/O Controller Hub when the Start Bus Master bit (D31:F2:BAR+ 00h, bit 0) is cleared in the Command register. When this bit is read as a 0, all data transferred from the drive during the previous bus master command is visible in system memory, unless the bus master command was aborted. 1 = Set by the Intel® 631xESB/632xESB I/O Controller Hub when the Start bit is written to the Command register.

23.2.3 BMID[P,S] – Bus Master IDE Descriptor Table Pointer Register (D31:F2)

Address Offset:	Primary: BAR + 04h–07h Secondary: BAR + 0Ch–0Fh	Attribute:	R/W
Default Value:	All bits undefined	Size:	32 bits

Bit	Description
31:2	**Address of Descriptor Table (ADDR)** – R/W. The bits in this field correspond to A[31:2]. The Descriptor Table must be DWord-aligned. The Descriptor Table must not cross a 64-K boundary in memory.
1:0	Reserved

23.2.4 BMINDEX[P,S] – Bus Master Indirect AHCI Index Register Register (D31:F2)

Address Offset:	BAR + 10h–13h	Attribute:	RW, RO
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:10	Reserved
09:02	**Index:** This index register is used to select the Dword offset of the Memory Mapped AHCI register to be accessed. A Dword, Word or Byte access is specified by the active byte enables of the I/O access to the Data register.
1:0	Reserved

23.2.5 BMDATA[P,S] – Bus Master Indirect AHCI Data Register Register (D31:F2)

Address Offset:	BAR + 14h–17h	Attribute:	RW
Default Value:	See register description	Size:	32 bits

Bit	Description
31:00	**Data:** The data register is a "window" through which data is read or written to the memory mapped register pointed to by the index register. A physical register is not actually implemented as the data is actually stored in the memory mapped registers. Since this is not a physical register, the "default" value is the same as the default value of the register pointed to by index.

23.3 AHCI Registers (D31:F2)

The memory mapped registers within the SATA controller exist in non-cacheable memory space. Additionally, locked accesses are not supported. If software attempts to perform locked transactions to the registers, indeterminate results may occur. Register accesses shall have a maximum size of 64-bits; 64-bit access must not cross an 8-byte alignment boundary.

The registers are broken into two sections – generic host control and port control. The port control registers are the same for all ports, and there are as many registers banks as there are ports.

Table 23-3. AHCI Register Address Map

ABAR + Offset	Mnemonic	Register
00–1F	GHC	Generic Host Control
20–FF	–	Reserved
100–17F	P0PCR	Port 0 port control registers
180–1FF	P1PCR	Port 1 port control registers
200–27F	P2PCR	Port 2 port control registers
280–2FF	P3PCR	Port 3 port control registers
300–37F	P4PCR	Port 4 port control registers
380–3FF	P5PCR	Port 5 port control registers

23.3.1 AHCI Generic Host Control Registers (D31:F2)

Table 23-4. Generic Host Controller Register Address Map

ABAR + Offset	Mnemonic	Register	Default	Type
00–03	CAP	Host Capabilities	C6001F03h	R/WO, RO
04–07	GHC	Global Intel® 631xESB/632xESB I/O Controller Hub Control	00000000h	R/W
08–0B	IS	Interrupt Status	00000000h	R/WC
0C–0F	PI	Ports Implemented	00000000h	R/WO
10-13	VS	AHCI Version	00010000h	RO

23.3.1.1 CAP – Host Capabilities Register (D31:F2)

Address Offset:	ABAR + 00h–03h	Attribute:	R/WO, RO
Default Value:	C6001F03h	Size:	32 bits

All bits in this register that are R/WO are reset only by PLTRST#.

Bit	Description
31	**Supports 64-bit Addressing (S64A)** – RO. Indicates that the SATA controller can access 64-bit data structures. The 32-bit upper bits of the port DMA Descriptor, the PRD Base, and each PRD entry are read/write.
30	**Supports Command Queue Acceleration (SCQA) –** RO. Hardwired to 1 to indicate that the SATA controller supports SATA command queuing via the DMA Setup FIS. The Intel® 631xESB/632xESB I/O Controller Hub handles DMA Setup FISes natively, and can handle auto-activate optimization through that FIS.
29	Reserved.
28	**Supports Interlock Switch (SIS) –** R/WO. Indicates whether the SATA controller supports interlock switches on its ports for use in Hot-Plug operations. This value is loaded by platform BIOS prior to OS initialization. If this bit is set, BIOS must also map the SATAGP pins to the SATA controller through GPIO space.
27	**Supports Staggered Spin-up (SSS) –** R/WO. Indicates whether the SATA controller supports staggered spin-up on its ports, for use in balancing power spikes. This value is loaded by platform BIOS prior to OS initialization. 0 = Staggered spin-up not supported. 1 = Staggered spin-up supported.
26	**Supports Aggressive Link Power Management (SALP) –** RO. Hardwired to 1 to indicate that the SATA controller supports auto-generating link requests to the partial or slumber states when there are no commands to process.
25	**Supports Activity LED (SAL)** – RO. Indicates that the SATA controller supports a single output pin (SATALED#) which indicates activity.
24	Reserved.
23:20	**Interface Speed Support (ISS)** – RO. Indicates the maximum speed the SATA controller can support on its ports. 0h =1.5 Gb/s.
19	**Supports Non-Zero DMA Offsets (SNZO)** – RO. Reserved, as per the *AHCI Specification Revision 1.0*
18	Reserved.
17	**Supports Port Multiplier (PMS)** – R/WO. Port multiplier not supported. BIOS/SW shall write this bit to '0' during AHCI initialization.
16	Supports Port Multiplier FIS Based Switching (PMFS) – RO. Reserved, as per the *AHCI Specification Revision 1.0*
15	Reserved. Returns 0.
14	Slumber State Capable (SSC) – RO. The SATA controller supports the slumber state.
13	Partial State Capable (PSC) – RO. The SATA controller supports the partial state.
12:8	Number of Command Slots (NCS) – RO. Hardwired to 1Fh to indicate support for 32 slots.
7:5	Reserved. Returns 0.
4:0	Number of Ports (NPS) – RO. Hardwired to 5h to indicate support for 6 ports. Note that the number of ports indicated in this field may be more than the number of ports indicated in the PI (ABAR + 0Ch) register.

23.3.1.2 GHC – Global Intel® 631xESB/632xESB I/O Controller Hub Control Register (D31:F2)

Address Offset: ABAR + 04h–07h
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

Bit	Description
31	**AHCI Enable (AE)** – R/W. When set, indicates that an AHCI driver is loaded and the controller will be talked to via AHCI mechanisms. This can be used by an Intel® 631xESB/632xESB I/O Controller Hub that supports both legacy mechanisms (such as SFF-8038i) and AHCI to know when the controller will not be talked to as legacy. When set, software will only talk to the Intel® 631xESB/632xESB I/O Controller Hub using AHCI. The Intel® 631xESB/632xESB I/O Controller Hub will not have to allow command processing via both AHCI and legacy mechanisms. When cleared, software will only talk to the Intel® 631xESB/632xESB I/O Controller Hub using legacy mechanisms. Software shall set this bit to '1' before accessing other AHCI registers.
30:2	Reserved. Returns 0.
1	**Interrupt Enable (IE) –** R/W. This global bit enables interrupts from the Intel® 631xESB/632xESB I/O Controller Hub. 0 = All interrupt sources from all ports are disabled. 1 = Interrupts are allowed from the AHCI Controller.
0	**HBA Reset (HR)** – R/W. Resets AHCI Controller. 0 = No effect 1 = When set by SW, this bit causes an internal reset of the AHCI Controller. All state machines that relate to data transfers and queuing return to an idle condition, and all ports are re-initialized via COMRESET. ***Note:*** For further details, consult section 12.3.3 of the *Serial ATA Advanced Host Controller Interface Specification*.

23.3.1.3 IS – Interrupt Status Register (D31:F2)

Address Offset: ABAR + 08h–0Bh
Default Value: 00000000h
Attribute: R/WC, RO
Size: 32 bits

This register indicates which of the ports within the controller have an interrupt pending and require service.

Bit	Description
31:6	Reserved. Returns 0.
5	**Interrupt Pending Status Port[5] (IPS[5]) –** R/WC**.** 0 = No interrupt pending. 1 = Port 5 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt.
4	**Interrupt Pending Status Port[4] (IPS[4]) –** R/WC**.** 0 = No interrupt pending. 1 = Port 4 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt.
3	**Interrupt Pending Status Port[3] (IPS[3]) –** R/WC**.** 0 = No interrupt pending. 1 = Port 3 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt.

Bit	Description
2	**Interrupt Pending Status Port[2] (IPS[2]) –** R/WC 0 = No interrupt pending. 1 = Port 2 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt.
1	**Interrupt Pending Status Port[1] (IPS[1]) –** R/WC. 0 = No interrupt pending. 1 = Port 1has an interrupt pending. Software can use this information to determine which ports require service after an interrupt.
0	**Interrupt Pending Status Port[0] (IPS[0]) –** R/WC. 0 = No interrupt pending. 1 = Port 0 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt.

23.3.1.4 PI – Ports Implemented Register (D31:F2)

Address Offset: ABAR + 0Ch–0Fh
Attribute: R/WO, RO
Default Value: 00000000h
Size: 32 bits

This register indicates which ports are exposed to the Intel® 631xESB/632xESB I/O Controller Hub. It is loaded by platform BIOS. It indicates which ports that the device supports are available for software to use. For ports that are not available, software must not read or write to registers within that port.

Bit	Description
31:6	Reserved. Returns 0.
5	**Ports Implemented Port 5 (PI5)** – R/WO. 0 = The port is not implemented. 1 = The port is implemented.
4	**Ports Implemented Port 4 (PI4)** – R/WO. 0 = The port is not implemented. 1 = The port is implemented.
3	**Ports Implemented Port 3 (PI3)** – R/WO. 0 = The port is not implemented. 1 = The port is implemented.
2	**Ports Implemented Port 2 (PI2)** – R/WO. 0 = The port is not implemented. 1 = The port is implemented.
1	**Ports Implemented Port 1 (PI1)** – R/WO. 0 = The port is not implemented. 1 = The port is implemented.
0	**Ports Implemented Port 0 (PI0) –** R/WO. 0 = The port is not implemented. 1 = The port is implemented.

23.3.1.5 VS – AHCI Version (D31:F2)

Address Offset: ABAR + 10h–13h
Attribute: RO
Default Value: 00010000h
Size: 32 bits

This register indicates the major and minor version of the AHCI specification. It is BCD encoded. The upper two bytes represent the major version number, and the lower two bytes represent the minor version number. Example: Version 3.12 would be represented as 00030102h. The current version of the specification is 1.0 (00010000h).

Bit	Description
31:16	Major Version Number (MJR) – RO. Indicates the major version is "1"
15:0	Minor Version Number (MNR) – RO. Indicates the minor version is "0".

23.3.1.6 SGPIOCR – SGPIO Control Register (SATA-D31:F2)

Address Offset: ABAR + A0h–A3h
Default Value: 00000000h
Attribute: RO, RW
Size: 32 bits

Bit	Description
31:22	Reserved.
21:19	**Drive 5 Data (D5DAT) – RW:** Indicates the data to be driven out for Drive 5 on SDATAOUT1.
18:16	**Drive 4 Data (D4DAT) – RW:** Indicates the data to be driven out for Drive 4 on SDATAOUT1.
15:13	**Drive 3 Data (D3DAT) – RW:** Indicates the data to be driven out for Drive 3 on SDATAOUT0.
12:10	**Drive 2 Data (D2DAT) – RW**: Indicates the data to be driven out for Drive 2 on SDATAOUT0.
09:07	**Drive 1 Data (D1DAT) – RW**: Indicates the data to be driven out for Drive 1 on SDATAOUT0.
06:04	**Drive 0 Data (D0DAT) – RW**: Indicates the data to be driven out for Drive 0 on SDATAOUT0.
03:00	**SLOAD Vendor Specific Message (SVSM) – RW:** Indicates the vendor-specific message to be driven on to SGPIO bus on SLOAD pin.

23.3.2 Port Registers (D31:F2)

Table 23-5. Port [5:0] DMA Register Address Map (Sheet 1 of 3)

ABAR + Offset	Mnemonic	Register
100–103	P0CLB	Port 0 Command List Base Address
104–107	P0CLBU	Port 0 Command List Base Address Upper 32-Bits
108–10B	P0FB	Port 0 FIS Base Address
10C–10F	P0FBU	Port 0 FIS Base Address Upper 32-Bits
110–113	P0S	Port 0 Status
114–117	P0IE	Port 0 Interrupt Enable
118–11C	P0CMD	Port 0 Command
11D–11F	–	Reserved
120–123	P0TFD	Port 0 Task File Data
124–127	P0SIG	Port 0 Signature
128–12B	P0SSTS	Port 0 Serial ATA Status
12C–12F	P0SCTL	Port 0 Serial ATA Control
130–133	P0SERR	Port 0 Serial ATA Error
134–137	P0SACT	Port 0 Device Status
138–13B	P0CI	Port 0 Command Issue
13C–17F	–	Reserved
180–183	P1CLB	Port 1 Command List Base Address
184–187	P1CLBU	Port 1 Command List Base Address Upper 32-Bits

Table 23-5. Port [5:0] DMA Register Address Map (Sheet 2 of 3)

ABAR + Offset	Mnemonic	Register
188–18B	P1FB	Port 1 FIS Base Address
18C–18F	P1FBU	Port 1 FIS Base Address Upper 32-Bits
190–193	P1S	Port 1 Status
194–197	P1IE	Port 1 Interrupt Enable
198–19C	P1CMD	Port 1 Command
19D–19F	–	Reserved
1A0–1A3	P1TFD	Port 1 Task File Data
1A4–1A7	P1SIG	Port 1 Signature
1A8–1AB	P1SSTS	Port 1 Serial ATA Status
1AC–1AF	P1SCTL	Port 1 Serial ATA Control
1B0–1B3	P1SERR	Port 1 Serial ATA Error
1B4–1B7	P1SACT	Port 1 Device Status
1B8–1BB	P1CI	Port 1 Command Issue
1BC–1FF	–	Reserved
200–203	P2CLB	Port 2 Command List Base Address
204–207	P2CLBU	Port 2 Command List Base Address Upper 32-Bits
208–20B	P2FB	Port 2 FIS Base Address
20C–20F	P2FBU	Port 2 FIS Base Address Upper 32-Bits
210–213	P2S	Port 2 Status
214–217	P2IE	Port 2 Interrupt Enable
218–21C	P2CMD	Port 2 Command
21D–21F	–	Reserved
220–223	P2TFD	Port 2 Task File Data
224–227	P2SIG	Port 2 Signature
228–22B	P2SSTS	Port 2 Serial ATA Status
22C–22F	P2SCTL	Port 2 Serial ATA Control
230–233	P2SERR	Port 2 Serial ATA Error
234–237	P2SACT	Port 2 Device Status
238–23B	P2CI	Port 2 Command Issue
23C–27F	–	Reserved
280–283	P3CLB	Port 3 Command List Base Address
284–287	P3CLBU	Port 3 Command List Base Address Upper 32-Bits
288–28B	P3FB	Port 3 FIS Base Address
28C–28F	P3FBU	Port 3 FIS Base Address Upper 32-Bits
290–293	P3S	Port 3 Status
294–297	P3IE	Port 3 Interrupt Enable
298–29C	P3CMD	Port 3 Command
19D–19F	–	Reserved
2A0–2A3	P3TFD	Port 3 Task File Data
2A4–2A7	P3SIG	Port 3 Signature
2A8–2AB	P3SSTS	Port 3 Serial ATA Status

Table 23-5. Port [5:0] DMA Register Address Map (Sheet 3 of 3)

ABAR + Offset	Mnemonic	Register
2AC–2AF	P3SCTL	Port 3 Serial ATA Control
2B0–2B3	P3SERR	Port 3 Serial ATA Error
2B4–2B7	P3SACT	Port 3 Device Status
2B8–2BB	P3CI	Port 3 Command Issue
2BC–2FF	–	Reserved
300–303	P4CLB	Port 4Command List Base Address
304–307	P4CLBU	Port 3 Command List Base Address Upper 32-Bits
308–30B	P4FB	Port 4 FIS Base Address
30C–30F	P4FBU	Port 4 FIS Base Address Upper 32-Bits
310–313	P4S	Port 4 Status
314–317	P4IE	Port 4 Interrupt Enable
318–31C	P4CMD	Port 4 Command
31D–31F	–	Reserved
320–323	P4TFD	Port 4 Task File Data
324–327	P4SIG	Port 4 Signature
328–32B	P4SSTS	Port 4 Serial ATA Status
32C–32F	P4SCTL	Port 4 Serial ATA Control
330–333	P4SERR	Port 4 Serial ATA Error
334–337	P4SACT	Port 4 Device Status
338–33B	P4CI	Port 4 Command Issue
33C–37F	–	Reserved
380–383	P5CLB	Port 5 Command List Base Address
384–387	P5CLBU	Port 5 Command List Base Address Upper 32-Bits
388–38B	P5FB	Port 5 FIS Base Address
38C–38F	P5FBU	Port 5 FIS Base Address Upper 32-Bits
390–393	P5S	Port 5 Status
394–397	P5IE	Port 5 Interrupt Enable
398–39C	P5CMD	Port 5 Command
39D–39F	–	Reserved
3A0–3A3	P5TFD	Port5 Task File Data
3A4–3A7	P5SIG	Port 5 Signature
3A8–3AB	P5SSTS	Port 5 Serial ATA Status
3AC–3AF	P5SCTL	Port 5 Serial ATA Control
3B0–3B3	P5SERR	Port 5 Serial ATA Error
3B4–3B7	P5SACT	Port 5 Device Status
3B8–3BB	P5CI	Port 5 Command Issue
3BC–3FF	–	Reserved

23.3.2.1 PxCLB – Port [5:0] Command List Base Address Register (D31:F2)

Address Offset:	Port 0: ABAR + 100h Port 1: ABAR + 180h Port 2: ABAR + 200h Port 3: ABAR + 280h Port 4: ABAR + 300h Port 5: ABAR + 380h	Attribute:	R/W, RO
Default Value:	Undefined	Size:	32 bits

Bit	Description
31:10	**Command List Base Address (CLB) –** R/W**.** Indicates the 32-bit base for the command list for this port. This base is used when fetching commands to execute. The structure pointed to by this address range is 1 KByte in length. This address must be 1 KB aligned as indicated by bits 31:10 being read/write**.**
9:0	Reserved – RO

23.3.2.2 PxCLBU – Port [5:0] Command List Base Address Upper 32-Bits Register (D31:F2)

Address Offset:	Port 0: ABAR + 104h Port 1: ABAR + 184h Port 2: ABAR + 204h Port 3: ABAR + 284h Port 4: ABAR + 304h Port 5: ABAR + 384h	Attribute:	R/W
Default Value:	Undefined	Size:	32 bits

Bit	Description
31:0	**Command List Base Address Upper (CLBU) –** R/W**.** Indicates the upper 32-bits for the command list base address for this port. This base is used when fetching commands to execute.

23.3.2.3 PxFB – Port [5:0] FIS Base Address Register (D31:F2)

Address Offset:	Port 0: ABAR + 108h Port 1: ABAR + 188h Port 2: ABAR + 208h Port 3: ABAR + 288h Port 4: ABAR + 308h Port 5: ABAR + 388h	Attribute:	R/W, RO
Default Value:	Undefined	Size:	32 bits

Bit	Description
31:8	**FIS Base Address (FB) –** R/W**.** Indicates the 32-bit base for received FISes. The structure pointed to by this address range is 256 bytes in length. This address must be 256 byte aligned as indicated by bits 31:3 being read/write.
7:0	Reserved – RO

23.3.2.4 PxFBU – Port [5:0] FIS Base Address Upper 32-Bits Register (D31:F2)

Address Offset:	Port 0: ABAR + 10Ch Port 1: ABAR + 18Ch Port 2: ABAR + 20Ch Port 2: ABAR + 20Ch Port 4: ABAR + 38Ch Port 5: ABAR + 48Ch	Attribute:	R/W
Default Value:	Undefined	Size:	32 bits

Bit	Description
31:3	**Command List Base Address Upper (CLBU) –** R/W**.** Indicates the upper 32-bits for the received FIS base for this port.
2:0	Reserved

23.3.2.5 PxIS – Port [5:0] Interrupt Status Register (D31:F2)

Address Offset:	Port 0: ABAR + 110h Port 1: ABAR + 190h Port 2: ABAR + 210h Port 3: ABAR + 290h Port 4: ABAR + 310h Port 5: ABAR + 390h	Attribute:	R/WC, RO
Default Value:	00000000h	Size:	32 bits

Bit	Description
31	**Cold Port Detect Status (CPDS) –** RO**.** Cold presence not supported.
30	**Task File Error Status (TFES)** – R/WC. This bit is set whenever the status register is updated by the device and the error bit (PxTFD.bit 0) is set.
29	**Host Bus Fatal Error Status (HBFS) –** R/WC**.** Indicates that the Intel® 631xESB/632xESB I/O Controller Hub encountered an error that it cannot recover from due to a bad software pointer. In PCI, such an indication would be a target or master abort.
28	**Host Bus Data Error Status (HBDS) –** R/WC**.** Indicates that the Intel® 631xESB/632xESB I/O Controller Hub encountered a data error (uncorrectable ECC / parity) when reading from or writing to system memory.
27	**Interface Fatal Error Status (IFS) –** R/WC**.** Indicates that the Intel® 631xESB/632xESB I/O Controller Hub encountered an error on the SATA interface which caused the transfer to stop.
26	**Interface Non-fatal Error Status (INFS)** – R/WC. Indicates that the Intel® 631xESB/632xESB I/O Controller Hub encountered an error on the SATA interface but was able to continue operation.
25	Reserved
24	**Overflow Status (OFS) –** R/WC**.** Indicates that the Intel® 631xESB/632xESB I/O Controller Hub received more bytes from a device than was specified in the PRD table for the command.
23	**Incorrect Port Multiplier Status (IPMS)** – R/WC. Indicates that the Intel® 631xESB/632xESB I/O Controller Hub received a FIS from a device whose Port Multiplier field did not match what was expected. ***Note:*** Port Multiplier not supported by Intel® 631xESB/632xESB I/O Controller Hub.
22	**PhyRdy Change Status** (PRCS): 0 = Set to 0. Indicates the internal PhyRdy signal Changed state. This bit reflects the state of PxSERR.DIAG.N. Unlike most of the other bits in the register, this bit is RO and is only cleared when PxSERR.DIAG.N is cleared. The internal PhyRdy signal also transitions when the port interface enters PARTIAL or SLUMBER power management states. PARTIAL or SLUMBER must be disabled when Surprise Removal Notification is desired; otherwise, the power management state transitions will appear as false insertion and removal events.
21:8	Reserved
7	**Device Interlock Status (DIS) –** R/WC. When set, indicates that a platform interlock switch has been opened or closed, which may lead to a change in the connection state of the device.This bit is only valid in systems that support an interlock switch (CAP.SIS [ABAR+00:bit 28] set). For systems that do not support an interlock switch, this bit will always be '0'.

Bit	Description
6	**Port Connect Change Status (PCS) –** RO**.** This bit reflects the state of PxSERR.DIAG.X. (ABAR+130h/1D0h/230h/2D0h, bit 26) Unlike other bits in this register, this bit is only cleared when PxSERR.DIAG.X is cleared. 0 = No change in Current Connect Status. 1 = Change in Current Connect Status.
5	**Descriptor Processed (DPS) –** R/WC**.** A PRD with the I bit set has transferred all its data.
4	**Unknown FIS Interrupt (UFS) –** RO**.** An unknown FIS was received and has been copied into system memory. This bit reflects the state of PxSERR.DIAG[F] (ABAR+130h/1D0h/230h/2D0h, bit 25). Unlike other bits in this register, this bit is only cleared when PxSERR.DIAG[F] is cleared.
3	**Set Device Bits Interrupt (SDBS) –** R/WC**.** A Set Device Bits FIS has been received with the I bit set and has been copied into system memory.
2	**DMA Setup FIS Interrupt (DSS) –** R/WC**.** A DMA Setup FIS has been received with the I bit set and has been copied into system memory.
1	**PIO Setup FIS Interrupt (PSS) –** R/WC**.** A PIO Setup FIS has been received with the I bit set, it has been copied into system memory, and the data related to that FIS has been transferred.
0	**Device to Host Register FIS Interrupt (DHRS) –** R/WC**.** A D2H Register FIS has been received with the I bit set, and has been copied into system memory.

23.3.2.6 PxIE – Port [5:0] Interrupt Enable Register (D31:F2)

Address Offset:	Port 0: ABAR + 114h Port 1: ABAR + 194h Port 2: ABAR + 214h Port 3: ABAR + 294h Port 4: ABAR + 314h Port 5: ABAR + 394h	Attribute:	R/W, RO
Default Value:	00000000h	Size:	32 bits

This register enables and disables the reporting of the corresponding interrupt to system software. When a bit is set (‘1’) and the corresponding interrupt condition is active, then an interrupt is generated. Interrupt sources that are disabled (‘0’) are still reflected in the status registers.

Bit	Description
31	Cold Presence Detect Enable (CPDE) – RO. Cold Presence Detect not supported.
30	**Task File Error Enable (TFEE) –** R/W**.** When set, and GHC.IE and PxTFD.STS.ERR (due to a reception of the error register from a received FIS) are set, interrupt will be generated.
29	**Host Bus Fatal Error Enable (HBFE) –** R/W**.** When set, and GHC.IE and PxS.HBFS are set, interrupt will be generated.
28	**Host Bus Data Error Enable (HBDE) –** R/W**.** When set, and GHC.IE and PxS.HBDS are set, interrupt will be generated.
27	**Interface Fatal Error Enable (IFE)** – R/W. When set, GHC.IE is set, and PxIS.IFS is set, interrupt will be generated.
26	**Interface Non-fatal Error Enable (INFE)** – R/W. When set, GHC.IE is set, and PxIS.INFS is set, interrupt will be generated.
25	Reserved - Should be written as ‘0’
24	**Overflow Error Enable (OFE) –** R/W**.** When set, and GHC.IE and PxS.OFS are set, interrupt will be generated.
23	**Incorrect Port Multiplier Enable (IPME)** – R/W. When set, and GHC.IE and PxIS.IPMS are set, the Intel® 631xESB/632xESB I/O Controller Hub will generate an interrupt. ***Note:*** Should be written as ‘0’. Port Multiplier not supported.
22	**PhyRdy Change Interrupt Enable (PRCIE)**: 0 = Disable. 1 = When set, and GHC.IE is set, and PxIS.PRCS is set, interrupt will be generated.
21:8	Reserved - Should be written as ‘0’

Bit	Description
7	**Device Interlock Enable (DIE) –** R/W. When set, and PxIS.DIS is set, interrupt will be generated. For systems that do not support an interlock switch, this bit shall be a read-only '0'.
6	**Port Change Interrupt Enable (PCE) –** R/W**.** When set, and GHC.IE and PxS.PCS are set, interrupt will be generated.
5	**Descriptor Processed Interrupt Enable (DPE) –** R/W**.** When set, and GHC.IE and PxS.DPS are set, interrupt will be generated
4	**Unknown FIS Interrupt Enable (UFIE) –** R/W**.** When set, and GHC.IE is set and an unknown FIS is received, the ICH6 will generate this interrupt.
3	**Set Device Bits FIS Interrupt Enable (SDBE) –** R/W**.** When set, and GHC.IE and PxS.SDBS are set, interrupt will be generated.
2	**DMA Setup FIS Interrupt Enable (DSE) –** R/W**.** When set, and GHC.IE and PxS.DSS are set, interrupt will be generated.
1	**PIO Setup FIS Interrupt Enable (PSE) –** R/W**.** When set, and GHC.IE and PxS.PSS are set, interrupt will be generated.
0	**Device to Host Register FIS Interrupt Enable (DHRE) –** R/W**.** When set, and GHC.IE and PxS.DHRS are set, interrupt will be generated.

23.3.2.7 PxCMD – Port [5:0] Command Register (D31:F2)

Address Offset:	Port 0: ABAR + 118h Port 1: ABAR + 198h Port 2: ABAR + 218h Port 3: ABAR + 298h Port 4: ABAR + 318h Port 5: ABAR + 398h	Attribute:	R/W, RO, R/WO
Default Value:	0000w00wh where w = 00?0b (for?, see bit description)	Size:	32 bits

Bit	Description
31:28	**Interface Communication Control (ICC) –** R/W**.** This is a four bit field which can be used to control reset and power states of the interface. Writes to this field will cause actions on the interface, either as primitives or an OOB sequence, and the resulting status of the interface will be reported in the PxSSTS register (Address offset Port 0:ABAR+124h, Port 1: ABAR+1A4h, Port 2: ABAR+224h, Port 3: ABAR+2A4h). Value – Definition Fh–7h: Reserved 6h: Slumber: This will cause the Intel® 631xESB/632xESB I/O Controller Hub to request a transition of the interface to the slumber state. The SATA device may reject the request and the interface will remain in its current state 5h–3h: Reserved 2h: Partial: This will cause the Intel® 631xESB/632xESB I/O Controller Hub to request a transition of the interface to the partial state. The SATA device may reject the request and the interface will remain in its current state. 1h: Active: This will cause the Intel® 631xESB/632xESB I/O Controller Hub to request a transition of the interface into the active state. 0h: No-Op / Idle: When software reads this value, it indicates the Intel® 631xESB/632xESB I/O Controller Hub is not in the process of changing the interface state or sending a device reset, and a new link command may be issued. When system software writes a non-reserved value other than No-Op (0h), the Intel® 631xESB/632xESB I/O Controller Hub will perform the action and update this field back to Idle (0h). If software writes to this field to change the state to a state the link is already in (for example, interface is in the active state and a request is made to go to the active state), the Intel® 631xESB/632xESB I/O Controller Hub will take no action and return this field to Idle.
27	**Aggressive Slumber / Partial (ASP) –** R/W**.** When set, and the ALPE bit (bit 26) is set, the Intel® 631xESB/632xESB I/O Controller Hub will aggressively enter the slumber state when it clears the PxCI register and the PxSACT register is cleared. When cleared, and the ALPE bit is set, the Intel® 631xESB/632xESB I/O Controller Hub will aggressively enter the partial state when it clears the PxCI register and the PxSACT register is cleared.
26	**Aggressive Link Power Management Enable (ALPE) –** R/W**.** When set, the Intel® 631xESB/632xESB I/O Controller Hub will aggressively enter a lower link power state (partial or slumber) based upon the setting of the ASP bit (bit 27).
25	**Drive LED on ATAPI Enable (DLAE) –** R/W**.** When set, the Intel® 631xESB/632xESB I/O Controller Hub will drive the LED pin active for ATAPI commands (PxCLB[CHz.A] set) in addition to ATA commands. When cleared, the Intel® 631xESB/632xESB I/O Controller Hub will only drive the LED pin active for ATA commands. See Section 5.18.1.8 for details on the activity LED.
24	**HDevice is ATAPI (ATAPI) –** R/W. When set, the connected device is an ATAPI device. This bit is used by the Intel® 631xESB/632xESB I/O Controller Hub to control whether or not to generate the desktop LED when commands are active. See Section 5.18.1.8 for details on the activity LED.
23:20	Reserved
19	Interlock Switch Attached to Port (ISP) – R/WO. When interlock switches are supported in the platform (CAP.SIS [ABAR+00h:bit 28] set), this indicates whether this particular port has an interlock switch attached. This bit can be used by system software to enable such features as aggressive power management, as disconnects can always be detected regardless of PHY state with an interlock switch. When this bit is set, it is expected that HPCP (bit 18) in this register is also set. No action on the state of this bit – it is for system software only. For example, if this bit is cleared, and an interlock switch toggles, the Intel® 631xESB/632xESB I/O Controller Hub still treats it as a proper interlock switch event.

Bit	Description
18	**Hot Plug Capable Port (HPCP)** – R/WO. 0 = Port is not capable of Hot-Plug. 1 = Port is Hot-Plug capable. This indicates whether the platform exposes this port to a device which can be Hot-Plugged. SATA by definition is Hot-Pluggable, but not all platforms are constructed to allow the device to be removed (it may be screwed into the chassis, for example). This bit can be used by system software to indicate a feature such as "eject device" to the end-user. No action on the state of this bit - it is for system software only. For example, if this bit is cleared, and a Hot-Plug event occurs, the Intel® 631xESB/632xESB I/O Controller Hub still treats it as a proper Hot-Plug event.
17	**Port Multiplier Attached (PMA) –** RO / R/W. When this bit is set, a port multiplier is attached to the Intel® 631xESB/632xESB I/O Controller Hub for this port. When cleared, a port multiplier is not attached to this port. This bit is RO '0' when CAP.PMS (offset ABAR+00h:bit 17) = '0' and R/W when CAP.PMS = '1'. ***Note:*** Port Multiplier is not supported.
16	Port Multiplier FIS Based Switching Enable (PMFSE) – RO. FIS-based switching is not supported.
15	**Controller Running (CR) –** RO. When this bit is set, the DMA engines for a port are running. See section 5.2.2 of the *Serial ATA AHCI Specification* for details on when this bit is set and cleared.
14	**FIS Receive Running (FR)** – RO. When set, the FIS Receive DMA engine for the port is running. See section 12.2.2 of the *Serial ATA AHCI Specification* for details on when this bit is set and cleared by the Intel® 631xESB/632xESB I/O Controller Hub.
13	**Interlock Switch State (ISS)** – RO. For systems that support interlock switches (via CAP.SIS [ABAR+00h:bit 28]), if an interlock switch exists on this port (via ISP in this register), this bit indicates the current state of the interlock switch. A '0' indicates the switch is closed, and a '1' indicates the switch is opened. For systems that do not support interlock switches, or if an interlock switch is not attached to this port, this bit reports '0'.
12:8	**Current Command Slot (CCS) –** RO**.** Indicates the current command slot the Intel® 631xESB/632xESB I/O Controller Hub is processing. This field is valid when the ST bit is set in this register, and is constantly updated by the Intel® 631xESB/632xESB I/O Controller Hub. This field can be updated as soon as the Intel® 631xESB/632xESB I/O Controller Hub recognizes an active command slot, or at some point soon after when it begins processing the command. This field is used by software to determine the current command issue location of the Intel® 631xESB/632xESB I/O Controller Hub. In queued mode, software shall not use this field, as its value does not represent the current command being executed. Software shall only use PxCI and PxSACT when running queued commands.
7:5	Reserved
4	**FIS Receive Enable (FRE)** – R/W. When set, the Intel® 631xESB/632xESB I/O Controller Hub may post received FISes into the FIS receive area pointed to by PxFB (ABAR+108h/188h/208h/288h) and PxFBU (ABAR+10Ch/18Ch/20Ch/28Ch). When cleared, received FISes are not accepted, except for the first D2H (device-to-host) register FIS after the initialization sequence. System software must not set this bit until PxFB (PxFBU) have been programmed with a valid pointer to the FIS receive area, and if software wishes to move the base, this bit must first be cleared, and software must wait for the FR bit (bit 14) in this register to be cleared.
3	Port Selector Activate (PSA) – RO. Port Selector not supported.
2	Power On Device (POD) **–** RO**.** Cold presence detect not supported.
1	**Spin-Up Device (SUD)** – R/W / RO This bit is R/W and defaults to '0' for systems that support staggered spin-up (R/W when CAP.SSS (ABAR+00h:bit 27) is '1'). Bit is RO '1' for systems that do not support staggered spin-up (when CAP.SSS is '0'). 0 = No action. 1 = On an edge detect from '0' to '1', the Intel® 631xESB/632xESB I/O Controller Hub starts a COMRESET initialization sequence to the device.
0	**Start (ST) –** R/W**.** When set, the Intel® 631xESB/632xESB I/O Controller Hub may process the command list. When cleared, the Intel® 631xESB/632xESB I/O Controller Hub may not process the command list. Whenever this bit is changed from a 0 to a 1, the Intel® 631xESB/632xESB I/O Controller Hub starts processing the command list at entry 0. Whenever this bit is changed from a 1 to a 0, the PxCI register is cleared by the Intel® 631xESB/632xESB I/O Controller Hub upon the Intel® 631xESB/632xESB I/O Controller Hub putting the controller into an idle state. Refer to section 12.2.1 of the *Serial ATA AHCI Specification* for important restrictions on when ST can be set to '1'.

23.3.2.8 PxTFD – Port [5:0] Task File Data Register (D31:F2)

Address Offset:	Port 0: ABAR + 120h Port 1: ABAR + 1A0h Port 2: ABAR + 220h Port 3: ABAR + 2A0h Port 4: ABAR + 320h Port 5: ABAR + 3A0h	Attribute:	RO
Default Value:	0000007Fh	Size:	32 bits

This is a 32-bit register that copies specific fields of the task file when FISes are received. The FISes that contain this information are:

- D2H Register FIS
- PIO Setup FIS
- Set Device Bits FIS

Bit	Description
31:16	Reserved
15:8	**Error (ERR) –** RO**.** Contains the latest copy of the task file error register.
7:0	**Status (STS) –** RO**.** Contains the latest copy of the task file status register. Fields of note in this register that affect AHCI. Bit FieldDefinition 7 BSYIndicates the interface is busy 6:4 n/a Not applicable 3 DRQIndicates a data transfer is requested 2:1 n/aNot applicable 0 ERRIndicates an error during the transfer.

23.3.2.9 PxSIG – Port [5:0] Signature Register (D31:F2)

Address Offset:	Port 0: ABAR + 124h Port 1: ABAR + 1A4h Port 2: ABAR + 224h Port 3: ABAR + 2A4h Port 4: ABAR + 324h Port 5: ABAR + 3A4h	Attribute:	RO
Default Value:	FFFFFFFFh	Size:	32 bits

This is a 32-bit register which contains the initial signature of an attached device when the first D2H Register FIS is received from that device. It is updated once after a reset sequence.

Bit	Description
31:0	**Signature (SIG) –** RO**.** Contains the signature received from a device on the first D2H register FIS. The bit order is as follows: Bit Field 31:24 LBA High Register 23:16 LBA Mid Register 15:8 LBA Low Register 7:0 Sector Count Register

23.3.2.10 PxSSTS – Port [5:0] Serial ATA Status Register (D31:F2)

Address Offset:	Port 0: ABAR + 128h Port 1: ABAR + 1A8h Port 2: ABAR + 228h Port 3: ABAR + 2A8h Port 4: ABAR + 328h Port 5: ABAR + 3A8h	Attribute:	RO
Default Value:	00000000h	Size:	32 bits

This is a 32-bit register that conveys the current state of the interface and host. The Intel® 631xESB/632xESB I/O Controller Hub updates it continuously and asynchronously. When the Intel® 631xESB/632xESB I/O Controller Hub transmits a COMRESET to the device, this register is updated to its reset values.

Bit	Description
31:12	Reserved
11:8	**Interface Power Management (IPM) –** RO**.** Indicates the current interface state: Value Definition 0h Device not present or communication not established 1h Interface in active state 2h Interface in PARTIAL power management state 6h Interface in SLUMBER power management state All other values reserved.
7:4	**Current Interface Speed (SPD)** – RO. Indicates the negotiated interface communication speed. **Value Definition** 0h Device not present or communication not established 1h Generation 1 communication rate negotiated (1.5Gbps) 2h Generation 2 communication rate negotiated (3.0Gbps) All other values reserved
3:0	**Device Detection (DET) –** RO**.** Indicates the interface device detection and Phy state: **Value Definition** 0h No device detected and Phy communication not established 1h Device presence detected but Phy communication not established 3h Device presence detected and Phy communication established 4h Phy in offline mode as a result of the interface being disabled or running in a BIST loopback mode All other values reserved

23.3.2.11 PxSSTS – Port [5:0] Serial ATA Control Register (D31:F2)

Address Offset:	Port 0: ABAR + 12Ch Port 1: ABAR + 1ACh Port 2: ABAR + 22Ch Port 3: ABAR + 2ACh Port 4: ABAR + 32Ch Port 5: ABAR + 3ACh	Attribute:	R/W, RO
Default Value:	00000004h	Size:	32 bits

This is a 32-bit read-write register by which software controls SATA capabilities. Writes to the SControl register result in an action being taken by the Intel® 631xESB/632xESB I/O Controller Hub or the interface. Reads from the register return the last value written to it.

Bit	Description
31:16	Reserved
19:16	Port Multiplier Port (PMP) – RO. This field is not used by AHCI
15:12	Select Power Management (SPM) – RO. This field is not used by AHCI

Bit	Description
11:8	**Interface Power Management Transitions Allowed (IPM) –** R/W**.** Indicates which power states that is allowed to transition to: Value Definition 0h No interface restrictions 1h Transitions to the PARTIAL state disabled 2h Transitions to the SLUMBER state disabled 3h Transitions to both PARTIAL and SLUMBER states disabled All other values reserved
7:4	**Speed Allowed (SPD)** – R/W. Indicates the highest allowable speed of the interface. Value Definition 0h No speed negotiation restrictions 1h Limit speed negotiation to Generation 1 communication rate (1.5Gbps) 2h Limit speed negotiation to Generation 2 communication rate (3.0Gbps) All other values reserved.
3:0	**Device Detection Initialization (DET) –** R/W**.** Controls the Intel® 631xESB/632xESB I/O Controller Hub's device detection and interface initialization. **Value Definition** 0h No device detection or initialization action requested 1h Perform interface communication initialization sequence to establish communication. This is functionally equivalent to a hard reset and results in the interface being reset and communications re-initialized 4h Disable the Serial ATA interface and put Phy in offline mode All other values reserved. When this field is written to a 1h, the Intel® 631xESB/632xESB I/O Controller Hub initiates COMRESET and starts the initialization process. When the initialization is complete, this field shall remain 1h until set to another value by software. This field may only be changed to 1h or 4h when PxCMD.ST is '0'. Changing this field while the Intel® 631xESB/632xESB I/O Controller Hub is running results in undefined behavior.

23.3.2.12 PxSERR – Port [3:0] Serial ATA Error Register (D31:F2)

Address Offset:	Port 0: ABAR + 130h Port 1: ABAR + 1D0h Port 2: ABAR + 230h Port 3: ABAR + 2D0h	Attribute:	R/WC
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:16	**Diagnostics (DIAG) –** R/WC**.** Contains diagnostic error information for use by diagnostic software in validating correct operation or isolating failure modes: Bits Description 31:27Reserved 26 **Exchanged (X)**: When set to one this bit indicates a COMINIT signal was received. This bit is reflected in the interrupt register PxIS.PCS. 25 **Unrecognized FIS Type (F)**: Indicates that one or more FISs were received by the Transport layer with good CRC, but had a type field that was not recognized. 24 **Transport state transition error (T)**: Indicates that an error has occurred in the transition from one state to another within the Transport layer since the last time this bit was cleared. 23 **Link Sequence Error (S)**: Indicates that one or more Link state machine error conditions was encountered. The Link Layer state machine defines the conditions under which the link layer detects an erroneous transition. 22 **Handshake Error (H)**: Indicates that one or more R_ERR handshake response was received in response to frame transmission. Such errors may be the result of a CRC error detected by the recipient, a disparity or 8b/10b decoding error, or other error condition leading to a negative handshake on a transmitted frame. 21 **CRC Error (C)**: Indicates that one or more CRC errors occurred with the Link Layer. 20 **Disparity Error (D)**: This field is not used by AHCI. 19 **10b to 8b Decode Error (B)**: Indicates that one or more 10b to 8b decoding errors occurred. 18 **Comm Wake (W)**: Indicates that a Comm Wake signal was detected by the Phy. 17 **Phy Internal Error (I)**: Indicates that the Phy detected some internal error. 16 **PhyRdy Change (N)**: Indicates that the PhyRdy signal changed state.
15:0	**Error (ERR) –** R/WC**.** The ERR field contains error information for use by host software in determining the appropriate response to the error condition. If one or more of bits 11:8 of this register are set, the controller will stop the current transfer. Bits Description 15:12Reserved 11 **Internal Error (E)**: The SATA controller failed due to a master or target abort when attempting to access system memory. 10 **Protocol Error (P)**: A violation of the Serial ATA protocol was detected. 9 **Persistent Communication or Data Integrity Error (C)**: A communication error that was not recovered occurred that is expected to be persistent. Persistent communications errors may arise from faulty interconnect with the device, from a device that has been removed or has failed, or a number of other causes. 8 **Transient Data Integrity Error (T)**: A data integrity error occurred that was not recovered by the interface. 7:2 Reserved 1 **Recovered Communications Error (M)**: Communications between the device and host was temporarily lost but was re-established. This can arise from a device temporarily being removed, from a temporary loss of Phy synchronization, or from other causes and may be derived from the PhyNRdy signal between the Phy and Link layers. 0 **Recovered Data Integrity Error (I)**: A data integrity error occurred that was recovered by the interface through a retry operation or other recovery action.

23.3.2.13 PxSACT – Port [3:0] Serial ATA Active (D31:F2)

Address Offset:	Port 0: ABAR + 134h Port 1: ABAR + 1D4h Port 2: ABAR + 234h Port 3: ABAR + 2D4h Port 4: ABAR + 334h Port 5: ABAR + 3D4h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:0	**Device Status (DS) –** R/W**.** System software sets this bit for SATA queuing operations prior to setting the PxCI.CI bit in the same command slot entry. This field is cleared via the Set Device Bits FIS. This field is also cleared when PxCMD.ST (ABAR+118h/198h/218h/298h:bit 0) is cleared by software, and as a result of a COMRESET or SRST.

23.3.2.14 PxCI – Port [3:0] Command Issue Register (D31:F2)

Address Offset:	Port 0: ABAR + 138h Port 1: ABAR + 1D8h Port 2: ABAR + 238h Port 3: ABAR + 2D8h Port 4: ABAR + 338h Port 5: ABAR + 3D8h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:0	**Commands Issued (CI) –** R/W**.** This field is set by software to indicate that a command has been built-in system memory for a command slot and may be sent to the device. When the Intel® 631xESB/632xESB I/O Controller Hub receives a FIS which clears the BSY and DRQ bits for the command, it clears the corresponding bit in this register for that command slot. This field is also cleared when PxCMD.ST (ABAR+118h/198h/218h/298h:bit 0) is cleared by software.

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24 SMBus Controller Registers (D31:F3)

24.1 PCI Configuration Registers (SMBUS – D31:F3)

Table 24-1. SMBus Controller PCI Register Address Map (SMBUS – D31:F3)

Offset	Mnemonic	Register Name	Default	Type
00–01h	VID	Vendor Identification	8086	RO
02–03h	DID	Device Identification	269Bh	RO
04–05h	PCICMD	PCI Command	0000h	R/W, RO
06–07h	PCISTS	PCI Status	0280h	RO, R/WC
08h	RID	Revision Identification	See register description.	RO
09h	PI	Programming Interface	00h	RO
0Ah	SCC	Sub Class Code	05h	RO
0Bh	BCC	Base Class Code	0Ch	RO
20–23h	SMB_BASE	SMBus Base Address	00000001h	R/W, RO
2C–2Dh	SVID	Subsystem Vendor Identification	00h	RO
2E–2Fh	SID	Subsystem Identification	00h	R/WO
3Ch	INT_LN	Interrupt Line	00h	R/W
3Dh	INT_PN	Interrupt Pin	See description	RO
40h	HOSTC	Host Configuration	00h	R/W

Note: Registers that are not shown should be treated as Reserved (See Section 2.1 for details).

24.1.1 VID – Vendor Identification Register (SMBUS – D31:F3)

Address: 00–01h
Default Value: 8086h
Attribute: RO
Size: 16 bits

Bit	Description
15:0	Vendor ID – RO. This is a 16-bit value assigned to Intel

24.1.2 DID – Device Identification Register (SMBUS – D31:F3)

Address: 02–03h
Default Value: 269Bh
Attribute: RO
Size: 16 bits

Bit	Description
15:0	Device ID – RO. Refer to Table 2-33

24.1.3 PCICMD – PCI Command Register (SMBUS – D31:F3)

Address: 04–05h
Default Value: 0000h
Attributes: RO, R/W
Size: 16 bits

Bit	Description
15:11	Reserved
10	**Interrupt Disable –** R/W. 0 = Enable 1 = Disables SMBus to assert its PIRQB# signal.
9	Fast Back to Back Enable (FBE) – RO. Hardwired to 0.
8	**SERR# Enable (SERR_EN) –** R/W. 0 = Enables SERR# generation. 1 = Disables SERR# generation.
7	Wait Cycle Control (WCC) – RO. Hardwired to 0.
6	**Parity Error Response (PER)** – R/W. 0 = Disable 1 = Sets Detected Parity Error bit (D31:F3:06, bit 15) when a parity error is detected.
5	VGA Palette Snoop (VPS) – RO. Hardwired to 0.
4	Postable Memory Write Enable (PMWE) – RO. Hardwired to 0.
3	Special Cycle Enable (SCE) – RO. Hardwired to 0.
2	Bus Master Enable (BME) – RO. Hardwired to 0.
1	Memory Space Enable (MSE) – RO. Hardwired to 0.
0	**I/O Space Enable (IOSE) –** R/W. 0 = Disable 1 = Enables access to the SM Bus I/O space registers as defined by the Base Address Register.

24.1.4 PCISTS – PCI Status Register (SMBUS – D31:F3)

Address: 06–07h
Default Value: 0280h
Attributes: RO, R/WC
Size: 16 bits

Note: For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 to the bit has no effect.

Bit	Description
15	**Detected Parity Error (DPE)** – R/WC. 0 = No parity error detected. 1 = Parity error detected.
14	**Signaled System Error (SSE) –** R/WC. 0 = No system error detected. 1 = System error detected.
13	Received Master Abort (RMA) – RO. Hardwired to 0.
12	Received Target Abort (RTA) – RO. Hardwired to 0.
11	**Signaled Target Abort (STA) –** R/WC. 0 = Intel® 631xESB/632xESB I/O Controller Hub did Not terminate transaction for this function with a target abort. 1 = The function is targeted with a transaction that the Intel® 631xESB/632xESB I/O Controller Hub terminates with a target abort.
10:9	DEVSEL# Timing Status (DEVT) – RO. This 2-bit field defines the timing for DEVSEL# assertion for positive decode. 01 = Medium timing.
8	Data Parity Error Detected (DPED) – RO. Hardwired to 0.
7	Fast Back to Back Capable (FB2BC) – RO. Hardwired to 1.

6	User Definable Features (UDF) – RO. Hardwired to 0.
5	66 MHz Capable (66MHZ_CAP) – RO. Hardwired to 0.
4	Capabilities List (CAP_LIST) – RO. Hardwired to 0 because there are no capability list structures in this function
3	**Interrupt Status (INTS) –** RO. This bit indicates that an interrupt is pending. It is independent from the state of the Interrupt Enable bit in the PCI Command register.
2:0	Reserved

24.1.5 RID – Revision Identification Register (SMBUS – D31:F3)

Offset Address: 08h Attribute: RO
Default Value: See bit description Size: 8 bits

Bit	Description
7:0	**Revision ID –** RO. Refer to Table 2-33 or the *Intel® 631xESB/632xESB I/O Controller Hub EDS Specification Update - NDA* for the value of the Revision ID Register

24.1.6 PI – Programming Interface Register (SMBUS – D31:F3)

Offset Address: 09h Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Description
7:0	Reserved

24.1.7 SCC – Sub Class Code Register (SMBUS – D31:F3)

Address Offset: 0Ah Attributes: RO
Default Value: 05h Size: 8 bits

Bit	Description
7:0	Sub Class Code (SCC) – RO. 05h = SM Bus serial controller

24.1.8 BCC – Base Class Code Register (SMBUS – D31:F3)

Address Offset: 0Bh Attributes: RO
Default Value: 0Ch Size: 8 bits

Bit	Description
7:0	Base Class Code (BCC) – RO. 0Ch = Serial controller.

24.1.9 SMB_BASE – SMBUS Base Address Register (SMBUS – D31:F3)

Address Offset:	20–23h	Attribute:	R/W, RO
Default Value:	00000001h	Size:	32-bits

Bit	Description
31:16	Reserved – RO
15:5	**Base Address –** R/W. This field provides the 32-byte system I/O base address for the SMB logic.
4:1	Reserved – RO
0	IO Space Indicator – RO. Hardwired to 1 indicating that the SMB logic is I/O mapped.

24.1.10 SVID – Subsystem Vendor Identification Register (SMBUS – D31:F2/F4)

Address Offset:	2Ch–2Dh	Attribute:	RO
Default Value:	0000h	Size:	16 bits
Lockable:	No	Power Well:	Core

Bit	Description
15:0	Subsystem Vendor ID (SVID) – RO. The SVID register, in combination with the Subsystem ID (SID) register, enables the operating system (OS) to distinguish subsystems from each other. The value returned by reads to this register is the same as that which was written by BIOS into the IDE SVID register. ***Note:*** Software can write to this register only once per core well reset. Writes should be done as a single 16-bit cycle.

24.1.11 SID – Subsystem Identification Register (SMBUS – D31:F2/F4)

Address Offset:	2Eh–2Fh	Attribute:	R/WO
Default Value:	0000h	Size:	16 bits
Lockable:	No	Power Well:	Core

Bit	Description
15:0	Subsystem ID (SID) – RO. The SID register, in combination with the SVID register, enables the operating system (OS) to distinguish subsystems from each other. The value returned by reads to this register is the same as that which was written by BIOS into the IDE SID register. ***Note:*** Software can write to this register only once per core well reset. Writes should be done as a single 16-bit cycle.

24.1.12 INT_LN – Interrupt Line Register (SMBUS – D31:F3)

Address Offset:	3Ch	Attributes:	R/W
Default Value:	00h	Size:	8 bits

Bit	Description
7:0	**Interrupt Line (INT_LN) –** R/W. Not used. It is to communicate to software the interrupt line that the interrupt pin is connected to PIRQB#.

24.1.13 INT_PN – Interrupt Pin Register (SMBUS – D31:F3)

Address Offset: 3Dh
Default Value: See description
Attributes: RO
Size: 8 bits

Bit	Description
7:0	Interrupt PIN (INT_PN) – RO. This reflects the value of D31IP.SMIP in chipset configuration space.

24.1.14 HOSTC – Host Configuration Register (SMBUS – D31:F3)

Address Offset: 40h
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:3	Reserved
2	I^2C_EN – R/W. 0 = SMBus behavior. 1 = Enabled to communicate with I^2C devices. This will change the formatting of some commands.
1	**SMB_SMI_EN –** R/W. 0 = SMBus interrupts will not generate an SMI#. 1 = Any source of an SMB interrupt will instead be routed to generate an SMI#. Refer to Section 5.19.6 (Interrupts / SMI#). This bit needs to be set for SMBALERT# to be enabled.
0	**SMBus Host Enable (HST_EN) –** R/W. 0 = Disable the SMBus Host controller. 1 = Enable. The SMB Host controller interface is enabled to execute commands. The INTREN bit (offset SMBASE + 02h, bit 0) needs to be enabled for the SMB Host controller to interrupt or SMI#. Note that the SMB Host controller will not respond to any new requests until all interrupt requests have been cleared.

24.2 SMBus I/O Registers

Table 24-2. SMBus I/O Register Address Map (Sheet 1 of 2)

SMB_BASE + Offset	Mnemonic	Register Name	Default	Type
00h	HST_STS	Host Status	00h	R/WC, RO, R/WC (special)
02h	HST_CNT	Host Control	00h	R/W, WO
03h	HST_CMD	Host Command	00h	R/W
04h	XMIT_SLVA	Transmit Slave Address	00h	R/W
05h	HST_D0	Host Data 0	00h	R/W
06h	HST_D1	Host Data 1	00h	R/W
07h	HOST_BLOCK_DB	Host Block Data Byte	00h	R/W
08h	PEC	Packet Error Check	00h	R/W
09h	RCV_SLVA	Receive Slave Address	44h	R/W
0A–0Bh	SLV_DATA	Receive Slave Data	0000h	RO
0Ch	AUX_STS	Auxiliary Status	00h	R/WC, RO
0Dh	AUX_CTL	Auxiliary Control	00h	R/W
0Eh	SMLINK_PIN_CTL	SMLink Pin Control (TCO Compatible Mode)	See register description	R/W, RO

Table 24-2. SMBus I/O Register Address Map (Sheet 2 of 2)

SMB_BASE + Offset	Mnemonic	Register Name	Default	Type
0Fh	SMBUS_PIN_CTL	SMBus Pin Control	See register description	R/W, RO
10h	SLV_STS	Slave Status	00h	R/WC
11h	SLV_CMD	Slave Command	00h	R/W
14h	NOTIFY_DADDR	Notify Device Address	00h	RO
16h	NOTIFY_DLOW	Notify Data Low Byte	00h	RO
17h	NOTIFY_DHIGH	Notify Data High Byte	00h	RO

24.2.1 HST_STS – Host Status Register (SMBUS – D31:F3)

Register Offset: SMBASE + 00h
Default Value: 00h
Attribute: R/WC, R/WC (special), RO
Size: 8-bits

All status bits are set by hardware and cleared by the software writing a one to the particular bit position. Writing a zero to any bit position has no effect.

Bit	Description
7	**Byte Done Status (DS)** – R/WC. 0 = Software can clear this by writing a 1 to it. 1 = Host controller received a byte (for Block Read commands) or if it has completed transmission of a byte (for Block Write commands) when the 32-byte buffer is not being used. Note that this bit will be set, even on the last byte of the transfer. This bit is not set when transmission is due to the LAN interface heartbeat. This bit has no meaning for block transfers when the 32-byte buffer is enabled. ***Note:*** When the last byte of a block message is received, the host controller will set this bit. However, it will not immediately set the INTR bit (bit 1 in this register). When the interrupt handler clears the BYTE_DONE_STS bit, the message is considered complete, and the host controller will then set the INTR bit (and generate another interrupt). Thus, for a block message of n bytes, the Intel® 631xESB/632xESB I/O Controller Hub will generate n+1 interrupts. The interrupt handler needs to be implemented to handle these cases.
6	**INUSE_STS** – R/WC (special). This bit is used as semaphore among various independent software threads that may need to use the Intel® 631xESB/632xESB I/O Controller Hub's SMBus logic, and has no other effect on hardware. 0 = After a full PCI reset, a read to this bit returns a 0. 1 = After the first read, subsequent reads will return a 1. A write of a 1 to this bit will reset the next read value to 0. Writing a 0 to this bit has no effect. Software can poll this bit until it reads a 0, and will then own the usage of the host controller.
5	SMBALERT_STS – R/WC. 0 = Interrupt or SMI# was not generated by SMBALERT#. Software clears this bit by writing a 1 to it. 1 = The source of the interrupt or SMI# was the SMBALERT# signal. This bit is only cleared by software writing a 1 to the bit position or by RSMRST# going low. If the signal is programmed as a GPI, then this bit will never be set.
4	**FAILED –** R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = The source of the interrupt or SMI# was a failed bus transaction. This bit is set in response to the KILL bit being set to terminate the host transaction.
3	BUS_ERR – R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = The source of the interrupt of SMI# was a transaction collision.

Bit	Description
2	DEV_ERR – R/WC. 0 = Software clears this bit by writing a 1 to it. The Intel® 631xESB/632xESB I/O Controller Hub will then deassert the interrupt or SMI#. 1 = The source of the interrupt or SMI# was due to one of the following: • illegal Command Field, • Unclaimed Cycle (host initiated), • Host Device Time-out Error.
1	**INTR –** R/WC (special). This bit can only be set by termination of a command. INTR is not dependent on the INTREN bit (offset SMBASE + 02h, bit 0) of the Host controller register (offset 02h). It is only dependent on the termination of the command. If the INTREN bit is not set, then the INTR bit will be set, although the interrupt will not be generated. Software can poll the INTR bit in this non-interrupt case. 0 = Software clears this bit by writing a 1 to it. The Intel® 631xESB/632xESB I/O Controller Hub then deasserts the interrupt or SMI#. 1 = The source of the interrupt or SMI# was the successful completion of its last command.
0	**HOST_BUSY** – RO. 0 = Cleared by the Intel® 631xESB/632xESB I/O Controller Hub when the current transaction is completed. 1 = Indicates that the Intel® 631xESB/632xESB I/O Controller Hub is running a command from the host interface. No SMB registers should be accessed while this bit is set, except the BLOCK DATA BYTE Register. The BLOCK DATA BYTE Register can be accessed when this bit is set only when the SMB_CMD bits in the Host Control Register are programmed for Block command or I^2C Read command. This is necessary in order to check the DONE_STS bit.

24.2.2 HST_CNT – Host Control Register (SMBUS – D31:F3)

Register Offset:	SMBASE + 02h	Attribute:	R/W, WO
Default Value:	00h	Size:	8-bits

Note: A read to this register will clear the byte pointer of the 32-byte buffer.

Bit	Description
7	**PEC_EN**. – R/W. 0 = SMBus host controller does not perform the transaction with the PEC phase appended. 1 = Causes the host controller to perform the SMBus transaction with the Packet Error Checking phase appended. For writes, the value of the PEC byte is transferred from the PEC Register. For reads, the PEC byte is loaded in to the PEC Register. This bit must be written prior to the write in which the **START** bit is set.
6	**START –** WO. 0 = This bit will always return 0 on reads. The HOST_BUSY bit in the Host Status register (offset 00h) can be used to identify when the Intel® 631xESB/632xESB I/O Controller Hub has finished the command. 1 = Writing a 1 to this bit initiates the command described in the SMB_CMD field. All registers should be setup prior to writing a 1 to this bit position.
5	**LAST_BYTE –** WO. This bit is used for Block Read commands. 1 = Software sets this bit to indicate that the next byte will be the last byte to be received for the block. This causes the Intel® 631xESB/632xESB I/O Controller Hub to send a NACK (instead of an ACK) after receiving the last byte. ***Note:*** Once the SECOND_TO_STS bit in TCO2_STS register (D31:F0, TCOBASE+6h, bit 1) is set, the LAST_BYTE bit also gets set. While the SECOND_TO_STS bit is set, the LAST_BYTE bit cannot be cleared. This prevents the Intel® 631xESB/632xESB I/O Controller Hub from running some of the SMBus commands (Block Read/Write, I^2C Read, Block I^2C Write).

Bit	Description
4:2	**SMB_CMD –** R/W. The bit encoding below indicates which command the Intel® 631xESB/632xESB I/O Controller Hub is to perform. If enabled, the Intel® 631xESB/632xESB I/O Controller Hub will generate an interrupt or SMI# when the command has completed If the value is for a non-supported or reserved command, the Intel® 631xESB/632xESB I/O Controller Hub will set the device error (DEV_ERR) status bit (offset SMBASE + 00h, bit 2) and generate an interrupt when the START bit is set. The Intel® 631xESB/632xESB I/O Controller Hub will perform no command, and will not operate until DEV_ERR is cleared. 000 = **Quick**: The slave address and read/write value (bit 0) are stored in the transmit slave address register. 001 = **Byte**: This command uses the transmit slave address and command registers. Bit 0 of the slave address register determines if this is a read or write command. 010 = **Byte Data**: This command uses the transmit slave address, command, and DATA0 registers. Bit 0 of the slave address register determines if this is a read or write command. If it is a read, the DATA0 register will contain the read data. 011 = **Word Data**: This command uses the transmit slave address, command, DATA0 and DATA1 registers. Bit 0 of the slave address register determines if this is a read or write command. If it is a read, after the command completes, the DATA0 and DATA1 registers will contain the read data. 100 = **Process Call:** This command uses the transmit slave address, command, DATA0 and DATA1 registers. Bit 0 of the slave address register determines if this is a read or write command. After the command completes, the DATA0 and DATA1 registers will contain the read data. 101 = **Block**: This command uses the transmit slave address, command, DATA0 registers, and the Block Data Byte register. For block write, the count is stored in the DATA0 register and indicates how many bytes of data will be transferred. For block reads, the count is received and stored in the DATA0 register. Bit 0 of the slave address register selects if this is a read or write command. For writes, data is retrieved from the first n (where n is equal to the specified count) addresses of the SRAM array. For reads, the data is stored in the Block Data Byte register. 110 = **I^2C Read**: This command uses the transmit slave address, command, DATA0, DATA1 registers, and the Block Data Byte register. The read data is stored in the Block Data Byte register. The Intel® 631xESB/632xESB I/O Controller Hub continues reading data until the NAK is received. **111 = Block Process:** This command uses the transmit slave address, command, DATA0 and the Block Data Byte register. For block write, the count is stored in the DATA0 register and indicates how many bytes of data will be transferred. For block read, the count is received and stored in the DATA0 register. Bit 0 of the slave address register always indicate a write command. For writes, data is retrieved from the first m (where m is equal to the specified count) addresses of the SRAM array. For reads, the data is stored in the Block Data Byte register. ***Note:*** E32B bit in the Auxiliary Control register must be set for this command to work.
1	**KILL –** R/W. 0 = Normal SMBus host controller functionality. 1 = Kills the current host transaction taking place, sets the FAILED status bit, and asserts the interrupt (or SMI#). This bit, once set, must be cleared by software to allow the SMBus host controller to function normally.
0	**INTREN –** R/W. 0 = Disable. 1 = Enable the generation of an interrupt or SMI# upon the completion of the command.

24.2.3 HST_CMD – Host Command Register (SMBUS – D31:F3)

Register Offset: SMBASE + 03h
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	This 8-bit field is transmitted by the host controller in the command field of the SMBus protocol during the execution of any command.

24.2.4 XMIT_SLVA – Transmit Slave Address Register (SMBUS – D31:F3)

Register Offset:	SMBASE + 04h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

This register is transmitted by the host controller in the slave address field of the SMBus protocol.

Bit	Description
7:1	**Address –** R/W. This field provides a 7-bit address of the targeted slave.
0	**RW –** R/W. Direction of the host transfer. 0 = Write 1 = Read

24.2.5 HST_D0 – Host Data 0 Register (SMBUS – D31:F3)

Register Offset:	SMBASE + 05h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

Bit	Description
7:0	**Data0/Count –** R/W. This field contains the eight bit data sent in the DATA0 field of the SMBus protocol. For block write commands, this register reflects the number of bytes to transfer. This register should be programmed to a value between 1 and 32 for block counts. A count of 0 or a count above 32 will result in unpredictable behavior. The host controller does not check or log illegal block counts.

24.2.6 HST_D1 – Host Data 1 Register (SMBUS – D31:F3)

Register Offset:	SMBASE + 06h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

Bit	Description
7:0	**Data1 –** R/W. This 8-bit register is transmitted in the DATA1 field of the SMBus protocol during the execution of any command.

24.2.7 Host_BLOCK_DB – Host Block Data Byte Register (SMBUS – D31:F3)

Register Offset: SMBASE + 07h
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	**Block Data (BDTA) –** R/W. This is either a register, or a pointer into a 32-byte block array, depending upon whether the E32B bit is set in the Auxiliary Control register. When the E32B bit (offset SMBASE + 0Dh, bit 1) is cleared, this is a register containing a byte of data to be sent on a block write or read from on a block read, just as it behaved on the ICH3. When the E32B bit is set, reads and writes to this register are used to access the 32-byte block data storage array. An internal index pointer is used to address the array, which is reset to 0 by reading the HCTL register (offset 02h). The index pointer then increments automatically upon each access to this register. The transfer of block data into (read) or out of (write) this storage array during an SMBus transaction always starts at index address 0. When the E2B bit is set, for writes, software will write up to 32-bytes to this register as part of the setup for the command. After the Host controller has sent the Address, Command, and Byte Count fields, it will send the bytes in the SRAM pointed to by this register. When the E2B bit is cleared for writes, software will place a single byte in this register. After the host controller has sent the address, command, and byte count fields, it will send the byte in this register. If there is more data to send, software will write the next series of bytes to the SRAM pointed to by this register and clear the DONE_STS bit. The controller will then send the next byte. During the time between the last byte being transmitted to the next byte being transmitted, the controller will insert wait-states on the interface. When the E2B bit is set for reads, after receiving the byte count into the Data0 register, the first series of data bytes go into the SRAM pointed to by this register. If the byte count has been exhausted or the 32-byte SRAM has been filled, the controller will generate an SMI# or interrupt (depending on configuration) and set the DONE_STS bit. Software will then read the data. During the time between when the last byte is read from the SRAM to when the DONE_STS bit is cleared, the controller will insert wait-states on the interface.

24.2.8 PEC – Packet Error Check (PEC) Register (SMBUS – D31:F3)

Register Offset: SMBASE + 08h
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	**PEC_DATA –** R/W. This 8-bit register is written with the 8-bit CRC value that is used as the SMBus PEC data prior to a write transaction. For read transactions, the PEC data is loaded from the SMBus into this register and is then read by software. Software must ensure that the INUSE_STS bit is properly maintained to avoid having this field over-written by a write transaction following a read transaction.

24.2.9 RCV_SLVA – Receive Slave Address Register (SMBUS – D31:F3)

Register Offset: SMBASE + 09h
Default Value: 44h
Lockable: No
Attribute: R/W
Size: 8 bits
Power Well: Resume

Bit	Description
7	Reserved
6:0	**SLAVE_ADDR –** R/W. This field is the slave address that the Intel® 631xESB/632xESB I/O Controller Hub decodes for read and write cycles. the default is not 0, so the SMBus Slave Interface can respond even before the processor comes up (or if the processor is dead). This register is cleared by RSMRST#, but not by PLTRST#.

24.2.10 SLV_DATA – Receive Slave Data Register (SMBUS – D31:F3)

Register Offset:	SMBASE + 0Ah–0Bh	Attribute:	RO
Default Value:	0000h	Size:	16 bits
Lockable:	No	Power Well:	Resume

This register contains the 16-bit data value written by the external SMBus master. The processor can then read the value from this register. This register is reset by RSMRST#, but not PLTRST#

Bit	Description
15:8	**Data Message Byte 1 (DATA_MSG1) –** RO. See Section 5.21.2 for a discussion of this field.
7:0	**Data Message Byte 0 (DATA_MSG0) –** RO. See Section 5.21.2 for a discussion of this field.

24.2.11 AUX_STS – Auxiliary Status Register (SMBUS – D31:F3)

Register Offset:	SMBASE + 0Ch	Attribute:	R/WC, RO
Default Value:	00h	Size:	8 bits
Lockable:	No	Power Well:	Resume

Bit	Description
7:2	Reserved
1	**SMBus TCO Mode (STCO)** – RO. This bit reflects the strap setting of TCO compatible mode vs. Advanced TCO mode. 0 = In the compatible TCO mode. 1 = In the advanced TCO mode.
0	**CRC Error (CRCE) –** R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = This bit is set if a received message contained a CRC error. When this bit is set, the DERR bit of the host status register will also be set. This bit will be set by the controller if a software abort occurs in the middle of the CRC portion of the cycle or an abort happens after the Intel® 631xESB/632xESB I/O Controller Hub has received the final data bit transmitted by an external slave.

24.2.12 AUX_CTL – Auxiliary Control Register (SMBUS – D31:F3)

Register Offset:	SMBASE + 0Dh	Attribute:	R/W
Default Value:	00h	Size:	8 bits
Lockable:	No	Power Well:	Resume

Bit	Description
7:2	Reserved
1	**Enable 32-Byte Buffer (E32B) –** R/W. 0 = Disable. 1 = Enable. When set, the Host Block Data register is a pointer into a 32-byte buffer, as opposed to a single register. This enables the block commands to transfer or receive up to 32-bytes before the Intel® 631xESB/632xESB I/O Controller Hub generates an interrupt.
0	**Automatically Append CRC (AAC) –** R/W. 0 = Will not automatically append the CRC. 1 = Will automatically append the CRC. This bit must not be changed during SMBus transactions or undetermined behavior will result. It should be programmed only once during the lifetime of the function.

24.2.13 SMLINK_PIN_CTL – SMLink Pin Control Register (SMBUS – D31:F3)

Register Offset:	SMBASE + 0Eh	Attribute:	R/W, RO
Default Value:	See below	Size:	8 bits

Note: This register is in the resume well and is reset by RSMRST#.

This register is only applicable in the TCO compatible mode.

Bit	Description
7:3	Reserved
2	**SMLINK_CLK_CTL** – R/W. 0 = Intel® 631xESB/632xESB I/O Controller Hub will drive the SMLINK0 pin low, independent of what the other SMLINK logic would otherwise indicate for the SMLINK0 pin. 1 = The SMLINK0 pin is **not** overdriven low. The other SMLINK logic controls the state of the pin. (Default)
1	**SMLINK1_CUR_STS** – RO. This read-only bit has a default value that is dependent on an external signal level. This pin returns the value on the SMLINK1 pin. This allows software to read the current state of the pin. 0 = Low 1 = High
0	**SMLINK0_CUR_STS** – RO. This read-only bit has a default value that is dependent on an external signal level. This pin returns the value on the SMLINK0 pin. This allows software to read the current state of the pin. 0 = Low 1 = High

24.2.14 SMBUS_PIN_CTL – SMBUS Pin Control Register (SMBUS – D31:F3)

Register Offset:	SMBASE + 0Fh	Attribute:	R/W, RO
Default Value:	See below	Size:	8 bits

Note: This register is in the resume well and is reset by RSMRST#.

Bit	Description
7:3	Reserved
2	**SMBCLK_CTL** – R/W. 1 = The SMBCLK pin is **not** overdriven low. The other SMBus logic controls the state of the pin. 0 = Intel® 631xESB/632xESB I/O Controller Hub drives the SMBCLK pin low, independent of what the other SMB logic would otherwise indicate for the SMBCLK pin. (Default)
1	**SMBDATA_CUR_STS** – RO. This read-only bit has a default value that is dependent on an external signal level. This pin returns the value on the SMBDATA pin. This allows software to read the current state of the pin. 0 = Low 1 = High
0	**SMBCLK_CUR_STS** – RO. This read-only bit has a default value that is dependent on an external signal level. This pin returns the value on the SMBCLK pin. This allows software to read the current state of the pin. 0 = Low 1 = High

24.2.15 SLV_STS – Slave Status Register (SMBUS – D31:F3)

Register Offset:	SMBASE + 10h	Attribute:	R/WC
Default Value:	00h	Size:	8 bits

Note: This register is in the resume well and is reset by RSMRST#.

All bits in this register are implemented in the 64 kHz clock domain. Therefore, software must poll this register until a write takes effect before assuming that a write has completed internally.

Bit	Description
7:1	Reserved
0	**HOST_NOTIFY_STS –** R/WC. The Intel® 631xESB/632xESB I/O Controller Hub sets this bit to a 1 when it has completely received a successful Host Notify Command on the SMLink pins. Software reads this bit to determine that the source of the interrupt or SMI# was the reception of the Host Notify Command. Software clears this bit after reading any information needed from the Notify address and data registers by writing a 1 to this bit. Note that the Intel® 631xESB/632xESB I/O Controller Hub will allow the Notify Address and Data registers to be over-written once this bit has been cleared. When this bit is 1, the Intel® 631xESB/632xESB I/O Controller Hub will NACK the first byte (host address) of any new “Host Notify” commands on the SMLink. Writing a 0 to this bit has no effect.

24.2.16 SLV_CMD – Slave Command Register (SMBUS – D31:F3)

Register Offset:	SMBASE + 11h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

Note: This register is in the resume well and is reset by RSMRST#.

Bit	Description
7:3	Reserved
2	**SMBALERT_DIS –** R/W. 0 = Allows the generation of the interrupt or SMI#. 1 = Software sets this bit to block the generation of the interrupt or SMI# due to the SMBALERT# source. This bit is logically inverted and ANDed with the SMBALERT_STS bit (offset SMBASE + 00h, bit 5). The resulting signal is distributed to the SMI# and/or interrupt generation logic. This bit does not effect the wake logic.
1	**HOST_NOTIFY_WKEN –** R/W. Software sets this bit to 1 to enable the reception of a Host Notify command as a wake event. When enabled this event is “OR”ed in with the other SMBus wake events and is reflected in the SMB_WAK_STS bit of the General Purpose Event 0 Status register. 0 = Disable 1 = Enable
0	**HOST_NOTIFY_INTREN –** R/W. Software sets this bit to 1 to enable the generation of interrupt or SMI# when HOST_NOTIFY_STS (offset SMBASE + 10h, bit 0) is 1. This enable does not affect the setting of the HOST_NOTIFY_STS bit. When the interrupt is generated, either PIRQB# or SMI# is generated, depending on the value of the SMB_SMI_EN bit (D31:F3:40h, bit 1). If the HOST_NOTIFY_STS bit is set when this bit is written to a 1, then the interrupt (or SMI#) will be generated. The interrupt (or SMI#) is logically generated by AND’ing the STS and INTREN bits. 0 = Disable 1 = Enable

24.2.17 NOTIFY_DADDR – Notify Device Address Register (SMBUS – D31:F3)

Register Offset:	SMBASE + 14h	Attribute:	RO
Default Value:	00h	Size:	8 bits

Note: This register is in the resume well and is reset by RSMRST#.

Bit	Description
7:1	**DEVICE_ADDRESS –** RO. This field contains the 7-bit device address received during the Host Notify protocol of the SMBus 2.0 Specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit (D31:F3:SMBASE +10, bit 0) is set to 1.
0	Reserved

24.2.18 NOTIFY_DLOW – Notify Data Low Byte Register (SMBUS – D31:F3)

Register Offset:	SMBASE + 16h	Attribute:	RO
Default Value:	00h	Size:	8 bits

Note: This register is in the resume well and is reset by RSMRST#.

Bit	Description
7:0	**DATA_LOW_BYTE –** RO. This field contains the first (low) byte of data received during the Host Notify protocol of the SMBus 2.0 specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit (D31:F3:SMBASE +10, bit 0) is set to 1.

24.2.19 NOTIFY_DHIGH – Notify Data High Byte Register (SMBUS – D31:F3)

Register Offset:	SMBASE + 17h	Attribute:	RO
Default Value:	00h	Size:	8 bits

Note: This register is in the resume well and is reset by RSMRST#.

Bit	Description
7:0	**DATA_HIGH_BYTE –** RO. This field contains the second (high) byte of data received during the Host Notify protocol of the SMBus 2.0 specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit (D31:F3:SMBASE +10, bit 0) is set to 1.

§§

25 LAN Controller and BMC Registers (Bn:F0/F1/F2/F3/F4/F5/F7)

The Intel® 631xESB/632xESB I/O Controller Hub integrated LAN controller resides at PCI Bus n, Device 0, Function 0 on the secondary side of the Intel® 631xESB/632xESB I/O Controller Hub's virtual PCI-to-PCI bridge. This Bus is assigned a number during PCI bus enumeration, configured by BIOS during system configuration. The LAN controller acts as both a master and a slave on the PCI bus. As a master, the LAN controller interacts with the system main memory to access data for transmission or deposit received data. As a slave, some of the LAN controller's control structures are accessed by the host processor to read or write information to the on-chip registers. The processor also provides the LAN controller with the necessary commands and pointers that allow it to process receive and transmit data.

25.1 LAN Controller Registers (Bn:F0/F1)

Note: Address locations that are not shown should be treated as Reserved (See Section 2.3 for details).

Table 25-1. Intel® 6321ESB I/O Controller Hub Integrated LAN Controller PCI Register Address Map (LAN0 – Bn:F0), (LAN1 – Bn:F1) (Sheet 1 of 3)

Offset	Mnemonic	Register Name	Default	Type
Mandatory PCI Configuration Registers				
00–01h	VID	Vendor Identification	8086h	RO
02–03h	DID	Device Identification	See register desc.	RO
04–05h	PCICMD	PCI Command	0000h	RO, RW
06–07h	PCISTS	PCI Status	0010h	RO, R/WC
08h	RID	Revision Identification	See register desc.	RO
09h	PI	Programming Interface	00h	RO
0Ah	SCC	Sub Class Code	00h	RO
0Bh	BCC	Base Class Code	01h/02h	RO
0Ch	CLS	Cache Line Size	10h	R/W
0Dh	PMLT	Primary Master Latency Timer	00h	R/W
0Eh	HEADTYP	Header Type	00h/80h	RO

Table 25-1. Intel® 6321ESB I/O Controller Hub Integrated LAN Controller PCI Register Address Map (LAN0 – Bn:F0), (LAN1 – Bn:F1) (Sheet 2 of 3)

Offset	Mnemonic	Register Name	Default	Type
BAR registers for 32-bit addressing modes				
10–13h	CSR_MEM_BASE	CSR Memory–Mapped Base Address	00000000h	R/W, RO
14–17h	CSR_FLASH_BASE	CSR Flash Base Address	00000000h	R/W, RO
18–1Bh	CSR_IO_BASE	CSR I/O–Mapped Base Address	00000001h	R/W, RO
2C–2Dh	SVID	Subsystem Vendor Identification	See register desc	RO
2E–2Fh	SID	Subsystem Identification	See register desc	RO
30-33H	CSR_EXP_ROM_BASE	CSR Expansion ROM Base Address	00000000h	R/W
34h	CAP_PTR	Capabilities Pointer	C8h	RO
3Ch	INT_LN	Interrupt Line	00h	R/W
3Dh	INT_PN	Interrupt Pin	01h	RO
3Eh	MIN_GNT	Minimum Grant	00h	RO
3Fh	MAX_LAT	Maximum Latency	00h	RO
PCI Power Management Registers				
C8h	CAP_ID	Capability ID	01h	RO
C9h	NXT_PTR	Next Item Pointer	D0h	RO
CA–CBh	PM_CAP	Power Management Capabilities	See register desc	RO
CC–CDh	PMCSR	Power Management Control/Status	2000h	R/W, RO, R/WC
CF	PCIDATA	PCI Power Management Data	00h	RO
Message Signaled Interrupt Configuration Registers				
D0h	MSI_CAP_ID	MSI Capability ID	05h	RO
D1h	MSI_NXT_PTR	MSI t Next Item Pointer	E0h	RO
D2-D3	MSI_MCR	MSI Control Register	0080	R/W
D4-D7h	MSI_MAR_LOW	MSI Message Low Address	00000000h	R/W
D8-DB	MSI_MAR_HIGH	MSI Message High Address	00000000h	R/W
DC-DD	MSI_MDR	Message Data Register	0000	R/W
PCI Express* Configuration Registers				
E0h	PCI Express_CAP_ID	PCI Express Capability Identification Register	10h	RO
E1h	PCI Express_NXT_PTR	PCI Express Next Item Pointer	00h	RO
E2-E3	PCI Express_CAP	PCI Express Capability	0001h	RO
E4-E7h	PCI Express_DEV_CAP	PCI Express Device Capability	00000CC1h	RO
E8-E9	PCI Express_DEV_CONT	PCI Express Device Control	2810h	R/W
EA-EB	PCI Express_DEV_STATUS	PCI Express Device Status	0000h	RO
EC-EF	PCI Express_LINK_CAP	PCI Express Link Capability	See register desc	RO
F0-F1	PCI Express_LINK_CONT	PCI Express Link Control	0000h	R/W
F2-F3	PCI Express_LINK_STATUS	PCI Express Link Status	1041h	RO
PCI Express* Extended Configuration Registers				
100-103h	PCI Express_EXT_CAP_ID	PCI Express Extended Capability Identification Register	00010001h	RO

Table 25-1. Intel® 6321ESB I/O Controller Hub Integrated LAN Controller PCI Register Address Map (LAN0 – Bn:F0), (LAN1 – Bn:F1) (Sheet 3 of 3)

Offset	Mnemonic	Register Name	Default	Type
104-107h	UNCORR_ERR_STATUS	Uncorrectable Error Status	00000000h	R/WCS
108-10Bh	UNCORR_ERR_MASK	Uncorrectable Error Mask	00000000h	R/WS
10C-10Fh	UNCORR_ERR_SEV	Uncorrectable Error Severity	00062011h	R/WS
110-113h	CORR_ERR_STATUS	Correctable Error Status	00000000h	R/WCS
114-117h	CORR_ERR_MASK	Correctable Error Mask	00000000h	R/WS
118-11Bh	FST_ERR_PT	First Error Pointer	00000000h	RO
11C-128h	HEAD_LOG	Head Log	0h	RO

25.1.1 VID – Vendor Identification Register (Bn:F0/F1)

Offset Address: 00–01h Attribute: RO
Default Value: 8086h Size: 16 bits

Bit	Description
15:0	**Vendor ID** – RO. This is a 16-bit value assigned to Intel.

25.1.2 DID – Device Identification Register (Bn:F0/F1)

These are the Device ID values which should be put in the EEPROM for the various LAN modes.

Offset Address: 02–03h Attribute: RO
Default Value: See bit description Size: 16 bits

Bit	Description
15:0	Device ID – RO. This is a 16-bit value assigned to the Intel® 6321ESB I/O Controller Hub integrated LAN controller. 1. LAN0: If Word 0Ah bit 0 is set in the EEPROM, the Device ID is loaded from the EEPROM, Word 0Dh after the hardware reset. If not set, the default value is 1081h. 2. LAN1: If Word 0Ah bit 0 is set in the EEPROM, the Device ID is loaded from the EEPROM, Word 11h after the hardware reset. If not set the default value is 1081h. 1096h = Intel® 6321ESB I/O Controller Hub IOAT LAN Copper: Dual Port 10/100/1000mbit Ethernet controller integrated into Intel® 6321ESB I/O Controller Hub, copper interface, with IO Acceleration Technology 1097h = Intel® 6321ESB I/O Controller Hub IOAT LAN fiber: Dual Port 1000mbit Ethernet controller integrated into Intel® 6321ESB I/O Controller Hub; using fiber media from serdes port, with IO Acceleration Technology 1098h = Intel® 6321ESB I/O Controller Hub IOAT LAN SERDES: Dual Port 1000mbit Ethernet controller, 1000base-x backplane, with IO Acceleration Technology 10BAh= Intel® 6321ESB I/O Controller Hub IOAT LAN Copper: Single Port 10/100/1000 Mb Ethernet controller integrated into ESB2, with Intel I/O Acceleration Technology 10BBh= Intel® 6321ESB I/O Controller Hub IOAT LAN Super Pass Through (SPT) SERDES: Single Port 10/100/1000 Mb Ethernet controller integrated into Intel® 6321ESB I/O Controller Hub, with Intel I/O Acceleration Technology.

25.1.3 PCICMD – PCI Command Register (Bn:F0/F1)

Offset Address: 04–05h
Default Value: 0000h
Attribute: RO, R/W
Size: 16 bits

Bit	Description
15:11	Reserved
10	**Interrupt Disable** – R/W. 0 = Enable. 1 = Disables LAN controller to assert its INTA/INTB signal. ***Note:*** The Interrupt Disable register bit is a read-write bit that controls the ability of a PCI Express device to generate a legacy interrupt message. When set, devices are prevented from generating legacy interrupt messages.
9	**Fast Back to Back Enable (FBE)** – RO. Hardwired to 0. The integrated LAN controller will not run fast back-to-back PCI cycles.
8	**SERR# Enable (SERR_EN) –** R/W. 0 = Disable. 1 = Enable.
7	**Wait Cycle Enable (WCE) –** RO. Hardwired to 0. Not implemented.
6	**Parity Error Response (PER) –** R/W. 0 = The LAN controller will set PCISTS[8] upon receiving poisoned completion. 1 = The LAN controller will not set PCISTS[8] upon receiving poisoned completion.
5	**Palette Snoop Enable (PSE) –** RO. Hardwired to 0. Not Implemented.
4	**Memory Write and Invalidate Enable (MWIE) –** RO. Hardwired to 0. Not Implemented.
3	**Special Cycle Enable (SCE)** – RO. Hardwired to 0. The LAN controller ignores special cycles.
2	**Bus Master Enable (BME)** – R/W. 0 = Disable. 1 = Enable. The Intel® 6321ESB I/O Controller Hub's integrated LAN controller may function as a PCI bus master.
1	**Memory Space Enable (MSE) –** R/W. 0 = Disable. 1 = Enable. The Intel® 6321ESB I/O Controller Hub's integrated LAN controller will respond to the memory space accesses.
0	**I/O Space Enable (IOSE) –** R/W. 0 = Disable. 1 = Enable. The Intel® 6321ESB I/O Controller Hub's integrated LAN controller will respond to the I/O space accesses.

25.1.4 PCISTS – PCI Status Register (Bn:F0/F1)

Offset Address: 06–07h
Default Value: 0010h
Attribute: RO, R/WC
Size: 16 bits

Note: For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 to the bit has no effect.

Bit	Description
15	Detected Parity Error **(**DPE) – R/WC. When set, indicates that a poisoned completion was received.
14	Signaled System Error **(**SSE) – R/WC. When set, indicates that the LAN controller has sent an uncorrectable error message.
13	**Master Abort Status** (**RMA) –** R/WC. When set, indicates that the LAN controller has received a completion with unsupported request status.
12	**Received Target Abort (RTA) –** R/WC. When set, indicates that the LAN controller has received a completion with completion abort status.

Bit	Description
11	**Signaled Target Abort (STA) –** R/WC. When set, indicates that the LAN controller has sent a completion with completion abort status.
10:9	**DEVSEL Timing –** RO. Hardwired to 0.
8	**Data Parity Error Detected (DPED) –** R/WC. This bit will be set when PCICMD[6] is set and a poisoned completion was received.
7	**Fast Back to Back Capable (FB2BC)** – RO. Hardwired to 0. Not implemented.
6	Reserved.
5	**66 MHz Capable (66MHZ_CAP)** – RO. Hardwired to 0. Not implemented.
4	**Capabilities List (CAP_LIST) –** RO.Indicates that a device implements Extended Capabilities. This bit is hardwrite to 1.
3	**Interrupt Status (INTS) –** RO. This bit indicates that an interrupt is pending. It is independent from the state of the Interrupt Enable bit in the command register.
2:0	Reserved

25.1.5 RID – Revision Identification Register (Bn:F0/F1)

Offset Address: 08h Attribute: RO
Default Value: See bit description Size: 8 bits

Bit	Description
7:0	**Revision ID (RID)** – RO. This field value is set by the CRID mechanism described in Section 25.1.41. ***Note:*** LAN 0 and LAN 1 functions have the same revision ID.

25.1.6 PI – Programming Interface Register (Bn:F2)

Offset Address: 09h Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Description
7:0	**Programming Interface(PI)** – RO. This 8-bit value specifies the class code as the programming i/f class.

25.1.7 SCC – Sub Class Code Register (Bn:F0/F1)

Offset Address: 0Ah Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Description
7:0	**Sub Class Code (SCC)** – RO. This 8-bit value specifies the sub class of the device as an Ethernet controller.

25.1.8 BCC – Base Class Code Register (Bn:F0/F1)

Offset Address: 0Bh Attribute: RO
Default Value: 01h/02h Size: 8 bits

Bit	Description
7:0	**Base Class Code (BCC)** – RO. This 8-bit value specifies the base class of the device as a network controller.

25.1.9 CLS – Cache Line Size Register (Bn:F0/F1)

Offset Address: 0Ch
Default Value: 10h
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	Cache Line Size(CLS) – R/W. 0x10 is the hardware default for this register.

25.1.10 PMLT – Primary Master Latency Timer Register (Bn:F0/F1)

Offset Address: 0Dh
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	Reserved

25.1.11 HEADTYP – Header Type Register (Bn:F0/F1)

Offset Address: 0Eh
Default Value: 00h, 80h
Attribute: RO
Size: 8 bits

Bit	Description
7	**Multi-Function Device (MFD) –** RO. Hardwired to 0 to indicate a single function device, that is, If only a single function is active. 1 for multiple function
6:0	**Header Type (HTYPE) –** RO. This 7-bit field identifies the header layout of the configuration space as an Ethernet controller.

25.1.12 Base Address Registers (Bn:F0/F1)

The Base Address Registers (or BARs) are used to map the register space of the various functions.

25.1.12.1 CSR_MEM_BASE – CSR Memory-Mapped Base Address Register (Bn:F0/F1)

Offset Address: 10–13h
Default Value: 00000000h
Attribute: R/W, RO
Size: 32 bits

Note: The Intel® 6321ESB I/O Controller Hub's integrated LAN controller requires one BAR for memory mapping. Software determines which BAR (memory or I/O) is used to access the LAN controller's CSR registers.

Bit	Description
31:17	**Base Address (MEM_ADDR) –** R/W. This field contains the upper 15 bits of the base address provides 128KB of memory-Mapped space for the LAN controller's Control/Status registers.
16:4	Reserved
3	**Prefetchable (MEM_PF)** – RO. Hardwired to 0 to indicate that this is not a pre-fetchable memory-Mapped address range.
2:1	**Type (MEM_TYPE)** – RO. Hardwired to 00b to indicate the memory-Mapped address range may be located anywhere in 32-bit address space.
0	**Memory-Space Indicator (MEM_SPACE)** – RO. Hardwired to 0 to indicate that this base address maps to memory space.

25.1.12.2 CSR_FLASH_BASE – CSR Flash Base Address Register (Bn:F0/F1)

Offset Address:	14–17h	Attribute:	R/W, RO
Default Value:	00000000h	Size:	32 bits

Note: 1. The Intel® 6321ESB I/O Controller Hub's integrated LAN controller requires one BAR for Flash mapping. Software determines which BAR (memory or I/O) is used to access the LAN controller's CSR registers.

2. This BAR exist depending on EEPROM setting.

Bit	Description
31:24/16	**Base Address (MEM_ADDR) –** R/W. This field contains the upper 20 bits of the base address and provides 4 Kbytes of memory-Mapped space for the LAN controller's memory mapped flash.
23/15:4	Reserved
3	**Prefetchable (MEM_PF)** – RO. Hardwired to 0 to indicate that this is not a pre-fetchable memory-Mapped address range.
2:1	**Type (MEM_TYPE)** – RO. Hardwired to 00b to indicate the memory-Mapped address range may be located anywhere in 32-bit address space.
0	**Memory-Space Indicator (MEM_SPACE)** – RO. Hardwired to 0 to indicate that this base address maps to memory space.

25.1.12.3 CSR_IO_BASE – CSR I/O-Mapped Base Address Register (Bn:F0/F1)

Offset Address:	18–1Bh	Attribute:	R/W, RO
Default Value:	00000001h	Size:	32 bits

Note: 1. The Intel® 6321ESB I/O Controller Hub's integrated LAN controller requires one BAR for I/O mapping. Software determines which BAR (memory or I/O) is used to access the LAN controller's CSR registers.

2. This BAR exist depending on EEPROM setting.

Bit	Description
31:5	**Base Address (IO_ADDR)** – R/W. This field provides 32 bytes of I/O-Mapped address space for the LAN controller's Control/Status registers.
4:1	Reserved
0	**I/O Space Indicator (IO_SPACE)** – RO. Hardwired to 1 to indicate that this base address maps to I/O space.

25.1.13 SVID – Subsystem Vendor Identification(Bn:F0/F1)

Offset Address:	2C–2D	Attribute:	RO
Default Value:	8086h	Size:	16 bits

Bit	Description
15:0	**Subsystem Vendor ID (SVID)** – RO. This value may be loaded automatically from the EEPROM address 0Ch upon power up or reset if Word 0Ah bit 1 is set. A value of 0x8086 is default for this field upon power up if the EEPROM does not respond or is not programmed.

25.1.14 SID – Subsystem Identification (Bn:F0/F1)

Offset Address: 2E–2Fh
Default Value: 0000h
Attribute: RO
Size: 16 bits

Bit	Description
15:0	**Subsystem ID (SID)** – RO. This value may be loaded automatically from the EEPROM address 0Bh upon power up if Word 0Ah bit 1 is set. A value of 0x0000 is default for this field upon power up if the EEPROM does not respond or is not programmed.

25.1.15 CSR_EXP_ROM_BASE – CSR Expansion ROM Base Address

Offset Address: 30–33h
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

Bit	Description
31:11	**Base Address (EXP_ROM_ADDR)** – R/W. Hardwired to 0 depending on the memory mapping window size. The LAN Expansion ROM spaces can be either 64K, up to 8MB in power of 2. Mapping window size is set by the EEPROM word 0Fh.
10:1	Reserved
0	**Expansion ROM Access Enable (EXP_ROM_EN)** – R/W. 1 enables expansion ROM access. 0 disables expansion ROM access.

This register is used to define the address and size information for boot-time access to the optional FLASH memory. Only the LAN 0/LAN 1 and IDE functions may have this window. It is enabled by the EEPROM words 24h, 14h and 1Ch for LAN 0, LAN 1 and IDE functions respectively. This register returns zero value for functions without expansion ROM window.

25.1.16 CAP_PTR – Capabilities Pointer (Bn:F0/F1)

Offset Address: 34h
Default Value: C8h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Capabilities Pointer (CAP_PTR)** – RO. Hardwired to C8h to indicate the offset within configuration space for the location of the Power Management registers.

25.1.17 INT_LN – Interrupt Line Register (Bn:F0/F1)

Offset Address: 3Ch
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	**Interrupt Line (INT_LN) –** R/W. This field identifies the system interrupt line to which the LAN controller's PCI interrupt request (as defined in the Interrupt Pin Register) is routed.

25.1.18 INT_PN – Interrupt Pin Register (Bn:F0/F1)

Offset Address: 3Dh
Default Value: 01h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Interrupt Pin (INT_PN)** – RO. LAN 0 / LAN 1 - A value of 01h / 02h indicates that this function implements legacy interrupt on INTA# / INTB# respectively. Loaded from EEPROM word 24h / 14h for LAN 0 and LAN 1 respectively.

25.1.19 MIN_GNT – Minimum Grant Register (Bn:F0/F1)

Offset Address: 3Eh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Minimum Grant (MIN_GNT)** – RO. Not used, hardwired to 00h.

25.1.20 MAX_LAT – Maximum Latency Register (Bn:F0/F1)

Offset Address: 3Fh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Maximum Latency (MAX_LAT)** – RO. Not used, hardwired to 00h.

25.1.21 CAP_ID – Capability Identification Register (Bn:F0/F1)

Offset Address: C8h
Default Value: 01h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Capability ID (CAP_ID)** – RO. Hardwired to 01h to indicate that the Intel® 6321ESB I/O Controller Hub's integrated LAN controller supports PCI Power Management.

25.1.22 NXT_PTR – Next Item Pointer (Bn:F0/F1)

Offset Address: C9h
Default Value: D0h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Next Item Pointer (NXT_PTR)** – RO. Hardwired to D0h to indicate that MSI is the next capability item in the capabilities list.

25.1.23 PM_CAP – Power Management Capabilities (Bn:F0/F1)

Offset Address: CA–CBh
Default Value: See bit description
Attribute: RO
Size: 16 bits

Bit	Description
15:11	**PME Support (PME_SUP)** – RO. This 5-bit field indicates the power states in which the LAN controller may assert PME#. The default value depends on EEPROM word 0Ah. 00000b = No PME at all states. 01001b = PME at D0 and $D3_{hot}$ 11001b = PME at D0, $D3_{hot}$ and $D3_{cold}$
10:9	**Hardwired to '0'.**
8:6	**Auxiliary Current (AUX_CUR)** – RO. Hardwired to 000b to indicate that the LAN controller implements the Data registers.
5	**Device Specific Initialization (DSI)** – RO. Hardwired to 1 to indicate that special initialization of this function is required (beyond the standard PCI configuration header) before the generic class device driver is able to use it. DSI is required for the LAN controller after D3-to-D0 reset.
4	Reserved
3	**PME Clock (PME_CLK)** – RO. Hardwired to 0 to indicate that the LAN controller does not require a clock to generate a power management event.
2:0	**Version (VER) –** RO. Hardwired to 010b to indicate that the LAN controller complies with of the *PCI Power Management Specification, Revision 1.1.*

25.1.24 PMCSR – Power Management Control Status Register (Bn:F0/F1)

Offset Address: CC–CDh
Default Value: 2000h
Attribute: RO, R/W, R/WC
Size: 16 bits

Bit	Description
15	PME Status **(PME_STAT)** – R/WC. 0 = Software clears this bit by writing a 1 to it. This also de-asserts the PE_WAKE# signal, when enabled, and stops PM_PME messages transmission. 1 = Set upon occurrence of a wakeup event, independent of the state of the PME enable bit.
14:13	**Data Scale (DSCALE) –** RO. This field indicates the data register scaling factor. It equals 01b for all supported registers: 0,3,4,7 and 8, as selected by the “Data Select” field.
12:9	**Data Select (DSEL) –** R/W. This field is used to select which data is reported through the Data register and Data Scale field.
8	**PME Enable (PME_EN)** – R/W. This bit enables the Intel® 6321ESB I/O Controller Hub’s integrated LAN controller to set a Power Management Event in order to wake the system, through the PE_WAKE# signal or through a PM_PME message. 0 = The device will not set a PME event. 1 = Enable setting PME event when PME Status is set.
7:2	Reserved
1:0	**Power State (PWR_ST) –** R/W. This 2-bit field is used to determine the current power state of the integrated LAN controller, and to put it into a new power state. The definition of the field values is as follows: 00 = D0 01/10 = Reserved 11 = D3

25.1.25 PCIDATA – PCI Power Management Data Register (Bn:F0/F1)

Offset Address: CFh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Power Management Data (PWR_MGT) –** RO. State dependent power consumption and heat dissipation data.

This optional register is used to report power consumption and heat dissipation. Reported register is controlled by the Data_Select field in the PMCSR, and the power scale is reported in the Data_Scale field in the PMCSR. The data of this field is loaded from the EEPROM if PM is enabled in the EEPROM or with a default value of 0x00 otherwise. The values for Intel® 6321ESB I/O Controller Hub LAN controller functions is shown in Table 25.2.

Table 25-2. Data Register Structure

Function	D0 (consume/dissipate)	D3 (consume/dissipate)	Common	Data_Scale
Data_Select	(0x0 / 0x4)	(0x3 / 0x7)	(0x8)	
Function 0	EEP addr 22h	EEP addr 22h [4:0]	EEP addr 22h [7:5]	01b
Function 1	EEP addr 22h	EEP addr 22h [4:0]	EEP addr 22h [7:5]	01b

25.1.26 MSI_CAP_ID – Capability Identification Register (Bn:F0/F1)

Offset Address: D0h
Default Value: 05h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Capability ID (CAP_ID)** – RO. Hardwired to 05h to indicate that the linked list item is being the Message Signaled Interrupt registers.

25.1.27 MSI_NXT_PTR – Next Item Pointer (Bn:F0/F1)

Offset Address: D1h
Default Value: E0h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Next Item Pointer (NXT_PTR)** – RO. Hardwired to E0h to indicate that PCI Express capability is the next item in the capability list.

25.1.28 MSI_MCR – Message Control Register (Bn:F0/F1)

Offset Address: D2–D3h
Default Value: 0080h
Attribute: RO
Size: 16 bits

Bit	Description
15:8	Reserved. Reads as 0.
7	**64 Support (64_SUP)** – RO. Hardwired to 1 to indicate that the LAN controller is capable of generating 64 bit message addresses.
6:4	**Multiple Message Enable(MM_ENABLE)** – RO. Hardwired to 000b to indicate that the LAN controller supports single message per function.
3:1	**Multiple Message Capable(MM_CAP)** – RO. Hardwired to 000b to indicate that the LAN controller capable of single requested message per function.
0	**MSI ENABLE(MSI_ENABLE) –** R/W. If 1, the LAN controller will generate MSI for interrupt assertion instead of INTx signaling.

25.1.29 MSI_MAR_LOW – Message Address Low Register (Bn:F0/F1)

Offset Address: D4–D7h
Default Value: 00000000h
Attribute: RO, R/W, R/WC
Size: 32 bits

Bit	Description
31:0	**Message Address Low(MSG_ADDR_LOW) –** R/W. Written by the system to indicate the lower 32 bits of the address to use for the MSI memory write transaction. The lower two bits will always return 0 regardless of the write operation.

25.1.30 MSI_MAR_HIGH – Message Address High Register (Bn:F0/F1)

Offset Address: D8–DBh
Default Value: 0000h
Attribute: RO, R/W, R/WC
Size: 16 bits

Bit	Description
31:0	**Message Address High(MSG_ADDR_HIGH) –** R/W. This field contains the upper 32 bits of the address to use for the MSI memory write transaction.

25.1.31 MSI_MDR – Message Data Register (Bn:F0/F1)

Offset Address: DC–DDh
Default Value: 0000h
Attribute: R/W
Size: 16 bits

Bit	Description
15:0	**Message Data(MSG_DATA) –** R/W. Written by the system to indicate the lower 16 bits of the data written in the MSI memory write DWORD transaction. The upper 16 bits of the transaction are written as 0

25.1.32 PCI Express_CAP_ID – PCI Express* Capability Identification Register (Bn:F0/F1)

Offset Address: E0h
Default Value: 10h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Capability ID (CAP_ID)** – RO. Hardwired to 10h to indicate that the linked list item is being the PCI Express Capability Registers.

25.1.33 PCI Express_NXT_PTR – PCI Express* Next Item Pointer (Bn:F0/F1)

Offset Address: E1h
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Next Item Pointer (NXT_PTR)** – RO. Hardwired to 00h to indicate that it is the last item in the capability linked list.

25.1.34 PCI Express_CAP – PCI Express* Capability Register (Bn:F0/F1)

Offset Address: E2–E3h
Default Value: 0001h
Attribute: RO
Size: 16 bits

Bit	Description
15:14	Reserved.
13:9	**Interrupt Message Number (INT_MSG_NUM)** – RO. Multiple MSI per function is not supported. Hardwired to 00000b
8	**Slot Implemented** – RO. Slot option not implemented hardwired to 0.
7:4	**Device/Port Type** – RO. Indicates the type of PCI Express functions. Hardwired to 0001b
3:0	**Capability version(CAP_VERSION) –** RO. Indicates the PCI Express capability structure version number 0001b.

25.1.35 PCI Express_DEV_CAP – PCI Express* Device Capability Register (Bn:F0/F1)

Offset Address: E4–E7h
Default Value: 00000CC1h
Attribute: RO, R/W, R/WC
Size: 32 bits

Bit	Description
31:28	Reserved.
27:26	**Slot Power Limit Scale** – RO. Used in upstream port only. Hardwired to 00b.
25:18	**Slot Power Limit Value** – RO. Used in upstream port only. Hardwired to 00b
17:15	Reserved.
14	**Power Indicator Present** – RO. Hardwired to 0b
13	**Attention Indicator Present** – RO. Hardwired to 0b
12	**Attention Button Present** – RO. Hardwired to 0b

Bit	Description
11:9	**Endpoint L1 Acceptable Latency** – RO. This field indicates the acceptable latency that Intel® 6321ESB I/O Controller Hub LAN can withstand due to the transition from L1 state to the L0 state. All functions share the same value loaded from the EEPROM PCI Express* init configuration 1 Word 18h
8:6	**Endpoint L0s Acceptable Latency** – L0s is not supported by Intel® 6321ESB I/O Controller Hub LAN.
5	**Extended Tag Field Supported –** RO. Max supported size of the Tag field. Intel® 6321ESB I/O Controller Hub supported 5-bit Tag field for all functions.
4:3	**Phantom Function Supported** – RO. Hardwired to 00b. Not supported.
2:0	**Max Payload Size Supported** – RO. This field indicates the maximum payload that the device can support for TLPs. It is loaded from the EEPROM PCI Express init configuration 3 Word 1Ah bit 8 with a default value of 256B.

25.1.36 PCI Express_DEV_CONT – PCI Express* Device Control Register (Bn:F0/F1)

Offset Address: E8–E9h
Default Value: 2810h
Attribute: RO, R/W
Size: 16 bits

Bit	Description
15	Reserved.
14:12	**Max Read Request Size** - this field sets maximum read request size for the Device as a requester. The default value is 010b (512B) for the LAN devices.
11	**Enable No Snoop** – R/W. Snoop is gated by NONSNOOP bits in the GCR register in the CSR space. Default is 1b
10	**Auxiliary Power PM Enable** - when set enables the device to draw AUX power independent of PME AUX power.
9	**Phantom Function Enable** – RW. Hardwired to 0b
8	**Extended Tag Field Enable** – RW. Hardwired to 0b
7:5	**Max Payload Size** – RW. This field sets maximum TLP payload size for the device functions. As a receiver the device must handle TLPs as large as the set value. As transmitter, the device must not generate TLPs exceeding the set value.The Max Payload Size Supported in the device capabilities register indicates permissible values that can be programmed. Default value is 000b(128 Bytes)
4	**Enable Relaxed Ordering** – If this bit is set, the device is permitted to set the Relaxed Ordering bit in the attribute field of write transactions that do not need strong ordering. Default to 1b
3	**Unsupported Request Reporting Enable** – RW. Enable error report.
2	**Fatal Error Reporting Enable** – RW. Enable error report.
1	**Non-Fatal Error Reporting Enable** – RW. Enable error report.
0	**Correctable Error Reporting Enable** – RW. Enable error report.

25.1.37 PCI Express_DEV_STATUS – PCI Express* Device Status Register (Bn:F0/F1)

Offset Address: EA–EBh
Default Value: 0000h
Attribute: RO, R/W, R/WC
Size: 16 bits

Bit	Description
15:6	Reserved.
5	**Transaction Pending** – RO. Indicates whether Intel® 6321ESB I/O Controller Hub LAN has any transaction pending.
4	**Aux Power Detected**– RO. Hardwired to '1'

Bit	Description
3	**Unsupported Request Detected** – R/WC. Indicates that Intel® 6321ESB I/O Controller Hub LAN received an unsupported request. Intel® 6321ESB I/O Controller Hub LAN can't distinguish which function causes the error.
2	**Fatal Error Detected** – R/WC. Indicates status of fatal error detection.
1	**Non-Fatal Error Detected** – R/WC. Indicates status of non-fatal error detection.
0	**Correctable Error Detected** – R/WC. Indicates status of correctable error detection.

25.1.38 PCI Express_LINK_CAP – PCI Express* Link Capability Register (Bn:F0/F1)

Offset Address: EC–EFh Attribute: RO, R/W
Default Value: See description Size: 16 bits

Bit	Description
31:24	**Port Number** – RO. The PCI Express* port number for the given PCI Express Link. Field is set in the Link training phase. Default to 0x0.
23:18	Reserved.
17:15	**L1 Exit Latency**- Indicates the exit latency from L1 to L0 state. This field is loaded from the EEPROM PCI Express init configuration 1 Word 18h. Default to 110b (32-64us).
14:12	**L0s Exit Latency**-L0s is not supported by Intel® 6321ESB I/O Controller Hub LAN.
11:10	**Active State Link PM Support** – RO. Indicates the level of active state power management supported in Intel® 6321ESB I/O Controller Hub LAN.This field is loaded from the EEPROM PCI Express init configuration 3 Word 1Ah. Intel® 6321ESB I/O Controller Hub LAN does not support L1 and L0s, hence the encoding should be 00b
9:4	**Max Link Width** – RO. Indicates the max link width. Intel® 6321ESB I/O Controller Hub LAN controller can support by 4-link width. The field is loaded from the EEPROM PCI Express init configuration 3 Word 1Ah with a default value of 4 lanes. Default to 00100b
3:0	**Max Link Speed** – RO. Indicates a max link speed of 2.5 Gbps. Default to 0001b

25.1.39 PCI Express_LINK_CONT – PCI Express* Link Control Register (Bn:F0/F1)

Offset Address: F0–F1h Attribute: R/W
Default Value: 0000h Size: 16 bits

Bit	Description
15:8	Reserved.
7	**Extended Synch** – RW. This bit forces extra TS2 transmission at recovery from L1 prior to L0.
6	**Common Clock Configuration** – RW. When set indicates that Intel® 6321ESB I/O Controller Hub and the component at the other end of the link are operating with a common reference clock. A value of 0 indicates that they operating with an asynchronous clock. This parameter affects the L1 Exit Latency.
5	**Retrain Clock** – RO. Not applicable for endpoint devices, hardwired to 0.
4	**Link Disable** – RO. Not applicable for endpoint devices, hardwired to 0.

Bit	Description
3	**Read Completion Boundary** – RW.
2	Reserved.
1:0	**Active State Link PM Control –** R/W. this field controls the active state PM supported on the link. Link PM functionality is determined by the lowest common denominator of all functions. Defined encodings are: 00b ASPM Disabled 01b L0s Entry Supported 10b Reserved 11b L0s and L1 Supported Intel® 6321ESB I/O Controller Hub LAN does not support L0s and L1 ASPM

25.1.40 PCI Express_LINK_STATUS – PCI Express* Link Status Register (Bn:F0/F1)

Offset Address: F2–F3h
Default Value: 1041h
Attribute: R/W
Size: 16 bits

Bit	Description
15:13	Reserved.
12	**Slot Clock Configuration** – When set, it indicates it uses the physical reference clock that the platform provides on the connector. This bit value is loaded from EEPROM word 1Ah. Default is 1.
11	**Link Training** – RO. Indicates that link training is in progress.
10	**Link Training Error** – RO. Hardwire to 0
9:4	**Negotiated Link Width** – RO. Indicates the negotiated width of the link.
3:0	**Link Speed** – RO. Indicates the negotiated link speed. 0001b is the only defined speed which is 2.5 Gbps.

25.1.41 CRID Implementation

As part of the Intel® 6321ESB I/O Controller Hub LAN controller development, the CRID mechanism is implemented. This mechanism allows for the BIOS to change the Revision ID of the chipset components to achieve compatibility to a given SW image. The mechanism consist of a write once by the BIOS of a key into the RevID register that will fix the revision ID returned by the different PCI Express functions.

25.1.41.1 Assumptions and Guidelines

- As each PCI Express function in Intel® 6321ESB I/O Controller Hub LAN controller can be disabled, we need a mechanism that is independent of which function is enabled.
- In order to keep flexibility, the CRID values will be stored in EPROM.

25.1.41.2 Implementation

After PCI Express reset 3 CRID values will be read from the EPROM and stored in registers. The default values of these registers if no EPROM is present are equal to the RevID.

A write of a key to RevID (8 lower bits of address 0x8 in PCI Express configuration space) of any of the function will lock the key value into a register common to all functions. After this write, the RevID will become read only until the next PCI Express reset or power up reset.

This key value will fix which value is read back when the RevID register of any function is accessed according to the following table:

Table 25-3. RevID Register

Key	CRID #
0x1D	CRID #1
0x2D	CRID #2
0x3D	CRID #3
Other	RevID

25.1.41.3 RevID Register Description

In any of Intel® 6321ESB I/O Controller Hub LAN controller's PCI Express config space:

Offset	Byte 3	Byte 2	Byte 1	Byte 0
0xB - 0x8	Class Code (RO) Default according to function			Revision ID (Write once, after that RO) Values from EPROM.

25.1.42 PCI Express* Extended Configuration Registers

PCI Express Extended Configuration Register is allocated using a linked list of optional or required PCI Express extended capabilities following a format resembling PCI capability structures. The first PCI Express extended capability is located at offset 0x100 in the device configuration space. The first DWORD of the capability structure identifies the capability/version and points to the next capability.

25.1.42.1 PCI Express Extended Capability Identification Register

Bit	Description
31:20	**Next Capability Pointer** – RO. Next PCI Express Extended Capability Pointer
19:16	**Version Number** – RO. PCI Express Advanced Error Reporting Extended Capability Version Number
15:0	**Extended Capability ID** – RO. PCI Express Extended Capability ID indicating Advanced Error Reporting Capability

25.1.42.2 Uncorrectable Error Status

The Uncorrectable Error Status register reports error status of individual uncorrectable error sources on a PCI Express device. An individual error status bit that is set to "1" indicates that a particular error occurred; software may clear an error status by writing a 1 to the respective bit.

Bit	Description
31:21	Reserved
20	**Unsupported Request Error Status** – R/WCS
19	**ECRC Error Status (Optional)** – R/WCS
18	**Malformed TLP Status** – R/WCS
17	**Receiver Overflow Status (Optional)** – R/WCS
16	**Unexpected Completion Status** – R/WCS
15	**Completer Abort Status (Optional)** – R/WCS

Bit	Description
14	**Completion Timeout Status** – R/WCS
13	**Flow Control Protocol Error Status (Optional)** – R/WCS
12	**Poisoned TLP Status** – R/WCS
11:5	Reserved
4	**Data Link Protocol Error Status** – R/WCS
3:1	Reserved
0	**Training Error Status (Optional)** – R/WCS

25.1.42.3 Uncorrectable Error Mask

The Uncorrectable Error Mask register controls reporting of individual uncorrectable errors by device to the host bridge via a PCI Express error message. A masked error (respective bit set in mask register) is not reported to the host bridge by an individual device. There is a mask bit per bit of the Uncorrectable Error Status register.

Bit	Description
31:21	Reserved
20	**Unsupported Request Error Status** – R/WS
19	**ECRC Error Status (Optional)** – R/WS
18	**Malformed TLP Status** – R/WS
17	**Receiver Overflow Status (Optional)** – R/WS
16	**Unexpected Completion Status** – R/WS
15	**Completer Abort Status (Optional)** – R/WS
14	**Completion Timeout Status** – R/WS
13	**Flow Control Protocol Error Status (Optional)** – R/WS
12	**Poisoned TLP Status** – R/WS
11:5	Reserved
4	**Data Link Protocol Error Status** – R/WS
3:1	Reserved
0	**Training Error Status (Optional)** – R/WS

25.1.42.4 Uncorrectable Error Severity

The Uncorrectable Error Severity register controls whether an individual uncorrectable error is reported as a fatal error. An uncorrectable error is reported as fatal when the corresponding error bit in the severity register is set. If the bit is cleared, the corresponding error is considered fatal. If the bit is set, the corresponding error is considered non-fatal.

Bit	Description
31:21	Reserved
20	**Unsupported Request Error Status** – R/WS
19	**ECRC Error Status (Optional)** – R/WS
18	**Malformed TLP Status** – R/WS
17	**Receiver Overflow Status (Optional)** – R/WS
16	**Unexpected Completion Status** – R/WS

Bit	Description
15	**Completer Abort Status (Optional)** – R/WS
14	**Completion Timeout Status** – R/WS
13	**Flow Control Protocol Error Status (Optional)** – R/WS
12	**Poisoned TLP Status** – R/WS
11:5	Reserved
4	**Data Link Protocol Error Status** – R/WS
3:1	Reserved
0	**Training Error Status (Optional)** – R/WS

25.1.42.5 Correctable Error Status

The Correctable Error Status register reports error status of individual correctable error sources on a PCI Express device. When an individual error status bit is set to “1” it indicates that a particular error occurred; software may clear an error status by writing a 1 to the respective bit.

Bit	Description
31:13	Reserved
12	**Replay Timer Timeout Status** – R/WCS
11:9	Reserved
8	**REPLAY_NUM Rollover Status** – R/WCS
7	**Bad DLLP Status** – R/WCS
6	**Bad TLP Status** – R/WCS
5:1	Reserved
0	**Receiver Error Status (Optional)** – R/WCS

25.1.42.6 Correctable Error Mask

The Correctable Error Mask register controls reporting of individual correctable errors by device to the host bridge via a PCI Express error message. A masked error (respective bit set in mask register) is not reported to the host bridge by an individual device. There is a mask bit per bit in the Correctable Error Status register.

Bit	Description
31:13	Reserved
12	**Replay Timer Timeout Status** – R/WCS
11:9	Reserved
8	**REPLAY_NUM Rollover Status** – R/WCS
7	**Bad DLLP Status** – R/WCS
6	**Bad TLP Status** – R/WCS
5:1	Reserved
0	**Receiver Error Status (Optional)** – R/WCS

25.1.42.7 First Error Pointer

The First Error Pointer is a read-only register that identifies the bit position of the first uncorrectable error reported in the Uncorrectable Error Status register.

Bit	Description
31:4	Reserved
3:0	Vector pointing to the first recorded error in the Uncorrectable Error Status register.

25.1.42.8 Header Log

The header log register captures the header for the transaction that generated an error. This register is 16 bytes.

Bit	Description
127:0	Header of the packet in error (TLP or DLLP).

25.2 IDE Redirection Controller Configuration Registers (Bn:F2)

Table 25-4. IDE PCI Configuration Register Address Map Bn:F2) (Sheet 1 of 2)

Offset	Mnemonic	Register Name	Default	Type
Mandatory PCI Configuration Registers				
00–01h	VID	Vendor Identification	8086h	RO
02–03h	DID	Device Identification	1084h	RO
04–05h	PCICMD	PCI Command	0000h	RO, RW
06–07h	PCISTS	PCI Status	0010h	RO, R/WC
08h	RID	Revision Identification	See register desc.	RO
09h	PI	Programming Interface	85h	RO
0Ah	SCC	Sub Class Code	01h	RO
0Bh	BCC	Base Class Code	01h	RO
0Ch	CLS	Cache Line Size	10h	R/W
0Dh	PMLT	Primary Master Latency Timer	00h	R/W
0Eh	HEADTYP	Header Type	00h	RO
BAR registers for 32-bit addressing modes				
10–13h	IDE_P_COMMAND_BLK_IO_BASE	IDE Primary Command Block I/O–Mapped Base Address	00000001h	R/W, RO
14–17h	IDE_P_CONTROL_BLK_IO_BASE	IDE Primary Control Block I/O–Mapped Base Address	00000001h	R/W, RO
18–1Bh	IDE_S_COMMAND_BLK_IO_BASE	IDE Secondary Command Block I/O–Mapped Base Address	00000001h	R/W, RO
1C–1Fh	IDE_S_CONTROL_BLK_IO_BASE	IDE Secondary Control Block I/O–Mapped Base Address	00000001h	R/W, RO
20–23h	IDE_BUS_MASTER_IO_BASE	IDE BUS MASTER I/O–Mapped Base Address	00000001h	R/W, RO

Table 25-4. IDE PCI Configuration Register Address Map Bn:F2) (Sheet 2 of 2)

Offset	Mnemonic	Register Name	Default	Type
2C–2Dh	SVID	Subsystem Vendor Identification	8086h	RO
2E–2Fh	SID	Subsystem Identification	0000h	RO
30-33h	CSR_EXP_ROM_BASE	CSR Expansion ROM Base Address	00000000h	R/W
34h	CAP_PTR	Capabilities Pointer	C8h	RO
3Ch	INT_LN	Interrupt Line	00h	R/W
3Dh	INT_PN	Interrupt Pin	04h	RO
3Eh	MIN_GNT	Minimum Grant	00h	RO
3Fh	MAX_LAT	Maximum Latency	00h	RO
PCI Power Management Registers				
C8h	CAP_ID	Capability ID	01h	RO
C9h	NXT_PTR	Next Item Pointer	D0h	RO
CA–CBh	PM_CAP	Power Management Capabilities	See bit description	RO
CC–CDh	PMCSR	Power Management Control/Status	0000h	R/W, RO, R/WC
CF	PCIDATA	PCI Power Management Data	00h	RO
Message Signaled Interrupt Configuration Registers				
D0h	MSI_CAP_ID	MSI Capability ID	05h	RO
D1h	MSI_NXT_PTR	MSI t Next Item Pointer	E0h	RO
D2-D3	MSI_MCR	MSI Control Register	0080	R/W
D4-D7h	MSI_MAR_LOW	MSI Message Low Address	00000000h	R/W
D8-DB	MSI_MAR_HIGH	MSI Message High Address	00000000h	R/W
DC-DD	MSI_MDR	Message Data Register	0000	R/W
PCI Express* Configuration Registers				
E0h	PCI Express_CAP_ID	PCI Express Capability Identification Register	10h	RO
E1h	PCI Express_NXT_PTR	PCI Express Next Item Pointer	00h	RO
E2-E3	PCI Express_CAP	PCI Express Capability	0011	RO
E4-E7h	PCI Express_DEV_CAP	PCI Express Device Capability	00000CC1h	RO
E8-E9	PCI Express_DEV_CONT	PCI Express Device Control	2810h	R/W
EA-EB	PCI Express_DEV_STATUS	PCI Express Device Status	0000h	RO
EC-EF	PCI Express_LINK_CAP	PCI Express Link Capability	See register desc.	RO
F0-F1	PCI Express_LINK_CONT	PCI Express Link Control	0000h	R/W
F2-F3	PCI Express_LINK_STATUS	PCI Express Link Status	1011h	RO

25.2.1 VID – Vendor Identification Register (Bn:F0/F1)

Offset Address: 00–01h
Default Value: 8086h
Attribute: RO
Size: 16 bits

Bit	Description
15:0	**Vendor ID** – RO. This is a 16-bit value assigned to Intel.

25.2.2 DID – Device Identification Register (Bn:F2)

Offset Address: 02–03h
Default Value: 1084h
Attribute: RO
Size: 16 bits

Bit	Description
15:0	Device ID - RO. This is a 16-bit value assigned to the Intel® 6321ESB I/O Controller Hub integrated IDE Redirection Controller. If Word 0Ah bit 0 is set in the EEPROM, the Device ID is loaded from the EEPROM, Word 102h/42h after the hardware reset. If not set, the default value is 1084h.

25.2.3 PCICMD – PCI Command Register (Bn:F2)

Offset Address: 04–05h
Default Value: 0000h
Attribute: RO, R/W
Size: 16 bits

Bit	Description
15:11	Reserved
10	**Interrupt Disable** – R/W. 0 = Enable. 1 = Disables IDE Redirection Controller to assert its INTD signal. The Interrupt Disable register bit is a read-write bit that controls the ability of a PCI Express device to generate a legacy interrupt message. When set, devices are prevented from generating legacy interrupt messages.
9	**Fast Back to Back Enable (FBE)** – RO. Hardwired to 0. The integrated IDE Redirection Controller will not run fast back-to-back PCI cycles.
8	**SERR# Enable (SERR_EN) –** R/W. 0 = Disable. 1 = Enable. Allow SERR# to be asserted.
7	**Wait Cycle Enable (WCC) –** RO. Hardwired to 0. Not implemented.
6	**Parity Error Response (PER) –** R/W. 0 = The IDE Redirection Controller will ignore PCI parity errors. 1 = The IDE Redirection Controller controller will take normal action when a PCI parity error is detected and will enable generation of parity on ESI.
5	**Palette Snoop Enable (PSE) –** RO. Hardwired to 0. Not Implemented.
4	**Memory Write and Invalidate Enable (MWIE) –** RO. Hardwired to 0. Not Implemented.
3	**Special Cycle Monitoring (SCM) –** RO. Hardwired to 0. The IDE Redirection Controller ignores special cycles.
2	**Bus Master Enable (BME)** – R/W. 0 = Disable. 1 = Enable. The Intel® 6321ESB I/O Controller Hub's integrated IDE Redirection Controller may function as a PCI bus master.
1	**Memory Space Enable (MSE) –** R/W. 0 = Disable. 1 = Enable. The Intel® 6321ESB I/O Controller Hub's integrated IDE Redirection Controller will respond to the memory space accesses.
0	**I/O Space Enable (IOSE) –** R/W. 0 = Disable. 1 = Enable. The Intel® 6321ESB I/O Controller Hub's integrated IDE Redirection Controller will respond to the I/O space accesses.

25.2.4 PCISTS – PCI Status Register (Bn:F2)

Offset Address: 06–07h
Default Value: 0010h
Attribute: RO, R/WC
Size: 16 bits

Note: For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 to the bit has no effect.

Bit	Description
15	**Detected Parity Error (DPE)** – R/WC. 0 = Parity error Not detected. 1 = The Intel® 6321ESB I/O Controller Hub's integrated IDE Redirection Controller has detected a parity error on the PCI bus (will be set even if Parity Error Response is disabled in the PCI Command register).
14	**Signaled System Error (SSE) –** R/WC. 0 = Integrated IDE Redirection Controller has **not** asserted SERR# 1 = The Intel® 6321ESB I/O Controller Hub's integrated IDE Redirection Controller has asserted SERR#. SERR# can be routed to cause NMI, SMI#, or interrupt.
13	**Master Abort Status** (**RMA) –** R/WC. 0 = Master Abort not generated 1 = The Intel® 6321ESB I/O Controller Hub's integrated IDE Redirection Controller (as a PCI master) has generated a master abort.
12	**Received Target Abort (RTA) –** R/WC. 0 = Target abort Not received. 1 = The Intel® 6321ESB I/O Controller Hub's integrated IDE Redirection Controller (as a PCI master) has received a target abort.
11	**Signaled Target Abort (STA) –** R/WC. 0 = Target abort Not signaled. 1 = The Intel® 6321ESB I/O Controller Hub's integrated IDE Redirection Controller (as a PCI master) has signaled a target abort.
10:9	**DEVSEL Timing –** RO. Hardwired to 0. Not implemented.
8	**Data Parity Error Detected (DPED) –** R/WC. 0 = Parity error Not detected (conditions below are not met). 1 = All of the following three conditions have been met: 1. The IDE Redirection Controller is acting as bus master 2. The IDE Redirection Controller has asserted PERR# (for reads) or detected PERR# asserted (for writes) 3. The Parity Error Response bit in the IDE Redirection Controller's PCI Command Register is set.
7	**Fast Back to Back Capable (FB2BC**) – RO. Hardwired to 0. Not implemented.
6	**Reserved.**
5	**66 MHz Capable (66MHZ_CAP) –** RO. Hardwired to 0. Not implemented.
4	**Capabilities List (CAP_LIST) –** RO. Indicates that a device implements Extended Capabilities. 0 = The EEPROM indicates that the integrated IDE Redirection Controller does not support extended capabilities. 1 = The EEPROM indicates that the integrated IDE Redirection Controller supports PCI Power Management, message signaled interrupts, and the PCI express extensions.
3	**Interrupt Status (INTS) –** RO. This bit indicates that an interrupt is pending. It is independent from the state of the Interrupt Enable bit in the command register.
2:0	Reserved

25.2.5 RID – Revision Identification Register (Bn:F2)

Offset Address: 08h
Default Value: See bit description
Attribute: RO
Size: 8 bits

Bit	Description
7:0	Revision ID (RID) – RO. The default revision ID of this device is 00h. The value of the rev ID is a logic OR between the default value and the value in the EEPROM word 1Eh. Refer to Table 2-33 or the *Intel® 631xESB/632xESB I/O Controller Hub EDS Specification Update* for the value of the Revision ID Register.

25.2.6 PI – Programming Interface Register (Bn:F2)

Offset Address: 09h
Default Value: 85h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Programming Interface(PI)** – RO. This 8-bit value specifies the class code as the programming i/f class.

25.2.7 SCC – Sub Class Code Register (Bn:F2)

Offset Address: 0Ah
Default Value: 01h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Sub Class Code (SCC)** – RO. This 8-bit value specifies the sub class of the device as an IDE redirection controller.

25.2.8 BCC – Base Class Code Register (Bn:F2)

Offset Address: 0Bh
Default Value: 01h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Base Class Code (BCC)** – RO. This 8-bit value specifies the base class of the device as a mass storage controller.

25.2.9 CLS – Cache Line Size Register (Bn:F2)

Offset Address: 0Ch
Default Value: See register desc.
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	Cache Line Size(CLS) – R/W. Implement for legacy compatibility purposes but has no impact on any PCI Express device functionality. Loaded from EEPROM 1Ah.

25.2.10 PMLT – Primary Master Latency Timer Register (Bn:F2)

Offset Address: 0Dh
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	Not used. Hardwired to zero

25.2.11 HEADTYP – Header Type Register (Bn:F2)

Offset Address: 0Eh
Default Value: 00h, 80h
Attribute: RO
Size: 8 bits

Bit	Description
7	**Multi-Function Device (MFD) –** RO. Hardwired to 0 to indicate a single function device, that is, If only a single IDE Redirection Function is active. 1 for multiple function
6:0	**Header Type (HTYPE) –** RO. This 7-bit field identifies the header layout of the configuration space as an IDE redirection controller.

25.2.12 Base Address Registers (Bn:F2)

IDE Function has no 64-bit addressing since IDE has only IO mapping window. BAR32 bit in the EEPROM set to 1 (Word 0Ah)

32-bit Addressing Mode

25.2.12.1 IDE_P_COMMAND_BLK_IO_BASE – IDE Primary Command Block I/O-Mapped Base Address Register (Bn:F2)

Offset Address: 10–13h
Default Value: 00000001h
Attribute: R/W, RO
Size: 32 bits

Note: The Intel® 6321ESB I/O Controller Hub's integrated IDE redirection controller requires one BAR for memory mapping. Software determines which BAR (memory or I/O) is used to access the LAN controller's CSR registers.

Bit	Description
31:3	**Base Address (IO_ADDR)** – R/W. This field provides 8 bytes of I/O-Mapped address space for the IDE I/O space
2:1	Reserved
0	**I/O Space Indicator (IO_SPACE) –** RO. Hardwired to 1 to indicate that this base address maps to I/O space.

25.2.12.2 IDE_P_CONTROL_BLK_IO_BASE – IDE Primary Control Block I/O-Mapped Base Address Register (Bn:F2)

Offset Address: 14–17h
Default Value: 00000001h
Attribute: R/W, RO
Size: 32 bits

Note: The Intel® 6321ESB I/O Controller Hub's integrated IDE Redirection Controller requires one BAR for memory mapping. Software determines which BAR (memory or I/O) is used to access the LAN controller's CSR registers.

Bit	Description
31:2	**Base Address (IO_ADDR)** – R/W. This field provides 4 bytes of I/O-Mapped address space for the IDE I/O space
1	Reserved
0	**I/O Space Indicator (IO_SPACE) –** RO. Hardwired to 1 to indicate that this base address maps to I/O space.

25.2.12.3 IDE_S_COMMAND_BLK_IO_BASE – IDE Secondary Command Block I/O-Mapped Base Address Register (Bn:F2)

Offset Address:	18–1Bh	Attribute:	R/W, RO
Default Value:	00000001h	Size:	32 bits

Note: The Intel® 6321ESB I/O Controller Hub's integrated IDE Redirection Controller requires one BAR for memory mapping. Software determines which BAR (memory or I/O) is used to access the LAN controller's CSR registers.

Bit	Description
31:3	**Base Address (IO_ADDR)** – R/W. This field provides 8 bytes of I/O-Mapped address space for the IDE I/O space
2:1	Reserved
0	**I/O Space Indicator (IO_SPACE) –** RO. Hardwired to 1 to indicate that this base address maps to I/O space.

25.2.12.4 IDE_S_CONTROL_BLK_IO_BASE – IDE Secondary Control Block I/O-Mapped Base Address Register (Bn:F2)

Offset Address:	1C–1Fh	Attribute:	R/W, RO
Default Value:	00000001h	Size:	32 bits

Note: The Intel® 6321ESB I/O Controller Hub's integrated IDE Redirection Controller requires one BAR for memory mapping. Software determines which BAR (memory or I/O) is used to access the LAN controller's CSR registers.

Bit	Description
31:2	**Base Address (IO_ADDR)** – R/W. This field provides 4 bytes of I/O-Mapped address space for the IDE I/O space
1	Reserved
0	I/O Space Indicator (IO_SPACE) – RO. Hardwired to 1 to indicate that this base address maps to I/O space.

25.2.12.5 IDE_BUS_MASTER_IO_BASE – IDE Bus Master I/O-Mapped Base Address Register (Bn:F2)

Offset Address:	20-23h	Attribute:	R/W, RO
Default Value:	00000001h	Size:	32 bits

Note: The Intel® 6321ESB I/O Controller Hub's integrated IDE Redirection Controller requires one BAR for memory mapping. Software determines which BAR (memory or I/O) is used to access the LAN controller's CSR registers.

Bit	Description
31:4	**Base Address (IO_ADDR)** – R/W. This field provides 16 bytes of I/O-Mapped address space for the IDE I/O space.
3:1	Reserved
0	**I/O Space Indicator (IO_SPACE)** – RO. Hardwired to 1 to indicate that this base address maps to I/O space.

25.2.13 SVID – Subsystem Vendor Identification(Bn:F2)

Offset Address: 2C–2D
Default Value: 8086h
Attribute: RO
Size: 16 bits

Bit	Description
15:0	**Subsystem Vendor ID (SVID)** – RO. This value may be loaded automatically from the EEPROM address 0Ch upon power up or reset if the EEPROM is present (and properly programmed) and if Word 0Ah bit 1 is set. A value of 0x8086 is default for this field upon power up if the EEPROM does not respond or is not programmed.

25.2.14 SID – Subsystem Identification (Bn:F2)

Offset Address: 2E–2Fh
Default Value: 0000h
Attribute: RO
Size: 16 bits

Bit	Description
15:0	**Subsystem ID (SID) –** RO. This value may be loaded automatically from the EEPROM address 105h/45h upon power up with a default value of 0x0000 if the EEPROM is present (and properly programmed) and if Word 0Ah bit 1 is set.

25.2.15 CSR_EXP_ROM_BASE – CSR Expansion ROM Base Address

Offset Address: 30–33h
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

Bit	Description
31:11	**Base Address (EXP_ROM_ADDR)** – R/W. Hardwired to 0 depending on the memory mapping window size. The LAN Expansion ROM spaces can be either 64K, up to 8MB in power of 2. Mapping window size is set by the EEPROM word 0Fh.
10:1	Reserved
0	**Expansion ROM Access Enable (EXP_ROM_EN)** – R/W. 1 enables expansion ROM access. 0 disables expansion ROM access.

This register is used to define the address and size information for boot-time access to the optional FLASH memory. Only the LAN 0/LAN 1 and IDE functions may have this window. It is enabled by the EEPROM words 24h, 14h and 1Ch for LAN 0, LAN 1 and IDE functions respectively. This register returns zero value for functions without expansion ROM window.

25.2.16 CAP_PTR – Capabilities Pointer (Bn:F2)

Offset Address: 34h
Default Value: C8h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Capabilities Pointer (CAP_PTR)** – RO. Hardwired to C8h to indicate the offset within configuration space for the location of the Power Management registers.

25.2.17 INT_LN – Interrupt Line Register (Bn:F2)

Offset Address: 3Ch
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	**Interrupt Line (INT_LN) –** R/W. This field identifies the system interrupt line to which the LAN controller's PCI interrupt request pin (as defined in the Interrupt Pin Register) is routed.

25.2.18 INT_PN – Interrupt Pin Register (Bn:F2)

Offset Address: 3Dh
Default Value: 04h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Interrupt Pin (INT_PN)** – RO. IDE Redirection Controller - A value of 0x1 / 0x2 / 0x3 / 0x4 indicates that this function implements legacy interrupt on INTA / INTB / INTC / INTD respectively. Loaded from EEPROM word 21h.

25.2.19 MIN_GNT – Minimum Grant Register (Bn:F2)

Offset Address: 3Eh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	Minimum Grant (MIN_GNT) – RO. Not used, hardwired to 00h.

25.2.20 MAX_LAT – Maximum Latency Register (Bn:F2)

Offset Address: 3Fh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	Maximum Latency (MAX_LAT) – RO. Not used, hardwired to 00h.

25.2.21 CAP_ID – Capability Identification Register (Bn:F2)

Offset Address: C8h
Default Value: 01h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Capability ID (CAP_ID)** – RO. Hardwired to 01h to indicate that the Intel® 6321ESB I/O Controller Hub's integrated IDE Redirection Controller supports PCI Power Management.

25.2.22 NXT_PTR – Next Item Pointer (Bn:F2)

Offset Address: C9h
Default Value: D0h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Next Item Pointer (NXT_PTR)** – RO. Hardwired to D0h to indicate that power management is the last item in the capabilities list.

25.2.23 PM_CAP – Power Management Capabilities (Bn:F2)

Offset Address: CA–CBh
Default Value: See bit description
Attribute: RO
Size: 16 bits

Bit	Description
15:11	**PME Support (PME_SUP)** – RO. This 5-bit field indicates the power states in which the IDE Redirection Controller may assert PME#. The default value depends on EEPROM word 0Ah. 00000b = No PME at all states. 01001b = PME at D0 and $D3_{hot}$ 11001b = PME at D0, $D3_{hot}$ and $D3_{cold}$
10:9	**Hardwired to '0'.**
8:6	**Auxiliary Current (AUX_CUR)** – RO. Hardwired to 000b to indicate that the IDE Redirection Controller implements the Data registers. The auxiliary power consumption is the same as the current consumption reported in the D3 state in the Data register.
5	**Device Specific Initialization (DSI)** – RO. Hardwired to 1 to indicate that special initialization of this function is required (beyond the standard PCI configuration header) before the generic class device driver is able to use it. DSI is required for the IDE Redirection Controller after D3-to-D0 reset.
4	Reserved
3	**PME Clock (PME_CLK)** – RO. Hardwired to 0 to indicate that the IDE Redirection Controller does not require a clock to generate a power management event.
2:0	**Version (VER) –** RO. Hardwired to 010b to indicate that the IDE Redirection Controller complies with of the *PCI Power Management Specification, Revision 1.1.*

25.2.24 PMCSR – Power Management Control/Status Register Bn:F2)

Offset Address: CC–CDh
Default Value: 0000h
Attribute: RO, R/W, R/WC
Size: 16 bits

Bit	Description
15	PME Status **(PME_STAT)** – R/WC. 0 = Software clears this bit by writing a 1 to it. This also deasserts the PME# signal and clears the PME status bit in the Power Management Driver Register. When the PME# signal is enabled, the PME# signal reflects the state of the PME status bit. 1 = Set upon occurrence of a wakeup event, independent of the state of the PME enable bit.
14:13	**Data Scale (DSCALE) –** RO. This field indicates the data register scaling factor. It equals 10b for all supported registers: 0,3,4,7 and 8, as selected by the “Data Select” field.
12:9	**Data Select (DSEL) –** R/W. This field is used to select which data is reported through the Data register and Data Scale field.
8	**PME Enable (PME_EN)** – R/W. This bit enables the Intel® 6321ESB I/O Controller Hub’s integrated IDE Redirection Controller to assert PME#. 0 = The device will not assert PME#. 1 = Enable PME# assertion when PME Status is set.
7:2	Reserved
1:0	**Power State (PWR_ST) –** R/W. This 2-bit field is used to determine the current power state of the integrated IDE Redirection Controller, and to put it into a new power state. The definition of the field values is as follows: 00 = D0 01/10 = Reserved 11 = D3

25.2.25 PCIDATA – PCI Power Management Data Register (Bn:F2)

Offset Address: CFh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Power Management Data (PWR_MGT) –** RO. State dependent power consumption and heat dissipation data.

This optional register is used to report power consumption and heat dissipation. Reported register is controlled by the Data_Select field in the PMCSR, and the power scale is reported in the Data_Scale field in the PMCSR. The data of this field is loaded from the EEPROM if PM is enabled in the EEPROM or with a default value of 0x00 otherwise. The values for Intel® 6321ESB I/O Controller Hub IDE Redirection Controller functions is shown in Table 25-5.

Table 25-5. Data Register Structure

Function	D0 (consume/ dissipate)	D3 (consume/ dissipate)	Common	Data_Scale
Data_Select	**(0x0 / 0x4)**	**(0x3 / 0x7)**	**(0x8)**	
IDE Redirection	EEP addr 100/40h	EEP addr 101/41h	0x00	10b

25.2.26 MSI_CAP_ID – Capability Identification Register (Bn:F2)

Offset Address: D0h
Default Value: 05h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Capability ID (CAP_ID)** – RO. Hardwired to 05h to indicate that the linked list item as being the Message Signaled Interrupt registers.

25.2.27 MSI_NXT_PTR – Next Item Pointer (Bn:F2)

Offset Address: D1h
Default Value: E0h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Next Item Pointer (NXT_PTR)** – RO. Hardwired to E0h to indicate that PCI Express capability is the next item in the capability list.

25.2.28 MSI_MCR – Message Control Register (Bn:F2)

Offset Address: D2–D3h
Default Value: 0080
Attribute: RO
Size: 16 bits

Bit	Description
15:11	Reserved.
7	**64 Support (64_SUP)** – RO. Hardwired to 1 to indicate that the IDE Redirection Controller is capable of generating 64 bit message addresses.

Bit	Description
6:4	**Multiple Message Enable(MM_ENABLE)** – RO. Hardwired to 000b to indicate that the IDE Redirection Controller supports single message per function.
3:1	**Multiple Message Capable(MM_CAP)** – RO. Hardwired to 000b to indicate that the IDE Redirection Controller capable of single requested message per function.
0	**MSI ENABLE(MSI_ENABLE) –** R/W. If 1, the IDE Redirection Controller will generate MSI for interrupt assertion instead of INTx signaling.

25.2.29 MSI_MAR_LOW – Message Address Low Register (Bn:F2)

Offset Address: D4–D7h
Default Value: 00000000h
Attribute: RO, R/W, R/WC
Size: 32 bits

Bit	Description
7:2	**Message Address Low(MSG_ADDR_LOW) –** R/W. Written by the system to indicate the lower 32 bits of the address to use for the MSI memory write transaction. The lower two bits will always return 0 regardless of the write operation.

25.2.30 MSI_MAR_HIGH – Message Address High Register (Bn:F2)

Offset Address: D8–DBh
Default Value: 0000h
Attribute: RO, R/W, R/WC
Size: 16 bits

Bit	Description
31:0	**Message Address High(MSG_ADDR_HIGH) –** R/W. This field contains the upper 32 bits of the address to use for the MSI memory write transaction.

25.2.31 MSI_MDR – Message Data Register (Bn:F2)

Offset Address: DC–DDh
Default Value: 0000h
Attribute: R/W
Size: 16 bits

Bit	Description
15:0	**Message Data(MSG_DATA) –** R/W. Written by the system to indicate the lower 16 bits of the data written in the MSI memory write DWORD transaction. The upper 16 bits of the transaction are written as 0

25.2.32 PCI Express_CAP_ID – PCI Express* Capability Identification Register (Bn:F2)

Offset Address: E0h
Default Value: 10h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Capability ID (CAP_ID)** – RO. Hardwired to 10h to indicate that the linked list item as being the PCI Express Capability Registers.

25.2.33 PCI Express_NXT_PTR – PCI Express* Next Item Pointer (Bn:F2)

Offset Address: E1h
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Next Item Pointer (NXT_PTR)** – RO. Hardwired to 00h to indicate that it is the last item in the capability linked list.

25.2.34 PCI Express_CAP – PCI Express* Capability Register (Bn:F2)

Offset Address: E2–E3h
Default Value: 0011
Attribute: RO
Size: 16 bits

Bit	Description
15:14	Reserved.
13:9	**Interrupt Message Number (INT_MSG_NUM)** – RO. Multiple MSI per function is not supported. Hardwired to 00000b
8	**Slot Implemented** – RO. Slot option not implemented hardwired to 0.
7:4	**Device/Port Type** – RO. Indicates the type of PCI Express functions. The value of for IDE Redirection Function is loaded from the EEPROM word 19h bit 13.
3:0	**Capability version(CAP_VERSION) –** RO. Indicates the PCI Express capability structure version number 0001b.

25.2.35 PCI Express_DEV_CAP – PCI Express* Device Capability Register (Bn:F2)

Offset Address: E4–E7h
Default Value: 00000CC1h
Attribute: RO, R/W, R/WC
Size: 32 bits

Bit	Description
31:28	Reserved.
27:26	**Slot Power Limit Scale** – RO. Used in upstream port only. Hardwired to 00b.
25:18	**Slot Power Limit Value** – RO. Used in upstream port only. Hardwired to 00b
17:15	Reserved.
14	**Power Indicator Present** – RO. Hardwired to 0b
13	**Attention Indicator Present** – RO. Hardwired to 0b
12	**Attention Button Present** – RO. Hardwired to 0b
11:9	**Endpoint L1 Acceptable Latency** – RO. This field indicates the acceptable latency that Intel® 6321ESB I/O Controller Hub LAN core can withstand due to the transition from L1 state to the L0 state. All functions share the same value loaded from the EEPROM PCI Express* init configuration 1 Word 18h
8:6	**Endpoint L0s Acceptable Latency** – RO. This field indicates the acceptable latency that Intel® 6321ESB I/O Controller Hub LAN core can withstand due to the transition from L0s state to the L0 state. All functions share the same value loaded from the EEPROM PCI Express init configuration 1 Word 18h.

Bit	Description
5	**Extended Tag Field Supported –** RO. Max supported size of the Tag field. Intel® 6321ESB I/O Controller Hub supported 5-bit Tag field for all functions.
4:3	**Phantom Function Supported** – RO. Hardwired to 00b. Not supported.
2:0	**Max Payload Size Supported** – RO. This field indicates the maximum payload that the device can support for TLPs. It is loaded from the EEPROM PCI Express init configuration 3 Word 1Ah bit 8 with a default value of 256B.

25.2.36 PCI Express_DEV_CONT – PCI Express* Device Control Register (Bn:F2)

Offset Address: E8–E9h
Default Value: 2810h
Attribute: RO, R/W
Size: 16 bits

Bit	Description
15	Reserved.
14:12	**Max Read Request Size** - this field sets maximum read request size for the Device as a requester. The default value is 010b (512B) for the LAN devices.
11	**Enable No Snoop** – R/W. Snoop is gated by NONSNOOP bits in the GCR register in the CSR space. Default is 1b
10	**Auxiliary Power PM Enable** - when set enables the device to draw AUX power independent of PME AUX power. Intel® 6321ESB I/O Controller Hub LAN core is a multi function device, therefore allowed to draw AUX power if at least one of the functions has this bit sets
9	**Phantom Function Enable** – RW. Hardwired to 0b
8	**Extended Tag Field Enable** – RW. Hardwired to 0b
7:5	**Max Payload Size** – RW. This field sets maximum TLP payload size for the device functions. As a receiver the device must handle TLPs as large as the set value. As transmitter, the device must not generate TLPs exceeding the set value.The Max Payload Size Supported in the device capabilities register indicates permissible values that can be programmed. Default value is 000b(128 Bytes)
4	**Enable Relaxed Ordering** – If this bit is set, the device is permitted to set the Relaxed Ordering bit in the attribute field of write transactions that do not need strong ordering. Default to 1b
3	**Unsupported Request Reporting Enable** – RW. Enable error report.
2	**Fatal Error Reporting Enable** – RW. Enable error report.
1	**Non-Fatal Error Reporting Enable** – RW. Enable error report.
0	**Correctable Error Reporting Enable** – RW. Enable error report.

25.2.37 PCI Express_DEV_STATUS – PCI Express* Device Status Register (Bn:F2)

Offset Address: EA–EBh
Default Value: 0000h
Attribute: RO, R/W, R/WC
Size: 16 bits

Bit	Description
15:6	Reserved.
5	**Transaction Pending** – RO. Indicates whether Intel® 6321ESB I/O Controller Hub LAN has any transaction pending. (Transactions include completions for any outstanding non-posted request for all used traffic classes).
4	**Aux Power Detected**– RO. If this bit is set, the device is permitted to set the Relaxed Ordering bit in the attribute field of write transactions that do not need strong ordering. Default to 1b
3	**Unsupported Request Detected** – R/WC. Indicates that Intel® 6321ESB I/O Controller Hub LAN received an unsupported request. Intel® 6321ESB I/O Controller Hub LAN can't distinguish which function causes the error.

Bit	Description
2	**Fatal Error Detected** – R/WC. Enable error report.
1	**Non-Fatal Error Detected** – R/WC. Enable error report.
0	**Correctable Error Detected** – R/WC. Enable error report.

25.2.38 PCI Express_LINK_CAP – PCI Express* Link Capability Register (Bn:F2)

Offset Address: EC–EFh Attribute: RO, R/W
Default Value: See description Size: 16 bits

Bit	Description
31:24	**Port Number** – RO. The PCI Express* port number for the given PCI Express Link. Field is set in the Link training phase. Default to 0x0.
23:18	Reserved.
17:15	**L1 Exit Latency**- Indicates the exit latency from L1 to L0 state. This field is loaded from the EEPROM PCI Express init configuration 1 Word 18h. Default to 110b (32-64us).
14:12	**L0s Exit Latency**- Indicates the exit latency from L0s to L0 state. This field is loaded from the EEPROM PCI Express init configuration 1 Word 18h (two values for Common PCI Express clock or Separate PCI Express clock). Default to 001b (64-128ns).
11:10	**Active State Link PM Support** – RO. Indicates the level of active state power management supported in Intel® 6321ESB I/O Controller Hub LAN core. Defined encodings are: 00bReserved 01bL0s Entry Supported 10bReserved 11bL0s and L1 Supported This field is loaded from the EEPROM PCI Express init configuration 3 Word 1Ah.Default to 11b
9:4	**Max Link Width** – RO. Indicates the max link width. Intel® 6321ESB I/O Controller Hub LAN controller can support by 1 and by 4-link width. The field is loaded from the EEPROM PCI Express init configuration 3 Word 1Ah with a default value of 4 lanes. Default to 00100b.
3:0	**Max Link Speed** – RO. Indicates a max link speed of 2.5 Gbps. Default to 0001b

25.2.39 PCI Express_LINK_CONT – PCI Express* Link Control Register (Bn:F2)

Offset Address: F0–F1h Attribute: R/W
Default Value: 0000h Size: 16 bits

Bit	Description
15:8	Reserved.
7	**Extended Synch** – RW. This bit forces extended Tx of FTS ordered set in FTS and extra TS2 at exit from L1 prior to enter L0.
6	**Common Clock Configuration** – RW. When set indicates that Intel® 6321ESB I/O Controller Hub and the component at the other end of the link are operating with a common reference clock. A value of 0 indicates that they operating with an asynchronous clock. This parameter affects the L0s Exit Latencies.
5	**Retrain Clock** – RO. Not applicable for endpoint devices, hardwired to 0.
4	**Link Disable** – RO. Not applicable for endpoint devices, hardwired to 0.

Bit	Description
3	**Read Completion Boundary** – RW.
2	Reserved.
1:0	**Active State Link PM Control –** R/W. this field controls the active state PM supported on the link. Link PM functionality is determined by the lowest common denominator of all functions. Defined encodings are: 00b PM Disabled 01b L0s Entry Supported 10b Reserved 11b L0s and L1 Supported

25.2.40 PCI Express_LINK_STATUS – PCI Express* Link Status Register (Bn:F2)

Offset Address: F2–F3h
Default Value: 1011h
Attribute: R/W
Size: 16 bits

Bit	Description
15:13	Reserved.
12	**Slot Clock Configuration** – When set, it indicates it uses the physical reference clock that the platform provides on the connector. This bit must be cleared uses an independent clock. Default to be 1b.
11	**Link Training** – RO. Indicates that link training is in progress.
10	**Link Training Error** – RO. Indicates that link training error has occurred.
9:4	**Negotiated Link Width** – RO. Indicates the negotiated width of the link. 000001b = x1 000100b = x4
3:0	**Link Speed** – RO. Indicates a max link speed of 2.5 Gbps. Default to 0001b

25.3 Serial Port Redirection Controller Configuration Registers (Bn:F3)

Table 25-6. SERIAL PCI Configuration Register Address Map Bn:F3) (Sheet 1 of 3)

Offset	Mnemonic	Register Name	Default	Type
Mandatory PCI Configuration Registers				
00–01h	VID	Vendor Identification	8086h	RO
02–03h	DID	Device Identification	1085h	RO
04–05h	PCICMD	PCI Command	0000h	RO, RW
06–07h	PCISTS	PCI Status	0010h	RO, R/WC
08h	RID	Revision Identification	See register desc.	RO
09h	PI	Program Interface	02h	RO
0Ah	SCC	Sub Class Code	00h	RO
0Bh	BCC	Base Class Code	07	RO
0Ch	CLS	Cache Line Size	10h	R/W
0Dh	PMLT	Primary Master Latency Timer	00h	R/W
0Eh	HEADTYP	Header Type	00h	RO

Table 25-6. SERIAL PCI Configuration Register Address Map Bn:F3) (Sheet 2 of 3)

Offset	Mnemonic	Register Name	Default	Type
BAR Registers for 64-Bit Addressing Modes				
10–13h	SER_IO_BASE	Serial I/O–Mapped Base Address	00000001h	R/W, RO
14–17h	SER_MEM_BASE_LOW	Serial Memory–Mapped Base Low Address	00000004h	R/W, RO
18–1Bh	SER_MEM_BASE_HIGH	Serial Memory–Mapped Base High Address	00000000h	R/W, RO
BAR Registers for 32-Bit Addressing Modes				
10–13h	SER_IO_BASE	Serial I/O–Mapped Base Address	00000001h	R/W, RO
14–17h	SER_MEM_BASE	Serial Memory–Mapped Base Address	00000000h	R/W, RO
2C–2Dh	SVID	Subsystem Vendor Identification	8086h	RO
2E–2Fh	SID	Subsystem Identification	0000h	RO
34h	CAP_PTR	Capabilities Pointer	C8h	RO
3Ch	INT_LN	Interrupt Line	00h	R/W
3Dh	INT_PN	Interrupt Pin	03h	RO
3Eh	MIN_GNT	Minimum Grant	00h	RO
3Fh	MAX_LAT	Maximum Latency	00h	RO
PCI Power Management Registers				
C8h	CAP_ID	Capability ID	01h	RO
C9h	NXT_PTR	Next Item Pointer	D0h	RO
CA–CBh	PM_CAP	Power Management Capabilities	See bit description	RO
CC–CDh	PMCSR	Power Management Control/ Status	0000h	R/W, RO, R/ WC
CF	PCIDATA	PCI Power Management Data	00h	RO
Message Signaled Interrupt Configuration Registers				
D0h	MSI_CAP_ID	MSI Capability ID	05h	RO
D1h	MSI_NXT_PTR	MSI t Next Item Pointer	E0h	RO
D2-D3	MSI_MCR	MSI Control Register	0080	R/W
D4-D7h	MSI_MAR_LOW	MSI Message Low Address	00000000h	R/W
D8-DB	MSI_MAR_HIGH	MSI Message High Address	00000000h	R/W
DC-DD	MSI_MDR	Message Data Register	0000	R/W
PCI Express* Configuration Registers				
E0h	PCI Express_CAP_ID	PCI Express Capability Identification Register	10h	RO
E1h	PCI Express_NXT_PTR	PCI Express Next Item Pointer	00h	RO
E2-E3	PCI Express_CAP	PCI Express Capability	0011	RO
E4-E7h	PCI Express_DEV_CAP	PCI Express Device Capability	00000CC1h	RO
E8-E9	PCI Express_DEV_CONT	PCI Express Device Control	2810h	R/W
EA-EB	PCI Express_DEV_STATUS	PCI Express Device Status	0000h	RO

Table 25-6. SERIAL PCI Configuration Register Address Map Bn:F3) (Sheet 3 of 3)

Offset	Mnemonic	Register Name	Default	Type
EC-EF	PCI Express_LINK_CAP	PCI Express Link Capability	See description	RO
F0-F1	PCI Express_LINK_CONT	PCI Express Link Control	0000h	R/W
F2-F3	PCI Express_LINK_STATUS	PCI Express Link Status	1011h	RO

25.3.1 DID – Device Identification Register (Bn:F3)

Offset Address: 02–03h
Default Value: 1085h
Attribute: RO
Size: 16 bits

Bit	Description
15:0	**Device ID** - RO. This is a 16-bit value assigned to the Intel® 6321ESB I/O Controller Hub integrated Serial Port Redirection Controller. If Word 0Ah bit 0 is set in the EEPROM, the Device ID is loaded from the EEPROM, Word 103h/43h after the hardware reset. If not set, the default value is 1085h.

25.3.2 PCICMD – PCI Command Register (Bn:F3)

Offset Address: 04–05h
Default Value: 0000h
Attribute: RO, R/W
Size: 16 bits

Bit	Description
15:11	Reserved
10	**Interrupt Disable** – R/W. 0 = Enable. 1 = Disables Serial Port Redirection Controller to assert its INTC signal. The Interrupt Disable register bit is a read-write bit that controls the ability of a PCI Express device to generate a legacy interrupt message. When set, devices are prevented from generating legacy interrupt messages.
9	Fast Back to Back Enable (FBE) – RO. Hardwired to 0. The integrated Serial Port Redirection Controller will not run fast back-to-back PCI cycles.
8	**SERR# Enable (SERR_EN) –** R/W. 0 = Disable. 1 = Enable. Allow SERR# to be asserted.
7	Wait Cycle Control (WCC) – RO. Hardwired to 0. Not implemented.
6	**Parity Error Response (PER) –** R/W. 0 = The Serial Port Redirection Controller will ignore PCI parity errors. 1 = The integrated Serial Port Redirection Controller will take normal action when a PCI parity error is detected and will enable generation of parity on ESI.
5	**Palette Snoop Enable (PSE) –** RO. Hardwired to 0. Not Implemented.
4	Memory Write and Invalidate Enable (MWIE) – RO. Hardwired to 0. Not Implemented.
3	Special Cycle Enable (SCE) – RO. Hardwired to 0. The Serial Port Redirection Controller ignores special cycles.

Bit	Description
2	**Bus Master Enable (BME)** – R/W. 0 = Disable. 1 = Enable. The Intel® 6321ESB I/O Controller Hub's integrated Serial Port Redirection Controller may function as a PCI bus master.
1	**Memory Space Enable (MSE) –** R/W. 0 = Disable. 1 = Enable. The Intel® 6321ESB I/O Controller Hub's integrated Serial Port Redirection Controller will respond to the memory space accesses.
0	**I/O Space Enable (IOSE) –** R/W. 0 = Disable. 1 = Enable. The Intel® 6321ESB I/O Controller Hub's integrated Serial Port Redirection Controller will respond to the I/O space accesses.

25.3.3 PCISTS – PCI Status Register (Bn:F3)

Offset Address: 06–07h
Default Value: 0010h
Attribute: RO, R/WC
Size: 16 bits

Note: For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 to the bit has no effect.

Bit	Description
15	Detected Parity Error **(**DPE) – R/WC. 0 = Parity error Not detected. 1 = The Intel® 6321ESB I/O Controller Hub's integrated Serial Port Redirection Controller has detected a parity error on the PCI bus (will be set even if Parity Error Response is disabled in the PCI Command register).
14	Signaled System Error **(**SSE) – R/WC. 0 = Integrated Serial Port Redirection Controller has **not** asserted SERR# 1 = The Intel® 6321ESB I/O Controller Hub's integrated Serial Port Redirection Controller has asserted SERR#. SERR# can be routed to cause NMI, SMI#, or interrupt.
13	**Master Abort Status (RMA) –** R/WC. 0 = Master Abort not generated 1 = The Intel® 6321ESB I/O Controller Hub's integrated Serial Port Redirection Controller (as a PCI master) has generated a master abort.
12	**Received Target Abort (RTA) –** R/WC. 0 = Target abort Not received. 1 = The Intel® 6321ESB I/O Controller Hub's integrated Serial Port Redirection Controller (as a PCI master) has received a target abort.
11	**Signaled Target Abort (STA) –** R/WC. 0 = Target abort Not signaled. 1 = The Intel® 6321ESB I/O Controller Hub's integrated Serial Port Redirection Controller (as a PCI master) has signaled a target abort.
10:9	DEVSEL Timing – RO. Hardwired to 0.
8	**Data Parity Error Detected (DPED) –** R/WC. 0 = Parity error Not detected (conditions below are not met). 1 = All of the following three conditions have been met: 1. The Serial Port Redirection Controller is acting as bus master 2. The Serial Port Redirection Controller has asserted PERR# (for reads) or detected PERR# asserted (for writes) 3. The Parity Error Response bit in the Serial Port Redirection Controller's PCI Command Register is set.
7	Fast Back to Back Capable (FB2BC) – RO. Hardwired to 0. The device does not accept fast back-to-back transactions.
6	Reserved.
5	66 MHz Capable (66MHZ_CAP) – RO. Hardwired to 0. The device does not support 66 MHz PCI.

Bit	Description
4	**Capabilities List (CAP_LIST) –** RO. Indicates that a device implements Extended Capabilities. 0 = The EEPROM indicates that the integrated Serial Port Redirection Controller does not support extended capabilities. 1 = The EEPROM indicates that the integrated Serial Port Redirection Controller supports PCI Power Management, message signaled interrupts, and the PCI express extensions.
3	**Interrupt Status (INTS) –** RO. This bit indicates that an interrupt is pending. It is independent from the state of the Interrupt Enable bit in the command register.
2:0	Reserved

25.3.4 RID – Revision Identification Register (Bn:F3)

Offset Address: 08h Attribute: RO
Default Value: See bit description Size: 8 bits

Bit	Description
7:0	**Revision ID (RID)** – RO. The default revision ID of this device is 00h. The value of the rev ID is a logic OR between the default value and the value in the EEPROM word 1Eh. Refer to Table 2-33 or the *Intel® 631xESB/632xESB I/O Controller Hub EDS Specification Update* for the value of the Revision ID Register.

25.3.5 PI – Programming Interface Register (Bn:F3)

Offset Address: 09h Attribute: RO
Default Value: 02h Size: 8 bits

Bit	Description
7:0	**Programming Interface(PI)** – RO.This 8-bit value specifies the interface code.

25.3.6 SCC – Sub Class Code Register (Bn:F3)

Offset Address: 0Ah Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Description
7:0	**Sub Class Code (SCC)** – RO. This 8-bit value specifies the sub class of the device as an 16550 COM port redirection controller.

25.3.7 BCC – Base Class Code Register (Bn:F3)

Offset Address: 0Bh Attribute: RO
Default Value: 07h Size: 8 bits

Bit	Description
7:0	**Base Class Code (BCC)** – RO. This 8-bit value specifies the base class of the device as a 16550 COM port controller.

25.3.8 CLS – Cache Line Size Register (Bn:F3)

Offset Address: 0Ch
Default Value: See register desc.
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	**Cache Line Size(CLS)** – R/W. Implement for legacy compatibility purposes but has no impact on any PCI Express device functionality. Loaded from EEPROM 1Ah.

25.3.9 PMLT – Primary Master Latency Timer Register (Bn:F3)

Offset Address: 0Dh
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	Not used. Hardwired to zero.

25.3.10 HEADTYP – Header Type Register (Bn:F3)

Offset Address: 0Eh
Default Value: 00h, 80h
Attribute: RO
Size: 8 bits

Bit	Description;
7	**Multi-Function Device (MFD) –** RO. Hardwired to 0 to indicate a single function device, that is, If only a single Serial Port Redirection Function is active. 1 for multiple function
6:0	**Header Type (HTYPE) –** RO. This 7-bit field identifies the header layout of the configuration space as an Serial Port Redirection Controller.

25.3.11 Base Address Registers (Bn:F3)

64-bit Addressing Mode

No EEPROM or the BAR32 EEPROM bit set to 0 (Word 0Ah)

25.3.11.1 SER_IO_BASE – Serial I/O-Mapped Base Address Register (Bn:F3)

Offset Address: 10–13h
Default Value: 00000001h
Attribute: R/W, RO
Size: 32 bits

Note: The Intel® 6321ESB I/O Controller Hub's integrated Serial Port Redirection Controller requires one BAR for memory mapping. Software determines which BAR (memory or I/O) is used to access the Serial Port Redirection Controller's CSR registers.

Bit	Description
31:3	**Base Address (IO_ADDR)** – R/W. This field provides 8 bytes of I/O-Mapped address space for the serial I/O space.
2:1	Reserved
0	**I/O Space Indicator (IO_SPACE) –** RO. Hardwired to 1 to indicate that this base address maps to I/O space.

25.3.11.2 SER_MEM_LOW_BASE – Serial Memory-Mapped Base Address Low Register (Bn:F3)

Offset Address: 14-17h Attribute: R/W, RO
Default Value: 00000004h Size: 32 bits

Note: The Intel® 6321ESB I/O Controller Hub's integrated Serial Port Redirection Controller requires one BAR for memory mapping. Software determines which BAR (memory or I/O) is used to access the Serial Port Redirection Controller's CSR registers.

Bit	Description
31:12	**Base Address (MEM_ADDR) –** R/W. This field contains the upper 20 bits of the base address provides 4 KB for the serial memory spaces.
11:4	Reserved
3	**Prefetchable (MEM_PF)** – RO. Hardwired to 0 to indicate that this is not a pre-fetchable memory-Mapped address range.
2:1	**Type (MEM_TYPE)** – RO. Hardwired to 10b to indicate the memory-Mapped address range may be located anywhere in 64-bit address space.
0	**Memory-Space Indicator (MEM_SPACE)** – RO. Hardwired to 0 to indicate that this base address maps to memory space.

25.3.11.3 SER_MEM_HIGH_BASE – Serial Memory-Mapped Base Address High Register (Bn:F3)

Offset Address: 18–1Bh Attribute: R/W, RO
Default Value: 00000000h Size: 32 bits

Note: The Intel® 6321ESB I/O Controller Hub's integrated Serial Port Redirection Controller requires one BAR for memory mapping. Software determines which BAR (memory or I/O) is used to access the Serial Port Redirection Controller's CSR registers.

Bit	Description
31:0	**Base Address (MEM_ADDR) –** R/W. This field contains the upper 32 bits of the base address provides 4 KB of memory-Mapped space for the serial memory spaces

32-bit Addressing Mode

BAR32 bit in the EEPROM set to 1 (Word 0Ah).

25.3.11.4 SER_IO_BASE – Serial I/O-Mapped Base Address Register (Bn:F3)

Offset Address: 10-13h Attribute: R/W, RO
Default Value: 00000001h Size: 32 bits

Note: The Intel® 6321ESB I/O Controller Hub's integrated Serial Port Redirection Controller requires one BAR for memory mapping. Software determines which BAR (memory or I/O) is used to access the Serial Port Redirection Controller's CSR registers.

Bit	Description
31:3	**Base Address (IO_ADDR)** – R/W. This field provides 8 bytes of I/O-Mapped address space for the serial port I/O space.
2:1	Reserved
0	**I/O Space Indicator (IO_SPACE) –** RO. Hardwired to 1 to indicate that this base address maps to I/O space.

25.3.11.5 SER_MEM_BASE – Serial Memory-Mapped Base Address Register (Bn:F3)

Offset Address: 14-17h Attribute: R/W, RO
Default Value: 00000000h Size: 32 bits

Note: The Intel® 6321ESB I/O Controller Hub's integrated Serial Port Redirection Controller requires one BAR for memory mapping. Software determines which BAR (memory or I/O) is used to access the Serial Port Redirection Controller's CSR registers.

Bit	Description
31:12	**Base Address (MEM_ADDR) –** R/W. This field contains the upper 20 bits of the base address provides 4 KB for the serial memory spaces.
11:4	Reserved
3	**Prefetchable (MEM_PF)** – RO. Hardwired to 0 to indicate that this is not a pre-fetchable memory-Mapped address range.
2:1	**Type (MEM_TYPE)** – RO. Hardwired to 10b to indicate the memory-Mapped address range may be located anywhere in 64-bit address space.
0	**Memory-Space Indicator (MEM_SPACE)** – RO. Hardwired to 0 to indicate that this base address maps to memory space.

25.3.12 SVID – Subsystem Vendor Identification (Bn:F3)

Offset Address: 2C–2D Attribute: RO
Default Value: 8086h Size: 16 bits

Bit	Description
15:0	**Subsystem Vendor ID (SVID)** – RO. This value may be loaded automatically from the EEPROM address 0Ch upon power up or reset if the EEPROM is present (and properly programmed) and if Word 0Ah bit 1 is set. A value of 0x8086 is default for this field upon power up if the EEPROM does not respond or is not programmed.

25.3.13 SID – Subsystem Identification (Bn:F3)

Offset Address: 2E–2Fh Attribute: RO
Default Value: 0000h Size: 16 bits

Bit	Description
15:0	**Subsystem ID (SID) –** RO. This value may be loaded automatically from the EEPROM address 106h/46h upon power up with a default value of 0x0000 if the EEPROM is present (and properly programmed) and if Word 0Ah bit 1 is set.

25.3.14 CAP_PTR – Capabilities Pointer (Bn:F3)

Offset Address: 34h Attribute: RO
Default Value: C8h Size: 8 bits

Bit	Description
7:0	**Capabilities Pointer (CAP_PTR)** – RO. Hardwired to C8h to indicate the offset within configuration space for the location of the Power Management registers.

25.3.15 INT_LN – Interrupt Line Register (Bn:F3)

Offset Address: 3Ch
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	**Interrupt Line (INT_LN) –** R/W. This field identifies the system interrupt line to which the Serial Port Redirection Controller's PCI interrupt request pin (as defined in the Interrupt Pin Register) is routed.

25.3.16 INT_PN – Interrupt Pin Register (Bn:F3)

Offset Address: 3Dh
Default Value: 03h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Interrupt Pin (INT_PN)** – RO. Serial Port Function - A value of 1 / 2 / 3 / 4 indicates that this function implements legacy interrupt on INTA / INTB / INTC / INTD respectively. Loaded from EEPROM word 21h.

25.3.17 MIN_GNT – Minimum Grant Register (Bn:F0/F1)

Offset Address: 3Eh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Minimum Grant (MIN_GNT)** – RO. Not used, hardwired to 00h.

25.3.18 MAX_LAT – Maximum Latency Register (Bn:F0/F1)

Offset Address: 3Fh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Maximum Latency (MAX_LAT)** – RO. Not used, hardwired to 00h.

25.3.19 CAP_ID – Capability Identification Register (Bn:F3)

Offset Address: C8h
Default Value: 01h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Capability ID (CAP_ID)** – RO. Hardwired to 01h to indicate that the Intel® 6321ESB I/O Controller Hub's integrated Serial Port Redirection Controller supports PCI Power Management.

25.3.20 NXT_PTR – Next Item Pointer (Bn:F3)

Offset Address: C9h
Default Value: D0h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Next Item Pointer (NXT_PTR)** – RO. Hardwired to D0h to indicate that MSI is the next capability item in the capabilities list.

25.3.21 PM_CAP – Power Management Capabilities (Bn:F3)

Offset Address: CA–CBh
Default Value: See bit description
Attribute: RO
Size: 16 bits

Bit	Description
15:11	**PME Support (PME_SUP)** – RO. This 5-bit field indicates the power states in which the Serial Port Redirection Controller may assert PME#. The default value depends on EEPROM word 0Ah. 00000b = No PME at all states. 01001b = PME at D0 and $D3_{hot}$ 11001b = PME at D0, $D3_{hot}$ and $D3_{cold}$
10:9	**Hardwired to '0'.**
8:6	**Auxiliary Current (AUX_CUR)** – RO. Hardwired to 000b to indicate that the Serial Port Redirection Controller implements the Data registers. The auxiliary power consumption is the same as the current consumption reported in the D3 state in the Data register.
5	**Device Specific Initialization (DSI)** – RO. Hardwired to 1 to indicate that special initialization of this function is required (beyond the standard PCI configuration header) before the generic class device driver is able to use it. DSI is required for the Serial Port Redirection Controller after D3-to-D0 reset.
4	Reserved
3	**PME Clock (PME_CLK)** – RO. Hardwired to 0 to indicate that the Serial Port Redirection Controller does not require a clock to generate a power management event.
2:0	**Version (VER) –** RO. Hardwired to 010b to indicate that the Serial Port Redirection Controller complies with of the *PCI Power Management Specification, Revision 1.1*.

25.3.22 PMCSR – Power Management Control/Status Register (Bn:F3)

Offset Address: CC–CDh
Default Value: 0000h
Attribute: RO, R/W, R/WC
Size: 16 bits

Bit	Description
15	PME Status **(PME_STAT)** – R/WC. 0 = Software clears this bit by writing a 1 to it. This also deasserts the PME# signal and clears the PME status bit in the Power Management Driver Register. When the PME# signal is enabled, the PME# signal reflects the state of the PME status bit. 1 = Set upon occurrence of a wakeup event, independent of the state of the PME enable bit.
14:13	**Data Scale (DSCALE) –** RO. This field indicates the data register scaling factor. It equals 10b for all supported registers: 0,3,4,7 and 8, as selected by the “Data Select” field.
12:9	**Data Select (DSEL) –** R/W. This field is used to select which data is reported through the Data register and Data Scale field.
8	**PME Enable (PME_EN)** – R/W. This bit enables the Intel® 6321ESB I/O Controller Hub’s integrated Serial Port Redirection Controller to assert PME#. 0 = The device will not assert PME#. 1 = Enable PME# assertion when PME Status is set.
7:2	Reserved
1:0	**Power State (PWR_ST) –** R/W. This 2-bit field is used to determine the current power state of the integrated Serial Port Redirection Controller, and to put it into a new power state. The definition of the field values is as follows: 00 = D0 01/10 = Reserved 11 = D3

25.3.23 PCIDATA – PCI Power Management Data Register (Bn:F3)

Offset Address: CFh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Power Management Data (PWR_MGT) –** RO. State dependent power consumption and heat dissipation data.

This optional register is used to report power consumption and heat dissipation. Reported register is controlled by the Data_Select field in the PMCSR, and the power scale is reported in the Data_Scale field in the PMCSR. The data of this field is loaded from the EEPROM if PM is enabled in the EEPROM or with a default value of 0x00 otherwise. The values for Intel® 6321ESB I/O Controller Hub Serial Port Redirection Controller functions is shown in Table 25-7.

Table 25-7. Data Register Structure

Function	D0 (consume/ dissipate)	D3 (consume/ dissipate)	Common	Data_Scale
Data_Select	**(0x0 / 0x4)**	**(0x3 / 0x7)**	**(0x8)**	
Serial Port Redirection	EEP addr 22h	EEP addr 101/41h	0x00	10b

25.3.24 MSI_CAP_ID – Capability Identification Register (Bn:F3)

Offset Address: D0h
Default Value: 05h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Capability ID (CAP_ID)** – RO. Hardwired to 05h to indicate that the linked list item as being the Message Signaled Interrupt registers.

25.3.25 MSI_NXT_PTR – Next Item Pointer (Bn:F3)

Offset Address: D1h
Default Value: E0h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Next Item Pointer (NXT_PTR)** – RO. Hardwired to E0h to indicate that PCI Express capability is the next item in the capability list.

25.3.26 MSI_MCR – Message Control Register (Bn:F3)

Offset Address: D2–D3h
Default Value: 0080
Attribute: RO
Size: 16 bits

Bit	Description
15:11	Reserved.
7	**64 Support (64_SUP)** – RO. Hardwired to 1 to indicate that the Serial Port Redirection Controller is capable of generating 64 bit message addresses.

Bit	Description
6:4	**Multiple Message Enable(MM_ENABLE)** – RO. Hardwired to 000b to indicate that the Serial Port Redirection Controller supports single message per function.
3:1	**Multiple Message Capable(MM_CAP)** – RO. Hardwired to 000b to indicate that the Serial Port Redirection Controller capable of single requested message per function.
0	**MSI ENABLE(MSI_ENABLE) –** R/W. If 1, the Serial Port Redirection Controller will generate MSI for interrupt assertion instead of INTx signaling.

25.3.27 MSI_MAR_LOW – Message Address Low Register (Bn:F3)

Offset Address: D4–D7h
Default Value: 00000000h
Attribute: RO, R/W, R/WC
Size: 32 bits

Bit	Description
7:2	**Message Address Low(MSG_ADDR_LOW) –** R/W. Written by the system to indicate the lower 32 bits of the address to use for the MSI memory write transaction. The lower two bits will always return 0 regardless of the write operation.

25.3.28 MSI_MAR_HIGH – Message Address High Register (Bn:F3)

Offset Address: D8–DBh
Default Value: 0000h
Attribute: RO, R/W, R/WC
Size: 16 bits

Bit	Description
31:0	**Message Address High(MSG_ADDR_HIGH) –** R/W. This field contains the upper 32 bits of the address to use for the MSI memory write transaction.

25.3.29 MSI_MDR – Message Data Register (Bn:F3)

Offset Address: DC–DDh
Default Value: 0000h
Attribute: R/W
Size: 16 bits

Bit	Description
15:0	**Message Data(MSG_DATA) –** R/W. Written by the system to indicate the lower 16 bits of the data written in the MSI memory write DWORD transaction. The upper 16 bits of the transaction are written as 0

25.3.30 PCI Express_CAP_ID – PCI Express* Capability Identification Register (Bn:F3)

Offset Address: E0h
Default Value: 10h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Capability ID (CAP_ID)** – RO. Hardwired to 10h to indicate that the linked list item as being the PCI Express Capability Registers.

25.3.31 PCI Express_NXT_PTR – PCI Express* Next Item Pointer (Bn:F3)

Offset Address: E1h
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Next Item Pointer (NXT_PTR)** – RO. Hardwired to 00h to indicate that it is the last item in the capability linked list.

25.3.32 PCI Express_CAP – PCI Express* Capability Register (Bn:F3)

Offset Address: E2–E3h
Default Value: 0011
Attribute: RO
Size: 16 bits

Bit	Description
15:14	Reserved.
13:9	**Interrupt Message Number (INT_MSG_NUM)** – RO. Multiple MSI per function is not supported. Hardwired to 00000b
8	**Slot Implemented** – RO. Slot option not implemented hardwired to 0.
7:4	**Device/Port Type** – RO. Indicates the type of PCI Express functions. Hardwired to 0001b
3:0	**Capability version(CAP_VERSION) –** RO. Indicates the PCI Express capability structure version number 0001b.

25.3.33 PCI Express_DEV_CAP – PCI Express* Device Capability Register (Bn:F3)

Offset Address: E4–E7h
Default Value: 00000CC1h
Attribute: RO, R/W, R/WC
Size: 32 bits

Bit	Description
31:28	Reserved.
27:26	**Slot Power Limit Scale** – RO. Used in upstream port only. Hardwired to 00b.
25:18	**Slot Power Limit Value** – RO. Used in upstream port only. Hardwired to 00b
17:15	Reserved.
14	**Power Indicator Present** – RO. Hardwired to 0b
13	**Attention Indicator Present** – RO. Hardwired to 0b
12	**Attention Button Present** – RO. Hardwired to 0b
11:9	**Endpoint L1 Acceptable Latency** – RO. This field indicates the acceptable latency that Intel® 6321ESB I/O Controller Hub LAN core can withstand due to the transition from L1 state to the L0 state. All functions share the same value loaded from the EEPROM PCI Express init configuration 1 Word 18h
8:6	**Endpoint L0s Acceptable Latency** – RO. This field indicates the acceptable latency that Intel® 6321ESB I/O Controller Hub LAN core can withstand due to the transition from L0s state to the L0 state. All functions share the same value loaded from the EEPROM PCI Express init configuration 1 Word 18h.
5	**Extended Tag Field Supported –** RO. Indicates the PCI Express capability structure version number 0001b.
4:3	**Phantom Function Supported** – RO. Indicates the type of PCI Express functions. Hardwired to 0001b
2:0	**Max Payload Size Supported** – RO. Indicates the type of PCI Express functions. Hardwired to 0001b

25.3.34 PCI Express_DEV_CONT – PCI Express* Device Control Register (Bn:F3)

Offset Address: E8–E9h
Default Value: 2810h
Attribute: RO, R/W
Size: 16 bits

Bit	Description
15	Reserved.
14:12	**Max Read Request Size** - this field sets maximum read request size for the Device as a requester. The default value is 010b (512B) for the LAN devices.
11	**Enable No Snoop** – R/W. Snoop is gated by NONSNOOP bits in the GCR register in the CSR space. Default is 1b
10	**Auxiliary Power PM Enable** - when set enables the device to draw AUX power independent of PME AUX power. Intel® 6321ESB I/O Controller Hub LAN core is a multi function device, therefore allowed to draw AUX power if at least one of the functions has this bit sets
9	**Phantom Function Enable** – RW. Hardwired to 0b
8	**Extended Tag Field Enable** – RW. Hardwired to 0b
7:5	**Max Payload Size** – RW. Slot option not implemented hardwired to 0.
4	**Enable Relaxed Ordering** – If this bit is set, the device is permitted to set the Relaxed Ordering bit in the attribute field of write transactions that do not need strong ordering. Default to 1b
3	**Unsupported Request Reporting Enable** – RW. Enable error report.
2	**Fatal Error Reporting Enable** – RW. Enable error report.
1	**Non-Fatal Error Reporting Enable** – RW. Enable error report.
0	**Correctable Error Reporting Enable** – RW. Enable error report.

25.3.35 PCI Express_DEV_STATUS – PCI Express* Device Status Register (Bn:F3)

Offset Address: EA–EBh
Default Value: 0000h
Attribute: RO, R/W, R/WC
Size: 16 bits

Bit	Description
15:6	Reserved.
5	**Transaction Pending** – RO. Slot option not implemented hardwired to 0.
4	**Aux Power Detected**– RO. If this bit is set, the device is permitted to set the Relaxed Ordering bit in the attribute field of write transactions that do not need strong ordering. Default to 1b
3	**Unsupported Request Detected** – R/WC. Enable error report.
2	**Fatal Error Detected** – R/WC. Enable error report.
1	**Non-Fatal Error Detected** – R/WC. Enable error report.
0	**Correctable Error Detected** – R/WC. Enable error report.

25.3.36 PCI Express_LINK_CAP – PCI Express* Link Capability Register (Bn:F3)

Offset Address: EC–EFh
Default Value: See description
Attribute: RO, R/W
Size: 16 bits

Bit	Description
31:24	**Port Number** – RO. The PCI Express* port number for the given PCI Express Link. Field is set in the Link training phase. Default to 0x0.
23:18	Reserved.
17:15	**L1 Exit Latency**- Indicates the exit latency from L1 to L0 state. This field is loaded from the EEPROM PCI Express init configuration 1 Word 18h. Default to 110b (32-64us).
14:12	**L0s Exit Latency**- Indicates the exit latency from L0s to L0 state. This field is loaded from the EEPROM PCI Express init configuration 1 Word 18h (two values for Common PCI Express clock or Separate PCI Express clock). Default to 001b (64-128ns).
11:10	**Active State Link PM Support** – RO. Indicates the level of active state power management supported in Intel® 6321ESB I/O Controller Hub LAN core. Defined encodings are: 00bReserved 01bL0s Entry Supported 10bReserved 11bL0s and L1 Supported This field is loaded from the EEPROM PCI Express init configuration 3 Word 1Ah.Default to 11b
9:4	**Max Link Width** – RO. Indicates the max link width. Intel® 6321ESB I/O Controller Hub LAN controller can support by 1 and by 4-link width. The field is loaded from the EEPROM PCI Express init configuration 3 Word 1Ah with a default value of 4 lanes. Default to 00100b.
3:0	**Max Link Speed** – RO. Indicates a max link speed of 2.5 Gbps. Default to 0001b

25.3.37 PCI Express_LINK_CONT – PCI Express* Link Control Register (Bn:F3)

Offset Address: F0–F1h
Default Value: 0000h
Attribute: R/W
Size: 16 bits

Bit	Description
15:8	Reserved.
7	**Extended Synch** – RW. This bit forces extended Tx of FTS ordered set in FTS and extra TS2 at exit from L1 prior to enter L0.
6	**Common Clock Configuration** – RW. When set indicates that Intel® 6321ESB I/O Controller Hub and the component at the other end of the link are operating with a common reference clock. A value of 0 indicates that they operating with an asynchronous clock. This parameter affects the L0s Exit Latencies.
5	**Retrain Clock** – RO. Not applicable for endpoint devices, hardwired to 0.
4	**Link Disable** – RO. Not applicable for endpoint devices, hardwired to 0.
3	**Read Completion Boundary** – R/W
2	Reserved.
1:0	**Message Data(MSG_DATA) –** R/W. this field controls the active state PM supported on the link. Link PM functionality is determined by the lowest common denominator of all functions. Defined encodings are: 00b PM Disabled 01b L0s Entry Supported 10b Reserved 11b L0s and L1 Supported

25.3.38 PCI Express_LINK_STATUS – PCI Express* Link Status Register (Bn:F3)

Offset Address: F2–F3h
Default Value: 1011h
Attribute: R/W
Size: 16 bits

Bit	Description
15:13	Reserved.
12	**Slot Clock Configuration** – When set, it indicates it uses the physical reference clock that the platform provides on the connector. This bit must be cleared uses an independent clock. Default to be 1b.
11	**Link Training** – RO. Indicates that link training is in progress.
10	**Link Training Error** – RO. Indicates that link training error has occurred.
9:4	**Negotiated Link Width** – RO. Indicates the negotiated width of the link. 000001b = x1 000100b = x4
3:0	**Link Speed** – RO. Indicates a max link speed of 2.5 Gbps. Default to 0001b

25.4 IPMI/KCS0 Controller Configuration Registers (Bn:F4)

Table 25-8. IPMI/KCS0 PCI Configuration Register Address Map Bn:F4) (Sheet 1 of 2)

Offset	Mnemonic	Register Name	Default	Type
Mandatory PCI Configuration Registers				
00–01h	VID	Vendor Identification	8086h	RO
02–03h	DID	Device Identification	1086h	RO
04–05h	PCICMD	PCI Command	0000h	RO, RW
06–07h	PCISTS	PCI Status	0010h	RO, R/WC
08h	RID	Revision Identification	See register description	RO
09h	PI	Program Interface	01h	RO
0Ah	SCC	Sub Class Code	07h	RO
0Bh	BCC	Base Class Code	0C	RO
0Ch	CLS	Cache Line Size	See register description	R/W
0Dh	PMLT	Primary Master Latency Timer	00h	R/W
0Eh	HEADTYP	Header Type	00h	RO
BAR registers for 64-bit addressing modes				
10–13h	IPMI_KCS_MEM_BASE_LOW	IPMI/KCS Mem–Mapped Low Base Address	00000004h	R/W, RO
14–17h	IPMI_KCS_MEM_BASE_HIGH	IPMI/KCS Mem–Mapped Base Address	00000000h	R/W, RO
18–1Bh	IPMI_KCS_IO_BASE	IPMI/KCS I/O–Mapped Base Address	00000001h	R/W, RO
BAR registers for 32-bit addressing modes				
10–13h	IPMI_KCS_MEM_BASE	IPMI/KCS Mem–Mapped Base Address	00000000h	R/W, RO

Table 25-8. IPMI/KCS0 PCI Configuration Register Address Map Bn:F4) (Sheet 2 of 2)

Offset	Mnemonic	Register Name	Default	Type
14–17h	IPMI_KCS_IO_BASE	IPMI/KCS I/O–Mapped Base Address	00000001h	R/W, RO
2C–2Dh	SVID	Subsystem Vendor Identification	8086h	RO
2E–2Fh	SID	Subsystem Identification	0000h	RO
34h	CAP_PTR	Capabilities Pointer	C8h	RO
3Ch	INT_LN	Interrupt Line	00h	R/W
3Dh	INT_PN	Interrupt Pin	04h	RO
3Eh	MIN_GNT	Minimum Grant	00h	RO
3Fh	MAX_LAT	Maximum Latency	00h	RO
PCI Power Management Registers				
C8h	CAP_ID	Capability ID	01h	RO
C9h	NXT_PTR	Next Item Pointer	D0h	RO
CA–CBh	PM_CAP	Power Management Capabilities	See bit description	RO
CC–CDh	PMCSR	Power Management Control/ Status	0000h	R/W, RO, R/WC
CF	PCIDATA	PCI Power Management Data	00h	RO
Message Signaled Interrupt Configuration Registers				
D0h	MSI_CAP_ID	MSI Capability ID	05h	RO
D1h	MSI_NXT_PTR	MSI t Next Item Pointer	E0h	RO
D2-D3	MSI_MCR	MSI Control Register	0080	R/W
D4-D7h	MSI_MAR_LOW	MSI Message Low Address	00000000h	R/W
D8-DB	MSI_MAR_HIGH	MSI Message High Address	00000000h	R/W
DC-DD	MSI_MDR	Message Data Register	0000	R/W
PCI Express* configuration registers				
E0h	PCI Express_CAP_ID	PCI Express Capability Identification Register	10h	RO
E1h	PCI Express_NXT_PTR	PCI Express Next Item Pointer	00h	RO
E2-E3	PCI Express_CAP	PCI Express Capability	0011	RO
E4-E7h	PCI Express_DEV_CAP	PCI Express Device Capability	00000000h	RO
E8-E9	PCI Express_DEV_CONT	PCI Express Device Control	2810h	R/W
EA-EB	PCI Express_DEV_STATUS	PCI Express Device Status	0000h	RO
EC-EF	PCI Express_LINK_CAP	PCI Express Link Capability	See description	RO
F0-F1	PCI Express_LINK_CONT	PCI Express Link Control	0000h	R/W
F2-F3	PCI Express_LINK_STATUS	PCI Express Link Status	1011h	RO

25.4.1 VID – Vendor Identification Register (Bn:F0/F1)

Offset Address: 00–01h
Default Value: 8086h
Attribute: RO
Size: 16 bits

Bit	Description
15:0	**Vendor ID** – RO. This is a 16-bit value assigned to Intel.

25.4.2 DID – Device Identification Register (Bn:F4)

Offset Address: 02–03h
Default Value: 1086h
Attribute: RO
Size: 16 bits

Bit	Description
15:0	**Device ID** - RO. This is a 16-bit value assigned to the Intel® 6321ESB I/O Controller Hub integrated IPMI/KCS0 Controller. If Word 0Ah bit 0 is set in the EEPROM, the Device ID is loaded from the EEPROM, Word 104h/44h after the hardware reset. If not set, the default value is 1086h.

25.4.3 PCICMD – PCI Command Register (Bn:F4)

Offset Address: 04–05h
Default Value: 0000h
Attribute: RO, R/W
Size: 16 bits

15:11	Reserved
10	**Interrupt Disable** – R/W. 0 = Enable. 1 = Disables Serial Port Redirection Controller to assert its INTD signal. The Interrupt Disable register bit is a read-write bit that controls the ability of a PCI Express device to generate a legacy interrupt message. When set, devices are prevented from generating legacy interrupt messages.
9	Fast Back to Back Enable (FBE) – RO. Hardwired to 0. The integrated IPMI/KCS0 Controller will not run fast back-to-back PCI cycles.
8	**SERR# Enable (SERR_EN) –** R/W. 0 = Disable. 1 = Enable. Allow SERR# to be asserted.
7	Wait Cycle Control (WCC) – RO. Hardwired to 0. Not implemented.
6	**Parity Error Response (PER) –** R/W. 0 = The IPMI/KCS0 Controller will ignore PCI parity errors. 1 = The integrated IPMI/KCS0 Controller will take normal action when a PCI parity error is detected and will enable generation of parity on ESI.
5	VGA Palette Snoop (VPS) – RO. Hardwired to 0. Not Implemented.
4	Memory Write and Invalidate Enable (MWIE) – RO. Hardwired to 0. Not Implemented.
3	Special Cycle Enable (SCE) – RO. Hardwired to 0. The IPMI/KCS0 Controller ignores special cycles.
2	**Bus Master Enable (BME)** – R/W. 0 = Disable. 1 = Enable. The Intel® 6321ESB I/O Controller Hub's integrated IPMI/KCS0 Controller may function as a PCI bus master.
1	**Memory Space Enable (MSE) –** R/W. 0 = Disable. 1 = Enable. The Intel® 6321ESB I/O Controller Hub's integrated IPMI/KCS0 Controller will respond to the memory space accesses.
0	**I/O Space Enable (IOSE) –** R/W. 0 = Disable. 1 = Enable. The Intel® 6321ESB I/O Controller Hub's integrated IPMI/KCS0 Controller will respond to the I/O space accesses.
15:11	Reserved

25.4.4 PCISTS – PCI Status Register (Bn:F4)

Offset Address: 06–07h
Default Value: 0010h
Attribute: RO, R/WC
Size: 16 bits

Note: For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 to the bit has no effect.

Bit	Description
15	Detected Parity Error **(**DPE) – R/WC. 0 = Parity error Not detected. 1 = The Intel® 6321ESB I/O Controller Hub's integrated IPMI/KCS0 Controller has detected a parity error on the PCI bus (will be set even if Parity Error Response is disabled in the PCI Command register).
14	Signaled System Error **(**SSE) – R/WC. 0 = Integrated IPMI/KCS0 Controller has **not** asserted SERR# 1 = The Intel® 6321ESB I/O Controller Hub's integrated IPMI/KCS0 Controller has asserted SERR#. SERR# can be routed to cause NMI, SMI#, or interrupt.
13	**Master Abort Status (RMA) –** R/WC. 0 = Master Abort not generated 1 = The Intel® 6321ESB I/O Controller Hub's integrated IPMI/KCS0 Controller (as a PCI master) has generated a master abort.
12	**Received Target Abort (RTA) –** R/WC. 0 = Target abort Not received. 1 = The Intel® 6321ESB I/O Controller Hub's integrated IPMI/KCS0 Controller (as a PCI master) has received a target abort.
11	**Signaled Target Abort (STA) –** R/WC. 0 = Target abort Not signaled. 1 = The Intel® 6321ESB I/O Controller Hub's integrated IPMI/KCS0 Controller (as a PCI master) has signaled a target abort.
10:9	DEVSEL Timing – RO. Hardwired to 0.
8	**Data Parity Error Detected (DPED) –** R/WC. 0 = Parity error Not detected (conditions below are not met). 1 = All of the following three conditions have been met: 1. The IPMI/KCS0 Controller is acting as bus master 2. The IPMI/KCS0 Controller has asserted PERR# (for reads) or detected PERR# asserted (for writes) 3. The Parity Error Response bit in the IPMI/KCS0 Controller's PCI Command Register is set.
7	Fast Back to Back Capable (FB2BC) – RO. Hardwired to 0. The device does not accept fast back-to-back transactions.
6	Reserved.
5	66 MHz Capable (66MHZ_CAP) – RO. Hardwired to 0. The device does not support 66 MHz PCI.
4	**Capabilities List (CAP_LIST) –** RO. Indicates that a device implements Extended Capabilities. 0 = The EEPROM indicates that the integrated IPMI/KCS0 Controller does not support extended capabilities. 1 = The EEPROM indicates that the integrated IPMI/KCS0 Controller supports PCI Power Management, message signaled interrupts, and the PCI express extensions.
3	**Interrupt Status (INTS) –** RO. This bit indicates that an interrupt is pending. It is independent from the state of the Interrupt Enable bit in the command register.
2:0	Reserved

25.4.5 RID – Revision Identification Register (Bn:F4)

Offset Address: 08h Attribute: RO
Default Value: See bit description Size: 8 bits

Bit	Description
7:0	**Revision ID (RID)** – RO. The default revision ID of this device is 00h. The value of the rev ID is a logic OR between the default value and the value in the EEPROM word 1Eh.

25.4.6 PI – Programming Interface Register (Bn:F4)

Offset Address: 09h
Default Value: 01h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Programming Interface(PI)** – RO. This field is loaded from EEPROM, word 4Eh/10Eh

25.4.7 SCC – Sub Class Code Register (Bn:F4)

Offset Address: 0Ah
Default Value: 07h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Sub Class Code (SCC)** – RO. This 8-bit value specifies the sub class of the device as an IPMI/KCS controller. This field is loaded from EEPROM, word 4Eh/10Eh

25.4.8 BCC – Base Class Code Register (Bn:F4)

Offset Address: 0Bh
Default Value: 0Ch
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Base Class Code (BCC)** – RO. This 8-bit value specifies the base class of the device as a IPMI/KCS controller. This field is loaded from EEPROM, word 4Fh/10Fh

25.4.9 CLS – Cache Line Size Register (Bn:F4)

Offset Address: 0Ch
Default Value: See register desc.
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	Cache Line Size(CLS) – R/W. Implement for legacy compatibility purposes but has no impact on any PCI Express device functionality. Loaded from EEPROM 1Ah.

25.4.10 PMLT – Primary Master Latency Timer Register (Bn:F4)

Offset Address: 0Dh
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	Not used. Hardwired to zero.

25.4.11 HEADTYP – Header Type Register (Bn:F4)

Offset Address: 0Eh
Default Value: 00h, 80h
Attribute: RO
Size: 8 bits

Bit	Description
7	**Multi-Function Device (MFD) –** RO. Hardwired to 0 to indicate a single function device, that is, If only a single LAN function is active. 1 for multiple function
6:0	**Header Type (HTYPE) –** RO. This 7-bit field identifies the header layout of the configuration space as an Ethernet controller.

25.4.12 Base Address Registers (Bn:F4)

64-bit Addressing Mode

No EEPROM or the BAR32 EEPROM bit set to 0 (Word 0Ah).

25.4.12.1 IPMI_KCS_MEM_BASE_LOW – IPMI/KCS Memory-Mapped Base Address Low Register (Bn:F4)

Offset Address:	10-13h	Attribute:	R/W, RO
Default Value:	00000004h	Size:	32 bits

Note: The Intel® 6321ESB I/O Controller Hub's integrated IPMI/KCS0 Controller requires one BAR for memory mapping. Software determines which BAR (memory or I/O) is used to access the IPMI/KCS0 Controller's CSR registers.

Bit	Description
31:12	**Base Address (MEM_ADDR) –** R/W. This field contains the upper 20 bits of the base address provides 4 KB of memory-Mapped space for the IPMI/KCS function.
11:4	Reserved
3	**Prefetchable (MEM_PF)** – RO. Hardwired to 0 to indicate that this is not a pre-fetchable memory-Mapped address range.
2:1	**Type (MEM_TYPE)** – RO. Hardwired to 10b to indicate the memory-Mapped address range may be located anywhere in 64-bit address space.
0	**Memory-Space Indicator (MEM_SPACE)** – RO. Hardwired to 0 to indicate that this base address maps to memory space.

25.4.12.2 IPMI_KCS_MEM_BASE_HIGH – IPMI/KCS Memory-Mapped Base Address High Register (Bn:F4)

Offset Address:	14–17h	Attribute:	R/W, RO
Default Value:	00000000h	Size:	32 bits

Note: The Intel® 6321ESB I/O Controller Hub's integrated IPMI/KCS0 Controller requires one BAR for memory mapping. Software determines which BAR (memory or I/O) is used to access the IPMI/KCS0 Controller's CSR registers.

Bit	Description
31:0	**Base Address (MEM_ADDR) –** R/W. This field contains the upper 32 bits of the base address provides 4 KB of memory-Mapped space for the IPMI/KCS function.

25.4.12.3 IPMI_KCS_IO_BASE – IPMI/KCS I/O-Mapped Base Address Register (Bn:F4)

Offset Address:	18–1Bh	Attribute:	R/W, RO
Default Value:	00000001h	Size:	32 bits

Note: The Intel® 6321ESB I/O Controller Hub's integrated IPMI/KCS0 Controller requires one BAR for memory mapping. Software determines which BAR (memory or I/O) is used to access the IPMI/KCS0 Controller's CSR registers.

Bit	Description
31:2	**Base Address (IO_ADDR)** – R/W. This field provides 4 bytes of I/O-Mapped address space for the IPMI/KCS function.
1	Reserved
0	**I/O Space Indicator (IO_SPACE) –** RO. Hardwired to 1 to indicate that this base address maps to I/O space.

32-bit Addressing Mode

BAR32 bit in the EEPROM set to 1 (Word 0Ah).

25.4.12.4 IPMI_KCS_MEM_BASE – IPMI/KCS Memory-Mapped Base Address Register (Bn:F4)

Offset Address: 10-13h Attribute: R/W, RO
Default Value: 00000000h Size: 32 bits

Note: The Intel® 6321ESB I/O Controller Hub's integrated IPMI/KCS0 Controller requires one BAR for memory mapping. Software determines which BAR (memory or I/O) is used to access the IPMI/KCS0 Controller's CSR registers.

Bit	Description
31:12	**Base Address (MEM_ADDR) –** R/W. This field contains the upper 20 bits of the base address provides 4 KB of memory-Mapped space for the IPMI/KCS function.
11:4	Reserved
3	**Prefetchable (MEM_PF)** – RO. Hardwired to 0 to indicate that this is not a pre-fetchable memory-Mapped address range.
2:1	**Type (MEM_TYPE)** – RO. Hardwired to 00b to indicate the memory-Mapped address range may be located anywhere in 32-bit address space.
0	**Memory-Space Indicator (MEM_SPACE)** – RO. Hardwired to 0 to indicate that this base address maps to memory space.

25.4.12.5 IPMI_KCS_IO_BASE – IPMI/KCS I/O-Mapped Base Address Register (Bn:F4)

Offset Address: 14-17h Attribute: R/W, RO
Default Value: 00000001h Size: 32 bits

Note: The Intel® 6321ESB I/O Controller Hub's integrated IPMI/KCS0 Controller requires one BAR for memory mapping. Software determines which BAR (memory or I/O) is used to access the IPMI/KCS0 Controller's CSR registers.

Bit	Description
31:2	**Base Address (IO_ADDR)** – R/W. This field provides 4 bytes of I/O-Mapped address space for the IPMI/KCS function.
1	Reserved
0	**I/O Space Indicator (IO_SPACE)** – RO. Hardwired to 1 to indicate that this base address maps to I/O space.

25.4.13 SVID – Subsystem Vendor Identification(Bn:F4)

Offset Address: 2C–2D
Default Value: 8086h
Attribute: RO
Size: 16 bits

Bit	Description
15:0	**Subsystem Vendor ID (SVID)** – RO. This value may be loaded automatically from the EEPROM address 0Ch upon power up or reset if the EEPROM is present (and properly programmed) and if Word 0Ah bit 1 is set. A value of 0x8086 is default for this field upon power up if the EEPROM does not respond or is not programmed.

25.4.14 SID – Subsystem Identification (Bn:F4)

Offset Address: 2E–2Fh
Default Value: 0000h
Attribute: RO
Size: 16 bits

Bit	Description
15:0	**Subsystem ID (SID)** – RO. This value may be loaded automatically from the EEPROM address 107h/47h upon power up with a default value of 0x0000 if the EEPROM is present (and properly programmed) and if Word 0Ah bit 1 is set.

25.4.15 CAP_PTR – Capabilities Pointer (Bn:F4)

Offset Address: 34h
Default Value: C8h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Capabilities Pointer (CAP_PTR)** – RO. Hardwired to C8h to indicate the offset within configuration space for the location of the Power Management registers.

25.4.16 INT_LN – Interrupt Line Register (Bn:F4)

Offset Address: 3Ch
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	**Interrupt Line (INT_LN) –** R/W. This field identifies the system interrupt line to which the IPMI/KCS0 Controller's PCI interrupt request pin (as defined in the Interrupt Pin Register) is routed.

25.4.17 INT_PN – Interrupt Pin Register (Bn:F4)

Offset Address: 3Dh
Default Value: 04h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Interrupt Pin (INT_PN)** – RO. IPMI/KCS Function - A value of 0x1 / 0x2 / 0x3 / 0x4 indicates that this function implements legacy interrupt on INTA / INTB / INTC / INTD respectively. Loaded from EEPROM word 21h.

25.4.18 MIN_GNT – Minimum Grant Register (Bn:F4)

Offset Address: 3Eh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Minimum Grant (MIN_GNT)** – RO. Not used, hardwired to 00h.

25.4.19 MAX_LAT – Maximum Latency Register (Bn:F4)

Offset Address: 3Fh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Maximum Latency (MAX_LAT)** – RO. Not used, hardwired to 00h.

25.4.20 CAP_ID – Capability Identification Register (Bn:F4)

Offset Address: C8h
Default Value: 01h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Capability ID (CAP_ID)** – RO. Hardwired to 01h to indicate that the Intel® 6321ESB I/O Controller Hub's integrated IPMI/KCS0 Controller supports PCI Power Management.

25.4.21 NXT_PTR – Next Item Pointer (Bn:F4)

Offset Address: C9h
Default Value: D0h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Next Item Pointer (NXT_PTR)** – RO. Hardwired to D0h to indicate that power management is the last item in the capabilities list.

25.4.22 PM_CAP – Power Management Capabilities (Bn:F4)

Offset Address: CA–CBh
Default Value: See bit description
Attribute: RO
Size: 16 bits

Bit	Description
15:11	**PME Support (PME_SUP)** – RO. This 5-bit field indicates the power states in which the IPMI/KCS0 Controller may assert PME#. The default value depends on EEPROM word 0Ah. 00000b = No PME at all states. 01001b = PME at D0 and $D3_{hot}$ 11001b = PME at D0, $D3_{hot}$ and $D3_{cold}$
10:9	**Hardwired to '0'.**
8:6	**Auxiliary Current (AUX_CUR)** – RO. Hardwired to 000b to indicate that the IPMI/KCS0 Controller implements the Data registers. The auxiliary power consumption is the same as the current consumption reported in the D3 state in the Data register.
5	**Device Specific Initialization (DSI)** – RO. Hardwired to 1 to indicate that special initialization of this function is required (beyond the standard PCI configuration header) before the generic class device driver is able to use it. DSI is required for the IPMI/KCS0 Controller after D3-to-D0 reset.

Bit	Description
4	Reserved
3	**PME Clock (PME_CLK)** – RO. Hardwired to 0 to indicate that the IPMI/KCS0 Controller does not require a clock to generate a power management event.
2:0	**Version (VER) –** RO. Hardwired to 010b to indicate that the IPMI/KCS0 Controller complies with of the *PCI Power Management Specification, Revision 1.1.*

25.4.23 PMCSR – Power Management Control/Status Register (Bn:F4)

Offset Address: CC–CDh
Default Value: 0000h
Attribute: RO, R/W, R/WC
Size: 16 bits

Bit	Description
15	**PME Status (PME_STAT)** – R/WC. 0 = Software clears this bit by writing a 1 to it. This also deasserts the PME# signal and clears the PME status bit in the Power Management Driver Register. When the PME# signal is enabled, the PME# signal reflects the state of the PME status bit. 1 = Set upon occurrence of a wakeup event, independent of the state of the PME enable bit.
14:13	**Data Scale (DSCALE) –** RO. This field indicates the data register scaling factor. It equals 10b for all supported registers: 0,3,4,7 and 8, as selected by the “Data Select” field.
12:9	**Data Select (DSEL) –** R/W. This field is used to select which data is reported through the Data register and Data Scale field.
8	**PME Enable (PME_EN)** – R/W. This bit enables the Intel® 6321ESB I/O Controller Hub’s integrated IPMI/KCS0 Controller to assert PME#. 0 = The device will not assert PME#. 1 = Enable PME# assertion when PME Status is set.
7:2	Reserved
1:0	**Power State (PWR_ST) –** R/W. This 2-bit field is used to determine the current power state of the integrated IPMI/KCS0 Controller, and to put it into a new power state. The definition of the field values is as follows: 00 = D0 01/10 = Reserved 11 = D3

25.4.24 PCIDATA – PCI Power Management Data Register (Bn:F4)

Offset Address: CFh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Power Management Data (PWR_MGT) –** RO. State dependent power consumption and heat dissipation data.

This optional register is used to report power consumption and heat dissipation. Reported register is controlled by the Data_Select field in the PMCSR, and the power scale is reported in the Data_Scale field in the PMCSR. The data of this field is loaded from the EEPROM if PM is enabled in the EEPROM or with a default value of 0x00 otherwise. The values for Intel® 6321ESB I/O Controller Hub Serial Port Redirection Controller functions is shown in Table 25-9.

Table 25-9. Data Register Structure

Function	D0 (consume/ dissipate)	D3 (consume/ dissipate)	Common	Data_Scale
Data_Select	(0x0 / 0x4)	(0x3 / 0x7)	(0x8)	
IPMI/KCS	EEP addr 22h	EEP addr 101/41h	0x00	10b

25.4.25 MSI_CAP_ID – Capability Identification Register (Bn:F4)

Offset Address: D0h
Default Value: 05h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Capability ID (CAP_ID)** – RO. Hardwired to 05h to indicate that the linked list item as being the Message Signaled Interrupt registers.

25.4.26 MSI_NXT_PTR – Next Item Pointer (Bn:F4)

Offset Address: D1h
Default Value: E0h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Next Item Pointer (NXT_PTR)** – RO. Hardwired to E0h to indicate that PCI Express capability is the next item in the capability list.

25.4.27 MSI_MCR – Message Control Register (Bn:F4)

Offset Address: D2–D3h
Default Value: 0080
Attribute: RO
Size: 16 bits

Bit	Description
15:11	Reserved.
7	**64 Support (64_SUP)** – RO. Hardwired to 1 to indicate that the IPMI/KCS0 Controller is capable of generating 64 bit message addresses.
6:4	**Multiple Message Enable(MM_ENABLE)** – RO. Hardwired to 000b to indicate that the IPMI/ KCS0 Controller supports single message per function.
3:1	**Multiple Message Capable(MM_CAP)** – RO. Hardwired to 000b to indicate that the IPMI/KCS0 Controller capable of single requested message per function.
0	**MSI ENABLE(MSI_ENABLE) –** R/W. If 1, the IPMI/KCS0 Controller will generate MSI for interrupt assertion instead of INTx signaling.

25.4.28 MSI_MAR_LOW – Message Address Low Register (Bn:F4)

Offset Address: D4–D7h
Default Value: 00000000h
Attribute: RO, R/W, R/WC
Size: 32 bits

Bit	Description
7:2	**Message Address Low(MSG_ADDR_LOW) –** R/W. Written by the system to indicate the lower 32 bits of the address to use for the MSI memory write transaction. The lower two bits will always return 0 regardless of the write operation.

25.4.29 MSI_MAR_HIGH – Message Address High Register (Bn:F4)

Offset Address: D8–DBh
Default Value: 0000h
Attribute: RO, R/W, R/WC
Size: 16 bits

Bit	Description
31:0	**Message Address High(MSG_ADDR_HIGH) –** R/W. This field contains the upper 32 bits of the address to use for the MSI memory write transaction.

25.4.30 MSI_MDR – Message Data Register (Bn:F4)

Offset Address: DC–DDh
Default Value: 0000h
Attribute: R/W
Size: 16 bits

Bit	Description
15:0	**Message Data(MSG_DATA) –** R/W. Written by the system to indicate the lower 16 bits of the data written in the MSI memory write DWORD transaction. The upper 16 bits of the transaction are written as 0

25.4.31 PCI Express_CAP_ID – PCI Express* Capability Identification Register (Bn:F4)

Offset Address: E0h
Default Value: 10h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Capability ID (CAP_ID)** – RO. Hardwired to 10h to indicate that the linked list item as being the PCI Express Capability Registers.

25.4.32 PCI Express_NXT_PTR – PCI Express* Next Item Pointer (Bn:F4)

Offset Address: E1h
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Next Item Pointer (NXT_PTR)** – RO. Hardwired to 00h to indicate that it is the last item in the capability linked list.

25.4.33 PCI Express_CAP – PCI Express* Capability Register (Bn:F4)

Offset Address: E2–E3h
Default Value: 0011
Attribute: RO
Size: 16 bits

Bit	Description
15:14	Reserved.
13:9	**Interrupt Message Number (INT_MSG_NUM)** – RO. Multiple MSI per function is not supported. Hardwired to 00000b
8	**Slot Implemented** – RO. Slot option not implemented hardwired to 0.
7:4	**Device/Port Type** – RO. Indicates the type of PCI Express functions. Hardwired to 0001b
3:0	**Capability version(CAP_VERSION) –** RO. Indicates the PCI Express capability structure version number 0001b.

25.4.34 PCI Express_DEV_CAP – PCI Express* Device Capability Register (Bn:F4)

Offset Address: E4–E7h
Default Value: 00000000h
Attribute: RO, R/W, R/WC
Size: 32 bits

Bit	Description
31:28	Reserved.
27:26	**Slot Power Limit Scale** – RO. Used in upstream port only. Hardwired to 00b.
25:18	**Slot Power Limit Value** – RO. Used in upstream port only. Hardwired to 00b
17:15	Reserved.
14	**Power Indicator Present** – RO. Hardwired to 0b
13	**Attention Indicator Present** – RO. Hardwired to 0b
12	**Attention Button Present** – RO. Hardwired to 0b
11:9	**Endpoint L1 Acceptable Latency** – RO. This field indicates the acceptable latency that Intel® 6321ESB I/O Controller Hub LAN core can withstand due to the transition from L1 state to the L0 state. All functions share the same value loaded from the EEPROM PCI Express* init configuration 1 Word 18h
8:6	**Endpoint L0s Acceptable Latency** – RO. This field indicates the acceptable latency that Intel® 6321ESB I/O Controller Hub LAN core can withstand due to the transition from L0s state to the L0 state. All functions share the same value loaded from the EEPROM PCI Express init configuration 1 Word 18h.
5	**Extended Tag Field Supported –** RO. Indicates the PCI Express capability structure version number 0001b.
4:3	**Phantom Function Supported** – RO. Indicates the type of PCI Express functions. Hardwired to 0001b
2:0	**Max Payload Size Supported** – RO. Indicates the type of PCI Express functions. Hardwired to 0001b

25.4.35 PCI Express_DEV_CONT – PCI Express* Device Control Register (Bn:F4)

Offset Address: E8–E9h
Default Value: 2810h
Attribute: RO, R/W
Size: 16 bits

Bit	Description
15	Reserved.
14:12	**Max Read Request Size** - this field sets maximum read request size for the Device as a requester. The default value is 010b (512B) for the LAN devices.
11	**Enable No Snoop** – R/W. Snoop is gated by NONSNOOP bits in the GCR register in the CSR space. Default is 1b
10	**Auxiliary Power PM Enable** - when set enables the device to draw AUX power independent of PME AUX power. Intel® 6321ESB I/O Controller Hub LAN core is a multi function device, therefore allowed to draw AUX power if at least one of the functions has this bit sets
9	**Phantom Function Enable** – RW. Hardwired to 0b
8	**Extended Tag Field Enable** – RW. Hardwired to 0b
7:5	**Max Payload Size** – RW. Slot option not implemented hardwired to 0.
4	**Enable Relaxed Ordering** – If this bit is set, the device is permitted to set the Relaxed Ordering bit in the attribute field of write transactions that do not need strong ordering. Default to 1b
3	**Unsupported Request Reporting Enable** – RW. Enable error report.
2	**Fatal Error Reporting Enable** – RW. Enable error report.
1	**Non-Fatal Error Reporting Enable** – RW. Enable error report.
0	**Correctable Error Reporting Enable** – RW. Enable error report.

25.4.36 PCI Express_DEV_STATUS – PCI Express* Device Status Register (Bn:F4)

Offset Address: EA–EBh
Default Value: 0000h
Attribute: RO, R/W, R/WC
Size: 16 bits

Bit	Description
15:6	Reserved.
5	**Transaction Pending** – RO. Slot option not implemented hardwired to 0.
4	**Aux Power Detected**– RO. If this bit is set, the device is permitted to set the Relaxed Ordering bit in the attribute field of write transactions that do not need strong ordering. Default to 1b
3	**Unsupported Request Detected** – R/WC. Enable error report.
2	**Fatal Error Detected** – R/WC. Enable error report.
1	**Non-Fatal Error Detected** – R/WC. Enable error report.
0	**Correctable Error Detected** – R/WC. Enable error report.

25.4.37 PCI Express_LINK_CAP – PCI Express* Link Capability Register (Bn:F4)

Offset Address: EC–EFh
Default Value: See description
Attribute: RO, R/W
Size: 16 bits

Bit	Description
31:24	**Port Number** – RO. The PCI Express* port number for the given PCI Express Link. Field is set in the Link training phase. Default to 0x0.
23:18	Reserved.
17:15	**L1 Exit Latency**- Indicates the exit latency from L1 to L0 state. This field is loaded from the EEPROM PCI Express init configuration 1 Word 18h. Default to 110b (32-64us).
14:12	**L0s Exit Latency**- Indicates the exit latency from L0s to L0 state. This field is loaded from the EEPROM PCI Express init configuration 1 Word 18h (two values for Common PCI Express clock or Separate PCI Express clock). Default to 001b (64-128ns).
11:10	**Active State Link PM Support –** RO. Indicates the level of active state power management supported in Intel® 6321ESB I/O Controller Hub LAN core. Defined encodings are: 00b Reserved 01b L0s Entry Supported 10b Reserved 11b L0s and L1 Supported This field is loaded from the EEPROM PCI Express init configuration 3 Word 1Ah.Default to 11b
9:4	**Max Link Width** – RO.Indicates the max link width. Intel® 6321ESB I/O Controller Hub LAN controller can support by 1 and by 4-link width. The field is loaded from the EEPROM PCI Express init configuration 3 Word 1Ah with a default value of 4 lanes. Default to 00100b.
3:0	**Max Link Speed** – RO. Indicates a max link speed of 2.5 Gbps. Default to 0001b

25.4.38 PCI Express_LINK_CONT – PCI Express* Link Control Register (Bn:F4)

Offset Address: F0–F1h
Default Value: 0000h
Attribute: R/W
Size: 16 bits

Bit	Description
15:8	Reserved.
7	**Extended Synch** – RW. This bit forces extended Tx of FTS ordered set in FTS and extra TS2 at exit from L1 prior to enter L0.
6	**Common Clock Configuration** – RW. When set indicates that Intel® 6321ESB I/O Controller Hub and the component at the other end of the link are operating with a common reference clock. A value of 0 indicates that they operating with an asynchronous clock. This parameter affects the L0s Exit Latencies.
5	**Retrain Clock** – RO. Not applicable for endpoint devices, hardwired to 0.
4	**Link Disable** – RO. Not applicable for endpoint devices, hardwired to 0.
3	**Read Completion Boundary** – RW.
2	Reserved.
1:0	**Active State Link PM Control –** R/W. this field controls the active state PM supported on the link. Link PM functionality is determined by the lowest common denominator of all functions. Defined encodings are: 00b PM Disabled 01b L0s Entry Supported 10b Reserved 11b L0s and L1 Supported

25.4.39 PCI Express_LINK_STATUS – PCI Express* Link Status Register (Bn:F4)

Offset Address: F2–F3h
Default Value: 1011h
Attribute: R/W
Size: 16 bits

Bit	Description
15:13	Reserved.
12	**Slot Clock Configuration** – When set, it indicates it uses the physical reference clock that the platform provides on the connector. This bit must be cleared uses an independent clock.Default to be 1b.
11	**Link Training** – RO. Indicates that link training is in progress.
10	**Link Training Error** – RO. Indicates that link training error has occurred.
9:4	**Negotiated Link Width** – RO. Indicates the negotiated width of the link. 000001b = x1 000100b = x4
3:0	**Link Speed** – RO. Indicates a max link speed of 2.5 Gbps. Default to 0001b

25.5 UHCI Redirection Controller Configuration Registers (Bn:F5)

Table 25-10. UHCI Configuration Register Address Map Bn:F5) (Sheet 1 of 2)

Offset	Mnemonic	Register Name	Default	Type
Mandatory PCI Configuration Registers				
00–01h	VID	Vendor Identification	8086h	RO
02–03h	DID	Device Identification	1087h	RO
04–05h	PCICMD	PCI Command	0000h	RO, RW
06–07h	PCISTS	PCI Status	0010h	RO, R/WC
08h	RID	Revision Identification	See register description.	RO
09h	PI	Program Interface	00h	RO
0Ah	SCC	Sub Class Code	03h	RO
0Bh	BCC	Base Class Code	0C	RO
0Ch	CLS	Cache Line Size	See register description.	R/W
0Dh	PMLT	Primary Master Latency Timer	00h	R/W
0Eh	HEADTYP	Header Type	00h	RO
BAR registers for 64-bit addressing modes				
10–13h	UHCI_MEM_BASE_LOW	UHCI Mem–Mapped Low Base Address	00000000h	R/W, RO
14–17h	UHCI_MEM_BASE_HIGH	UHCI Mem–Mapped Base Address	00000000h	R/W, RO
20–23h	UHCI_IO_BASE	UHCI I/O–Mapped Base Address	00000001h	R/W, RO
BAR registers for 32-bit addressing modes				
10–13h	UHCI_MEM_BASE	UHCI Mem–Mapped Base Address	00000000h	R/W, RO
20–23h	UHCI_IO_BASE	UHCI I/O–Mapped Base Address	00000001h	R/W, RO
2C–2Dh	SVID	Subsystem Vendor Identification	8086h	RO
2E–2Fh	SID	Subsystem Identification	0000h	RO
34h	CAP_PTR	Capabilities Pointer	C8h	RO
3Ch	INT_LN	Interrupt Line	00h	R/W
3Dh	INT_PN	Interrupt Pin	04h	RO
3Eh	MIN_GNT	Minimum Grant	00h	RO
3Fh	MAX_LAT	Maximum Latency	00h	RO
60h	USBRN	USB Release Number	10h	RO
C0h	USB_LEGSUP	USB interrupt Mechanism	2000h	RO, R/W
PCI Power Management Registers				
C8h	CAP_ID	Capability ID	01h	RO

Table 25-10. UHCI Configuration Register Address Map Bn:F5) (Sheet 2 of 2)

Offset	Mnemonic	Register Name	Default	Type
C9h	NXT_PTR	Next Item Pointer	D0h	RO
CA–CBh	PM_CAP	Power Management Capabilities	See bit description	RO
CC–CDh	PMCSR	Power Management Control/ Status	0000h	R/W, RO, R/ WC
CF	PCIDATA	PCI Power Management Data	00h	RO
Message Signaled Interrupt Configuration Registers				
D0h	MSI_CAP_ID	MSI Capability ID	05h	RO
D1h	MSI_NXT_PTR	MSI t Next Item Pointer	E0h	RO
D2-D3	MSI_MCR	MSI Control Register	0080	R/W
D4-D7h	MSI_MAR_LOW	MSI Message Low Address	00000000h	R/W
D8-DB	MSI_MAR_HIGH	MSI Message High Address	00000000h	R/W
DC-DD	MSI_MDR	Message Data Register	0000	R/W
PCI Express* Configuration Registers				
E0h	PCI Express_CAP_ID	PCI Express* Capability Identification Register	10h	RO
E1h	PCI Express_NXT_PTR	PCI Express Next Item Pointer	00h	RO
E2-E3	PCI Express_CAP	PCI Express Capability	0011	RO
E4-E7h	PCI Express_DEV_CAP	PCI Express Device Capability	00000000h	RO
E8-E9	PCI Express_DEV_CONT	PCI Express Device Control	2810h	R/W
EA-EB	PCI Express_DEV_STATUS	PCI Express Device Status	0000h	RO
EC-EF	PCI Express_LINK_CAP	PCI Express Link Capability	See bit description	RO
F0-F1	PCI Express_LINK_CONT	PCI Express Link Control	0000h	R/W
F2-F3	PCI Express_LINK_STATUS	PCI Express Link Status	1011h	RO

25.5.1 VID – Vendor Identification Register (Bn:F0/F1)

Offset Address: 00–01h
Default Value: 8086h
Attribute: RO
Size: 16 bits

Bit	Description
15:0	**Vendor ID** – RO. This is a 16-bit value assigned to Intel.

25.5.2 DID – Device Identification Register (Bn:F5)

Offset Address: 02–03h
Default Value: 1087h
Attribute: RO
Size: 16 bits

Bit	Description
15:0	**Device ID –** RO. This is a 16-bit value assigned to the Intel® 6321ESB I/O Controller Hub integrated UHCI redirection Controller. If Word 0Ah bit 0 is set in the EEPROM, the Device ID is loaded from the EEPROM, Word 110h/50h after the hardware reset. If not set, the default value is 1087h.

25.5.3 PCICMD – PCI Command Register (Bn:F5)

Offset Address: 04–05h
Default Value: 0000h
Attribute: RO, R/W
Size: 16 bits

Bit	Description
15:11	Reserved
10	**Interrupt Disable** – R/W. 0 = Enable. 1 = Disables UHCI Redirection Controller to assert its INTD signal. The Interrupt Disable register bit is a read-write bit that controls the ability of a PCI Express device to generate a legacy interrupt message. When set, devices are prevented from generating legacy interrupt messages.
9	Fast Back to Back Enable (FBE) – RO. Hardwired to 0. The integrated UHCI Redirection Controller will not run fast back-to-back PCI cycles.
8	**SERR# Enable (SERR_EN) –** R/W. 0 = Disable. 1 = Enable. Allow SERR# to be asserted.
7	Wait Cycle Control (WCC) – RO. Hardwired to 0. Not implemented.
6	**Parity Error Response (PER) –** R/W. 0 = The UHCI Redirection Controller will ignore PCI parity errors. 1 = The integrated UHCI Redirection Controller will take normal action when a PCI parity error is detected and will enable generation of parity on ESI.
5	**Palette Snoop Enable (PSE) –** RO. Hardwired to 0. Not Implemented.
4	Memory Write and Invalidate Enable (MWIE) – RO. Hardwired to 0. Not Implemented.
3	**Special Cycle Monitoring (SCM) –** RO. Hardwired to 0. The IDE Redirection Controller ignores special cycles.
2	**Bus Master Enable (BME)** – R/W. 0 = Disable. 1 = Enable. The Intel® 6321ESB I/O Controller Hub's integrated UHCI Redirection Controller may function as a PCI bus master.
1	**Memory Space Enable (MSE) –** R/W. 0 = Disable. 1 = Enable. The Intel® 6321ESB I/O Controller Hub's integrated UHCI Redirection Controller will respond to the memory space accesses.
0	**I/O Space Enable (IOSE) –** R/W. 0 = Disable. 1 = Enable. The Intel® 6321ESB I/O Controller Hub's integrated UHCI Redirection Controller will respond to the I/O space accesses.

25.5.4 PCISTS – PCI Status Register (Bn:F5)

Offset Address: 06–07h
Default Value: 0010h
Attribute: RO, R/WC
Size: 16 bits

Note: For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 to the bit has no effect.

Bit	Description
15	**Detected Parity Error (DPE)** – R/WC. 0 = Parity error Not detected. 1 = The Intel® 6321ESB I/O Controller Hub's integrated UHCI Redirection Controller has detected a parity error on the PCI bus (will be set even if Parity Error Response is disabled in the PCI Command register).
14	**Signaled System Error (SSE)** – R/WC. 0 = Integrated UHCI Redirection Controller has **not** asserted SERR# 1 = The Intel® 6321ESB I/O Controller Hub's integrated UHCI Redirection Controller has asserted SERR#. SERR# can be routed to cause NMI, SMI#, or interrupt.
13	**Master Abort Status (RMA) –** R/WC. 0 = Master Abort not generated 1 = The Intel® 6321ESB I/O Controller Hub's integrated UHCI Redirection Controller (as a PCI master) has generated a master abort.
12	**Received Target Abort (RTA) –** R/WC. 0 = Target abort Not received. 1 = The Intel® 6321ESB I/O Controller Hub's integrated UHCI Redirection Controller (as a PCI master) has received a target abort.
11	**Signaled Target Abort (STA) –** R/WC. 0 = Target abort Not signaled. 1 = The Intel® 6321ESB I/O Controller Hub's integrated UHCI Redirection Controller (as a PCI master) has signaled a target abort.
10:9	DEVSEL Timing – RO. Hardwired to 0.
8	**Data Parity Error Detected (DPED) –** R/WC. 0 = Parity error Not detected (conditions below are not met). 1 = All of the following three conditions have been met: 1. The UHCI Redirection Controller is acting as bus master 2. The UHCI Redirection Controller has asserted PERR# (for reads) or detected PERR# asserted (for writes) 3. The Parity Error Response bit in the UHCI Redirection Controller's PCI Command Register is set.
7	Fast Back to Back Capable (FB2BC) – RO. Hardwired to 0. The device does not accept fast back-to-back transactions.
6	Reserved.
5	66 MHz Capable (66MHZ_CAP) – RO. Hardwired to 0. Not implemented.
4	**Capabilities List (CAP_LIST) –** RO. Indicates that a device implements Extended Capabilities. 0 = The EEPROM indicates that the integrated UHCI Redirection Controller does not support extended capabilities. 1 = The EEPROM indicates that the integrated UHCI Redirection Controller supports PCI Power Management, message signaled interrupts, and the PCI express extensions.
3	**Interrupt Status (INTS) –** RO. This bit indicates that an interrupt is pending. It is independent from the state of the Interrupt Enable bit in the command register.
2:0	Reserved

25.5.5 RID – Revision Identification Register (Bn:F5)

Offset Address: 08h
Default Value: See bit description
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Revision ID (RID)** – RO. The default revision ID of this device is 00h. The value of the rev ID is a logic OR between the default value and the value in the EEPROM word 1Eh. Refer to Table 2-33 or the *Intel® 631xESB/632xESB I/O Controller Hub EDS Specification Update* for the value of the Revision ID Register.

25.5.6 PI – Programming Interface Register (Bn:F5)

Offset Address: 09h
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Programming Interface(PI)** – RO.

25.5.7 SCC – Sub Class Code Register (Bn:F5)

Offset Address: 0Ah
Default Value: 03h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Sub Class Code (SCC)** – RO. This 8-bit value specifies the sub class of the device as an UHCI redirection controller.

25.5.8 BCC – Base-Class Code Register (Bn:F5)

Offset Address: 0Bh
Default Value: 0Ch
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Base Class Code (BCC)** – RO. This 8-bit value specifies the base class of the device as a mass storage controller.

25.5.9 CLS – Cache Line Size Register (Bn:F5)

Offset Address: 0Ch
Default Value: See register desc.
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	Cache Line Size(CLS) – R/W. Implement for legacy compatibility purposes but has no impact on any PCI Express device functionality. Loaded from EEPROM 1Ah.

25.5.10 PMLT – Primary Master Latency Timer Register (Bn:F5)

Offset Address: 0Dh
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	Not used. Hardwired to zero

25.5.11 HEADTYP – Header Type Register (Bn:F5)

Offset Address: 0Eh
Default Value: 00h, 80h
Attribute: RO
Size: 8 bits

Bit	Description
7	**Multi-Function Device (MFD) –** RO. Hardwired to 0 to indicate a single function device, that is, If only a single LAN function is active. 1 for multiple function
6:0	**Header Type (HTYPE) –** RO. This 7-bit field identifies the header layout of the configuration space as an Ethernet controller.

25.5.12 Base Address Registers (Bn:F5)

64-bit Addressing Mode

No EEPROM or the BAR32 EEPROM bit set to 0 (Word 0Ah)

25.5.12.1 UHCI_MEM_BASE_LOW – UHCI Memory-Mapped Base Address Low Register (Bn:F5)

Offset Address:	10-13h	Attribute:	R/W, RO
Default Value:	00000000h	Size:	32 bits

Note: The Intel® 6321ESB I/O Controller Hub's integrated UHCI Redirection Controller requires one BAR for memory mapping. Software determines which BAR (memory or I/O) is used to access the UHCI Redirection Controller's CSR registers.

Bit	Description
31:12	**Base Address (MEM_ADDR) –** R/W. This field contains the upper 20 bits of the base address provides 4 KB of memory-Mapped space for the UHCI function.
11:4	Reserved
3	**Prefetchable (MEM_PF)** – RO. Hardwired to 0 to indicate that this is not a pre-fetchable memory-Mapped address range.
2:1	**Type (MEM_TYPE)** – RO. Hardwired to 10b to indicate the memory-Mapped address range may be located anywhere in 64-bit address space.
0	**Memory-Space Indicator (MEM_SPACE)** – RO. Hardwired to 0 to indicate that this base address maps to memory space.

25.5.12.2 UHCI_MEM_BASE_HIGH – UHCI Memory-Mapped Base Address High Register (Bn:F5)

Offset Address:	14–17h	Attribute:	R/W, RO
Default Value:	00000000h	Size:	32 bits

Note: The Intel® 6321ESB I/O Controller Hub's integrated UHCI Redirection Controller requires one BAR for memory mapping. Software determines which BAR (memory or I/O) is used to access the UHCI Redirection Controller's CSR registers.

Bit	Description
31:0	**Base Address (MEM_ADDR) –** R/W. This field contains the upper 32 bits of the base address provides 4 KB of memory-Mapped space for the UHCI function.

25.5.12.3 UHCI_IO_BASE – UHCI I/O-Mapped Base Address Register (Bn:F5)

Offset Address:	20–23h	Attribute:	R/W, RO
Default Value:	00000001h	Size:	32 bits

Note: The Intel® 6321ESB I/O Controller Hub's integrated UHCI Redirection Controller requires one BAR for memory mapping. Software determines which BAR (memory or I/O) is used to access the UHCI Redirection Controller's CSR registers.

Bit	Description
31:5	**Base Address (IO_ADDR)** – R/W. This field provides 4 bytes of I/O-Mapped address space for the UHCI function.
4:1	Reserved
0	**I/O Space Indicator (IO_SPACE) –** RO. Hardwired to 1 to indicate that this base address maps to I/O space.

32-bit Addressing Mode

25.5.12.4 UHCI_MEM_BASE – UHCI Memory-Mapped Base Address Register (Bn:F5)

Offset Address:	10-13h	Attribute:	R/W, RO
Default Value:	00000000h	Size:	32 bits

Note: The Intel® 6321ESB I/O Controller Hub's integrated UHCI Redirection Controller requires one BAR for memory mapping. Software determines which BAR (memory or I/O) is used to access the UHCI Redirection Controller's CSR registers.

Bit	Description
31:12	**Base Address (MEM_ADDR) –** R/W. This field contains the upper 20 bits of the base address provides 4 KB of memory-Mapped space for the UHCI function.
11:4	Reserved
3	**Prefetchable (MEM_PF)** – RO. Hardwired to 0 to indicate that this is not a pre-fetchable memory-Mapped address range.
2:1	**Type (MEM_TYPE)** – RO. Hardwired to 00b to indicate the memory-Mapped address range may be located anywhere in 32-bit address space.
0	**Memory-Space Indicator (MEM_SPACE)** – RO. Hardwired to 0 to indicate that this base address maps to memory space.

25.5.12.5 UHCI_IO_BASE – UHCI I/O-Mapped Base Address Register (Bn:F5)

Offset Address:	20-23h	Attribute:	R/W, RO
Default Value:	00000001h	Size:	32 bits

Note: The Intel® 6321ESB I/O Controller Hub's integrated UHCI Redirection Controller requires one BAR for memory mapping. Software determines which BAR (memory or I/O) is used to access the UHCI Redirection Controller's CSR registers.

Bit	Description
31:5	**Base Address (IO_ADDR)** – R/W. This field provides 4 bytes of I/O-Mapped address space for the UHCI function.
4:1	Reserved
0	**I/O Space Indicator (IO_SPACE)** – RO. Hardwired to 1 to indicate that this base address maps to I/O space.

25.5.13 SVID – Subsystem Vendor Identification(Bn:F5)

Offset Address:	2C–2D	Attribute:	RO
Default Value:	8086h	Size:	16 bits

Bit	Description
15:0	**Subsystem Vendor ID (SVID)** – RO. This value may be loaded automatically from the EEPROM address 0Ch upon power up or reset if the EEPROM is present (and properly programmed) and if Word 0Ah bit 1 is set. A value of 0x8086 is default for this field upon power up if the EEPROM does not respond or is not programmed.

25.5.14 SID – Subsystem Identification (Bn:F5)

Offset Address: 2E–2Fh
Default Value: 0000h
Attribute: RO
Size: 16 bits

Bit	Description
15:0	**Subsystem ID (SID)** – RO. This value may be loaded automatically from the EEPROM address 113h/53h upon power up with a default value of 0x0000 if the EEPROM is present (and properly programmed) and if Word 0Ah bit 1 is set.

25.5.15 CAP_PTR – Capabilities Pointer (Bn:F5)

Offset Address: 34h
Default Value: C8h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Capabilities Pointer (CAP_PTR)** – RO. Hardwired to C8h to indicate the offset within configuration space for the location of the Power Management registers.

25.5.16 INT_LN – Interrupt Line Register (Bn:F5)

Offset Address: 3Ch
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	**Interrupt Line (INT_LN) –** R/W. This field identifies the system interrupt line to which the UHCI Redirection Controller's PCI interrupt request pin (as defined in the Interrupt Pin Register) is routed.

25.5.17 INT_PN – Interrupt Pin Register (Bn:F5)

Offset Address: 3Dh
Default Value: 04h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Interrupt Pin (INT_PN)** – RO. UHCI Function - A value of 0x1 / 0x2 / 0x3 / 0x4 indicates that this function implements legacy interrupt on INTA / INTB / INTC / INTD respectively. Loaded from EEPROM word 0x6B/0x12B.

25.5.18 MIN_GNT – Minimum Grant Register (Bn:F5)

Offset Address: 3Eh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Minimum Grant (MIN_GNT)** – RO. Not used, hardwired to 00h.

25.5.19 MAX_LAT – Maximum Latency Register (Bn:F5)

Offset Address: 3Fh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Maximum Latency (MAX_LAT)** – RO. Not used, hardwired to 00h.

25.5.20 USB_RELNUM – USB Release Number (Bn:F5)

Offset Address: 60h
Default Value: 10h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	Serial Bus Release Number – RO. Hardwired to 10h to indicates compliance with USB 1.0 spec.

25.5.21 USB_LEGSUP – USB Interrupt Mechanism(Bn:F5)

Offset Address: C0h
Default Value: 2000h
Attribute: R/W,RO
Size: 16 bits

Note: The Command Register indicates the command to be executed by the serial bus host controller.

Bit	Description
15:14	Reserved
13	USBPIRQEN – R/W. This bit is used to prevent the USB controller from generating an interrupt due to transactions on its ports. Note that, when disabled, it will probably be configured to generate an SMI using bit 4 of this register. Default to 1 for compatibility with older USB software. Mapped to UHCI_INT[5] 0 = Disable 1 = Enable. Default to 1
12	SMIBYUSB - RO. This bit indicates if an interrupt event occurred from this controller. The interrupt from the controller is taken before the enable in bit 13 has any effect to create this read-only bit. Note that even if the corresponding enable bit is not set in Bit 4, this bit may still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Software should clear the interrupts via the USB controllers. Writing a 1 to this bit will have no effect. Mapped to UHCI_INT[6] 1 = Event Occurred. 0 = No Event. Default to 0
11:5	Reserved
4	USBSMIEN - R/W, SMI on USB IRQ Enable Mapped to UHCI_INT[4] 0 = Disable 1 = Enable. USB interrupt will cause an SMI event.
3:0	Reserved

25.5.22 CAP_ID – Capability Identification Register (Bn:F5)

Offset Address: C8h
Default Value: 01h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Capability ID (CAP_ID)** – RO. Hardwired to 01h to indicate that the Intel® 6321ESB I/O Controller Hub's integrated UHCI Redirection Controller supports PCI Power Management.

25.5.23 NXT_PTR – Next Item Pointer (Bn:F5)

Offset Address: C9h
Default Value: D0h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Next Item Pointer (NXT_PTR)** – RO. Hardwired to D0h to indicate that power management is the last item in the capabilities list.

25.5.24 PM_CAP – Power Management Capabilities (Bn:F5)

Offset Address: CA–CBh
Default Value: See bit description
Attribute: RO
Size: 16 bits

Bit	Description
15:11	**PME Support (PME_SUP)** – RO. This 5-bit field indicates the power states in which the UHCI Redirection Controller may assert PME#. The default value depends on EEPROM word 0Ah. 00000b = No PME at all states. 01001b = PME at D0 and $D3_{hot}$ 11001b = PME at D0, $D3_{hot}$ and $D3_{cold}$
10:9	**Hardwired to '0'.**
8:6	**Auxiliary Current (AUX_CUR)** – RO. Hardwired to 000b to indicate that the UHCI Redirection Controller implements the Data registers. The auxiliary power consumption is the same as the current consumption reported in the D3 state in the Data register.
5	**Device Specific Initialization (DSI)** – RO. Hardwired to 1 to indicate that special initialization of this function is required (beyond the standard PCI configuration header) before the generic class device driver is able to use it. DSI is required for the UHCI Redirection Controller after D3-to-D0 reset.
4	Reserved
3	**PME Clock (PME_CLK)** – RO. Hardwired to 0 to indicate that the UHCI Redirection Controller does not require a clock to generate a power management event.
2:0	**Version (VER) –** RO. Hardwired to 010b to indicate that the UHCI Redirection Controller complies with of the *PCI Power Management Specification, Revision 1.1.*

25.5.25 PMCSR – Power Management Control/Status Register (Bn:F5)

Offset Address: CC–CDh
Default Value: 0000h
Attribute: RO, R/W, R/WC
Size: 16 bits

Bit	Description
15	PME Status **(PME_STAT)** – R/WC. 0 = Software clears this bit by writing a 1 to it. This also deasserts the PME# signal and clears the PME status bit in the Power Management Driver Register. When the PME# signal is enabled, the PME# signal reflects the state of the PME status bit. 1 = Set upon occurrence of a wakeup event, independent of the state of the PME enable bit.
14:13	**Data Scale (DSCALE) –** RO. This field indicates the data register scaling factor. It equals 10b for all supported registers: 0,3,4,7 and 8, as selected by the “Data Select” field.
12:9	**Data Select (DSEL) –** R/W. This field is used to select which data is reported through the Data register and Data Scale field.
8	**PME Enable (PME_EN)** – R/W. This bit enables the Intel® 6321ESB I/O Controller Hub’s integrated UHCI Redirection Controller to assert PME#. 0 = The device will not assert PME#. 1 = Enable PME# assertion when PME Status is set.
7:2	Reserved
1:0	**Power State (PWR_ST) –** R/W. This 2-bit field is used to determine the current power state of the integrated UHCI Redirection Controller, and to put it into a new power state. The definition of the field values is as follows: 00 = D0 01/10 = Reserved 11 = D3

25.5.26 PCIDATA – PCI Power Management Data Register (Bn:F5)

Offset Address: CFh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Power Management Data (PWR_MGT) –** RO. State dependent power consumption and heat dissipation data.

This optional register is used to report power consumption and heat dissipation. Reported register is controlled by the Data_Select field in the PMCSR, and the power scale is reported in the Data_Scale field in the PMCSR. The data of this field is loaded from the EEPROM if PM is enabled in the EEPROM or with a default value of 0x00 otherwise. The values for Intel® 6321ESB I/O Controller Hub UHCI Redirection Controller functions is shown in Table 25-11.

Table 25-11. Data Register Structure

Function	D0 (consume/ dissipate)	D3 (consume/ dissipate)	Common	Data_Scale
Data_Select	**(0x0 / 0x4)**	**(0x3 / 0x7)**	**(0x8)**	
UHCI Redirection controller	EEP addr 119h/59h	EEP addr 11Ah/5Ah	EEP addr 22h	10b

25.5.27 MSI_CAP_ID – Capability Identification Register (Bn:F5)

Offset Address: D0h
Default Value: 05h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Capability ID (CAP_ID)** – RO. Hardwired to 05h to indicate that the linked list item as being the Message Signaled Interrupt registers.

25.5.28 MSI_NXT_PTR – Next Item Pointer (Bn:F5)

Offset Address: D1h
Default Value: E0h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Next Item Pointer (NXT_PTR)** – RO. Hardwired to E0h to indicate that PCI Express capability is the next item in the capability list.

25.5.29 MSI_MCR – Message Control Register (Bn:F5)

Offset Address: D2–D3h
Default Value: 0080
Attribute: RO
Size: 16 bits

Bit	Description
15:11	Reserved.
7	**64 Support (64_SUP)** – RO. Hardwired to 1 to indicate that the UHCI Redirection Controller is capable of generating 64 bit message addresses.

Bit	Description
6:4	**Multiple Message Enable(MM_ENABLE)** – RO. Hardwired to 000b to indicate that the UHCI Redirection Controller supports single message per function.
3:1	**Multiple Message Capable(MM_CAP)** – RO. Hardwired to 000b to indicate that the UHCI Redirection Controller capable of single requested message per function.
0	**MSI ENABLE(MSI_ENABLE) –** R/W. If 1, the UHCI Redirection Controller will generate MSI for interrupt assertion instead of INTx signaling.

25.5.30 MSI_MAR_LOW – Message Address Low Register (Bn:F5)

Offset Address: D4–D7h
Default Value: 00000000h
Attribute: RO, R/W, R/WC
Size: 32 bits

Bit	Description
7:2	**Message Address Low(MSG_ADDR_LOW) –** R/W. Written by the system to indicate the lower 32 bits of the address to use for the MSI memory write transaction. The lower two bits will always return 0 regardless of the write operation.

25.5.31 MSI_MAR_HIGH – Message Address High Register (Bn:F5)

Offset Address: D8–DBh
Default Value: 0000h
Attribute: RO, R/W, R/WC
Size: 16 bits

Bit	Description
31:0	**Message Address High(MSG_ADDR_HIGH) –** R/W. This field contains the upper 32 bits of the address to use for the MSI memory write transaction.

25.5.32 MSI_MDR – Message Data Register (Bn:F5)

Offset Address: DC–DDh
Default Value: 0000h
Attribute: R/W
Size: 16 bits

Bit	Description
15:0	**Message Data(MSG_DATA) –** R/W. Written by the system to indicate the lower 16 bits of the data written in the MSI memory write DWORD transaction. The upper 16 bits of the transaction are written as 0

25.5.33 PCI Express_CAP_ID – PCI Express* Capability Identification Register (Bn:F5)

Offset Address: E0h
Default Value: 10h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Capability ID (CAP_ID)** – RO. Hardwired to 10h to indicate that the linked list item as being the PCI Express Capability Registers.

25.5.34 PCI Express_NXT_PTR – PCI Express* Next Item Pointer (Bn:F5)

Offset Address: E1h
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Next Item Pointer (NXT_PTR)** – RO. Hardwired to 00h to indicate that it is the last item in the capability linked list.

25.5.35 PCI Express_CAP – PCI Express* Capability Register (Bn:F5)

Offset Address: E2–E3h
Default Value: 0011
Attribute: RO
Size: 16 bits

Bit	Description
15:14	Reserved.
13:9	**Interrupt Message Number (INT_MSG_NUM)** – RO. Multiple MSI per function is not supported. Hardwired to 00000b
8	**Slot Implemented** – RO. Slot option not implemented hardwired to 0.
7:4	**Device/Port Type** – RO. Indicates the type of PCI Express functions. Hardwired to 0001b
3:0	**Capability version(CAP_VERSION) –** RO. Indicates the PCI Express capability structure version number 0001b.

25.5.36 PCI Express_DEV_CAP – PCI Express* Device Capability Register (Bn:F5)

Offset Address: E4–E7h
Default Value: 00000000h
Attribute: RO, R/W, R/WC
Size: 32 bits

Bit	Description
31:28	Reserved.
27:26	**Slot Power Limit Scale** – RO. Used in upstream port only. Hardwired to 00b.
25:18	**Slot Power Limit Value** – RO. Used in upstream port only. Hardwired to 00b
17:15	Reserved.
14	**Power Indicator Present** – RO. Hardwired to 0b
13	**Attention Indicator Present** – RO. Hardwired to 0b
12	**Attention Button Present** – RO. Hardwired to 0b
11:9	**Endpoint L1 Acceptable Latency** – RO. This field indicates the acceptable latency that Intel® 6321ESB I/O Controller Hub LAN core can withstand due to the transition from L1 state to the L0 state. All functions share the same value loaded from the EEPROM PCI Express* init configuration 1 Word 18h
8:6	**Endpoint L0s Acceptable Latency** – RO. This field indicates the acceptable latency that Intel® 6321ESB I/O Controller Hub LAN core can withstand due to the transition from L0s state to the L0 state. All functions share the same value loaded from the EEPROM PCI Express init configuration 1 Word 18h.
5	**Extended Tag Field Supported –** RO. Indicates the PCI Express capability structure version number 0001b.
4:3	**Phantom Function Supported** – RO. Indicates the type of PCI Express functions. Hardwired to 0001b
2:0	**Max Payload Size Supported** – RO. Indicates the type of PCI Express functions. Hardwired to 0001b

25.5.37 PCI Express_DEV_CONT – PCI Express* Device Control Register (Bn:F5)

Offset Address: E8–E9h
Default Value: 2810h
Attribute: RO, R/W
Size: 16 bits

Bit	Description
15	Reserved.
14:12	**Max Read Request Size** - this field sets maximum read request size for the Device as a requester. The default value is 010b (512B) for the LAN devices.
11	**Enable No Snoop** – R/W. Snoop is gated by NONSNOOP bits in the GCR register in the CSR space. Default is 1b
10	**Auxiliary Power PM Enable** - when set enables the device to draw AUX power independent of PME AUX power. Intel® 6321ESB I/O Controller Hub LAN core is a multi function device, therefore allowed to draw AUX power if at least one of the functions has this bit sets
9	**Phantom Function Enable** – RW. Hardwired to 0b
8	**Extended Tag Field Enable** – RW. Hardwired to 0b
7:5	**Max Payload Size** – RW. Slot option not implemented hardwired to 0.
4	**Enable Relaxed Ordering** – If this bit is set, the device is permitted to set the Relaxed Ordering bit in the attribute field of write transactions that do not need strong ordering. Default to 1b
3	**Unsupported Request Reporting Enable** – RW. Enable error report.
2	**Fatal Error Reporting Enable** – RW. Enable error report.
1	**Non-Fatal Error Reporting Enable** – RW. Enable error report.
0	**Correctable Error Reporting Enable** – RW. Enable error report.

25.5.38 PCI Express_DEV_STATUS – PCI Express* Device Status Register (Bn:F5)

Offset Address: EA–EBh
Default Value: 0000h
Attribute: RO, R/W, R/WC
Size: 16 bits

Bit	Description
15:6	Reserved.
5	**Transaction Pending** – RO. Slot option not implemented hardwired to 0.
4	**Aux Power Detected**– RO. If this bit is set, the device is permitted to set the Relaxed Ordering bit in the attribute field of write transactions that do not need strong ordering. Default to 1b
3	**Unsupported Request Detected** – R/WC. Enable error report.
2	**Fatal Error Detected** – R/WC. Enable error report.
1	**Non-Fatal Error Detected** – R/WC. Enable error report.
0	**Correctable Error Detected** – R/WC. Enable error report.

25.5.39 PCI Express_LINK_CAP – PCI Express* Link Capability Register (Bn:F5)

Offset Address: EC–EFh
Default Value: See description
Attribute: RO, R/W
Size: 16 bits

Bit	Description
31:24	**Port Number** – RO. The PCI Express* port number for the given PCI Express Link. Field is set in the Link training phase. Default to 0x0.
23:18	Reserved.
17:15	**L1 Exit Latency**- Indicates the exit latency from L1 to L0 state. This field is loaded from the EEPROM PCI Express init configuration 1 Word 18h. Default to 110b (32-64us).
14:12	**L0s Exit Latency**- Indicates the exit latency from L0s to L0 state. This field is loaded from the EEPROM PCI Express init configuration 1 Word 18h (two values for Common PCI Express clock or Separate PCI Express clock). Default to 001b (64-128ns).
11:10	**Active State Link PM Support –** RO. Indicates the level of active state power management supported in Intel® 6321ESB I/O Controller Hub LAN core. Defined encodings are: 00b Reserved 01b L0s Entry Supported 10b Reserved 11b L0s and L1 Supported This field is loaded from the EEPROM PCI Express init configuration 3 Word 1Ah.Default to 11b
9:4	**Max Link Width** – RO. Indicates the max link width. Intel® 6321ESB I/O Controller Hub LAN controller can support by 1 and by 4-link width. The field is loaded from the EEPROM PCI Express init configuration 3 Word 1Ah with a default value of 4 lanes. Default to 00100b.
3:0	**Max Link Speed** – RO. Indicates a max link speed of 2.5 Gbps. Default to 0001b

25.5.40 PCI Express_LINK_CONT – PCI Express* Link Control Register (Bn:F5)

Offset Address: F0–F1h
Default Value: 0000h
Attribute: R/W
Size: 16 bits

Bit	Description
15:8	Reserved.
7	**Extended Synch** – RW. This bit forces extended Tx of FTS ordered set in FTS and extra TS2 at exit from L1 prior to enter L0.
6	**Common Clock Configuration** – RW. When set indicates that Intel® 6321ESB I/O Controller Hub and the component at the other end of the link are operating with a common reference clock. A value of 0 indicates that they operating with an asynchronous clock. This parameter affects the L0s Exit Latencies.
5	**Retrain Clock** – RO. Not applicable for endpoint devices, hardwired to 0.
4	**Link Disable** – RO. Not applicable for endpoint devices, hardwired to 0.
3	**Read Completion Boundary** – RW.
2	Reserved.
1:0	**Active State Link PM Control –** R/W. this field controls the active state PM supported on the link. Link PM functionality is determined by the lowest common denominator of all functions. Defined encodings are: 00b PM Disabled 01b L0s Entry Supported 10b Reserved 11b L0s and L1 Supported

25.5.41 PCI Express_LINK_STATUS – PCI Express* Link Status Register (Bn:F5)

Offset Address: F2–F3h
Default Value: 1011h
Attribute: R/W
Size: 16 bits

Bit	Description
15:13	Reserved.
12	**Slot Clock Configuration** – When set, it indicates it uses the physical reference clock that the platform provides on the connector. This bit must be cleared uses an independent clock. Default to be 1b.
11	**Link Training** – RO. Indicates that link training is in progress.
10	**Link Training Error** – RO. Indicates that link training error has occurred.
9:4	**Negotiated Link Width** – RO. Indicates the negotiated width of the link. 000001b = x1 000100b = x4
3:0	**Link Speed** – RO. Indicates a max link speed of 2.5 Gbps. Default to 0001b

25.6 BT Controller Configuration Registers (Bn:F7)

Table 25-12. BT PCI Configuration Register Address Map Bn:F7) (Sheet 1 of 2)

Offset	Mnemonic	Register Name	Default	Type
Mandatory PCI Configuration Registers				
00–01h	VID	Vendor Identification	8086h	RO
02–03h	DID	Device Identification	1089h	RO
04–05h	PCICMD	PCI Command	0000h	RO, RW
06–07h	PCISTS	PCI Status	0010h	RO, R/WC
08h	RID	Revision Identification	See register description.	RO
09h	PI	Program Interface	02h	RO
0Ah	SCC	Sub Class Code	07h	RO
0Bh	BCC	Base Class Code	0C	RO
0Ch	CLS	Cache Line Size	See register description.	R/W
0Dh	PMLT	Primary Master Latency Timer	00h	R/W
0Eh	HEADTYP	Header Type	00h	RO
		BAR registers for 64-bit addressing modes		
10–13h	BT_MEM_BASE_LOW	BT Mem–Mapped Low Base Address	00000002h	R/W, RO
14–17h	BT_MEM_BASE_HIGH	BT Mem–Mapped Base Address	00000000h	R/W, RO
18–1Bh	BT_IO_BASE	BT I/O–Mapped Base Address	00000001h	R/W, RO
		BAR registers for 32-bit addressing modes		
10–13h	BT_MEM_BASE	BT Mem–Mapped Base Address	00000000h	R/W, RO
14–17h	BT_IO_BASE	BT I/O–Mapped Base Address	00000001h	R/W, RO
2C–2Dh	SVID	Subsystem Vendor Identification	8086h	RO

Table 25-12. BT PCI Configuration Register Address Map Bn:F7) (Sheet 2 of 2)

Offset	Mnemonic	Register Name	Default	Type
2E–2Fh	SID	Subsystem Identification	0000h	RO
34h	CAP_PTR	Capabilities Pointer	C8h	RO
3Ch	INT_LN	Interrupt Line	00h	R/W
3Dh	INT_PN	Interrupt Pin	03h	RO
3Eh	MIN_GNT	Minimum Grant	00h	RO
3Fh	MAX_LAT	Maximum Latency	00h	RO
PCI Power Management Registers				
C8h	CAP_ID	Capability ID	01h	RO
C9h	NXT_PTR	Next Item Pointer	D0h	RO
CA–CBh	PM_CAP	Power Management Capabilities	See bit description	RO
CC–CDh	PMCSR	Power Management Control/Status	0000h	R/W, RO, R/WC
CF	PCIDATA	PCI Power Management Data	00h	RO
Message Signaled Interrupt Configuration Registers				
D0h	MSI_CAP_ID	MSI Capability ID	05h	RO
D1h	MSI_NXT_PTR	MSI t Next Item Pointer	E0h	RO
D2-D3	MSI_MCR	MSI Control Register	0080	R/W
D4-D7h	MSI_MAR_LOW	MSI Message Low Address	00000000h	R/W
D8-DB	MSI_MAR_HIGH	MSI Message High Address	00000000h	R/W
DC-DD	MSI_MDR	Message Data Register	0000	R/W
PCI Express configuration registers				
E0h	PCI Express_CAP_ID	PCI Express Capability Identification Register	10h	RO
E1h	PCI Express_NXT_PTR	PCI Express Next Item Pointer	00h	RO
E2-E3	PCI Express_CAP	PCI Express Capability	0011	RO
E4-E7h	PCI Express_DEV_CAP	PCI Express Device Capability	00000CC1h	RO
E8-E9	PCI Express_DEV_CONT	PCI Express Device Control	2810h	R/W
EA-EB	PCI Express_DEV_STATUS	PCI Express Device Status	0000h	RO
EC-EF	PCI Express_LINK_CAP	PCI Express Link Capability	See bit description	RO
F0-F1	PCI Express_LINK_CONT	PCI Express Link Control	0000h	R/W
F2-F3	PCI Express_LINK_STATUS	PCI Express Link Status	1011h	RO

25.6.1 VID – Vendor Identification Register (Bn:F0/F1)

Offset Address: 00–01h
Default Value: 8086h
Attribute: RO
Size: 16 bits

Bit	Description
15:0	**Vendor ID** – RO. This is a 16-bit value assigned to Intel.

25.6.2 DID – Device Identification Register (Bn:F7)

Offset Address: 02–03h
Default Value: 1089h
Attribute: RO
Size: 16 bits

Bit	Description
15:0	**Device ID –** RO. This is a 16-bit value assigned to the Intel® 6321ESB I/O Controller Hub integrated BT Controller. If Word 0Ah bit 0 is set in the EEPROM, the Device ID is loaded from the EEPROM, Word 112h/52h after the hardware reset. If not set, the default value is 1089h.

25.6.3 PCICMD – PCI Command Register (Bn:F7)

Offset Address: 04–05h
Default Value: 0000h
Attribute: RO, R/W
Size: 16 bits

Bit	Description
15:11	Reserved
10	**Interrupt Disable** – R/W. 0 = Enable. 1 = Disables BT Controller to assert its INTA signal. The Interrupt Disable register bit is a read-write bit that controls the ability of a PCI Express device to generate a legacy interrupt message. When set, devices are prevented from generating legacy interrupt messages.
9	Fast Back to Back Enable (FBE) – RO. Hardwired to 0. The integrated BT Controller will not run fast back-to-back PCI cycles.
8	**SERR# Enable (SERR_EN) –** R/W. 0 = Disable. 1 = Enable. Allow SERR# to be asserted.
7	Wait Cycle Control (WCC) – RO. Hardwired to 0. Not implemented.
6	**Parity Error Response (PER) –** R/W. 0 = The BT Controller will ignore PCI parity errors. 1 = The integrated BT Controller will take normal action when a PCI parity error is detected and will enable generation of parity on ESI.
5	**Palette Snoop Enable (PSE) –** RO. Hardwired to 0. Not Implemented.
4	Memory Write and Invalidate Enable (MWIE) – RO. Hardwired to 0. Not Implemented.
3	**Special Cycle Monitoring (SCM) –** RO. Hardwired to 0. The BT Controller ignores special cycles.
2	**Bus Master Enable (BME)** – R/W. 0 = Disable. 1 = Enable. The Intel® 6321ESB I/O Controller Hub's integrated BT Controller may function as a PCI bus master.
1	**Memory Space Enable (MSE) –** R/W. 0 = Disable. 1 = Enable. The Intel® 6321ESB I/O Controller Hub's integrated BT Controller will respond to the memory space accesses.
0	**I/O Space Enable (IOSE) –** R/W. 0 = Disable. 1 = Enable. The Intel® 6321ESB I/O Controller Hub's integrated BT Controller will respond to the I/O space accesses.

25.6.4 PCISTS – PCI Status Register (Bn:F7)

Offset Address: 06–07h
Default Value: 0010h
Attribute: RO, R/WC
Size: 16 bits

Note: For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 to the bit has no effect.

Bit	Description
15	**Detected Parity Error (DPE)** – R/WC. 0 = Parity error Not detected. 1 = The Intel® 6321ESB I/O Controller Hub's integrated BT Controller has detected a parity error on the PCI bus (will be set even if Parity Error Response is disabled in the PCI Command register).
14	**Signaled System Error (SSE)** – R/WC. 0 = Integrated BT Controller has **not** asserted SERR# 1 = The Intel® 6321ESB I/O Controller Hub's integrated BT Controller has asserted SERR#. SERR# can be routed to cause NMI, SMI#, or interrupt.
13	**Master Abort Status (RMA) –** R/WC. 0 = Master Abort not generated 1 = The Intel® 6321ESB I/O Controller Hub's integrated BT Controller (as a PCI master) has generated a master abort.
12	**Received Target Abort (RTA) –** R/WC. 0 = Target abort Not received. 1 = The Intel® 6321ESB I/O Controller Hub's integrated BT Controller (as a PCI master) has received a target abort.
11	**Signaled Target Abort (STA) –** R/WC. 0 = Target abort Not signaled. 1 = The Intel® 6321ESB I/O Controller Hub's integrated BT Controller (as a PCI master) has signaled a target abort.
10:9	DEVSEL Timing – RO. Hardwired to 0.
8	**Data Parity Error Detected (DPED) –** R/WC. 0 = Parity error Not detected (conditions below are not met). 1 = All of the following three conditions have been met: 1. The BT Controller is acting as bus master 2. The BT Controller has asserted PERR# (for reads) or detected PERR# asserted (for writes) 3. The Parity Error Response bit in the BT Controller's PCI Command Register is set.
7	Fast Back to Back Capable (FB2BC) – RO. Hardwired to 0. The device does not accept fast back-to-back transactions.
6	Reserved.
5	**66 MHz Capable (66MHZ_CAP) –** RO. Hardwired to 0. Not implemented.
4	**Capabilities List (CAP_LIST) –** RO. Indicates that a device implements Extended Capabilities. 0 = The EEPROM indicates that the integrated BT Controller does not support extended capabilities. 1 = The EEPROM indicates that the integrated BT Controller supports PCI Power Management, message signaled interrupts, and the PCI express extensions.
3	**Interrupt Status (INTS) –** RO. This bit indicates that an interrupt is pending. It is independent from the state of the Interrupt Enable bit in the command register.
2:0	Reserved

25.6.5 RID – Revision Identification Register (Bn:F7)

Offset Address: 08h Attribute: RO
Default Value: See bit description Size: 8 bits

Bit	Description
7:0	**Revision ID (RID)** – RO. The default revision ID of this device is 00h. The value of the rev ID is a logic OR between the default value and the value in the EEPROM word 1Eh. Refer to Table 2-33 or the *Intel® 6321ESB I/O Controller Hub EDS Specification Update* for the value of the Revision ID Register.

25.6.6 PI – Programming Interface Register (Bn:F7)

Offset Address: 09h Attribute: RO
Default Value: 02h Size: 8 bits

Bit	Description
7:0	**Programming Interface(PI)** – RO. This field is loaded from EEPROM, word 57h/117h.

25.6.7 SCC – Sub Class Code Register (Bn:F7)

Offset Address: 0Ah Attribute: RO
Default Value: 07h Size: 8 bits

Bit	Description
7:0	**Sub Class Code (SCC)** – RO. This 8-bit value specifies the sub class of the device as an BT controller. This field is loaded from EEPROM, word 57h/117h.

25.6.8 BCC – Base-Class Code Register (Bn:F7)

Offset Address: 0Bh Attribute: RO
Default Value: 0Ch Size: 8 bits

Bit	Description
7:0	**Base Class Code (BCC)** – RO. This 8-bit value specifies the base class of the device as a mass storage controller. This field is loaded from EEPROM, word 58/118h.

25.6.9 CLS – Cache Line Size Register (Bn:F7)

Offset Address: 0Ch Attribute: R/W
Default Value: See register desc. Size: 8 bits

Bit	Description
7:0	Cache Line Size(CLS) – R/W. Implement for legacy compatibility purposes but has no impact on any PCI Express device functionality. Loaded from EEPROM 1Ah.

25.6.10 PMLT – Primary Master Latency Timer Register (Bn:F7)

Offset Address: 0Dh Attribute: R/W
Default Value: 00h Size: 8 bits

Bit	Description
7:0	Not used. Hardwired to zero

25.6.11 HEADTYP – Header Type Register (Bn:F7)

Offset Address: 0Eh
Default Value: 00h, 80h
Attribute: RO
Size: 8 bits

Bit	Description
7	**Multi-Function Device (MFD) –** RO. Hardwired to 0 to indicate a single function device, that is, If only a single LAN function is active. 1 for multiple function
6:0	**Header Type (HTYPE) –** RO. This 7-bit field identifies the header layout of the configuration space as an Ethernet controller.

25.6.12 Base Address Registers (Bn:F7)

64-bit Addressing Mode

25.6.12.1 BT_MEM_BASE_LOW – BT Memory-Mapped Base Address Low Register (Bn:F7)

Offset Address: 10-13h
Default Value: 00000002h
Attribute: R/W, RO
Size: 32 bits

Note: The Intel® 6321ESB I/O Controller Hub's integrated BT Controller requires one BAR for memory mapping. Software determines which BAR (memory or I/O) is used to access the BT Controller's CSR registers.

Bit	Description
31:12	**Base Address (MEM_ADDR) –** R/W. This field contains the upper 20 bits of the base address provides 4 KB of memory-Mapped space for the IPMI/KCS function.
11:4	Reserved
3	**Prefetchable (MEM_PF)** – RO. Hardwired to 0 to indicate that this is not a pre-fetchable memory-Mapped address range.
2:1	**Type (MEM_TYPE)** – RO. Hardwired to 01b to indicate the memory-Mapped address range may be located anywhere in 64-bit address space.
0	**Memory-Space Indicator (MEM_SPACE)** – RO. Hardwired to 0 to indicate that this base address maps to memory space.

25.6.12.2 BT_MEM_BASE_HIGH – BT Memory-Mapped Base Address High Register (Bn:F7)

Offset Address: 14–17h
Default Value: 00000000h
Attribute: R/W, RO
Size: 32 bits

Note: The Intel® 6321ESB I/O Controller Hub's integrated BT Controller requires one BAR for memory mapping. Software determines which BAR (memory or I/O) is used to access the BT Controller's CSR registers.

Bit	Description
31:0	**Base Address (MEM_ADDR) –** R/W. This field contains the upper 32 bits of the base address provides 4 KB of memory-Mapped space for the BT function.

25.6.12.3 BT_IO_BASE – BT I/O-Mapped Base Address Register (Bn:F7)

Offset Address: 18–1Bh Attribute: R/W, RO
Default Value: 00000001h Size: 32 bits

Note: The Intel® 6321ESB I/O Controller Hub's integrated BT Controller requires one BAR for memory mapping. Software determines which BAR (memory or I/O) is used to access the BT Controller's CSR registers.

Bit	Description
31:3	**Base Address (IO_ADDR)** – R/W. This field provides 4 bytes of I/O-Mapped address space for the BT function.
2:1	Reserved
0	**I/O Space Indicator (IO_SPACE) –** RO. Hardwired to 1 to indicate that this base address maps to I/O space.

32-bit Addressing Mode

25.6.12.4 BT_MEM_BASE – BT Memory-Mapped Base Address Register (Bn:F7)

Offset Address: 10-13h Attribute: R/W, RO
Default Value: 00000000h Size: 32 bits

Note: The Intel® 6321ESB I/O Controller Hub's integrated BT Controller requires one BAR for memory mapping. Software determines which BAR (memory or I/O) is used to access the BT Controller's CSR registers.

Bit	Description
31:12	**Base Address (MEM_ADDR) –** R/W. This field contains the upper 20 bits of the base address provides 4 KB of memory-Mapped space for the BT function.
11:4	Reserved
3	**Prefetchable (MEM_PF)** – RO. Hardwired to 0 to indicate that this is not a pre-fetchable memory-Mapped address range.
2:1	**Type (MEM_TYPE)** – RO. Hardwired to 00b to indicate the memory-Mapped address range may be located anywhere in 32-bit address space.
0	**Memory-Space Indicator (MEM_SPACE)** – RO. Hardwired to 0 to indicate that this base address maps to memory space.

25.6.12.4.1 BT_IO_BASE – BT I/O-Mapped Base Address Register (Bn:F7)

Offset Address: 14-17h Attribute: R/W, RO
Default Value: 00000001h Size: 32 bits

Note: The Intel® 6321ESB I/O Controller Hub's integrated BT Controller requires one BAR for memory mapping. Software determines which BAR (memory or I/O) is used to access the BT Controller's CSR registers.

Bit	Description
31:2	**Base Address (IO_ADDR)** – R/W. This field provides 4 bytes of I/O-Mapped address space for the BT function.
1	Reserved
0	**I/O Space Indicator (IO_SPACE)** – RO. Hardwired to 1 to indicate that this base address maps to I/O space.

25.6.13 SVID – Subsystem Vendor Identification(Bn:F7)

Offset Address: 2C–2D
Default Value: 8086h
Attribute: RO
Size: 16 bits

Bit	Description
15:0	**Subsystem Vendor ID (SVID)** – RO. This value may be loaded automatically from the EEPROM address 0Ch upon power up or reset if the EEPROM is present (and properly programmed) and if Word 0Ah bit 1 is set. A value of 0x8086 is default for this field upon power up if the EEPROM does not respond or is not programmed.

25.6.14 SID – Subsystem Identification (Bn:F7)

Offset Address: 2E–2Fh
Default Value: 0000h
Attribute: RO
Size: 16 bits

Bit	Description
15:0	**Subsystem ID (SID)** – RO. This value may be loaded automatically from the EEPROM address 115h/55h upon power up with a default value of 0x0000 if the EEPROM is present (and properly programmed) and if Word 0Ah bit 1 is set.

25.6.15 CAP_PTR – Capabilities Pointer (Bn:F7)

Offset Address: 34h
Default Value: C8h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Capabilities Pointer (CAP_PTR)** – RO. Hardwired to C8h to indicate the offset within configuration space for the location of the Power Management registers.

25.6.16 INT_LN – Interrupt Line Register (Bn:F7)

Offset Address: 3Ch
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	**Interrupt Line (INT_LN) –** R/W. This field identifies the system interrupt line to which the BT Controller's PCI interrupt request pin (as defined in the Interrupt Pin Register) is routed.

25.6.17 INT_PN – Interrupt Pin Register (Bn:F7)

Offset Address: 3Dh
Default Value: 03h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Interrupt Pin (INT_PN)** – RO. BT Function - A value of 0x1 / 0x2 / 0x3 / 0x4 indicates that this function implements legacy interrupt on INTA / INTB / INTC / INTD respectively. Loaded from EEPROM word 0x6B/0x12B.

25.6.18 MIN_GNT – Minimum Grant Register (Bn:F7)

Offset Address: 3Eh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Minimum Grant (MIN_GNT)** – RO. Not used, hardwired to 00h.

25.6.19 MAX_LAT – Maximum Latency Register (Bn:F7)

Offset Address: 3Fh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Maximum Latency (MAX_LAT)** – RO. Not used, hardwired to 00h.

25.6.20 CAP_ID – Capability Identification Register (Bn:F7)

Offset Address: C8h
Default Value: 01h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Capability ID (CAP_ID)** – RO. Hardwired to 01h to indicate that the Intel® 6321ESB I/O Controller Hub's integrated BT Controller supports PCI Power Management.

25.6.21 NXT_PTR – Next Item Pointer (Bn:F7)

Offset Address: C9h
Default Value: D0h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Next Item Pointer (NXT_PTR)** – RO. Hardwired to D0h to indicate that power management is the last item in the capabilities list.

25.6.22 PM_CAP – Power Management Capabilities (Bn:F7)

Offset Address: CA–CBh
Default Value: See bit description
Attribute: RO
Size: 16 bits

Bit	Description
15:11	**PME Support (PME_SUP)** – RO. This 5-bit field indicates the power states in which the BT Controller may assert PME#. The default value depends on EEPROM word 0Ah. 00000b = No PME at all states. 01001b = PME at D0 and $D3_{hot}$ 11001b = PME at D0, $D3_{hot}$ and $D3_{cold}$
10:9	**Hardwired to '0'.**
8:6	**Auxiliary Current (AUX_CUR)** – RO. Hardwired to 000b to indicate that the BT Controller implements the Data registers. The auxiliary power consumption is the same as the current consumption reported in the D3 state in the Data register.
5	**Device Specific Initialization (DSI)** – RO. Hardwired to 1 to indicate that special initialization of this function is required (beyond the standard PCI configuration header) before the generic class device driver is able to use it. DSI is required for the BT Controller after D3-to-D0 reset.

Bit	Description
4	Reserved
3	**PME Clock (PME_CLK)** – RO. Hardwired to 0 to indicate that the BT Controller does not require a clock to generate a power management event.
2:0	**Version (VER) –** RO. Hardwired to 010b to indicate that the BT Controller complies with of the *PCI Power Management Specification, Revision 1.1.*

25.6.23 PMCSR – Power Management Control/Status Register (Bn:F7)

Offset Address: CC–CDh
Default Value: 0000h
Attribute: RO, R/W, R/WC
Size: 16 bits

Bit	Description
15	PME Status **(PME_STAT)** – R/WC. 0 = Software clears this bit by writing a 1 to it. This also deasserts the PME# signal and clears the PME status bit in the Power Management Driver Register. When the PME# signal is enabled, the PME# signal reflects the state of the PME status bit. 1 = Set upon occurrence of a wakeup event, independent of the state of the PME enable bit.
14:13	**Data Scale (DSCALE) –** RO. This field indicates the data register scaling factor. It equals 10b for all supported registers: 0,3,4,7 and 8, as selected by the “Data Select” field.
12:9	**Data Select (DSEL) –** R/W. This field is used to select which data is reported through the Data register and Data Scale field.
8	**PME Enable (PME_EN)** – R/W. This bit enables the Intel® 6321ESB I/O Controller Hub’s integrated BT Controller to assert PME#. 0 = The device will not assert PME#. 1 = Enable PME# assertion when PME Status is set.
7:2	Reserved
1:0	**Power State (PWR_ST) –** R/W. This 2-bit field is used to determine the current power state of the integrated BT Controller, and to put it into a new power state. The definition of the field values is as follows: 00 = D0 01/10 = Reserved 11 = D3

25.6.24 PCIDATA – PCI Power Management Data Register (Bn:F7)

Offset Address: CFh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Power Management Data (PWR_MGT) –** RO. State dependent power consumption and heat dissipation data.

This optional register is used to report power consumption and heat dissipation. Reported register is controlled by the Data_Select field in the PMCSR, and the power scale is reported in the Data_Scale field in the PMCSR. The data of this field is loaded from the EEPROM if PM is enabled in the EEPROM or with a default value of 0x00 otherwise. The values for Intel® 6321ESB I/O Controller Hub UHCI Redirection Controller functions is shown in Table 25-13.

Table 25-13. Data Register Structure

Function	D0 (consume/ dissipate)	D3 (consume/ dissipate)	Common	Data_Scale
Data_Select	(0x0 / 0x4)	(0x3 / 0x7)	(0x8)	
BT Function	EEP addr 119/59h	EEP addr 11A/5Ah	EEP addr 22h	10b

25.6.25 MSI_CAP_ID – Capability Identification Register (Bn:F7)

Offset Address: D0h
Default Value: 05h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Capability ID (CAP_ID)** – RO. Hardwired to 05h to indicate that the linked list item as being the Message Signaled Interrupt registers.

25.6.26 MSI_NXT_PTR – Next Item Pointer (Bn:F7)

Offset Address: D1h
Default Value: E0h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Next Item Pointer (NXT_PTR)** – RO. Hardwired to E0h to indicate that PCI Express capability is the next item in the capability list.

25.6.27 MSI_MCR – Message Control Register (Bn:F7)

Offset Address: D2–D3h
Default Value: 0080
Attribute: RO
Size: 16 bits

Bit	Description
15:11	Reserved.
7	**64 Support (64_SUP)** – RO. Hardwired to 1 to indicate that the BT Controller is capable of generating 64 bit message addresses.
6:4	**Multiple Message Enable(MM_ENABLE)** – RO. Hardwired to 000b to indicate that the BT Controller supports single message per function.
3:1	**Multiple Message Capable(MM_CAP)** – RO. Hardwired to 000b to indicate that the BT Controller capable of single requested message per function.
0	**MSI ENABLE(MSI_ENABLE) –** R/W. If 1, the BT Controller will generate MSI for interrupt assertion instead of INTx signaling.

25.6.28 MSI_MAR_LOW – Message Address Low Register (Bn:F7)

Offset Address: D4–D7h
Default Value: 00000000h
Attribute: RO, R/W, R/WC
Size: 32 bits

Bit	Description
7:2	**Message Address Low(MSG_ADDR_LOW) –** R/W. Written by the system to indicate the lower 32 bits of the address to use for the MSI memory write transaction. The lower two bits will always return 0 regardless of the write operation.

25.6.29 MSI_MAR_HIGH – Message Address High Register (Bn:F7)

Offset Address: D8–DBh
Default Value: 0000h
Attribute: RO, R/W, R/WC
Size: 16 bits

Bit	Description
31:0	**Message Address High(MSG_ADDR_HIGH) –** R/W. This field contains the upper 32 bits of the address to use for the MSI memory write transaction.

25.6.30 MSI_MDR – Message Data Register (Bn:F7)

Offset Address: DC–DDh
Default Value: 0000h
Attribute: R/W
Size: 16 bits

Bit	Description
15:0	**Message Data(MSG_DATA) –** R/W. Written by the system to indicate the lower 16 bits of the data written in the MSI memory write DWORD transaction. The upper 16 bits of the transaction are written as 0

25.6.31 PCI Express_CAP_ID – PCI Express* Capability Identification Register (Bn:F7)

Offset Address: E0h
Default Value: 10h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Capability ID (CAP_ID)** – RO. Hardwired to 10h to indicate that the linked list item as being the PCI Express* Capability Registers.

25.6.32 PCI Express_NXT_PTR – PCI Express* Next Item Pointer (Bn:F7)

Offset Address: E1h
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Next Item Pointer (NXT_PTR)** – RO. Hardwired to 00h to indicate that it is the last item in the capability linked list.

25.6.33 PCI Express_CAP – PCI Express* Capability Register (Bn:F7)

Offset Address: E2–E3h
Default Value: 0011
Attribute: RO
Size: 16 bits

Bit	Description
15:14	Reserved.
13:9	**Interrupt Message Number (INT_MSG_NUM)** – RO. Multiple MSI per function is not supported. Hardwired to 00000b
8	**Slot Implemented** – RO. Slot option not implemented hardwired to 0.
7:4	**Device/Port Type** – RO. Indicates the type of PCI Express* functions. The value of for IDE Redirection Function is loaded from the EEPROM word 19h bit 13.
3:0	**Capability version(CAP_VERSION) –** RO. Indicates the PCI Express capability structure version number 0001b.

25.6.34 PCI Express_DEV_CAP – PCI Express* Device Capability Register (Bn:F7)

Offset Address: E4–E7h
Default Value: 00000CC1h
Attribute: RO, R/W, R/WC
Size: 32 bits

Bit	Description
31:28	Reserved.
27:26	**Slot Power Limit Scale** – RO. Used in upstream port only. Hardwired to 00b.
25:18	**Slot Power Limit Value** – RO. Used in upstream port only. Hardwired to 00b
17:15	Reserved.
14	**Power Indicator Present** – RO. Hardwired to 0b
13	**Attention Indicator Present** – RO. Hardwired to 0b
12	**Attention Button Present** – RO. Hardwired to 0b
11:9	**Endpoint L1 Acceptable Latency** – RO. This field indicates the acceptable latency that Intel® 6321ESB I/O Controller Hub LAN core can withstand due to the transition from L1 state to the L0 state. All functions share the same value loaded from the EEPROM PCI Express* init configuration 1 Word 18h
8:6	**Endpoint L0s Acceptable Latency** – RO. This field indicates the acceptable latency that Intel® 6321ESB I/O Controller Hub LAN core can withstand due to the transition from L0s state to the L0 state. All functions share the same value loaded from the EEPROM PCI Express init configuration 1 Word 18h.
5	**Extended Tag Field Supported –** RO. Indicates the PCI Express capability structure version number 0001b.
4:3	**Phantom Function Supported** – RO. Indicates the type of PCI Express functions. Hardwired to 0001b
2:0	**Max Payload Size Supported** – RO. Indicates the type of PCI Express functions. Hardwired to 0001b

25.6.35 PCI Express_DEV_CONT – PCI Express* Device Control Register (Bn:F7)

Offset Address: E8–E9h
Default Value: 2810h
Attribute: RO, R/W
Size: 16 bits

Bit	Description
15	Reserved.
14:12	**Max Read Request Size** - this field sets maximum read request size for the Device as a requester. The default value is 010b (512B) for the LAN devices.
11	**Enable No Snoop** – R/W. Snoop is gated by NONSNOOP bits in the GCR register in the CSR space. Default is 1b
10	**Auxiliary Power PM Enable** - when set enables the device to draw AUX power independent of PME AUX power. Intel® 6321ESB I/O Controller Hub LAN core is a multi function device, therefore allowed to draw AUX power if at least one of the functions has this bit sets
9	**Phantom Function Enable** – RW. Hardwired to 0b
8	**Extended Tag Field Enable** – RW. Hardwired to 0b
7:5	**Max Payload Size** – RW. Slot option not implemented hardwired to 0.
4	**Enable Relaxed Ordering** – If this bit is set, the device is permitted to set the Relaxed Ordering bit in the attribute field of write transactions that do not need strong ordering. Default to 1b
3	**Unsupported Request Reporting Enable** – RW. Enable error report.
2	**Fatal Error Reporting Enable** – RW. Enable error report.
1	**Non-Fatal Error Reporting Enable** – RW. Enable error report.
0	**Correctable Error Reporting Enable** – RW. Enable error report.

25.6.36 PCI Express_DEV_STATUS – PCI Express* Device Status Register (Bn:F7)

Offset Address: EA–EBh
Default Value: 0000h
Attribute: RO, R/W, R/WC
Size: 16 bits

Bit	Description
15:6	Reserved.
5	**Transaction Pending** – RO. Slot option not implemented hardwired to 0.
4	**Aux Power Detected**– RO. If this bit is set, the device is permitted to set the Relaxed Ordering bit in the attribute field of write transactions that do not need strong ordering. Default to 1b
3	**Unsupported Request Detected** – R/WC. Enable error report.
2	**Fatal Error Detected** – R/WC. Enable error report.
1	**Non-Fatal Error Detected** – R/WC. Enable error report.
0	**Correctable Error Detected** – R/WC. Enable error report.

25.6.37 PCI Express_LINK_CAP – PCI Express* Link Capability Register (Bn:F7)

Offset Address: EC–EFh
Default Value: See description
Attribute: RO, R/W
Size: 16 bits

Bit	Description
31:24	**Port Number** – RO. The PCI Express* port number for the given PCI Express Link. Field is set in the Link training phase. Default to 0x0.
23:18	Reserved.
17:15	**L1 Exit Latency**- Indicates the exit latency from L1 to L0 state. This field is loaded from the EEPROM PCI Express init configuration 1 Word 18h. Default to 110b (32-64us).
14:12	**L0s Exit Latency**- Indicates the exit latency from L0s to L0 state. This field is loaded from the EEPROM PCI Express init configuration 1 Word 18h (two values for Common PCI Express clock or Separate PCI Express clock). Default to 001b (64-128ns).
11:10	**Active State Link PM Support –** RO. Indicates the level of active state power management supported in Intel® 6321ESB I/O Controller Hub LAN core. Defined encodings are: 00b Reserved 01b L0s Entry Supported 10b Reserved 11b L0s and L1 Supported This field is loaded from the EEPROM PCI Express init configuration 3 Word 1Ah.Default to 11b
9:4	**Max Link Width** – RO. Indicates the max link width. Intel® 6321ESB I/O Controller Hub LAN controller can support by 1 and by 4-link width. The field is loaded from the EEPROM PCI Express init configuration 3 Word 1Ah with a default value of 4 lanes. Default to 00100b.
3:0	**Max Link Speed** – RO. Indicates a max link speed of 2.5 Gbps. Default to 0001b

25.6.38 PCI Express_LINK_CONT – PCI Express* Link Control Register (Bn:F7)

Offset Address: F0–F1h
Default Value: 0000h
Attribute: R/W
Size: 16 bits

Bit	Description
15:8	Reserved.
7	**Extended Synch** – RW. This bit forces extended Tx of FTS ordered set in FTS and extra TS2 at exit from L1 prior to enter L0.
6	**Common Clock Configuration** – RW. When set indicates that Intel® 6321ESB I/O Controller Hub and the component at the other end of the link are operating with a common reference clock. A value of 0 indicates that they operating with an asynchronous clock. This parameter affects the L0s Exit Latencies.
5	**Retrain Clock** – RO. Not applicable for endpoint devices, hardwired to 0.
4	**Link Disable** – RO. Not applicable for endpoint devices, hardwired to 0.
3	**Read Completion Boundary** – RW.
2	Reserved.
1:0	**Active State Link PM Control –** R/W. this field controls the active state PM supported on the link. Link PM functionality is determined by the lowest common denominator of all functions. Defined encodings are: 00b PM Disabled 01b L0s Entry Supported 10b Reserved 11b L0s and L1 Supported

25.6.39 PCI Express_LINK_STATUS – PCI Express* Link Status Register (Bn:F7)

Offset Address: F2–F3h
Default Value: 1011h
Attribute: R/W
Size: 16 bits

Bit	Description
15:13	Reserved.
12	**Slot Clock Configuration** – When set, it indicates it uses the physical reference clock that the platform provides on the connector. This bit must be cleared uses an independent clock. Default to be 1b.
11	**Link Training** – RO. Indicates that link training is in progress.
10	**Link Training Error** – RO. Indicates that link training error has occurred.
9:4	**Negotiated Link Width** – RO. Indicates the negotiated width of the link. 000001b = x1 000100b = x4
3:0	**Link Speed** – RO. Indicates a max link speed of 2.5 Gbps. Default to 0001b

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26 High-Precision Event Timer Registers

The timer registers are memory-mapped in a non-indexed scheme. This allows the processor to directly access each register without having to use an index register. The timer register space is 1024 bytes. The registers are generally aligned on 64-bit boundaries to simplify implementation with IA64 processors. There are four possible memory address ranges beginning at 1) FED0_0000h, 2) FED0_1000h, 3) FED0_2000h., 4) FED0_3000h. The choice of address range will be selected by configuration bits in High Precision Timer Configuration Register (offset 3404h in the memory mapped Chipset Configuration Registers).

Behavioral Rules:

1. Software must not attempt to read or write across register boundaries. For example, a 32-bit access should be to offset x0h, x4h, x8h, or xCh. 32-bit accesses should not be to 01h, 02h, 03h, 05h, 06h, 07h, 09h, 0Ah, 0Bh, 0Dh, 0Eh, or 0Fh. Any accesses to these offsets will result in an unexpected behavior, and may result in a master abort. However, these accesses should not result in system hangs. 64-bit accesses can only be to x0h and must not cross 64-bit boundaries.
2. Software should not write to read-only registers.
3. Software should not expect any particular or consistent value when reading reserved registers or bits.

26.1 Memory Mapped Registers

Table 26-1. Memory-Mapped Registers (Sheet 1 of 2)

Offset	Mnemonic	Register	Default	Type
000–007h	GCAP_ID	General Capabilities and Identification	0429B17F8086A201h	RO
008–00Fh	–	Reserved	–	–
010–017h	GEN_CONF	General Configuration	0000h	R/W
018–01Fh	–	Reserved	–	–
020–027h	GINTR_STA	General Interrupt Status	0000h	R/WC
028–0EFh	–	Reserved	–	–
0F0–0F7h	MAIN_CNT	Main Counter Value	N/A	R/W
0F8–0FFh	–	Reserved	–	–
100–107h	TIM1_CONF	Timer 0 Configuration and Capabilities	N/A	R/W
108–10Fh	TIM1_COMP	Timer 0 Comparator Value	N/A	R/W
110–11Fh	–	Reserved	–	–
120–127h	TIM2_CONF	Timer 1 Configuration and Capabilities	N/A	R/W
128–12Fh	TIM2_COMP	Timer 1 Comparator Value	N/A	R/W
130–13Fh	–	Reserved	–	–
140–147h	TIM3_CONF	Timer 2 Configuration and Capabilities	N/A	R/W

Table 26-1. Memory-Mapped Registers (Sheet 2 of 2)

Offset	Mnemonic	Register	Default	Type
148–14Fh	TIM3_COMP	Timer 2 Comparator Value	N/A	R/W
150–15Fh	–	Reserved	–	–
160–3FFh	–	Reserved	–	–

Notes:
1. Reads to reserved registers or bits will return a value of 0.
2. Software must not attempt locks to the memory-mapped I/O ranges for High-Precision Timers. If attempted, the lock is not honored, which means potential deadlock conditions may occur.

26.1.1 GCAP_ID – General Capabilities and Identification Register

Address Offset: 00h Attribute: RO
Default Value: 0429B17F8086A201h Size: 64 bits

Bit	Description
63:32	Main Counter Tick Period (COUNTER_CLK_PER_CAP) – RO. This field indicates the period at which the counter increments in femptoseconds (10^-15 seconds). This will return 0429B17F when read. This indicates a period of 69841279 fs (69.841279 ns).
31:16	Vendor ID Capability (VENDOR_ID_CAP) – RO. This is a 16-bit value assigned to Intel.
15	Legacy Replacement Rout Capable (LEG_RT_CAP) – RO. Hardwired to 1. Legacy Replacement Interrupt Rout option is supported.
14	Reserved. This bit returns 0 when read.
13	Counter Size Capability (COUNT_SIZE_CAP) – RO. Hardwired to 1. Counter is 64-bit wide.
12:8	Number of Timer Capability (NUM_TIM_CAP) – RO. This field indicates the number of timers in this block. 02h = Three timers.
7:0	Revision Identification (REV_ID) – RO. This indicates which revision of the function is implemented. Default value will be 01h.

26.1.2 GEN_CONF – General Configuration Register

Address Offset: 010h Attribute: R/W
Default Value: 0000000000000000h Size: 64 bits

Bit	Description
63:2	Reserved. These bits return 0 when read.
1	**Legacy Replacement Rout (LEG_RT_CNF)** – R/W. If the ENABLE_CNF bit and the LEG_RT_CNF bit are both set, then the interrupts will be routed as follows: • Timer 0 is routed to IRQ0 in 8259 or IRQ2 in the I/O APIC • Timer 1 is routed to IRQ8 in 8259 or IRQ8 in the I/O APIC • Timer 2-n is routed as per the routing in the timer n config registers. • If the Legacy Replacement Rout bit is set, the individual routing bits for Timers 0 and 1 (APIC) will have no impact. • If the Legacy Replacement Rout bit is not set, the individual routing bits for each of the timers are used. • This bit will default to 0. BIOS can set it to 1 to enable the legacy replacement routing, or 0 to disable the legacy replacement routing.
0	**Overall Enable (ENABLE_CNF)** – R/W. This bit must be set to enable any of the timers to generate interrupts. If this bit is 0, then the main counter will halt (will not increment) and no interrupts will be caused by any of these timers. For level-triggered interrupts, if an interrupt is pending when the ENABLE_CNF bit is changed from 1 to 0, the interrupt status indications (in the various TxX_INT_STS bits) will not be cleared. Software must write to the TxX_INT_STS bits to clear the interrupts. ***Note:*** This bit will default to 0. BIOS can set it to 1 or 0.

26.1.3 GINTR_STA – General Interrupt Status Register

Address Offset: 020h
Default Value: 0000000000000000h
Attribute: R/W, R/WC
Size: 64 bits

Bit	Description
63:3	Reserved. These bits will return 0 when read.
2	**Timer 2 Interrupt Active (T02_INT_STS)** – R/W. Same functionality as Timer 0.
1	**Timer 1 Interrupt Active (T01_INT_STS)** – R/W. Same functionality as Timer 0.
0	**Timer 0 Interrupt Active (T00_INT_STS)** – R/WC. The functionality of this bit depends on whether the edge or level-triggered mode is used for this timer. (default = 0) If set to level-triggered mode: This bit will be set by hardware if the corresponding timer interrupt is active. Once the bit is set, it can be cleared by software writing a 1 to the same bit position. Writes of 0 to this bit will have no effect. If set to edge-triggered mode: This bit should be ignored by software. Software should always write 0 to this bit. ***Note:*** Defaults to 0. In edge triggered mode, this bit will always read as 0 and writes will have no effect.

26.1.4 MAIN_CNT – Main Counter Value Register

Address Offset: 0F0h
Default Value: N/A
Attribute: R/W
Size: 64 bits

Bit	Description
63:0	**Counter Value (COUNTER_VAL[63:0])** – R/W. Reads return the current value of the counter. Writes load the new value to the counter. ***Notes:*** 1. Writes to this register should only be done while the counter is halted. 2. Reads to this register return the current value of the main counter. 3. 32-bit counters will always return 0 for the upper 32-bits of this register. 4. If 32-bit software attempts to read a 64-bit counter, it should first halt the counter. Since this delays the interrupts for all of the timers, this should be done only if the consequences are understood. It is strongly recommended that 32-bit software only operate the timer in 32-bit mode. 5. Reads to this register are monotonic. No two consecutive reads return the same value. The second of two reads always returns a larger value (unless the timer has rolled over to 0).

26.1.5 TIMn_CONF – Timer n Configuration and Capabilities Register

Address Offset: Timer 0: 100–107h, Timer 1: 120–127h, Timer 2: 140–147h
Default Value: N/A
Attribute: RO, R/W
Size: 64 bits

Note: The letter n can be 0, 1, or 2, referring to Timer 0, 1 or 2.

Bit	Description
63:56	Reserved. These bits will return 0 when read.
55:52, 43	**Timer Interrupt Rout Capability (TIMERn_INT_ROUT_CAP)** – RO. Timer 0, 1:Bits 52, 53, 54, and 55 in this field (corresponding to IRQ 20, 21, 22, and 23) have a value of 1. Writes will have no effect. Timer 2:Bits 43, 52, 53, 54, and 55 in this field (corresponding to IRQ 11, 20, 21, 22, and 23) have a value of 1. Writes will have no effect. ***Note:*** If IRQ 11 is used for HPET #2, software should ensure IRQ 11 is not shared with any other devices to guarantee the proper operation of HPET #2.
51:44, 42:14	Reserved**.** These bits return 0 when read.
13:9	**Interrupt Rout (TIMERn_INT_ROUT_CNF) –** R/W. This 5-bit field indicates the routing for the interrupt to the I/O (x) APIC. Software writes to this field to select which interrupt in the I/O (x) will be used for this timer's interrupt. If the value is not supported by this particular timer, then the value read back will not match what is written. The software must only write valid values. ***Notes:*** 1. If the Legacy Replacement Rout bit is set, then Timers 0 and 1 will have a different routing, and this bit field has no effect for those two timers. 2. Timer 0,1: Software is responsible to make sure it programs a valid value (20, 21, 22, or 23) for this field. The Intel® 6321ESB I/O Controller Hub logic does not check the validity of the value written. 3. Timer 2: Software is responsible to make sure it programs a valid value (11, 20, 21, 22, or 23) for this field. The Intel® 6321ESB I/O Controller Hub logic does not check the validity of the value written.
8	**Timer n 32-bit Mode (TIMERn_32MODE_CNF) –** R/W or RO. Software can set this bit to force a 64-bit timer to behave as a 32-bit timer. Timer 0:Bit is read/write (default to 0). 1 = 64 bit; 0 = 32 bit Timers 1, 2:Hardwired to 0. Writes have no effect (since these two timers are 32-bits).
7	Reserved**.** This bit returns 0 when read.
6	**Timer n Value Set (TIMERn_VAL_SET_CNF)** – R/W. Software uses this bit only for Timer 0 if it has been set to periodic mode. By writing this bit to a 1, the software is then allowed to directly set the timer's accumulator. Software does **not** have to write this bit back to 1 (it automatically clears). Software should not write a 1 to this bit position if the timer is set to non-periodic mode. ***Note:*** This bit will return 0 when read. Writes will only have an effect for Timer 0 if it is set to periodic mode. Writes will have no effect for Timers 1 and 2.
5	**Timer n Size (TIMERn_SIZE_CAP)** – RO. This read only field indicates the size of the timer. Timer 0:Value is 1 (64-bits). Timers 1, 2:Value is 0 (32-bits).
4	**Periodic Interrupt Capable (TIMERn_PER_INT_CAP)** – RO. If this bit is 1, the hardware supports a periodic mode for this timer's interrupt. Timer 0: Hardwired to 1 (supports the periodic interrupt). Timers 1, 2: Hardwired to 0 (does not support periodic interrupt).
3	**Timer n Type (TIMERn_TYPE_CNF)** – R/W or RO. Timer 0:Bit is read/write. 0 = Disable timer to generate periodic interrupt; 1 = Enable timer to generate a periodic interrupt. Timers 1, 2: Hardwired to 0. Writes have no affect.

Bit	Description
2	**Timer n Interrupt Enable (TIMERn_INT_ENB_CNF) –** R/W. This bit must be set to enable timer n to cause an interrupt when it times out. 1 = Enable. 0 = Disable (Default). The timer can still count and generate appropriate status bits, but will not cause an interrupt.
1	**Timer Interrupt Type (TIMERn_INT_TYPE_CNF)** – R/W. 0 =The timer interrupt is edge triggered. This means that an edge-type interrupt is generated. If another interrupt occurs, another edge will be generated. 1 =The timer interrupt is level triggered. This means that a level-triggered interrupt is generated. The interrupt will be held active until it is cleared by writing to the bit in the General Interrupt Status Register. If another interrupt occurs before the interrupt is cleared, the interrupt will remain active.
0	Reserved**.** These bits will return 0 when read.

Note: Reads or writes to unimplemented timers should not be attempted. Read from any unimplemented registers will return an undetermined value.

26.1.6 TIMn_COMP – Timer n Comparator Value Register

Address Offset: Timer 0: 108h–10Fh,
Timer 1: 128h–12Fh,
Timer 2: 148h–14Fh
Attribute: R/W
Default Value: N/A Size: 64 bit

Bit	Description
63:0	**Timer Compare Value** – R/W. Reads to this register return the current value of the comparator Timers 0, 1, or 2 are configured to non-periodic mode: Writes to this register load the value against which the main counter should be compared for this timer. • When the main counter equals the value last written to this register, the corresponding interrupt can be generated (if so enabled). • The value in this register does not change based on the interrupt being generated. Timer 0 is configured to periodic mode: • When the main counter equals the value last written to this register, the corresponding interrupt can be generated (if so enabled). • After the main counter equals the value in this register, the value in this register is increased by the value last written to the register. For example, if the value written to the register is 00000123h, then 1. An interrupt will be generated when the main counter reaches 00000123h. 2. The value in this register will then be adjusted by the hardware to 00000246h. 3. Another interrupt will be generated when the main counter reaches 00000246h 4. The value in this register will then be adjusted by the hardware to 00000369h • As each periodic interrupt occurs, the value in this register will increment. When the incremented value is greater than the maximum value possible for this register (FFFFFFFFh for a 32-bit timer or FFFFFFFFFFFFFFFFh for a 64-bit timer), the value will wrap around through 0. For example, if the current value in a 32-bit timer is FFFF0000h and the last value written to this register is 20000, then after the next interrupt the value will change to 00010000h Default value for each timer is all 1s for the bits that are implemented. For example, a 32-bit timer has a default value of 00000000FFFFFFFFh. A 64-bit timer has a default value of FFFFFFFFFFFFFFFFh.

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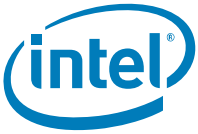

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