PCF8564A

Real time clock and calendar

Rev. 3 — 26 August 2013 Product data sheet

1. General description

The PCF8564A is a CMOS[1] real-time clock and calendar optimized for low power consumption. A programmable clock output, interrupt output and voltage low detector are also provided. All addresses and data are transferred serially via the two-line bidirectional I^2C-bus. Maximum bus speed is 400 kbit/s. The built-in word address register is incremented automatically after each written or read data byte.

2. Features and benefits

- Provides year, month, day, weekday, hours, minutes, and seconds based on a 32.768 kHz quartz crystal
- Wide clock operating voltage: 1.0 V to 5.5 V
- Low back-up current typical 250 nA at 3.0 V and 25 °C
- 400 kHz two-wire I^2C interface (1.8 V to 5.5 V)
- Low-voltage detector
- Alarm and timer functions
- Two integrated oscillator capacitors
- Programmable clock output for peripheral devices (32.768 kHz, 1.024 kHz, 32 Hz, and 1 Hz)
- Internal Power-On Reset (POR)
- I^2C slave address: read A3h, write A2h

3. Applications

- Timing devices
  - Time of the day tracking
  - Process timing
  - Alarm
- Portable instruments
- Electronic metering
- Battery powered products

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 20.

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCF8564AU	bare die	wire bond die; 9 bonding pads	PCF8564AU
PCF8564AUG	bare die	9 bumps	PCF8564AUG

4.1 Ordering options

Table 2. Ordering options

Product type number	Sales item (12NC)	Orderable part number	IC revision	Delivery form
PCF8564AU/10AB/1	935289478005	PCF8564AU/10AB/1,0	1	wafer, sawn, on FFC
PCF8564AU/5BB/1	935289319015	PCF8564AU/5BB/1,01	1	unsawn wafer
PCF8564AU/5GB/1	935289477015	PCF8564AU/5GB/1,01	1	unsawn wafer
PCF8564AU/5GC/1	935293569015	PCF8564AU/5GC/1,01	1	unsawn wafer
PCF8564AUG/12HB/1	935301011005	PCF8564AUG/12HB/1V	1	wafer, sawn, on 8 inch metal FFC; chips with soft bumps[1]

[1] Bump hardness, see Table 36.

5. Marking

Table 3. Marking codes

Type number	Marking code
PCF8564AU	PC8564A-1
PCF8564AUG	PC8564A-1

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

6. Block diagram

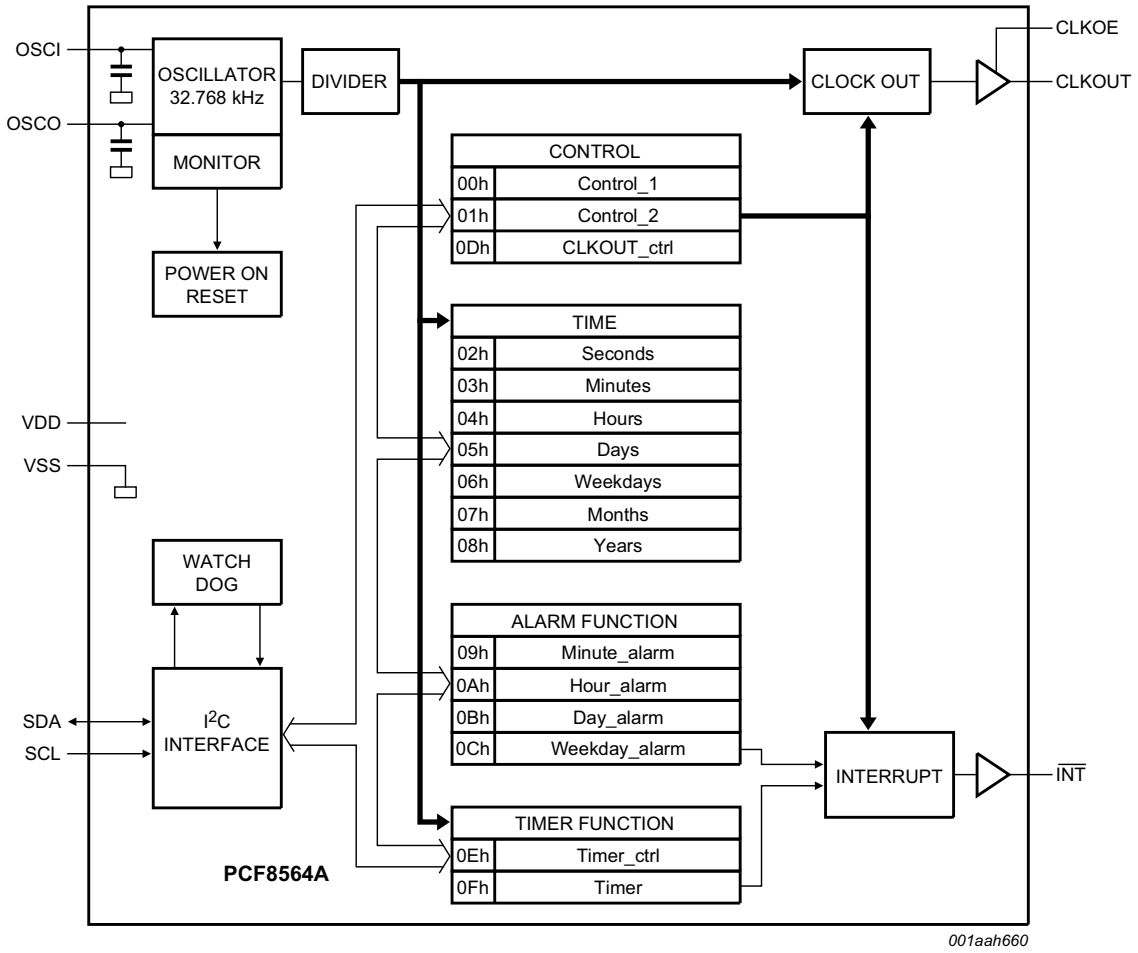


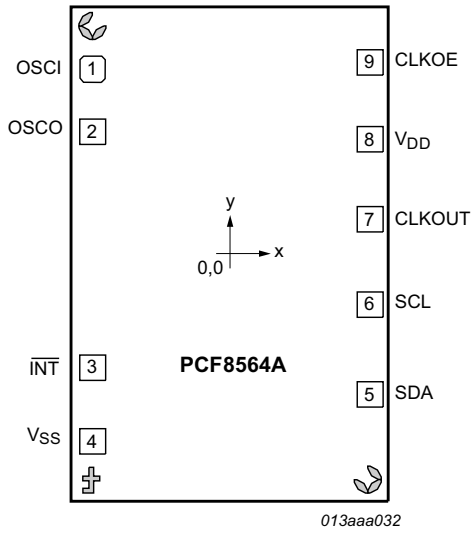
Fig 1. Block diagram of PCF8564A

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

7. Pinning information

7.1 Pinning



Viewed from active side. For mechanical details, see Figure 27 and Figure 28.

Fig 2. Pinning diagram of PCF8564A

7.2 Pin description

Table 4. Pin description

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Pin	Description
OSCI	1	oscillator input
OSCO	2	oscillator output
$\overline{INT}$	3	interrupt output, open-drain, active LOW
V_{SS}	4	ground[1]
SDA	5	serial data input and output
SCL	6	serial clock input
CLKOUT	7	clock output, push-pull
V_{DD}	8	supply voltage
CLKOE	9	CLKOUT enable input

[1] The substrate (rear side of the die) is at V_{SS} potential and must not be connected.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

8. Functional description

The PCF8564A contains sixteen 8-bit registers with an auto-incrementing address register, an on-chip 32.768 kHz oscillator with integrated capacitors, a frequency divider which provides the source clock for the RTC, a programmable clock output, a timer, a voltage low detector, and a 400 kHz I^2C-bus interface.

All sixteen registers (see Table 5) are designed as addressable 8-bit parallel registers although not all bits are implemented. The first two registers (memory address 00h and 01h) are used as control and/or status registers. The addresses 02h through 08h are used as counters for the clock function (seconds up to years counters). Address locations 09h through 0Ch contain alarm registers which define the conditions for an alarm. Address 0Dh controls the CLKOUT output frequency. 0Eh and 0Fh are the timer control and timer registers, respectively.

The seconds, minutes, hours, days, months, years, as well as the minute alarm, hour alarm, and day alarm registers are all coded in BCD format.

8.1 CLKOUT output

A programmable square wave is available at the CLKOUT pin. Frequencies of 32.768 kHz, 1.024 kHz, 32 Hz and 1 Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator. CLKOUT is a CMOS push-pull output, and if disabled it becomes logic 0.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

8.2 Register organization

Table 5. Register overview

Bit positions labelled as - are not implemented. Bit positions labelled as N should always be written with logic 0. After reset, all registers are set according to Table 28.

Address	Register name	Bit							
		7	6	5	4	3	2	1	0
Control registers									
00h	Control_1	TEST1	N	STOP	N	TESTC	N	N	N
01h	Control_2	N	N	N	TI_TP	AF	TF	AIE	TIE
Time and date registers									
02h	Seconds	VL	SECONDS (0 to 59)						
03h	Minutes	-	MINUTES (0 to 59)						
04h	Hours	-	-	HOURS (0 to 23)					
05h	Days	-	-	DAYS (1 to 31)					
06h	Weekdays	-	-	-	-	-	WEEKDAYS		
07h	Months	C	-	-	MONTH (1 to 12)				
08h	Years	YEARS (0 to 99)							
Alarm registers									
09h	Minute_alarm	AEN_M	MINUTE_ALARM (0 to 59)						
0Ah	Hour_alarm	AEN_H	-	HOUR_ALARM (0 to 23)					
0Bh	Day_alarm	AEN_D	-	DAY_ALARM (1 to 31)					
0Ch	Weekday_alarm	AEN_W	-	-	-	-	WEEKDAY_ALARM		
CLKOUT control register									
0Dh	CLKOUT_ctrl	FE	-	-	-	-	-	FD[1:0]	
Timer registers									
0Eh	Timer_ctrl	TE	-	-	-	-	-	TD[1:0]	
0Fh	Timer	TV[7:0]							

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

8.3 Control registers

8.3.1 Register Control_1

Table 6. Control_1 - control and status register 1 (address 00h) bit description

Bit	Symbol	Value	Description	Reference
7	TEST1	0[1]	normal mode; • must be set to logic 0 during normal operations	Section 8.9
		1	EXT_CLK test mode (see Section 8.9)	
6	N	0[2]	default value	
5	STOP	0[1]	RTC source clock runs	Section 8.10
		1	• RTC divider chain flip-flops are asynchronously set to logic 0 • the RTC clock is stopped (CLKOUT at 32.768 kHz is still available)	
4	N	0[2]	default value	
3	TESTC	0	Power-On Reset (POR) override facility is disabled; • set to logic 0 for normal operation (see Section 8.11.1)	Section 8.11.1
		1[1]	Power-On Reset (POR) override is enabled	
2 to 0	N	000[2]	default value	

[1] Default value.

[2] Bits labeled as N should always be written with logic 0.

8.3.2 Register Control_2

Table 7. Control_2 - control and status register 2 (address 01h) bit description

Bit	Symbol	Value	Description	Reference
7 to 5	N	000[1]	default value	
4	TI_TP	0[2]	$\overline{INT}$ is active when TF is active (subject to the status of TIE)	
		1	$\overline{INT}$ pulses active according to Table 8 (subject to the status of TIE); • **Remark:** note that if AF and AIE are active then $\overline{INT}$ will be permanently active	Section 8.3.2.1 and Section 8.8
3	AF	0[2]	alarm flag inactive	Section 8.3.2.1
		1	alarm flag active	
2	TF	0[2]	timer flag inactive	Section 8.3.2.1
		1	timer flag active	
1	AIE	0[2]	alarm interrupt disabled	Section 8.3.2.1
		1	alarm interrupt enabled	
0	TIE	0[2]	timer interrupt disabled	Section 8.3.2.1
		1	timer interrupt enabled	

[1] Bits labeled as N should always be written with logic 0.

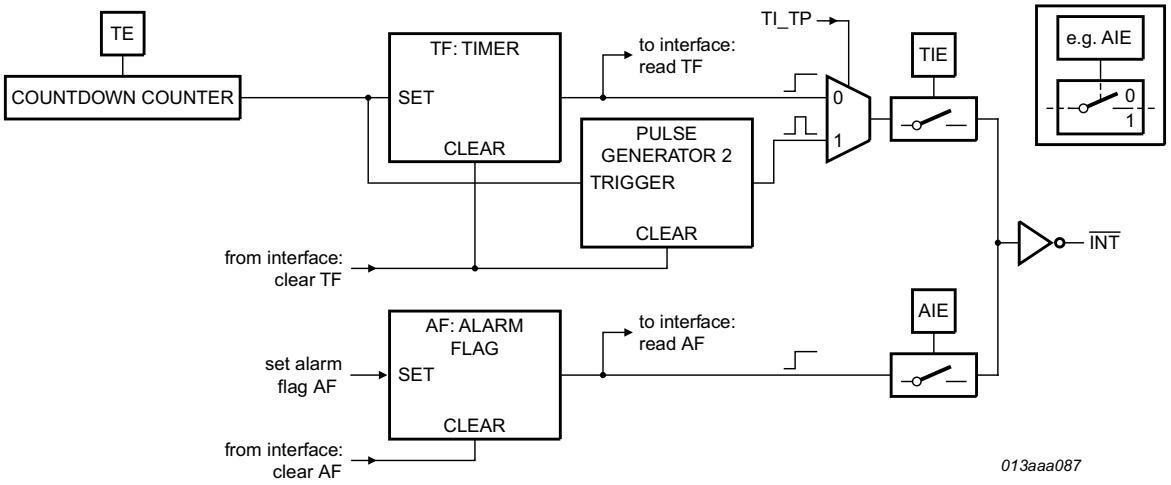
[2] Default value.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

8.3.2.1 Interrupt output

Bits TF and AF: When an alarm occurs, AF is set to 1. Similarly, at the end of a timer countdown, TF is set to 1. These bits maintain their value until overwritten by command. If both timer and alarm interrupts are required in the application, the source of the interrupt can be determined by reading these bits. To prevent one flag being overwritten while clearing another, a logic AND is performed during a write access.



When bits TIE and AIE are disabled, pin $\overline{INT}$ will remain high-impedance.

Fig 3. Interrupt scheme

Bits TIE and AIE: These bits activate or deactivate the generation of an interrupt when TF or AF is asserted respectively. The interrupt is the logical OR of these two conditions when both AIE and TIE are set.

Countdown timer interrupts: The pulse generator for the countdown timer interrupt uses an internal clock and is dependent on the selected source clock for the countdown timer and on the countdown value TV. As a consequence, the width of the interrupt pulse varies (see Table 8).

Table 8. $\overline{INT}$ operation (bit TI_TP = 1)[1]

Source clock (Hz)	$\overline{INT}$ period (s)	
	TV = 1[2]	TV > 1
4096	$1/8192$	$1/4096$
64	$1/128$	$1/64$
1	$1/64$	$1/64$
$1/60$	$1/64$	$1/64$

[1] TF and $\overline{INT}$ become active simultaneously.

[2] TV = loaded countdown value. Timer is stopped when TV = 0.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

8.4 Time and date registers

The majority of the registers are coded in the BCD format to simplify application use.

8.4.1 Register Seconds

Table 9. Seconds - seconds and clock integrity status register (address 02h) bit description

Bit	Symbol	Value	Place value	Description
7	VL	0	-	clock integrity is guaranteed
		1[1]	-	integrity of the clock information is not guaranteed
6 to 4	SECONDS	0 to 5	ten's place	actual seconds coded in BCD format, see Table 10
3 to 0		0 to 9	unit place	

[1] Start-up value.

Table 10. Seconds coded in BCD format

Seconds value in decimal	Upper-digit (ten's place)			Digit (unit place)			
	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	0	0	0	0	0	0	0
01	0	0	0	0	0	0	1
02	0	0	0	0	0	1	0
:							
09	0	0	0	1	0	0	1
10	0	0	1	0	0	0	0
:							
58	1	0	1	1	0	0	0
59	1	0	1	1	0	0	1

8.4.1.1 Voltage low detector and clock monitor

The PCF8564A has an on-chip voltage low detector. When V_{DD} drops below V_{low} the VL (Voltage Low) flag is set to indicate that the integrity of the clock information is no longer guaranteed. The VL flag can only be cleared by command.

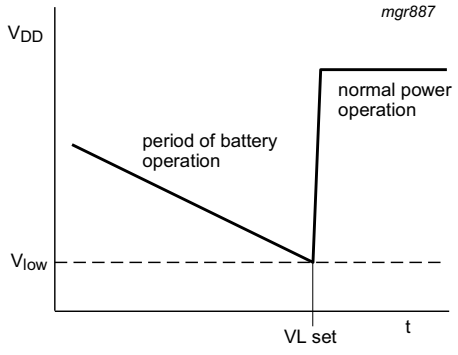


Fig 4. Voltage low detection

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

The VL flag is intended to detect the situation when V_{DD} is decreasing slowly, for example under battery operation. Should the oscillator stop or V_{DD} reach V_{low} before power is re-asserted, then the VL flag will be set. This indicates that the time is possibly corrupted.

8.4.2 Register Minutes

Table 11. Minutes - minutes register (address 03h) bit description

Bit	Symbol	Value	Place value	Description
7	-	-	-	unused
6 to 4	MINUTES	0 to 5	ten's place	actual minutes coded in BCD format
3 to 0		0 to 9	unit place	

8.4.3 Register Hours

Table 12. Hours - hours register (address 04h) bit description

Bit	Symbol	Value	Place value	Description
7 to 6	-	-	-	unused
5 to 4	HOURS	0 to 2	ten's place	actual hours coded in BCD format
3 to 0		0 to 9	unit place	

8.4.4 Register Days

Table 13. Days - days register (address 05h) bit description

Bit	Symbol	Value	Place value	Description
7 to 6	-	-	-	unused
5 to 4	DAYS[1]	0 to 3	ten's place	actual day coded in BCD format
3 to 0		0 to 9	unit place	

[1] The PCF8564A compensates for leap years by adding a 29th day to February if the year counter contains a value which is exactly divisible by 4, including the year 00.

8.4.5 Register Weekdays

Table 14. Weekdays - weekdays register (address 06h) bit description

Bit	Symbol	Value	Description
7 to 3	-	-	unused
2 to 0	WEEKDAYS	0 to 6	actual weekday values, see Table 15

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

Table 15. Weekday assignments

Day[1]	Bit		
	2	1	0
Sunday	0	0	0
Monday	0	0	1
Tuesday	0	1	0
Wednesday	0	1	1
Thursday	1	0	0
Friday	1	0	1
Saturday	1	1	0

[1] Definition may be re-assigned by the user.

8.4.6 Register Months

Table 16. Months - months and century flag register (address 07h) bit description

Bit	Symbol	Value	Place value	Description
7	C[1]	0[2]	-	indicates the century is x
		1	-	indicates the century is x + 1
6 to 5	-	-	-	unused
4	MONTHS	0 to 1	ten's place	actual month coded in BCD format, see Table 17
3 to 0		0 to 9	unit place	

[1] This bit may be re-assigned by the user.

[2] This bit is toggled when the register Years overflows from 99 to 00.

Table 17. Month assignments coded in BCD format

Month	Upper-digit (ten's place)	Digit (unit place)			
	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
January	0	0	0	0	1
February	0	0	0	1	0
March	0	0	0	1	1
April	0	0	1	0	0
May	0	0	1	0	1
June	0	0	1	1	0
July	0	0	1	1	1
August	0	1	0	0	0
September	0	1	0	0	1
October	1	0	0	0	0
November	1	0	0	0	1
December	1	0	0	1	0

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

8.4.7 Register Years

Table 18. Years - years register (08h) bit description

Bit	Symbol	Value	Place value	Description
7 to 4	YEARS	0 to 9	ten's place	actual year coded in BCD format[1]
3 to 0		0 to 9	unit place	

[1] When the register Years overflows from 99 to 00, the century bit C in the register Months is toggled.

The PCF8564A compensates for leap years by adding a 29th day to February if the year counter contains a value which is divisible by 4, including the year 00.

8.5 Setting and reading the time

Figure 5 shows the data flow and data dependencies starting from the 1 Hz clock tick.

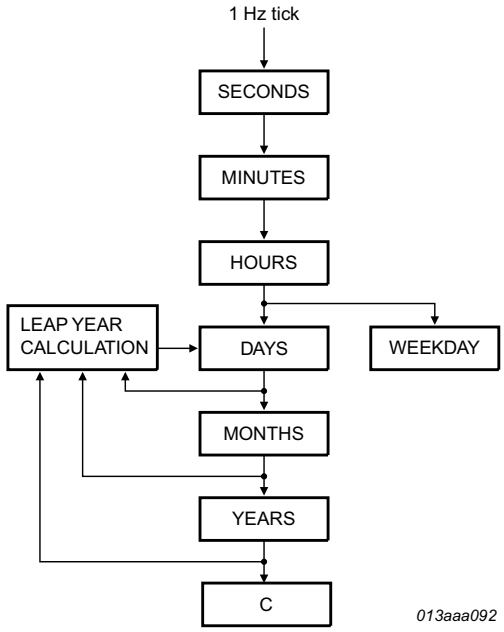


Fig 5. Data flow for the time function

During read/write operations, the time counting circuits (memory locations 02h through 08h) are blocked.

This prevents

- Faulty writing or reading of the clock and calendar during a carry condition
- Incrementing the time registers, during the read cycle

After this read/write access is completed, the time circuit is released again and any pending request to increment the time counters, that occurred during the read access, is serviced. A maximum of 1 request can be stored; therefore, all accesses must be completed within 1 second (see Figure 6).

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

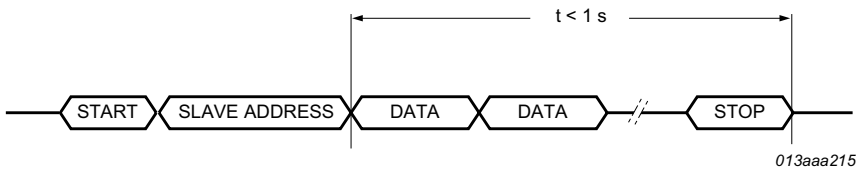


Fig 6. Access time for read/write operations

As a consequence of this method, it is very important to make a read or write access in one go, that is, setting or reading seconds through to years should be made in one single access. Failing to comply with this method could result in the time becoming corrupted.

As an example, if the time (seconds through to hours) is set in one access and then in a second access the date is set, it is possible that the time may increment between the two accesses. A similar problem exists when reading. A roll over may occur between reads thus giving the minutes from one moment and the hours from the next.

Recommended method for reading the time:

1. Send a START condition and the slave address for write (A2h).
2. Set the address pointer to 2 (seconds) by sending 02h.
3. Send a RE-START condition or STOP followed by START.
4. Send the slave address for read (A3h).
5. Read the seconds.
6. Read the minutes.
7. Read the hours.
8. Read the days.
9. Read the weekdays.
10. Read the century and month.
11. Read the years.
12. Send a STOP condition.

8.6 Alarm registers

8.6.1 Register Minute_alarm

Table 19. Minute_alarm - minute alarm register (address 09h) bit description

Bit	Symbol	Value	Place value	Description
7	AEN_M	0	-	minute alarm is enabled
		1[1]	-	minute alarm is disabled
6 to 4	MINUTE_ALARM	0 to 5	ten's place	minute alarm information coded in BCD format
3 to 0		0 to 9	unit place	

[1] Default value.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

8.6.2 Register Hour_alarm

Table 20. Hour_alarm - hour alarm register (address 0Ah) bit description

Bit	Symbol	Value	Place value	Description
7	AEN_H	0	-	hour alarm is enabled
		1[1]	-	hour alarm is disabled
6	-	-	-	unused
5 to 4	HOUR_ALARM	0 to 2	ten's place	hour alarm information coded in BCD format
3 to 0		0 to 9	unit place	

[1] Default value.

8.6.3 Register Day_alarm

Table 21. Day_alarm - day alarm register (address 0Bh) bit description

Bit	Symbol	Value	Place value	Description
7	AEN_D	0	-	day alarm is enabled
		1[1]	-	day alarm is disabled
6	-	-	-	unused
5 to 4	DAY_ALARM	0 to 3	ten's place	day alarm information coded in BCD format
3 to 0		0 to 9	unit place	

[1] Default value.

8.6.4 Register Weekday_alarm

Table 22. Weekday_alarm - weekday alarm register (address 0Ch) bit description

Bit	Symbol	Value	Description
7	AEN_W	0	weekday alarm is enabled
		1[1]	weekday alarm is disabled
6 to 3	-	-	unused
2 to 0	WEEKDAY_ALARM	0 to 6	weekday alarm information coded in BCD format

[1] Default value.

8.6.5 Alarm flag

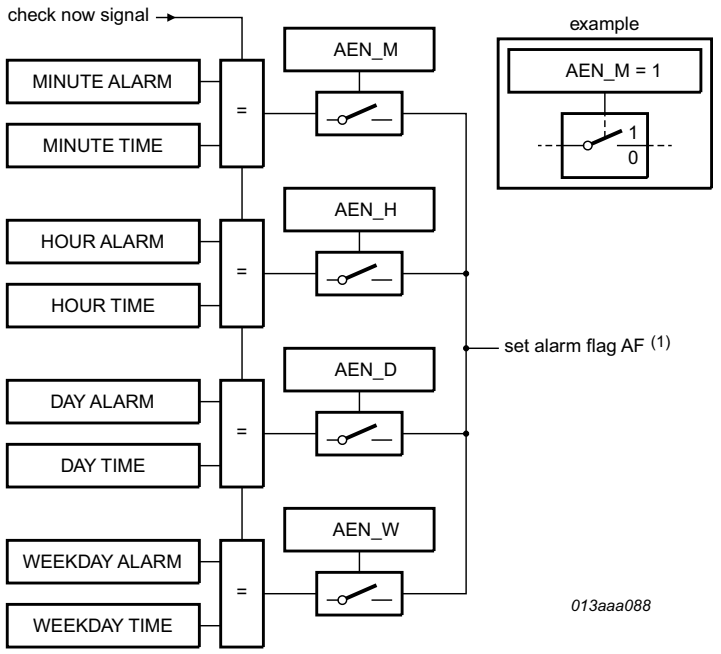
By clearing the MSB of one or more of the alarm registers AEN_x (Alarm Enable), the corresponding alarm condition(s) are active. When an alarm occurs, AF is set to logic 1. The asserted AF can be used to generate an interrupt ($\overline{INT}$). The AF is cleared by command.

The registers at addresses 09h through 0Ch contain alarm information. When one or more of these registers is loaded with a valid minute, hour, day, or weekday and its corresponding Alarm Enable bit (AEN_x) is logic 0, then that information is compared with the current minute, hour, day, and weekday. When all enabled comparisons first match, the Alarm Flag (AF in register Control_2) is set to logic 1.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

The generation of interrupts from the alarm function is controlled via bit AIE. If bit AIE is enabled, the $\overline{INT}$ pin follows the condition of bit AF. AF will remain set until cleared by command. Once AF has been cleared, it will only be set again when the time increments to match the alarm condition once more. Alarm registers which have their AEN_x bit at logic 1 are ignored.



(1) Only when all enabled alarm settings are matching.
It's only on increment to a matched case that the alarm flag is set, see Section 8.6.5.

Fig 7. Alarm function block diagram

8.7 Register CLKOUT_ctrl and clock output

A programmable square wave is available at pin CLKOUT. Operation is controlled by the FE bit in register CLKOUT_ctrl at address 0Dh and the CLKOUT output enable pin (CLKOE). To enable pin CLKOUT pin CLKOE must be set HIGH.

Frequencies of 32.768 kHz (default), 1.024 kHz, 32 Hz, and 1 Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

Table 23. CLKOUT_ctrl - CLKOUT control register (address 0Dh) bit description

Bit	Symbol	Value	Description
7	FE	0	the CLKOUT output is inhibited and CLKOUT output is set to logic 0
		1[1]	the CLKOUT output is activated
6 to 2	-	-	unused
1 to 0	FD[1:0]		frequency output at pin CLKOUT
		00[1]	32.768 kHz
		01	1.024 kHz
		10	32 Hz
		11	1 Hz

[1] Default value.

8.8 Timer function

The 8-bit countdown timer at address 0Fh is controlled by the timer control register at address 0Eh. The timer control register determines one of 4 source clock frequencies for the timer (4.096 kHz, 64 Hz, 1 Hz, or $1/60$ Hz) and enables or disables the timer. The timer counts down from a software-loaded 8-bit binary value. At the end of every countdown, the timer sets the TF (Timer Flag) to logic 1. The TF may only be cleared using the interface.

The generation of interrupts from the timer function is controlled via bit TIE. If bit TIE is enabled the $\overline{\text{INT}}$ pin follows the condition of bit TF. The interrupt may be generated as a pulsed signal every countdown period or as a permanently active signal which follows the condition of the timer flag TF. TI_TP is used for this mode control. When reading the timer, the current countdown value is returned.

8.8.1 Register Timer_ctrl

Table 24. Timer_ctrl - timer control register (address 0Eh) bit description

Bit	Symbol	Value	Description
7	TE	0[1]	timer is disabled
		1	timer is enabled
6 to 2	-	-	unused
1 to 0	TD[1:0]		timer source clock frequency select[2]
		00	4.096 kHz
		01	64 Hz
		10	1 Hz
		11[2]	$1/60$ Hz

[1] Default value.

[2] These bits determine the source clock for the countdown timer; when not in use, TD[1:0] should be set to $1/60$ Hz for power saving.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

8.8.2 Register Timer

Table 25. Timer - timer register (address 0Fh) bit description

Bit	Symbol	Value	Description
7 to 0	TV[7:0]	0h to FFh	countdown timer value[1]

[1] Countdown period in seconds: $CountdownPeriod = \frac{TV}{SourceClockFrequency}$ where TV is the countdown timer value.

Table 26. Timer register bits value range

Bit							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
128	64	32	16	8	4	2	1

The timer register is an 8-bit binary countdown timer. It is enabled or disabled via the timer control register. The source clock for the timer is also selected by the timer control register. Other timer properties such as single or periodic interrupt generation are controlled via the register Control_2 (address 01h).

For accurate read back of the count down value, the I^2C-bus clock (SDA) must be operating at a frequency of at least twice the selected timer clock. Since it is not possible to freeze the countdown timer counter during read back, it is recommended to read the register twice and check for consistent results.

8.9 EXT_CLK test mode

The test mode is entered by setting the TEST1 bit of register Control_1 to logic 1. The CLKOUT pin then becomes an input. The test mode replaces the internal 64 Hz signal with that applied to the CLKOUT pin. Every 64 positive edges applied to CLKOUT then generates an increment of one second.

The signal applied to the CLKOUT pin should have a minimum pulse width of 300 ns and a maximum period of 1000 ns. The 64 Hz clock, now sourced from CLKOUT, is divided down to 1 Hz by a 2^6 divide chain called a prescaler. The prescaler can be set to a known state by using the STOP bit. When the STOP bit is set, the prescaler is reset to logic 0. (STOP must be cleared before the prescaler can operate.)

From a STOP condition, the first 1 second increment will take place after 32 positive edges on CLKOUT. Thereafter, every 64 positive edges will cause a 1 second increment.

Remark: Entry into EXT_CLK test mode is not synchronized to the internal 64 Hz clock. When entering the test mode, no assumption as to the state of the prescaler can be made.

8.9.1 Operation example

1. Set EXT_CLK test mode (Bit 7 Control_1 = 1).
2. Set STOP (Bit 5 Control_1 = 1).
3. Clear STOP (Bit 5 Control_1 = 0).
4. Set time registers to desired value.
5. Apply 32 clock pulses to CLKOUT.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

6. Read time registers to see the first change.
7. Apply 64 clock pulses to CLKOUT.
8. Read time registers to see the second change.

Repeat 7 and 8 for additional increments.

8.10 STOP bit function

The function of the STOP bit is to allow for accurate starting of the time circuits. The STOP bit function will cause the upper part of the prescaler (F_2 to F_{14}) to be held in reset and thus no 1 Hz ticks will be generated (see Figure 8). The time circuits can then be set and will not increment until the STOP bit is released (see Figure 9 and Table 27).

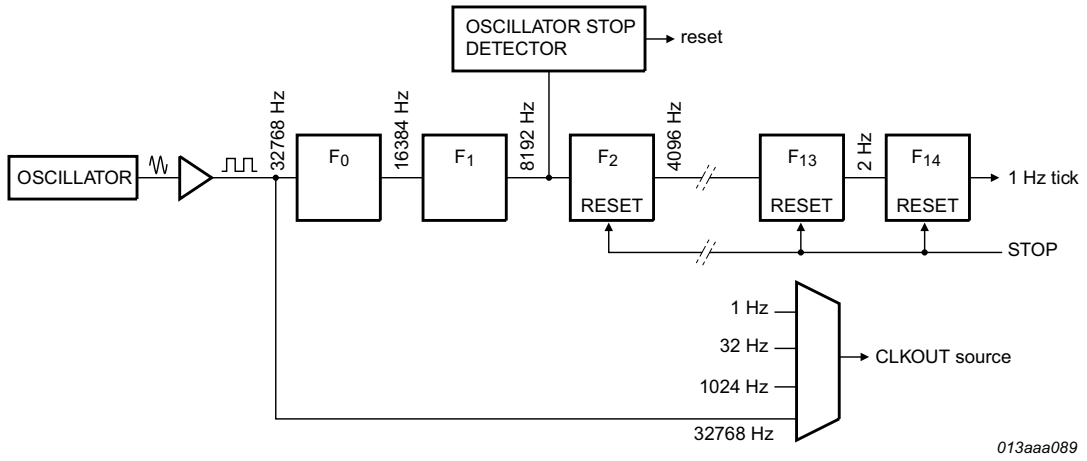


Fig 8. STOP bit functional diagram

The STOP bit function will not affect the output of 32.768 kHz on CLKOUT, but will stop the generation of 1.024 kHz, 32 Hz and 1 Hz.

The lower two stages of the prescaler (F_0 and F_1) are not reset and because the I^2C-bus is asynchronous to the crystal oscillator, the accuracy of re-starting the time circuits will be between zero and one 8.192 kHz cycle (see Figure 9).

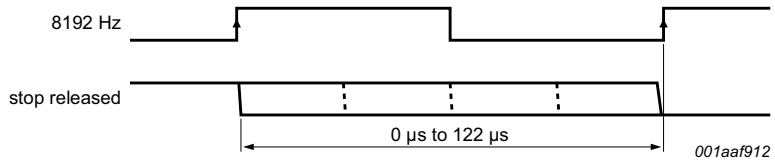
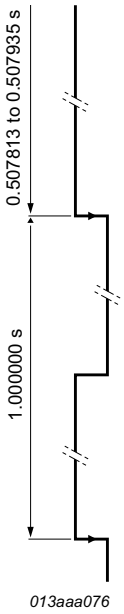


Fig 9. STOP bit release timing

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

Table 27. First increment of time circuits after STOP bit release

Bit STOP	Prescaler bits F_0F_1-F_2 to F_{14} [1]	1 Hz tick	Time hh:mm:ss	Comment
Clock is running normally				
0	01-0 0001 1101 0100		12:45:12	prescaler counting normally
STOP bit is activated by user. F_0F_1 are not reset and values cannot be predicted externally				
1	XX-0 0000 0000 0000		12:45:12	prescaler is reset; time circuits are frozen
New time is set by user				
1	XX-0 0000 0000 0000		08:00:00	prescaler is reset; time circuits are frozen
STOP bit is released by user				
0	XX-0 0000 0000 0000		08:00:00	prescaler is now running
	XX-1 0000 0000 0000		08:00:00	-
	XX-0 1000 0000 0000		08:00:00	-
	XX-1 1000 0000 0000		08:00:00	-
	:		:	:
	11-1 1111 1111 1110		08:00:00	-
	00-0 0000 0000 0001		08:00:01	0 to 1 transition of F_{14} increments the time circuits
	10-0 0000 0000 0001		08:00:01	-
	:		:	:
	11-1 1111 1111 1111		08:00:01	-
	00-0 0000 0000 0000		08:00:01	-
	10-0 0000 0000 0000		08:00:01	-
	:		:	-
	11-1 1111 1111 1110		08:00:01	-
	00-0 0000 0000 0001		08:00:02	0 to 1 transition of F_{14} increments the time circuits

[1] F_0 is clocked at 32.768 kHz.

The first increment of the time circuits is between 0.507813 s and 0.507935 s after STOP bit is released. The uncertainty is caused by the prescaler bits F_0 and F_1 not being reset (see Table 27) and the unknown state of the 32 kHz clock.

8.11 Reset

The PCF8564A includes an internal reset circuit which is active whenever the oscillator is stopped. In the reset state the I^2C-bus logic is initialized including the address pointer and all registers are set according to Table 28. I^2C-bus communication is not possible during reset.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

Table 28. Register reset values[1]

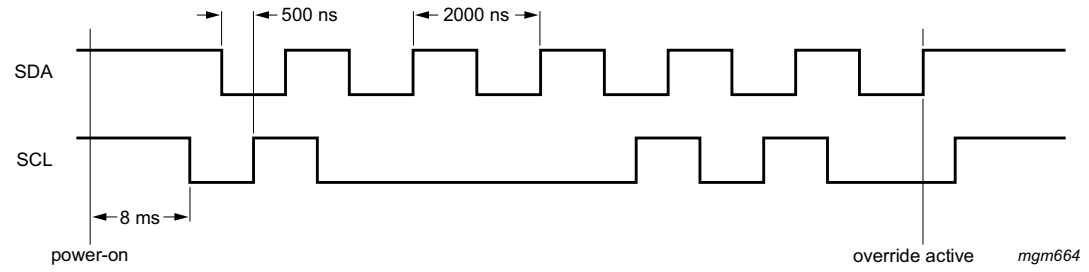
Address	Register name	Bit							
		7	6	5	4	3	2	1	0
00h	Control_1	0	0	0	0	1	0	0	0
01h	Control_2	0	0	0	0	0	0	0	0
02h	Seconds	1	x	x	x	x	x	x	x
03h	Minutes	x	x	x	x	x	x	x	x
04h	Hours	x	x	x	x	x	x	x	x
05h	Days	x	x	x	x	x	x	x	x
06h	Weekdays	x	x	x	x	x	x	x	x
07h	Months	x	x	x	x	x	x	x	x
08h	Years	x	x	x	x	x	x	x	x
09h	Minute_alarm	1	x	x	x	x	x	x	x
0Ah	Hour_alarm	1	x	x	x	x	x	x	x
0Bh	Day_alarm	1	x	x	x	x	x	x	x
0Ch	Weekday_alarm	1	x	x	x	x	x	x	x
0Dh	CLKOUT_ctrl	1	x	x	x	x	x	0	0
0Eh	Timer_ctrl	0	x	x	x	x	x	1	1
0Fh	Timer	x	x	x	x	x	x	x	x

[1] Registers marked ‘x’ are undefined at power-on and unchanged by subsequent resets.

8.11.1 Power-On Reset (POR) override

The POR duration is directly related to the crystal oscillator start-up time. Due to the long start-up times experienced by these types of circuits, a circuit has been implemented to disable the POR and speed up functional test of the module. The setting of this mode requires that the I^2C signals on the pins SDA and SCL are toggled as illustrated in Figure 10. All timings shown are required minimums.

Once the override mode has been entered, the chip immediately stops, being reset, and normal operation may begin, i.e., entry into the EXT_CLK test mode via I^2C access. The override mode may be cleared by writing logic 0 to TESTC. TESTC must be set to logic 1 before re-entry into the override mode is possible. Setting TESTC to logic 0 during normal operation has no effect, except to prevent entry into the POR override mode.



Allow 500 ns between the edges of either signal.

Fig 10. POR override sequence

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

9. Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial DAta line (SDA) and a Serial CLock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

9.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal (see Figure 11).

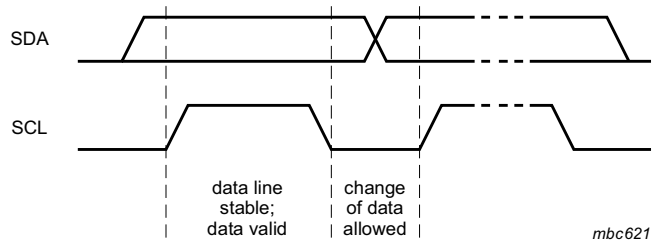


Fig 11. Bit transfer

9.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the START condition (S). A LOW-to-HIGH transition of the data line, while the clock is HIGH, is defined as the STOP condition (P), see Figure 12.

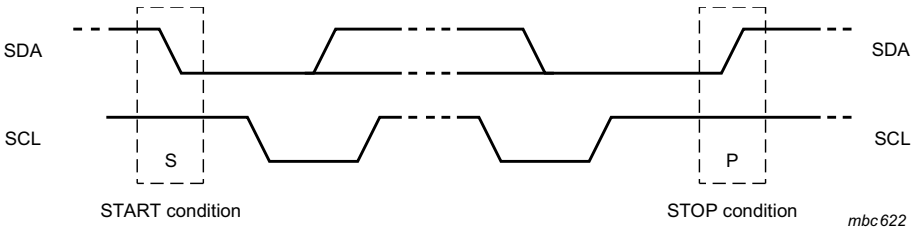


Fig 12. Definition of START and STOP conditions

9.3 System configuration

A device generating a message is a transmitter, a device receiving a message is the receiver. The device that controls the message is the master; and the devices which are controlled by the master are the slaves (see Figure 13).

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

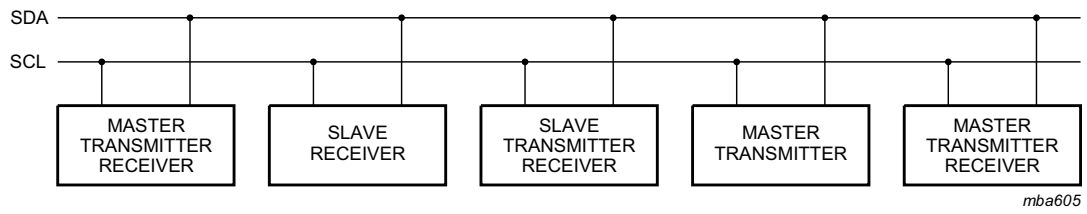


Fig 13. System configuration

9.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge cycle.

- A slave receiver, which is addressed, must generate an acknowledge after the reception of each byte.
- Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the I^2C-bus is shown in Figure 14.

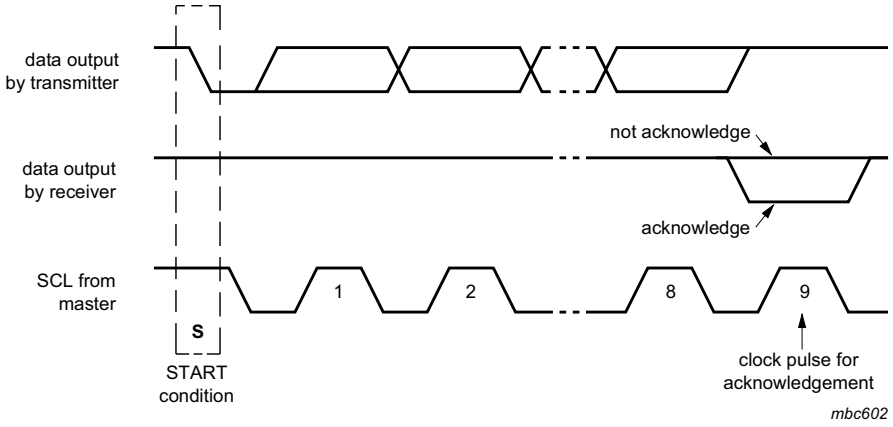


Fig 14. Acknowledgment on the I^2C-bus

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

10. I²C-bus protocol

10.1 Addressing

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure.

The PCF8564A acts as a slave receiver or slave transmitter. Therefore, the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line.

Two slave addresses are reserved for the PCF8564A:

Read: A3h (1010 0011)

Write: A2h (1010 0010)

The PCF8564A slave address is shown in Figure 14.

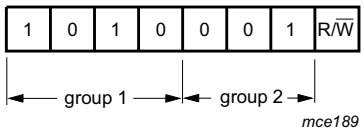


Fig 15. Slave address

10.2 Clock and calendar READ or WRITE cycles

Figure 16, Figure 17, and Figure 18 show the I²C-bus configuration for the different PCF8564A READ and WRITE cycles. The word address is a 4-bit value that defines which register is to be accessed next. The upper four bits of the word address are not used.

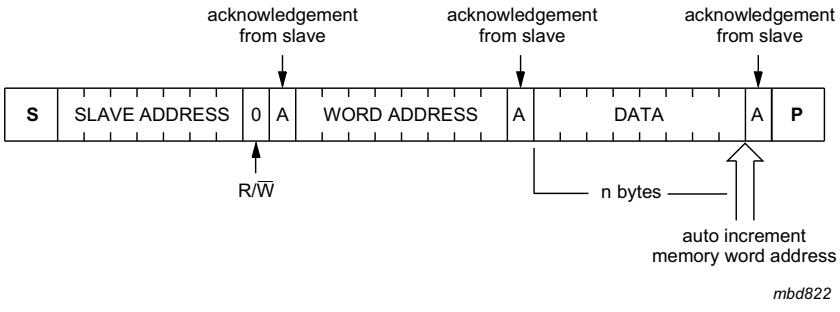


Fig 16. Master transmits to slave receiver (WRITE mode)

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

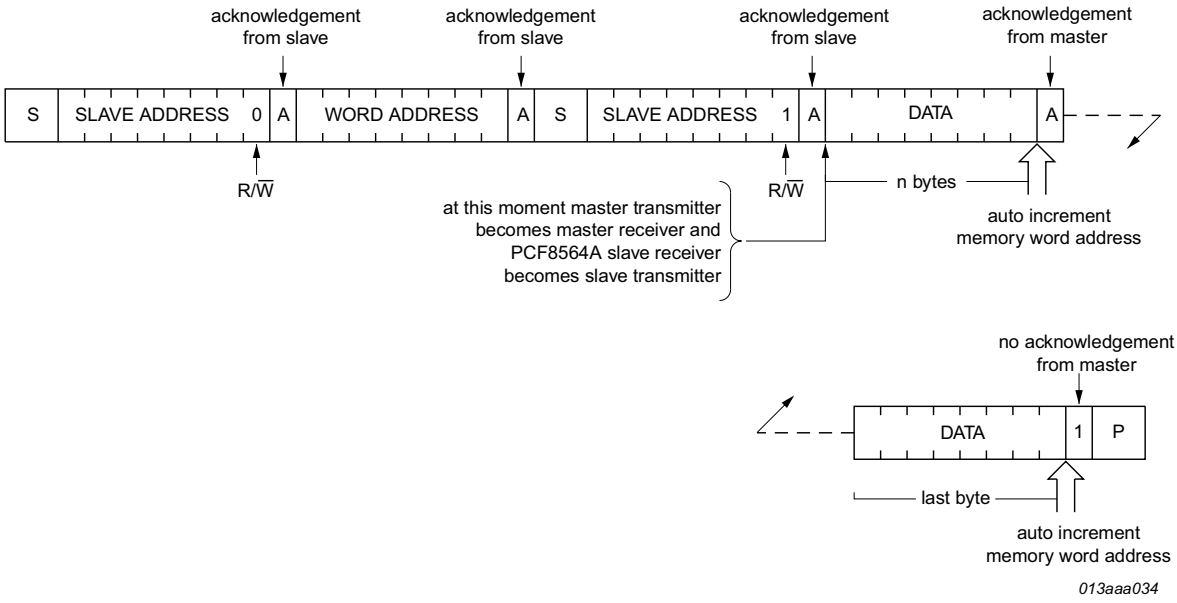


Fig 17. Master reads word after setting word address (write word address; READ data)

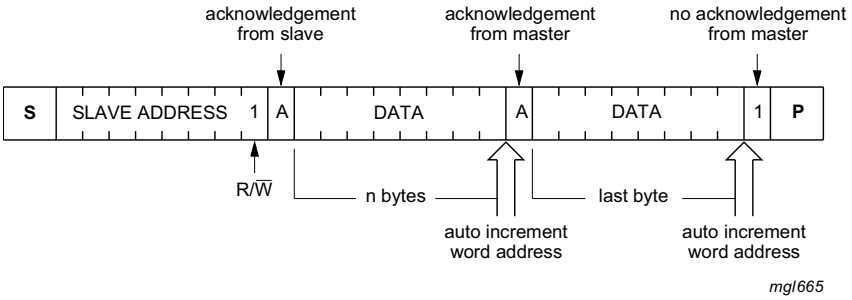
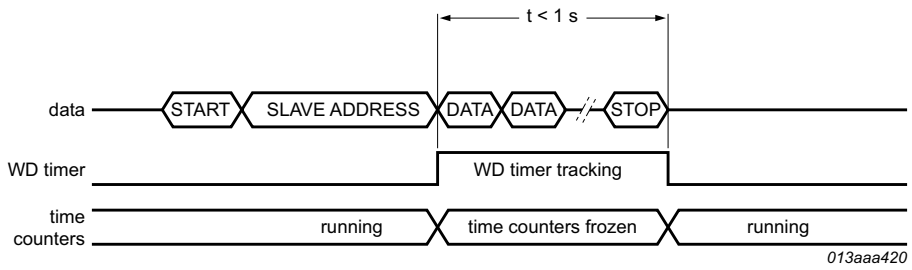


Fig 18. Master reads slave immediately after first byte (READ mode)

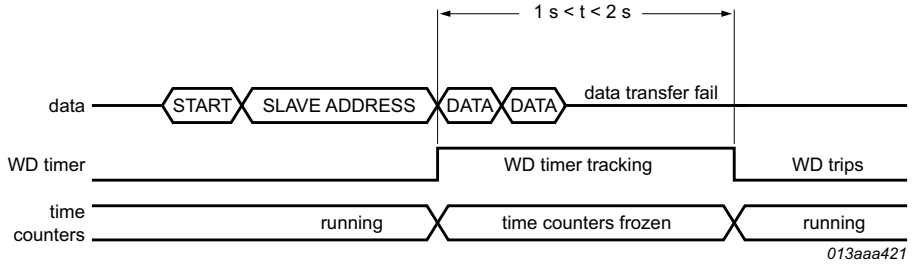
All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

10.3 Interface watchdog timer



a. Correct data transfer: read or write



b. Incorrect data transfer; read or write

Fig 19. Interface watchdog timer

During read/write operations, the time counting circuits are frozen. To prevent a situation where the accessing device becomes locked and does not clear the interface, the PCF8564A has a built in watchdog timer. Should the interface be active for more than 1 s from the time a valid slave address is transmitted, then the PCF8564A will automatically clear the interface and allow the time counting circuits to continue counting. The watchdog will trigger between 1 s and 2 s after receiving a valid slave address. Each time the watchdog period is exceeded, 1 s will be lost from the time counters.

The watchdog is implemented to prevent the excessive loss of time due to interface access failure e.g. if main power is removed from a battery backed-up system during an interface access.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

11. Internal circuitry

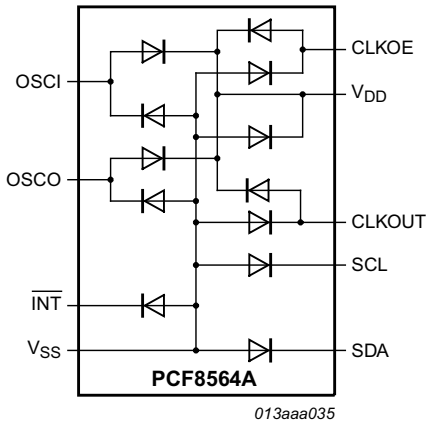


Fig 20. Device diode protection diagram

12. Safety notes

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

CAUTION

Semiconductors are light sensitive. Exposure to light sources can cause the IC to malfunction. The IC must be protected against light. The protection must be applied to all sides of the IC.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

13. Limiting values

Table 29. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			–0.5	+6.5	V
V_I	input voltage			–0.5	+6.5	V
V_O	output voltage			–0.5	+6.5	V
I_{DD}	supply current			–50.0	+50.0	mA
I_I	input current			–10.0	+10.0	mA
I_O	output current			–10.0	+10.0	mA
I_{SS}	ground supply current			–50.0	+50.0	mA
P_{tot}	total power dissipation			-	300	mW
V_{ESD}	electrostatic discharge voltage	HBM	[1]	-	±3500	V
		MM	[2]	-	±250	V
I_{lu}	latch-up current	all pins but OSCI	[3]	-	100	mA
T_{stg}	storage temperature		[4]	–65	+150	°C
T_{amb}	ambient temperature	operating device		–40	+85	°C

[1] Pass level; Human Body Model (HBM) according to Ref. 5 “JESD22-A114”.

[2] Pass level; Machine Model (MM), according to Ref. 6 “JESD22-A115”.

[3] Pass level; latch-up testing, according to Ref. 7 “JESD78” at maximum ambient temperature ($T_{amb(max)}$).

[4] According to the NXP store and transport conditions (see Ref. 11 “UM10569”) the devices have to be stored at a temperature of +5 °C to +45 °C and a humidity of 25 % to 75 %.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

14. Static characteristics

Table 30. Static characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; f_{osc} = 32.768 kHz; quartz R_s = 40 kΩ; C_L = 8 pF; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD}	supply voltage	interface inactive; T_{amb} = 25 °C	[1]	1.0	-	5.5	V
		interface active; f_{SCL} = 400 kHz	[1]	1.8	-	5.5	V
		for clock data integrity; T_{amb} = 25 °C		V_{low}	-	5.5	V
I_{DD}	supply current	interface active					
		f_{SCL} = 400 kHz		-	-	800	μA
		f_{SCL} = 100 kHz		-	-	200	μA
		interface inactive (f_{SCL} = 0 Hz); CLKOUT disabled; T_{amb} = 25 °C	[2] [3] [4]				
		V_{DD} = 5.0 V		-	275	550	nA
		V_{DD} = 3.0 V		-	250	500	nA
		V_{DD} = 2.0 V		-	225	450	nA
		interface inactive (f_{SCL} = 0 Hz); CLKOUT disabled; T_{amb} = −40 °C to +85 °C	[2] [3] [4]				
		V_{DD} = 5.0 V		-	500	750	nA
		V_{DD} = 3.0 V		-	400	650	nA
		V_{DD} = 2.0 V		-	400	600	nA
		interface inactive (f_{SCL} = 0 Hz); CLKOUT enabled at 32 kHz; T_{amb} = 25 °C	[4] [5] [6]				
		V_{DD} = 5.0 V		-	1500	3000	nA
		V_{DD} = 3.0 V		-	1000	2000	nA
		V_{DD} = 2.0 V		-	700	1400	nA
		interface inactive (f_{SCL} = 0 Hz); CLKOUT enabled at 32 kHz; T_{amb} = −40 °C to +85 °C	[4] [5] [6]				
		V_{DD} = 5.0 V		-	1700	3400	nA
		V_{DD} = 3.0 V		-	1100	2200	nA
		V_{DD} = 2.0 V		-	800	1600	nA
Inputs							
V_I	input voltage	on pins SDA and SCL		−0.5	-	+5.5	V
		on pins CLKOE and CLKOUT (test mode)		−0.5	-	V_{DD} + 0.5	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

Table 30. Static characteristics *...continued*

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; f_{osc} = 32.768 kHz; quartz R_s = 40 kΩ; C_L = 8 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{LI}	input leakage current	$V_I = V_{SS}$ or V_{DD}	-	0	-	µA
		post ESD event	−1	-	+1	µA
C_i	input capacitance	[7]	-	-	7	pF
Outputs						
V_O	output voltage	on pin CLKOUT	−0.5	-	V_{DD} + 0.5	V
		on pin $\overline{INT}$	−0.5	-	+5.5	V
I_{OL}	LOW-level output current	on pin SDA; V_{OL} = 0.4 V; V_{DD} = 5 V	3	-	-	mA
		on pin $\overline{INT}$; V_{OL} = 0.4 V; V_{DD} = 5 V	−1	-	-	mA
		on pin CLKOUT: V_{OL} = 0.4 V; V_{DD} = 5 V	−1	-	-	mA
I_{OH}	HIGH-level output current	on pin CLKOUT; V_{OH} = 4.6 V; V_{DD} = 5 V	1	-	-	mA
I_{LO}	output leakage current	$V_O = V_{SS}$ or V_{DD}	-	0	-	µA
		post ESD event	−1	-	+1	µA
Voltage detector						
V_{low}	low voltage	T_{amb} = 25 °C	-	0.9	1.0	V

[1] For reliable oscillator start-up at power-on: $V_{DD(po)min} = V_{DD(min)} + 0.3$ V.

[2] Timer source clock = $\frac{1}{60}$ Hz.

[3] CLKOUT disabled (FE = 0 or CLKOE = 0).

[4] V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

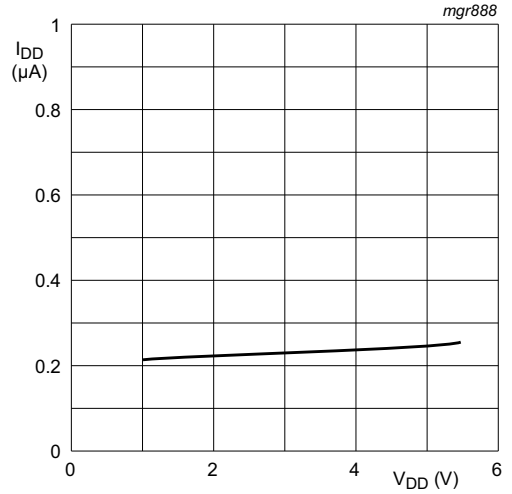
[5] CLKOUT is open circuit.

[6] Current consumption when the CLKOUT pin is enabled is a function of the load on the pin, the output frequency, and the supply voltage. The additional current consumption for a given load is calculated from: $I_{DD} = C \times V_{DD} \times F_{CLKOUT}$.

[7] Tested on sample basis.

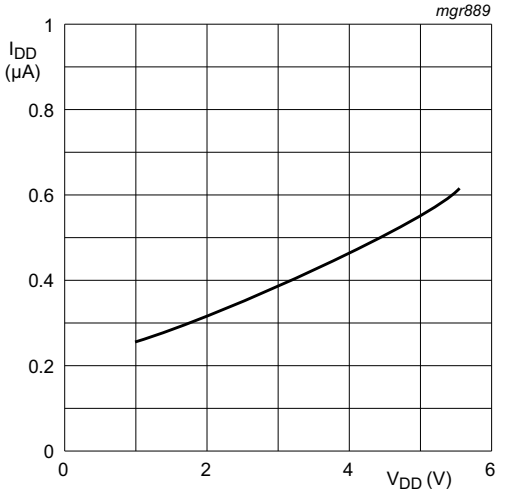
All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.



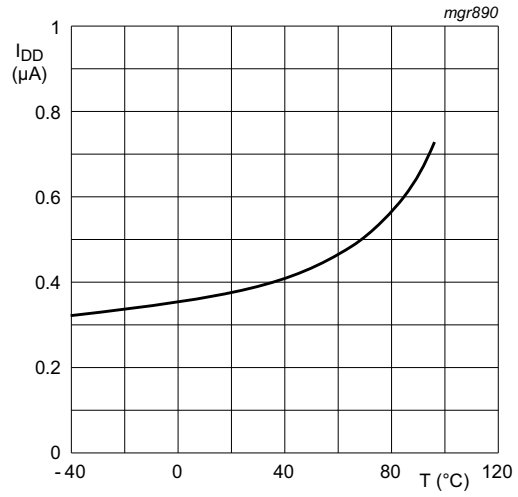
T_{amb} = 25 °C; timer = 1 minute; CLKOUT disabled.

Fig 21. I_{DD} as a function of V_{DD}



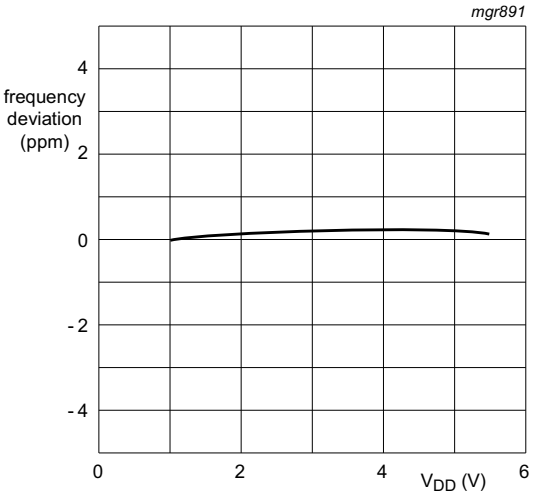
T_{amb} = 25 °C; timer = 1 minute; CLKOUT = 32 kHz.

Fig 22. I_{DD} as a function of V_{DD}



V_{DD} = 3 V; timer = 1 minute; CLKOUT = 32 kHz.

Fig 23. I_{DD} as a function of temperature



T_{amb} = 25 °C; normalized to V_{DD} = 3 V.

Fig 24. Frequency deviation as a function of V_{DD}

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

15. Dynamic characteristics

Table 31. Dynamic characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; f_{osc} = 32.768 kHz; quartz R_s = 40 kΩ; C_L = 8 pF; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Oscillator							
$C_{L(itg)}$	integrated load capacitance		[1]	6	8	10	pF
$\Delta f_{osc}/f_{osc}$	relative oscillator frequency variation	ΔV_{DD} = 200 mV; T_{amb} = 25 °C		-	0.2	-	ppm
Quartz crystal parameters							
R_S	series resistance			-	-	100	kΩ
C_L	load capacitance			-	8	-	pF
CLKOUT output							
δ_{CLKOUT}	duty cycle on pin CLKOUT		[2]	-	50	-	%
I²C-bus timing characteristics (see Figure 25)			[3][4]				
f_{SCL}	SCL clock frequency			-	-	400	kHz
$t_{HD;STA}$	hold time (repeated) START condition			0.6	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			0.6	-	-	µs
t_{LOW}	LOW period of the SCL clock			1.3	-	-	µs
t_{HIGH}	HIGH period of the SCL clock			0.6	-	-	µs
t_r	rise time of both SDA and SCL signals			-	-	0.3	µs
t_f	fall time of both SDA and SCL signals			-	-	0.3	µs
C_b	capacitive load for each bus line			-	-	400	pF
$t_{SU;DAT}$	data set-up time			100	-	-	ns
$t_{HD;DAT}$	data hold time			0	-	-	ns
$t_{SU;STO}$	set-up time for STOP condition			0.6	-	-	µs
$t_{w(spike)}$	spike pulse width			-	-	50	ns

[1] Integrated load capacitance, $C_{L(itg)}$, is a calculation of C_{OSCI} and C_{OSCO} in series: $C_{L(itg)} = \frac{(C_{OSCI} \cdot C_{OSCO})}{(C_{OSCI} + C_{OSCO})}$.

[2] Unspecified for f_{CLKOUT} = 32.768 kHz.

[3] All timing values are valid within the operating supply voltage at ambient temperature and referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

[4] A detailed description of the I²C-bus specification is given in Ref. 9 “UM10204”.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

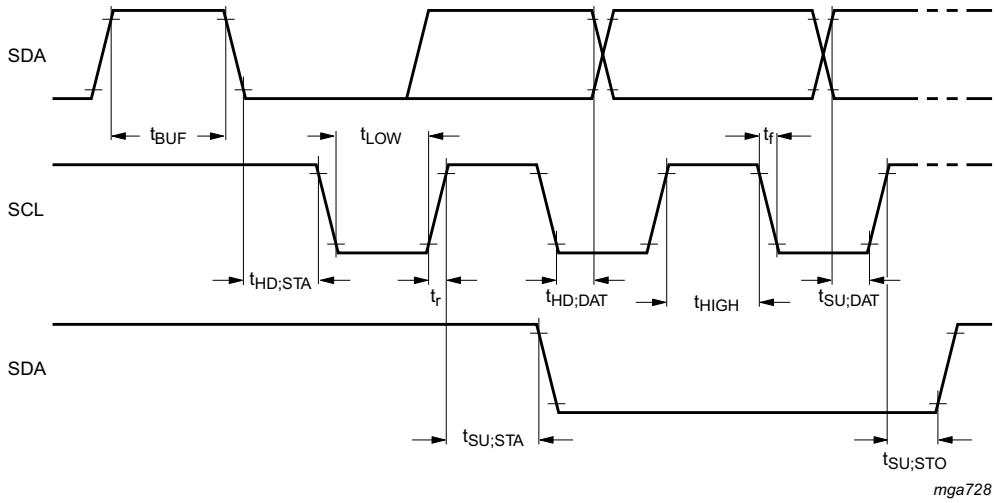
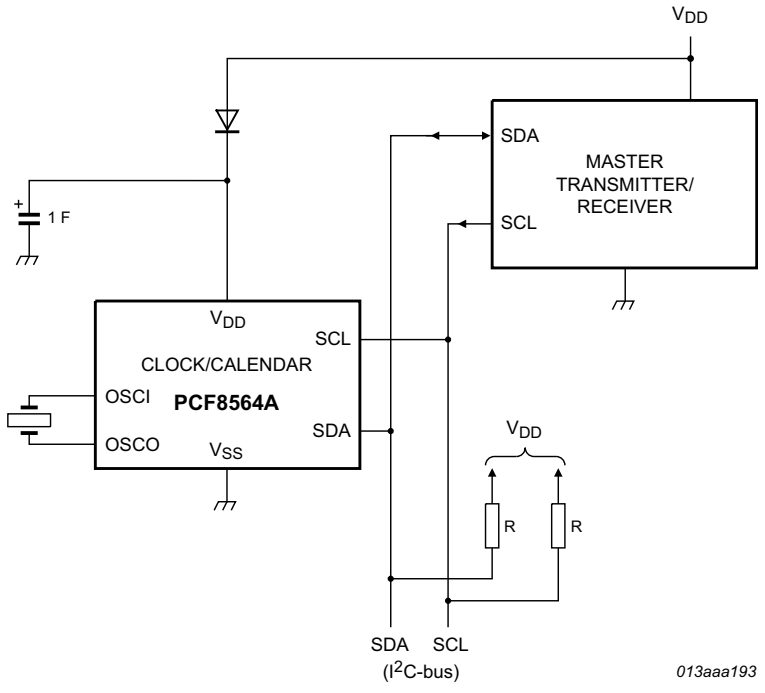


Fig 25. I²C-bus timing waveforms

16. Application information



Connect CLKOE to an appropriate level.

A 1 farad super capacitor combined with a low V_F diode can be used as a standby or back-up supply. With the RTC in its minimum power configuration, the RTC may operate for weeks.

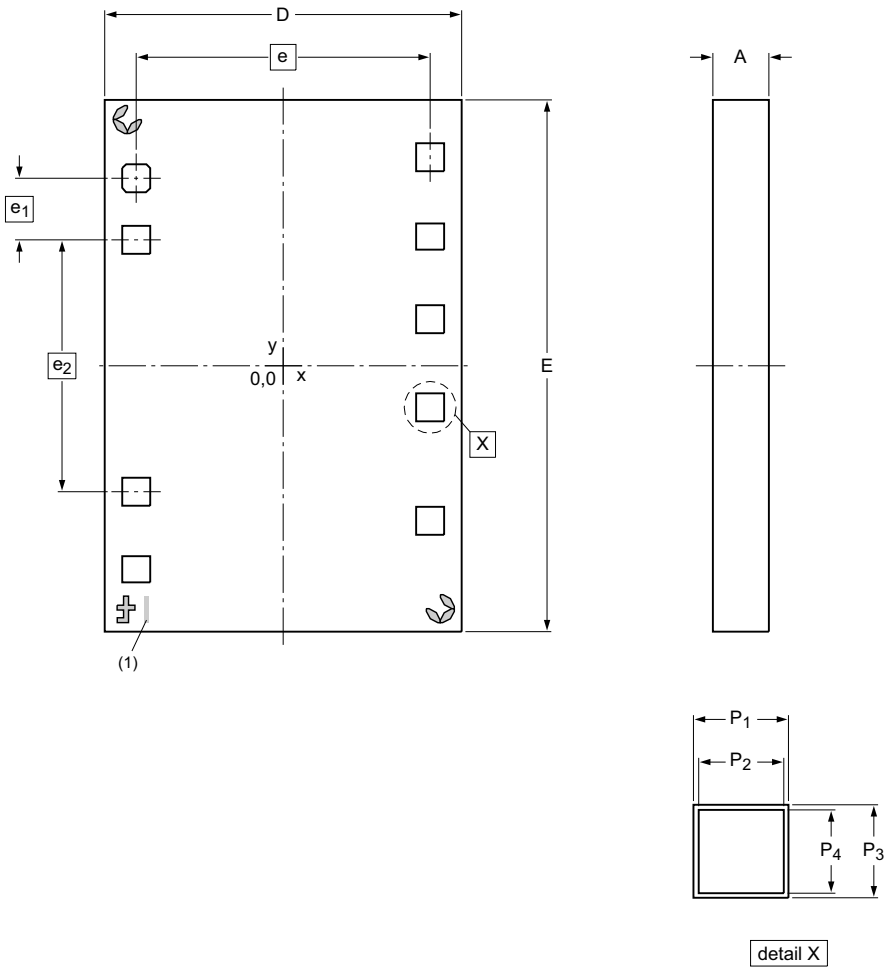
Fig 26. Application diagram

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

17. Bare die outline

Wire bond die; 9 bonding pads **PCF8564AU**



Note
1. Marking code: PC8564A-1
Figure not drawn to scale

pcf8564au_do

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
PCF8564AU						~~09-09-10~~ 13-07-16

Fig 27. Bare die outline of PCF8564AU/x

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

Table 32. Dimensions of PCF8564AU/x

Chip dimensions including saw line. Original dimensions are in mm.

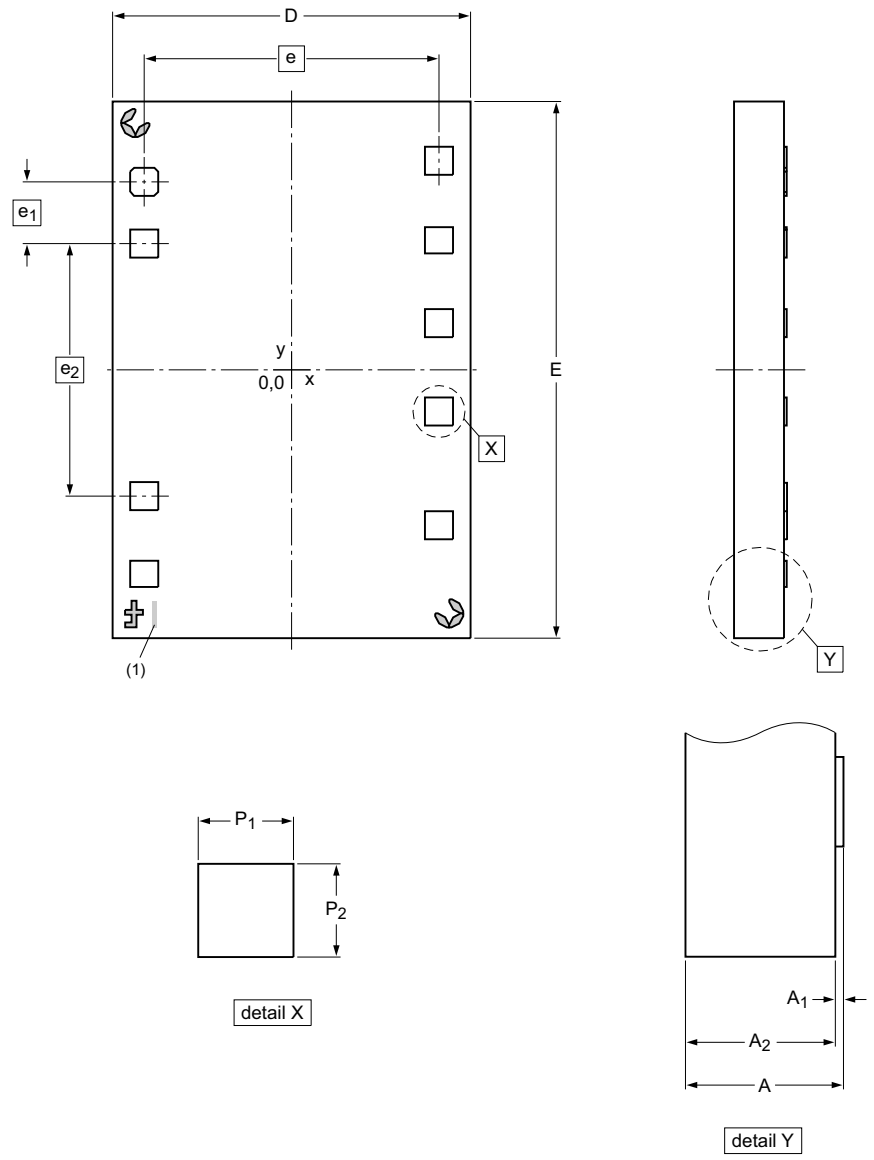
Unit (mm)	A	D	E	e	e_1	e_2	P_1	P_2	P_3	P_4
max	-	-	-	-	-	-	-	-	-	-
nom	[1]	1.26	1.89	1.05	0.22	0.9	0.1	0.09	0.1	0.09
min	-	-	-	-	-	-	-	-	-	-

[1] Depending on wafer thickness, see Table 37.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

Bare die; 9 bumps **PCF8564AUG**



Note
1. Marking code: PC8564A-1
Figure not drawn to scale

pcf8564aug_do

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
PCF8564AUG						13-08-26

Fig 28. Bare die outline of PCF8564AUG/x

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

Table 33. Dimensions of PCF8564AUG/x

Chip dimensions including saw line. Original dimensions are in mm.

Unit (mm)	A	A_1	A_2	D	E	e	e_1	e_2	P_1	P_2
max	-	-	-	-	-	-	-	-	-	-
nom	[1]	0.015	[1]	1.26	1.89	1.05	0.22	0.9	0.09	0.09
min	-	-	-	-	-	-	-	-	-	-

[1] Depending on wafer thickness, see Table 37.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

Table 34. Pin location of all PCF8564A types

All x/y coordinates represent the position of the center of each pin with respect to the center (x/y = 0) of the chip; see Figure 27 and Figure 28.

Symbol	Pad	X (μm)	Y (μm)	Description
OSCI	1	−523.0	689.4	oscillator input
OSCO	2	−523.0	469.4	oscillator output
$\overline{INT}$	3	−523.0	−429.8	open-drain interrupt output (active LOW)
V_{SS}	4	−523.0	−684.4	ground (substrate)
SDA	5	524.9	−523.8	serial data I/O
SCL	6	524.9	−138.6	serial clock input
CLKOUT	7	524.9	162.5	CMOS push-pull clock output
V_{DD}	8	524.9	443.3	supply
CLKOE	9	524.9	716.3	CLKOUT output enable

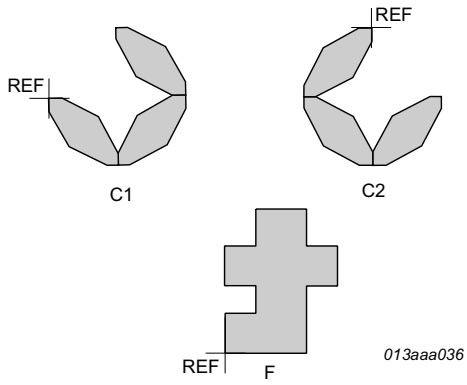


Fig 29. Alignment marks of all PCF8564A types

Table 35. Alignment marks of all PCF8564A types

All x/y coordinates represent the position of the REF point (see Figure 29) with respect to the center (x/y = 0) of the chip; see Figure 27 and Figure 28.

Alignment markers	Size (μm)	X (μm)	Y (μm)
C1	100 × 100	465.2	−826.3
C2	100 × 100	−523.0	890.0
F	90 × 117	−569.9	−885.5

Table 36. Gold bump hardness

Type number	Min	Max	Unit[1]
PCF8564AUG/12HB/1	35	80	HV

[1] Pressure of diamond head: 10 g to 50 g.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

18. Handling information

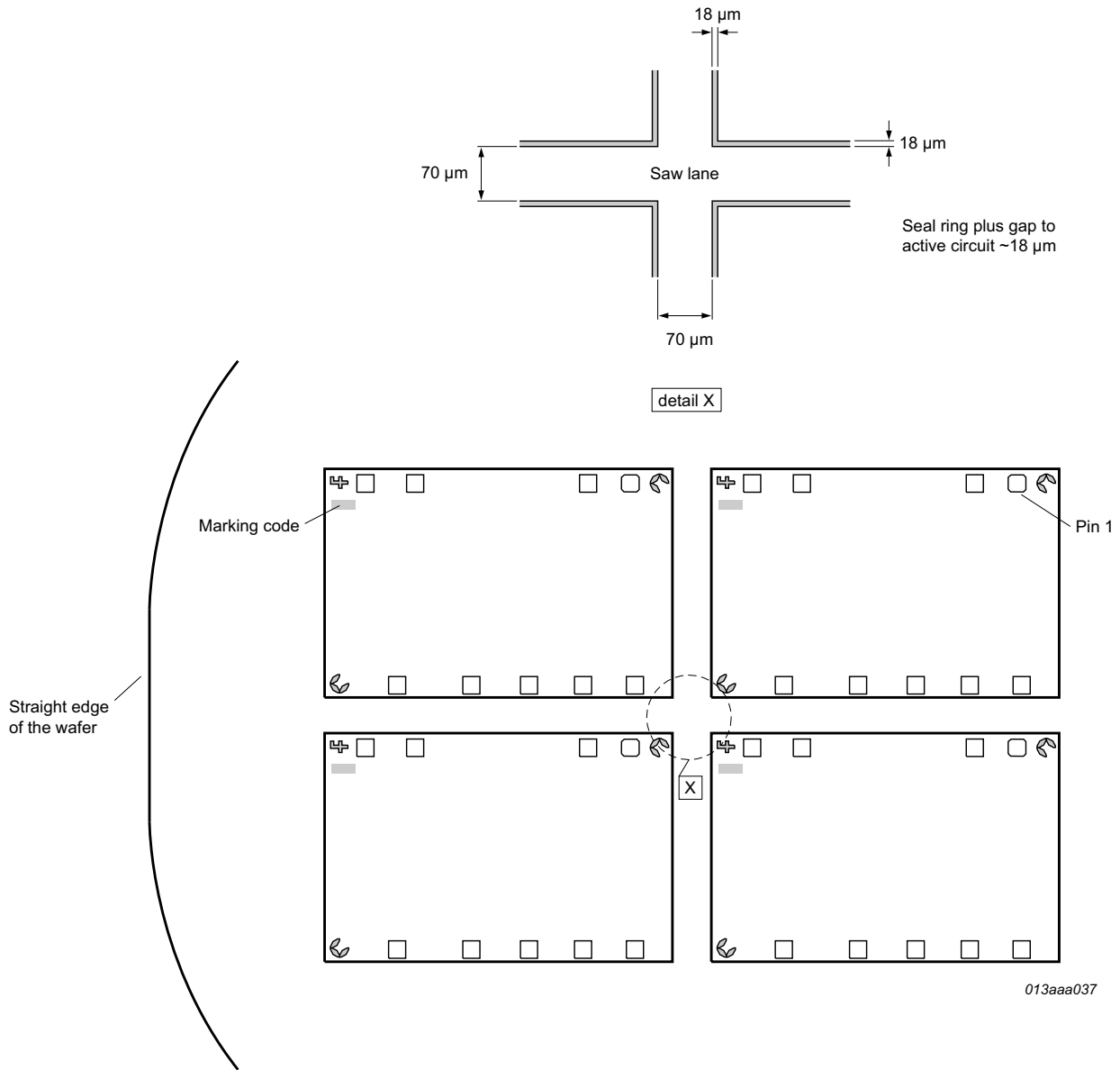
All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

19. Packing information

19.1 Wafer and Film Frame Carrier (FFC) information



Wafer thickness, see Table 37.

Fig 30. Wafer layout of PCF8564A

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

Table 37. PCF8564A wafer information

Type number	Wafer thickness	Wafer diameter	FFC for wafer size	Marking of bad die
PCF8564AU/5BB/1	0.28 mm	6 inch	-	inking
PCF8564AU/5GB/1	0.69 mm	6 inch	-	inking
PCF8564AU/5GC/1	0.69 mm	6 inch	-	wafer mapping
PCF8564AU/10AB/1	0.20 mm	6 inch	6 inch	inking
PCF8564AUG/12HB/1	0.15 mm	6 inch	8 inch	inking

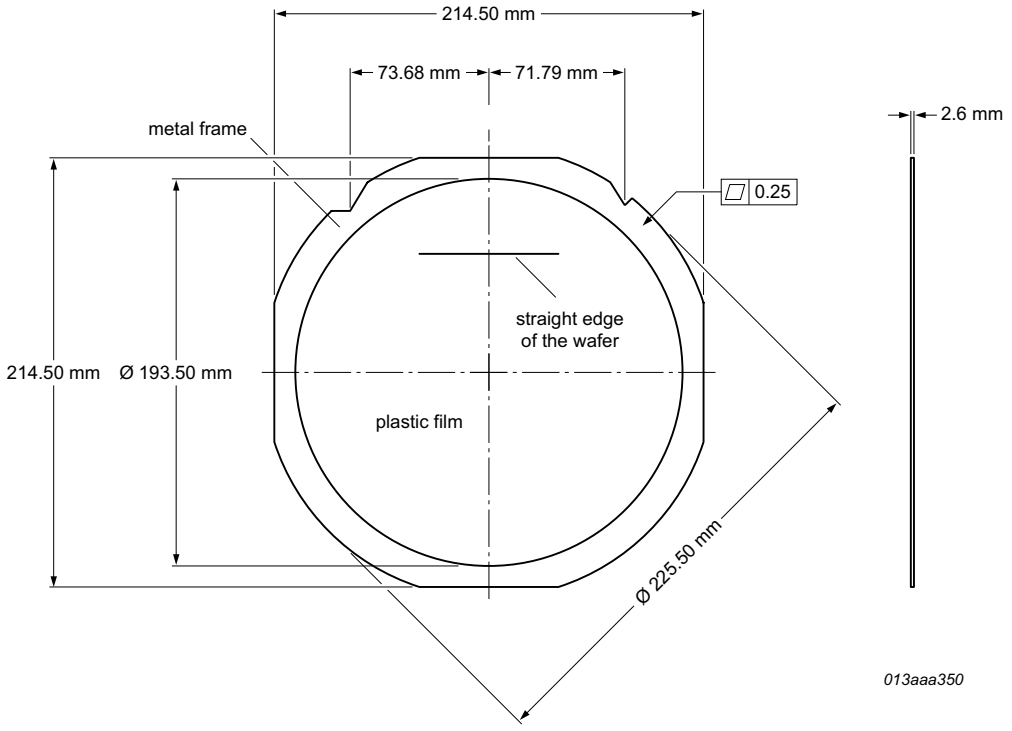


Fig 31. Film Frame Carrier (FFC) for 6 inch wafer (PCF8564AU/10AB/1)

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

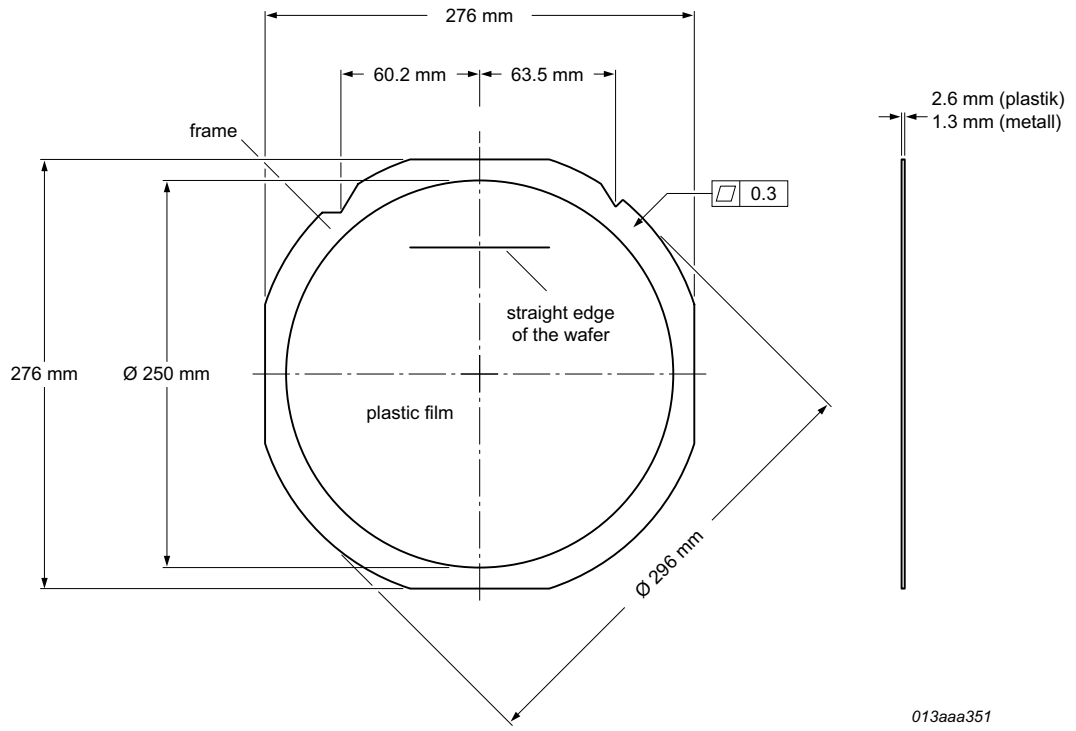


Fig 32. Film Frame Carrier (FFC) for 8 inch wafer (PCF8564AUG/12HB/1)

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

20. Abbreviations

Table 38. Abbreviations

Acronym	Description
BCD	Binary Coded Decimal
CMOS	Complementary Metal Oxide Semiconductor
FFC	Film Frame Carrier
HBM	Human Body Model
I^2C	Inter-Integrated Circuit
IC	Integrated Circuit
LSB	Least Significant Bit
MM	Machine Model
MOS	Metal Oxide Semiconductor
MSB	Most Significant Bit
MSL	Moisture Sensitivity Level
PCB	Printed-Circuit Board
POR	Power-On Reset
ROM	Read Only Memory
RTC	Real Time Clock
SCL	Serial CLock line
SDA	Serial DAta line

21. References

[1] **AN10439 —** Wafer Level Chip Size Package

[2] **AN10706 —** Handling bare die

[3] **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[4] **IEC 61340-5 —** Protection of electronic devices from electrostatic phenomena

[5] **JESD22-A114 —** Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[6] **JESD22-A115 —** Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)

[7] **JESD78 —** IC Latch-Up Test

[8] **JESD625-A —** Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

[9] **UM10204 —** I^2C-bus specification and user manual

[10] **UM10301 —** User Manual for NXP Real Time Clocks PCF85x3, PCA8565 and PCF2123, PCA2125

[11] **UM10569 —** Store and transport requirements

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

22. Revision history

Table 39. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCF8564A v.3	20130826	Product data sheet	-	PCF8564A v.2
Modifications:	• adjusted product and ordering information • added Figure 19			
PCF8564A v.2	20100930	Product data sheet	-	PCF8564A v.1
PCF8564A v.1	20091008	Product data sheet	-	-

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

23. Legal information

23.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

23.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

23.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Bare die — All die are tested on compliance with their related technical specifications as stated in this data sheet up to the point of wafer sawing and are handled in accordance with the NXP Semiconductors storage and transportation conditions. If there are data sheet limits not guaranteed, these will be separately indicated in the data sheet. There are no post-packing tests performed on individual die or wafers.

NXP Semiconductors has no control of third party procedures in the sawing, handling, packing or assembly of the die. Accordingly, NXP Semiconductors assumes no liability for device functionality or performance of the die or systems after third party sawing, handling, packing or assembly of the die. It is the responsibility of the customer to test and qualify their application in which the die is used.

All die sales are conditioned upon and subject to the customer entering into a written die sale agreement with NXP Semiconductors through its legal department.

23.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

I^2C-bus — logo is a trademark of NXP B.V.

24. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

25. Tables

Table 1. Ordering information 2
Table 2. Ordering options 2
Table 3. Marking codes 2
Table 4. Pin description 4
Table 5. Register overview 6
Table 6. Control_1 - control and status register 1 (address 00h) bit description 7
Table 7. Control_2 - control and status register 2 (address 01h) bit description 7
Table 8. $\overline{INT}$ operation (bit TI_TP = 1)[1] 8
Table 9. Seconds - seconds and clock integrity status register (address 02h) bit description 9
Table 10. Seconds coded in BCD format 9
Table 11. Minutes - minutes register (address 03h) bit description 10
Table 12. Hours - hours register (address 04h) bit description 10
Table 13. Days - days register (address 05h) bit description 10
Table 14. Weekdays - weekdays register (address 06h) bit description 10
Table 15. Weekday assignments 11
Table 16. Months - months and century flag register (address 07h) bit description 11
Table 17. Month assignments coded in BCD format . . .11
Table 18. Years - years register (08h) bit description 12
Table 19. Minute_alarm - minute alarm register (address 09h) bit description 13
Table 20. Hour_alarm - hour alarm register (address 0Ah) bit description 14
Table 21. Day_alarm - day alarm register (address 0Bh) bit description 14
Table 22. Weekday_alarm - weekday alarm register (address 0Ch) bit description 14
Table 23. CLKOUT_ctrl - CLKOUT control register (address 0Dh) bit description 16
Table 24. Timer_ctrl - timer control register (address 0Eh) bit description 16
Table 25. Timer - timer register (address 0Fh) bit description 17
Table 26. Timer register bits value range 17
Table 27. First increment of time circuits after STOP bit release 19
Table 28. Register reset values[1] 20
Table 29. Limiting values 27
Table 30. Static characteristics 28
Table 31. Dynamic characteristics 31
Table 32. Dimensions of PCF8564AU/x 34
Table 33. Dimensions of PCF8564AUG/x 36
Table 34. Pin location of all PCF8564A types 37
Table 35. Alignment marks of all PCF8564A types 37
Table 36. Gold bump hardness 37
Table 37. PCF8564A wafer information 40
Table 38. Abbreviations 42
Table 39. Revision history 43

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

26. Figures

Fig 1. Block diagram of PCF8564A 3
Fig 2. Pinning diagram of PCF8564A 4
Fig 3. Interrupt scheme 8
Fig 4. Voltage low detection 9
Fig 5. Data flow for the time function 12
Fig 6. Access time for read/write operations 13
Fig 7. Alarm function block diagram. 15
Fig 8. STOP bit functional diagram 18
Fig 9. STOP bit release timing 18
Fig 10. POR override sequence 20
Fig 11. Bit transfer 21
Fig 12. Definition of START and STOP conditions. 21
Fig 13. System configuration 22
Fig 14. Acknowledgment on the I^2C-bus 22
Fig 15. Slave address 23
Fig 16. Master transmits to slave receiver (WRITE mode) 23
Fig 17. Master reads word after setting word address (write word address; READ data) 24
Fig 18. Master reads slave immediately after first byte (READ mode) 24
Fig 19. Interface watchdog timer 25
Fig 20. Device diode protection diagram 26
Fig 21. I_{DD} as a function of V_{DD} 30
Fig 22. I_{DD} as a function of V_{DD} 30
Fig 23. I_{DD} as a function of temperature 30
Fig 24. Frequency deviation as a function of V_{DD} 30
Fig 25. I^2C-bus timing waveforms 32
Fig 26. Application diagram 32
Fig 27. Bare die outline of PCF8564AU/x 33
Fig 28. Bare die outline of PCF8564AUG/x 35
Fig 29. Alignment marks of all PCF8564A types 37
Fig 30. Wafer layout of PCF8564A 39
Fig 31. Film Frame Carrier (FFC) for 6 inch wafer (PCF8564AU/10AB/1) 40
Fig 32. Film Frame Carrier (FFC) for 8 inch wafer (PCF8564AUG/12HB/1) 41

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

27. Contents

1 General description 1
2 Features and benefits 1
3 Applications 1
4 Ordering information 2
4.1 Ordering options 2
5 Marking 2
6 Block diagram 3
7 Pinning information 4
7.1 Pinning 4
7.2 Pin description 4
8 Functional description 5
8.1 CLKOUT output 5
8.2 Register organization 6
8.3 Control registers 7
8.3.1 Register Control_1 7
8.3.2 Register Control_2 7
8.3.2.1 Interrupt output 8
8.4 Time and date registers 9
8.4.1 Register Seconds 9
8.4.1.1 Voltage low detector and clock monitor 9
8.4.2 Register Minutes 10
8.4.3 Register Hours 10
8.4.4 Register Days 10
8.4.5 Register Weekdays 10
8.4.6 Register Months 11
8.4.7 Register Years 12
8.5 Setting and reading the time 12
8.6 Alarm registers 13
8.6.1 Register Minute_alarm 13
8.6.2 Register Hour_alarm 14
8.6.3 Register Day_alarm 14
8.6.4 Register Weekday_alarm 14
8.6.5 Alarm flag 14
8.7 Register CLKOUT_ctrl and clock output 15
8.8 Timer function 16
8.8.1 Register Timer_ctrl 16
8.8.2 Register Timer 17
8.9 EXT_CLK test mode 17
8.9.1 Operation example 17
8.10 STOP bit function 18
8.11 Reset 19
8.11.1 Power-On Reset (POR) override 20
9 Characteristics of the I^2C-bus 21
9.1 Bit transfer 21
9.2 START and STOP conditions 21
9.3 System configuration 21
9.4 Acknowledge 22
10 I^2C-bus protocol 23
10.1 Addressing 23
10.2 Clock and calendar READ or WRITE cycles . 23
10.3 Interface watchdog timer 25
11 Internal circuitry 26
12 Safety notes 26
13 Limiting values 27
14 Static characteristics 28
15 Dynamic characteristics 31
16 Application information 32
17 Bare die outline 33
18 Handling information 38
19 Packing information 39
19.1 Wafer and Film Frame Carrier (FFC) information 39
20 Abbreviations 42
21 References 42
22 Revision history 43
23 Legal information 44
23.1 Data sheet status 44
23.2 Definitions 44
23.3 Disclaimers 44
23.4 Trademarks 45
24 Contact information 45
25 Tables 46
26 Figures 47
27 Contents 48

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2013. All rights reserved.

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 26 August 2013
Document identifier: PCF8564A