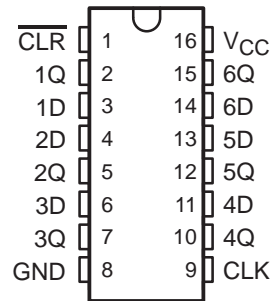


# SN74F174A HEX D-TYPE FLIP-FLOP WITH CLEAR

SDFS029B – D2932, MARCH 1987 – REVISED OCTOBER 1993

- Contains Six Flip-Flops With Single-Rail Outputs
- Buffered Clock and Direct Clear Inputs
- Applications Include:  
Buffer/Storage Registers  
Shift Registers  
Pattern Generators
- Fully Buffered Outputs for Maximum Isolation From External Disturbances
- Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs

D OR N PACKAGE  
(TOP VIEW)



## description

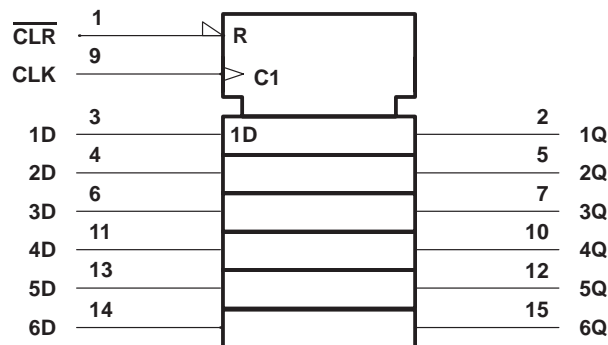
This monolithic, positive-edge-triggered flip-flop utilizes TTL circuitry to implement D-type flip-flop logic with a direct clear (CLR) input. Information at the data (D) inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

The SN74F174A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE  
(each flip-flop)

INPUTS			OUTPUT
CLR	CLK	D	Q
H	L	X	Q <sub>0</sub>
H	↑	H	H
H	↑	L	L
L	X	X	L

## logic symbol†

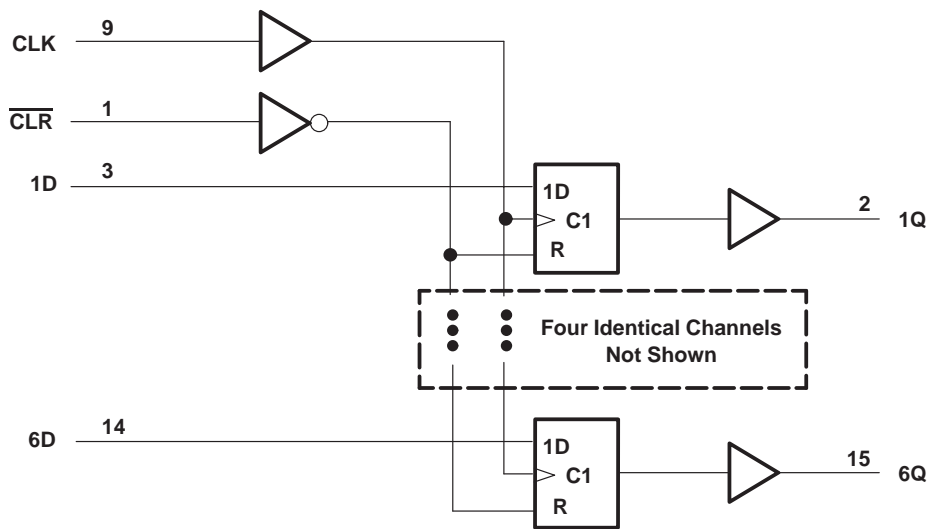


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74F174A  
HEX D-TYPE FLIP-FLOP  
WITH CLEAR

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–1.2 V to 7 V
Input current range	–30 mA to 5 mA
Voltage applied to any output in the high state	–0.5 V to $V_{CC}$
Current into any output in the low state	40 mA
Operating free-air temperature range	0°C to 70°C
Storage temperature range	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input-voltage ratings may be exceeded provided the input-current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{IK}$	Input clamp current			–18	mA
$I_{OH}$	High-level output current			–1	mA
$I_{OL}$	Low-level output current			20	mA
$T_A$	Operating free-air temperature	0		70	°C

# SN74F174A

## HEX D-TYPE FLIP-FLOP

### WITH CLEAR

SDFS029B – D2932, MARCH 1987 – REVISED OCTOBER 1993

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$			-1.2	V
$V_{OH}$	$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -1\text{ mA}$	2.5	3.4		V
	$V_{CC} = 4.75\text{ V}$ , $I_{OH} = -1\text{ mA}$	2.7			
$V_{OL}$	$V_{CC} = 4.5\text{ V}$ , $I_{OL} = 20\text{ mA}$		0.3	0.5	V
$I_I$	$V_{CC} = 5.5\text{ V}$ , $V_I = 7\text{ V}$			0.1	mA
$I_{IH}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 2.7\text{ V}$			20	$\mu\text{A}$
$I_{IL}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 0.5\text{ V}$			-0.6	mA
$I_{OS}‡$	$V_{CC} = 5.5\text{ V}$ , $V_O = 0$	-60		-150	mA
$I_{CCH}$	$V_{CC} = 5.5\text{ V}$ , See Note 2		30	45	mA
$I_{CCL}$	$V_{CC} = 5.5\text{ V}$ , See Note 3		39	55	mA

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTES: 2.  $I_{CCH}$  is measured with all outputs open, all data inputs and enable input at 4.5 V, and the clock input at 4.5 V after being momentarily grounded.

3.  $I_{CCL}$  is measured with all outputs open, all data inputs and enable input at 0 V, and the clock input at 4.5 V after being momentarily grounded.

### timing requirements

			V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		V <sub>CC</sub> = 4.5 V to 5.5 V, T <sub>A</sub> = MIN to MAX§		UNIT
			MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency		0	100	0	80	MHz
t <sub>w</sub>	Pulse duration	CLK high	4		4		ns
		CLK low	6		6		
		CLR low	5		5		
t <sub>su</sub>	Setup time before CLK↑	Data high or low	4.5		4.5		ns
		CLR high¶	5		5		
t <sub>h</sub>	Hold time after CLK↑	Data high or low	0.5		1		ns

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

¶ Inactive-state setup time is also referred to as recovery time.

### switching characteristics (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V}$ , $C_L = 50\text{ pF}$ , $R_L = 500\ \Omega$ , $T_A = 25^\circ\text{C}$			$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$ , $C_L = 50\text{ pF}$ , $R_L = 500\ \Omega$ , $T_A = \text{MIN to MAX}§$		UNIT
			MIN	TYP	MAX	MIN	MAX	
$f_{\text{max}}$			100	140		80		MHz
$t_{\text{PLH}}$	CLK	Any Q	2.7	4.5	8	2.7	9	ns
$t_{\text{PHL}}$			3.4	4.2	10	3.3	11	
$t_{\text{PHL}}$	$\overline{\text{CLR}}$	Any Q	4.2	6.3	14	4.2	15	ns

NOTE 4: Load circuits and waveforms are shown in Section 1.



## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74F174AD</a>	Obsolete	Production	SOIC (D)   16	-	-	Call TI	Call TI	0 to 70	F174A
<a href="#">SN74F174ADR</a>	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F174A
SN74F174ADR.A	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F174A
SN74F174ADRE4	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F174A
<a href="#">SN74F174AN</a>	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74F174AN
SN74F174AN.A	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74F174AN

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74F174ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74F174ADR	SOIC	D	16	2500	353.0	353.0	32.0

## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74F174AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74F174AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74F174AN.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74F174AN.A	N	PDIP	16	25	506	13.97	11230	4.32



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



## NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

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