

LVDS Interface LSI

35bit LVDS Receiver

5:35 DeSerializer

BU90R104

•General Description

The BU90R104 receiver operates from 8MHz to 112MHz wide clock range.

The BU90R104 converts the LVDS serial data streams back into 35bits of LVCMOS parallel data.

Data is transmitted seven times (7X) stream and reduce the cable number by 3(1/3) or less.

I/O Voltage range is 2.3 to 3.6V, so it is available for many products.

•Features

- 5 channels of LVDS data stream are converted to 35bits data of parallel LVCMOS level outputs.
- 30bits of RGB output data, 5bits of timing and control output data(HSYNC, VSYNC, DE, CTL1 and CTL2) are transmitted available.
- Support clock frequency from 8MHz up to 112MHz.
- Support consumer video format including 480i, 480P, 720P and 1080i as well.
- Support many kinds of PC video formats such as VGA, SVGA, XGA and SXGA.
- Provide 784Mbps per 1ch or 3.92Gbps per device throughput rate using 112MHz clock rate.

•Key Specifications

- Supply Voltage Range 2.30 to 3.60 V
- Operating Frequency 8 to 112 MHz
- Operating Temperature Range -40 to +85 °C

•Packages

- TQFP64V 12.0mm×12.0mm×1.0mm

•Applications

- Flat panel display
- Security camera, Digital camera
- Tablet

- User programmable LVCMOS data output triggering timing by using either rising or falling edge of clock.
- 30bit LVDS transmitter is recommended to use BU8254KVT.

●Block Diagram

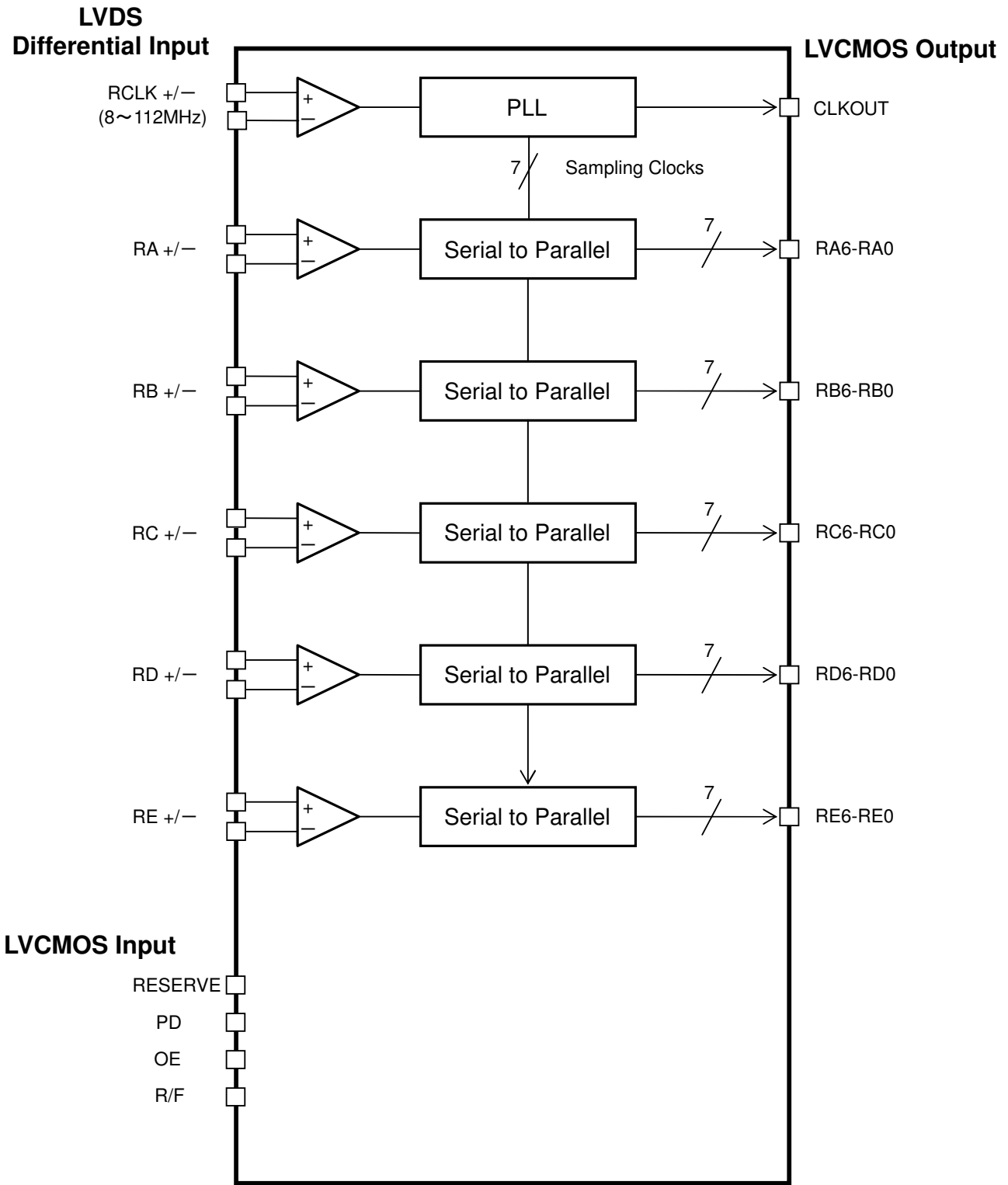


Figure 1. Block Diagram

●Pin Configuration

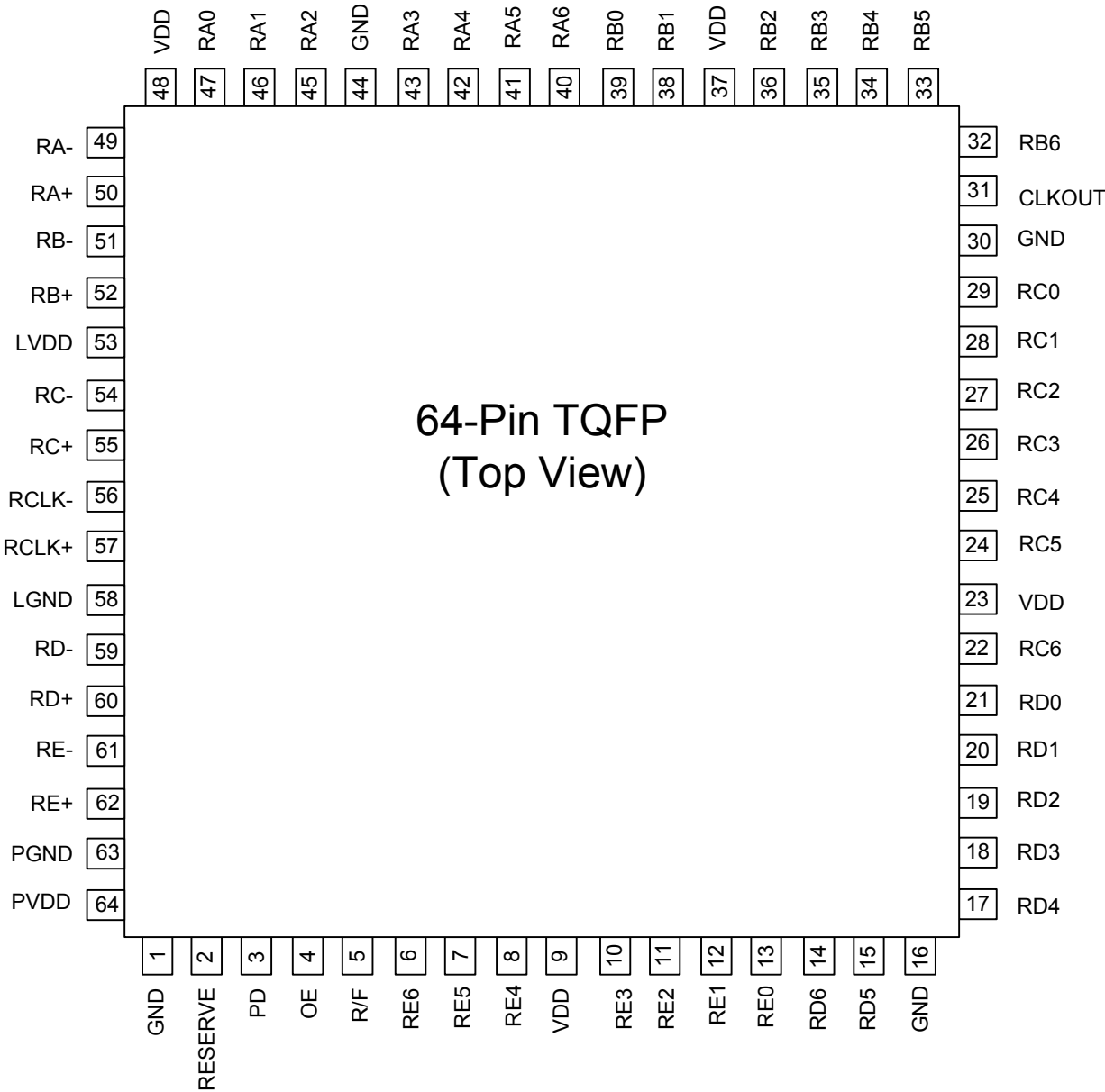


Figure 2. Pin Configuration (Top View)

●Pin Description

Pin Name	Pin No.	I/O	Description
RA+, RA-	50,49	LVDS Input	LVDS data input + : Positive input of LVDS data differential pair. - : Negative input of LVDS data differential pair.
RB+, RB-	52,51	LVDS Input	
RC+, RC-	55,54	LVDS Input	
RD+, RD-	60,59	LVDS Input	
RE+, RE-	62,61	LVDS Input	
RCLK+, RCLK-	57,56	LVDS Input	LVDS clock Input
RA6~RA0	40,41,42,43, 45,46,47	Output	LVCMOS data outputs.
RB6~RB0	32,33,34,35, 36,38,39	Output	
RC6~RC0	22,24,25,26, 27,28,29	Output	
RD6~RD0	14,15,17,18, 19,20,21	Output	
RE6~RE0	6,7,8,10, 11,12,13	Output	
RESERVE	2	Input	Reserved input must be "Low" for normal operation.
PD	3	Input	Power down input for the internal system. H : Normal operation. L : Power down (All output are "Low").
OE	4	Input	Power down input for the data output driver. H : Output enable (Normal operation). L : Output disable (All outputs are "Hi-Z").
R/F	5	Input	Select input pin for data output clock triggering edge. H : Output data is latched on rising edge. L : Output data is latched on falling edge.
VDD	9,23,37,48	Power	3.3V output driver and digital core power supply pin.
CLKOUT	31	Output	LVCMOS level clock output.
GND	1,16,30,44	Ground	Ground pin for both data output driver cells and the digital cores.
LVDD	53	Power	Power supply pin for LVDS core.
LGND	58	Ground	Ground pin for LVDS core.
PVDD	64	Power	Power supply pin for PLL core.
PGND	63	Ground	Ground pin for PLL core.

●Function Description

PD	R/F	OE	Data output (Rxn) ^(Note1)	Clock output
0	0	0	Hi-Z	Hi-Z
0	0	1	All fixed low	Fixed Low
0	1	0	Hi-Z	Hi-Z
0	1	1	All fixed low	Fixed Low
1	0	0	Hi-Z	Hi-Z
1	0	1	Data output	Output data is latched by falling edge of clock.
1	1	0	Hi-Z	Hi-Z
1	1	1	Data output	Output data is latched by rising edge of clock

(Note1): Rxn

x = A,B,C,D,E

n = 0,1,2,3,4,5,6

●Absolute Maximum Ratings

Parameter	Symbol	Ratings		Unit
		Min	Max	
Supply voltage	V_{DD}	-0.3	+4.0	V
Input voltage	V_{IN}	-0.3	$V_{DD}+0.3$	V
Output voltage	V_{OUT}	-0.3	$V_{DD}+0.3$	V
Storage temperature range	Tstg	-55	+125	°C

●Package power

Package	PD(W)	DERATING(W/°C) ^(Note2)
TQFP64V	0.7	0.007
	1.0 ^(Note3)	0.01 ^(Note3)

(Note2)At temperature $T_a > 25^{\circ}\text{C}$

(Note3)Package power when mounting on the PCB board.

The size of PCB board :70 × 70 × 1.6(mm³)

The material of PCB board :The FR4 glass epoxy board.(3% or less copper foil area)

●Recommended Operating Conditions

Parameter	Symbol	Ratings			Unit	Condition
		Min	Typ	Max		
Supply voltage	V_{DD}	2.3	3.3	3.6	V	VDD, LVDD, PVDD
Supply Noise Voltage	V_{NOZ}	-	-	0.1	V	
Operating temperature range	T_{opr}	-40	-	+85	°C	Clock frequency from 8MHz up to 90MHz
		0	-	+70	°C	Clock frequency from 90MHz up to 112MHz

•DC characteristics

Table 1. LVCMOS DC Specifications (VDD=2.3~3.6V, Ta=-40~+85°C)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
High Level Input Voltage	V_{IH}	$V_{DD} \times 0.8$	-	V_{DD}	V	
Low Level Input Voltage	V_{IL}	0.0	-	$V_{DD} \times 0.2$	V	
High Level Output Voltage	V_{OH}	$V_{DD}-0.5$	-	V_{DD}	V	$I_{OH}=-4mA$ (data) $I_{OH}=-8mA$ (clock)
Low Level Output Voltage	V_{OL}	0.0	-	0.4	V	$I_{OL}=4mA$ (data) $I_{OL}=8mA$ (clock)
Input Current	I_{INC}	-	-	± 10	μA	$0V \leq V_{IN} \leq V_{DD}$

Table 2. LVDS Receiver DC Specifications (VDD=2.3~3.6V, Ta=-40~+85°C)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Differential Input High threshold	V_{TH}	-	-	100	mV	$V_{OC}=1.2V$
Differential Input Low threshold	V_{TL}	-100	-	-	mV	$V_{OC}=1.2V$
Input Current	I_{INL}	-	-	± 25	μA	$V_{IN}=2.4V / 0V$ $V_{DD}=3.6V$
Common mode Voltage	V_{OC}	0.8	1.2	1.6	V	$V_{ID}=200mV$
Differential Input Voltage	$ V_{ID} $	100	-	600	mV	-

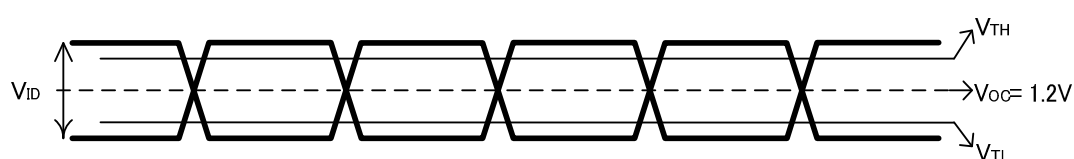


Figure 3. LVDS Receiver DC Specifications

•Supply Current

Parameter	Symbol	Limits		Unit	Conditions	
		Typ	Max			
Receiver supply current (Gray Scale Pattern)	I_{RCCG}	52	-	mA	$f_{CLKOUT}=90\text{MHz}$	$C_L=8\text{pF}$, $V_{DD}=3.3\text{V}$
Receiver supply current (Worst Case Pattern)	I_{RCCW}	95	-	mA	$f_{CLKOUT}=90\text{MHz}$	$C_L=8\text{pF}$, $V_{DD}=3.3\text{V}$
Receiver power down supply current	I_{RCCS}	-	10	μA	$\text{PD}=\text{L}$, $\text{OE}=\text{L}$	

Gray Scale Pattern

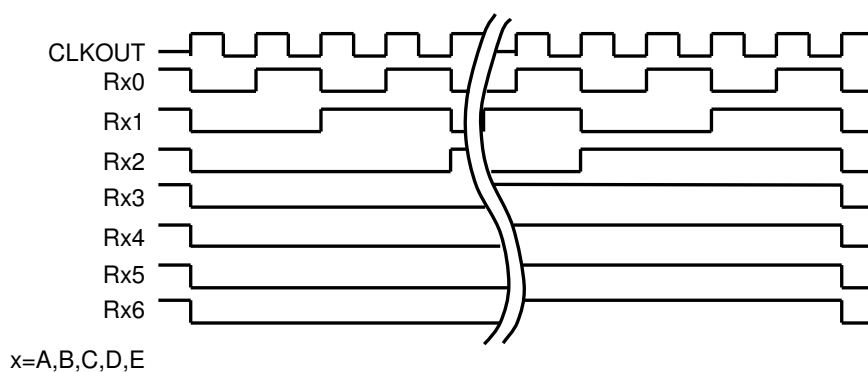


Figure 4. Gray Scale Pattern

Worst Case Pattern (Maximum power condition)

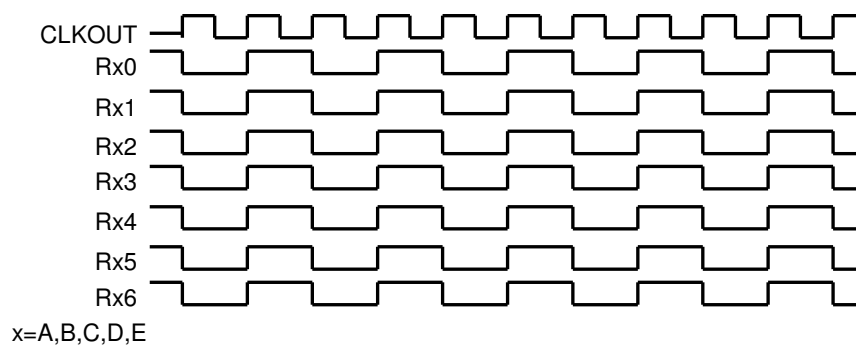


Figure 5. Worst Case Pattern

●AC characteristics

Table 3. Switching Characteristics (VDD=2.3~3.6V, Ta=-40~85°C)

Parameter	Symbol	Limits			Unit
		Min	Typ	Max	
CLKOUT Period	t_{RCP}	8.93	-	125	ns
CLKOUT "H" Time	t_{RCH}	-	$0.5t_{RCP}-1.0$	-	ns
CLKOUT "L" Time	t_{RCL}	-	$0.5t_{RCP}-1.0$	-	ns
LVC MOS Data Setup to CLKOUT	t_{RS}	$0.5t_{RCP}-1.4$	-	-	ns
LVC MOS Data Hold from CLKOUT	t_{RH}	$0.23t_{RCP}-1.0$	-	-	ns
LVC MOS Data Rise time	t_{TLH}	-	1.0	2.0	ns
LVC MOS Data Fall time	t_{THL}	-	1.0	2.0	ns
Input Data Position 0	t_{RIP1}	-0.25	0.0	+0.25	ns
Input Data Position 1	t_{RIP0}	$\frac{t_{RCIP}}{7}-0.25$	$\frac{t_{RCIP}}{7}$	$\frac{t_{RCIP}}{7}+0.25$	ns
Input Data Position 2	t_{RIP6}	$2\frac{t_{RCIP}}{7}-0.25$	$2\frac{t_{RCIP}}{7}$	$2\frac{t_{RCIP}}{7}+0.25$	ns
Input Data Position 3	t_{RIP5}	$3\frac{t_{RCIP}}{7}-0.25$	$3\frac{t_{RCIP}}{7}$	$3\frac{t_{RCIP}}{7}+0.25$	ns
Input Data Position 4	t_{RIP4}	$4\frac{t_{RCIP}}{7}-0.25$	$4\frac{t_{RCIP}}{7}$	$4\frac{t_{RCIP}}{7}+0.25$	ns
Input Data Position 5	t_{RIP3}	$5\frac{t_{RCIP}}{7}-0.25$	$5\frac{t_{RCIP}}{7}$	$5\frac{t_{RCIP}}{7}+0.25$	ns
Input Data Position 6	t_{RIP2}	$6\frac{t_{RCIP}}{7}-0.25$	$6\frac{t_{RCIP}}{7}$	$6\frac{t_{RCIP}}{7}+0.25$	ns
Phase Locked Loop Set Time	t_{RPLL}	-	-	10.0	ms
Clock Input Period	t_{RCIP}	8.93	-	125	ns

•AC Timing

■LVCMOS

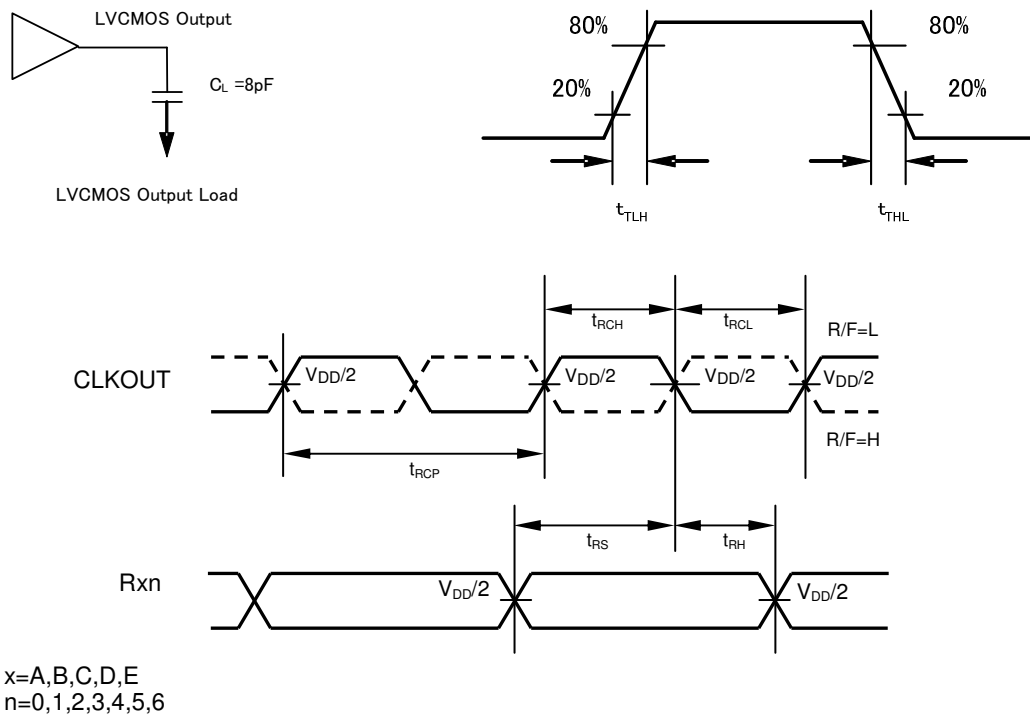


Figure 6. LVCMOS Output Timing

■Phase-Locked Loop Set Time

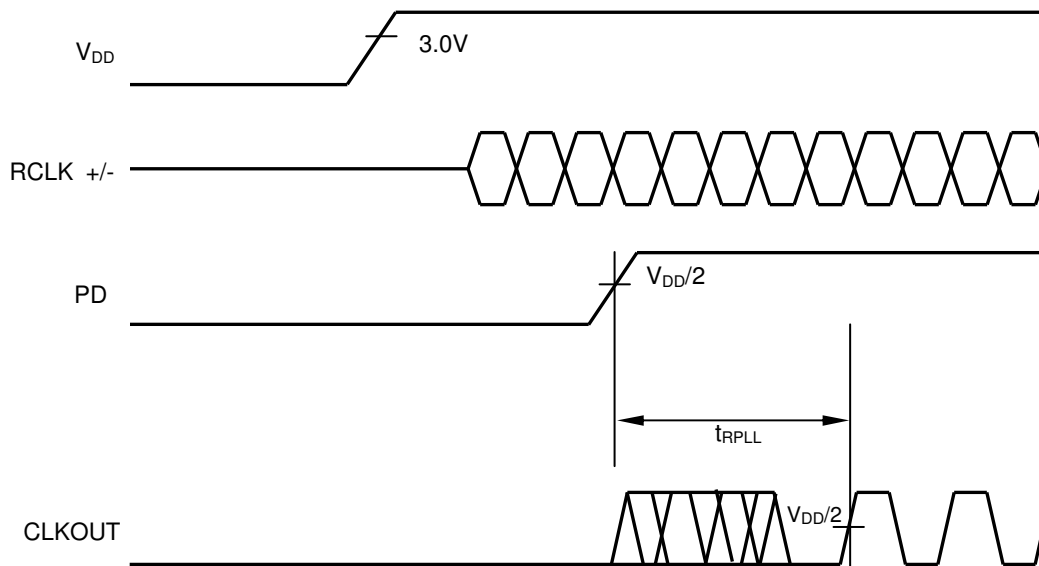


Figure 7. Phase-Locked Loop Set Time

●LVDS Data ,Clock Input Timing

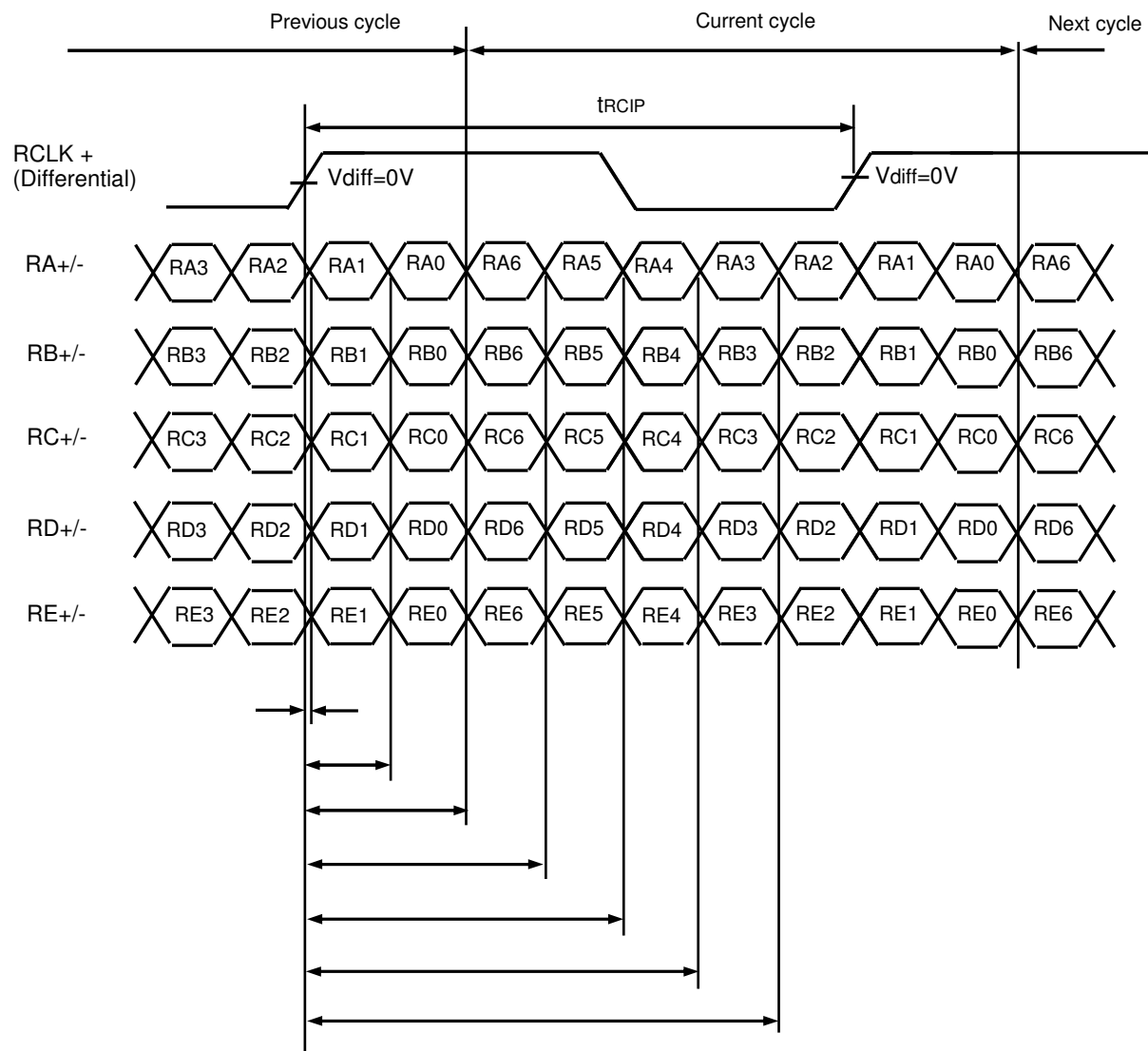


Figure 8. LVDS Data ,Clock Input Timing

●LVDS Data, Clock Input and LVCMOS Output Timing

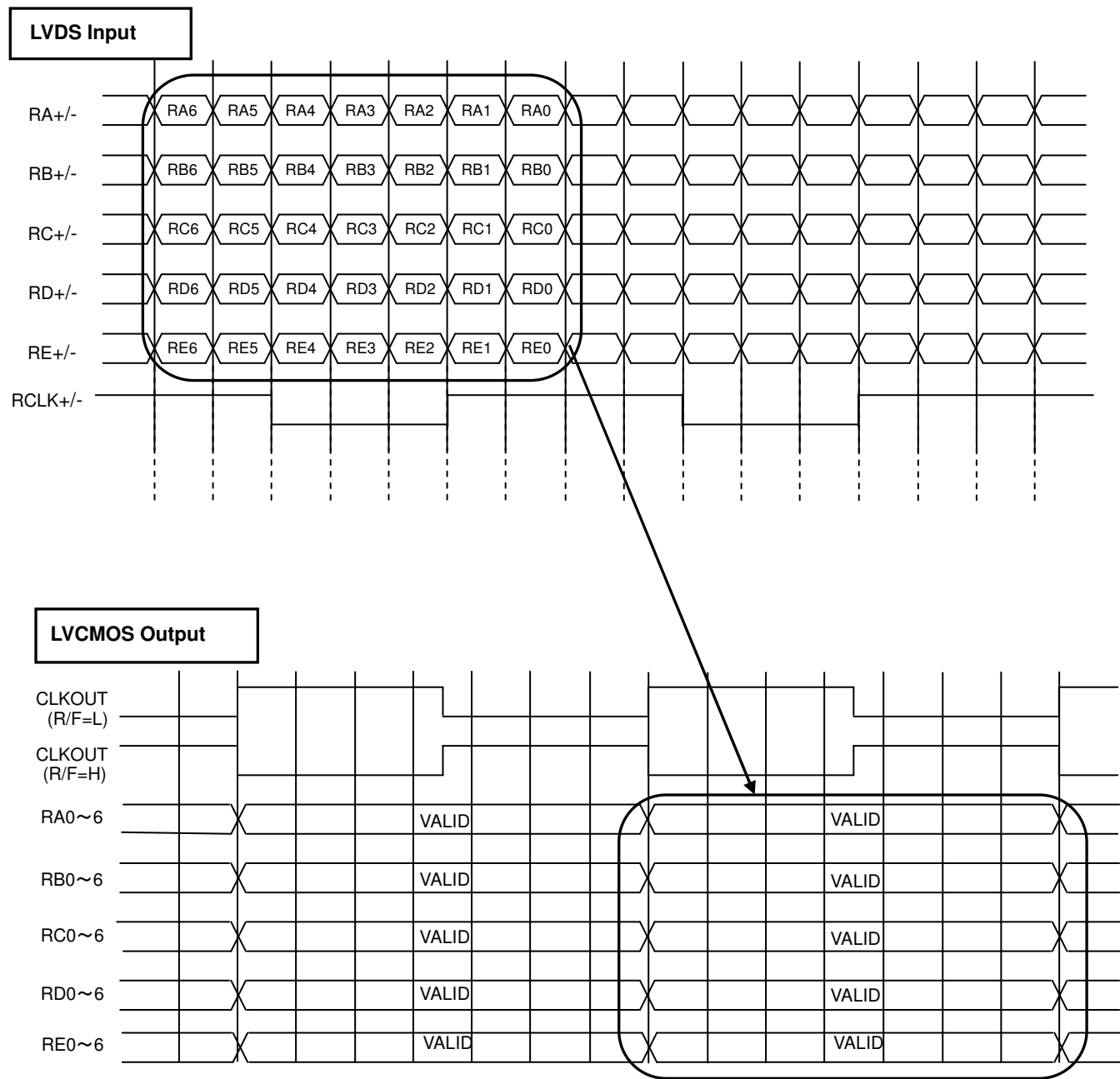


Figure 9. LVDS Data, Clock Input and LVCMOS Output Timing

●About the Power On Reset

Power on reset is not mandatory for this device.

(The PD pin should be set to high level when power on reset procedure is not used.)

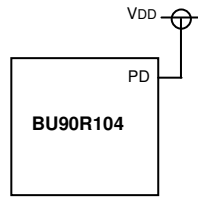


Figure 10. Terminal connection when power on reset is not used.

However, Power on reset procedure is strongly recommend for internal logic initialization by following two methods.

- ①The method of using CR circuit.
- ②The method of using external specific IC.

It is recommend to do enough examination for target application.

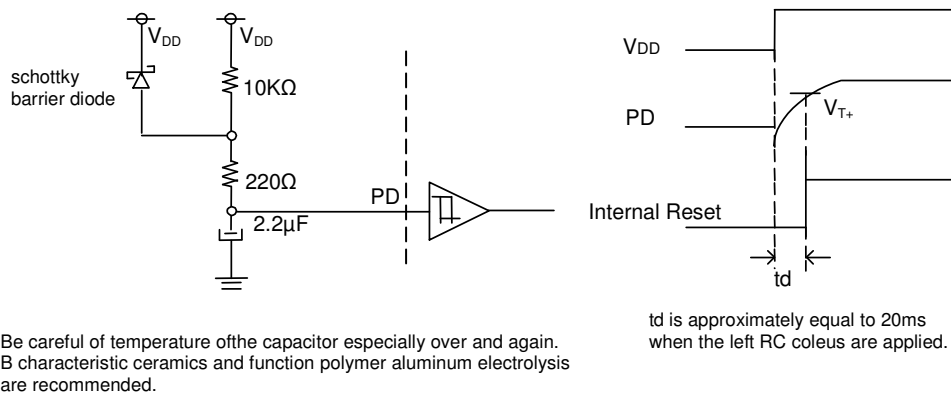


Figure 11. Power on reset by external a CR circuit

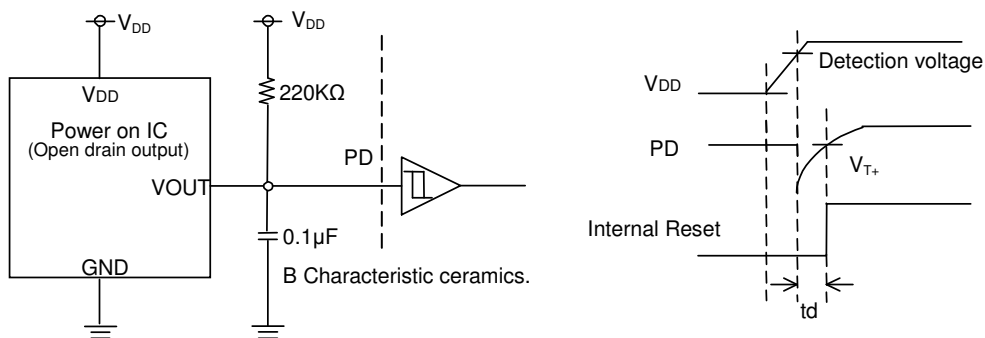


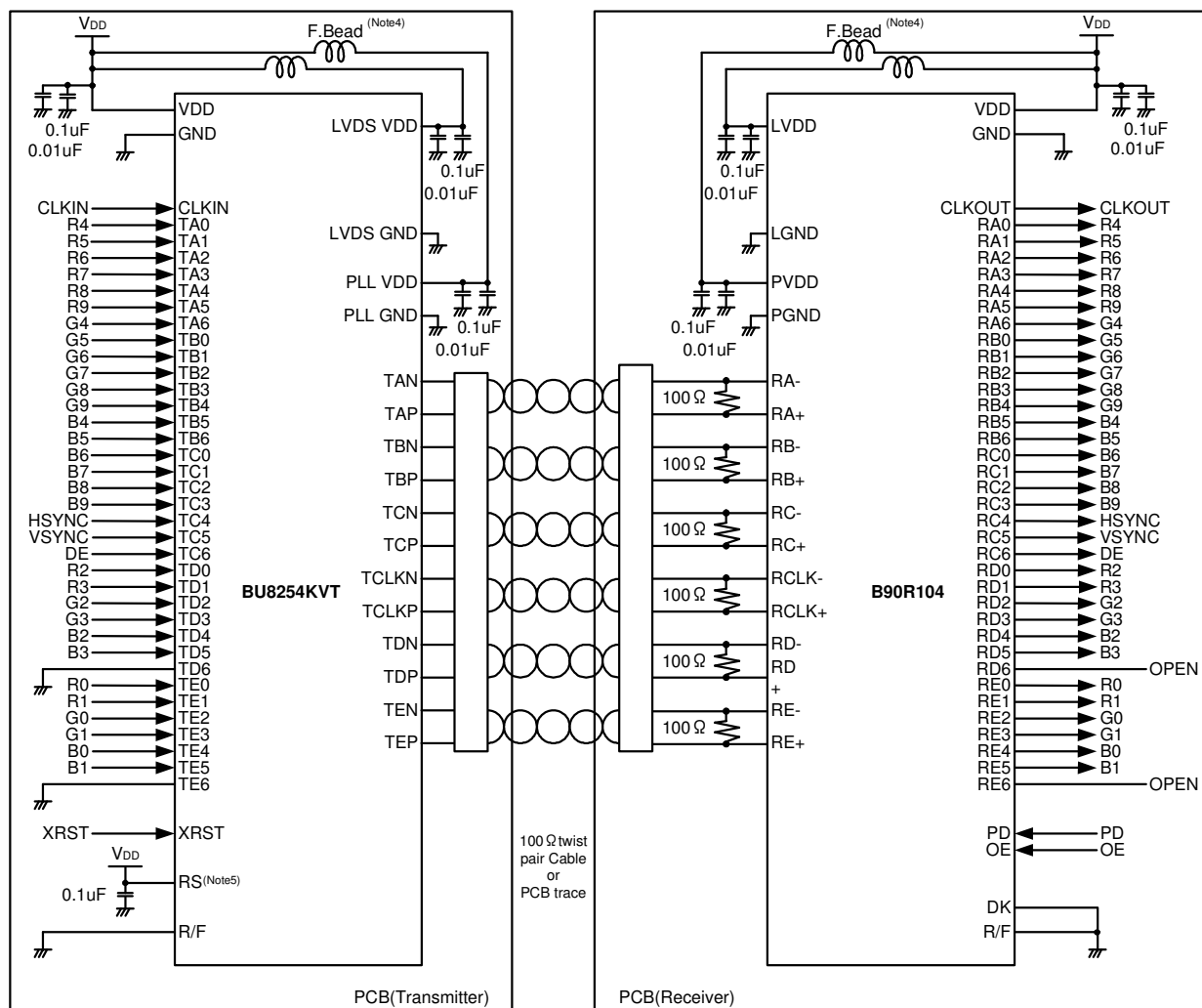
Figure 12. Power on reset by specific IC

●Application Circuit (10bit LVCMOS Level Input & LVCMOS Level Output)

Example:

BU8254KVT : LVCMOS level input/Falling edge/LVDS normal(350mV) swing output

BU90R104 : LVCMOS level output/Falling edge



(Note4) Recommended Parts:

F.Bead : BLM18A-Series (Murata Manufacturing Co.)

(Note5) If RS pin is tied to VDD, LVDS swing is 350 mV.

If RS pin is tied to GND, LVDS swing is 200 mV.

Figure 13. Application Circuit (10bit LVCMOS Level Input & LVCMOS Level Output)

●About the no used differential inputs

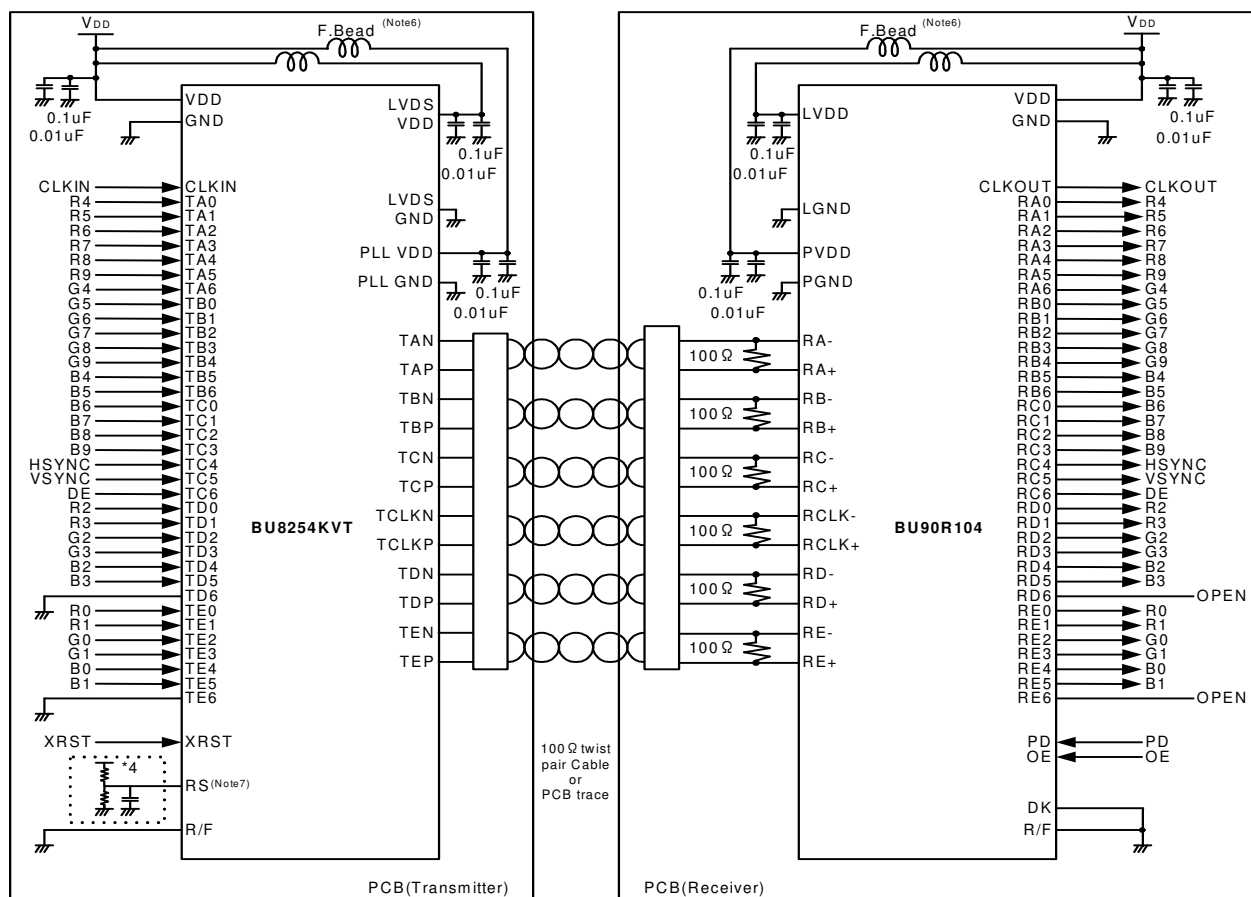
If there are no used differential inputs, be sure to set them into GND level.
The outputs are fixed High level, when differential inputs set GND.

•Application Circuit (10bit Small Swing Input & LVCMOS Level Output)

Example:

BU8254KVT : LVCMOS level input/Falling edge/LVDS normal(350mV) swing output

BU90R104 : LVCMOS level output/Falling edge

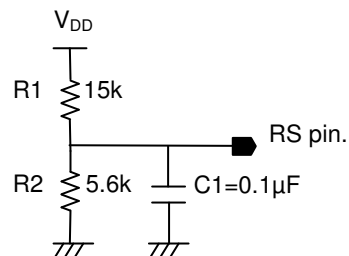


(Note6) Recommended Parts:

F.Bead : BLM18A-Series (Murata Manufacturing Co.)

(Note7) RS pin acts as VREF input pin when input voltage is set to half of high level signal input.

We recommend to locate by-pass condenser near the RS pin.



Example for LVTTTL(1.8V input): (R1,R2)=(15k Ω, 5.6k Ω)

Figure 14. Application Circuit (10bit Small Swing Input & LVCMOS Level Output)

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If there are any differences in translation version of this document formal version takes priority

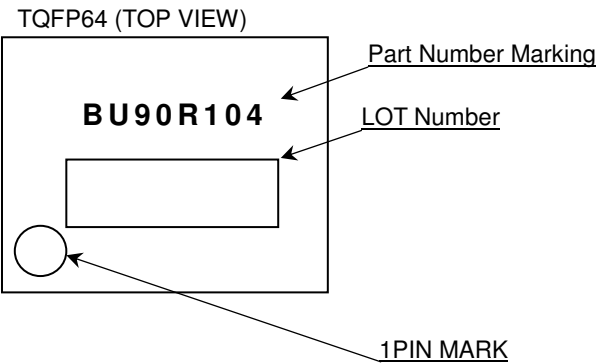
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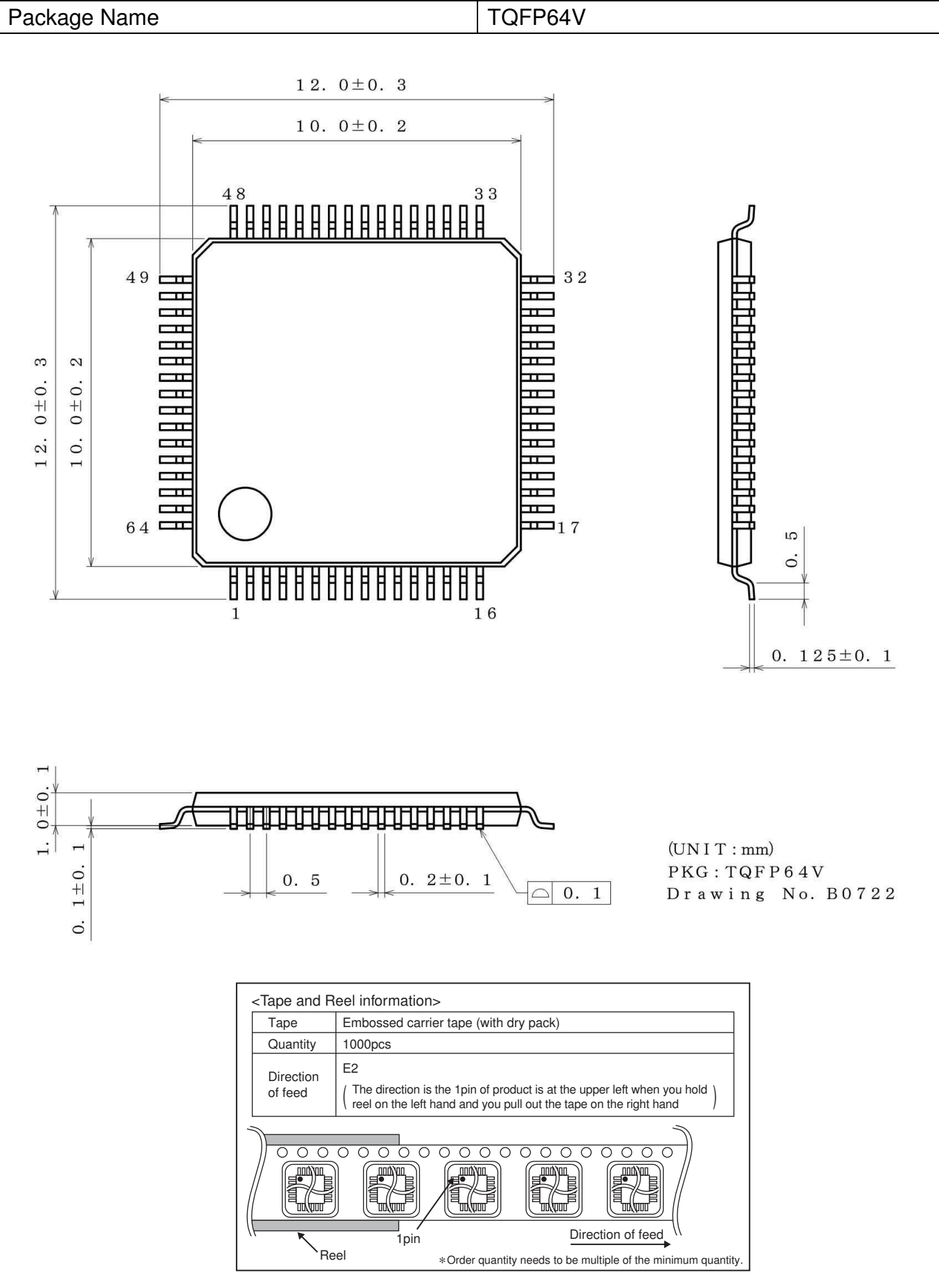
●Ordering part number

<table><tr><td>B</td><td>U</td></tr></table>	B	U	<table><tr><td>9</td><td>0</td><td>R</td><td>1</td><td>0</td><td>4</td></tr></table>	9	0	R	1	0	4	-	<table><tr><td>E</td><td>2</td></tr></table>	E	2
B	U												
9	0	R	1	0	4								
E	2												
Part No.	Part No. 90R104 Package TQFP64V		Packaging and forming specification E2: Embossed tape and reel										

●Marking Diagram



Physical Dimension, Tape and Reel Information



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