Unique and Novel Uses for ON Semiconductor's New One-Gate Family

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APPLICATION NOTE

INTRODUCTION

One–Gate logic devices have been in use for several years, and are nothing more than single–gate derivatives of their multi–gate cousins. Initial offerings were pioneered in Japan, to help solve particular problems the design community had encountered. Earlier, traditional ICs were packaged in 14 and 16 pin Dual–in–line Packages (DIPs), and the goal of the IC manufacturer was to get as much functionality as possible into a single–package device. Double, triple, quadruple, and quintuple versions of simple logic functions became the norm. The enormously successful 7400–TTL/LS logic family of standard bipolar logic IC's became the industry standard for nearly 20 years. Ceramic, and later plastic, dip packages became a staple item for logic designers. New, Small–Outline–Integrated–Circuit (SOIC) packages began to replace DIPs as packaging technologies evolved.

As CMOS process technologies emerged and began to gain popularity, the 4000 series CMOS family also followed industry trends. The 4000 series, was not only a low power family, but was also low speed. Improvements in CMOS technology accelerated process development efforts. The resulting products were faster than older bipolar families, and have become standards within the design community. These newer product families tended to be offered only in SOIC and smaller packages. The result of all the improvements in CMOS technology is that the older bipolar families are now rarely used, except for legacy designs. Families such as VHC now offer lower power, and higher speed and drive capabilities than LSTTL, at the same or lower cost.

The Japanese electronics industry is responsible for the majority of the world's consumer electronics designs. One trend in this area has been to get as much function into as small a space as possible, while conserving power. Owing to the huge number of units consumed, Japanese designers rely on techniques different from that of the rest of the world. To turn new designs quickly, Japanese circuit designers created an infrastructure to support rapid design of moderate sized gate arrays, as well as Application Specific Standard Products (ASSP). Previously designed gate arrays or ASSPs often needed one bit of buffering, logic, or switching in order to make the circuit usable in a new system design. Often there was not enough room to add an additional logic element on the chip and still keep the board size small. The designer was faced with having to re–design the entire chip or to add additional IC components to the board layout to accomplish the required task.

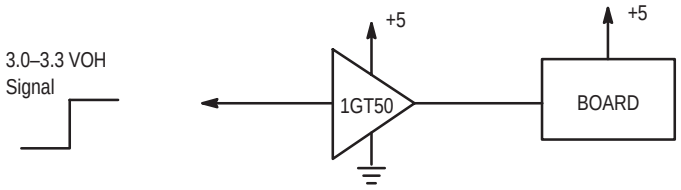
A solution to this dilemma was to use One–Gate designs, initially offered in the SOT–23, 5–pin package, and later in the even smaller SOT–353 (SC88A). The latter package takes up only 4.2 mm^2 of board space, and less than the area of a TSSOP–20 pin device. One–Gate products, now fabricated in a .6μ advanced high–speed CMOS technology, are very fast, with < 4 nsecs gate delays, and enough drive (8 mA) to support most typical applications. The package is so small, that it fits "in–line" with the trace that it is mounted on. The One–Gate device is performing only one function at a time. Because One–Gates can be mounted right where they are needed, additional direct benefits to the design are lower "ground bounce" effects, smaller number of de–coupling component requirements, shorter signal routing lines, and a significant reduction in overall board space.

One–Gate products are beginning to be universally recognized for the value they bring to a design. The design may be a consumer oriented portable product, or a larger computing system such as a workstation. The benefits of improved routing, reduced cross–talk effects, cleaner system signals, and elimination of previously required signal "clean–up components", are recognized as extremely important to overall system performance, and the use of One–Gate devices is expected to increase dramatically in the future.

Typical Application Cases:

Example #1

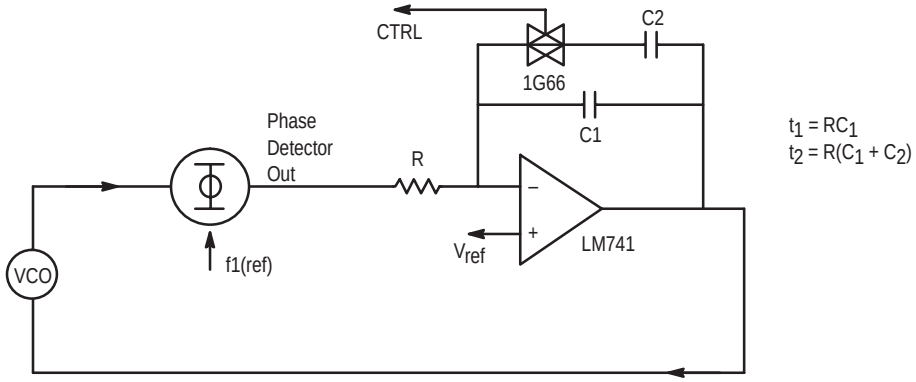
Problem: Interface a 3.0 Volt logic level serial input to a 5.0 Volt older board.
Solution: The 1GT50 provides an interface with no inversion



Discussion: This product is a new function in the industry standard family of One–Gate products. The 1GT50 operates at 5.0 Volts and interfaces seamlessly with 3.0 Volt logic levels. No resistors or other additional components are necessary. The device occupies minimum board space and contributes almost no loading (<10 Pf). It also provides up 8 mA of drive with minimum noise and ground bounce and only a small signal delay ($\sim$4 ns, depending upon load).

Example #2

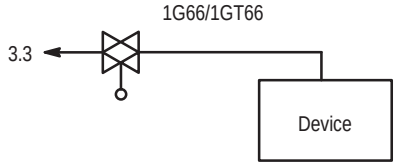
Problem: A Phase Locked Loop for a motor driver needs a fast attack time with a long steady state time constant.
Solution: The 1GT66 or 1G66 (standard industry functions) One–Gate Analog switches.



Discussion: Designers are familiar with this function in multi–gate families. Either of these two One–Gate devices, the 1GT66 or 1G66 (depending on system requirements), allows the designer to specify two time constants. The first time constant is selected for fast attack with perhaps 15% overshoot. The second time constant delivers maximum stability and minimum ripple. The analog switch takes up almost no room on the board and only requires one resistor and two capacitors, as well. When the analog switch is turned "on," it selects the time constant equal to: $\tau = 2\pi (C_1+C_2)$. The longer time constant is effective a few nanoseconds after being switched "on".

Example #3

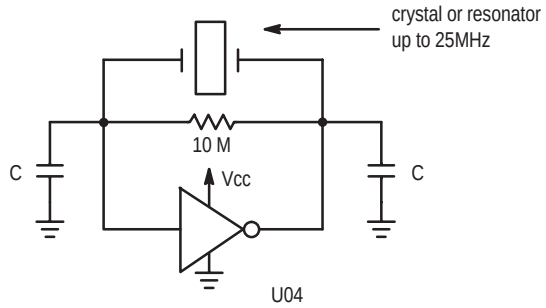
Problem: How to switch a low power 3.3 Volt device "on" from a TTL level source.
Solution: Use a 1G66 One–Gate with V_{dd} connected to the supply voltage of 3.3 volts as a high–side switch.



Discussion: The control pin on the industry standard 1G66 is over–voltage tolerant and may be driven by a 5.0 Volt logic driver. The switch will offer only 15 ohms of resistance, resulting in a drop of 0.15 Volts with a 10 mA load. This function can turn on a local oscillator, RF stage, small audio output, etc. This low cost switch provides an interface between the 5.0 Volt portion of the system and high–side switching. The One–Gate device occupies only 4.2 mm^2 of board space and requires no external resistors or capacitors.

Example #4

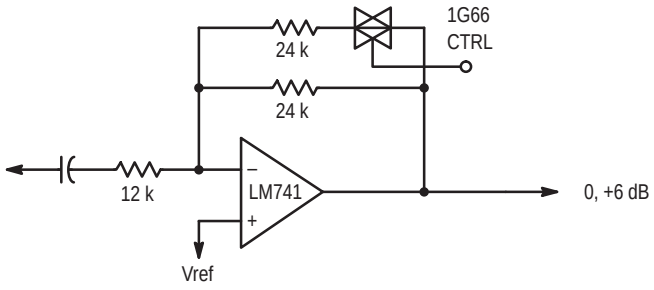
Problem: How to make a low–cost/area crystal–ceramic resonator oscillator
Solution: The industry standard One–Gate device, the 1GU04 unbuffered inverter.



Discussion: The 1GU04 makes a perfect oscillator for any fundamental mode crystal. A 10 Meg Ohm resistor placed from output to input puts the inverter in a Class–A state. The crystal manufacturer should determine the capacitor value. The Oscillator should function up to the maximum value of a fundamental crystal (~25 MHz). The designer can use an overtone crystal to achieve higher frequencies. The designer should follow recommendations of the crystal manufacturer. If buffering is required, any of the VHC one–gates or multi–gate buffers or inverters will perform admirably.

Example #5

Problem: How to create a dual gain audio amplifier with either 0 dB gain or +6 dB gain.
Solution: The use of an operational amplifier with selectable feedback resistance provides constant input and output impedance. Use a single gate analog switch to select/deselect resistors and provide either unity gain or +6 db.

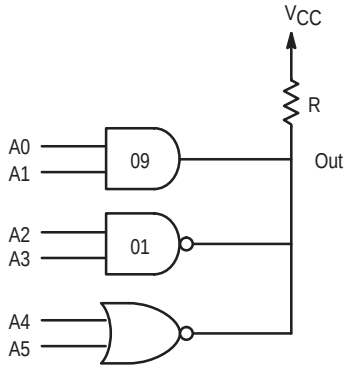


Example #6

Problem: For many years, programmable array logic (PAL's) were used to perform complex logic operations on multiple signals. In the wireless/hand–held world, PAL's consume too much power. An additional problem arises if the designer needs a complex set of "combinational" logic.

Solution: Depending on the number of terms needed, open drain single gate devices can provide an excellent solution. Open drain gates allow the outputs to be "wired–OR'ed" together so that the OR function is not only free, but is very low power, uses up very little space, and adds practically zero delay into the signal path. The following is an illustration of a complex function:
OUT = (A0 x A1) + (A2 x A3) + (A4 + A5)

Using three open drain One–Gate devices (09, 01, and 03), wire–OR the outputs. To attempt to accomplish this function with a PAL would be overkill in both power and board space. Using multi–gate logic would require four devices and >50 mm^2 of board space. The use of open drain devices provides a perfect solution, consuming only 13mm^2 of board space. Signal propagation delays would be <7ns, with minimum power consumption (determined by the value of R).



Out = (A0*A1) + (A2*A3) + (A4*A5)

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