Evaluation Board AD976/AD976A 16-Bit,100/200 kSPS ADC

Preliminary Technical Data EVAL-AD976/AD976ACB

FEATURES

- **Versatile Analog Signal Conditioning Circuitry**
- **Jumper Selectable Analog Input Ranges**
- **Analog and Digital Prototyping Area**
- **Flexible Power and Grounding Schemes**
- **On-Board Reference and Buffers**
- **16-Bit Parallel Buffered Outputs**
- **Ideal For DSP and Data Acquisition Card Interfaces**
- **EVAL-CONTROL BOARD Compatibility**
- **PC Software for Control and Data Analysis**

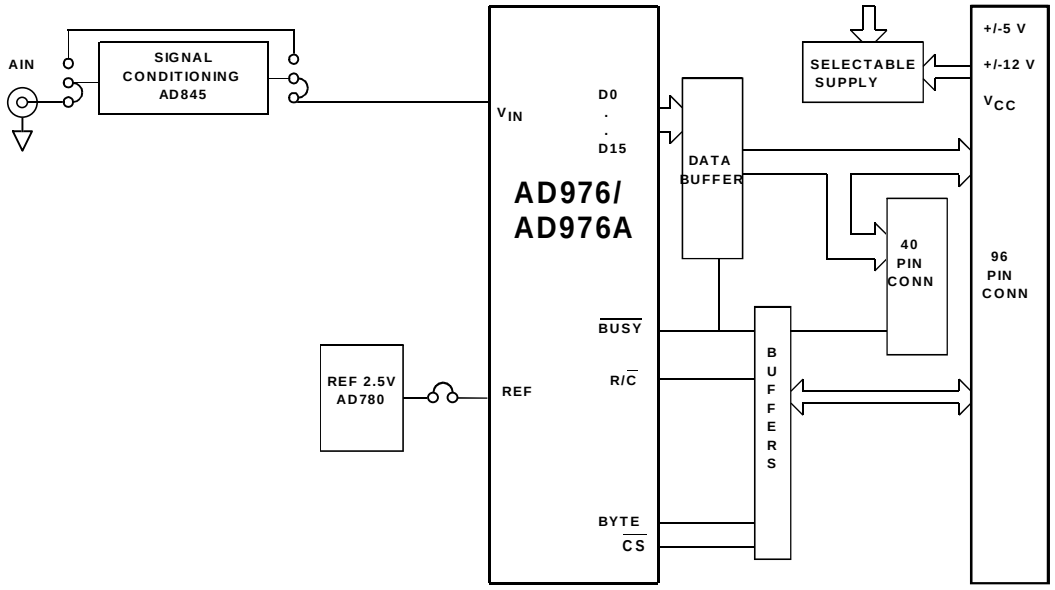
GENERAL DESCRIPTION

The EVAL-AD976/AD976ACB is an evaluation board for the AD976/AD976A 16-bit ADC. The AD976/AD976A is capable of a 100/200 ksps throughput rate, operates from a single +5V supply and uses a parallel interface.
The AD976/AD976A evaluation board is designed to demonstrate the ADC's performances and to provide an easy to understand interface for a variety of system applications. A full description of the AD976/AD976A is available in the AD976/AD976A data sheet and should be consulted when utilizing this evaluation board.

The EVAL-AD976/AD976ACB is ideal for use as either a stand-alone evaluation board to interface with customer application, or with the EVAL-CONTROL BOARD, also available from Analog Devices. The design offers the flexibility of applying external control signals and is capable of generating 16-bit conversion results as parallel buffered outputs.

On-board components include an AD780, a +2.5V ultra high precision bandgap reference, an AD845 signal conditioning op-amp, and digital buffers. The board interfaces with a 96-way connector for the EVAL-CONTROL BOARD, and a 40-pin IDC connector for parallel output data. BNC connector is provided for the low noise analog signal source and BNC connector is provided for an external read/convert input.

FUNCTIONAL BLOCK DIAGRAM



PRELIM. F

One Technology Way, P.O. Box 9106, Norwood. MA 02062-9106, U.S.A.
Tel: 617/329-4700 **Fax: 617/326-8703**

OPERATING THE EVAL-AD976/AD976ACB

The EVAL-AD976/AD976ACB is a four-layer board carefully laid out and tested to demonstrate the specific high accuracy performance of the device. Figure 2 shows the schematics of the evaluation board. Figure 3 shows the component side silk-screen. The layouts of the board are given in :
Component layer - Figure 4
Power layer - Figure 5
Ground layer - Figure 6
Circuit side layer - Figure 7.

The EVAL-AD976/AD976ACB is a flexible design that enables the user to choose among many different board configurations. The available test points are listed in Table I and a description of each selectable jumper is listed in Table II.

The evaluation board schematic shows the factory installed jumper selections. The EVAL-AD976/AD976ACB is configured to be powered through the EVAL-CONTROL BOARD, the AD780 external reference applied to the REF pin, the signal conditioning op-amp set with a gain of -2 and on-board R/$\overline{C}$ generation used. Conversion data is available at the outputs of two 8-bit registers, U4 and U5 for parallel transfer via the 40-pin IDC connector, P5 or the 96-pin DIN connector, P4. The AD976/AD976A conversion control inputs, R/$\overline{C}$ and $\overline{CS}$, are configured to provide continuous conversions with the $\overline{CS}$ input is set low and the R/$\overline{C}$ input connected to the output of the counter, U7.

The EVAL-AD976CB and EVAL-AD976ACB differ only by the frequency of the oscillator U8 which is respectively 1MHz and 2MHz for the AD976 and the AD976A.

Power Supplies and Grounding

The EVAL-AD976/AD976ACB power supply connectors and ground planes are configured to provide the multiple power and grounding configurations used in most system applications.

The evaluation board ground plane is separated into two sections: a plane for the digital interface circuitry and an analog plane for the AD976/AD976A and its analog input and external reference circuitry. To attain high resolution performance the board was designed to ensure that all digital ground return paths do not cross the analog ground return paths.

The EVAL-AD976/AD976ACB has three power supply blocks: a single 5V supply for the AD976/AD976A V_{ANA} and V_{DIG} power pins (P1), a 5V supply for the digital interface circuitry (P2), and a +/-12V supply for the analog signal conditioning circuitry (P3). All supplies are decoupled to ground with 10 µF tantalum and 0.1 µF ceramic capacitors. Figure 1 shows the recommended power connection diagram.

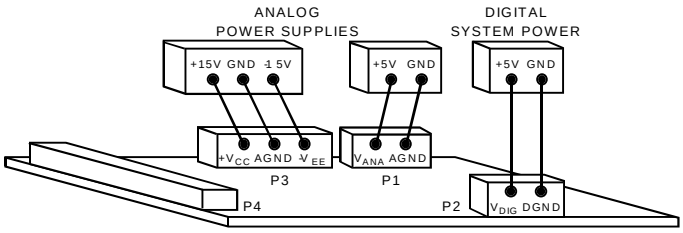


Figure 1. Power Connection Diagram

Assembly Options

The AD976 and AD976A on the evaluation board is configured for offset adjust and operation with the AD780 external reference. Remove the header shunt from JP4 to operate the AD976/AD976A with its internal reference. Connecting the header shunt to position A of JP4 allows trim adjusment of the AD976/AD976A gain error.

Offset adjustment is provided with the resistor, R6, connected as shown in the evaluation board schematic, and in Figure 7 of the datasheet.

To operate the AD976 without offset adjustment remove the 33.2 kΩ resistor, R6, and install it into the open location for resistor, R5.

To operate the AD976A without offset adjustment remove the 33.2 kΩ resistor, R6, and connect 66.4 kΩ resistor between V_{IN}, pin 1, and V_{ANA}, pin 27 of the AD976A.

TABLE I. EVAL-AD976CB/AD976ACB Test Points

Test Point	Available Signal
TP1	VANA
TP2	AGND
TP3	+VS
TP4	-VS
TP5	VDIG
TP6	SYSTEM DGND
TP7	AIN GND
TP8	VIN
TP9	CAP
TP10	AGND2
TP11	DGND
TP12	$\overline{BUSY}$
TP13	R/$\overline{C}$ GND

EVAL-CONTROL BOARD Interface

The EVAL-AD976/AD976ACB interfaces to the EVAL-CONTROL BOARD through the 96-way connector.

RUNNING THE EVAL-AD974CB SOFTWARE

Software Description

The EVAL-AD976/AD976ACB comes with software for analyzing the AD976/AD976A. Through the EVAL-CONTROL BOARD one can perform a histogram to determine code transition noise, and Fast Fourier Transforms (FFT's) to determine the Signal-to-Noise Ratio (SNR), Signal-to-Noise-plus-Distortion (SNRD) and Total-Harmonic-Distortion (THD). The front-end PC software has three screens as shown in Figure 8, 9 and 10. Figure 8 is the Setup Screen where sample rate, number of samples are selected. Figure 9 is the Histogram Screen, which allows to display the code distribution for DC input and computes the mean and standard deviation. Figure 10 is the FFT Screen, which performs an FFT on the captured data, computes the Signal-to-Noise Ratio (SNR), Signal-to-Noise-plus-Distortion (SNRD) and Total-Harmonic-Distortion (THD).

Software Installation

The EVAL-AD976/AD976ACB software runs under DOS 4.0 or higher. It requires a minimum of 386-based machine, with 500kB of base RAM and 500kB of free hard disk space and uses the COM1 serial port. It may be necessary to disable some TSR's (network TSR's for example) or load them into high memory, to ensure that adequate base memory is available. Operation under Windows 3.x is not recommended since the Windows COM interrupt can interfere with communication between the PC and the EVAL-CONTROL BOARD. For PC running under Windows 95, it is recommended to shut-down it using the option restart the computer in MS-DOS mode.

The EVAL-AD976/AD976ACB software installation process is:

- Create a new directory on the main PC drive and label this "AD976".

- Copy into this directory all files contained in the disk which accompanies the EVAL-AD976/AD976ACB.

- The software can be started typing "AD976".

Note that the Mouse Driver on the PC should be enabled before running the software. If this has not been loaded then the program will not run.

TABLE II. JUMPER DESCRIPTION

Jumper Designation	Function
JP1,2	These two jumpers are used to select the configuration of the op amp, U2. To configure the op-amp as an inverter install the header shunt of JP1 to position A and JP2 to position B. To configure the op-amp as a follower install the header shunt of JP2 to position A, and JP1 to position B.
JP3	The position of JP3 determines the source of the analog signal for the AD976/AD976A. To apply the AD976/AD976A analog input signal directly from the BNC connector, J1; set JP3 to position A. To select the output of the op-amp set JP3 to position B.
JP4	With JP4 set to position A, the AD976/AD976A uses its own internal reference but allows for an external gain adjustment through R8. Placing JP4 in position B selects the AD780 for use as an external reference. To use the AD976/AD976A internal reference without gain adjustment remove the shunt header of JP4.
JP5	The R/$\overline{C}$ control input to the AD976/AD976A can be driven from either an external source or an onboard clock source. With JP7 set to position A; JP5 selects the control input for the R/$\overline{C}$ pin of the AD976/AD976A. Set JP5 to position A to use the on-board square wave from the 74HC190 or set JP5 to position B to select an external R/$\overline{C}$ waveform from the BNC connector, J2.
JP6	Install JP6 to set the AD976/AD976A $\overline{CS}$ input to a logic low. Remove this jumper to allow an external $\overline{CS}$ input to be applied.
JP7	JP7 selects either one of the two external R/$\overline{C}$ control inputs from JP5 or the R/$\overline{C}$ output from the EVAL-CONTROL BOARD.
JP8	Install the header shunt of JP8 to position A to set the AD976/AD976A BYTE input to a logic low. Select position B to control the BYTE input to the AD976/AD976A by the EVAL-CONTROL BOARD.
JP9	The header shunt for JP9 should be installed when the power to the EVAL-AD976CB/AD976ACB is supplied from the EVAL-CONTROL BOARD or when a single power supply is applied to the EVAL-AD976/976ACB. Otherwise the shunt header should be left unconnected.
JP11	JP11 selects the digital power source for the AD976/AD976A. Install the shunt header to provide power from a +5 V supply (VANA) from the power block, P1. Remove the shunt header to apply a separate external +5 V supply for the VDIG pin of the AD976/AD976A or to monitor the current to the ADC.
JP12	JP12 is used to connect the +5V analog power plane, VANA, to the power plane for the digital interface circuitry, VDIG. Install the jumper to provide a single+5V external supply to all of the on-board components. Removal of this header shunt seperates the power supply for the AD976/AD976A from the supply of the digital interface circuitry. When used in conjunction with the EVAL-CONTROL BOARD, JP12 must be unconnected; VANA is the analog power, +5V, and VDIG is digital interface circuitry power, VCC, provided seperately from the EVAL-CONTROL BOARD.
JP14	The header shunt for JP14 connects the ground plane of the AD976/AD976A to the digital interface circuitry ground plane. Connect the header shunt on JP14 only when JP12 is installed.
JP15	JP15 selects the analog power source for the AD976/AD976A. Install the shunt header to provide power from a +5V supply (VANA) from the power block, P1. Remove the shunt header to apply a seperate external +5V supply for the VANA pin of the AD976/AD976A or to monitor the current to the ADC.
JP16,17	JP16 and JP17 select the power source for the analog amplifier. Position B allows an external bipolar power supply to be connected to the 3-pin power block P3. Position A selects the +/-12 V supply provided at the 96-pin connector, P4.

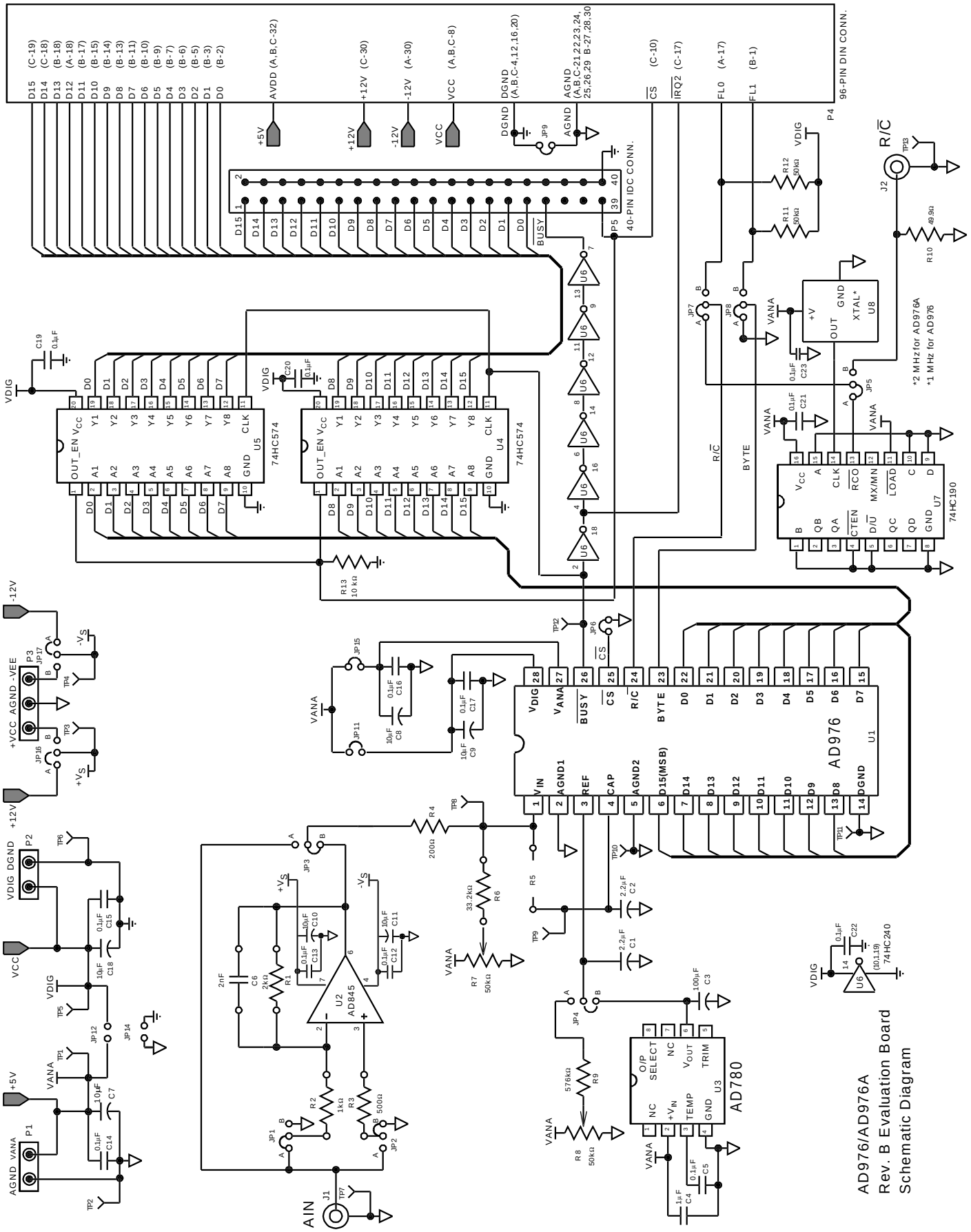


Figure 2. Schematic

Figure 3. Component side silkscreen (Not to Scale).

Figure 4. Component side (Not to Scale).

Figure 5. Power Layer (Not to Scale).

Figure 6. Ground layer (Not to Scale).

Figure 7. Circuit Side (Not to Scale).

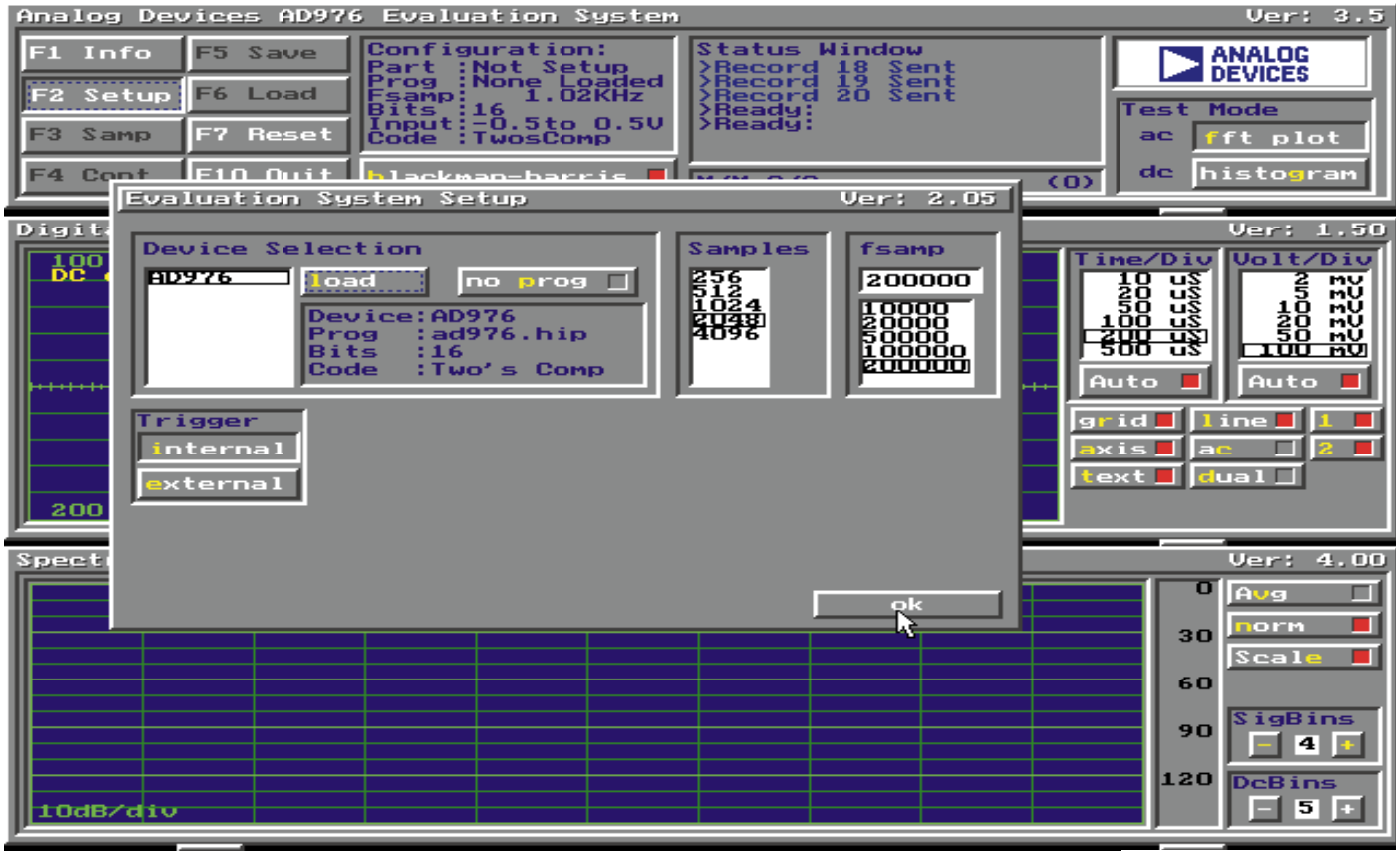


Figure 8. Setup screen.

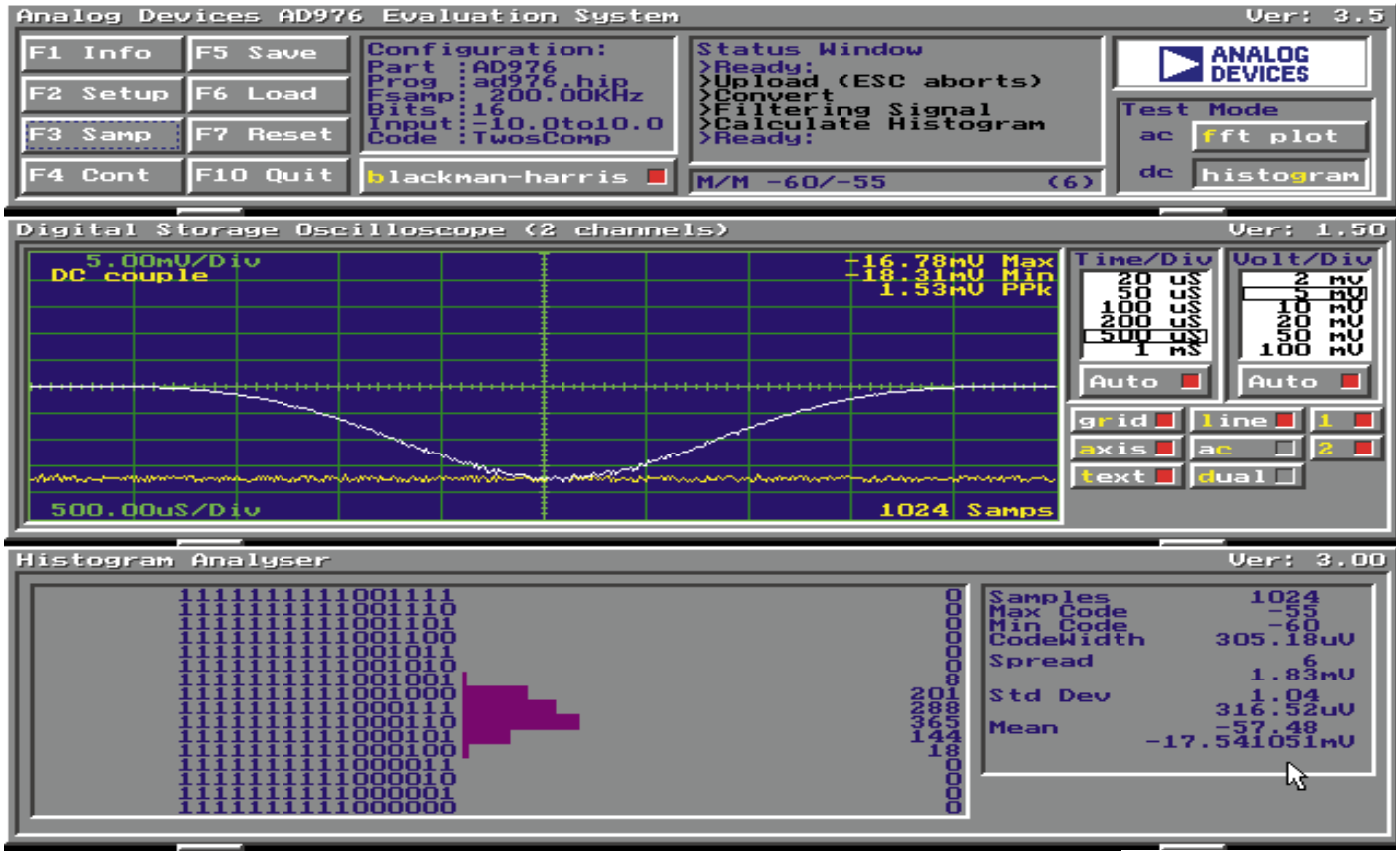


Figure 9. Histogram screen.

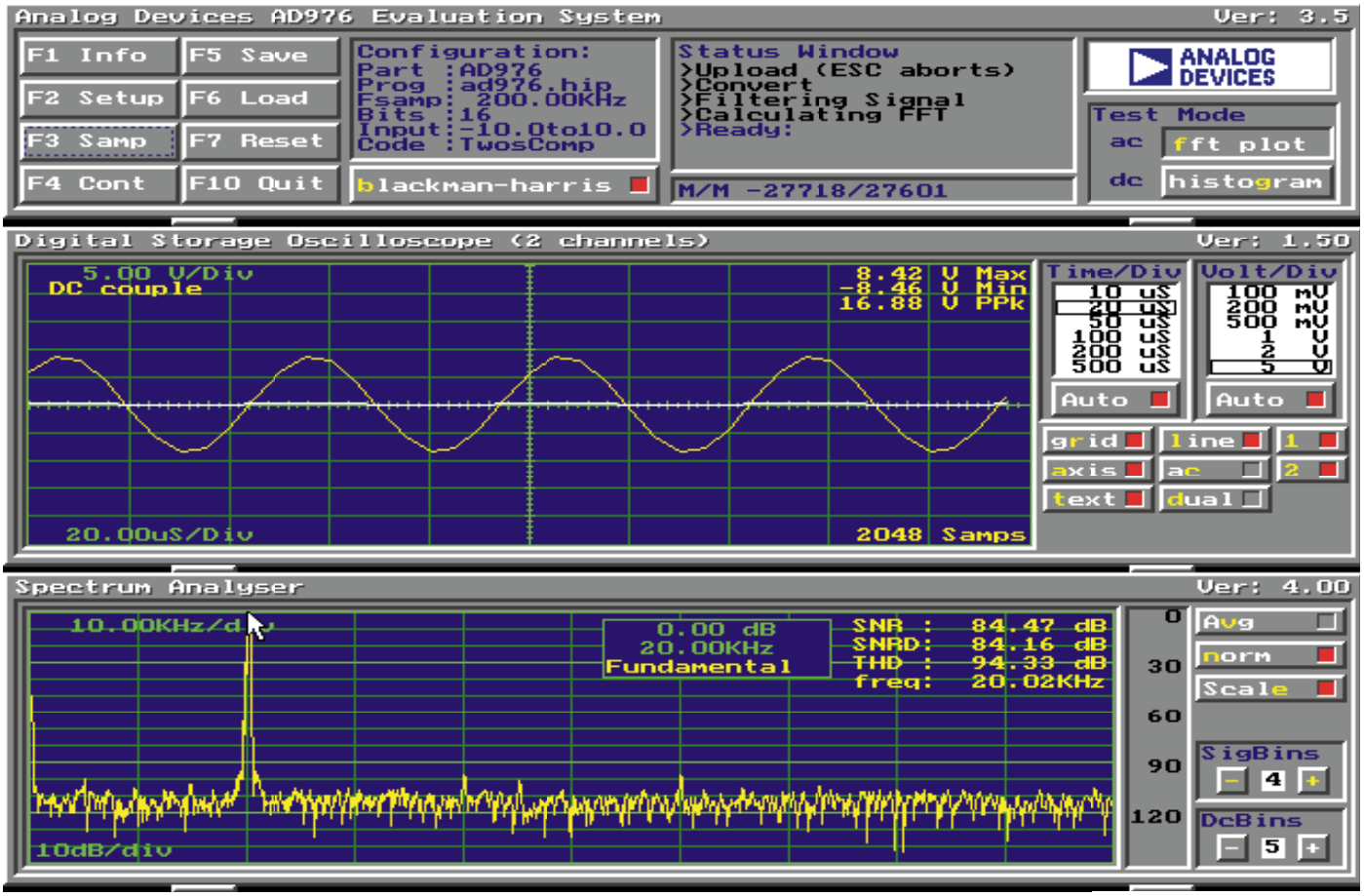


Figure 10. FFT screen.