National Semiconductor

MICROCIRCUIT DATA SHEET

MNLM2940-5.0-X REV 1A1

Original Creation Date: 07/22/96
Last Update Date: 10/08/99
Last Major Revision Date: 09/01/99

1A LOW DROPOUT REGULATOR

General Description

The LM2940 positive voltage regulator features the ability to source 1A of ouput current with a dropout voltage of typically 0.5V and a maximum of 1V over the entire temperature range. Furthermore, a quiescent current reduction circuit has been included which reduces the ground current when the differential between the input voltage and the output voltage exceeds approximately 3V. The quiescent current with 1A of output current and an input-output differential of 5V is therefore only 30 mA. Higher quiescent currents only exist when the regulator is in the dropout mode (Vin - Vout $\leq$ 3V).

Designed also for vehicular applications, the LM2940 and all regulated circuitry are protected from reverse battery installations or 2-battery jumps. During line transients, such as load dump when the input voltage can momentarily exceed the specified maximum operating voltage, the regulator will automatically shut down to protect both the internal circuits and the load. The LM2940 cannot be harmed by temporary mirror-image insertion. Familiar regulator features such as short circuit and thermal overload protection are also provided.

Industry Part Number

LM2940

NS Part Numbers

LM2940J-5.0/883
LM2940K-5.0/883
LM2940WG-5.0/883

Prime Die

LM2940

Controlling Document

SEE FEATURES SECTION

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{o}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Dropout voltage typically 0.5V @ Io = 1A
- Output current in excess of 1A
- Output voltage trimmed before assembly
- Reverse battery protection
- Internal short circuit current limit
- Mirror image insertion protection
- CONTROLLING DOCUMENT

LM2940J-5.0/883	5962-8958701EA
LM2940K-5.0/883	5962-8958701YA
LM2940WG5.0/883	5962-8958701XA

(Absolute Maximum Ratings)

(Note 1)

Input Voltage (Survival Voltage ≤100ms)		60V
Internal Power Dissipation (Note 2, 3)		Internally Limited
Maximum Junction Temperature		150 C
Storage Temperature Range		-65 C to +150 C
Lead Temperature (Soldering, 10 seconds)		300 C
Thermal Resistance		
ThetaJA		
T03 Pkg	(Still Air)	40 C/W
T03 Pkg	(500LF/Min Air Flow)	TBD
CERDIP	(Still Air)	73 C/W
CERDIP	(500LF/Min Air Flow)	37 C/W
CERAMIC SOIC	(Still Air)	122 C/W
CERAMIC SOIC	(500LF/Min Air Flow)	77 C/W
ThetaJC		
T03		5 C/W
CERDIP (Note 3)		3 C/W
CERAMIC SOIC (Note 3)		5 C/W
Package Weight		
T03 Pkg		TBD
CERDIP		1970mg
CERAMIC SOIC		360mg
ESD Susceptibility (Note 4)		4000V

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions see the Electrical Characteristics. The guaranteed specification apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: The package material for these devices allows much improved heat transfer over our standard ceramic packages. In order to take full advantage of this improved heat transfer, heat sinking must be provided between the package base (directly beneath the die), and either metal traces on, or thermal vias through, the printed circuit board. Without this additional heat sinking, device power dissipation must be calculated using junction-to-ambient, rather than junction-to-case, thermal resistance. It must not be assumed that the device leads will provide substantial heat transfer out of the package, since the thermal resistance of the leadframe material is very poor, relative to the material of the package base. The stated junction-to-case thermal resistance is for the package material only, and does not account for the additional thermal resistance between the package base and the printed circuit board. The user must determine the value of the additional thermal resistance and must combine this with the stated value for the package, to calculate the total allowed power dissipation for the device.

Note 4: Human body model, 100pF discharged through 1.5K Ohms

Recommended Operating Conditions

(Note 1)

Input Voltage	26V
Operating Temperature Range	-55 C $\leq$ TA $\leq$ +125 C

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Electrical Characteristics

DC PARAMETERS:

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vin = 10V, Io = 1A, Cout = 22uF

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vout	Output Voltage	Vin = 10V, Io = 5mA			4.85	5.15	V	1
					4.75	5.25	V	2, 3
		Vin = 6V, Io = 5mA			4.85	5.15	V	1
					4.75	5.25	V	2, 3
		Vin = 7V, Io = 5mA			4.85	5.15	V	1
					4.75	5.25	V	2, 3
		Vin = 26V, Io = 5mA			4.85	5.15	V	1
					4.75	5.25	V	2, 3
		Vin = 10V, Io = 1A			4.85	5.15	V	1
					4.75	5.25	V	2, 3
		Vin = 6V, Io = 1A			4.85	5.15	V	1
					4.75	5.25	V	2, 3
		Vin = 6V, Io = 50mA			4.85	5.15	V	1
					4.75	5.25	V	2, 3
		Vin = 10V, Io = 50mA			4.85	5.15	V	1
					4.75	5.25	V	2, 3
	Reverse Polarity Input Voltage DC	Ro = 100 Ohms	1		-15		V	1, 2, 3
Iq	Quiescent Current	Vin = 10V, Io = 5mA			0	15	mA	1
					0	20	mA	2, 3
		Vin = 7V, Io = 5mA			0	15	mA	1
					0	20	mA	2, 3
		Vin = 26V, Io = 5mA			0	15	mA	1
					0	20	mA	2, 3
		Vin = 10V, Io = 1A			0	50	mA	1
					0	100	mA	2, 3
Vrline	Line Regulation	7V ≤ Vin ≤ 26V, Io = 5mA			-40	40	mV	1
					-50	50	mV	2, 3
Vrload	Load Regulation	Vin = 10V, 50mA ≤ Io ≤ 1A			-50	50	mV	1
					-100	100	mV	2, 3

Electrical Characteristics

DC PARAMETERS:(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vin = 10V, Io = 1A, Cout = 22uF

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vdo	Dropout Voltage	Io = 1A			0	0.7	V	1
					0	1	V	2, 3
		Io = 100mA			0	200	mV	1
					0	300	mV	2, 3
Isc	Short Circuit Current	Vin = 10V			1.5		A	1
					1.3		A	2, 3

AC PARAMETERS:

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vin = 10V, Io = 1A, Cout = 22uF

	Max Line Transient	Vo ≤ 6V, Ro = 100 Ohms, T = 20ms	1		40		V	7, 8A, 8B
	Reverse Polarity Input Voltage Transient	T = 20ms, Ro = 100 Ohms	1		-45		V	7, 8A, 8B
RR	Ripple Rejection	Vin = 10V, 1Vrms, f = 1KHz, Io = 5mA	1		60		dB	4
			1		50		dB	5, 6
No	Output Noise Voltage	Vin = 10V, Io = 5mA, 10Hz = 100KHz	1		0	700	uVrms	4, 5, 6
Zo	Output Impedance	Vin = 10V, Io = 100mA DC and 20mA AC, fo = 120Hz	1			1	Ohm	4, 5, 6

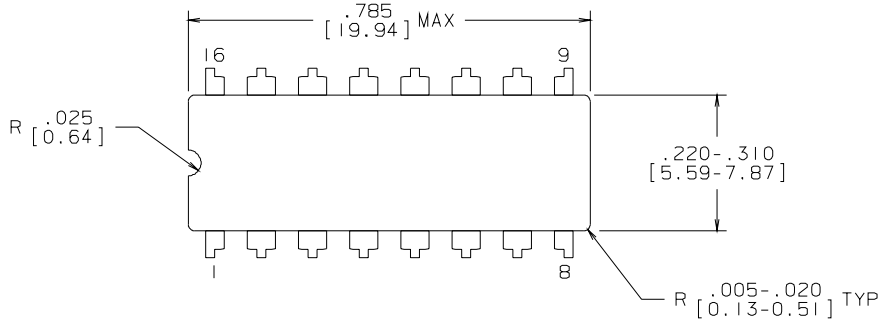
Note 1: Functional test only.

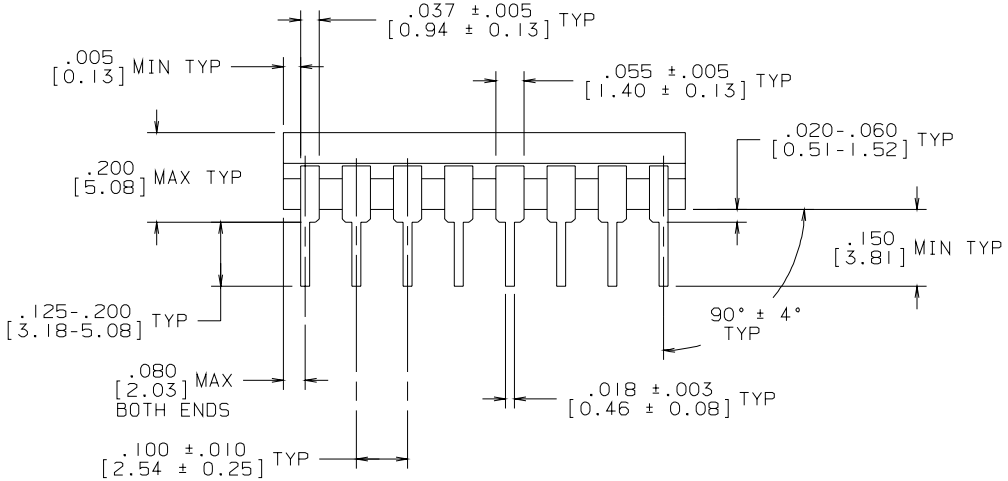
Graphics and Diagrams

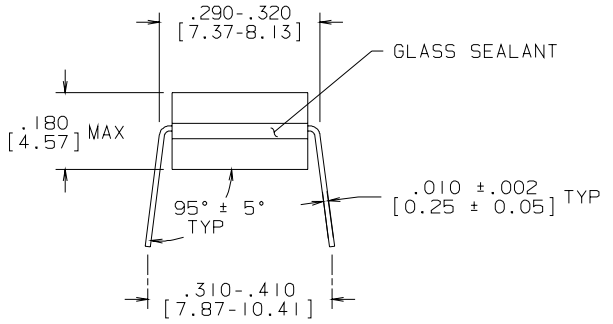
GRAPHICS#	DESCRIPTION
05826HRA2	METAL CAN (KA), TO-3, 2LD, LOW PROFILE (B/I CKT)
06332HRA2	CERDIP (J), 16 LEAD (B/I CKT)
06351HRA1	CERPACK (W), 16 LEAD (B/I CKT)
J16ARL	CERDIP (J), 16 LEAD (P/P DWG)
K02CRE	METAL CAN (KA), TO-3, 2LD, LOW PROFILE (P/P DWG)
P000137A	METAL CAN (KA), TO-3, 2LD, LOW PROFILE (PINOUT)
P000159A	CERDIP (J), 16 LEAD (PINOUT)
P000386A	CERAMIC SOIC (WG), 16 LEAD (PINOUT)
WG16ARC	CERAMIC SOIC (WG), 16 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	09996	09/15/93	TL/







MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AD, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

INCH
[MM]

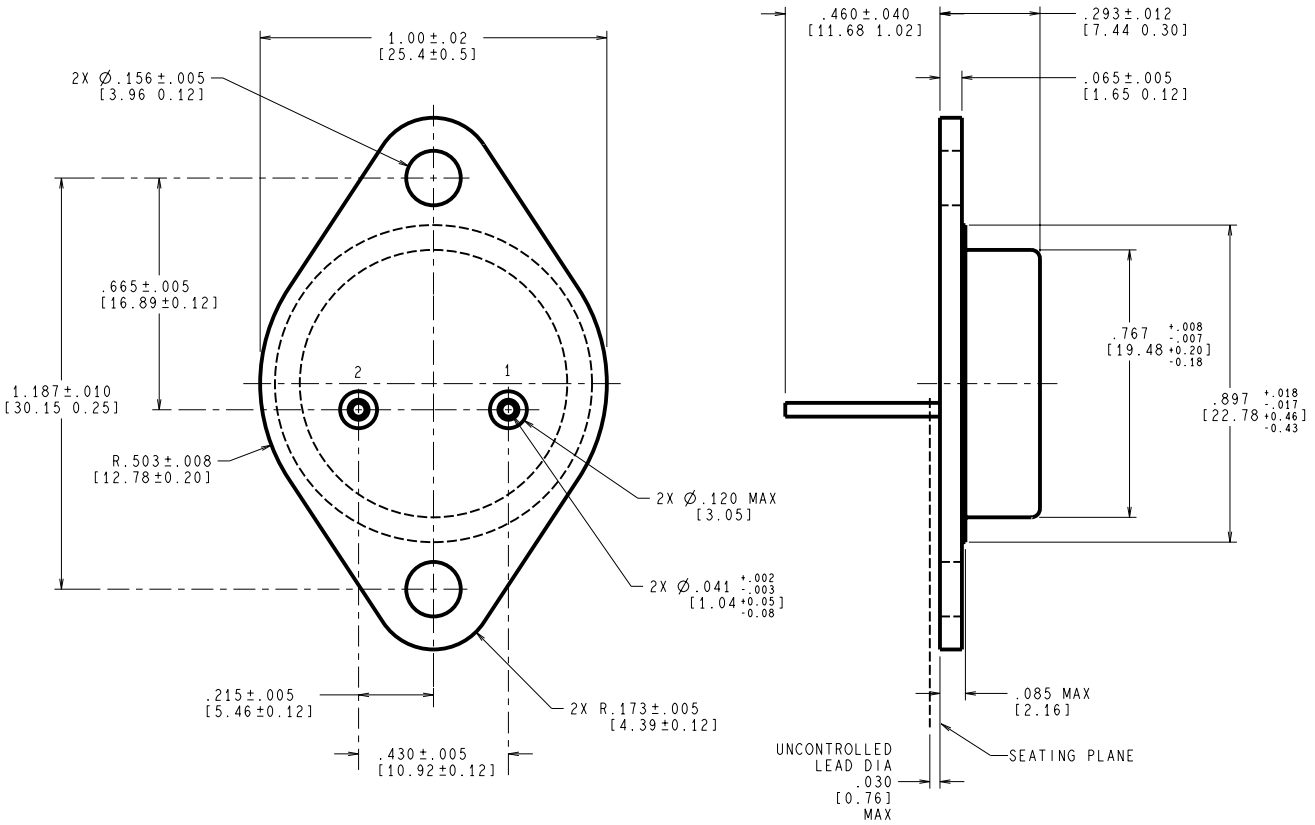
NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 16 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J16A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
E	REDRAW ON PRO/E; UPDATE MIL/AERO STAMP; NOTE 2: MIL-PRF-38535 WAS MIL-I-38535.	11155	09/15/95	MS/



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED

1. STANDARD HEADER TYPE SOLID BASE.
2. STANDARD LEAD FINISH:
   PER MIL-PRF-38535 TYPE X OR EQUIVALENT.
3. LEAD NOT BENT GREATER THAN 15° .
4. DIMENSIONS BASED ON JEDEC STANDARD TO-3,
   PUBLICATION 95, PAGE 98.

MIL-PRF-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: MARTA SUCHY	09/15/95
DFTG. CHK.	
ENGR. CHK.	

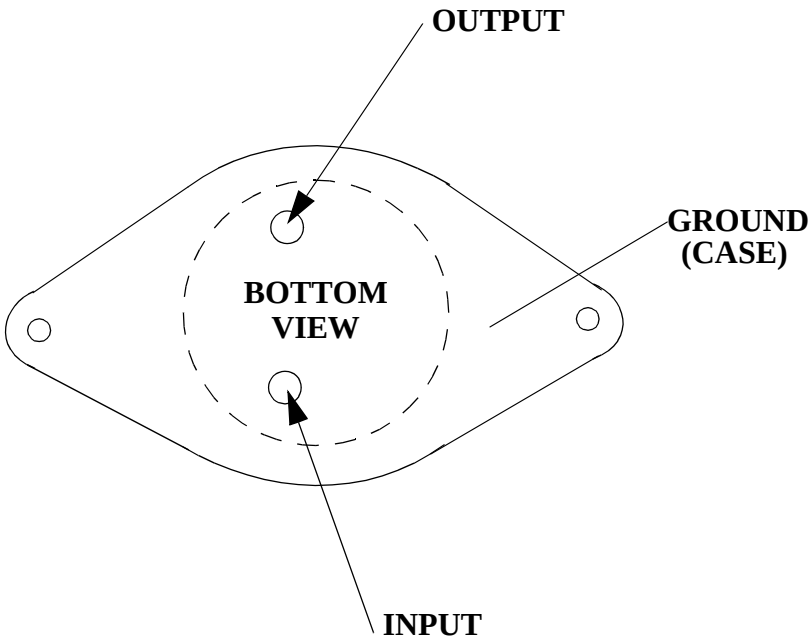
National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

METAL CAN, TO-3, 2 LEAD, LOW PROFILE

PROJECTION
INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-K02C	E

DO NOT SCALE DRAWING | SHEET 1 of 1



LM2940K-XX/883

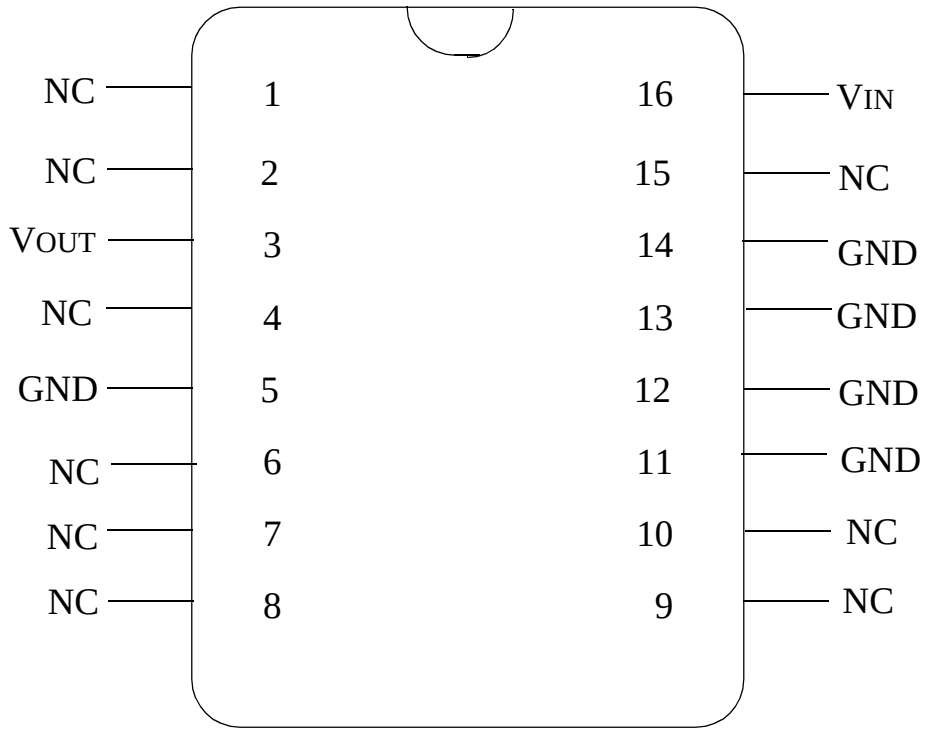
2 - LEAD TO3

CONNECTION DIAGRAM

BOTTOM VIEW

P000137A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LM2940J-XX

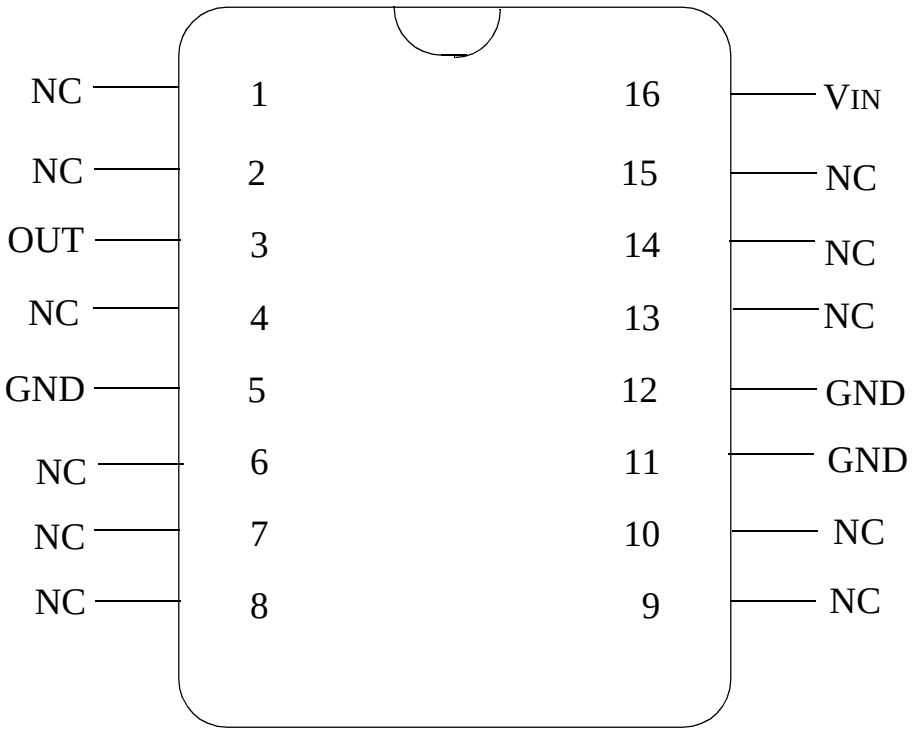
16 - LEAD DIP

CONNECTION DIAGRAM

TOP VIEW

P000159A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LM2940WG

16 - LEAD CERAMIC SOIC

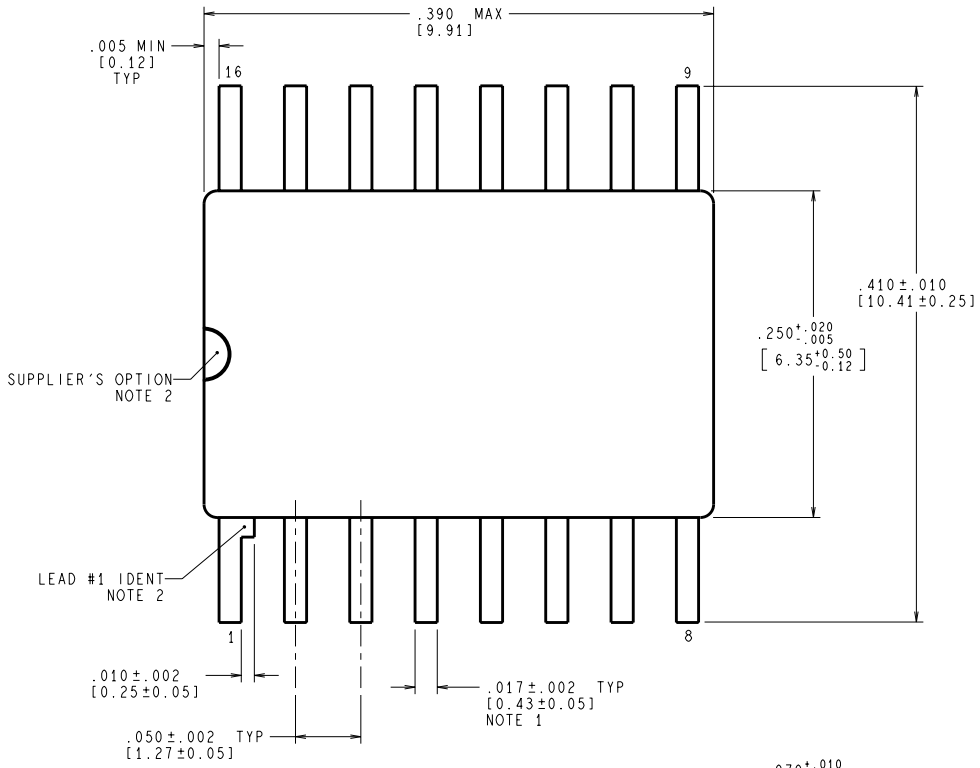
CONNECTION DIAGRAM

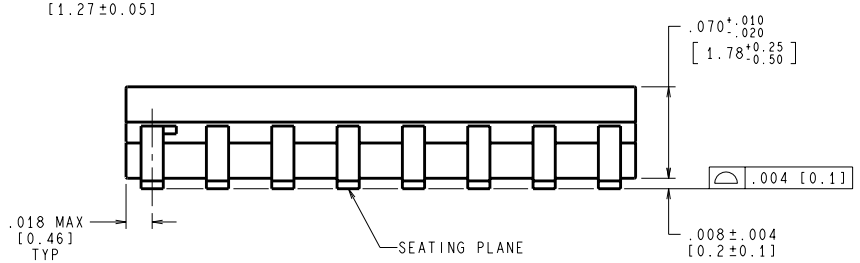
TOP VIEW

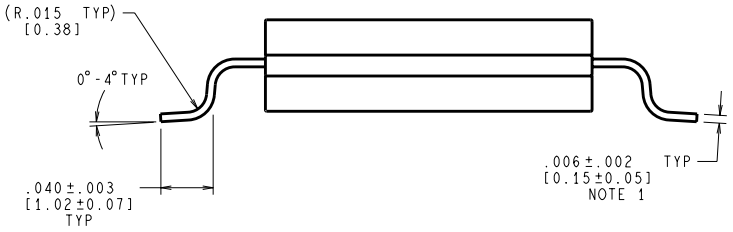
P000386A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11376	02/29/1996	MS/KH
B	LD PITCH TOL WAS ±.005; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R.006±.002; DIM .040±.003 WAS .037±.003	11443	04/19/1996	MS/KH
C	R .015[0.38] WAS R .006[0.15]	11840	10/08/1997	TL/







NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
2. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
3. NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-PRF-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: MARTA SUCHY	02/29/96
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK, 16 LEAD, GULL WING

PROJECTION
INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	(SC)MKT-WG16A	C

DO NOT SCALE DRAWING | SHEET 1 of 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0001534	12/15/98	Barbara Lopez	Initial Release of: MNLM2940-5.0-X Rev. 0A0. Added note for power dissipation and reference to thermal resistance for Aluminum Nitride package.
0B0	M0003110	02/03/99	Rose Malone	Update MDS: MNLM2940-5.0-X, Rev. 0A0 to MNLM2940-5.0-X, Rev. 0B0
0C1	M0003228	10/08/99	Rose Malone	Update MDS: MNLM2940-5.0-X, Rev. 0B0 to MNLM2940-5.0-X, Rev. 0C1.
1A1	M0003560	10/08/99	Rose Malone	Update MDS: MNLM2940-5.0-X, Rev. 0C1 to MNLM2940-5.0-X, Rev. 1A1. Updated Absolute Section Thermal Resistance temp. ThetaJa and ThetaJC to T03 package. Changed Vdo, Io = 100mA, Max. condition for subgroup 1 from 150mV to 200mV and subgroup 2 from 200mV to 300mV.