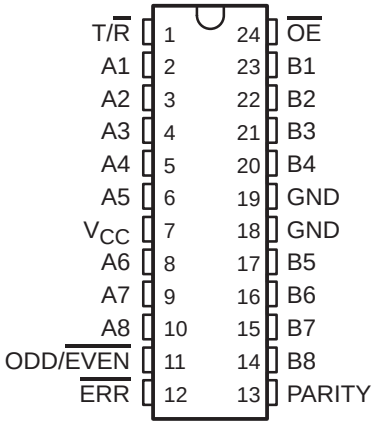
- **Combines ′F245 and ′F280B Functions in One Package**
- **High-Impedance N-P-N Inputs for Reduced Loading (70 μA in Low and High States)**
- **High Output Drive and Light Bus Loading**
- **3-State B Outputs Sink 64 mA and Source 15 mA**
- **Input Diodes for Termination Effects**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR NT PACKAGE
(TOP VIEW)



description

The SN74F657 contains eight noninverting buffers with 3-state outputs and an 8-bit parity generator/checker. It is intended for bus-oriented applications. The buffers have a specified current sinking capability of 24 mA at the A port and 64 mA at the B port.

The transmit/receive (T/$\overline{R}$) input determines the direction of the data flow through the bidirectional transceivers. When T/$\overline{R}$ is high, data is transmitted from the A port to the B port. When T/$\overline{R}$ is low, data is received at the A port from the B port.

When the output enable ($\overline{OE}$) input is high, both the A and B ports are placed in a high-impedance state (disabled). The ODD/$\overline{EVEN}$ input allows the user to select between odd or even parity systems. When transmitting from A port to B port (T/$\overline{R}$ high), PARITY is an output from the generator/checker. When receiving from B port to A port (T/$\overline{R}$ low), PARITY is an input.

When transmitting (T/$\overline{R}$ high), the parity select (ODD/$\overline{EVEN}$) input is made high or low as appropriate. The A port is then polled to determine the number of high bits.The PARITY output goes to the logic state determined by ODD/$\overline{EVEN}$ and the number of high bits on A port. When ODD/$\overline{EVEN}$ is low (for even parity) and the number of high bits on A port is odd, the PARITY will be high, transmitting even parity. If the number of high bits on A port is even, the PARITY will be low, keeping even parity.

When in the receive mode (T/$\overline{R}$ low), the B port is polled to determine the number of high bits. If ODD/$\overline{EVEN}$ is low (for even parity) and the number of highs on B port is:

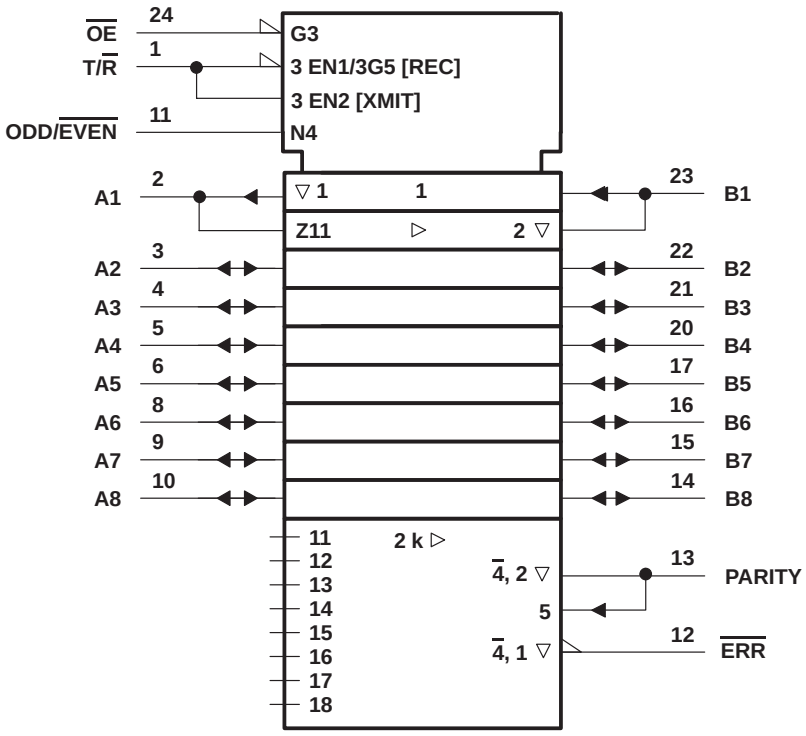
1. Odd and the PARITY input is high, then $\overline{ERR}$ will be high signifying no error.
2. Even and the PARITY input is high, then $\overline{ERR}$ will be low indicating an error.

The SN74F657 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

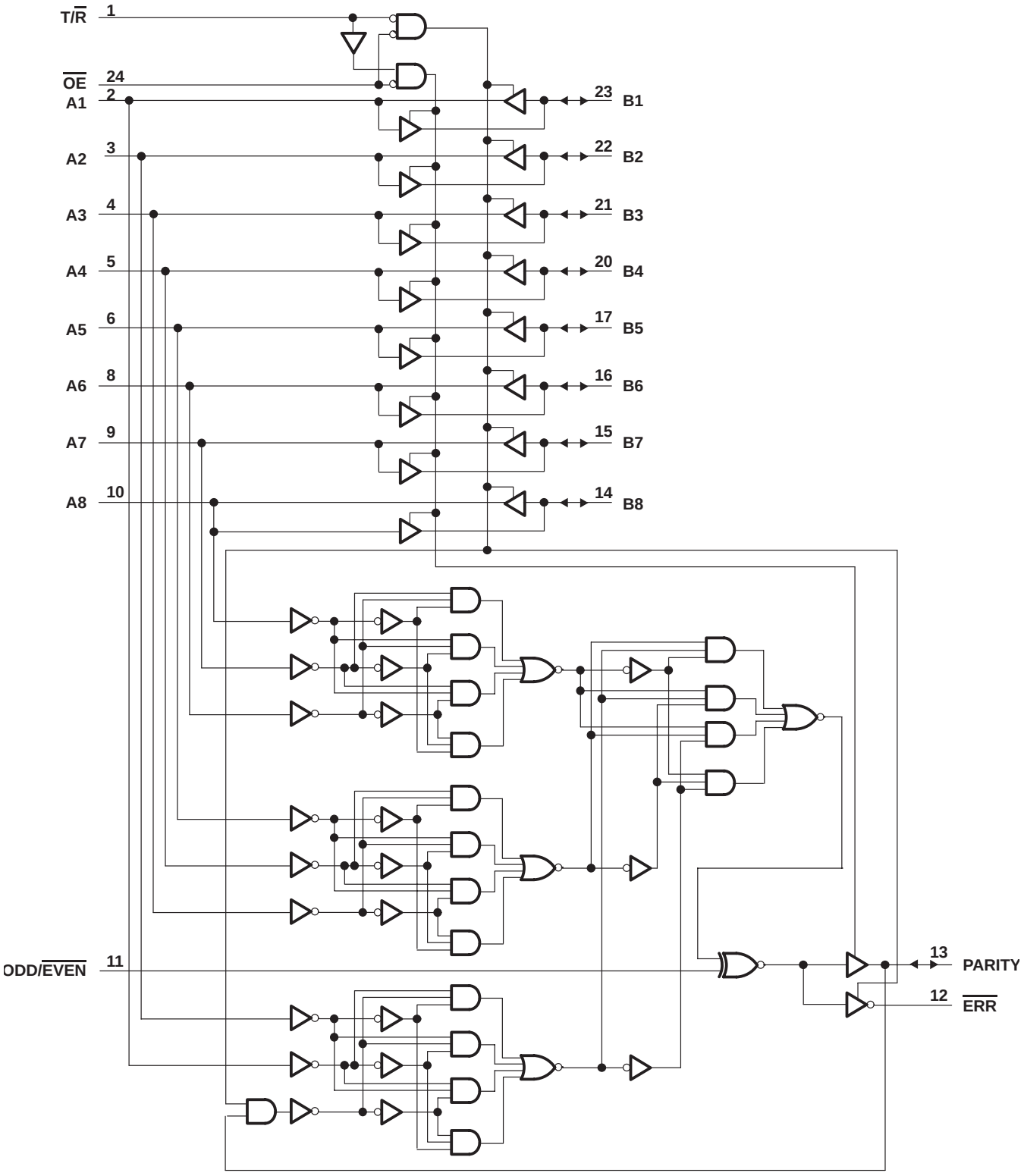
NUMBER OF A OR B INPUTS THAT ARE HIGH	INPUTS			INPUT/OUTPUT PARITY	OUTPUTS	
	$\overline{OE}$	T/$\overline{R}$	ODD/$\overline{EVEN}$		$\overline{ERR}$	OUTPUT MODE
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Don't care	H	X	X	Z	Z	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (excluding I/O ports) (see Note 1) . . . . . –1.2 V to 7 V
Input current range . . . . . –30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state . . . . . –0.5 V to 5.5 V
Voltage range applied to any output in the high state . . . . . –0.5 V to V_{CC}
Current into any output in the low state: A1–A8 . . . . . 48 mA
B1–B8 . . . . . 128 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input-voltage ratings may be exceeded provided the input-current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	A1–A8			–3	mA
		B1–B8, PARITY, $\overline{ERR}$			–12	
I_{OL}	Low-level output current	A1–A8			24	mA
		B1–B8, PARITY, $\overline{ERR}$			64	
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = – 18 mA				– 1.2	V
V_{OH}	Any output	V_{CC} = 4.5 V,	I_{OH} = – 3 mA		2.4	3.3		V
	B1–B8, PARITY, $\overline{ERR}$	V_{CC} = 4.5 V,	I_{OH} = – 15 mA		2	3.1		
	Any output	V_{CC} = 4.75 V,	I_{OH} = – 1 mA to – 3 mA		2.7			
V_{OL}	A1–A8	V_{CC} = 4.5 V	I_{OL} = 24 mA			0.35	0.5	V
	B1–B8, PARITY, $\overline{ERR}$		I_{OL} = 64 mA			0.42	0.55	
I_I	T/$\overline{R}$	V_{CC} = 0,	V_I = 7 V,	$\overline{OE}$ = 4.5 V			0.1	mA
	$\overline{OE}$	V_{CC} = 0,	V_I = 7 V,	T/$\overline{R}$ = 4.5 V			0.1	
	ODD/$\overline{EVEN}$	V_{CC} = 0,	V_I = 7 V				0.1	
	A1–A8	V_{CC} = 5.5 V,	V_I = 7 V				2	
	B1–B8						1	
I_{IH}‡	A, B, PARITY	V_{CC} = 5.5 V,	V_I = 2.7 V				70	µA
	T/$\overline{R}$, $\overline{OE}$						40	
	ODD/$\overline{EVEN}$						20	
I_{IL}‡	A, B, PARITY	V_{CC} = 5.5 V,	V_I = 0.5 V				– 70	µA
	T/$\overline{R}$, $\overline{OE}$						– 40	
	ODD/$\overline{EVEN}$						– 20	
I_{OS}§	A1–A8	V_{CC} = 5.5 V,	V_O = 0		– 60		– 150	mA
	B1–B8				– 100		– 225	
I_{OZH}	$\overline{ERR}$	V_{CC} = 5.5 V,	V_I = 2.7 V				50	µA
I_{OZL}	$\overline{ERR}$	V_{CC} = 5.5 V,	V_I = 0.5 V				–50	µA
I_{CCH}		V_{CC} = 5.5 V				90	125	mA
I_{CCL}		V_{CC} = 5.5 V				106	150	mA
I_{CCZ}		V_{CC} = 5.5 V				98	145	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2.5	4.2	7.5	2.5	8	ns
t_{PHL}			3	4	7.5	3	8	
t_{PLH}	A	PARITY	6	8.4	14	6	16	ns
t_{PHL}			6.8	8.5	15	6.8	16	
t_{PLH}	ODD/$\overline{\text{EVEN}}$	PARITY, $\overline{\text{ERR}}$	4	6.4	11	4	12	ns
t_{PHL}			4.5	6.9	11.5	4.5	12.5	
t_{PLH}	B	$\overline{\text{ERR}}$	8	12.7	20.5	7.5	22.5	ns
t_{PHL}			8	13.4	20.5	7.5	22.5	
t_{PLH}	PARITY	$\overline{\text{ERR}}$	6	8.1	15.5	6	16.5	ns
t_{PHL}			7.5	8.8	15.5	7.5	17	
t_{PZH}	$\overline{\text{OE}}$	A, B, PARITY, or $\overline{\text{ERR}}$‡	3	5.3	8	3	9	ns
t_{PZL}			4	5.4	9.5	4	11	
t_{PHZ}	$\overline{\text{OE}}$	A, B, PARITY, or $\overline{\text{ERR}}$‡	2	4.2	7.5	2	8	ns
t_{PLZ}			2	3.7	6	2	6.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ These delay times reflect the 3-state recovery time only and not the signal through the buffers or parity check circuitry. To assure valid information at the $\overline{\text{ERR}}$ output pin, time must be allowed for the signal to propagate through the drivers (B to A), and to the $\overline{\text{ERR}}$ output. Valid data at the $\overline{\text{ERR}}$ output is greater than or equal to (B to A) + (A to PARITY).

NOTE 2: Load circuits and waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74F657DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	F657	Samples
SN74F657NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	0 to 70	SN74F657NT	
SN74F657NTE4	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	0 to 70		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

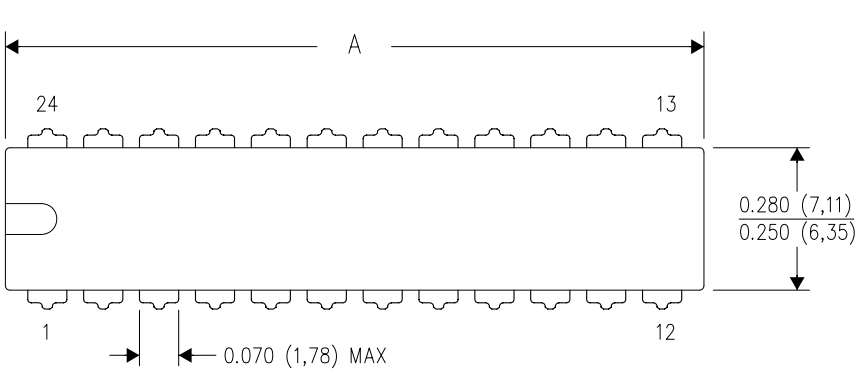
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

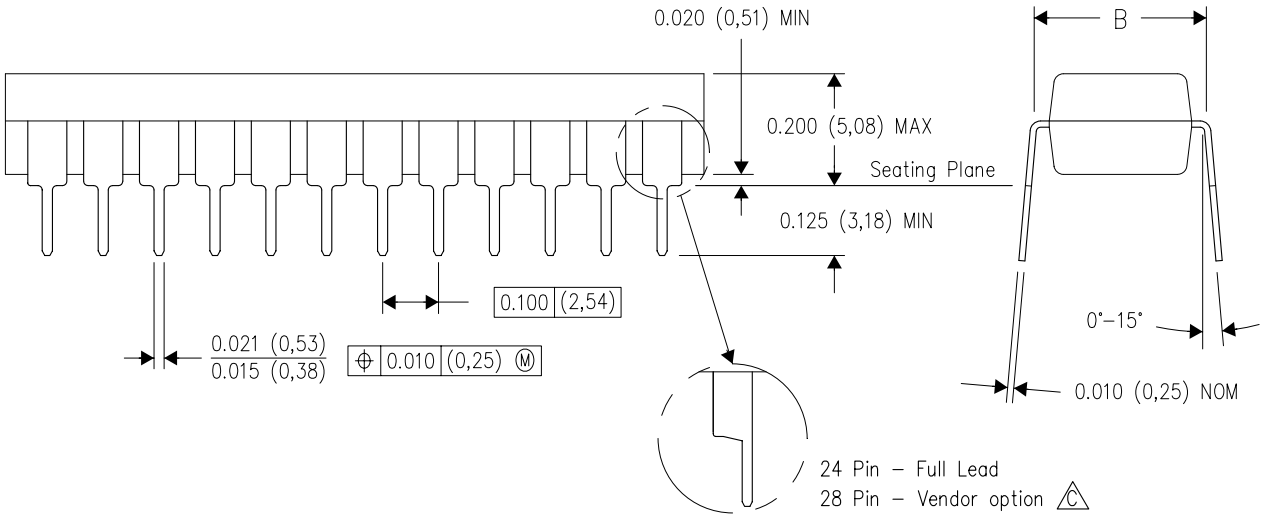
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

NT (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

24 PINS SHOWN



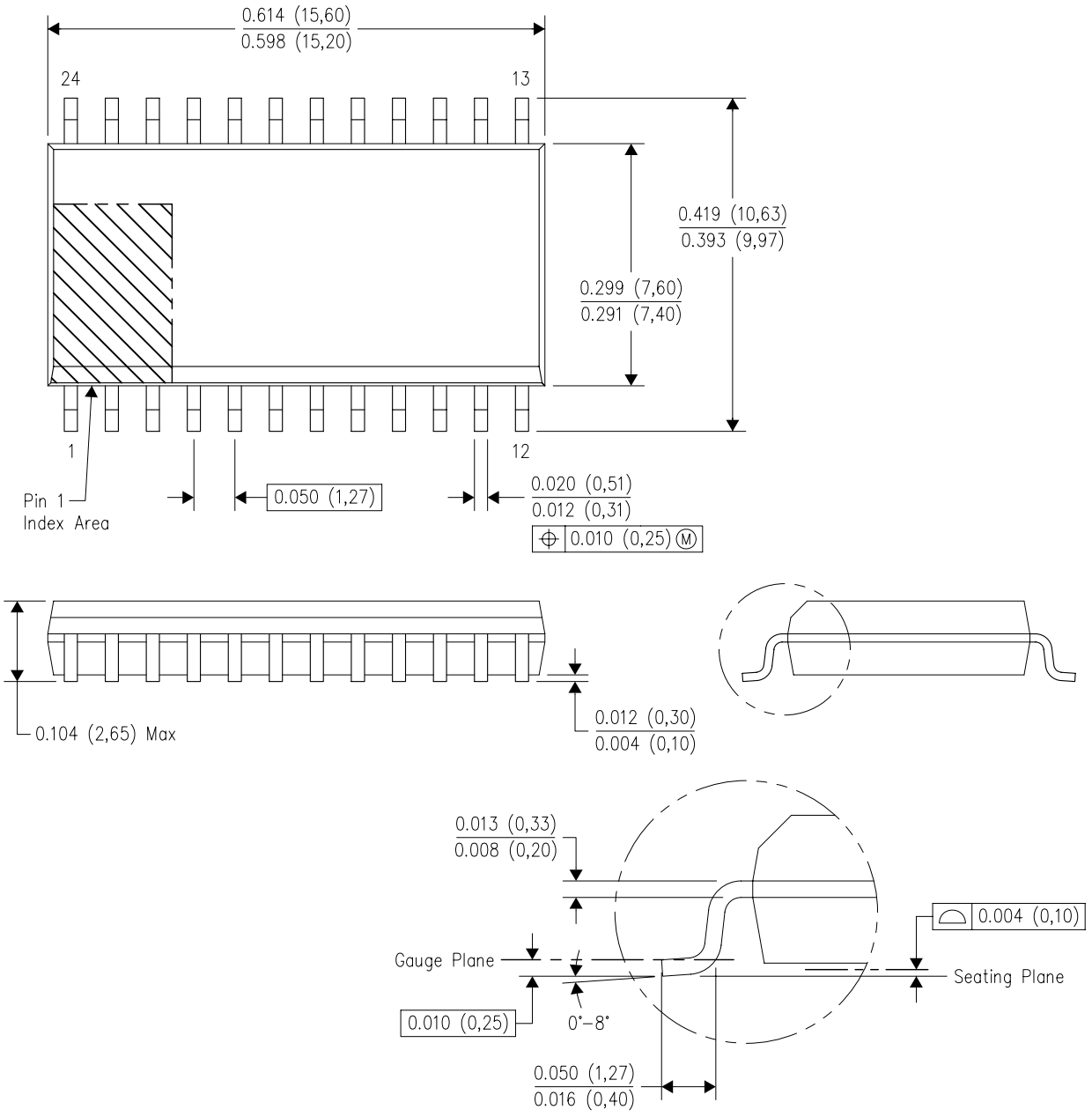
DIM \ PINS **	24	28
A MAX	1.260 (32,04)	1.425 (36,20)
A MIN	1.230 (31,24)	1.385 (35,18)
B MAX	0.310 (7,87)	0.315 (8,00)
B MIN	0.290 (7,37)	0.295 (7,49)



4040050/C 04/09

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. The 28 pin end lead shoulder width is a vendor option, either half or full width.

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

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