Jameco Part Number 1760562

LINEAR TECHNOLOGY

LTC6800
Rail-to-Rail
Input and Output,
Instrumentation Amplifier

FEATURES

- **116dB CMRR Independent of Gain**
- **Maximum Offset Voltage: 100μV**
- **Maximum Offset Voltage Drift: 250nV/°C**
- **–40°C to 125°C Operation**
- Rail-to-Rail Input Range
- Rail-to-Rail Output Swing
- Supply Operation: 2.7V to 5.5V
- Available in an MS8 and 3mm × 3mm × 0.8mm DFN Packages

APPLICATIONS

- Thermocouple Amplifiers
- Electronic Scales
- Medical Instrumentation
- Strain Gauge Amplifiers
- High Resolution Data Acquisition

DESCRIPTION

The LTC®6800 is a precision instrumentation amplifier. The CMRR is typically 116dB with a single 5V supply and is independent of gain. The input offset voltage is guaranteed below 100μV with a temperature drift of less than 250nV/°C. The LTC6800 is easy to use; the gain is adjustable with two external resistors, like a traditional op amp.

The LTC6800 uses charge balanced sampled data techniques to convert a differential input voltage into a single ended signal that is in turn amplified by a zero-drift operational amplifier.

The differential inputs operate from rail-to-rail and the single ended output swings from rail-to-rail. The LTC6800 is available in an MS8 surface mount package. For space limited applications, the LTC6800 is available in a 3mm × 3mm × 0.8mm dual fine pitch leadless package (DFN).
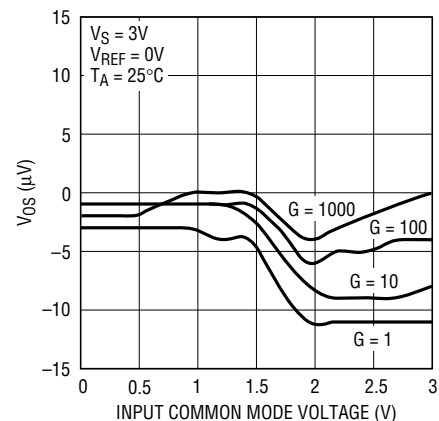
, LTC and LT are registered trademarks of Linear Technology Corporation.

TYPICAL APPLICATION

High Side Power Supply Current Sense
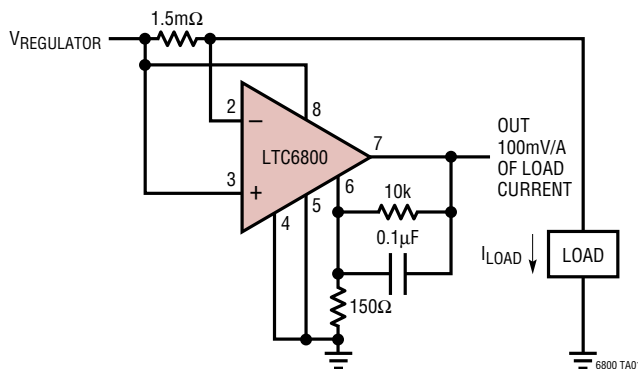
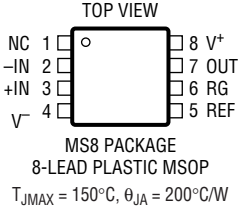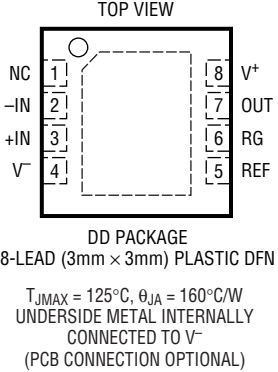**Typical Input Referred Offset vs Input Common Mode Voltage (V$_S$ = 3V)**

sn6800 6800fas

1

LTC6800

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-) 5.5V
Input Current .... ±10mA
$\left| V_{IN}^+ - V_{REF} \right|$ 5.5V
$\left| V_{IN}^- - V_{REF} \right|$ 5.5V
Output Short Circuit Duration .... Indefinite

Operating Temperature Range
(Note 7) .... −40°C to 125°C
Storage Temperature Range
   MS8 Package .... −65°C to 150°C
   DD Package .... −65°C to 125°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
TOP VIEW	LTC6800HMS8
NC 1 — 8 V+ −IN 2 — 7 OUT +IN 3 — 6 RG V− 4 — 5 REF MS8 PACKAGE 8-LEAD PLASTIC MSOP $T_{JMAX} = 150°C$, $\theta_{JA} = 200°C/W$	MS8 PART MARKING
	LTADE

	ORDER PART NUMBER
TOP VIEW	LTC6800HDD
NC 1 — 8 V+ −IN 2 — 7 OUT +IN 3 — 6 RG V− 4 — 5 REF DD PACKAGE 8-LEAD (3mm × 3mm) PLASTIC DFN $T_{JMAX} = 125°C$, $\theta_{JA} = 160°C/W$ UNDERSIDE METAL INTERNALLY CONNECTED TO V− (PCB CONNECTION OPTIONAL)	DD PART MARKING
	LAEP

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. $V^+ = 3V$, $V^- = 0V$, REF = 200mV. Output voltage swing is referenced to V^-. All other specifications reference the OUT pin to the REF pin.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 2)	$V_{CM} = 200mV$				±100	μV
Average Input Offset Drift (Note 2)	$T_A = -40°C$ to 85°C $T_A = 85°C$ to 125°C	● ●		 −1	±250 −2.5	nV/°C μV/°C
Common Mode Rejection Ratio (Notes 4, 5)	$A_V = 1$, $V_{CM} = 0V$ to 3V	●	85	113		dB
Integrated Input Bias Current (Note 3)	$V_{CM} = 1.2V$			4	10	nA
Integrated Input Offset Current (Note 3)	$V_{CM} = 1.2V$			1	3	nA
Input Noise Voltage	DC to 10Hz			2.5		μV$_{P-P}$
Power Supply Rejection Ratio (Note 6)	$V_S = 2.7V$ to 5.5V	●	110	116		dB
Output Voltage Swing High	$R_L = 2k$ to V^- $R_L = 10k$ to V^-	● ●	2.85 2.95	2.94 2.98		V V
Output Voltage Swing Low		●			20	mV
Gain Error	$A_V = 1$				0.1	%
Gain Nonlinearity	$A_V = 1$				100	ppm

ELECTRICAL CHARACTERISTICS
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 3V, V^- = 0V, REF = 200mV. Output voltage swing is referenced to V^-. All other specifications reference the OUT pin to the REF pin.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current	No Load	●			1.2	mA
Internal Op Amp Gain Bandwidth				200		kHz
Slew Rate				0.2		V/μs
Internal Sampling Frequency				3		kHz

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 5V, V^- = 0V, REF = 200mV. Output voltage swing is referenced to V^-. All other specifications reference the OUT pin to the REF pin.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 2)	V_{CM} = 200mV				±100	μV
Average Input Offset Drift (Note 2)	T_A = −40°C to 85°C	●			±250	nV/°C
	T_A = 85°C to 125°C	●		−1	−2.5	μV/°C
Common Mode Rejection Ratio (Notes 4, 5)	A_V = 1, V_{CM} = 0V to 5V	●	85	116		dB
Integrated Input Bias Current (Note 3)	V_{CM} = 1.2V			4	10	nA
Integrated Input Offset Current (Note 3)	V_{CM} = 1.2V			1	3	nA
Power Supply Rejection Ratio (Note 6)	V_S = 2.7V to 5.5V	●	110	116		dB
Output Voltage Swing High	R_L = 2k to V^-	●	4.85	4.94		V
	R_L = 10k to V^-	●	4.95	4.98		V
Output Voltage Swing Low		●			20	mV
Gain Error	A_V = 1				0.1	%
Gain Nonlinearity	A_V = 1				100	ppm
Supply Current	No Load	●			1.3	mA
Internal Op Amp Gain Bandwidth				200		kHz
Slew Rate				0.2		V/μs
Internal Sampling Frequency				3		kHz

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: These parameters are guaranteed by design. Thermocouple effects preclude measurement of these voltage levels in high speed automatic test systems. V_{OS} is measured to a limit determined by test equipment capability.

Note 3: If the total source resistance is less than 10k, no DC errors result from the input bias currents or the mismatch of the input bias currents or the mismatch of the resistances connected to −IN and +IN.

Note 4: The CMRR with a voltage gain, A_V, larger than 10 is 120dB (typ).

Note 5: At temperatures above 70°C, the common mode rejection ratio lowers when the common mode input voltage is within 100mV of the supply rails.

Note 6: The power supply rejection ratio (PSRR) measurement accuracy depends on the proximity of the power supply bypass capacitor to the device under test. Because of this, the PSRR is 100% tested to relaxed limits at final test. However, their values are guaranteed by design to meet the data sheet limits.

Note 7: The LTC6800H is guaranteed functional over the operating temperature range of −40°C to 125°C. Specifications over the −40°C to 125°C range (denoted by ●) are assured by design and characterization but are not tested or QA sampled at these temperatures.
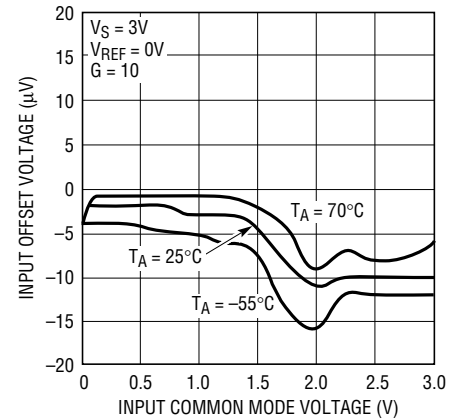
TYPICAL PERFORMANCE CHARACTERISTICS

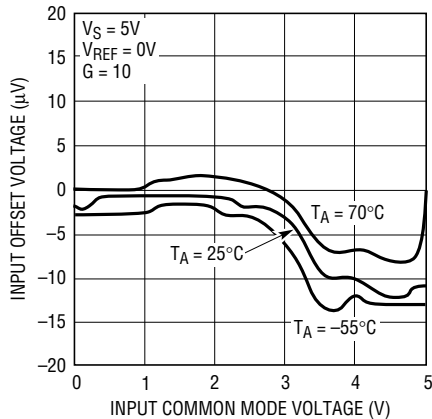**Input Offset Voltage vs Input Common Mode Voltage**
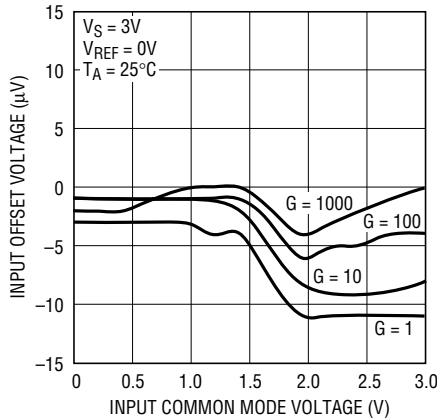
6800 G01

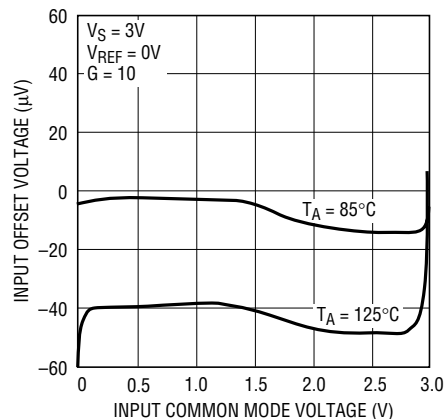**Input Offset Voltage vs Input Common Mode Voltage**
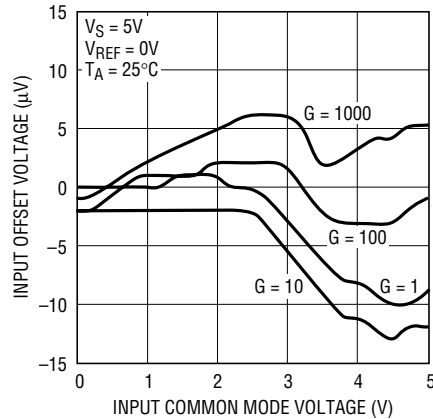
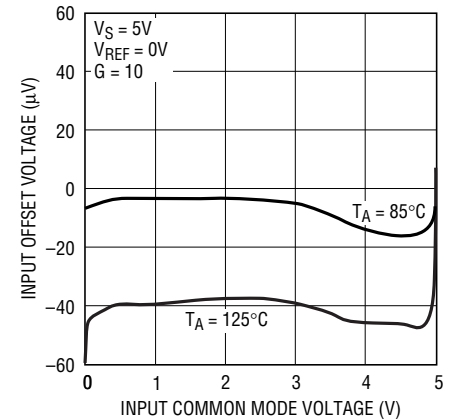2053 G02

Input Offset Voltage vs Input Common Mode Voltage
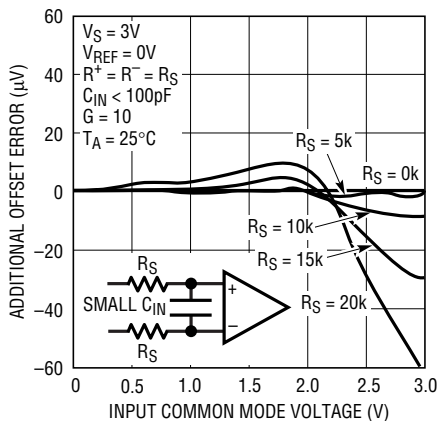

6800 G03

Input Offset Voltage vs Input Common Mode Voltage

6800 G04

Input Offset Voltage vs Input Common Mode Voltage, 85°C ≤ T_A ≤ 125°C

6800 G05

Input Offset Voltage vs Input Common Mode Voltage, 85°C ≤ T_A ≤ 125°C
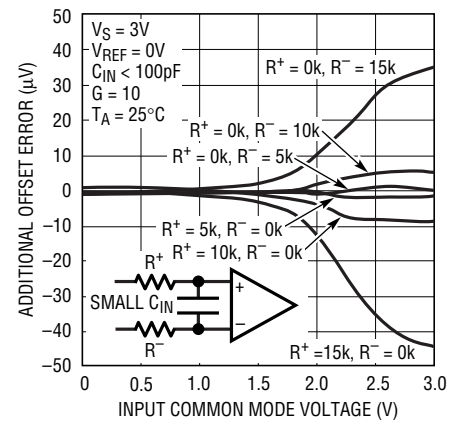

6800 G06

Additional Input Offset Due to Input R_S vs Input Common Mode (C_{IN} < 100pF)

6800 G07

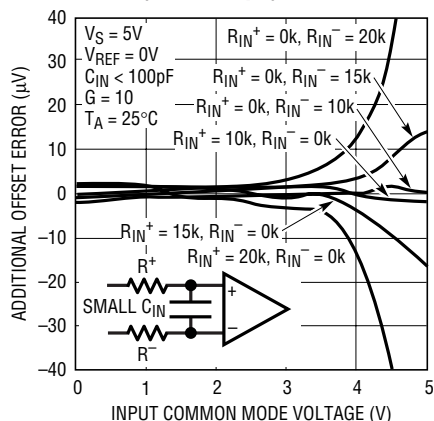**Additional Input Offset Due to Input R_S vs Input Common Mode (C_{IN} < 100pF)**
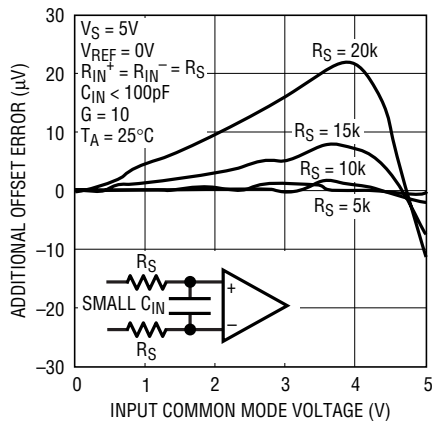
6800 G08

Additional Input Offset Due to Input R_S Mismatch vs Input Common Mode (C_{IN} < 100pF)

6800 G09
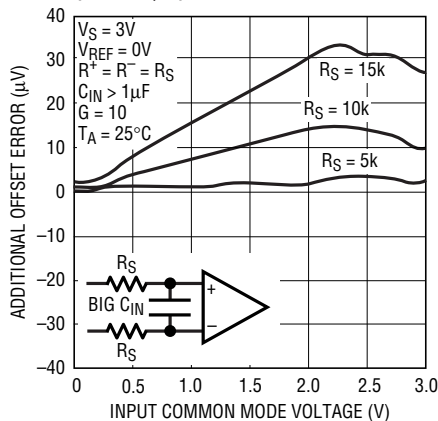
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TYPICAL PERFORMANCE CHARACTERISTICS

Additional Input Offset Due to Input R_S Mismatch vs Input Common Mode (C_IN < 100pF)
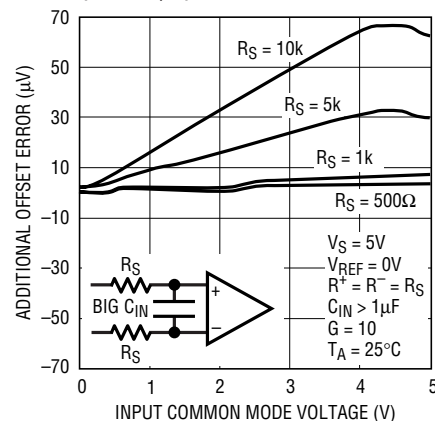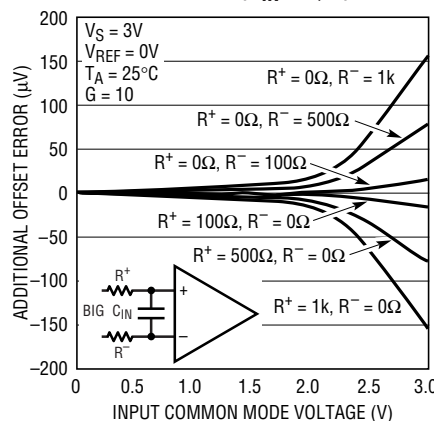

6800 G10

Additional Input Offset Due to Input R_S vs Input Common Mode (C_IN > 1μF)
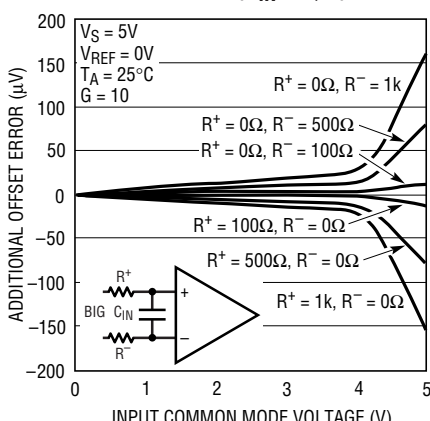

6800 G11

Additional Input Offset Due to Input R_S vs Input Common Mode (C_IN > 1μF)
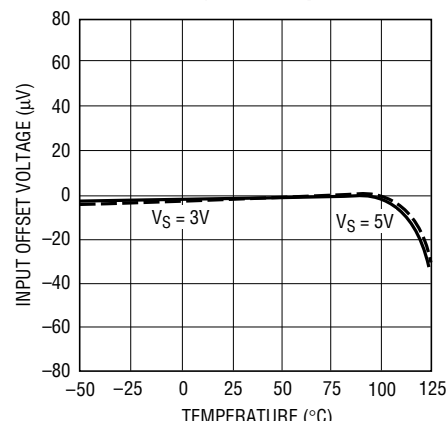

6800 G12

Additional Input Offset Due to Input R_S Mismatch vs Input Common Mode (C_IN > 1μF)

6800 G13

Additional Input Offset Due to Input R_S Mismatch vs Input Common Mode (C_IN > 1μF)

6800 G14

Offset Voltage vs Temperature

6800 G15

V_OS vs V_REF
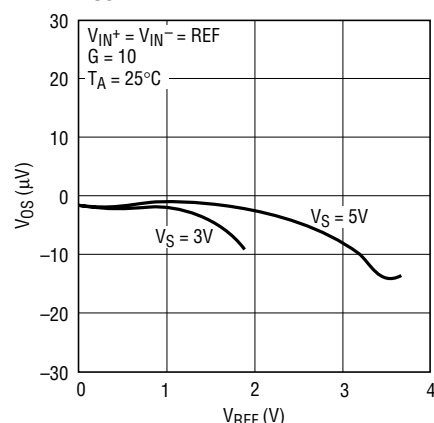
6800 G16

Gain Nonlinearity, G = 1
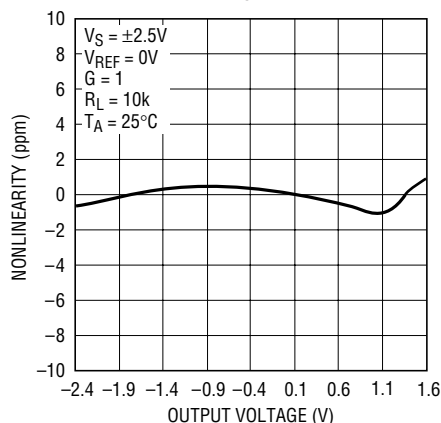
6800 G17

Gain Nonlinearity, G = 10
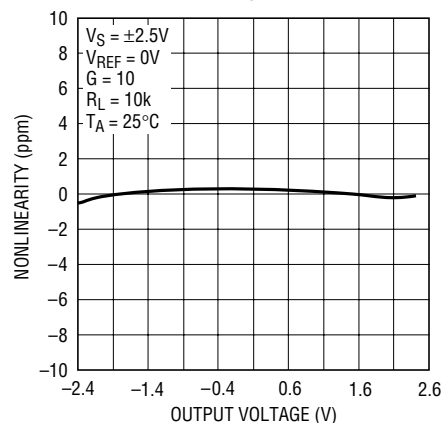
6800 G18

TYPICAL PERFORMANCE CHARACTERISTICS

CMRR vs Frequency
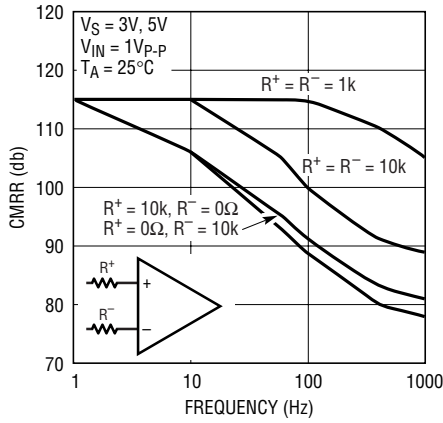
6800 G19

Input Voltage Noise Density vs Frequency
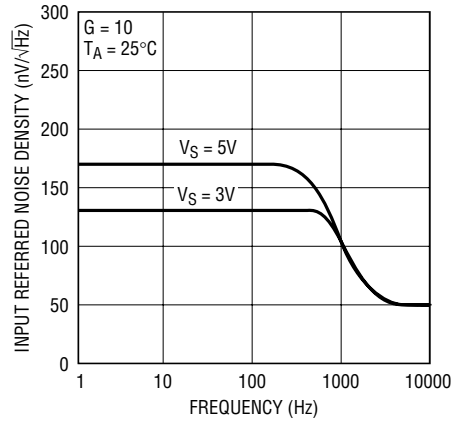
6800 G20

Input Referred Noise in 10Hz Bandwidth
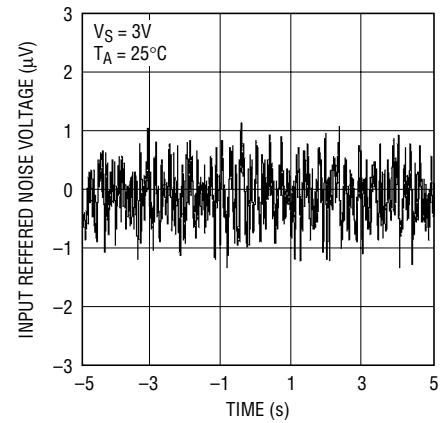
6800 G21

Input Referred Noise in 10Hz Bandwidth
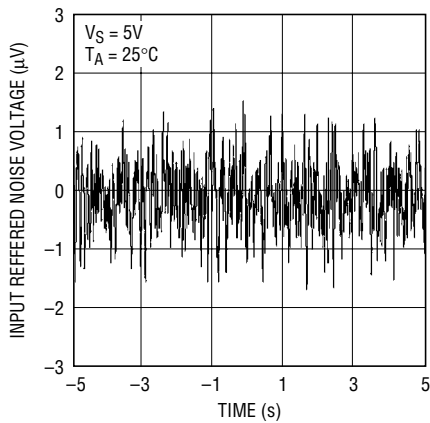
6800 G22

Output Voltage Swing vs Output Current
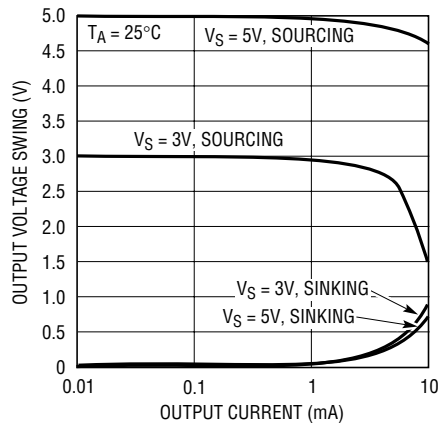
6800 G23

Supply Current vs Supply Voltage
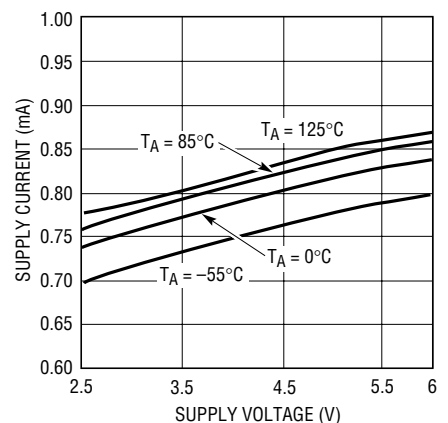
6800 G24

Low Gain Settling Time vs Settling Accuracy
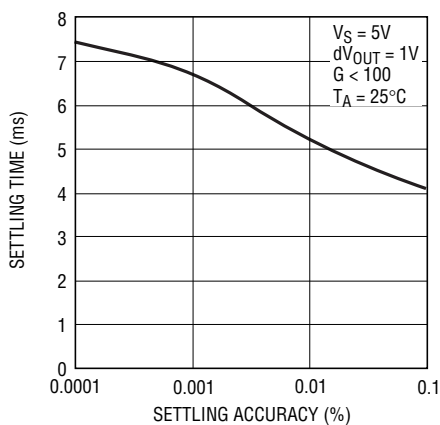
6800 G25

Settling Time vs Gain
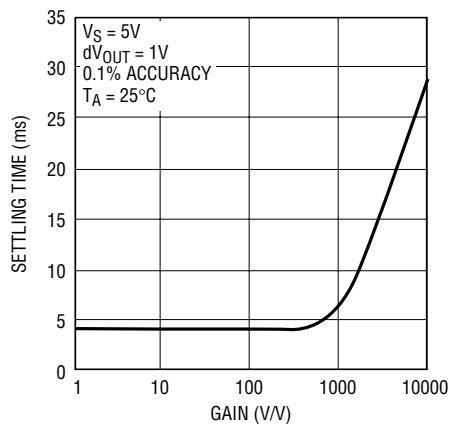
6800 G26

Internal Clock Frequency vs Supply Voltage

6800 G27

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6
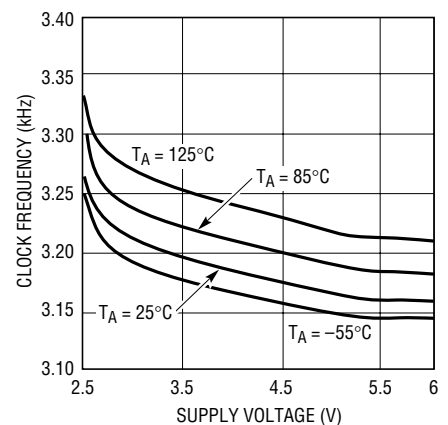
PIN FUNCTIONS

NC (Pin 1): Not Connected.

–IN (Pin 2): Inverting Input.

+IN (Pin 3): Noninverting Input.

V⁻ (Pin 4): Negative Supply.

REF (Pin 5): Voltage Reference (V_{REF}) for Amplifier Output.

RG (Pin 6): Inverting Input of Internal Op Amp. With a resistor, R2, connected between the OUT pin and the RG pin and a resistor, R1, between the RG pin and the REF pin, the DC gain is given by 1 + R2 / R1.

OUT (Pin 7): Amplifier Output.

$$V_{OUT} = GAIN\ (V_{+IN} - V_{-IN}) + V_{REF}$$

V⁺ (Pin 8): Positive Supply.

BLOCK DIAGRAM
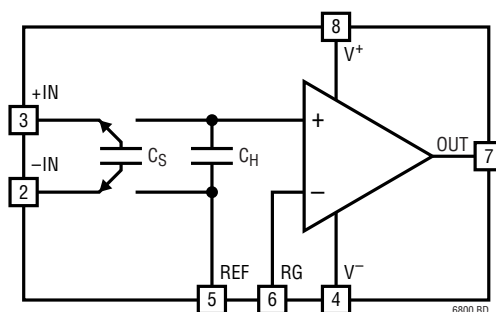
APPLICATIONS INFORMATION

Theory of Operation

The LTC6800 uses an internal capacitor (C_S) to sample a differential input signal riding on a DC common mode voltage (see Block Diagram). This capacitor's charge is transferred to a second internal hold capacitor (C_H) translating the common mode of the input differential signal to that of the REF pin. The resulting signal is amplified by a zero-drift op amp in the noninverting configuration. The RG pin is the negative input of this op amp and allows external programmability of the DC gain. Simple filtering can be realized by using an external capacitor across the feedback resistor.

Input Voltage Range

The input common mode voltage range of the LTC6800 is rail-to-rail. However, the following equation limits the size of the differential input voltage:

$$V^- \leq (V_{+IN} - V_{-IN}) + V_{REF} \leq V^+ - 1.3$$

where V_{+IN} and V_{-IN} are the voltages of the +IN and –IN pins respectively, V_{REF} is the voltage at the REF pin and V^+ is the positive supply voltage.

For example, with a 3V single supply and a 0V to 100mV differential input voltage, V_{REF} must be between 0V and 1.6V.

Settling Time

The sampling rate is 3kHz and the input sampling period during which C_S is charged to the input differential voltage V_{IN} is approximately 150µs. First assume that on each input sampling period, C_S is charged fully to V_{IN}. Since $C_S = C_H$ (= 1000pF), a change in the input will settle to N bits of accuracy at the op amp noninverting input after N clock cycles or 333µs(N). The settling time at the OUT pin is also affected by the settling of the internal op amp. Since the gain bandwidth of the internal op amp is typically 200kHz, the settling time is dominated by the switched capacitor front end for gains below 100 (see Typical Performance Characteristics).
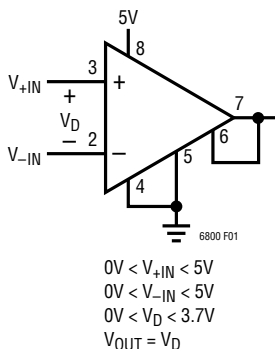
SINGLE SUPPLY, UNITY GAIN

0V < V_{+IN} < 5V
0V < V_{-IN} < 5V
0V < V_D < 3.7V
$V_{OUT} = V_D$

Figure 1

APPLICATIONS INFORMATION

Input Current

Whenever the differential input V_{IN} changes, C_H must be charged up to the new input voltage via C_S. This results in an input charging current during each input sampling period. Eventually, C_H and C_S will reach V_{IN} and, ideally, the input current would go to zero for DC inputs.

In reality, there are additional parasitic capacitors which disturb the charge on C_S every cycle even if V_{IN} is a DC voltage. For example, the parasitic bottom plate capacitor on C_S must be charged from the voltage on the REF pin to the voltage on the –IN pin every cycle. The resulting input charging current decays exponentially during each input sampling period with a time constant equal to $R_S C_S$. **If the voltage disturbance due to these currents settles before the end of the sampling period, there will be no errors due to source resistance or the source resistance mismatch between –IN and +IN. With R_S less than 10k, no DC errors occur due to this input current.**

In the Typical Performance Characteristics section of this data sheet, there are curves showing the additional error from nonzero source resistance in the inputs. If there are no large capacitors across the inputs, the amplifier is less sensitive to source resistance and source resistance mismatch. When large capacitors are placed across the inputs, the input charging currents described above result in larger DC errors, especially with source resistor mismatches.

Power Supply Bypassing

The LTC6800 uses a sampled data technique and therefore contains some clocked digital circuitry. It is therefore sensitive to supply bypassing. A 0.1μF ceramic capacitor must be connected between Pin 8 (V$^+$) and Pin 4 (V$^−$) with leads as short as possible.

TYPICAL APPLICATIONS

Precision ÷2

5V

0.1μF

V_{IN}

3
+

8

LTC6800

7

V_{OUT}

2
−

4
5
6

1k

$V_{OUT} = \dfrac{V_{IN}}{2}$

0.1μF

6800 TA03
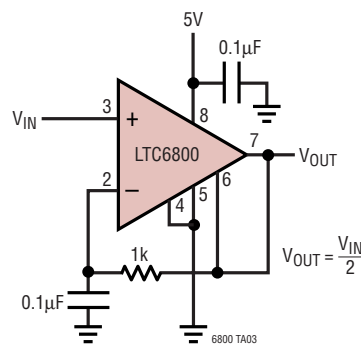
Precision Doubler (General Purpose)

2.5V 0.1μF

V_{IN}

3
+

8

LTC6800

7

V_{OUT}

2
−

5
6

4

$V_{OUT} = 2V_{IN}$

0.1μF

0.1μF

−2.5V

6800 TA04
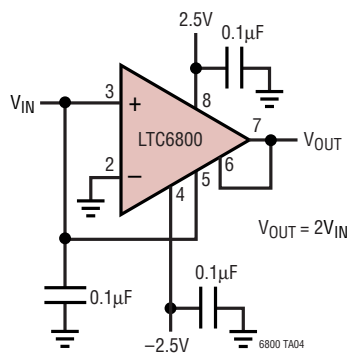
Precision Inversion (General Purpose)

2.5V 0.1μF

3
+

8

LTC6800

7

V_{OUT}

V_{IN}

2
−

5
6

4

$V_{OUT} = -V_{IN}$

0.1μF

−2.5V

6800 TA05
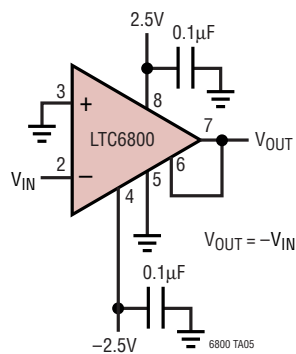
PACKAGE DESCRIPTION

**MS8 Package
8-Lead Plastic MSOP**
(Reference LTC DWG # 05-08-1660)

DETAIL "A"

0.254
(.010)

0° – 6° TYP

GAUGE PLANE

0.53 ± 0.152
(.021 ± .006)

0.18
(.007)

DETAIL "A"

1.10
(.043)
MAX

0.86
(.034)
REF

SEATING
PLANE

0.22 – 0.38
(.009 – .015)
TYP

0.65
(.0256)
BSC

0.127 ± 0.076
(.005 ± .003)

3.00 ± 0.102
(.118 ± .004)
(NOTE 3)

8 7 6 5

0.52
(.0205)
REF

4.90 ± 0.152
(.193 ± .006)

3.00 ± 0.102
(.118 ± .004)
(NOTE 4)

1 2 3 4

0.889 ± 0.127
(.035 ± .005)

3.20 – 3.45
(.126 – .136)

5.23
(.206)
MIN

0.42 ± 0.038
(.0165 ± .0015)
TYP

0.65
(.0256)
BSC

RECOMMENDED SOLDER PAD LAYOUT

MSOP (MS8) 0603

NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

**DD Package
8-Lead Plastic DFN (3mm × 3mm)**
(Reference LTC DWG # 05-08-1698)

PIN 1
TOP MARK

3.00 ±0.10
(4 SIDES)

0.200 REF

0.75 ±0.05

0.00 – 0.05

R = 0.115
TYP

5

0.38 ± 0.10

8

1.65 ± 0.10
(2 SIDES)

4

1

0.28 ± 0.05

0.50 BSC

2.38 ±0.10
(2 SIDES)

BOTTOM VIEW—EXPOSED PAD

0.675 ±0.05

3.5 ±0.05

1.65 ±0.05
(2 SIDES)

2.15 ±0.05

PACKAGE
OUTLINE

0.28 ± 0.05

0.50
BSC

2.38 ±0.05
(2 SIDES)

RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

(DD8) DFN 0203

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
4. EXPOSED PAD SHALL BE SOLDER PLATED

sn6800 6800fas

TYPICAL APPLICATION

Differential Bridge Amplifier

$$GAIN = 1 + \frac{R2}{R1}$$
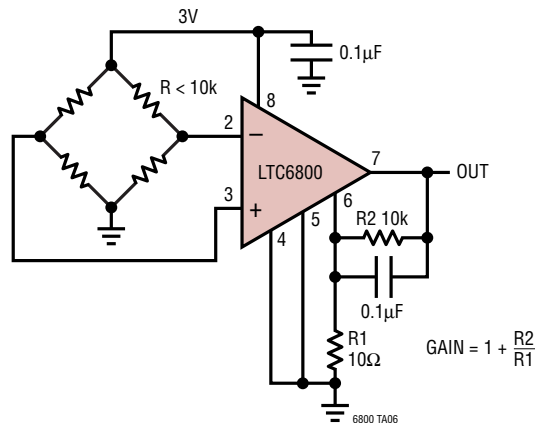
RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1100	Precision Zero Drift Instrumentation Amplifier	Fixed Gains of 10 or 100, 10μV Offset, 50pA Input Bias Current
LT®1101	Precision, Micropower, Single Supply Instrumentation Amplifier	Fixed Gains of 10 or 100, I_S < 105μA
LT1167	Single Resistor Gain Programmable, Precision Instrumentation Amplifier	Single Gain Set Resistor: G = 1 to 10,000, Low Noise: 7.5nV√Hz
LT1168	Low Power Single Resistor Gain Programmable, Precision Instrumentation Amplifier	I_{SUPPLY} = 530μA
LTC1043	Dual Precision Instrumentation Switched-Capacitor Building Block	Rail-to-Rail Input, 120dB CMRR
LT1789-1	Single Supply, Rail-to-Rail Output, Micropower Instrumentation Amplifier	I_{SUPPLY} = 80μA Maximum
LTC2050	Zero-Drift Operation Amplifier	SOT-23 Package, 3μV Max V_{OS}, 30nV/°C Max Drift
LTC2051	Dual Zero-Drift Operational Amplifier	MS8 Package, 3μV Max V_{OS}, 30nV/°C Max Drift
LTC2052	Quad Zero-Drift Operational Amplifier	GN-16 Package, 3μV Max V_{OS}, 30nV/°C Max Drift
LTC2053	Single Supply, Zero Drift, Rail-to-Rail Input and Output Instrumentation Amplifier	MS8 Package, 10μV Max V_{OS}, 50nV/°C Max Drift