

32K x 8 LOW VOLTAGE STATIC RAM

DECEMBER 2002

FEATURES

- Access time: 45, 70 ns
- Low active power: 70 mW
- Low standby power
 - 45 μ W CMOS standby
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Single 3.3V power supply

DESCRIPTION

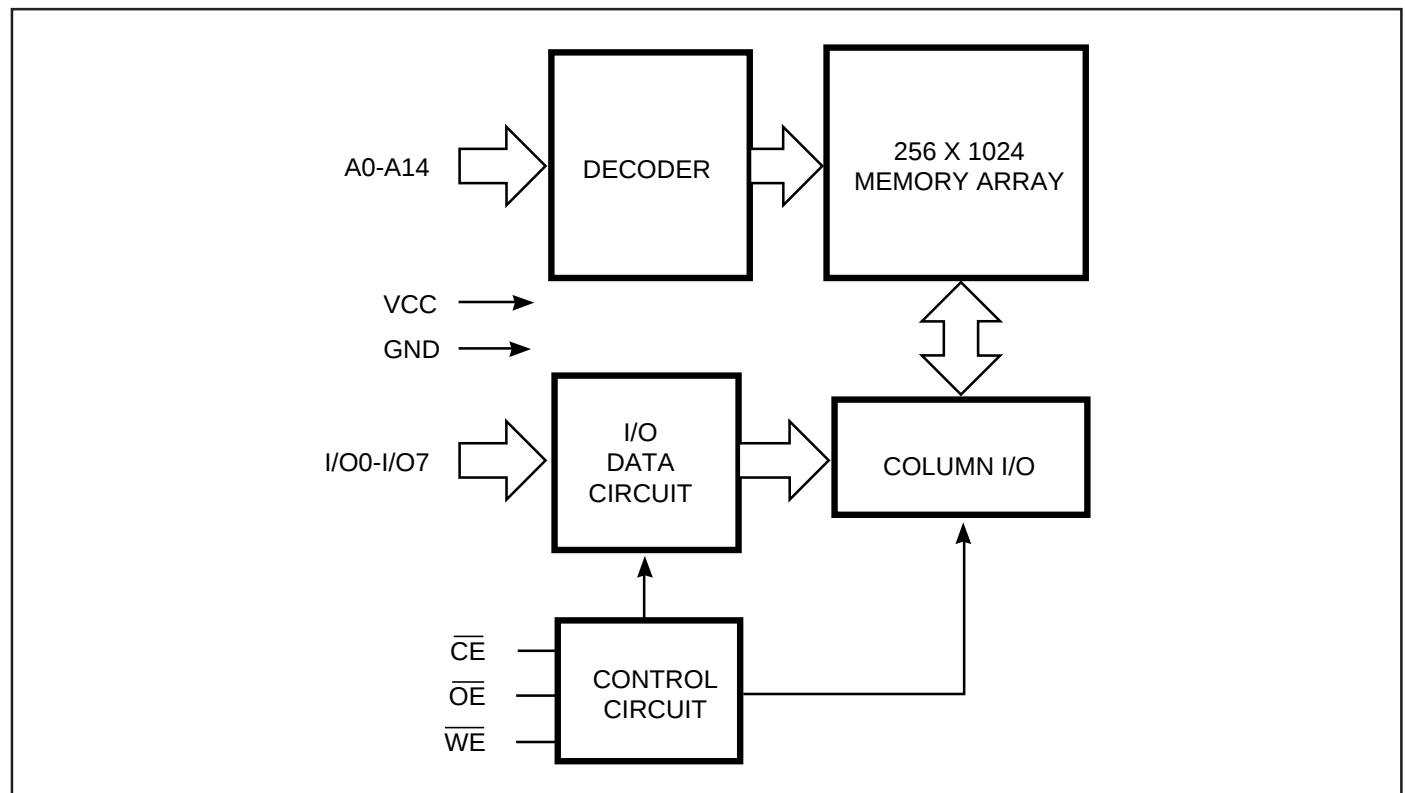
The *ISSI* IS62LV256 is a very high-speed, low power, 32,768-word by 8-bit static RAM. It is fabricated using *ISSI*'s high-performance CMOS double-metal technology.

When $\overline{CE}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation is reduced to 10 μ W (typical) with CMOS input levels.

Easy memory expansion is provided by using an active LOW Chip Enable ($\overline{CE}$) input and an active LOW Output Enable ($\overline{OE}$) input. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory.

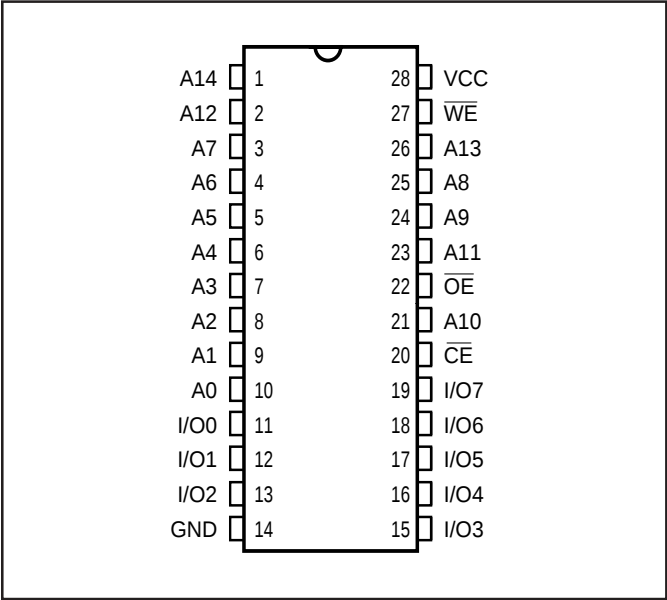
The IS62LV256 is pin compatible with other 32K x 8 SRAMs in 300-mil SOJ, 330-mil plastic SOP, and TSOP (Type I Normal and Reverse Bent) packages.

FUNCTIONAL BLOCK DIAGRAM

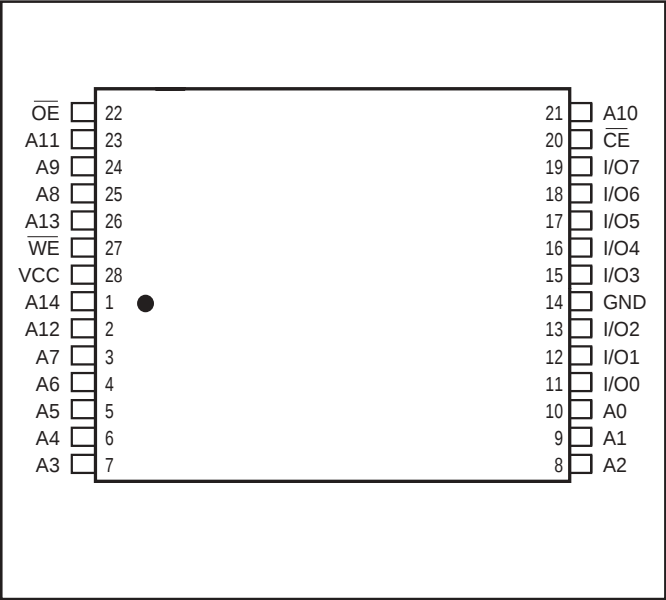


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PIN CONFIGURATION
28-Pin SOJ and SOP



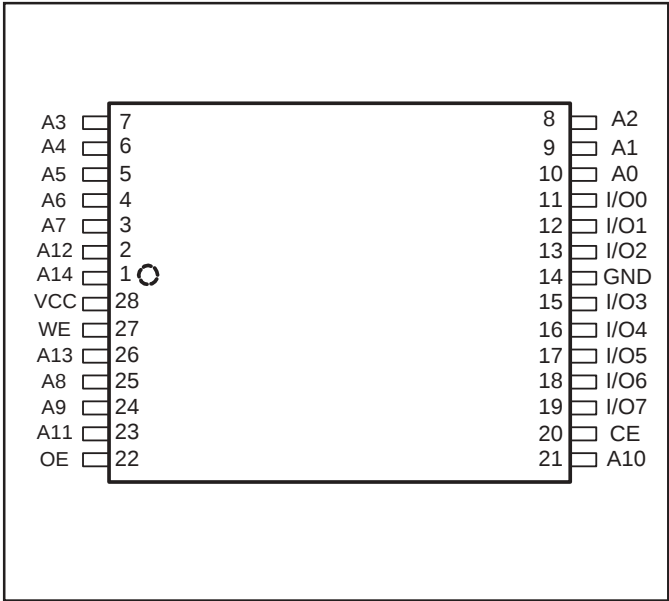
28-Pin TSOP (Type I) (Normal Bent)



PIN DESCRIPTIONS

A0-A14	Address Inputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
Vcc	Power
GND	Ground

28-Pin TSOP (Type I) (Reverse Bent)



TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O Operation	Vcc Current
Not Selected (Power-down)	X	H	X	High-Z	Isb1, Isb2
Output Disabled	H	L	H	High-Z	Icc1, Icc2
Read	H	L	L	DOUT	Icc1, Icc2
Write	L	L	X	DIN	Icc1, Icc2

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
V _{TERM}	Terminal Voltage with Respect to GND	−0.5 to +4.6	V
T _{BIAS}	Temperature Under Bias	−55 to +125	°C
T _{STG}	Storage Temperature	−65 to +150	°C
P _T	Power Dissipation	0.5	W
I _{OUT}	DC Output Current (LOW)	20	mA

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	3.3V ± 5%
Industrial	−40°C to +85°C	3.3V ± 5%

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = −1.0 mA	2.4	—	V	
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 2.1 mA	—	0.4	V	
V _{IH}	Input HIGH Voltage		2.2	V _{CC} + 0.3	V	
V _{IL}	Input LOW Voltage ⁽¹⁾		−0.3	0.8	V	
I _{LI}	Input Leakage	GND ≤ V _{IN} ≤ V _{CC}	Com. Ind.	−2 5	2 5	μA
I _{LO}	Output Leakage	GND ≤ V _{OUT} ≤ V _{CC} , Outputs Disabled	Com. Ind.	−2 −5	2 5	μA

Notes:

1. V_{IL} = −3.0V for pulse width less than 10 ns.
2. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions		-45 ns		-70 ns		Unit
				Min.	Max.	Min.	Max.	
I _{CC1}	V _{CC} Operating Supply Current	V _{CC} = Max., $\overline{CE} = V_{IL}$	Com.	—	20	—	20	mA
		I _{OUT} = 0 mA, f = 0	Ind.	—	30	—	30	
I _{CC2}	V _{CC} Dynamic Operating Supply Current	V _{CC} = Max., $\overline{CE} = V_{IL}$	Com.	—	35	—	30	mA
		I _{OUT} = 0 mA, f = f _{MAX}	Ind.	—	45	—	40	
I _{SB1}	TTL Standby Current (TTL Inputs)	V _{CC} = Max.,	Com.	—	2	—	2	mA
		V _{IN} = V _{IH} or V _{IL} $\overline{CE} \geq V_{IH}$, f = 0	Ind.	—	5	—	5	
I _{SB2}	CMOS Standby Current (CMOS Inputs)	V _{CC} = Max.,	Com.	—	90	—	90	μA
		$\overline{CE} \geq V_{CC} - 0.2V$, V _{IN} ≥ V _{CC} - 0.2V, or V _{IN} ≤ 0.2V, f = 0	Ind.	—	200	—	200	

Notes:

- At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

CAPACITANCE^(1,2)

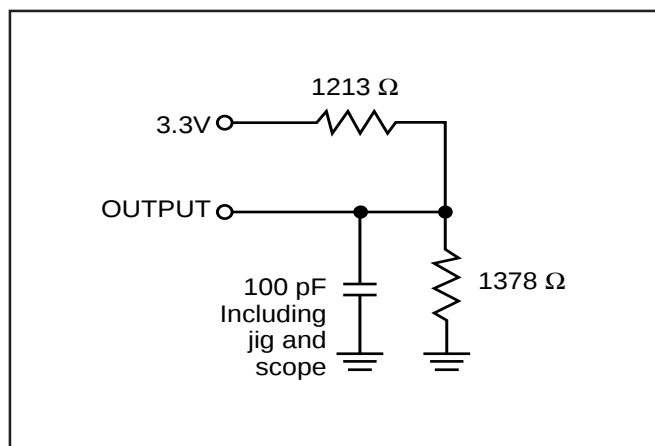
Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5	pF

Notes:

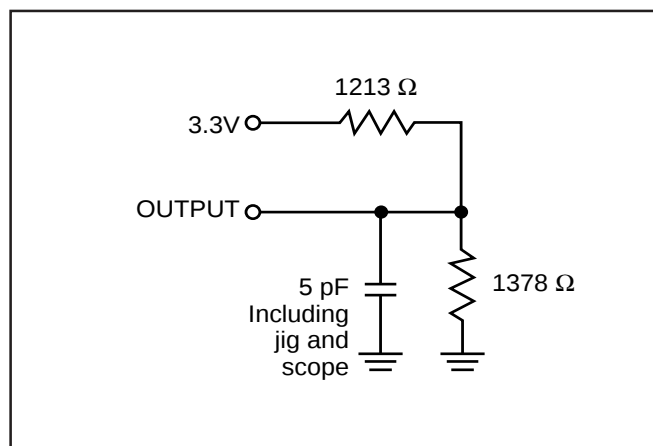
- Tested initially and after any design or process changes that may affect these parameters.
- Test conditions: T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	5 ns
Input and Output Timing and Reference Levels	1.5V
Output Load	See Figures 1a and 1b



Figures 1a



Figures 1b

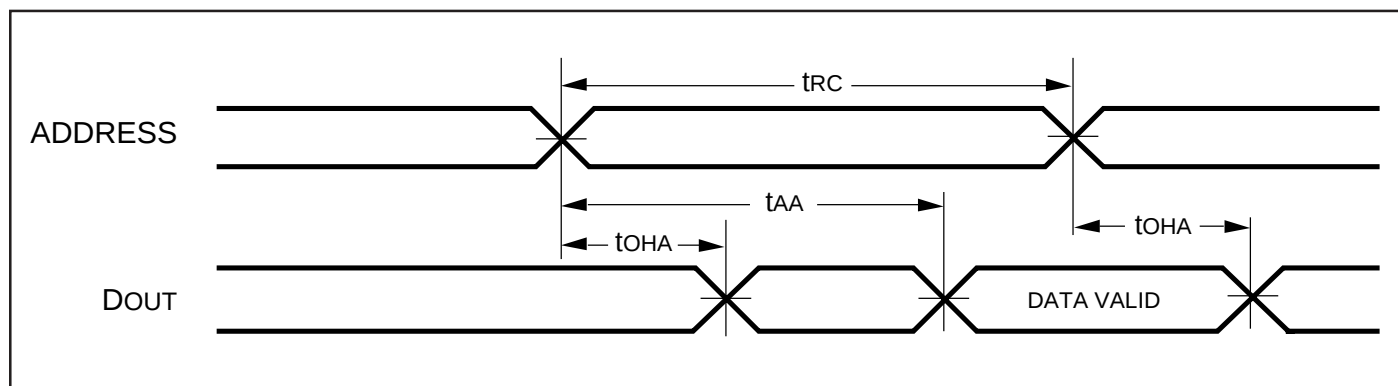
READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	-45 ns		-70 ns		Unit
		Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	45	—	70	—	ns
t_{AA}	Address Access Time	—	45	—	70	ns
t_{OHA}	Output Hold Time	2	—	2	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	45	—	70	ns
t_{DOE}	$\overline{OE}$ Access Time	—	25	—	35	ns
$t_{LZOE}^{(2)}$	$\overline{OE}$ to Low-Z Output	0	—	0	—	ns
$t_{HZOE}^{(2)}$	$\overline{OE}$ to High-Z Output	0	20	0	25	ns
$t_{LZCE}^{(2)}$	$\overline{CE}$ to Low-Z Output	3	—	3	—	ns
$t_{HZCE}^{(2)}$	$\overline{CE}$ to High-Z Output	0	20	0	25	ns
$t_{PU}^{(3)}$	$\overline{CE}$ to Power-Up	0	—	0	—	ns
$t_{PD}^{(3)}$	$\overline{CE}$ to Power-Down	—	30	—	50	ns

Notes:

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
- Tested with the load in Figure 1b. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
- Not 100% tested.

READ CYCLE NO. 1^(1,2)



The timing diagram illustrates the relationship between the ADDRESS, OE, CE, DOUT, and SUPPLY CURRENT signals. Key timing parameters are defined as follows:

- ADDRESS:** Shows the duration of valid address (t_{RC}).
- OE (Output Enable):** Shows the time from OE falling to data becoming valid (t_{AA}), the time from OE rising to data becoming high-impedance (t_{OHA}), and the time from OE rising to data becoming high-impedance (t_{HZOE}).
- CE (Chip Enable):** Shows the time from CE falling to data becoming valid (t_{DOE}), the time from CE rising to data becoming high-impedance (t_{LZOE}), the time from CE falling to data becoming valid (t_{ACE}), the time from CE rising to data becoming high-impedance (t_{HZCE}), and the time from CE falling to data becoming high-impedance (t_{LZCE}).
- DOUT (Data Output):** Shows the time from DOUT becoming high-impedance to data becoming valid (t_{PU}), the time from data becoming valid to DOUT becoming high-impedance (t_{PD}), and the time from DOUT becoming high-impedance to data becoming high-impedance (t_{HZCE}).
- SUPPLY CURRENT:** Shows the time from SUPPLY CURRENT rising to 50% to data becoming valid (t_{PU}), the time from data becoming valid to SUPPLY CURRENT falling to 50% (t_{PD}), and the time from SUPPLY CURRENT falling to 50% to data becoming high-impedance (t_{HZCE}).

1. $\overline{\text{WE}}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{\text{OE}}, \overline{\text{CE}} = \text{V}_{\text{IL}}$.
3. Address is valid prior to or coincident with $\overline{\text{CE}}$ LOW transitions.

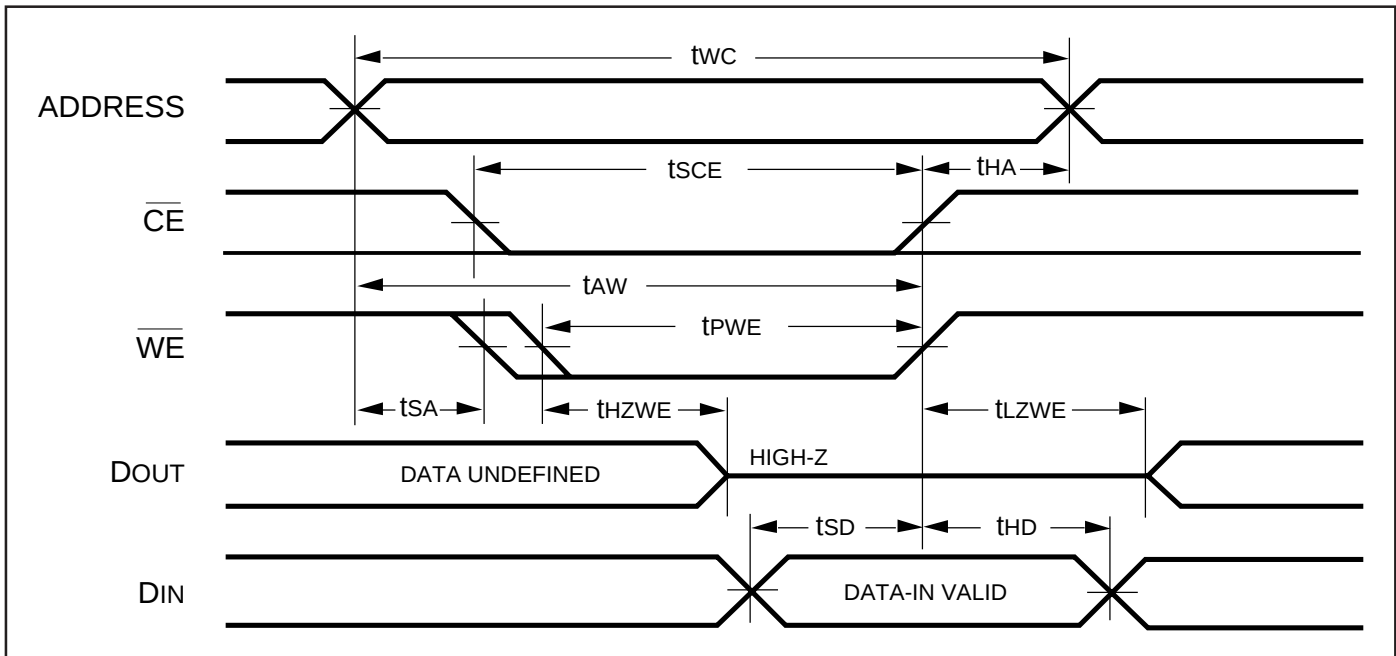
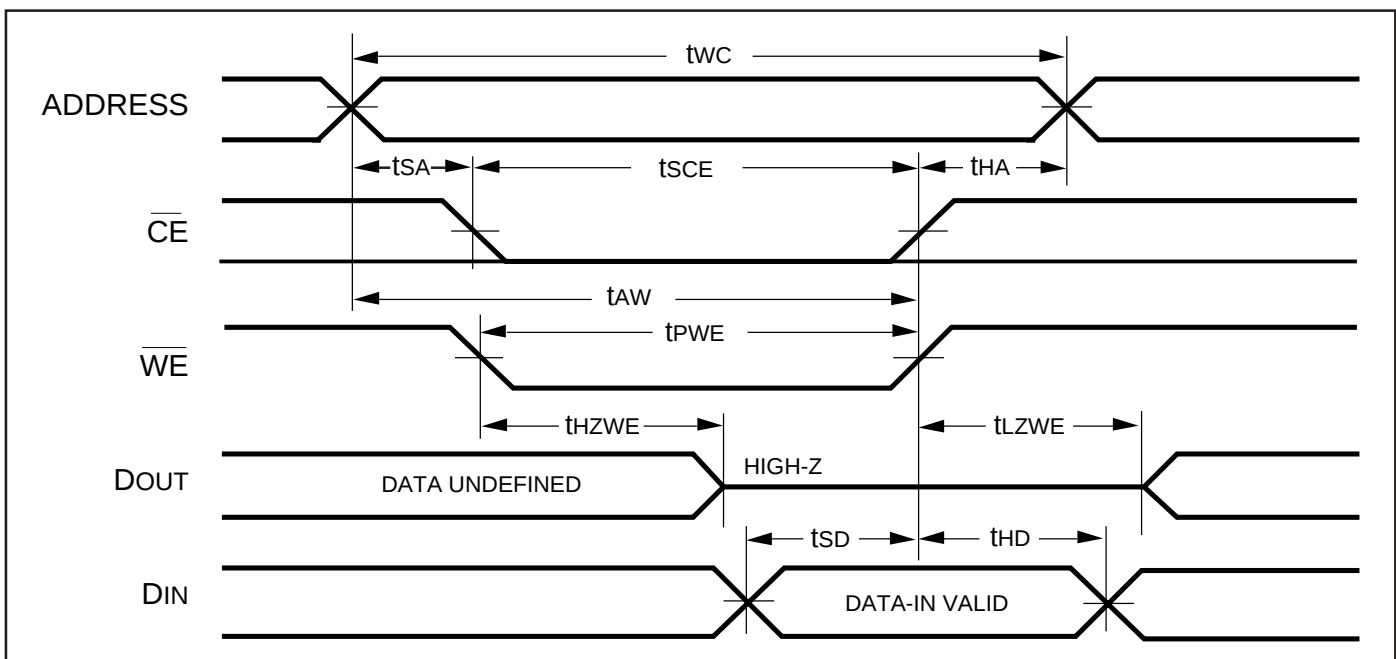
WRITE CYCLE SWITCHING CHARACTERISTICS^(1,2,3) (Over Operating Range)

Symbol	Parameter	-45 ns		-70 ns		Unit
		Min.	Max.	Min.	Max.	
t _{WC}	Write Cycle Time	45	—	70	—	ns
t _{SCE}	$\overline{\text{CE}}$ to Write End	35	—	60	—	ns
t _{AW}	Address Setup Time to Write End	25	—	60	—	ns
t _{HA}	Address Hold from Write End	0	—	0	—	ns
t _{SA}	Address Setup Time	0	—	0	—	ns
t _{PWE⁽⁴⁾}	$\overline{\text{WE}}$ Pulse Width	25	—	55	—	ns
t _{SD}	Data Setup to Write End	20	—	30	—	ns
t _{HD}	Data Hold from Write End	0	—	0	—	ns

Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
4. Tested with $\overline{\text{OE}}$ HIGH.

AC WAVEFORMS

WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)^(1,2)WRITE CYCLE NO. 2 ($\overline{CE}$ Controlled)^(1,2)

Notes:

1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} \cdot V_{IH}$.

ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
45	IS62LV256-45J	300-MIL PLASTIC SOJ
45	IS62LV256-45U	330-MIL SOP
45	IS62LV256-45T	TSOP (TYPE I NORMAL BENT)
70	IS62LV256-70U	330-MIL SOP
70	IS62LV256-70T	TSOP (TYPE I NORMAL BENT)
70	IS62LV256-70RT	TSOP (TYPE I REVERSE BENT)

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
45	IS62LV256-45JI	300-MIL PLASTIC SOJ
45	IS62LV256-45UI	330-mil SOP
45	IS62LV256-45TI	TSOP (TYPE I NORMAL BENT)
70	IS62LV256-70UI	330-mil SOP
70	IS62LV256-70TI	TSOP (TYPE I NORMAL BENT)
70	IS62LV256-70RTI	TSOP (TYPE I REVERSE BENT)