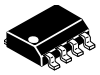
Document Number: MC33285
Rev. 5.0, 2/2007

Dual High-Side TMOS Driver

33285

HIGH-SIDE TMOS DRIVER



D SUFFIX
EF SUFFIX (PB-FREE)
98ASB42564B
8-PIN SOICN

A single input controls the 33285 in driving two external high-side N-Channel TMOS power FETs controlling incandescent or inductive loads. Pulse Width Modulated (PWM) input control to 1.0 kHz is possible. The 33285 contains a common internal charge pump used to enhance the Gate voltage of both FETs.

An external charge capacitor provides access to the charge pump output. Both external FETs are protected against inductive load transients by separate internal source-to-gate dynamic clamps. The power FETs are protected by the 33285 with short-circuit delay time of 800 µs. The device is designed to withstand reverse polarity battery and load dump transients, encountered in automotive applications.

Features

- PWM Capability
- Power TMOS Number One (OUT1) Short-Circuit Detection and Short-Circuit Protection
- Voltage Range 7.0 V ≤ 40 V
- Extended Temperature Range from -40°C ≤ 125°C
- Load Dump Protected
- Overvoltage Detection and Activation of OUT2 During Overvoltage
- Single Input Control for Both Output Stages
- Capacitor Value of 100 nF Connected to Pin CP
- Analog Input Control Measurement Detection
- OUT1 LOAD Leakage Measurement Detection
- Pb-Free Packaging Designated by Suffix Code EF

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MC33285D/R2	-40°C to 125°C	8 SOICN
MCZ33285EF/R2		

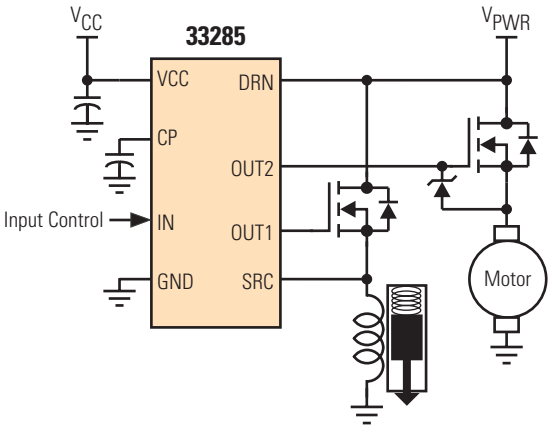


Figure 1. 33285 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

INTERNAL BLOCK DIAGRAM

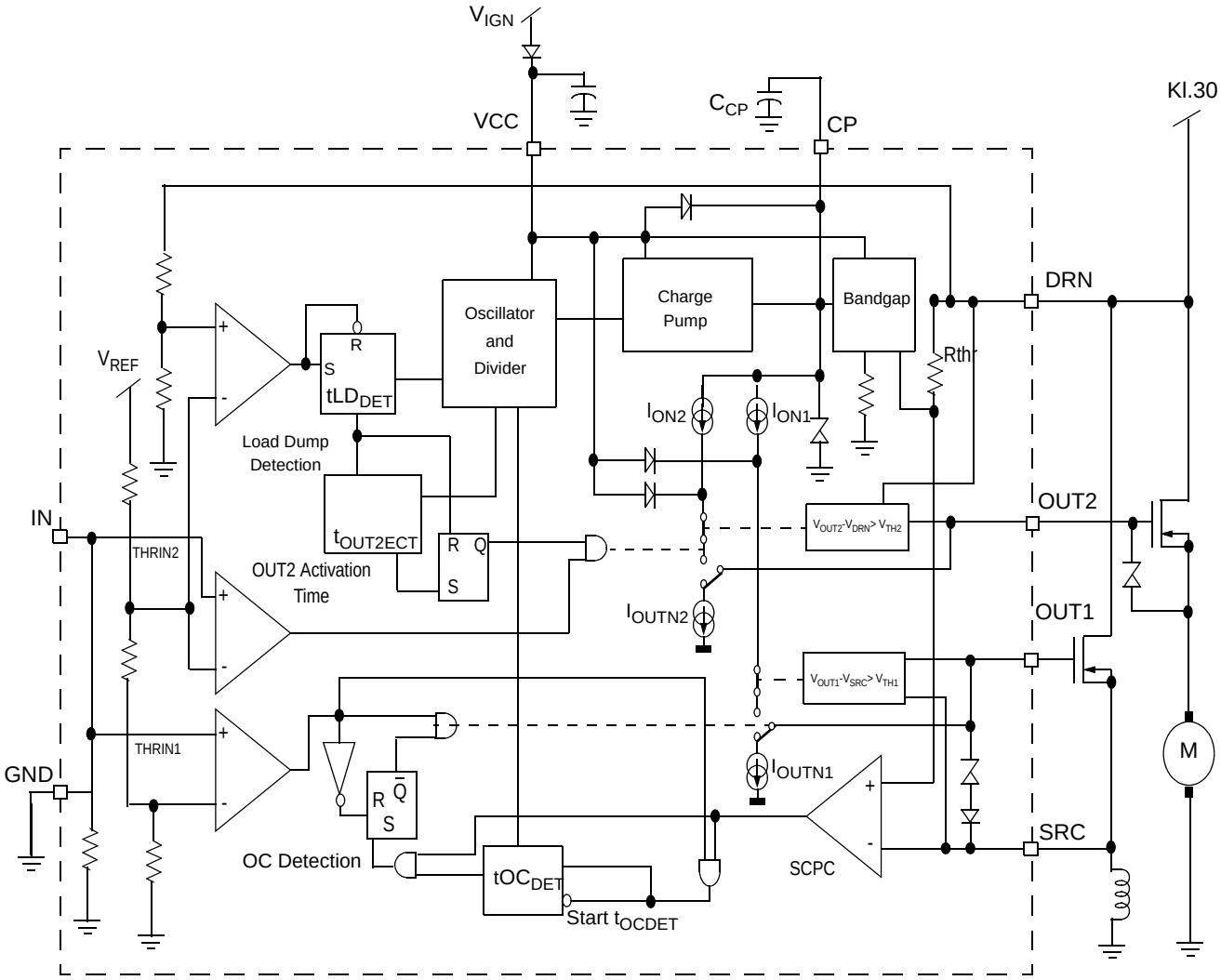


Figure 2. 33285 Simplified Internal Block and Typical Applications Diagram

PIN CONNECTIONS

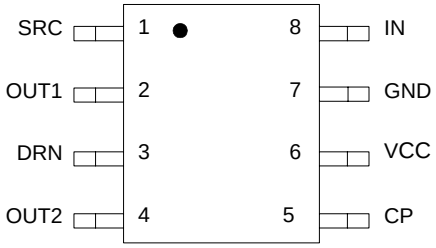


Figure 3. 33285 Pin Connections

Table 1. 33285 Pin Definitions

Pin Number	Pin Name	Formal Name	Definition
1	SRC	Source	OUT2 external FET Source connection
2	OUT1	Output 1	This pin is output number 1
3	DRN	Drain	OUT1 and OUT2 external FET Drain connection
4	OUT2	Output 2	This pin is output number 2
5	CP	Charge Pump	External capacitor connection for internal the Charge Pump
6	VCC	Voltage Power Supply	Battery supply voltage
7	GND	Ground	This is the ground pin.
8	IN	Input	Voltage level sensitive input for OUT1 and OUT2

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
Maximum Voltage at Pins OUT1 and OUT2	V_{OUT}	V_{VCC} + 20	V
Maximum Voltage at Pin CP	V_{CP}	50	V
Input Voltage V_I at DRN	V_{DRN}	-2.0 to 40	V
Input Voltage V_I at SRC	V_{SRC}	-5.0 to 40	V
Input Voltage at Pin VCC	V_{CC}	-2.0 to 40	V
Input Voltage at Pin IN. Condition: -2.0 V < V_{VCC} < 40 V	V_{IN}	-2.0 to V_{VCC}	V
Operational Voltage V_{VCC} at Pin VCC	V_{VCC}	7.0 to V_I	V
THERMAL RATINGS			
Storage Temperature	T_{STG}	-40 to150	°C
Operating Ambient Temperature	T_A	-40 to 125	°C
Peak Package Reflow Temperature During Reflow (1), (2)	T_{PPRT}	Note 2	°C

Notes

1. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
2. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL),
   Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions T_A from -40°C ≤ 125°C, V_{CC} from 7 V ≤ 20 V, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
OVERVOLTAGE AND OVER CURRENT					
Load Dump Activation Time	$t_{OUT2ACT}$	300	460	620	ms
Error Voltage Threshold	V_{DRN} - V_{SRC}	1.12	—	1.44	V
SRC PIN 1					
Leakage Current	ILC_{DET}	15	30	50	mA
Leakage Current Detection Time	tLC_{DET}	130	200	270	µA
DRN PIN 3					
Operating Current (7.0 V < V_{DRN} < 20 V)	I_{DRN}	—	—	1.5	mA
Leakage Current (0 V < V_{DRN} < 20 V, V_{VCC} < 4.0 V)	$I_{LEAK-DRN}$	-5.0	—	5.0	µA
OUT1, PIN 2, AND OUT2 PIN 4					
Output ON Voltage. Charge Pump ON	V_{ON}	—	—	V_{CC} + 15	V
Turn OFF Current, V_{OUT} > 0.5 V	I_{OUTOFF}	66	110	154	µA
V_{CC} PIN 6					
Supply Voltage Range	V_{CC}	7.0	—	40	V
Quiescent Supply Current at V_{CC} = 20 V	I_{CC}	—	—	10	mA
IN PIN 8					
Input Low Voltage OUT1	V_{IL}	—	—	0.7	V
Input High Voltage OUT1	V_{IH}	1.7	—	—	V
Input Hysteresis OUT1 and OUT2	V_{HYS}	0.4	—	—	V
Input Pull Down Current, 0.7 V < V_{IN} < 6.0 V	I_{IN}	7.5	15	16.5	µA
Open Input Voltage	V_{IOP}	—	—	0.7	V
Input Low Voltage OUT2	V_{IL2}	—	—	3.0	V
Input High Voltage OUT2	V_{IH2}	3.9	—	—	V

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

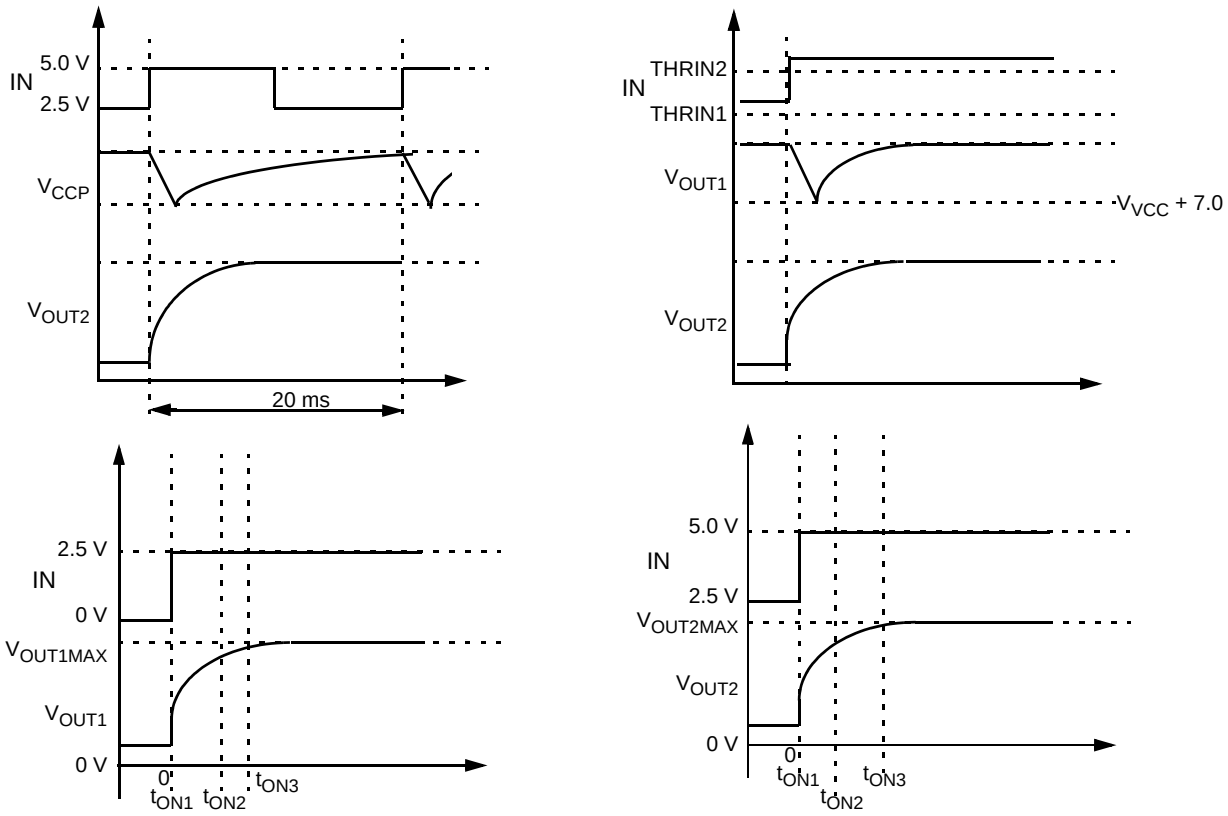
Characteristics noted under conditions T_A from -40°C ≤ 125°C, V_{CC} from 7 V ≤ 20 V, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
OVER VOLTAGE AND OVER CURRENT					
Load Dump Detection Time	tLD_{DET}	250	400	550	µs
Over Current Detection Time	tOC_{DET}	520	800	1080	µs
OUT1 PIN 2, AND OUT2 PIN 4					
Turn ON Time, OUT1: 8.0 nF, 10 µA; OUT2:16 nF, 10 µA	t_{ON}	—	—		ms
-7.0 V < V_{CC} < 10 V, V_{OUT} > V_{CC} + 7.0		—	—	1.5	
-10 V < V_{CC} < 20 V, V_{OUT} > V_{CC} + 11				1.5	

FUNCTIONAL DESCRIPTION

INTRODUCTION

The power FETs are turned ON by charging their gate capacities with a current flowing out of pins OUT1 and OUT2. During PWM, the values of table below are guaranteed. They are measured with 8.0 nF on OUT1 and 16 nF on OUT2. Test condition V_{IN}: ramp 0 V ≤ 2.5 V or 2.5 V ≤ 5.0 V.



VOLTAGE V_{VCC}	MINIMUM $V_{OUT}1$, OUT2 AFTER T_{ON1} = 100 µSEC	MINIMUM $V_{OUT}1$,OUT2 AFTER T_{ON2} = 1.0 µSEC	MINIMUM $V_{OUT}1$,OUT2 AFTER T_{ON3} = 1.5 µSEC
7.0 V < V_{VCC} < 10 V 10 V < V_{VCC} < 20 V 20 V < V_{VCC} < 40 V	V_{VCC} - 0.7 V V_{VCC} - 0.7 V V_{VCC} - 0.7 V	V_{VCC} + 5.95 V V_{VCC} + 9.35 V	V_{VCC} + 7.0 V V_{VCC} + 11 V

Figure 4. Turn On Behavior

The output voltages at OUT1 and OUT2 are limited by controlling the current sources I_{ON1}, I_{ON2} to avoid current flowing through the external or the internal zener diode.

When voltage power supply plus threshold voltage (V_{CC} + V_{TH}) is reached, the current sources are turned OFF.

- Threshold V_{TH1} for OUT1 output voltage control is 7.0 V < V_{TH1} < V_Z
- Threshold V_{TH2} for OUT2 output voltage control is 7.0 V < V_{TH2} < 15 V

Turn Off Characteristics

The power FETs on OUT1 and OUT2 are turned OFF by discharging the gate capacity with the constant discharge current I_{OUTOFF}.

- Discharge current $I_{OUTxOFF}$ is $I_{OUTxOFF}$ = 110 µA condition: V_{OUT} x > 0.5 V (V_{IN} < V_{THRxIN})

- Test conditions for switching OFF the power FETs:
  1. IN open
  2. Stages disabled via pin IN
  3. Stage OUT1 disabled by an over current error

33285

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

INTRODUCTION

The 33285 contains only one charge pump for two outputs.The outputs, OUT1 and OUT2, are switched ON and OFF by the input (IN) .There are three ways to control the outputs:

OUT1 can be switched alone

OUT1 and OUT2 can be switched together

OUT2 can be switched when OUT1 is already on

In the last case, the voltage drop on OUT1 when charging OUT2 is limited.

The external capacitor (C_{CP}) connected to the CHARGE PUMP (CP) pin is used to store the charge continuously delivered by the charge pump. The voltage on this pin is limited to a maximum value V_{CPMAX}. Both outputs are sourced with a constant current from C_{CP} to switch them ON. Additionally, the gates of the power FETs are precharged from voltage power supply (V_{CC}) to prevent C_{CP} from being discharged by a voltage on OUT1 or OUT2, is still lower than V_{VCC}. The values of the output voltages are limited to $V_{OUT1MAX}$ and $V_{OUT2MAX}$.

The power FET on OUT1 is protected against an exceeded gate-source voltage by an internal zener diode.

Channel One protects the N-Channel power FET on OUT1 undercurrent and short-circuit conditions. The drain-source voltage of the FET on OUT1 is checked if Channel One is switched ON. The internal error voltage threshold determines the maximum drain-source voltage allowing the power FET to stay in the ON state. If the measured drain-source voltage exceeds the internal error voltage threshold, the output of the short-circuit protection comparator (SCPC) is enabled. If the output of the SCPC is active longer than t_{OCDET}, output OUT1 is switched OFF.

After switching OFF the power FET on OUT1 by an short-circuit condition, the power FET can only be turned ON again by the input IN.

When switching OFF the power FETs their gate capacities are discharged by a constant current, I_{OUTOFF}.

If the input IN is disconnected, the 33285 outputs, OUT1 and OUT2, are in the OFF state.

If overvoltage occurs on the DRAIN (DRN) pin for a time period longer than t_{LDDET}, OUT2 is switched ON for the time $t_{OUT2ACT}$. In an overvoltage condition OUT1 is OFF if IN is below V_{IH}.

INTERNAL ZENER DIODE

An on-chip zener diode is placed between OUT1 and The SOURCE (SRC). Design guarantees $V_Z > V_{TH1}$. Zener clamping voltage between OUT1 and SRC is $V_{TH1} < V_Z < 20$ V

PWM CAPABILITY

The C_{PIC2} is PWM capable on OUT2. The loss of charge ON C_{CP} when switching ON OUT2 is refreshed until the Start on the next PWM cycle to a value sufficient to guarantee the specified turn ON behavior.

The PWM capability is measured with a test circuit and load conditions:

- PWM cycle is period T = 20 ms ; OUT2 is switched ON from 10 to 90 percent of T
- Test condition V_{IN} ramps 2.5 V ≤ 5.0 V according to PWM cycle defined above

CROSS TALK BETWEEN OUT1 AND OUT2

If output OUT2 is switched ON while OUT1 is already ON, the voltage drop occurring on OUT1 is limited.

Voltage drop on OUT1:

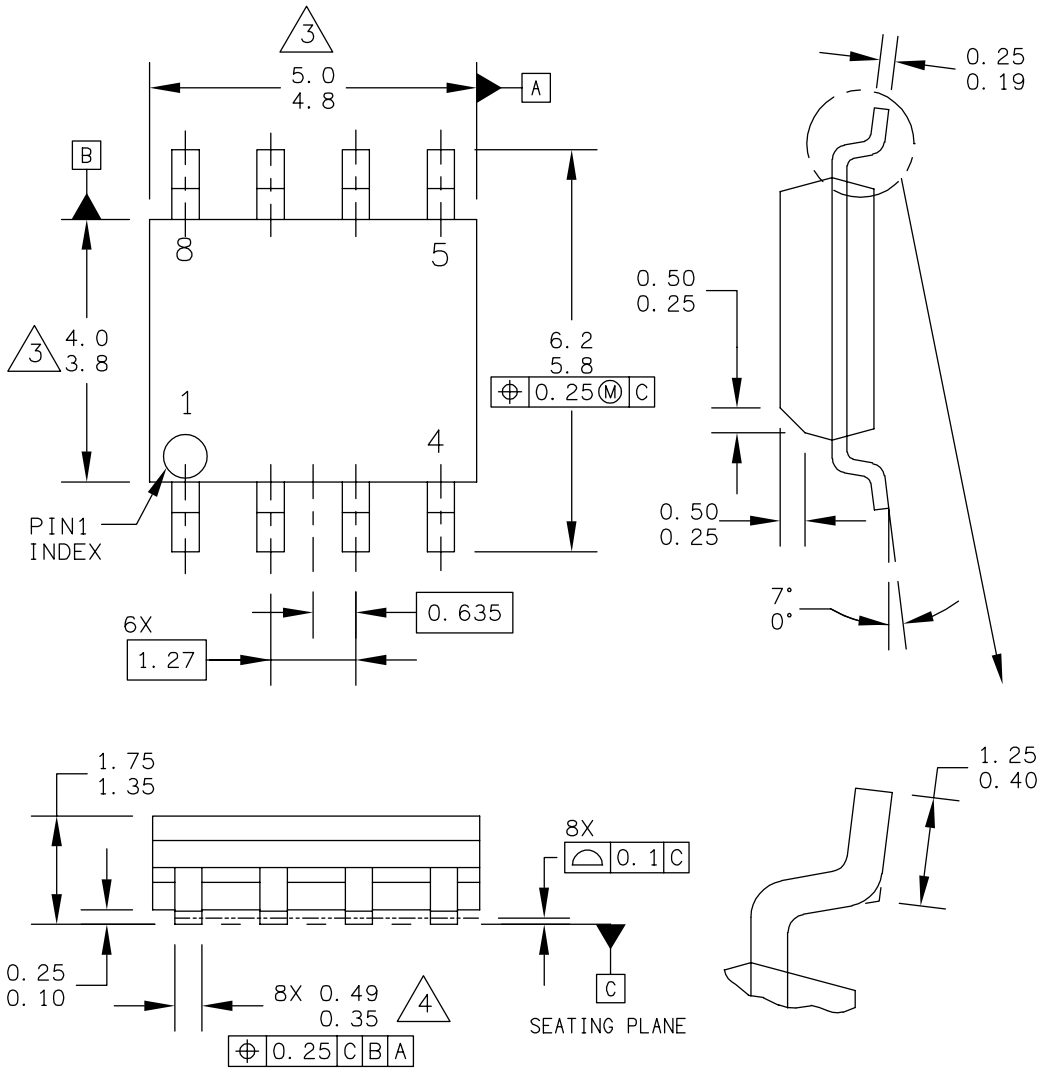
- 10 V < V_{VCC} < 20 V : OUT1 not below V_{VCC} + 7.0 V
- 7.0 V < V_{VCC} < 20 V : OUT1 not below V_{VCC} + 7.0 V

Each time OUT1 is switched ON, a current I_{LCDET} is sourced out of the SRC pin for the time t_{LCDET} to check if there is an external leakage current on that node in the application. The high-side switch on OUT1 is turned ON only if the test is successful.

PACKAGING

PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the “98A” listed below.



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D SUFFIX
EF SUFFIX (PB-FREE)
PLASTIC PACKAGE
98ASB42564B
ISSUE U

33285

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
4.0	9/2006	• Implemented Revision History page • Converted to Freescale format • Added part number MCZ33285EF (Pb-FREE) to Ordering Information
5.0	2/2007	• Added Peak Package Reflow Temperature During Reflow (1), (2) to Maximum Ratings • Added notes (1) and (2)

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