

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- Output Ports Have Equivalent  $26\text{-}\Omega$  Series Resistors, So No External Resistors Are Required
- Typical  $V_{OLP}$  (Output Ground Bounce)  $< 0.8\text{ V}$  at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $> 2\text{ V}$  at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200\text{ pF}$ ,  $R = 0$ )
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

#### description

This 16-bit buffer/driver is designed for 2.7-V to 3.6-V  $V_{CC}$  operation.

The SN74LVC162244 is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides true outputs and symmetrical active-low output-enable ( $\overline{OE}$ ) inputs. The outputs, which are designed to sink up to 12 mA, include  $26\text{-}\Omega$  resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC162244 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

FUNCTION TABLE  
(each 4-bit buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z



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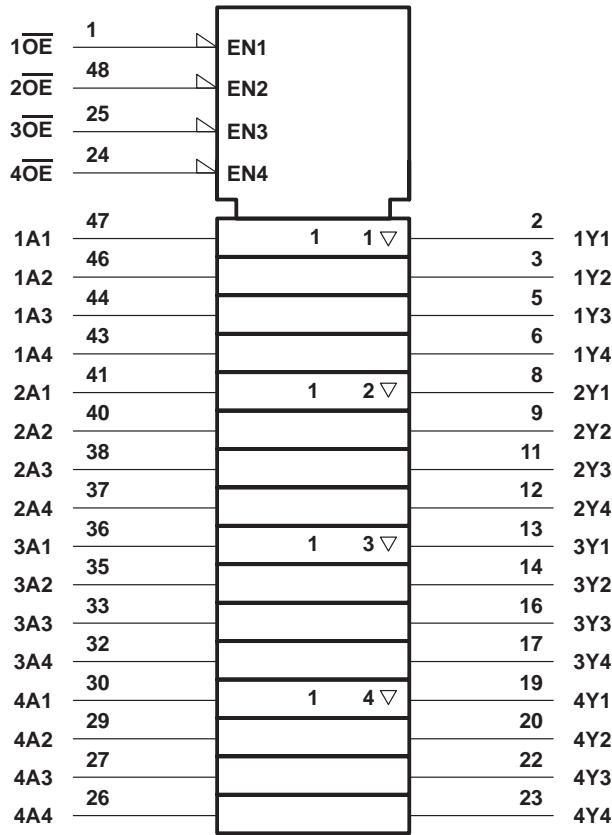


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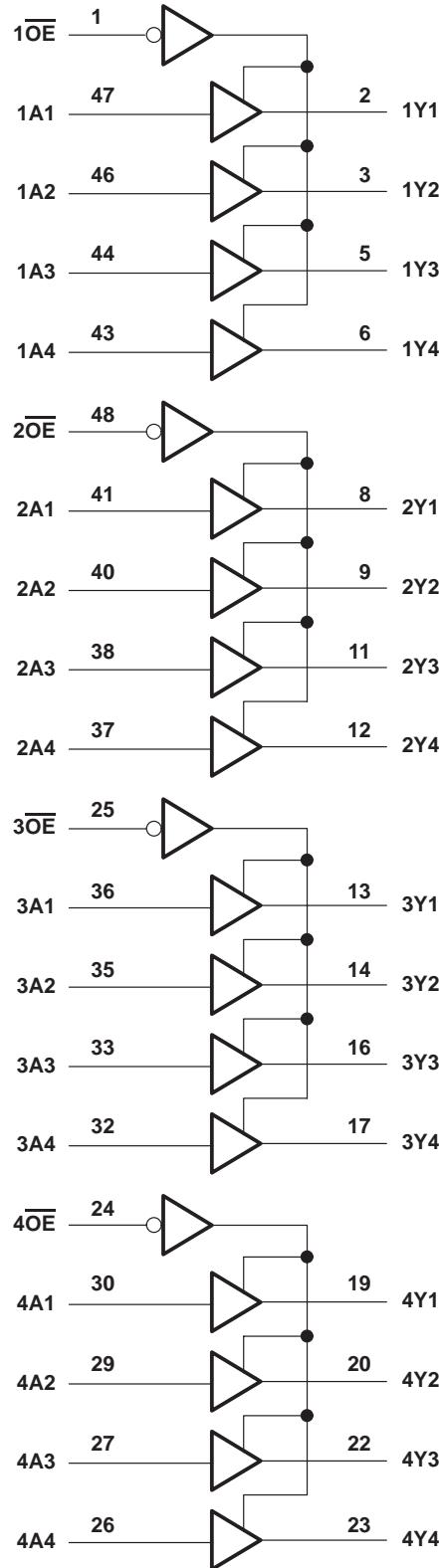
**SN74LVC162244**  
**16-BIT BUFFER/DRIVER**  
**WITH 3-STATE OUTPUTS**

SCAS545 – OCTOBER 1995

**logic symbol†**



**logic diagram (positive logic)**



† This symbol is in accordance with ANSI/IEEE Std 91-1984  
 and IEC Publication 617-12.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 4.6 V
Output voltage range, $V_O$ (see Notes 1 and 2) .....	-0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	±50 mA
Continuous current through $V_{CC}$ or GND .....	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DGG package .....	1 W
DL package .....	1.4 W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. This value is limited to 4.6 V maximum.  
 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.  
 For more information, refer to the *Package Thermal Considerations* application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

**recommended operating conditions (see Note 4)**

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2.7	3.6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V	2	V
$V_{IL}$	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V	0.8	V
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2.7$ V	-8	mA
		$V_{CC} = 3$ V	-12	
$I_{OL}$	Low-level output current	$V_{CC} = 2.7$ V	8	mA
		$V_{CC} = 3$ V	12	
$\Delta t/\Delta V$	Input transition rise or fall rate	0	10	ns/V
$T_A$	Operating free-air temperature	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

**SN74LVC162244**  
**16-BIT BUFFER/DRIVER**  
**WITH 3-STATE OUTPUTS**

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$V_{CC}^{\dagger}$	MIN	TYP <sup>‡</sup>	MAX	UNIT
$V_{OH}$	$I_{OH} = -100 \mu A$	MIN to MAX	$V_{CC} - 0.2$			V
	$I_{OH} = -6 \text{ mA}, V_{IH} = 2 \text{ V}$	3	2.4			
	$I_{OH} = -8 \text{ mA}, V_{IH} = 2 \text{ V}$	2.7	2			
	$I_{OH} = -12 \text{ mA}, V_{IH} = 2 \text{ V}$	3	2			
$V_{OL}$	$I_{OL} = 100 \mu A$	MIN to MAX		0.2		V
	$I_{OL} = 6 \text{ mA}, V_{IL} = 0.8 \text{ V}$	3		0.55		
	$I_{OL} = 8 \text{ mA}, V_{IL} = 0.8 \text{ V}$	2.7		0.6		
	$I_{OL} = 12 \text{ mA}, V_{IL} = 0.8 \text{ V}$	3		0.8		
$I_I$	$V_I = V_{CC}$ or GND	3.6		$\pm 5$	$\mu A$	
$I_I(\text{hold})$	$V_I = 0.8 \text{ V}$	3	75			$\mu A$
	$V_I = 2 \text{ V}$	3	-75			
	$V_I = 0$ to $3.6 \text{ V}$	3.6		$\pm 500$		
$I_{OZ}$	$V_O = V_{CC}$ or GND	3.6		$\pm 10$	$\mu A$	
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6		20	$\mu A$	
$\Delta I_{CC}$	One input at $V_{CC} - 0.6 \text{ V}$ , Other inputs at $V_{CC}$ or GND	2.7 V to 3.6 V		500	$\mu A$	
$C_i$	Control inputs $V_I = V_{CC}$ or GND	3.3		2.5	$pF$	
$C_o$	A or B ports $V_O = V_{CC}$ or GND	3.3		3.5	$pF$	

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

<sup>‡</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

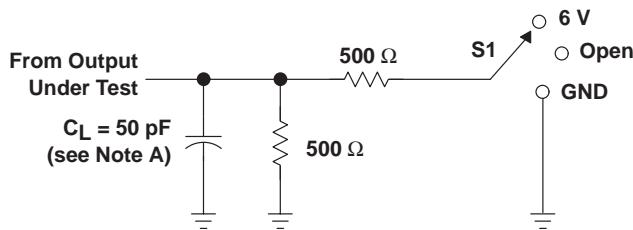
**switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 2.7 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
$t_{pd}$	A	Y	1.5	7	1.5	8	ns
$t_{en}$	$\overline{OE}$	Y	1.5	9	1.5	10	ns
$t_{dis}$	$\overline{OE}$	Y	1.5	7	1.5	8	ns

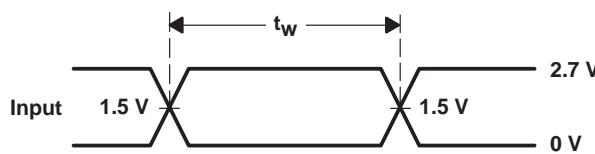
**operating characteristics,  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^\circ\text{C}$**

PARAMETER	TEST CONDITIONS		TYP	UNIT
	Cpd	Power dissipation capacitance per buffer/driver	Outputs enabled	
			Outputs disabled	
			$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	20 2 pF

PARAMETER MEASUREMENT INFORMATION

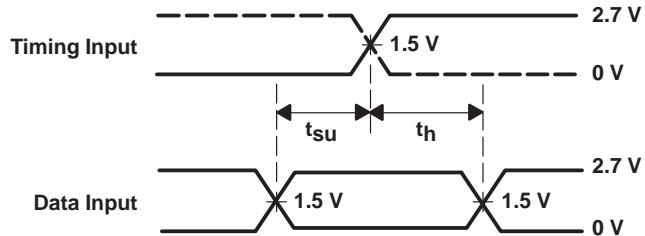


LOAD CIRCUIT FOR OUTPUTS

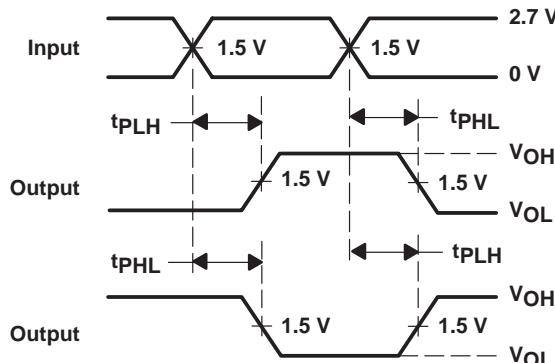


VOLTAGE WAVEFORMS  
PULSE DURATION

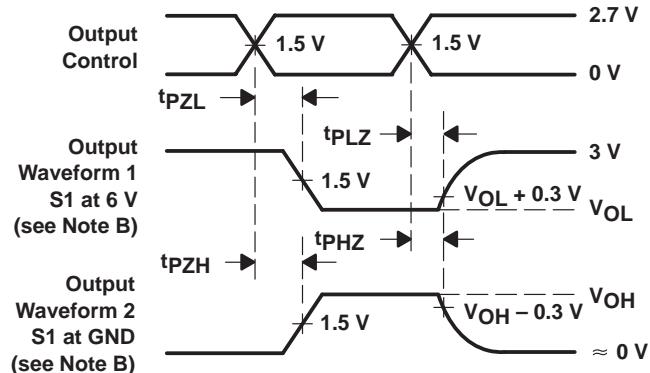
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

NOTES:

- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_f \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
- The outputs are measured one at a time with one transition per measurement.
- $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms



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