DSP Microcomputer

ADSP-2187L

FEATURES

PERFORMANCE

- 19 ns Instruction Cycle Time @ 3.3 Volts, 52 MIPS Sustained Performance
- Single-Cycle Instruction Execution
- Single-Cycle Context Switch
- 3-Bus Architecture Allows Dual Operand Fetches in Every Instruction Cycle
- Multifunction Instructions
- Power-Down Mode Featuring Low CMOS Standby Power Dissipation with 400 Cycle Recovery from Power-Down Condition
- Low Power Dissipation in Idle Mode

INTEGRATION

- ADSP-2100 Family Code Compatible, with Instruction Set Extensions
- 160K Bytes of On-Chip RAM, Configured as 32K Words Program Memory RAM and 32K Words Data Memory RAM
- Dual Purpose Program Memory for Instruction and Data Storage
- Independent ALU, Multiplier/Accumulator and Barrel Shifter Computational Units
- Two Independent Data Address Generators
- Powerful Program Sequencer Provides Zero Overhead Looping Conditional Instruction Execution
- Programmable 16-Bit Interval Timer with Prescaler
- 100-Lead TQFP

SYSTEM INTERFACE

- 16-Bit Internal DMA Port for High Speed Access to On-Chip Memory (Mode Selectable)
- 4 MByte Memory Interface for Storage of Data Tables and Program Overlays (Mode Selectable)
- 8-Bit DMA to Byte Memory for Transparent Program and Data Memory Transfers (Mode Selectable)
- I/O Memory Interface with 2048 Locations Supports Parallel Peripherals (Mode Selectable)
- Programmable Memory Strobe and Separate I/O Memory Space Permits "Glueless" System Design
- Programmable Wait State Generation
- Two Double-Buffered Serial Ports with Companding Hardware and Automatic Data Buffering
- Automatic Booting of On-Chip Program Memory from Byte-Wide External Memory, e.g., EPROM, or Through Internal DMA Port
- Six External Interrupts
- 13 Programmable Flag Pins Provide Flexible System Signaling
- UART Emulation through Software SPORT Reconfiguration
- ICE-Port™ Emulator Interface Supports Debugging in Final Systems

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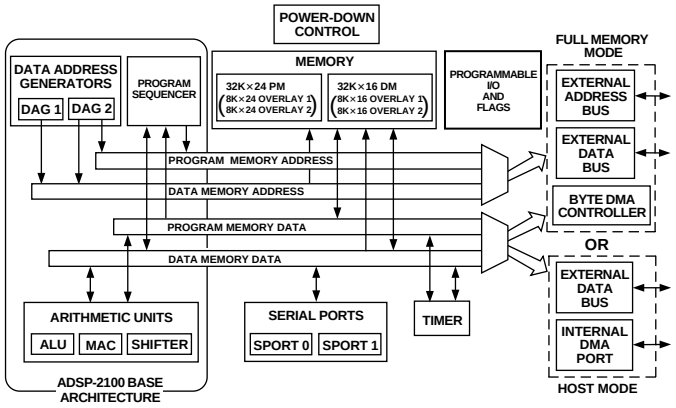
FUNCTIONAL BLOCK DIAGRAM



GENERAL NOTE

This data sheet represents specifications for the ADSP-2187L 3.3 V processor.

GENERAL DESCRIPTION

The ADSP-2187L is a single-chip microcomputer optimized for digital signal processing (DSP) and other high speed numeric processing applications.

The ADSP-2187L combines the ADSP-2100 family base architecture (three computational units, data address generators and a program sequencer) with two serial ports, a 16-bit internal DMA port, a byte DMA port, a programmable timer, Flag I/O, extensive interrupt capabilities and on-chip program and data memory.

The ADSP-2187L integrates 160K bytes of on-chip memory configured as 32K words (24-bit) of program RAM, and 32K words (16-bit) of data RAM. Power-down circuitry is also provided to meet the low power needs of battery operated portable equipment. The ADSP-2187L is available in 100-lead TQFP package.

In addition, the ADSP-2187L supports new instructions, which include bit manipulations—bit set, bit clear, bit toggle, bit test—new ALU constants, new multiplication instruction (x squared), biased rounding, result free ALU operations, I/O memory transfers and global interrupt masking, for increased flexibility.

Fabricated in a high speed, low power, CMOS process, the ADSP-2187L operates with a 19 ns instruction cycle time. Every instruction can execute in a single processor cycle.

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The ADSP-2187L's flexible architecture and comprehensive instruction set allow the processor to perform multiple operations in parallel. In one processor cycle the ADSP-2187L can:

- Generate the next program address
- Fetch the next instruction
- Perform one or two data moves
- Update one or two data address pointers
- Perform a computational operation

This takes place while the processor continues to:

- Receive and transmit data through the two serial ports
- Receive and/or transmit data through the internal DMA port
- Receive and/or transmit data through the byte DMA port
- Decrement timer

DEVELOPMENT SYSTEM

The ADSP-2100 Family Development Software, a complete set of tools for software and hardware system development, supports the ADSP-2187L. The System Builder provides a high level method for defining the architecture of systems under development. The Assembler has an algebraic syntax that is easy to program and debug. The Linker combines object files into an executable file. The Simulator provides an interactive instruction-level simulation with a reconfigurable user interface to display different portions of the hardware environment.

A PROM Splitter generates PROM programmer compatible files. The C Compiler, based on the Free Software Foundation's GNU C Compiler, generates ADSP-2187L assembly source code. The source code debugger allows programs to be corrected in the C environment. The Runtime Library includes over 100 ANSI-standard mathematical and DSP-specific functions.

The EZ-KIT Lite is a hardware/software kit offering a complete development environment for the entire ADSP-21xx family: an ADSP-218x based evaluation board with PC monitor software plus Assembler, Linker, Simulator, and PROM Splitter software. The ADSP-218x EZ-KIT Lite is a low cost, easy to use hardware platform on which you can quickly get started with your DSP software design. The EZ-KIT Lite includes the following features:

- 33 MHz ADSP-218x
- Full 16-bit Stereo Audio I/O with AD1847 SoundPort® Codec
- RS-232 Interface to PC with Windows 3.1 Control Software
- EZ-ICE® Connector for Emulator Control
- DSP Demo Programs

The ADSP-218x EZ-ICE Emulator aids in the hardware debugging of ADSP-2187L system. The emulator consists of hardware, host computer resident software and the target board connector. The ADSP-2187L integrates on-chip emulation support with a 14-pin ICE-Port interface. This interface provides a simpler target board connection requiring fewer mechanical clearance considerations than other ADSP-2100 Family EZ-ICEs. The ADSP-2187L device need not be removed from the target system when using the EZ-ICE, nor are any adapters needed. Due to the small footprint of the EZ-ICE connector, emulation can be supported in final board designs.

The EZ-ICE performs a full range of functions, including:

- In-target operation
- Up to 20 breakpoints
- Single-step or full-speed operation
- Registers and memory values can be examined and altered
- PC upload and download functions
- Instruction-level emulation of program booting and execution
- Complete assembly and disassembly of instructions
- C source-level debugging

See "Designing An EZ-ICE-Compatible Target System" in the *ADSP-2100 Family EZ-Tools Manual* (ADSP-2181 sections) as well as the Designing an EZ-ICE Compatible System section of this data sheet for the exact specifications of the EZ-ICE target board connector.

Additional Information

This data sheet provides a general overview of ADSP-2187L functionality. For additional information on the architecture and instruction set of the processor, see the *ADSP-2100 Family User's Manual, Third Edition*. For more information about the development tools, refer to the ADSP-2100 Family Development Tools Data Sheet.

ARCHITECTURE OVERVIEW

The ADSP-2187L instruction set provides flexible data moves and multifunction (one or two data moves with a computation) instructions. Every instruction can be executed in a single processor cycle. The ADSP-2187L assembly language uses an algebraic syntax for ease of coding and readability. A comprehensive set of development tools supports program development.

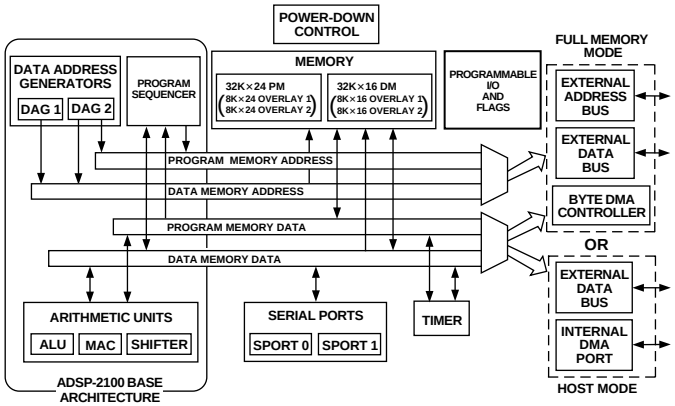

Figure 1. Functional Block Diagram

Figure 1 is an overall block diagram of the ADSP-2187L. The processor contains three independent computational units: the ALU, the multiplier/accumulator (MAC) and the shifter. The computational units process 16-bit data directly and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported. The MAC performs single-cycle multiply, multiply/add and multiply/subtract operations with 40 bits of accumulation. The shifter performs logical and arithmetic shifts, normalization, denormalization and derive exponent operations.

The shifter can be used to efficiently implement numeric format control including multiword and block floating-point representations.

The internal result (R) bus connects the computational units so that the output of any unit may be the input of any unit on the next cycle.

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A powerful program sequencer and two dedicated data address generators ensure efficient delivery of operands to these computational units. The sequencer supports conditional jumps, subroutine calls and returns in a single cycle. With internal loop counters and loop stacks, the ADSP-2187L executes looped code with zero overhead; no explicit jump instructions are required to maintain loops.

Two data address generators (DAGs) provide addresses for simultaneous dual operand fetches (from data memory and program memory). Each DAG maintains and updates four address pointers. Whenever the pointer is used to access data (indirect addressing), it is post-modified by the value of one of four possible modify registers. A length value may be associated with each pointer to implement automatic modulo addressing for circular buffers.

Efficient data transfer is achieved with the use of five internal buses:

- Program Memory Address (PMA) Bus
- Program Memory Data (PMD) Bus
- Data Memory Address (DMA) Bus
- Data Memory Data (DMD) Bus
- Result (R) Bus

The two address buses (PMA and DMA) share a single external address bus, allowing memory to be expanded off-chip, and the two data buses (PMD and DMD) share a single external data bus. Byte memory space and I/O memory space also share the external buses.

Program memory can store both instructions and data, permitting the ADSP-2187L to fetch two operands in a single cycle, one from program memory and one from data memory. The ADSP-2187L can fetch an operand from program memory and the next instruction in the same cycle.

In lieu of the address and data bus for external memory connection, the ADSP-2187L may be configured for 16-bit Internal DMA port (IDMA port) connection to external systems. The IDMA port is made up of 16 data/address pins and five control pins. The IDMA port provides transparent, direct access to the DSPs on-chip program and data RAM.

An interface to low cost byte-wide memory is provided by the Byte DMA port (BDMA port). The BDMA port is bidirectional and can directly address up to four megabytes of external RAM or ROM for off-chip storage of program overlays or data tables.

The byte memory and I/O memory space interface supports slow memories and I/O memory-mapped peripherals with programmable wait state generation. External devices can gain control of external buses with bus request/grant signals ($\overline{BR}$, $\overline{BGH}$, and $\overline{BG}$). One execution mode (Go Mode) allows the ADSP-2187L to continue running from on-chip memory. Normal execution mode requires the processor to halt while buses are granted.

The ADSP-2187L can respond to eleven interrupts. There can be up to six external interrupts (one edge-sensitive, two level-sensitive and three configurable) and seven internal interrupts generated by the timer, the serial ports (SPORTs), the Byte DMA port and the power-down circuitry. There is also a master $\overline{RESET}$ signal. The two serial ports provide a complete synchronous serial interface with optional companding in hardware and a wide variety of framed or frameless data transmit and receive modes of operation.

Each port can generate an internal programmable serial clock or accept an external serial clock.

The ADSP-2187L provides up to 13 general-purpose flag pins. The data input and output pins on SPORT1 can be alternatively configured as an input flag and an output flag. In addition, there are eight flags that are programmable as inputs or outputs and three flags that are always outputs.

A programmable interval timer generates periodic interrupts. A 16-bit count register (TCOUNT) is decremented every *n* processor cycle, where *n* is a scaling value stored in an 8-bit register (TSCALE). When the value of the count register reaches zero, an interrupt is generated and the count register is reloaded from a 16-bit period register (TPERIOD).

Serial Ports

The ADSP-2187L incorporates two complete synchronous serial ports (SPORT0 and SPORT1) for serial communications and multiprocessor communication.

Here is a brief list of the capabilities of the ADSP-2187L SPORTs. For additional information on Serial Ports, refer to the *ADSP-2100 Family User's Manual, Third Edition.*

- SPORTs are bidirectional and have a separate, double-buffered transmit and receive section.
- SPORTs can use an external serial clock or generate their own serial clock internally.
- SPORTs have independent framing for the receive and transmit sections. Sections run in a frameless mode or with frame synchronization signals internally or externally generated. Frame sync signals are active high or inverted, with either of two pulsewidths and timings.
- SPORTs support serial data word lengths from 3 to 16 bits and provide optional A-law and μ-law companding according to CCITT recommendation G.711.
- SPORT receive and transmit sections can generate unique interrupts on completing a data word transfer.
- SPORTs can receive and transmit an entire circular buffer of data with only one overhead cycle per data word. An interrupt is generated after a data buffer transfer.
- SPORT0 has a multichannel interface to selectively receive and transmit a 24- or 32-word, time-division multiplexed, serial bitstream.
- SPORT1 can be configured to have two external interrupts ($\overline{IRQ0}$ and $\overline{IRQ1}$) and the Flag In and Flag Out signals. The internally generated serial clock may still be used in this configuration.

PIN DESCRIPTIONS

The ADSP-2187L will be available in a 100-lead TQFP package. In order to maintain maximum functionality and reduce package size and pin count, some serial port, programmable flag, interrupt and external bus pins have dual, multiplexed functionality. The external bus pins are configured during $\overline{RESET}$ only, while serial port pins are software configurable during program execution. Flag and interrupt functionality is retained concurrently on multiplexed pins. In cases where pin functionality is reconfigurable, the default state is shown in plain text; alternate functionality is shown in italics. See Common-Mode Pin Descriptions.

Common-Mode Pin Descriptions

Pin Name(s)	# of Pins	Input/ Output	Function
$\overline{\text{RESET}}$	1	I	Processor Reset Input
$\overline{\text{BR}}$	1	I	Bus Request Input
$\overline{\text{BG}}$	1	O	Bus Grant Output
$\overline{\text{BGH}}$	1	O	Bus Grant Hung Output
$\overline{\text{DMS}}$	1	O	Data Memory Select Output
$\overline{\text{PMS}}$	1	O	Program Memory Select Output
$\overline{\text{IOMS}}$	1	O	Memory Select Output
$\overline{\text{BMS}}$	1	O	Byte Memory Select Output
$\overline{\text{CMS}}$	1	O	Combined Memory Select Output
$\overline{\text{RD}}$	1	O	Memory Read Enable Output
$\overline{\text{WR}}$	1	O	Memory Write Enable Output
$\overline{\text{IRQ2}}$/	1	I	Edge- or Level-Sensitive Interrupt
PF7		I/O	Request.[1] Programmable I/O Pin
$\overline{\text{IRQL0}}$/	1	I	Level-Sensitive Interrupt Requests[1]
PF6		I/O	Programmable I/O Pin
$\overline{\text{IRQL1}}$/	1	I	Level-Sensitive Interrupt Requests[1]
PF5		I/O	Programmable I/O Pin
$\overline{\text{IRQE}}$/	1	I	Edge-Sensitive Interrupt Requests[1]
PF4		I/O	Programmable I/O Pin
Mode D/	1	I	Mode Select Input—Checked Only During $\overline{\text{RESET}}$
PF3		I/O	Programmable I/O Pin During Normal Operation
Mode C/	1	I	Mode Select Input—Checked Only During $\overline{\text{RESET}}$
PF2		I/O	Programmable I/O Pin During Normal Operation
Mode B/	1	I	Mode Select Input—Checked Only During $\overline{\text{RESET}}$
PF1		I/O	Programmable I/O Pin During Normal Operation
Mode A/	1	I	Mode Select Input—Checked Only During $\overline{\text{RESET}}$
PF0		I/O	Programmable I/O Pin During Normal Operation
CLKIN, XTAL	2	I	Clock or Quartz Crystal Input
CLKOUT	1	O	Processor Clock Output
SPORT0	5	I/O	Serial Port I/O Pins
SPORT1	5	I/O	Serial Port I/O Pins
$\overline{\text{IRQ1:0}}$			Edge- or Level-Sensitive Interrupts,
FI, FO			Flag In, Flag Out[2]
$\overline{\text{PWD}}$	1	I	Power-Down Control Input
$\overline{\text{PWDACK}}$	1	O	Power-Down Control Output
FL0, FL1, FL2	3	O	Output Flags
VDD and GND	16	I	Power and Ground
EZ-Port	9	I/O	For Emulation Use

NOTES
[1]Interrupt/Flag Pins retain both functions concurrently. If IMASK is set to enable the corresponding interrupts, then the DSP will vector to the appropriate interrupt vector address when the pin is asserted, either by external devices, or set as a programmable flag.
[2]SPORT configuration determined by the DSP System Control Register. Software configurable.

Memory Interface Pins

The ADSP-2187L processor can be used in one of two modes, Full Memory Mode, which allows BDMA operation with full external overlay memory and I/O capability, or Host Mode, which allows IDMA operation with limited external addressing capabilities. The operating mode is determined by the state of the Mode C pin during $\overline{\text{RESET}}$ and cannot be changed while the processor is running. See tables for Full Memory Mode Pins and Host Mode Pins for descriptions.

Full Memory Mode Pins (Mode C = 0)

Pin Name(s)	# of Pins	Input/ Output	Function
A13:0	14	O	Address Output Pins for Program, Data, Byte and I/O Spaces
D23:0	24	I/O	Data I/O Pins for Program, Data, Byte and I/O Spaces (8 MSBs are also used as Byte Memory addresses)

Host Mode Pins (Mode C = 1)

Pin Name(s)	# of Pins	Input/ Output	Function
IAD15:0	16	I/O	IDMA Port Address/Data Bus
A0	1	O	Address Pin for External I/O, Program, Data or Byte access
D23:8	16	I/O	Data I/O Pins for Program, Data Byte and I/O spaces
$\overline{\text{IWR}}$	1	I	IDMA Write Enable
$\overline{\text{IRD}}$	1	I	IDMA Read Enable
IAL	1	I	IDMA Address Latch Pin
$\overline{\text{IS}}$	1	I	IDMA Select
$\overline{\text{IACK}}$	1	O	IDMA Port Acknowledge Configurable in Mode D; Open Source

In Host Mode, external peripheral addresses can be decoded using the A0, $\overline{\text{CMS}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$ and $\overline{\text{IOMS}}$ signals

Terminating Unused Pin

The following table shows the recommendations for terminating unused pins.

Pin Terminations

Pin Name	I/O 3-State (Z)	Reset State	Hi-Z* Caused By	Unused Configuration
XTAL	I	I		Float
CLKOUT	O	O		Float
A13:1 or	O (Z)	Hi-Z	$\overline{\text{BR}}$, $\overline{\text{EBR}}$	Float
IAD12:0	I/O (Z)	Hi-Z	$\overline{\text{IS}}$	Float
A0	O (Z)	Hi-Z	$\overline{\text{BR}}$, $\overline{\text{EBR}}$	Float
D23:8	I/O (Z)	Hi-Z	$\overline{\text{BR}}$, $\overline{\text{EBR}}$	Float
D7 or	I/O (Z)	Hi-Z	$\overline{\text{BR}}$, $\overline{\text{EBR}}$	Float
$\overline{\text{IWR}}$	I	I		High (Inactive)

D6 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IRD}$	I	I	$\overline{BR}$, $\overline{EBR}$	High (Inactive)
D5 or	I/O (Z)	Hi-Z		Float
IAL	I	I		Low (Inactive)
D4 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IS}$	I	I		High (Inactive)
D3 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IACK}$	**	**		**
D2:0 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
IAD15:13	I/O (Z)	Hi-Z	$\overline{IS}$	Float
$\overline{PMS}$	O (Z)	O	BR, EBR	Float
$\overline{DMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{BMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IOMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{CMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{RD}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{WR}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{BR}$	I	I		High (Inactive)
$\overline{BG}$	O (Z)	O	EE	Float
$\overline{BGH}$	O	O		Float
$\overline{IRQ2}$/PF7	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float
$\overline{IRQL0}$/PF6	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float
$\overline{IRQL1}$/PF5	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float
$\overline{IRQE}$/PF5	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float
SCLK0	I/O	I		Input = High or Low, Output = Float
RFS0	I/O	I		High or Low
DR0	I	I		High or Low
TFS0	I/O	O		High or Low
DT0	O	O		Float
SCLK1	I/O	I		Input = High or Low, Output = Float
RFS1/$\overline{RQ0}$	I/O	I		High or Low
DR1/$\overline{FI}$	I	I		High or Low
TFS1/$\overline{RQ1}$	I/O	O		High or Low
DT1/$\overline{FO}$	O	O		Float
$\overline{EE}$	I	I		
$\overline{EBR}$	I	I		
$\overline{EBG}$	O	O		
$\overline{ERESET}$	I	I		
$\overline{EMS}$	O	O		
$\overline{EINT}$	I	I		
ECLK	I	I		
ELIN	I	I		
ELOUT	O	O		

NOTES
*Hi-Z = High Impedance.
**Determined by MODE D pin:
Mode D = 0 and in host mode: $\overline{IACK}$ is an active, driven signal and cannot be "wire ORed." If unused, let float.
Mode D = 1 and in host mode: $\overline{IACK}$ is an open source and requires an external pull-down, but multiple $\overline{IACK}$ pins can be "wire ORed" together. If unused, let float.
1. If the CLKOUT pin is not used, turn it OFF.
2. If the Interrupt/Programmable Flag pins are not used, there are two options:
Option 1: When these pins are configured as INPUTS at reset and function as interrupts and input flag pins, pull the pins High (inactive).
Option 2: Program the unused pins as OUTPUTS, set them to 1, and let them float.
3. All bidirectional pins have three-stated outputs. When the pins is configured as an output, the output is Hi-Z (high impedance) when inactive.
4. CLKIN, RESET, and PF3:0 are not included in the table because these pins must be used.

Interrupts

The interrupt controller allows the processor to respond to the eleven possible interrupts and reset with minimum overhead. The ADSP-2187L provides four dedicated external interrupt input pins, $\overline{IRQ2}$, $\overline{IRQL0}$, $\overline{IRQL1}$ and $\overline{IRQE}$. In addition, SPORT1 may be reconfigured for $\overline{IRQ0}$, $\overline{IRQ1}$, FLAG_IN and FLAG_OUT, for a total of six external interrupts. The ADSP-2187L also supports internal interrupts from the timer, the byte DMA port, the two serial ports, software and the power-down control circuit. The interrupt levels are internally prioritized and individually maskable (except power down and reset). The $\overline{IRQ2}$, $\overline{IRQ0}$ and $\overline{IRQ1}$ input pins can be programmed to be either level- or edge-sensitive. $\overline{IRQL0}$ and $\overline{IRQL1}$ are level-sensitive and $\overline{IRQE}$ is edge sensitive. The priorities and vector addresses of all interrupts are shown in Table I.

Table I. Interrupt Priority and Interrupt Vector Addresses

Source of Interrupt	Interrupt Vector Address (Hex)
$\overline{RESET}$ (or Power-Up with PUCR = 1)	0000 (*Highest Priority*)
Power-Down (Nonmaskable)	002C
$\overline{IRQ2}$	0004
$\overline{IRQL1}$	0008
$\overline{IRQL0}$	000C
SPORT0 Transmit	0010
SPORT0 Receive	0014
$\overline{IRQE}$	0018
BDMA Interrupt	001C
SPORT1 Transmit or $\overline{IRQ1}$	0020
SPORT1 Receive or $\overline{IRQ0}$	0024
Timer	0028 (*Lowest Priority*)

Interrupt routines can either be nested with higher priority interrupts taking precedence or processed sequentially. Interrupts can be masked or unmasked with the IMASK register. Individual interrupt requests are logically ANDed with the bits in IMASK; the highest priority unmasked interrupt is then selected. The power-down interrupt is nonmaskable.

The ADSP-2187L masks all interrupts for one instruction cycle following the execution of an instruction that modifies the IMASK register. This does not affect serial port auto-buffering or DMA transfers.

The interrupt control register, ICNTL, controls interrupt nesting and defines the $\overline{IRQ0}$, $\overline{IRQ1}$ and $\overline{IRQ2}$ external interrupts to be either edge- or level-sensitive. The $\overline{IRQE}$ pin is an external edge-sensitive interrupt and can be forced and cleared. The $\overline{IRQL0}$ and $\overline{IRQL1}$ pins are external level-sensitive interrupts.

The IFC register is a write-only register used to force and clear interrupts. On-chip stacks preserve the processor status and are automatically maintained during interrupt handling. The stacks are twelve levels deep to allow interrupt, loop and subroutine nesting. The following instructions allow global enable or disable servicing of the interrupts (including power down), regardless of the state of IMASK. Disabling the interrupts does not affect serial port autobuffering or DMA.

ENA INTS;
DIS INTS;

When the processor is reset, interrupt servicing is enabled.

LOW POWER OPERATION

The ADSP-2187L has three low power modes that significantly reduce the power dissipation when the device operates under standby conditions. These modes are:

- Power-Down
- Idle
- Slow Idle

The CLKOUT pin may also be disabled to reduce external power dissipation.

Power-Down

The ADSP-2187L processor has a low power feature that lets the processor enter a very low power dormant state through hardware or software control. Here is a brief list of power-down features. Refer to the *ADSP-2100 Family User's Manual, Third Edition*, "System Interface" chapter, for detailed information about the power-down feature.

- Quick recovery from power-down. The processor begins executing instructions in as few as 400 CLKIN cycles.
- Support for an externally generated TTL or CMOS processor clock. The external clock can continue running during power-down without affecting the 400 CLKIN cycle recovery.
- Support for crystal operation includes disabling the oscillator to save power (the processor automatically waits 4096 CLKIN cycles for the crystal oscillator to start and stabilize), and letting the oscillator run to allow 400 CLKIN cycle start up.
- Power-down is initiated by either the power-down pin ($\overline{\text{PWD}}$) or the software power-down force bit Interrupt support allows an unlimited number of instructions to be executed before optionally powering down. The power-down interrupt also can be used as a non-maskable, edge-sensitive interrupt.
- Context clear/save control allows the processor to continue where it left off or start with a clean context when leaving the power-down state.
- The $\overline{\text{RESET}}$ pin also can be used to terminate power- down.
- Power-down acknowledge pin indicates when the processor has entered power-down.

Idle

When the ADSP-2187L is in the Idle Mode, the processor waits indefinitely in a low power state until an interrupt occurs. When an unmasked interrupt occurs, it is serviced; execution then continues with the instruction following the *IDLE* instruction. In Idle Mode IDMA, BDMA and autobuffer cycle steals still occur.

Slow Idle

The *IDLE* instruction on the ADSP-2187L slows the processor's internal clock signal, further reducing power consumption. The reduced clock frequency, a programmable fraction of the normal clock rate, is specified by a selectable divisor given in the *IDLE* instruction. The format of the instruction is

IDLE (n);

where n = 16, 32, 64 or 128. This instruction keeps the processor fully functional, but operating at the slower clock rate. While it is in this state, the processor's other internal clock signals, such as SCLK, CLKOUT and timer clock, are reduced by the same ratio. The default form of the instruction, when no clock divisor is given, is the standard *IDLE* instruction.

When the *IDLE (n)* instruction is used, it effectively slows down the processor's internal clock and thus its response time to incoming interrupts. The one-cycle response time of the standard idle state is increased by n, the clock divisor. When an enabled interrupt is received, the ADSP-2187L will remain in the idle state for up to a maximum of n processor cycles (n = 16, 32, 64 or 128) before resuming normal operation.

When the *IDLE (n)* instruction is used in systems that have an externally generated serial clock (SCLK), the serial clock rate may be faster than the processor's reduced internal clock rate. Under these conditions, interrupts must not be generated at a faster rate than can be serviced, due to the additional time the processor takes to come out of the idle state (a maximum of n processor cycles).

SYSTEM INTERFACE

Figure 2 shows a typical basic system configuration with the ADSP-2187L, two serial devices, a byte-wide EPROM, and optional external program and data overlay memories (mode selectable). Programmable wait state generation allows the processor to connect easily to slow peripheral devices. The ADSP-2187L also provides four external interrupts and two serial ports or six external interrupts and one serial port. Host Memory Mode allows access to the full external data bus, but limits addressing to a single address bit (A0) Additional system peripherals can be added in this mode through the use of external hardware to generate and latch address signals.

Clock Signals

The ADSP-2187L can be clocked by either a crystal or a TTL-compatible clock signal.

The CLKIN input cannot be halted, changed during operation or operated below the specified frequency during normal operation. The only exception is while the processor is in the power-down state. For additional information, refer to Chapter 9, *ADSP-2100 Family User's Manual, Third Edition,* for detailed information on this power-down feature.

If an external clock is used, it should be a TTL-compatible signal running at half the instruction rate. The signal is connected to the processor's CLKIN input. When an external clock is used, the XTAL input must be left unconnected.

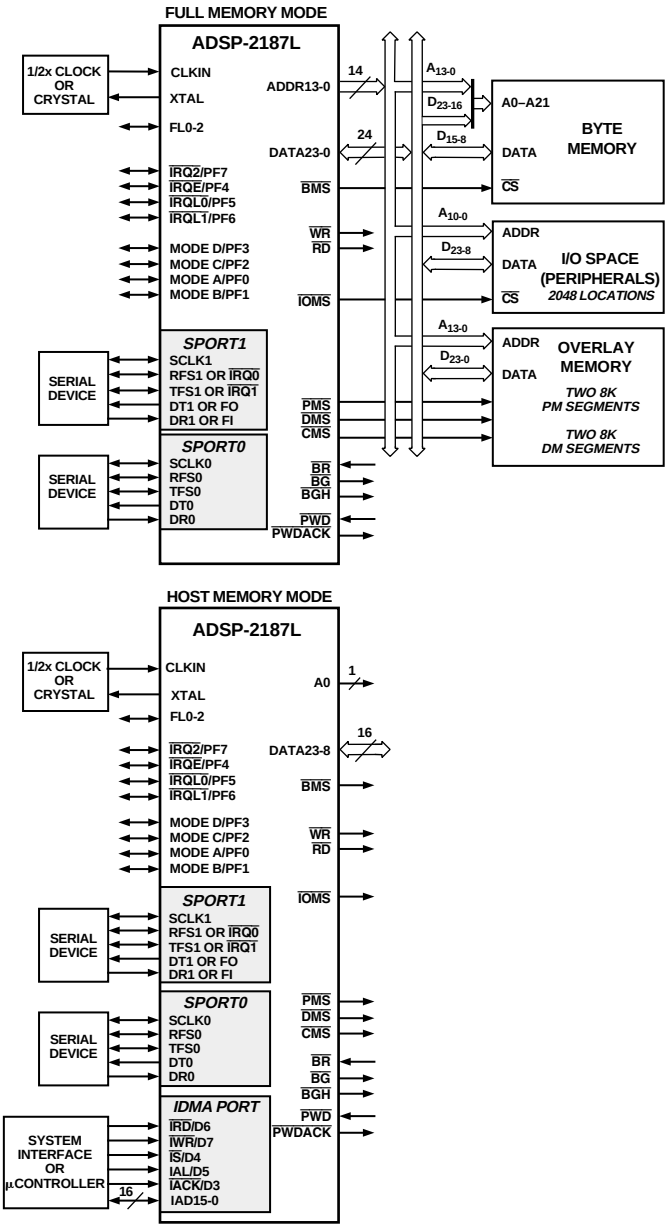


Figure 2. ADSP-2187L Basic System Configuration

The ADSP-2187L uses an input clock with a frequency equal to half the instruction rate; a 26.00 MHz input clock yields a 19 ns processor cycle (which is equivalent to 52 MHz). Normally, instructions are executed in a single processor cycle. All device timing is relative to the internal instruction clock rate, which is indicated by the CLKOUT signal when enabled.

Because the ADSP-2187L includes an on-chip oscillator circuit, an external crystal may be used. The crystal should be connected across the CLKIN and XTAL pins, with two capacitors connected as shown in Figure 3. Capacitor values are dependent on crystal type and should be specified by the crystal manufacturer. A parallel-resonant, fundamental frequency, microprocessor-grade crystal should be used.

A clock output (CLKOUT) signal is generated by the processor at the processor's cycle rate. This can be enabled and disabled by the CLK0DIS bit in the SPORT0 Autobuffer Control Register.

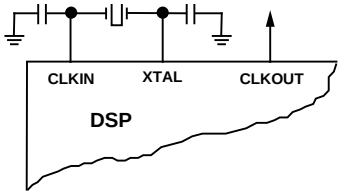


Figure 3. External Crystal Connections

Reset

The $\overline{\text{RESET}}$ signal initiates a master reset of the ADSP-2187L. The $\overline{\text{RESET}}$ signal must be asserted during the power-up sequence to assure proper initialization. $\overline{\text{RESET}}$ during initial power-up must be held long enough to allow the internal clock to stabilize. If $\overline{\text{RESET}}$ is activated any time after power-up, the clock continues to run and does not require stabilization time.

The power-up sequence is defined as the total time required for the crystal oscillator circuit to stabilize after a valid V_{DD} is applied to the processor, and for the internal phase-locked loop (PLL) to lock onto the specific crystal frequency. A minimum of 2000 CLKIN cycles ensures that the PLL has locked, but does not include the crystal oscillator start-up time. During this power-up sequence the $\overline{\text{RESET}}$ signal should be held low. On any subsequent resets, the $\overline{\text{RESET}}$ signal must meet the minimum pulsewidth specification, t_{RSP}.

The $\overline{\text{RESET}}$ input contains some hysteresis; however, if an RC circuit is used to generate the $\overline{\text{RESET}}$ signal, an external Schmidt trigger is recommended.

The master reset sets all internal stack pointers to the empty stack condition, masks all interrupts and clears the MSTAT register. When $\overline{\text{RESET}}$ is released, if there is no pending bus request and the chip is configured for booting, the boot-loading sequence is performed. The first instruction is fetched from on-chip program memory location 0x0000 once boot loading completes.

Table II. Modes of Operations[1]

MODE D[2]	MODE C[3]	MODE B[4]	MODE A[5]	Booting Method
X	0	0	0	BDMA feature is used to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. Chip is configured in Full Memory Mode.[6]
X	0	1	0	No Automatic boot operations occur. Program execution starts at external memory location 0. Chip is configured in Full Memory Mode. BDMA can still be used, but the processor does not automatically use or wait for these operations.
0	1	0	0	BDMA feature is used to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. Chip is configured in Host Mode. $\overline{\text{IACK}}$ has active pull-down. **(REQUIRES ADDITIONAL HARDWARE.)**
0	1	0	1	IDMA feature is used to load any internal memory as desired. Program execution is held off until internal program memory location 0 is written to. Chip is configured in Host Mode.[6] $\overline{\text{IACK}}$ has active pull-down.
1	1	0	0	BDMA feature is used to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. Chip is configured in Host Mode. $\overline{\text{IACK}}$ has active pull-down. **(REQUIRES ADDITIONAL HARDWARE.)**
1	1	0	1	IDMA feature is used to load any internal memory as desired. Program execution is held off until internal program memory location 0 is written to. Chip is configured in Host Mode. $\overline{\text{IACK}}$ requires external pull-down.[6]

NOTES
[1]All mode pins are recognized while $\overline{\text{RESET}}$ is active (low).
[2]When Mode D = 0 and in host mode, $\overline{\text{IACK}}$ is an active, driven signal and cannot be "wire ORed".
When Mode D = 1 and in host mode, $\overline{\text{IACK}}$ is an open source and requires an external pull-down, multiple $\overline{\text{IACK}}$ pins can be "wire ORed" together.
[3]When Mode C = 0, Full Memory enabled. When Mode C = 1, Host Memory Mode enabled.
[4]When Mode B = 0, Auto Booting enabled. When Mode B = 1, no Auto Booting.
[5]When Mode A = 0, BDMA enabled. When Mode A = 1, IDMA enabled.
[6]Considered as standard operating settings. Using these configurations allows for easier design and better memory management.

MODES OF OPERATION

Table II summarizes the ADSP-2187L memory modes.

Setting Memory Mode

Memory Mode selection for the ADSP-2187L is made during chip reset through the use of the Mode C pin. This pin is multiplexed with the DSP's PF2 pin, so care must be taken in how the mode selection is made. The two methods for selecting the value of Mode C are active and passive.

Passive configuration involves the use a pull-up or pull-down resistor connected to the Mode C pin. To minimize power consumption, or if the PF2 pin is to be used as an output in the DSP application, a weak pull-up or pull-down, on the order of 100 kΩ, can be used. This value should be sufficient to pull the pin to the desired level and still allow the pin to operate as a programmable flag output without undue strain on the processor's output driver. For minimum power consumption during power-down, reconfigure PF2 to be an input, as the pull-up or pull-down will hold the pin in a known state, and will not switch.

Active configuration involves the use of a three-statable external driver connected to the Mode C pin. A driver's output enable should be connected to the DSP's $\overline{\text{RESET}}$ signal such that it only drives the PF2 pin when $\overline{\text{RESET}}$ is active (low). When $\overline{\text{RESET}}$ is deasserted, the driver should three-state, thus allowing full use of the PF2 pin as either an input or output. To minimize power consumption during power-down, configure the programmable flag as an output when connected to a three-stated buffer. This ensures that the pin will be held at a constant level and not oscillate should the three-state driver's level hover around the logic switching point.

MEMORY ARCHITECTURE

The ADSP-2187L provides a variety of memory and peripheral interface options. The key functional groups are Program Memory, Data Memory, Byte Memory, and I/O. Refer to the following figures and tables for PM and DM memory allocations in the ADSP-2187L.

PROGRAM MEMORY

Program Memory (Full Memory Mode) is a 24-bit-wide space for storing both instruction opcodes and data. The ADSP-2187L has 32K words of Program Memory RAM on chip, and the capability of accessing up to two 8K external memory overlay spaces using the external data bus**.**

$\overline{\text{IACK}}$ Configuration

Mode D = 0 and in host Mode: $\overline{\text{IACK}}$ is an active, driven signal and cannot be "wire ORed."

Mode D = 1 and in host mode: $\overline{\text{IACK}}$ is an open source and requires an external pull-down, but multiple $\overline{\text{IACK}}$ pins can be "wire ORed" together.

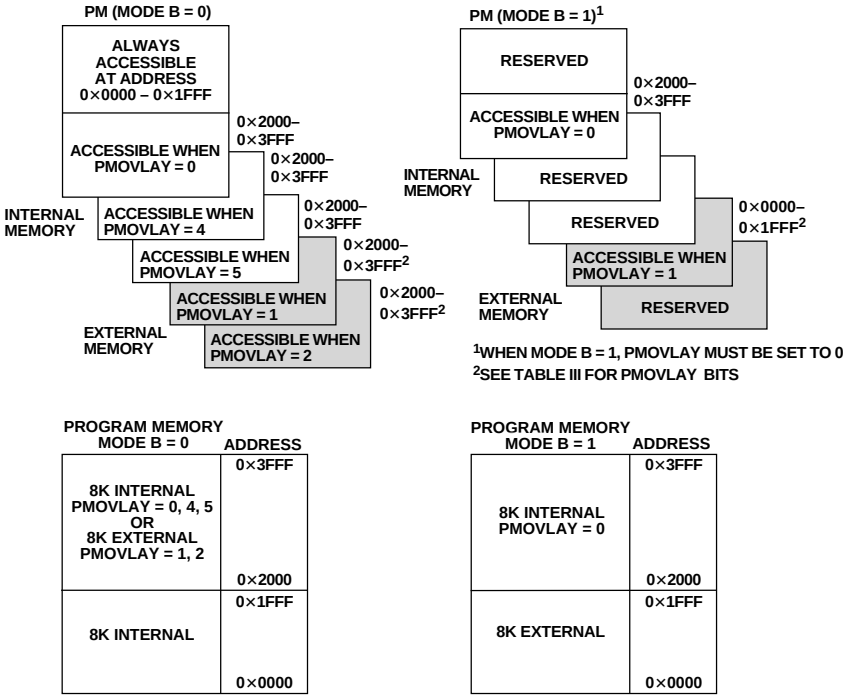


Figure 4. Program Memory

Program Memory (Host Mode) allows access to all internal memory. External overlay access is limited by a single external address line (A0). External program execution is not available in host mode due to a restricted data bus that is 16-bits wide only.

Table III. PMOVLAY Bits

PMOVLAY	Memory	A13	A12:0
0, 4, 5	Internal	Not Applicable	Not Applicable
1	External Overlay 1	0	13 LSBs of Address Between 0x2000 and 0x3FFF
2	External Overlay 2	1	13 LSBs of Address Between 0x2000 and 0x3FFF

DATA MEMORY

Data Memory (Full Memory Mode) is a 16-bit-wide space used for the storage of data variables and for memory-mapped control registers. The ADSP-2187L has 32K words on Data Memory RAM on chip, consisting of 16,352 user-accessible locations and 32 memory-mapped registers. Support also exists for up to two 8K external memory overlay spaces through the external data bus. All internal accesses complete in one cycle. Accesses to external memory are timed using the wait states specified by the DWAIT register.

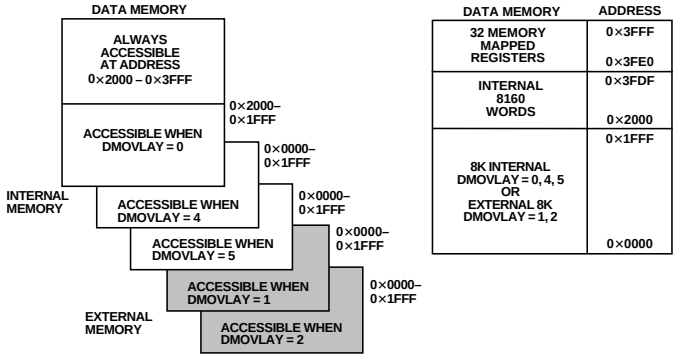


Figure 5. Data Memory Map

Data Memory (Host Mode) allows access to all internal memory. External overlay access is limited by a single external address line (A0). The DMOVLAY bits are defined in Table IV.

Table IV. DMOVLAY Bits

DMOVLAY	Memory	A13	A12:0
0, 4, 5	Internal	Not Applicable	Not Applicable
1	External Overlay 1	0	13 LSBs of Address Between 0x2000 and 0x3FFF
2	External Overlay 2	1	13 LSBs of Address Between 0x2000 and 0x3FFF

I/O Space (Full Memory Mode)
The ADSP-2187L supports an additional external memory space called I/O space. This space is designed to support simple connections to peripherals (such as data converters and external registers) or to bus interface ASIC data registers. I/O space supports 2048 locations of 16-bit wide data. The lower eleven bits of the external address bus are used; the upper three bits are undefined. Two instructions were added to the core ADSP-2100 Family instruction set to read from and write to I/O memory space. The I/O space also has four dedicated 3-bit wait state registers, IOWAIT0-3, that specify up to seven wait states to be automatically generated for each of four regions. The wait states act on address ranges as shown in Table V.

Table V. Wait States

Address Range	Wait State Register
0x000–0x1FF	IOWAIT0
0x200–0x3FF	IOWAIT1
0x400–0x5FF	IOWAIT2
0x600–0x7FF	IOWAIT3

Composite Memory Select ($\overline{\text{CMS}}$)
The ADSP-2187L has a programmable memory select signal that is useful for generating memory select signals for memories mapped to more than one space. The $\overline{\text{CMS}}$ signal is generated to have the same timing as each of the individual memory select signals ($\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$) but can combine their functionality.

Each bit in the CMSSEL register, when set, causes the $\overline{\text{CMS}}$ signal to be asserted when the selected memory select is asserted. For example, to use a 32K word memory to act as both program and data memory, set the $\overline{\text{PMS}}$ and $\overline{\text{DMS}}$ bits in the CMSSEL register and use the $\overline{\text{CMS}}$ pin to drive the chip select of the memory; use either $\overline{\text{DMS}}$ or $\overline{\text{PMS}}$ as the additional address bit.

The $\overline{\text{CMS}}$ pin functions like the other memory select signals, with the same timing and bus request logic. A 1 in the enable bit causes the assertion of the $\overline{\text{CMS}}$ signal at the same time as the selected memory select signal. All enable bits default to 1 at reset, except the $\overline{\text{BMS}}$ bit.

Boot Memory Select ($\overline{\text{BMS}}$) Disable
The ADSP-2187L also lets you boot the processor from one external memory space while using a different external memory space for BDMA transfers during normal operation. You can use the $\overline{\text{CMS}}$ to select the first external memory space for BDMA transfers and $\overline{\text{BMS}}$ to select the second external memory space for booting. The $\overline{\text{BMS}}$ signal can be disabled by setting Bit 3 of the System Control Register to 1. The System Control Register is illustrated in Figure 6.

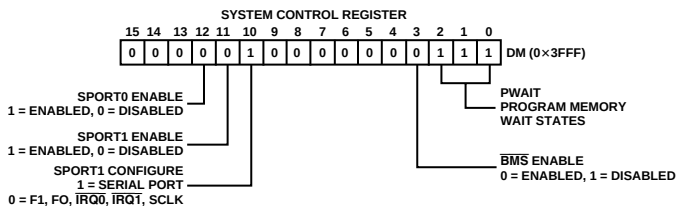


Figure 6. System Control Register

Byte Memory
The byte memory space is a bidirectional, 8-bit-wide, external memory space used to store programs and data. Byte memory is accessed using the BDMA feature. The BDMA Control Register is shown in Figure 7. The byte memory space consists of 256 pages, each of which is 16K × 8.

The byte memory space on the ADSP-2187L supports read and write operations as well as four different data formats. The byte memory uses data bits 15:8 for data. The byte memory uses data bits 23:16 and address bits 13:0 to create a 22-bit address. This allows up to a 4 meg × 8 (32 megabit) ROM or RAM to be used without glue logic. All byte memory accesses are timed by the BMWAIT register.

Byte Memory DMA (BDMA, Full Memory Mode)
The Byte memory DMA controller allows loading and storing of program instructions and data using the byte memory space. The BDMA circuit is able to access the byte memory space while the processor is operating normally, and steals only one DSP cycle per 8-, 16- or 24-bit word transferred.

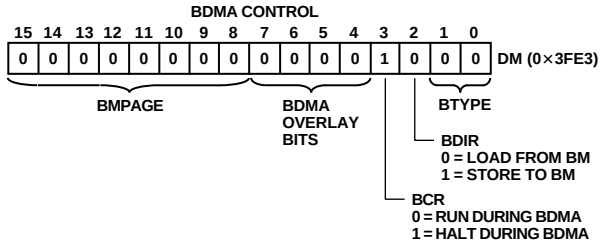


Figure 7. BDMA Control Register

The BDMA circuit supports four different data formats that are selected by the BTYPE register field. The appropriate number of 8-bit accesses are done from the byte memory space to build the word size selected. Table VI shows the data formats supported by the BDMA circuit.

Table VI. Data Formats

BTYPE	Internal Memory Space	Word Size	Alignment
00	Program Memory	24	Full Word
01	Data Memory	16	Full Word
10	Data Memory	8	MSBs
11	Data Memory	8	LSBs

Unused bits in the 8-bit data memory formats are filled with 0s. The BIAD register field is used to specify the starting address for the on-chip memory involved with the transfer. The 14-bit BEAD register specifies the starting address for the external byte memory space. The 8-bit BMPAGE register specifies the starting page for the external byte memory space. The BDIR register field selects the direction of the transfer. Finally the 14-bit BWCOUNT register specifies the number of DSP words to transfer and initiates the BDMA circuit transfers.

BDMA accesses can cross page boundaries during sequential addressing. A BDMA interrupt is generated on the completion of the number of transfers specified by the BWCOUNT register.

The BWCOUNT register is updated after each transfer so it can be used to check the status of the transfers. When it reaches zero, the transfers have finished and a BDMA interrupt is generated. The BMPAGE and BEAD registers must not be accessed by the DSP during BDMA operations.

The source or destination of a BDMA transfer will always be on-chip program or data memory.

When the BWCOUNT register is written with a nonzero value, the BDMA circuit starts executing byte memory accesses with wait states set by BMWAIT. These accesses continue until the count reaches zero. When enough accesses have occurred to create a destination word, it is transferred to or from on-chip memory. The transfer takes one DSP cycle. DSP accesses to external memory have priority over BDMA byte memory accesses.

The BDMA Context Reset bit (BCR) controls whether or not the processor is held off while the BDMA accesses are occurring. Setting the BCR bit to 0 allows the processor to continue operations. Setting the BCR bit to 1 causes the processor to stop execution while the BDMA accesses are occurring, to clear the context of the processor and start execution at address 0 when the BDMA accesses have completed.

The BDMA overlay bits specify the OVLAY memory blocks to be accessed for internal memory.

Internal Memory DMA Port (IDMA Port; Host Memory Mode)

The IDMA Port provides an efficient means of communication between a host system and the ADSP-2187L. The port is used to access the on-chip program memory and data memory of the DSP with only one DSP cycle per word overhead. The IDMA port cannot be used, however, to write to the DSP's memory-mapped control registers. A typical IDMA transfer process is described as follows:

1. Host starts IDMA transfer.
2. Host checks $\overline{\text{IACK}}$ control line to see if the DSP is busy.
3. Host uses $\overline{\text{IS}}$ and IAL control lines to latch either the DMA starting address (IDMAA) or the PM/DM OVLAY selection into the DSP's IDMA control registers.

   If IAD[15] = 1, the value of IAD[7:0] represent the IDMA overlay: IAD[14:8] must be set to 0.

   If IAD[15] = 0, the value of IAD[13:0] represent the starting address of internal memory to be accessed and IAD[14] reflects PM or DM for access.
4. Host uses $\overline{\text{IS}}$ and $\overline{\text{IRD}}$ (or $\overline{\text{IWR}}$) to read (or write) DSP internal memory (PM or DM).
5. Host checks IACK line to see if the DSP has completed the previous IDMA operation.
6. Host ends IDMA transfer.

The IDMA port has a 16-bit multiplexed address and data bus and supports 24-bit program memory. The IDMA port is completely asynchronous and can be written to while the ADSP-2187L is operating at full speed.

The DSP memory address is latched and then automatically incremented after each IDMA transaction. An external device can therefore access a block of sequentially addressed memory by specifying only the starting address of the block. This increases throughput as the address does not have to be sent for each memory access.

IDMA Port access occurs in two phases. The first is the IDMA Address Latch cycle. When the acknowledge is asserted, a 14-bit address and 1-bit destination type can be driven onto the bus by an external device. The address specifies an on-chip memory location; the destination type specifies whether it is a DM or PM access. The falling edge of the address latch signal latches this value into the IDMAA register.

Once the address is stored, data can either be read from or written to the ADSP-2187L's on-chip memory. Asserting the select line ($\overline{\text{IS}}$) and the appropriate read or write line ($\overline{\text{IRD}}$ and $\overline{\text{IWR}}$ respectively) signals the ADSP-2187L that a particular transaction is required. In either case, there is a one-processor-cycle delay for synchronization. The memory access consumes one additional processor cycle.

Once an access has occurred, the latched address is automatically incremented and another access can occur.

Through the IDMAA register, the DSP can also specify the starting address and data format for DMA operation. Asserting the IDMA port select (IS) and address latch enable (IAL) directs the ADSP-2187L to write the address onto the IAD0–14 bus into the IDMA Control Register. If IAD[15] is set to 0, IDMA latches the address. If IAD[15] is set to 1, IDMA latches OVLAY memory. The IDMA OVLAY and address are stored in separate memory-mapped registers. The IDMAA register, shown below, is memory mapped at address DM (0x3FE0). Note that the latched address (IDMAA) cannot be read back by the host. The IDMA OVLAY register is memory mapped at address DM (0x3FE7). See Figures 8 and 9 for more information on IDMA and DMA memory maps.

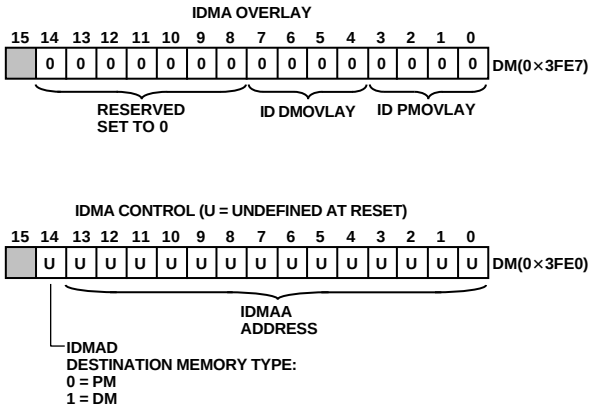


Figure 8. IDMA Control/OVLAY Registers

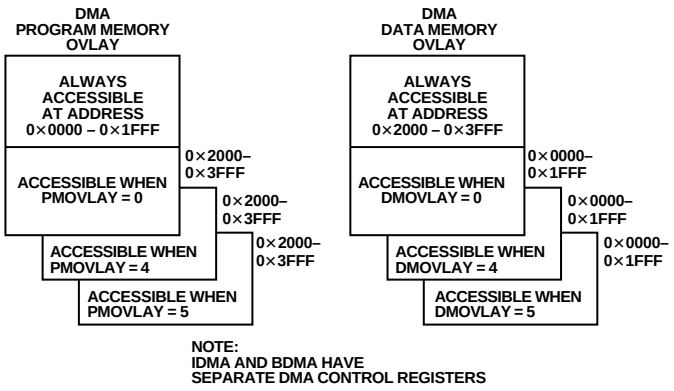


Figure 9. Direct Memory Access-PM and DM Memory Maps

Bootstrap Loading (Booting)

The ADSP-2187L has two mechanisms to allow automatic loading of the internal program memory after reset. The method for booting after reset is controlled by the Mode A, B and C configuration bits.

When the mode pins specify BDMA booting, the ADSP-2187L initiates a BDMA boot sequence when reset is released.

The BDMA interface is set up during reset to the following defaults when BDMA booting is specified: the BDIR, BMPAGE, BIAD and BEAD registers are set to 0, the BTYPE register is set to 0 to specify program memory 24-bit words, and the BWCOUNT register is set to 32. This causes 32 words of on-chip program memory to be loaded from byte memory. These 32 words are used to set up the BDMA to load in the remaining program code. The BCR bit is also set to 1, which causes program execution to be held off until all 32 words are loaded into on-chip program memory. Execution then begins at address 0.

The ADSP-2100 Family Development Software (Revision 5.02 and later) fully supports the BDMA booting feature and can generate byte memory space compatible boot code.

The IDLE instruction can also be used to allow the processor to hold off execution while booting continues through the BDMA interface. For BDMA accesses while in Host Mode, the addresses to boot memory must be constructed externally to the ADSP-2187L. The only memory address bit provided by the processor is A0.

IDMA Port Booting

The ADSP-2187L can also boot programs through its Internal DMA port. If Mode C = 1, Mode B = 0 and Mode A = 1, the ADSP-2187L boots from the IDMA port. IDMA feature can load as much on-chip memory as desired. Program execution is held off until on-chip program memory location 0 is written to.

Bus Request and Bus Grant (Full Memory Mode)

The ADSP-2187L can relinquish control of the data and address buses to an external device. When the external device requires access to memory, it asserts the bus request (BR) signal. If the ADSP-2187L is not performing an external memory access, it responds to the active BR input in the following processor cycle by:

- three-stating the data and address buses and the $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{CMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$ output drivers,
- asserting the bus grant ($\overline{\text{BG}}$) signal, and
- halting program execution.

If Go Mode is enabled, the ADSP-2187L will not halt program execution until it encounters an instruction that requires an external memory access.

If the ADSP-2187L is performing an external memory access when the external device asserts the $\overline{\text{BR}}$ signal, it will not three-state the memory interfaces or assert the $\overline{\text{BG}}$ signal until the processor cycle after the access completes. The instruction does not need to be completed when the bus is granted. If a single instruction requires two external memory accesses, the bus will be granted between the two accesses.

When the $\overline{\text{BR}}$ signal is released, the processor releases the $\overline{\text{BG}}$ signal, reenables the output drivers and continues program execution from the point at which it stopped.

The bus request feature operates at all times, including when the processor is booting and when $\overline{\text{RESET}}$ is active.

The $\overline{\text{BGH}}$ pin is asserted when the ADSP-2187L is ready to execute an instruction, but is stopped because the external bus is already granted to another device. The other device can release the bus by deasserting bus request. Once the bus is released, the ADSP-2187L deasserts $\overline{\text{BG}}$ and $\overline{\text{BGH}}$ and executes the external memory access.

Flag I/O Pins

The ADSP-2187L has eight general purpose programmable input/output flag pins. They are controlled by two memory mapped registers. The PFTYPE register determines the direction, 1 = output and 0 = input. The PFDATA register is used to read and write the values on the pins. Data being read from a pin configured as an input is synchronized to the ADSP-2187L's clock. Bits that are programmed as outputs will read the value being output. The PF pins default to input during reset.

In addition to the programmable flags, the ADSP-2187L has five fixed-mode flags, FLAG_IN, FLAG_OUT, FL0, FL1 and FL2. FL0-FL2 are dedicated output flags. FLAG_IN and FLAG_OUT are available as an alternate configuration of SPORT1.

Note: Pins PF0, PF1, PF2 and PF3 are also used for device configuration during reset.

INSTRUCTION SET DESCRIPTION

The ADSP-2187L assembly language instruction set has an algebraic syntax that was designed for ease of coding and readability. The assembly language, which takes full advantage of the processor's unique architecture, offers the following benefits:

- The algebraic syntax eliminates the need to remember cryptic assembler mnemonics. For example, a typical arithmetic add instruction, such as AR = AX0 + AY0, resembles a simple equation.
- Every instruction assembles into a single, 24-bit word that can execute in a single instruction cycle.
- The syntax is a superset ADSP-2100 Family assembly language and is completely source and object code compatible with other family members. Programs may need to be relocated to utilize on-chip memory and conform to the ADSP-2187L's interrupt vector and reset vector map.
- Sixteen condition codes are available. For conditional jump, call, return or arithmetic instructions, the condition can be checked and the operation executed in the same instruction cycle.
- Multifunction instructions allow parallel execution of an arithmetic instruction with up to two fetches or one write to processor memory space during a single instruction cycle.

DESIGNING AN EZ-ICE-COMPATIBLE SYSTEM

The ADSP-2187L has on-chip emulation support and an ICE-Port, a special set of pins that interface to the EZ-ICE. These features allow in-circuit emulation without replacing the target system processor by using only a 14-pin connection from the target system to the EZ-ICE. Target systems must have a 14-pin connector to accept the EZ-ICE's in-circuit probe, a 14-pin plug. See the ADSP-2100 Family EZ-Tools data sheet for complete information on ICE products.

Issuing the chip reset command during emulation causes the DSP to perform a full chip reset, including a reset of its memory mode. Therefore, it is vital that the mode pins are set correctly PRIOR to issuing a chip reset command from the emulator user interface. If you are using a passive method of maintaining mode information (as discussed in Setting Memory Modes) then it does not matter that the mode information is latched by an emulator reset. However, if you are using the $\overline{\text{RESET}}$ pin as a method of setting the value of the mode pins, then you have to take into consideration the effects of an emulator reset.

One method of ensuring that the values located on the mode pins are those desired is to construct a circuit like the one shown in Figure 10. This circuit forces the value located on the Mode A pin to logic high; regardless if it latched via the $\overline{\text{RESET}}$ or $\overline{\text{ERESET}}$ pin.

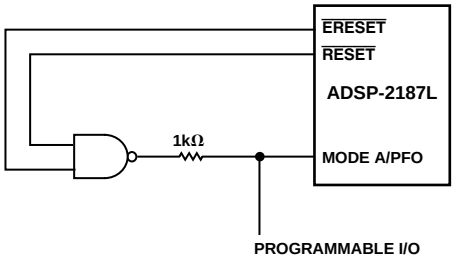


Figure 10. Mode A Pin/EZ-ICE Circuit

The ICE-Port interface consists of the following ADSP-2187L pins:

$\overline{\text{EBR}}$	$\overline{\text{EBG}}$	$\overline{\text{ERESET}}$
$\overline{\text{EMS}}$	$\overline{\text{EINT}}$	ECLK
ELIN	ELOUT	EE

These ADSP-2187L pins must be connected *only* to the EZ-ICE connector in the target system. These pins have no function except during emulation, and do not require pull-up or pull-down resistors. The traces for these signals between the ADSP-2187L and the connector must be kept as short as possible, no longer than three inches.

The following pins are also used by the EZ-ICE:

$\overline{\text{BR}}$	$\overline{\text{BG}}$
$\overline{\text{RESET}}$	GND

The EZ-ICE uses the EE (emulator enable) signal to take control of the ADSP-2187L in the target system. This causes the processor to use its $\overline{\text{ERESET}}$, $\overline{\text{EBR}}$ and $\overline{\text{EBG}}$ pins instead of the $\overline{\text{RESET}}$, $\overline{\text{BR}}$ and $\overline{\text{BG}}$ pins. The $\overline{\text{BG}}$ output is three-stated. These signals do not need to be jumper-isolated in your system.

The EZ-ICE connects to your target system via a ribbon cable and a 14-pin female plug. The ribbon cable is 10 inches in length with one end fixed to the EZ-ICE. The female plug is plugged onto the 14-pin connector (a pin strip header) on the target board.

Target Board Connector for EZ-ICE Probe
The EZ-ICE connector (a standard pin strip header) is shown in Figure 11. You must add this connector to your target board design if you intend to use the EZ-ICE. Be sure to allow enough room in your system to fit the EZ-ICE probe onto the 14-pin connector.

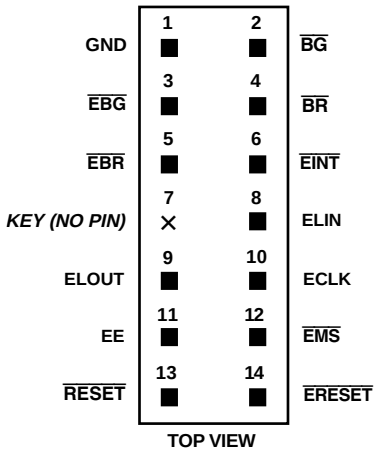


Figure 11. Target Board Connector for EZ-ICE

The 14-pin, 2-row pin strip header is keyed at the Pin 7 location—you must remove Pin 7 from the header. The pins must be 0.025 inch square and at least 0.20 inch in length. Pin spacing should be 0.1 × 0.1 inches. The pin strip header must have at least 0.15 inch clearance on all sides to accept the EZ-ICE probe plug.

Pin strip headers are available from vendors such as 3M, McKenzie and Samtec.

Target Memory Interface
For your target system to be compatible with the EZ-ICE emulator, it must comply with the memory interface guidelines listed below.

PM, DM, BM, IOM and CM
Design your Program Memory (PM), Data Memory (DM), Byte Memory (BM), I/O Memory (IOM) and Composite Memory (CM) external interfaces to comply with worst case device timing requirements and switching characteristics as specified in the DSP's data sheet. The performance of the EZ-ICE may approach published worst case specification for some memory access timing requirements and switching characteristics.

Note: If your target does not meet the worst case chip specification for memory access parameters, you may not be able to emulate your circuitry at the desired CLKIN frequency. Depending on the severity of the specification violation, you may have trouble manufacturing your system as DSP components statistically vary in switching characteristic and timing requirements within published limits.

Restriction: All memory strobe signals on the ADSP-2187L ($\overline{RD}$, $\overline{WR}$, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{CMS}$ and $\overline{IOMS}$) used in your target system must have 10 kΩ pull-up resistors connected when the EZ-ICE is being used. The pull-up resistors are necessary because there are no internal pull-ups to guarantee their state during prolonged three-state conditions resulting from typical EZ-ICE debugging sessions. These resistors may be removed at your option when the EZ-ICE is not being used.

Target System Interface Signals
When the EZ-ICE board is installed, the performance on some system signals changes. Design your system to be compatible with the following system interface signal changes introduced by the EZ-ICE board:

- EZ-ICE emulation introduces an 8 ns propagation delay between your target circuitry and the DSP on the $\overline{RESET}$ signal.
- EZ-ICE emulation introduces an 8 ns propagation delay between your target circuitry and the DSP on the $\overline{BR}$ signal.
- EZ-ICE emulation ignores $\overline{RESET}$ and $\overline{BR}$ when single-stepping.
- EZ-ICE emulation ignores $\overline{RESET}$ and $\overline{BR}$ when in Emulator Space (DSP halted).
- EZ-ICE emulation ignores the state of target $\overline{BR}$ in certain modes. As a result, the target system may take control of the DSP's external memory bus *only* if bus grant ($\overline{BG}$) is asserted by the EZ-ICE board's DSP.

RECOMMENDED OPERATING CONDITIONS

Parameter		K Grade Min	K Grade Max	B Grade Min	B Grade Max	Unit
V_{DD}	Supply Voltage	3.0	3.6	3.0	3.6	V
T_{AMB}	Ambient Operating Temperature	0	+70	–40	+85	°C

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	K/B Grades Min	Typ	Max	Unit
V_{IH}	Hi-Level Input Voltage[1, 2]	@ V_{DD} = max	2.0			V
V_{IH}	Hi-Level CLKIN Voltage	@ V_{DD} = max	2.2			V
V_{IL}	Lo-Level Input Voltage[1, 3]	@ V_{DD} = min			0.8	V
V_{OH}	Hi-Level Output Voltage[1, 4, 5]	@ V_{DD} = min				
		I_{OH} = –0.5 mA	2.4			V
		@ V_{DD} = min				
		I_{OH} = –100 µA[6]	V_{DD} – 0.3			V
V_{OL}	Lo-Level Output Voltage[1, 4, 5]	@ V_{DD} = min				
		I_{OL} = 2 mA			0.4	V
I_{IH}	Hi-Level Input Current[3]	@ V_{DD} = max				
		V_{IN} = V_{DD} max			10	µA
I_{IL}	Lo-Level Input Current[3]	@ V_{DD} = max				
		V_{IN} = 0 V			10	µA
I_{OZH}	Three-State Leakage Current[7]	@ V_{DD} = max				
		V_{IN} = V_{DD} max[8]			10	µA
I_{OZL}	Three-State Leakage Current[7]	@ V_{DD} = max				
		V_{IN} = 0 V[8]			10	µA
I_{DD}	Supply Current (Idle)[9]	@ V_{DD} = 3.3				
		t_{CK} = 19 ns[10]		10		mA
		t_{CK} = 25 ns[10]		8		mA
		t_{CK} = 30 ns[10]		7		mA
I_{DD}	Supply Current (Dynamic)[11]	@ V_{DD} = 3.3				
		T_{AMB} = +25°C				
		t_{CK} = 19 ns[10]		51		mA
		t_{CK} = 25 ns[10]		41		mA
		t_{CK} = 30 ns[10]		34		mA
C_I	Input Pin Capacitance[3, 6, 12]	@ V_{IN} = 2.5 V				
		f_{IN} = 1.0 MHz				
		T_{AMB} = +25°C			8	pF
C_O	Output Pin Capacitance[6, 7, 12, 13]	@ V_{IN} = 2.5 V				
		f_{IN} = 1.0 MHz				
		T_{AMB} = +25°C			8	pF

NOTES
[1]Bidirectional pins: D0–D23, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A1–A13, PF0–PF7.
[2]Input only pins: $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$.
[3]Input only pins: CLKIN, $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$.
[4]Output pins: $\overline{\text{BG}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, PWDACK, A0, DT0, DT1, CLKOUT, FL2–0, $\overline{\text{BGH}}$.
[5]Although specified for TTL outputs, all ADSP-2187L outputs are CMOS-compatible and will drive to V_{DD} and GND, assuming no dc loads.
[6]Guaranteed but not tested.
[7]Three-statable pins: A0–A13, D0–D23, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, DT0, DT1, SCLK0, SCLK1, TFS0, TFS1, RFS0, RFS1, PF0–PF7.
[8]0 V on $\overline{\text{BR}}$.
[9]Idle refers to ADSP-2187L state of operation during execution of IDLE instruction. Deasserted pins are driven to either V_{DD} or GND.
[10]V_{IN} = 0 V and 3 V. For typical figures for supply currents, refer to Power Dissipation section.
[11]I_{DD} measurement taken with all instructions executing from internal memory. 50% of the instructions are multifunction (types 1, 4, 5, 12, 13, 14), 30% are type 2 and type 6, and 20% are idle instructions.
[12]Applies to TQFP package type.
[13]Output pin capacitance is the capacitive load for any three-stated output pin.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . –0.3 V to +4.6 V
Input Voltage . . . . . –0.5 V to V_{DD} + 0.5 V
Output Voltage Swing . . . . . –0.5 V to V_{DD} + 0.5 V
Operating Temperature Range (Ambient) . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (5 sec) TQFP . . . . . +280°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD SENSITIVITY

The ADSP-2187L is an ESD (electrostatic discharge) sensitive device. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur to devices subjected to high energy electrostatic discharges.

The ADSP-2187L features proprietary ESD protection circuitry to dissipate high energy discharges (Human Body Model). Per method 3015 of MIL-STD-883, the ADSP-2187L has been classified as a Class 1 device.

Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination before devices are removed.

TIMING PARAMETERS

GENERAL NOTES

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add up parameters to derive longer times.

TIMING NOTES

Switching Characteristics specify how the processor changes its signals. You have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell you what the processor will do in a given circumstance. You can also use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing Requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

MEMORY TIMING SPECIFICATIONS

The table below shows common memory device specifications and the corresponding ADSP-2187L timing parameters, for your convenience.

Memory Device Specification	ADSP-2187L Timing Parameter	Timing Parameter Definition
Address Setup to Write Start	t_{ASW}	A0–A13, $\overline{xMS}$ Setup before $\overline{WR}$ Low
Address Setup to Write End	t_{AW}	A0–A13, $\overline{xMS}$ Setup before $\overline{WR}$ Deasserted
Address Hold Time	t_{WRA}	A0–A13, $\overline{xMS}$ Hold before $\overline{WR}$ Low
Data Setup Time	t_{DW}	Data Setup before $\overline{WR}$ High
Data Hold Time	t_{DH}	Data Hold after $\overline{WR}$ High
$\overline{OE}$ to Data Valid	t_{RDD}	$\overline{RD}$ Low to Data Valid
Address Access Time	t_{AA}	A0–A13, $\overline{xMS}$ to Data Valid

$\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{CMS}$, $\overline{IOMS}$.

FREQUENCY DEPENDENCY FOR TIMING SPECIFICATIONS

t_{CK} = Instruction Clock Period. t_{CKI} = External Clock Period. t_{CK} is defined as $0.5t_{CKI}$. The ADSP-2187L uses an input clock with a frequency equal to half the instruction rate: a 26 MHz input clock (which is equivalent to 38 ns) yields a 19 ns processor cycle (equivalent to 52 MHz). t_{CK} values within the range of $0.5t_{CKI}$ period should be substituted for all relevant timing parameters to obtain the specification value.

Example: $t_{CKH} = 0.5t_{CK} – 7$ ns = 0.5 (19 ns) – 7 ns = 2.5 ns

OUTPUT DRIVE CURRENTS

Figure 12 shows typical I-V characteristics for the output drivers of the ADSP-2187L. The curves represent the current drive capability of the output drivers as a function of output voltage.

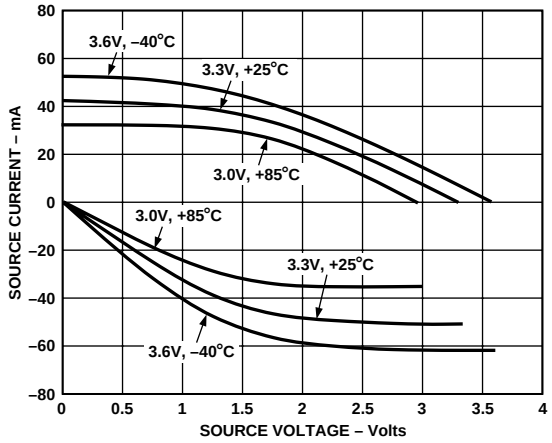
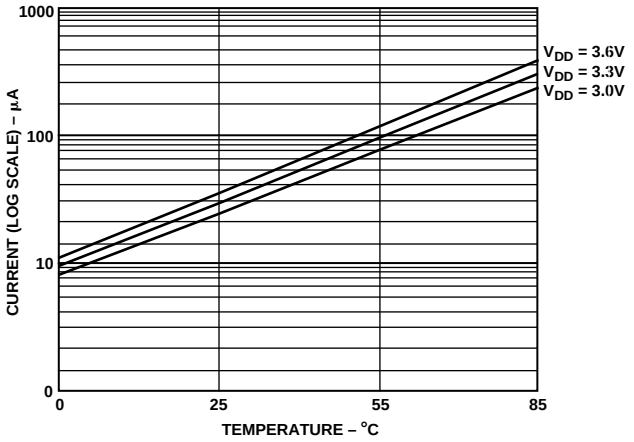


Figure 12. Typical Drive Currents

Figure 13 shows the typical power-down supply current.



NOTES:
1. REFLECTS ADSP-2187L OPERATION IN LOWEST POWER MODE. (SEE "SYSTEM INTERFACE" CHAPTER OF THE *ADSP-2100 FAMILY USER'S MANUAL* FOR DETAILS.)
2. CURRENT REFLECTS DEVICE OPERATING WITH NO INPUT LOADS.

Figure 13. Power-Down Supply Current (Typical)

POWER DISSIPATION

To determine total power dissipation in a specific application, the following equation should be applied for each output:

$$C \times V_{DD}^2 \times f$$

C = load capacitance, f = output switching frequency.

Example:

In an application where external data memory is used and no other outputs are active, power dissipation is calculated as follows:

Assumptions:

- External data memory is accessed every cycle with 50% of the address pins switching.
- External data memory writes occur every other cycle with 50% of the data pins switching.
- Each address and data pin has a 10 pF total load at the pin.
- The application operates at V_{DD} = 3.3 V and t_{CK} = 34.7 ns.

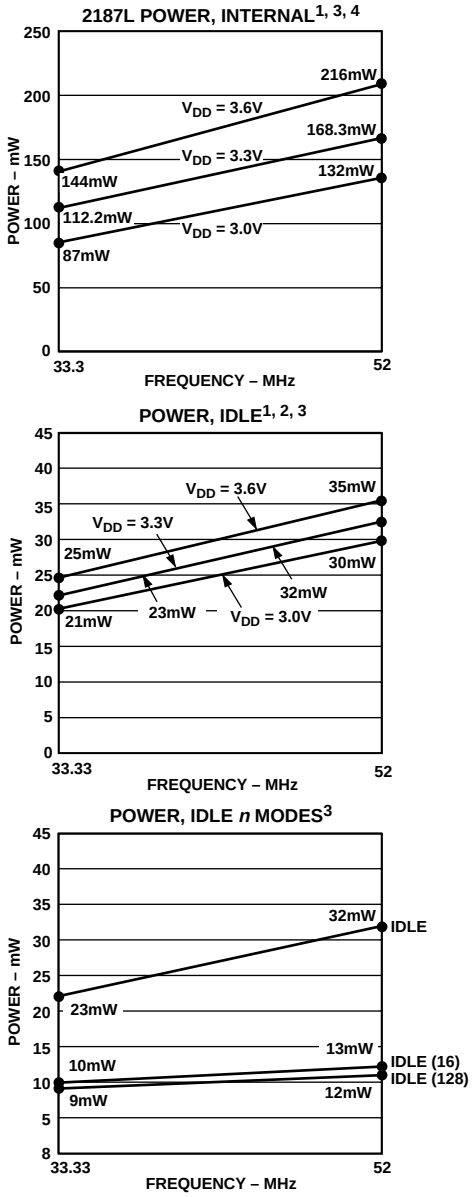
Total Power Dissipation = P_{INT} + $(C \times V_{DD}^2 \times f)$

P_{INT} = internal power dissipation from Power vs. Frequency graph, see Figure 14.

$(C \times V_{DD}^2 \times f)$ is calculated for each output:

	# of Pins	× C	× V_{DD}^2	× f	
Address, $\overline{DMS}$	8	× 10 pF	× 3.3^2 V	× 33.3 MHz	= 29.0 mW
Data Output, $\overline{WR}$	9	× 10 pF	× 3.3^2 V	× 16.67 MHz	= 16.3 mW
$\overline{RD}$	1	× 10 pF	× 3.3^2 V	× 16.67 MHz	= 1.8 mW
CLKOUT	1	× 10 pF	× 3.3^2 V	× 33.3 MHz	= 3.6 mW
					50.7 mW

Total power dissipation for this example is P_{INT} + 50.7 mW.



VALID FOR ALL TEMPERATURE GRADES.
1POWER REFLECTS DEVICE OPERATING WITH NO OUTPUT LOADS.
2IDLE REFERS TO ADSP-2187L STATE OF OPERATION DURING EXECUTION OF IDLE INSTRUCTION. DEASSERTED PINS ARE DRIVEN TO EITHER V_{DD} OR GND.
3TYPICAL POWER DISSIPATION AT 3.3V V_{DD} AND 25°C EXCEPT WHERE SPECIFIED.
4I_{DD} MEASUREMENT TAKEN WITH ALL INSTRUCTIONS EXECUTING FROM INTERNAL MEMORY. 50% OF THE INSTRUCTIONS ARE MULTIFUNCTION (TYPES 1, 4, 5, 12, 13, 14), 30% ARE TYPE 2 AND TYPE 6, AND 20% ARE IDLE INSTRUCTIONS.

Figure 14. Power vs. Frequency

CAPACITIVE LOADING

Figures 15 and 16 show the capacitive loading characteristics of the ADSP-2187L.

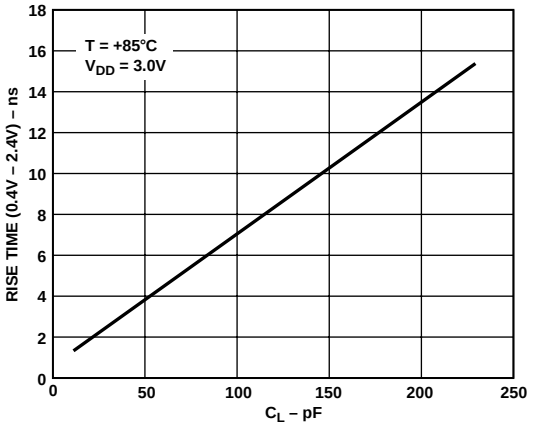


Figure 15. Typical Output Rise Time vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

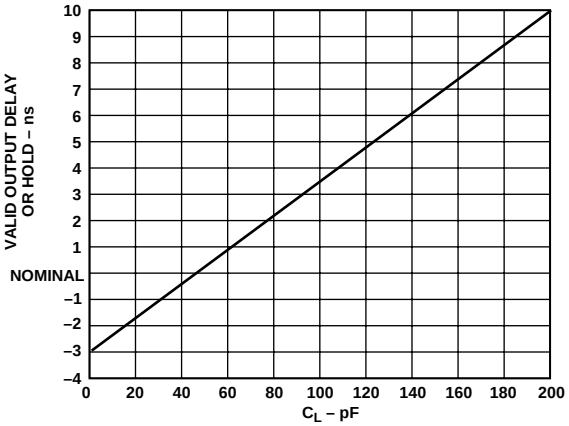


Figure 16. Typical Output Valid Delay or Hold vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

TEST CONDITIONS

Output Disable Time

Output pins are considered to be disabled when they have stopped driving and started a transition from the measured output high or low voltage to a high impedance state, see Figure 17. The output disable time (t_{DIS}) is the difference between $t_{MEASURED}$ and t_{DECAY}, see Figure 18. The time is the interval from when a reference signal reaches a high or low voltage level to when the output voltages have changed by 0.5 V from the measured output high or low voltage. The decay time, t_{DECAY}, is dependent on the capacitive load, C_L, and the current load, i_L, on the output pin. It can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \bullet 0.5V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. If multiple pins (such as the data bus) are disabled, the measurement value is that of the last pin to stop driving.

Figure 17. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high-impedance state to when they start driving. The output enable time (t_{ENA}) is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, see Figure 18. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

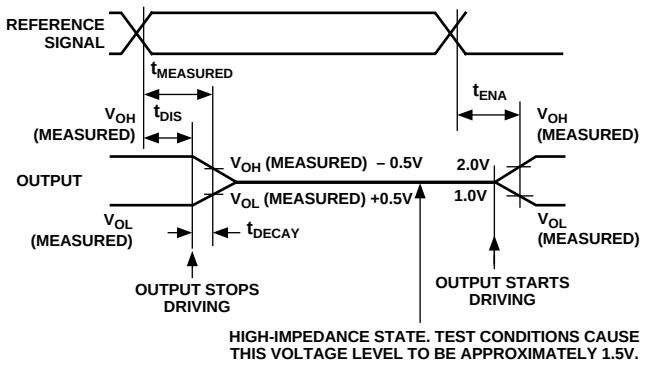


Figure 18. Output Enable/Disable

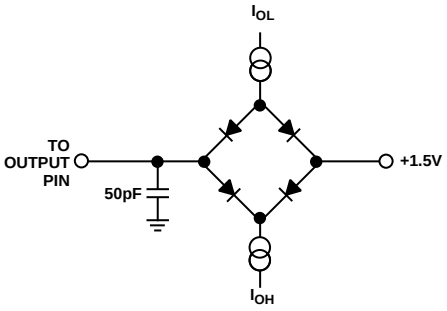


Figure 19. Equivalent Device Loading for AC Measurements (Including All Fixtures)

ENVIRONMENTAL CONDITIONS

Ambient Temperature Rating is shown below:

$T_{AMB} = T_{CASE} - (PD \times \theta_{CA})$
T_{CASE} = Case Temperature in °C
PD = Power Dissipation in W
θ_{CA} = Thermal Resistance (Case-to-Ambient)
θ_{JA} = Thermal Resistance (Junction-to-Ambient)
θ_{JC} = Thermal Resistance (Junction-to-Case)

Package	θ_{JA}	θ_{JC}	θ_{CA}
TQFP	50°C/W	2°C/W	48°C/W

TIMING PARAMETERS (See page 16, Frequency Depending for Timing Specifications, for timing definitions.)

Parameter		Min	Max	Unit
Clock Signals and Reset				
Timing Requirements:				
t_{CKI}	CLKIN External Clock Period	38	100	ns
t_{CKIL}	CLKIN Width Low	15		ns
t_{CKIH}	CLKIN Width High	15		ns
Switching Characteristics:				
t_{CKL}	CLKOUT Width Low	$0.5t_{CK} - 7$		ns
t_{CKH}	CLKOUT Width High	$0.5t_{CK} - 7$		ns
t_{CKOH}	CLKIN High to CLKOUT High	0	20	ns
Control Signals				
Timing Requirement:				
t_{RSP}	$\overline{\text{RESET}}$ Width Low	$5t_{CK}$[1]		ns
t_{MS}	Mode Setup before $\overline{\text{RESET}}$ High	2		ns
t_{MH}	Mode Hold after $\overline{\text{RESET}}$ High	5		ns

NOTE
[1]Applies after power-up sequence is complete. Internal phase lock loop requires no more than 2000 CLKIN cycles assuming stable CLKIN (not including crystal oscillator start-up time).

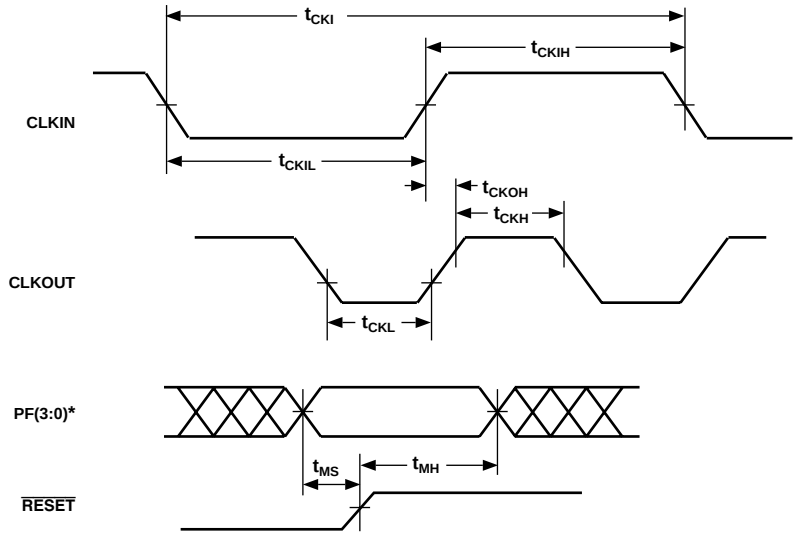


Figure 20. Clock Signals

Parameter		Min	Max	Unit
Interrupts and Flag				
Timing Requirements:				
t_{IFS}	$\overline{IRQx}$, FI, or PFx Setup before CLKOUT Low[1, 2, 3, 4]	$0.25t_{CK} + 15$		ns
t_{IFH}	$\overline{IRQx}$, FI, or PFx Hold after CLKOUT High[1, 2, 3, 4]	$0.25t_{CK}$		ns
Switching Characteristics:				
t_{FOH}	Flag Output Hold after CLKOUT Low[5]	$0.5t_{CK} - 7$		ns
t_{FOD}	Flag Output Delay from CLKOUT Low[5]		$0.15t_{CK} + 6$	ns

NOTES
[1]If $\overline{IRQx}$ and FI inputs meet t_{IFS} and t_{IFH} setup/hold requirements, they will be recognized during the current clock cycle; otherwise the signals will be recognized on the following cycle. (Refer to Interrupt Controller Operation in the Program Control chapter of the User's Manual for further information on interrupt servicing.)
[2]Edge-sensitive interrupts require pulsewidths greater than 10 ns; level-sensitive interrupts must be held low until serviced.
[3]$\overline{IRQx}$ = $\overline{IRQ0}$, $\overline{IRQ1}$, $\overline{IRQ2}$, $\overline{IRQL0}$, $\overline{IRQL1}$, $\overline{IRQE}$.
[4]PFx = PF0, PF1, PF2, PF3, PF4, PF5, PF6, PF7.
[5]Flag outputs = PFx, FL0, FL1, FL2, Flag_out4.

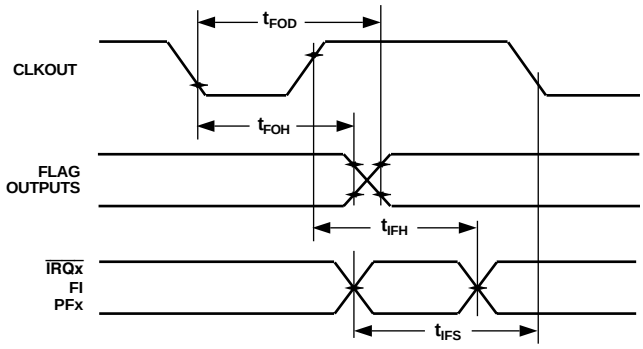


Figure 21. Interrupts and Flags

Parameter		Min	Max	Unit
Bus Request–Bus Grant				
Timing Requirements:				
t_{BH}	$\overline{BR}$ Hold after CLKOUT High[1]	$0.25t_{CK} + 2$		ns
t_{BS}	$\overline{BR}$ Setup before CLKOUT Low[1]	$0.25t_{CK} + 17$		ns
Switching Characteristics:				
t_{SD}	CLKOUT High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable		$0.25t_{CK} + 10$	ns
t_{SDB}	$\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BG}$ Low	0		ns
t_{SE}	$\overline{BG}$ High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable	0		ns
t_{SEC}	$\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable to CLKOUT High	$0.25t_{CK} - 4$		ns
t_{SDBH}	$\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BGH}$ Low[2]	0		ns
t_{SEH}	$\overline{BGH}$ High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable[2]	0		ns

NOTES
$\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.
[1]$\overline{BR}$ is an asynchronous signal. If $\overline{BR}$ meets the setup/hold requirements, it will be recognized during the current clock cycle; otherwise the signal will be recognized on the following cycle. Refer to the *ADSP-2100 Family User's Manual, Third Edition* for $\overline{BR}$/$\overline{BG}$ cycle relationships.
[2]$\overline{BGH}$ is asserted when the bus is granted and the processor requires control of the bus to continue.

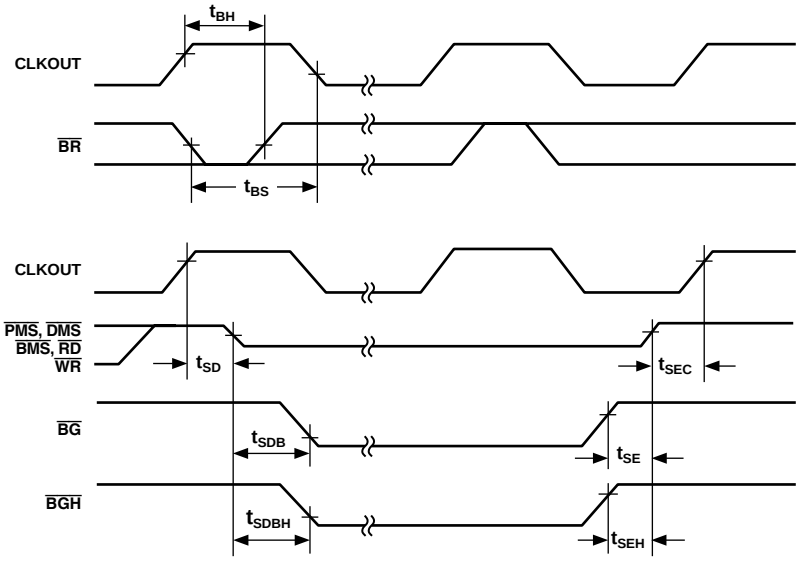


Figure 22. Bus Request–Bus Grant

Parameter		Min	Max	Unit
Memory Read				
Timing Requirements:				
t_{RDD}	$\overline{RD}$ Low to Data Valid		$0.5t_{CK} - 9 + w$	ns
t_{AA}	A0–A13, $\overline{xMS}$ to Data Valid		$0.75t_{CK} - 12.5 + w$	ns
t_{RDH}	Data Hold from $\overline{RD}$ High	0		ns
Switching Characteristics:				
t_{RP}	$\overline{RD}$ Pulsewidth	$0.5t_{CK} - 5 + w$		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	$0.25t_{CK} - 5$	$0.25t_{CK} + 7$	ns
t_{ASR}	A0–A13, $\overline{xMS}$ Setup before $\overline{RD}$ Low	$0.25t_{CK} - 6$		ns
t_{RDA}	A0–A13, $\overline{xMS}$ Hold after $\overline{RD}$ Deasserted	$0.25t_{CK} - 3$		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 5$		ns

w = wait states x t_{CK}
$\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

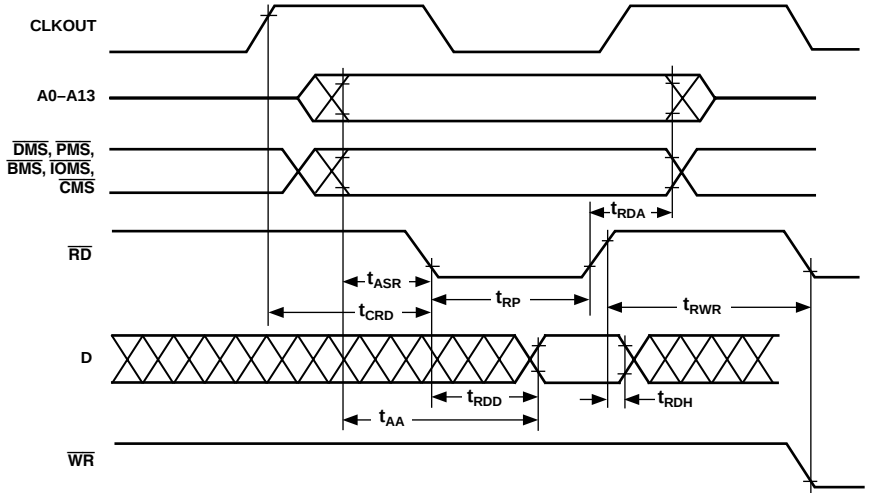


Figure 23. Memory Read

Parameter		Min	Max	Unit
Memory Write				
Switching Characteristics:				
t_{DW}	Data Setup before $\overline{WR}$ High	$0.5t_{CK} - 7 + w$		ns
t_{DH}	Data Hold after $\overline{WR}$ High	$0.25t_{CK} - 2$		ns
t_{WP}	$\overline{WR}$ Pulsewidth	$0.5t_{CK} - 5 + w$		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	0		ns
t_{ASW}	A0–A13, $\overline{xMS}$ Setup before $\overline{WR}$ Low	$0.25t_{CK} - 6$		ns
t_{DDR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	$0.25t_{CK} - 7$		ns
t_{CWR}	CLKOUT High to $\overline{WR}$ Low	$0.25t_{CK} - 5$	$0.25\ t_{CK} + 7$	ns
t_{AW}	A0–A13, $\overline{xMS}$, Setup before Deasserted	$0.75t_{CK} - 9 + w$		ns
t_{WRA}	A0–A13, $\overline{xMS}$ Hold after $\overline{WR}$ Deasserted	$0.25t_{CK} - 3$		ns
t_{WWR}	$\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 5$		ns

w = wait states x t_{CK}.
$\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

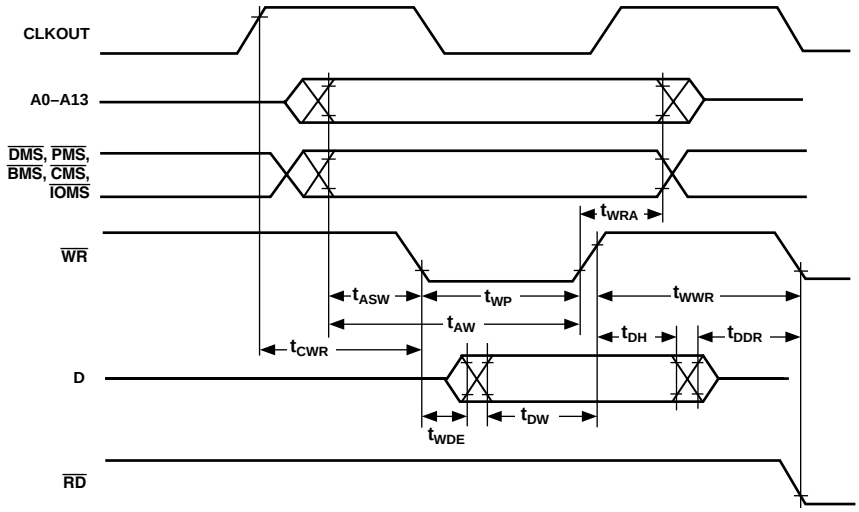


Figure 24. Memory Write

Parameter		Min	Max	Unit
Serial Ports				
Timing Requirements:				
t_{SCK}	SCLK Period	38		ns
t_{SCS}	DR/TFS/RFS Setup before SCLK Low	4		ns
t_{SCH}	DR/TFS/RFS Hold after SCLK Low	7		ns
t_{SCP}	$SCLK_{IN}$ Width	15		ns
Switching Characteristics:				
t_{CC}	CLKOUT High to $SCLK_{OUT}$	$0.25t_{CK}$	$0.25t_{CK} + 10$	ns
t_{SCDE}	SCLK High to DT Enable	0		ns
t_{SCDV}	SCLK High to DT Valid		15	ns
t_{RH}	TFS/RFS_{OUT} Hold after SCLK High	0		ns
t_{RD}	TFS/RFS_{OUT} Delay from SCLK High		15	ns
t_{SCDH}	DT Hold after SCLK High	0		ns
t_{TDE}	TFS (Alt) to DT Enable	0		ns
t_{TDV}	TFS (Alt) to DT Valid		14	ns
t_{SCDD}	SCLK High to DT Disable		15	ns
t_{RDV}	RFS (Multichannel, Frame Delay Zero) to DT Valid		15	ns

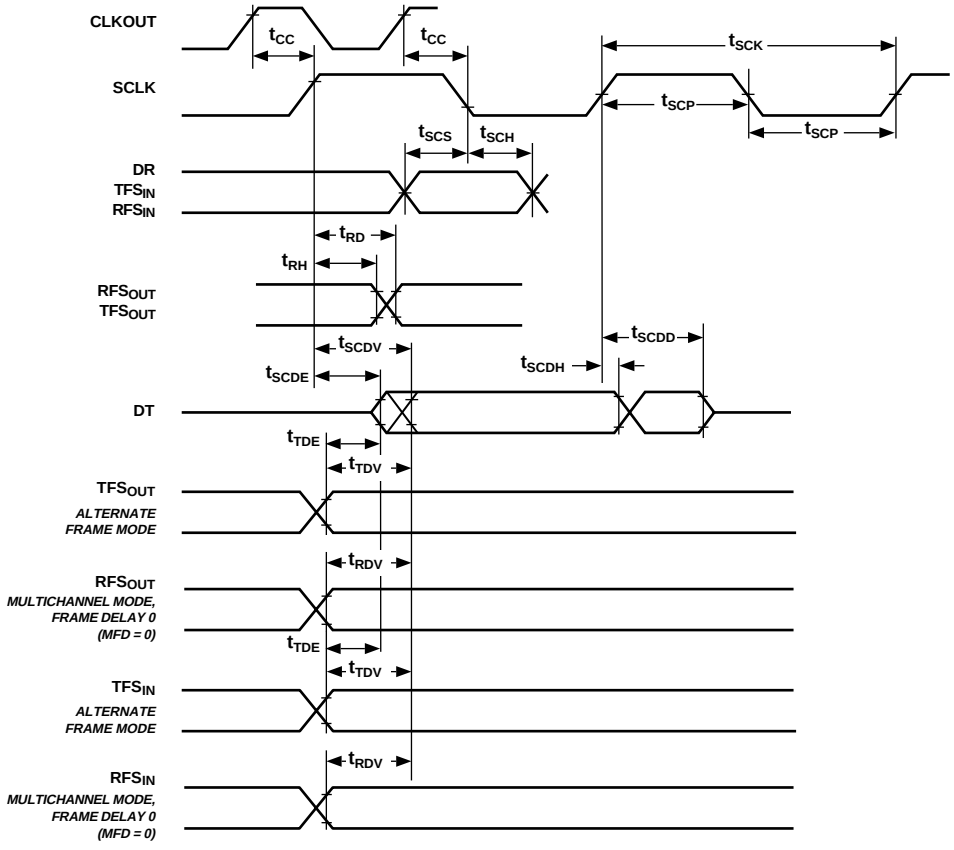


Figure 25. Serial Ports

Parameter		Min	Max	Unit
IDMA Address Latch				
Timing Requirements:				
t_{IALP}	Duration of Address Latch[1, 2]	10		ns
t_{IASU}	IAD15–0 Address Setup before Address Latch End[2]	5		ns
t_{IAH}	IAD15–0 Address Hold after Address Latch End[2]	2		ns
t_{IKA}	$\overline{IACK}$ Low before Start of Address Latch[2, 3]	0		ns
t_{IALS}	Start of Write or Read after Address Latch End[2, 3]	3		ns
t_{IALD}	Address Latch Start after Address Latch End[1, 2]	2		ns

NOTES
[1]Start of Address Latch = $\overline{IS}$ Low and IAL High.
[2]End of Address Latch = $\overline{IS}$ High or IAL Low.
[3]Start of Write or Read = $\overline{IS}$ Low and $\overline{IWR}$ Low or $\overline{IRD}$ Low.

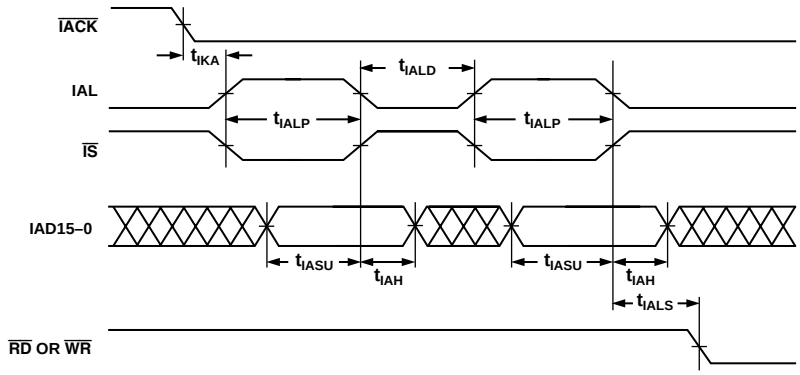


Figure 26. IDMA Address Latch

Parameter		Min	Max	Unit
IDMA Write, Short Write Cycle				
Timing Requirements:				
t_{IKW}	$\overline{IACK}$ Low before Start of Write[1]	0		ns
t_{IWP}	Duration of Write[1, 2]	15		ns
t_{IDSU}	IAD15–0 Data Setup before End of Write[2, 3, 4]	5		ns
t_{IDH}	IAD15–0 Data Hold after End of Write[2, 3, 4]	2		ns
Switching Characteristic:				
t_{IKHW}	Start of Write to $\overline{IACK}$ High	4	15	ns

NOTES
[1]Start of Write = $\overline{IS}$ Low and $\overline{IWR}$ Low.
[2]End of Write = $\overline{IS}$ High or $\overline{IWR}$ High.
[3]If Write Pulse ends before $\overline{IACK}$ Low, use specifications t_{IDSU}, t_{IDH}.
[4]If Write Pulse ends after $\overline{IACK}$ Low, use specifications t_{IKSU}, t_{IKH}.

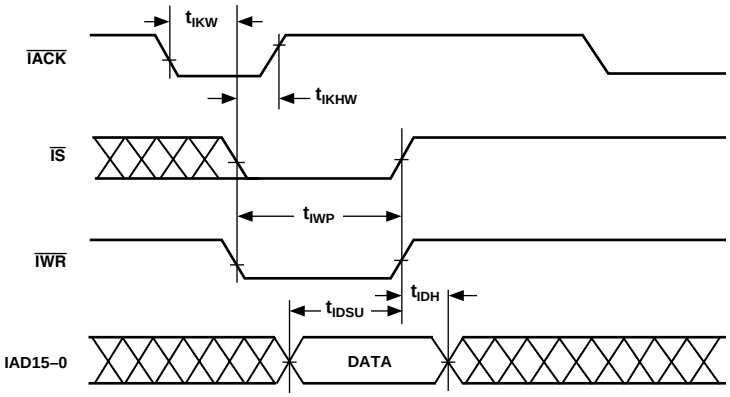


Figure 27. IDMA Write, Short Write Cycle

Parameter		Min	Max	Unit
IDMA Write, Long Write Cycle				
Timing Requirements:				
t_{IKW}	$\overline{IACK}$ Low before Start of Write[1]	0		ns
t_{IKSU}	IAD15–0 Data Setup before $\overline{IACK}$ Low[2, 3, 4]	$0.5t_{CK}$ + 10		ns
t_{IKH}	IAD15–0 Data Hold after $\overline{IACK}$ Low[2, 3, 4]	2		ns
Switching Characteristics:				
t_{IKLW}	Start of Write to $\overline{IACK}$ Low[4]	$1.5t_{CK}$		ns
t_{IKHW}	Start of Write to $\overline{IACK}$ High	4	15	ns

NOTES
[1]Start of Write = $\overline{IS}$ Low and $\overline{IWR}$ Low.
[2]If Write Pulse ends before $\overline{IACK}$ Low, use specifications t_{IDSU}, t_{IDH}.
[3]If Write Pulse ends after $\overline{IACK}$ Low, use specifications t_{IKSU}, t_{IKH}.
[4]This is the earliest time for $\overline{IACK}$ Low from Start of Write. For IDMA Write cycle relationships, please refer to the *ADSP-2100 Family User's Manual*, *Third Edition*.

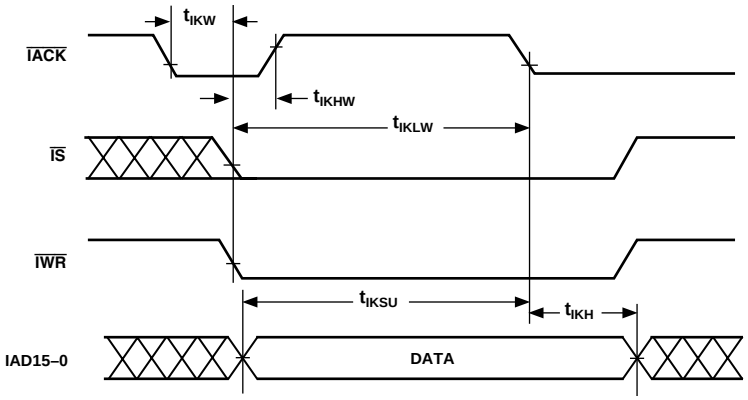


Figure 28. IDMA Write, Long Write Cycle

Parameter		Min	Max	Unit
IDMA Read, Long Read Cycle				
Timing Requirements:				
t_{IKR}	$\overline{IACK}$ Low before Start of Read[1]	0		ns
t_{IRK}	End of Read after $\overline{IACK}$ Low[2]	2		ns
Switching Characteristics:				
t_{IKHR}	$\overline{IACK}$ High after Start of Read[1]	4	15	ns
t_{IKDS}	IAD15–0 Data Setup before $\overline{IACK}$ Low	$0.5t_{CK} - 7$		ns
t_{IKDH}	IAD15–0 Data Hold after End of Read[2]	0		ns
t_{IKDD}	IAD15–0 Data Disabled after End of Read[2]		10	ns
t_{IRDE}	IAD15–0 Previous Data Enabled after Start of Read	0		ns
t_{IRDV}	IAD15–0 Previous Data Valid after Start of Read		10	ns
t_{IRDH1}	IAD15–0 Previous Data Hold after Start of Read (DM/PM1)[3]	$2t_{CK} - 5$		ns
t_{IRDH2}	IAD15–0 Previous Data Hold after Start of Read (PM2)[4]	$t_{CK} - 5$		ns

NOTES
[1]Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low.
[2]End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.
[3]DM read or first half of PM read.
[4]Second half of PM read.

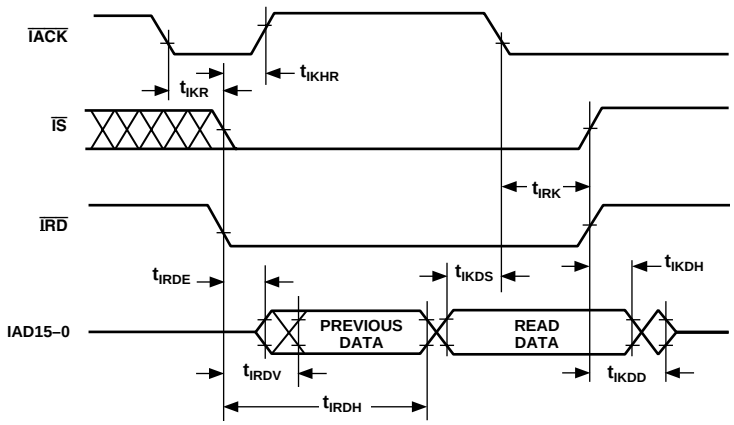


Figure 29. IDMA Read, Long Read Cycle

Parameter		Min	Max	Unit
IDMA Read, Short Read Cycle				
Timing Requirements:				
t_{IKR}	$\overline{IACK}$ Low before Start of Read[1]	0		ns
t_{IRP}	Duration of Read	15		ns
Switching Characteristics:				
t_{IKHR}	$\overline{IACK}$ High after Start of Read[1]	4	15	ns
t_{IKDH}	IAD15–0 Data Hold after End of Read[2]	0		ns
t_{IKDD}	IAD15–0 Data Disabled after End of Read[2]		10	ns
t_{IRDE}	IAD15–0 Previous Data Enabled after Start of Read	0		ns
t_{IRDV}	IAD15–0 Previous Data Valid after Start of Read		10	ns

NOTES
[1]Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low.
[2]End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.

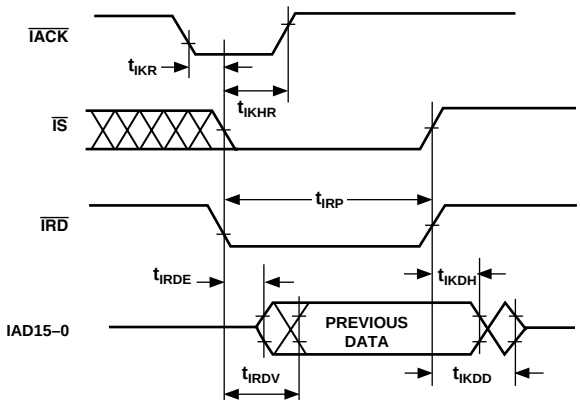
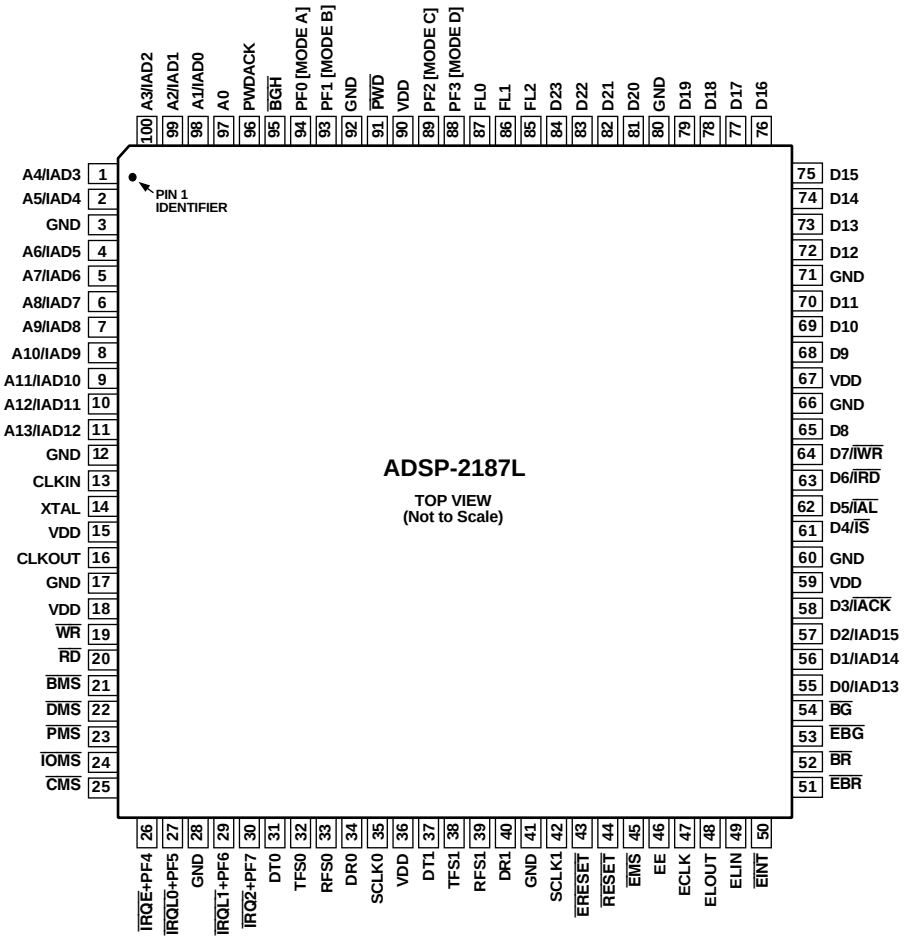


Figure 30. IDMA Read, Short Read Cycle

100-Lead TQFP Package Pinout



The ADSP-2187L package pinout is shown in the table below. Pin names in **bold** text replace the plain text named functions when Mode C = 1. A + sign separates two functions when either function can be active for either major I/O mode. Signals enclosed in brackets [ ] are state bits latched from the value of the pin at the deassertion of $\overline{\text{RESET}}$.

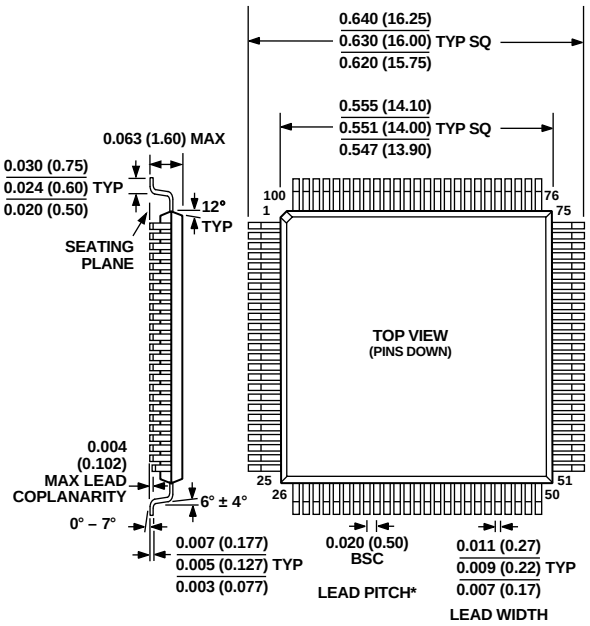
TQFP Pin Configurations

TQFP Number	Pin Name	TQFP Number	Pin Name	TQFP Number	Pin Name	TQFP Number	Pin Name
1	A4/**IAD3**	26	$\overline{\text{IRQE}}$ + PF4	51	$\overline{\text{EBR}}$	76	D16
2	A5/**IAD4**	27	$\overline{\text{IRQL0}}$ + PF5	52	$\overline{\text{BR}}$	77	D17
3	GND	28	GND	53	$\overline{\text{EBG}}$	78	D18
4	A6/**IAD5**	29	$\overline{\text{IRQL1}}$ + PF6	54	BG	79	D19
5	A7/**IAD6**	30	$\overline{\text{IRQ2}}$ + PF7	55	D0/**IAD13**	80	GND
6	A8/**IAD7**	31	DT0	56	D1/**IAD14**	81	D20
7	A9/**IAD8**	32	TFS0	57	D2/**IAD15**	82	D21
8	A10/**IAD9**	33	RFS0	58	D3/**$\overline{\text{IACK}}$**	83	D22
9	A11/**IAD10**	34	DR0	59	VDD	84	D23
10	A12/**IAD11**	35	SCLK0	60	GND	85	FL2
11	A13/**IAD12**	36	VDD	61	D4/**$\overline{\text{IS}}$**	86	FL1
12	GND	37	DT1	62	D5/**IAL**	87	FL0
13	CLKIN	38	TFS1	63	D6/**$\overline{\text{IRD}}$**	88	PF3 [Mode D]
14	XTAL	39	RFS1	64	D7/**$\overline{\text{IWR}}$**	89	PF2 [Mode C]
15	VDD	40	DR1	65	D8	90	VDD
16	CLKOUT	41	GND	66	GND	91	$\overline{\text{PWD}}$
17	GND	42	SCLK1	67	VDD	92	GND
18	VDD	43	$\overline{\text{ERESET}}$	68	D9	93	PF1 [Mode B]
19	$\overline{\text{WR}}$	44	$\overline{\text{RESET}}$	69	D10	94	PF0 [Mode A]
20	$\overline{\text{RD}}$	45	$\overline{\text{EMS}}$	70	D11	95	$\overline{\text{BGH}}$
21	$\overline{\text{BMS}}$	46	EE	71	GND	96	PWDACK
22	$\overline{\text{DMS}}$	47	ECLK	72	D12	97	A0
23	$\overline{\text{PMS}}$	48	ELOUT	73	D13	98	A1/**IAD0**
24	$\overline{\text{IOMS}}$	49	ELIN	74	D14	99	A2/**IAD1**
25	$\overline{\text{CMS}}$	50	$\overline{\text{EINT}}$	75	D15	100	A3/**IAD2**

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

100-Lead Metric Thin Plastic Quad Flatpack (TQFP) (ST-100)



*THE ACTUAL POSITION OF EACH LEAD IS WITHIN 0.0032 (0.08) FROM ITS IDEAL POSITION WHEN MEASURED IN THE LATERAL DIRECTION. CENTER FIGURE ARE TYPICAL UNLESS OTHERWISE NOTED.

C3174–3–7/98

ORDERING GUIDE

Part Number	Ambient Temperature Range	Instruction Rate (MHz)	Package Description	Package Option*
ADSP-2187LKST-160	0°C to +70°C	40	100-Lead TQFP	ST-100
ADSP-2187LBST-160	–40°C to +85°C	40	100-Lead TQFP	ST-100
ADSP-2187LKST-210	0°C to +70°C	52	100-Lead TQFP	ST-100
ADSP-2187LBST-210	–40°C to +85°C	52	100-Lead TQFP	ST-100

*ST = Plastic Thin Quad Flatpack (TQFP).

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