

Product Summary

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ max}$	$I_D \text{ max}$ $T_A = +25^\circ\text{C}$
30V	14mΩ @ $V_{GS} = 10\text{V}$	8.6A
	20mΩ @ $V_{GS} = 4.5\text{V}$	7.1A

Description

This MOSFET has been designed to minimize the on-state resistance ($R_{DS(ON)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

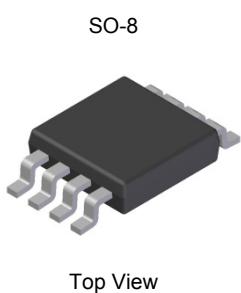
- Backlighting
- Power Management Functions
- DC-DC Converters

Features

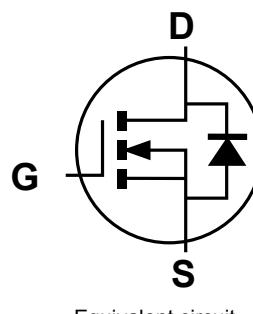
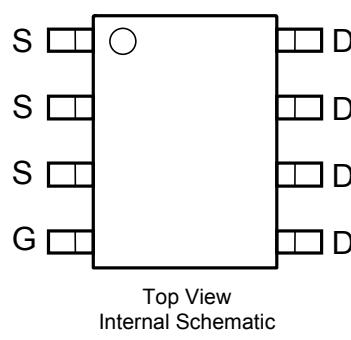
- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- Qualified to AEC-Q101 Standards for High Reliability

Mechanical Data

- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals Connections: See Diagram
- Terminals: Finish - Matte Tin annealed over Copper lead frame. Solderable per MIL-STD-202, Method 208 (E3)
- Weight: 0.072g (approximate)



Top View



Equivalent circuit

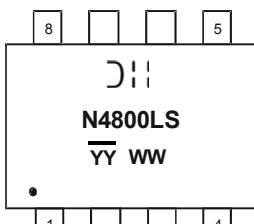
Ordering Information (Note 4)

Part Number	Case	Packaging
DMN4800LSS-13	SO-8	2500/Tape & Reel

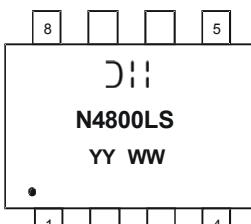
Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information



Chengdu A/T Site



Shanghai A/T Site

D!! = Manufacturer's Marking

N4800LS = Product Type Marking Code

YYWW = Date Code Marking

YY or YY = Year (ex: 13 = 2013)

WW = Week (01 - 53)

YY = Date Code Marking for SAT (Shanghai Assembly/ Test site)

YY = Date Code Marking for CAT (Chengdu Assembly/ Test site)

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V_{DSS}	30	V
Gate-Source Voltage			V_{GSS}	± 25	V
Continuous Drain Current (Note 6) $V_{GS} = 10\text{V}$	Steady State	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	8.6 6.3	A
	$t < 10\text{s}$	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	11.8 9.0	A
Maximum Body Diode Forward Current (Note 6)			I_S	2.4	A
Pulsed Drain Current (Note 7)			I_{DM}	50	A

Thermal Characteristics

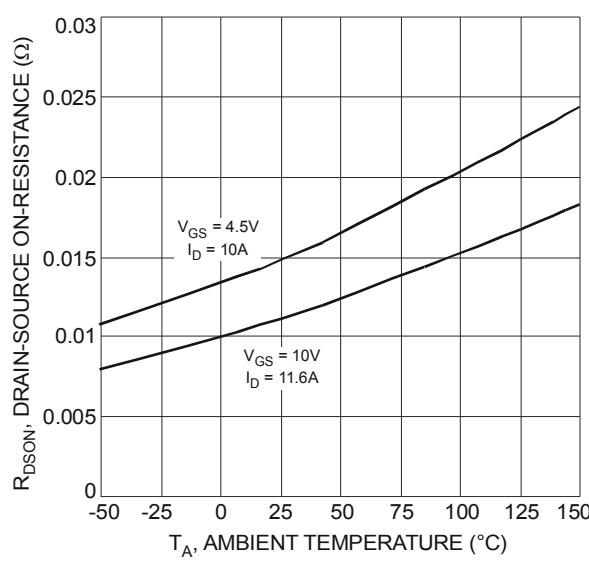
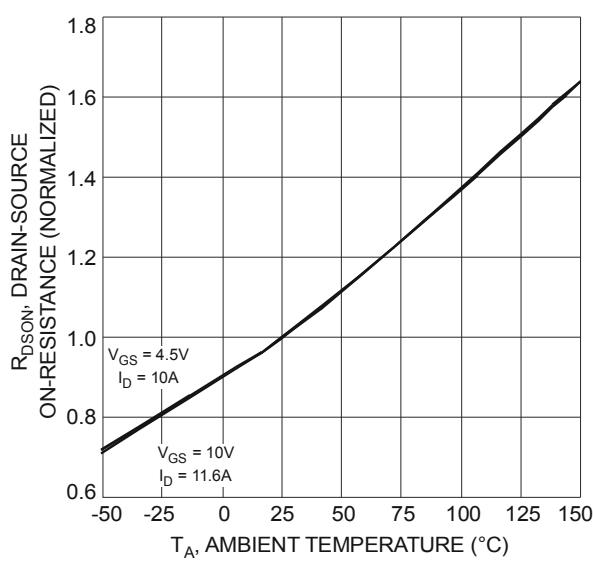
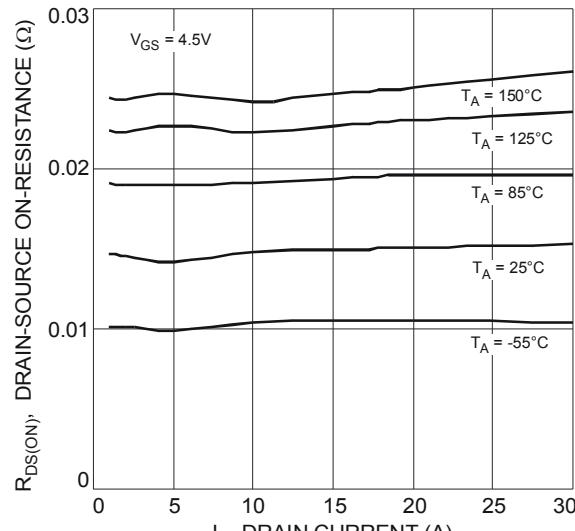
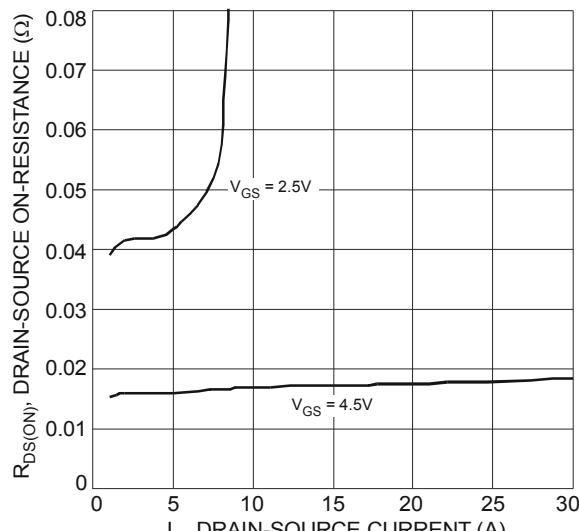
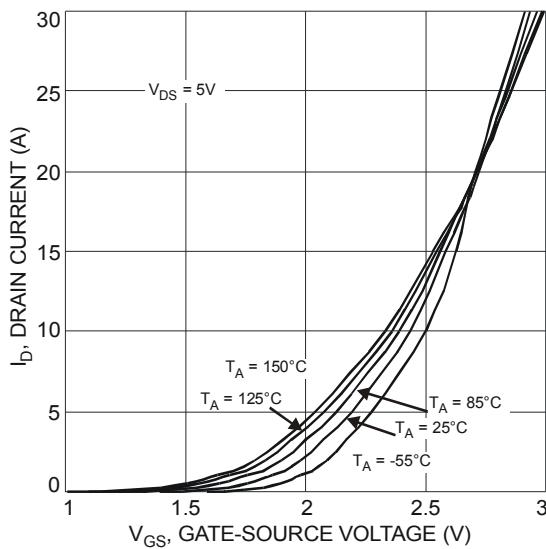
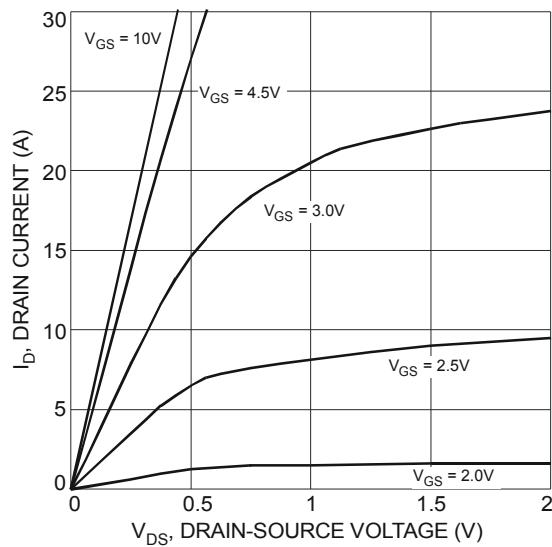
Characteristic		Symbol	Value	Units
Total Power Dissipation (Note 5)	$T_A = +25^\circ\text{C}$	P_D	1.46	W
	$T_A = +70^\circ\text{C}$		0.9	
Thermal Resistance, Junction to Ambient (Note 5)	Steady state	$R_{\theta JA}$	86	$^\circ\text{C}/\text{W}$
	$t < 10\text{s}$		46	
Total Power Dissipation (Note 6)	$T_A = +25^\circ\text{C}$	P_D	1.7	W
	$T_A = +70^\circ\text{C}$		1.0	
Thermal Resistance, Junction to Ambient (Note 6)	Steady state	$R_{\theta JA}$	75	$^\circ\text{C}/\text{W}$
	$t < 10\text{s}$		40	
Thermal Resistance, Junction to Case (Note 6)		$R_{\theta JC}$	15	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	30	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	μA	$V_{DS} = 30\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	± 100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(\text{th})}$	0.8	1.2	1.6	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(\text{ON})}$	—	11 14	14 20	$\text{m}\Omega$	$V_{GS} = 10\text{V}, I_D = 9\text{A}$ $V_{GS} = 4.5\text{V}, I_D = 7\text{A}$
Forward Transconductance	g_{fs}	—	8	—	S	$V_{DS} = 10\text{V}, I_D = 9\text{A}$
Diode Forward Voltage (Note 8)	V_{SD}	—	0.72	0.94	V	$V_{GS} = 0\text{V}, I_S = 1\text{A}$
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{iss}	—	798	—	pF	$V_{DS} = 10\text{V}, V_{GS} = 0\text{V}$ $f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	—	128	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	122	—	pF	
Gate Resistance	R_G	—	1.37	—	Ω	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Total Gate Charge	Q_g	—	8.7	—	nC	$V_{GS} = 5\text{V}, V_{DS} = 15\text{V}, I_D = 9\text{A}$
Gate-Source Charge	Q_{gs}	—	1.7	—		
Gate-Drain Charge	Q_{gd}	—	2.4	—		
Turn-On Delay Time	$t_{d(\text{on})}$	—	5.03	—	ns	$V_{DD} = 15\text{V}, V_{GEN} = 10\text{V}, R_L = 15\Omega, R_G = 6.0\Omega, I_D = 1\text{A}$
Rise Time	t_r	—	4.50	—		
Turn-Off Delay Time	$t_{d(\text{off})}$	—	26.33	—		
Fall Time	t_f	—	8.55	—		

Notes:

5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper pad layout
7. Repetitive rating, pulse width limited by junction temperature.
8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to product testing.



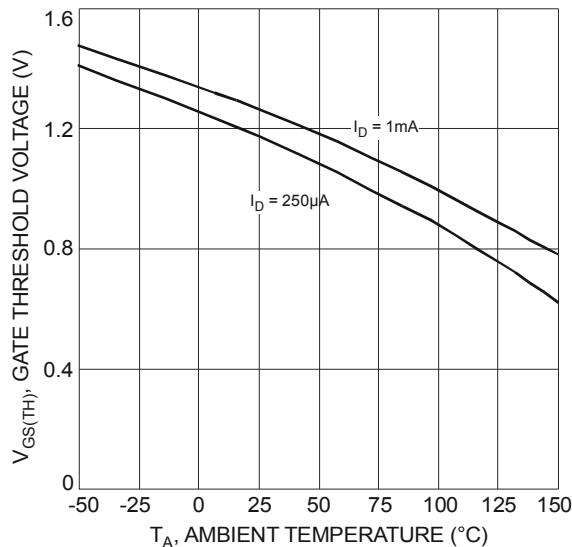


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

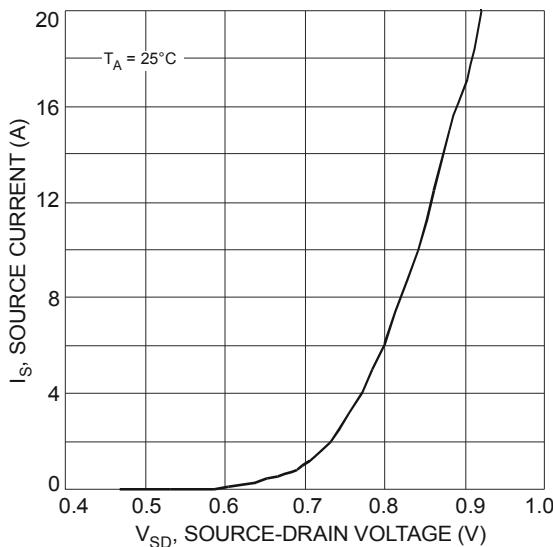


Fig. 8 Diode Forward Voltage vs. Current

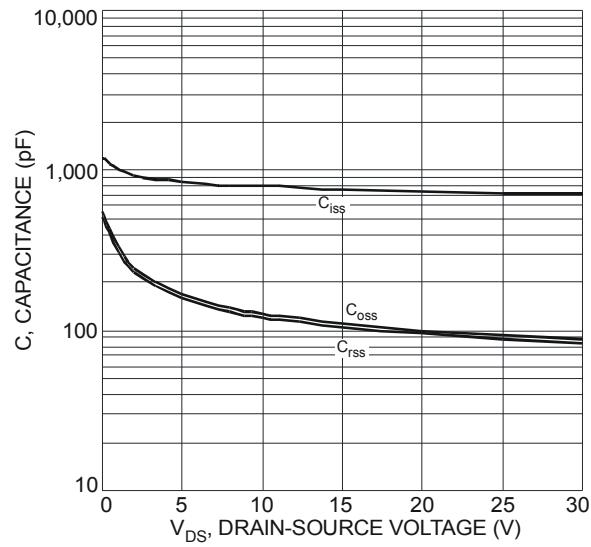


Fig. 9 Typical Total Capacitance

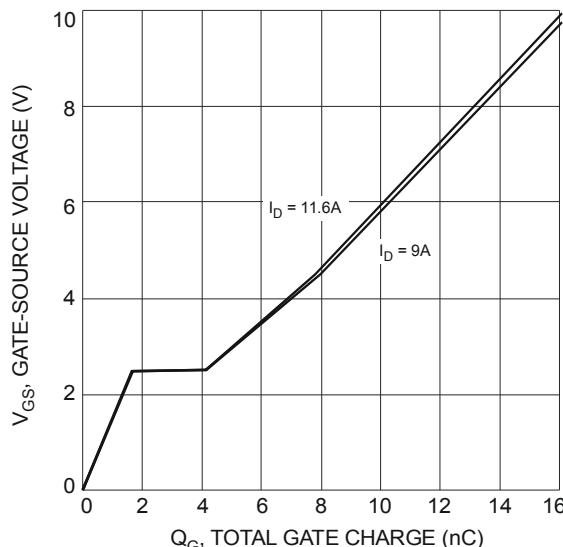


Fig. 10 Total Gate Charge

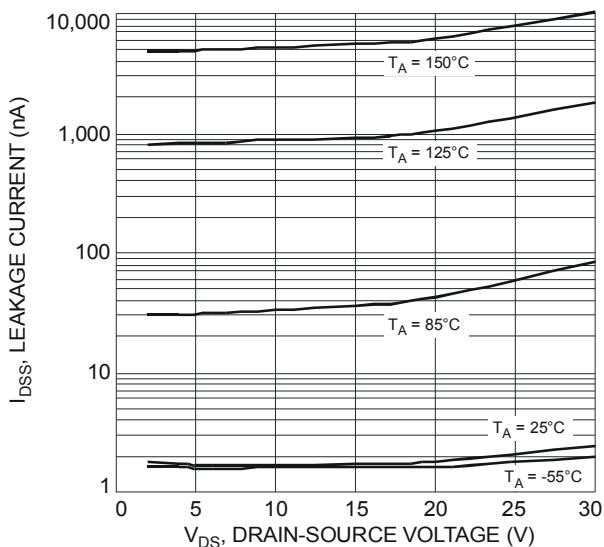


Fig. 11 Typical Leakage Current vs. Drain-Source Voltage

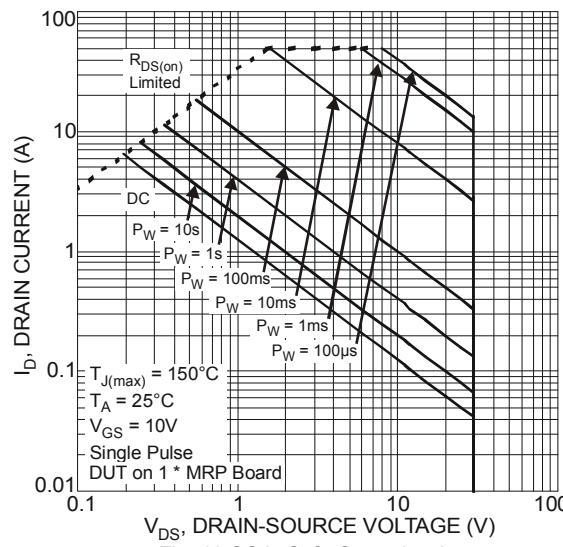


Fig. 12 SOA, Safe Operation Area

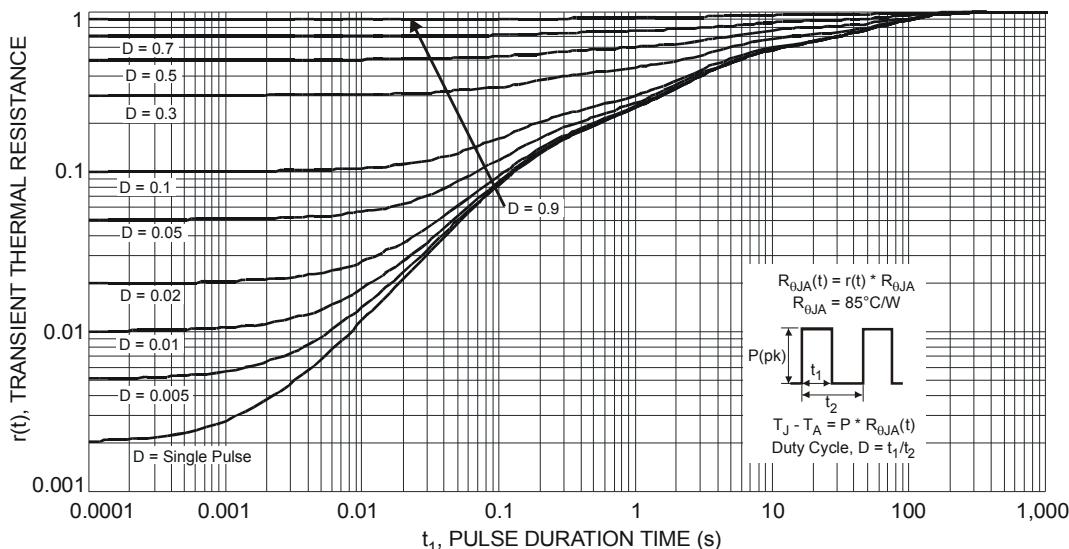
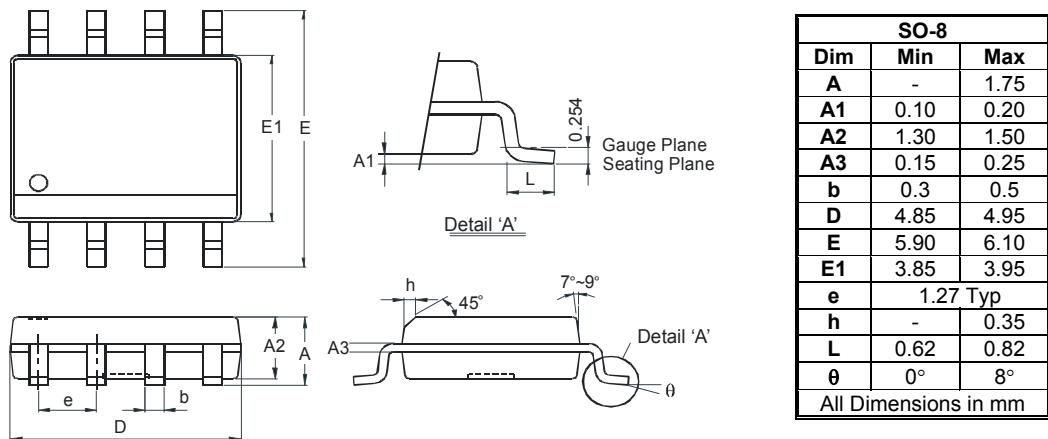
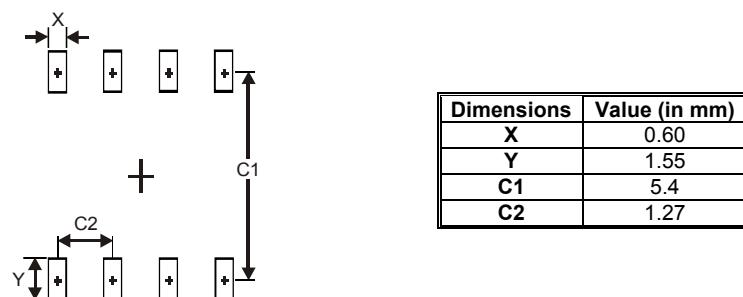


Fig. 13 Transient Thermal Response

Package Outline Dimensions



Suggested Pad Layout



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