

# EH3600TTS-5.000M

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## REGULATORY COMPLIANCE (Data Sheet downloaded on Nov 11, 2018)


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## ITEM DESCRIPTION

Quartz Crystal Clock Oscillators XO (SPXO) LVC MOS (CMOS) 3.3Vdc 4 Pad 3.2mm x 5.0mm Ceramic Surface Mount (SMD) 5.000MHz  $\pm 100$ ppm 0°C to +70°C

## ELECTRICAL SPECIFICATIONS

|                                       |                                                                                                                                                                                                                                         |
|---------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Nominal Frequency                     | 5.000MHz                                                                                                                                                                                                                                |
| Frequency Tolerance/Stability         | $\pm 100$ ppm Maximum (Inclusive of all conditions: Calibration Tolerance at 25°C, Frequency Stability over the Operating Temperature Range, Supply Voltage Change, Output Load Change, First Year Aging at 25°C, Shock, and Vibration) |
| Aging at 25°C                         | $\pm 5$ ppm/year Maximum                                                                                                                                                                                                                |
| Operating Temperature Range           | 0°C to +70°C                                                                                                                                                                                                                            |
| Supply Voltage                        | 3.3Vdc $\pm 10\%$                                                                                                                                                                                                                       |
| Input Current                         | 35mA Maximum (No Load)                                                                                                                                                                                                                  |
| Output Voltage Logic High (Voh)       | 2.7Vdc Minimum (IOH = -8mA)                                                                                                                                                                                                             |
| Output Voltage Logic Low (Vol)        | 0.5Vdc Maximum (IOL = +8mA)                                                                                                                                                                                                             |
| Rise/Fall Time                        | 6nSec Maximum (Measured at 20% to 80% of waveform)                                                                                                                                                                                      |
| Duty Cycle                            | 50 $\pm 5$ (%) (Measured at 50% of waveform)                                                                                                                                                                                            |
| Load Drive Capability                 | 30pF Maximum                                                                                                                                                                                                                            |
| Output Logic Type                     | CMOS                                                                                                                                                                                                                                    |
| Pin 1 Connection                      | Tri-State (High Impedance)                                                                                                                                                                                                              |
| Tri-State Input Voltage (Vih and Vil) | 70% of Vdd Minimum to enable output, 20% of Vdd Maximum to disable output, No Connect to enable output.                                                                                                                                 |
| Absolute Clock Jitter                 | $\pm 250$ pSec Maximum, $\pm 100$ pSec Typical                                                                                                                                                                                          |
| One Sigma Clock Period Jitter         | $\pm 50$ pSec Maximum, $\pm 40$ pSec Typical                                                                                                                                                                                            |
| Start Up Time                         | 10mSec Maximum                                                                                                                                                                                                                          |
| Storage Temperature Range             | -55°C to +125°C                                                                                                                                                                                                                         |

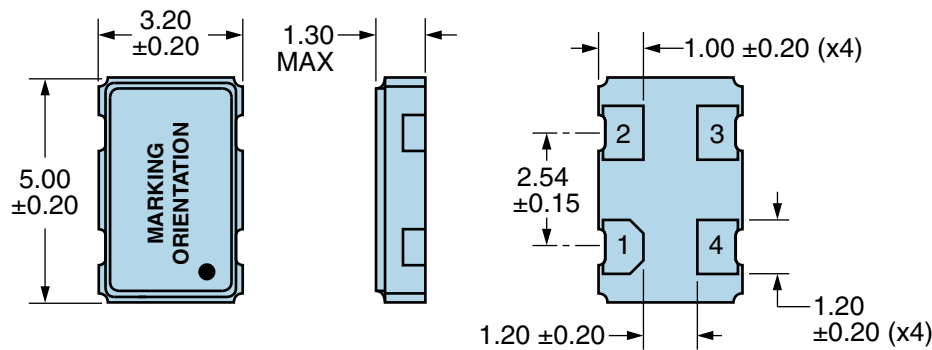
## ENVIRONMENTAL & MECHANICAL SPECIFICATIONS

|                              |                                       |
|------------------------------|---------------------------------------|
| Fine Leak Test               | MIL-STD-883, Method 1014, Condition A |
| Gross Leak Test              | MIL-STD-883, Method 1014, Condition C |
| Mechanical Shock             | MIL-STD-202, Method 213, Condition C  |
| Resistance to Soldering Heat | MIL-STD-202, Method 210               |
| Resistance to Solvents       | MIL-STD-202, Method 215               |
| Solderability                | MIL-STD-883, Method 2003              |
| Temperature Cycling          | MIL-STD-883, Method 1010              |
| Vibration                    | MIL-STD-883, Method 2007, Condition A |

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MECHANICAL DIMENSIONS (all dimensions in millimeters)

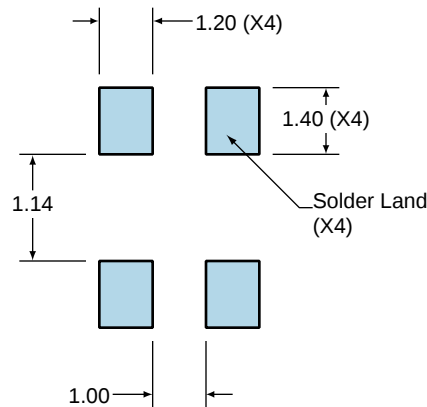


| PIN | CONNECTION         |
|-----|--------------------|
| 1   | Tri-State          |
| 2   | Ground/Case Ground |
| 3   | Output             |
| 4   | Supply Voltage     |

| LINE | MARKING                                                      |
|------|--------------------------------------------------------------|
| 1    | <b>E5.0000</b><br>E=Ecliptek Designator                      |
| 2    | <b>XXXXXX</b><br>XXXXXX=Ecliptek<br>Manufacturing Identifier |

Suggested Solder Pad Layout

All Dimensions in Millimeters



All Tolerances are ±0.1

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OUTPUT WAVEFORM & TIMING DIAGRAM



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## Test Circuit for CMOS Output



Note 1: An external 0.1µF low frequency tantalum bypass capacitor in parallel with a 0.01µF high frequency ceramic bypass capacitor close to the package ground and  $V_{DD}$  pin is required.

Note 2: A low capacitance (<12pF), 10X attenuation factor, high impedance (>10Mohms), and high bandwidth (>300MHz) passive probe is recommended.

Note 3: Capacitance value  $C_L$  includes sum of all probe and fixture capacitance.