

Dual 4-bit binary ripple counter

74LV393

FEATURES

- Optimized for Low Voltage applications: 1.0 to 3.6V
- Accepts TTL input levels between $V_{CC} = 2.7V$ and $V_{CC} = 3.6V$
- Typical V_{OLP} (output ground bounce) $< 0.8V$ @ $V_{CC} = 3.3V$, $T_{amb} = 25^{\circ}C$
- Typical V_{OHV} (output V_{OH} undershoot) $> 2V$ @ $V_{CC} = 3.3V$, $T_{amb} = 25^{\circ}C$
- Two 4-bit binary counters with individual clocks
- Divide-by any binary module up to 28 in one package
- Output capability: standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV393 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT393.

The 74LV393 is a dual 4-bit binary ripple counter with separate clocks ($1\overline{CP}$, $2\overline{CP}$) and master reset ($1MR$, $2MR$) inputs to each counter.

The operation of each half of the "393" is the same as the "93" except no external clock connections are required. The counters are triggered by a HIGH-to-LOW transition of the clock inputs. The counter outputs are internally connected to provide clock inputs to succeeding stages. The outputs of the ripple counter do not change synchronously and should not be used for high-speed address decoding.

The master resets are active-HIGH asynchronous inputs to each 4-bit counter identified by the "1" and "2" in the pin description.

A HIGH level on the nMR input overrides the clock and sets the outputs LOW.

QUICK REFERENCE DATA

$GND = 0V$; $T_{amb} = 25^{\circ}C$; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay $n\overline{CP}$ to nQ_0 nQ to nQ_{n+1} nMR to nQ_n	$C_L = 15pF$ $V_{CC} = 3.3V$	12 4 11	ns
f_{max}	Maximum clock frequency		99	MHz
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per flip-flop	$V_I = GND$ to V_{CC}^1	23	pF

NOTE:

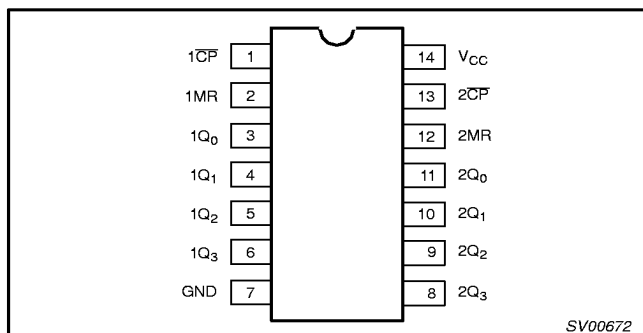
1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; C_L = output load capacity in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
14-Pin Plastic DIL	$-40^{\circ}C$ to $+125^{\circ}C$	74LV393 N	74LV393 N	SOT27-1
14-Pin Plastic SO	$-40^{\circ}C$ to $+125^{\circ}C$	74LV393 D	74LV393 D	SOT108-1
14-Pin Plastic SSOP Type II	$-40^{\circ}C$ to $+125^{\circ}C$	74LV393 DB	74LV393 DB	SOT337-1
14-Pin Plastic TSSOP Type I	$-40^{\circ}C$ to $+125^{\circ}C$	74LV393 PW	74LV393PW DH	SOT402-1

PIN CONFIGURATION



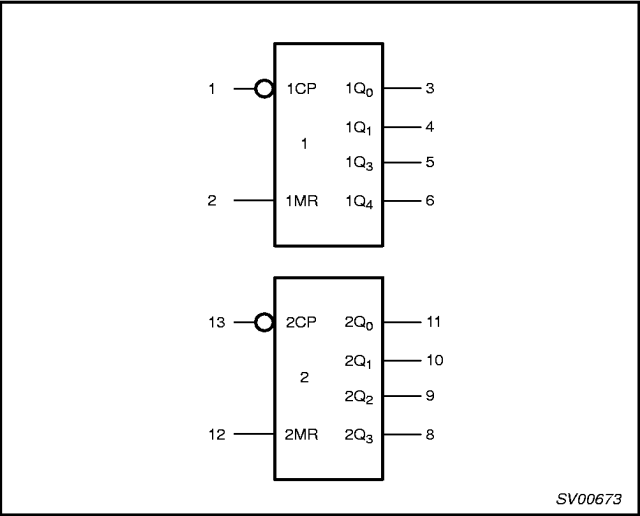
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 13	$1\overline{CP}$, $2\overline{CP}$	Clock inputs (HIGH-to-LOW, edge-triggered)
2, 12	$1MR$, $2MR$	Asynchronous master reset inputs (active HIGH)
3, 4, 5, 6 11, 10, 9, 8	$1Q_0$ to $1Q_3$ $2Q_0$ to $2Q_3$	Flip-flop outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

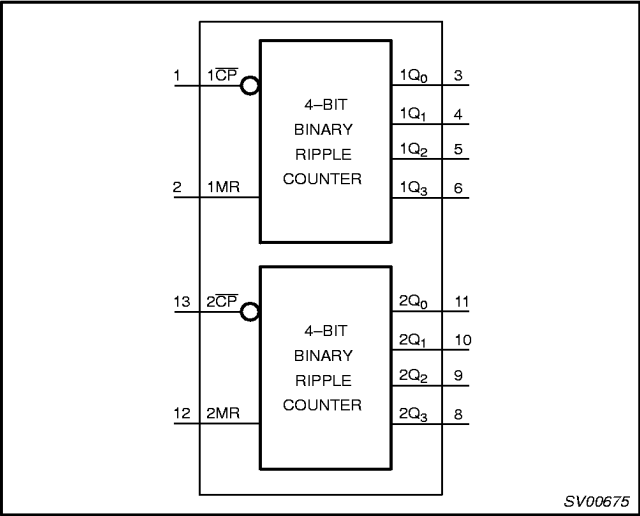
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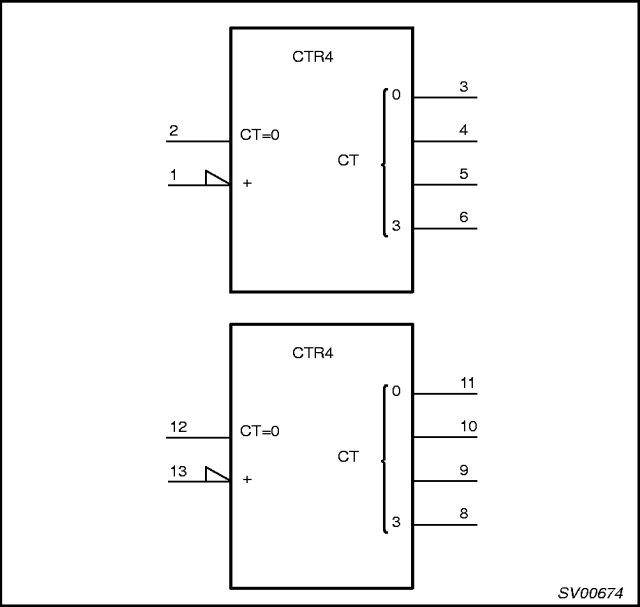
LOGIC SYMBOL



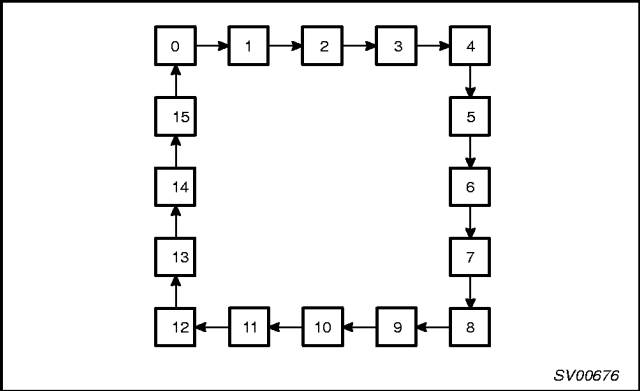
FUNCTIONAL DIAGRAM



LOGIC SYMBOL (IEEE/IEC)



STATE DIAGRAM



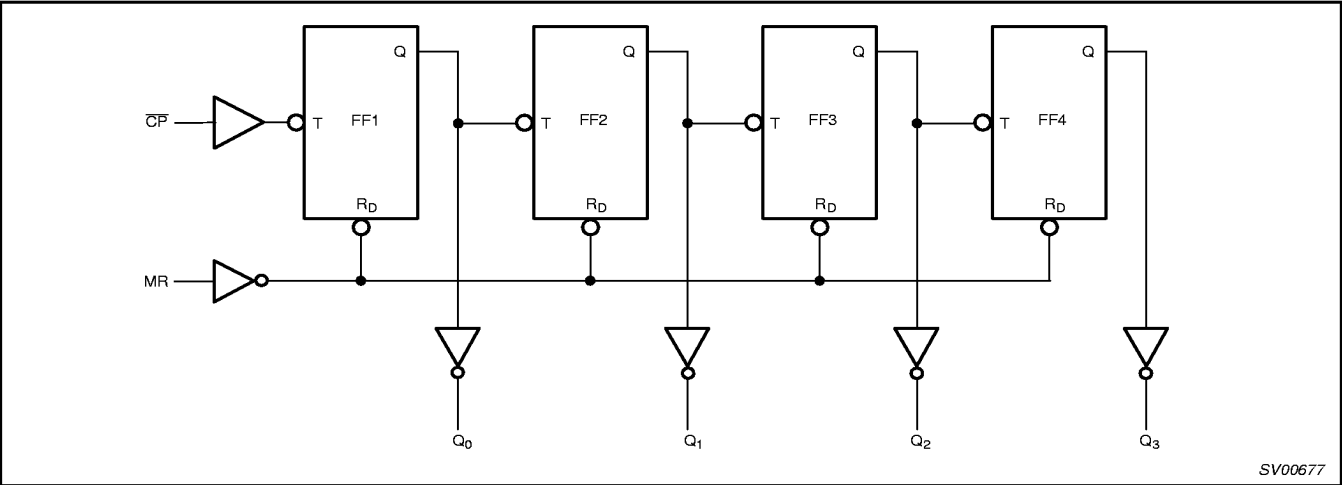
COUNT SEQUENCE FOR 1 COUNTER

COUNT	OUTPUTS			
	Q ₀	Q ₁	Q ₂	Q ₃
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

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LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	3.6	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics per device	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times except for Schmitt-trigger inputs	$V_{CC} = 1.0V$ to $2.0V$ $V_{CC} = 2.0V$ to $2.7V$ $V_{CC} = 2.7V$ to $3.6V$	– – –	– – –	500 200 100	ns/V

NOTES:
1. The LV is guaranteed to function down to $V_{CC} = 1.0V$ (input levels GND or V_{CC}); DC characteristics are guaranteed from $V_{CC} = 1.2V$ to $V_{CC} = 3.6V$.

ABSOLUTE MAXIMUM RATINGS^{1, 2}

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs – bus driver outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25 35	mA
$\pm I_{GND}, \pm I_{CC}$	DC V_{CC} or GND current for types with – standard outputs – bus driver outputs		50 70	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC CHARACTERISTICS FOR THE LV FAMILY

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP ¹	MAX	MIN	MAX	
V _{IH}	HIGH level Input voltage	V _{CC} = 1.2V	0.9			0.9		V
		V _{CC} = 2.0V	1.4			1.4		
		V _{CC} = 2.7 to 3.6V	2.0			2.0		
V _{IL}	LOW level Input voltage	V _{CC} = 1.2V			0.3		0.3	V
		V _{CC} = 2.0V			0.6		0.6	
		V _{CC} = 2.7 to 3.6V			0.8		0.8	
V _{OH}	HIGH level output voltage; all outputs	V _{CC} = 1.2V; V _I = V _{IH} or V _{IL} ; -I _O = 100μA		1.2				V
		V _{CC} = 2.0V; V _I = V _{IH} or V _{IL} ; -I _O = 100μA	1.8	2.0		1.8		
		V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; -I _O = 100μA	2.5	2.7		2.5		
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; -I _O = 100μA	2.8	3.0		2.8		
V _{OH}	HIGH level output voltage; STANDARD outputs	V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; -I _O = 6mA	2.40	2.82		2.20		V
V _{OH}	HIGH level output voltage; BUS driver outputs	V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; -I _O = 8mA	2.40	2.82		2.20		V
V _{OL}	LOW level output voltage; all outputs	V _{CC} = 1.2V; V _I = V _{IH} or V _{IL} ; I _O = 100μA		0				V
		V _{CC} = 2.0V; V _I = V _{IH} or V _{IL} ; I _O = 100μA		0	0.2		0.2	
		V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = 100μA		0	0.2		0.2	
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 100μA		0	0.2		0.2	
V _{OL}	LOW level output voltage; STANDARD outputs	V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 6mA		0.25	0.40		0.50	V
V _{OL}	LOW level output voltage; BUS driver outputs	V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 8mA		0.20	0.40		0.50	V
I _I	Input leakage current	V _{CC} = 3.6V; V _I = V _{CC} or GND			1.0		1.0	μA
I _{OZ}	3-State output OFF-state current	V _{CC} = 3.6V; V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND			5		10	μA
I _{CC}	Quiescent supply current; SSI	V _{CC} = 3.6V; V _I = V _{CC} or GND; I _O = 0			20.0		40	μA
	Quiescent supply current; flip-flops	V _{CC} = 3.6V; V _I = V _{CC} or GND; I _O = 0			20.0		80	
I _{CC}	Quiescent supply current; MSI	V _{CC} = 3.6V; V _I = V _{CC} or GND; I _O = 0			20.0		160	μA
	Quiescent supply current; LSI	V _{CC} = 3.6V; V _I = V _{CC} or GND; I _O = 0			500		1000	
ΔI _{CC}	Additional quiescent supply current per input	V _{CC} = 2.7V to 3.6V; V _I = V _{CC} - 0.6V			500		850	μA

NOTE:1. All typical values are measured at $T_{amb} = 25^\circ C$.

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AC CHARACTERISTICSGND = 0V; $t_r = t_f \leq 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 1\text{k}\Omega$

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				−40 to +85 °C			−40 to +125 °C		
				V _{CC} (V)	MIN	TYP ¹	MAX	MIN	
t _{PHL} /t _{PLH}	Propagation delay nCP to nQ ₀	Figure 1	1.2	—	75	—	—	—	ns
			2.0	—	26	49	—	60	
			2.7	—	19	36	—	44	
			3.0 to 3.6	—	14 ²	29	—	35	
t _{PHL} /t _{PLH}	Propagation delay nQ _n to nQ _{n+1}	Figure 1	1.2	—	25	—	—	—	ns
			2.0	—	9	17	—	20	
			2.7	—	6	13	—	15	
			3.0 to 3.6	—	5 ²	10	—	12	
t _{PHL}	Propagation delay nMR to nQ _n	Figure 2	1.2	—	70	—	—	—	ns
			2.0	—	24	44	—	54	
			2.7	—	18	33	—	40	
			3.0 to 3.6	—	13 ²	26	—	32	
t _W	Clock pulse width HIGH or LOW	Figure 1	2.0	34	10	—	41	—	ns
			2.7	25	8	—	30	—	
			3.0 to 3.6	20	6 ²	—	24	—	
t _W	Master reset pulse width; HIGH	Figure 2	2.0	34	12	—	41	—	ns
			2.7	25	9	—	30	—	
			3.0 to 3.6	20	7 ²	—	24	—	
t _{rem}	Removal time nMR to nCP	Figure 2	1.2	—	5	—	—	—	ns
			2.0	5	2	—	5	—	
			2.7	5	2	—	5	—	
			3.0 to 3.6	5	1 ²	—	5	—	
f _{max}	Maximum clock pulse frequency	Figure 1	2.0	14	53	—	12	—	MHz
			2.7	19	72	—	16	—	
			3.0 to 3.6	24	90 ²	—	20	—	

NOTES:

1. All typical values are measured at $T_{amb} = 25^\circ\text{C}$
2. Typical values are measured at $V_{CC} = 3.3\text{V}$

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AC WAVEFORMS

$V_M = 1.5V$ at $V_{CC} \geq 2.7V$
 $V_M = 0.5 * V_{CC}$ at $V_{CC} < 2.7V$
 V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

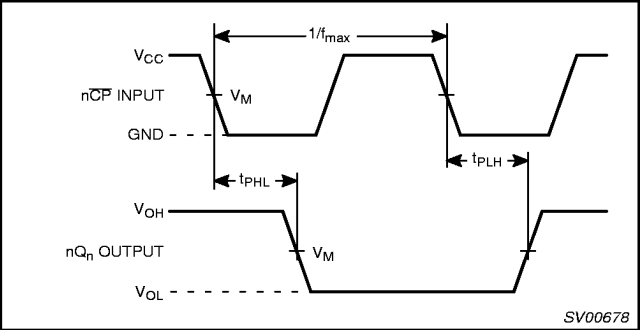


Figure 1. Clock (nCP) to output (1Qn, 2Qn) propagation delays, the clock pulse width, and the maximum clock frequency

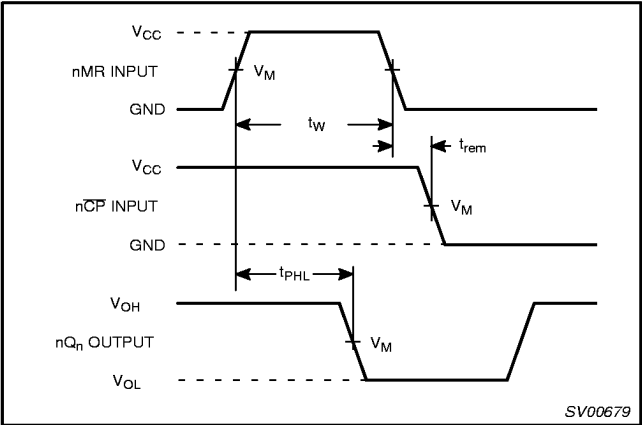


Figure 2. Master reset (nMR) pulse width, the master reset to output (Qn) propagation delays, and the master reset to clock (nCP) removal time

TEST CIRCUIT

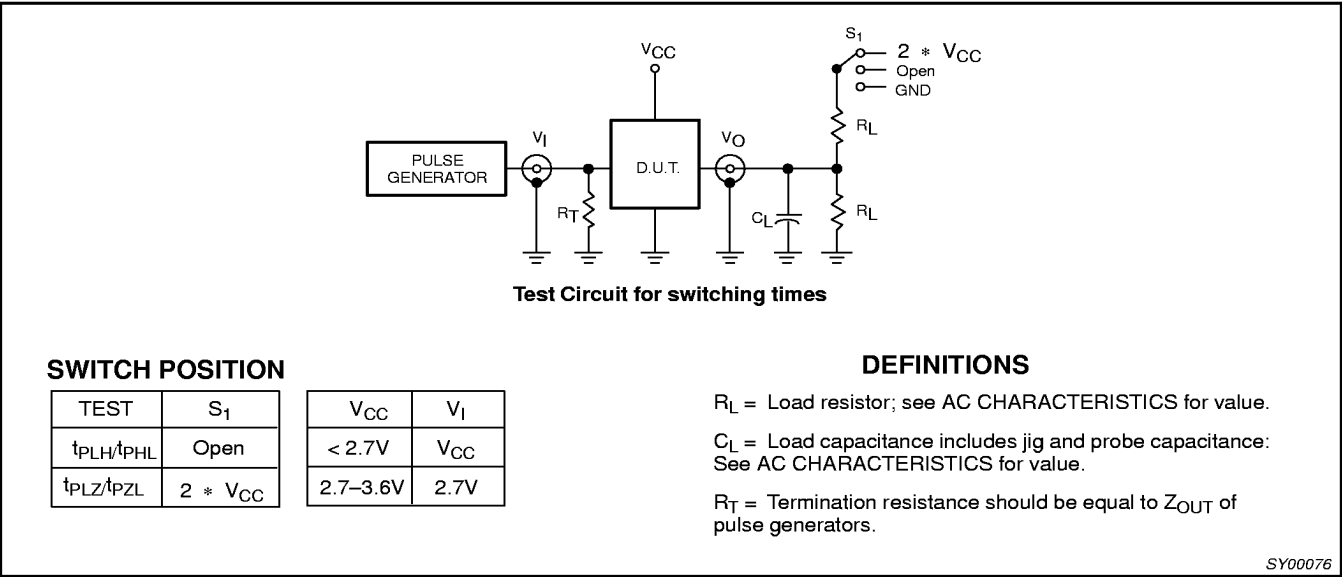


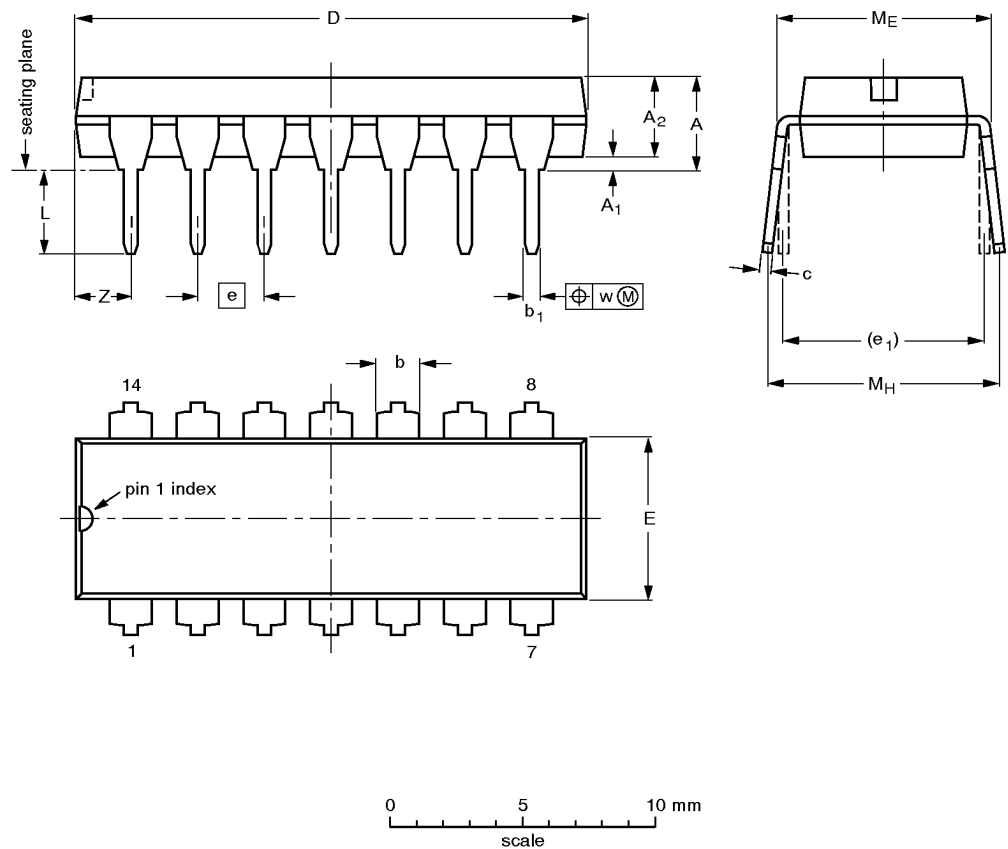
Figure 3. Load circuitry for switching times

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DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

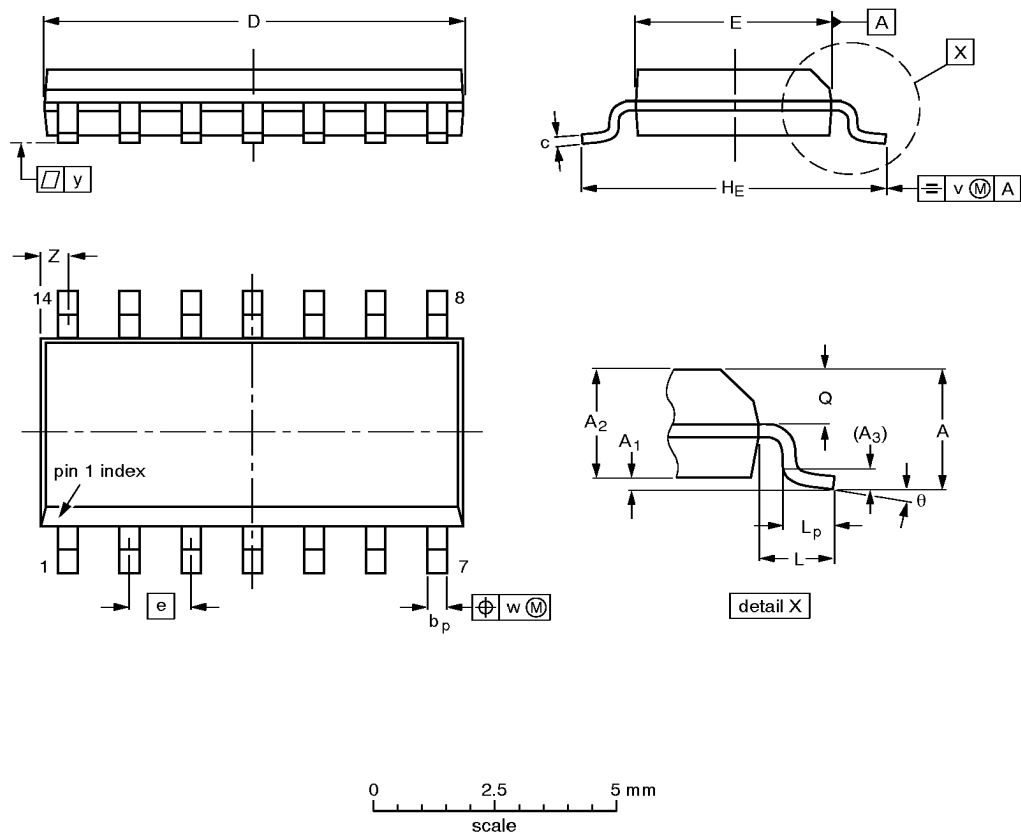
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT27-1	050G04	MO-001AA				92-11-17 95-03-11

Dual 4-bit binary ripple counter

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SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A _{max.}	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.35 0.34	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

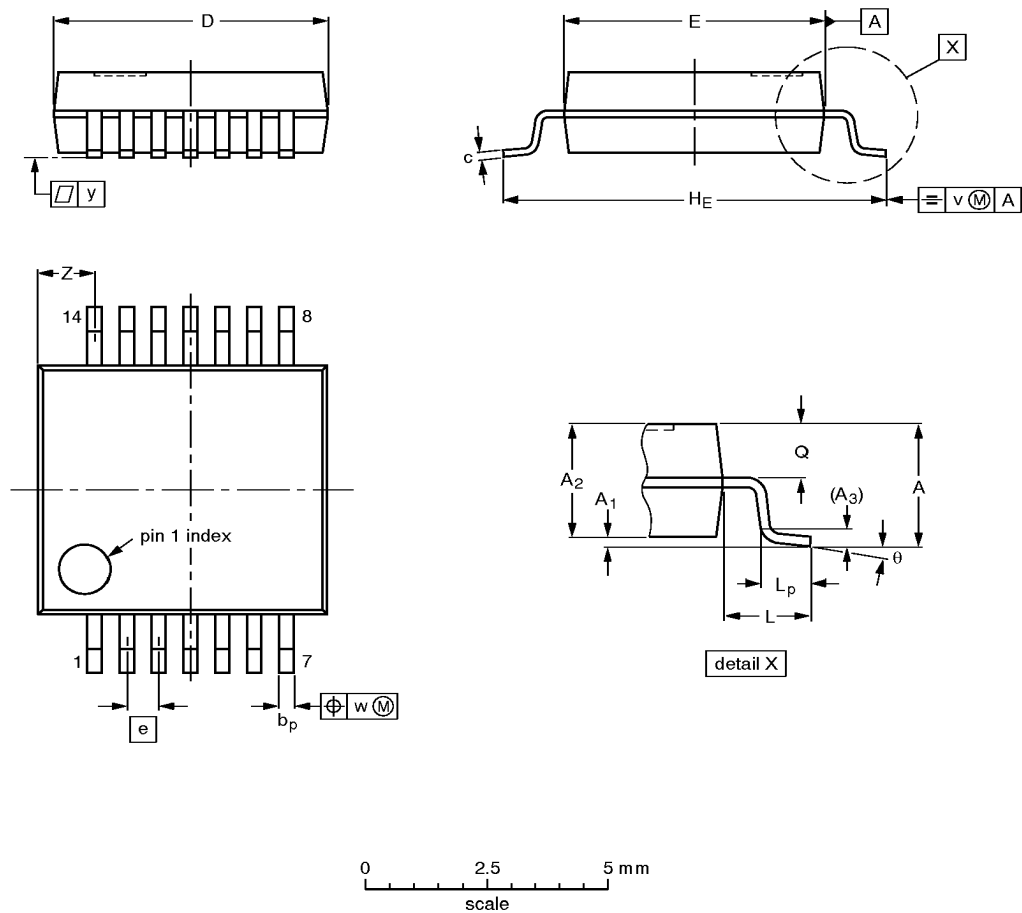
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				91-08-13 95-01-23

Dual 4-bit binary ripple counter

74LV393

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



DIMENSIONS (mm are the original dimensions)

UNIT	A _{max.}	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

Note
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

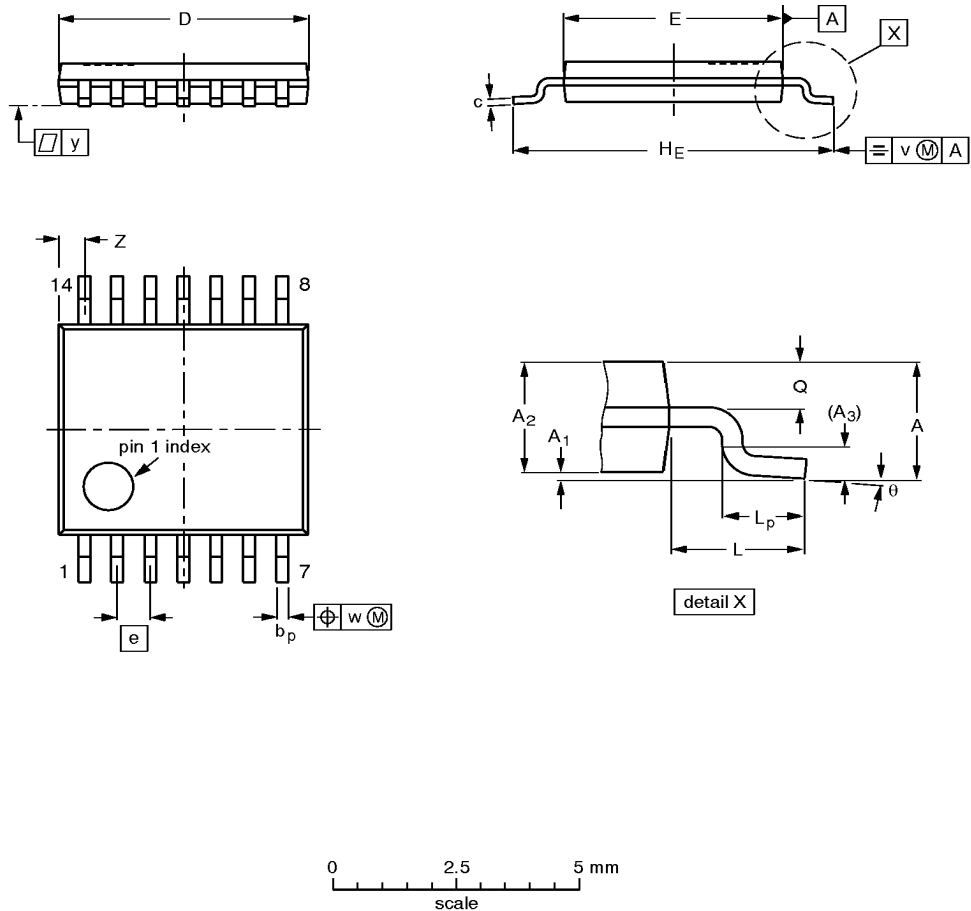
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT337-1		MO-150AB				95-02-04 96-01-18

Dual 4-bit binary ripple counter

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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



DIMENSIONS (mm are the original dimensions)

UNIT	A _{max.}	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT402-1		MO-153				94-07-12- 95-04-04