

## HALF-BRIDGE GATE DRIVER IN W-DFN3030-10 (Type TH)

### Description

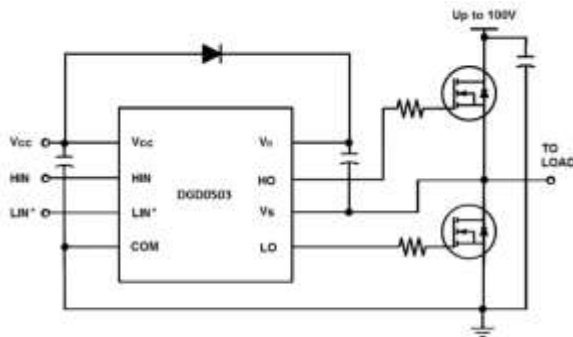
The DGD0503 is a high-voltage, high-speed gate driver capable of driving N-channel MOSFETs and IGBTs in a half-bridge configuration. High voltage processing techniques enable the DGD0503's high-side to switch to 100V in a bootstrap operation.

The DGD0503 logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) to interface easily with controlling devices. The driver output features high pulse current buffers designed for minimum driver cross conduction. DGD0503 has a fixed internal deadtime of 430ns (typical).

The DGD0503 is offered in the W-DFN3030-10 (Type TH) package and operates over an extended -40°C to +125°C temperature range.

### Applications

- DC-DC Converters
- DC-AC Inverters
- AC-DC Power Supplies
- Motor Controls
- Class D Power Amplifiers



Typical Configuration

### Features

- Floating High-Side Driver in Bootstrap Operation to 100V
- Drives Two N-Channel MOSFETs or IGBTs in a Half-Bridge Configuration
- 290mA Source/600mA Sink Output Current Capability
- Outputs Tolerant to Negative Transients
- Internal Dead Time of 430ns to Protect MOSFETs
- Wide Low Side Gate Driver Supply Voltage: 10V to 20V
- Logic Input (HIN and LIN\*) 3.3V Capability
- Schmitt Triggered Logic Inputs
- Undervoltage Lockout for V<sub>CC</sub> (Logic and Low-Side Supply)
- Extended Temperature Range: -40°C to +125°C
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony free. "Green" Device (Note 3)**

### Mechanical Data

- Case: W-DFN3030-10 (Type TH)
- Case Material: Molded Plastic. "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 3 per J-STD-020
- Terminals: Finish – Matte Tin Finish Solderable per MIL-STD-202, Method 208 <sup>(e3)</sup>
- Weight: 0.017 grams (Approximate)



Top View



Bottom View

W-DFN3030-10 (Type TH)

### Ordering Information (Note 4)

Part Number	Marking	Reel Size (inches)	Tape Width (mm)	Quantity Per Reel
DGD0503FN-7	DGD0503	7	8	3,000

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
  2. See [http://www.diodes.com/quality/lead\\_free.html](http://www.diodes.com/quality/lead_free.html) for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

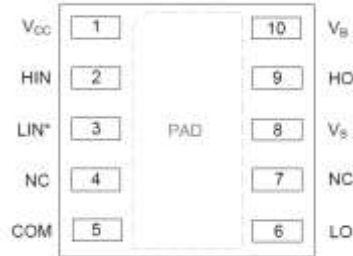
### Marking Information



DGD0503 = Product Type Marking Code  
YY = Year (ex: 17 = 2017)  
WW = Week (01 to 53)

## Pin Diagrams

(Top View)

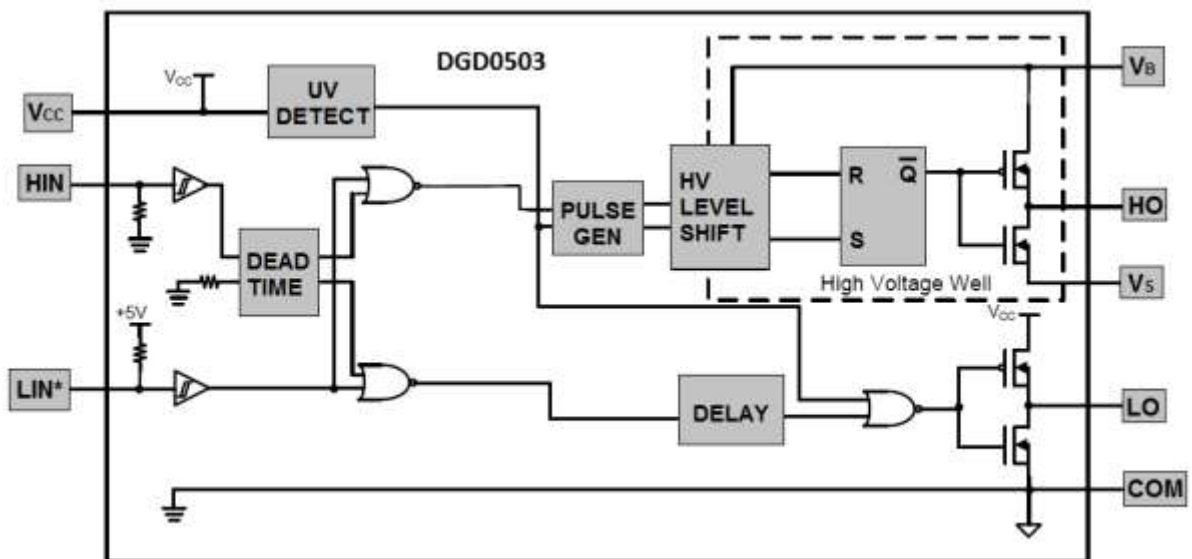


W-DFN3030-10 (Type TH)

## Pin Descriptions

Pin Number	Pin Name	Function
1	V <sub>CC</sub>	Logic and Low Side Supply
2	HIN	Logic Input for High-Side Gate Driver Output in Phase with HO
3	LIN*	Logic Input for Low-Side Gate Driver Output out of Phase with LO
4, 7	NC	No Connection (No Internal Connection)
5	COM	Low-Side and Logic Return
6	LO	Low-Side Gate Drive Output
8	V <sub>S</sub>	High-Side Floating Supply Return
9	HO	High-Side Gate Drive Output
10	V <sub>B</sub>	High-Side Floating Supply
PAD	Substrate	Connect to COM on PCB

## Functional Block Diagram



### Absolute Maximum Ratings (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
High-Side Floating Supply Voltage	V <sub>B</sub>	-0.3 to +124	V
High-Side Floating Supply Offset Voltage	V <sub>S</sub>	V <sub>B</sub> -24 to V <sub>B</sub> +0.3	V
High-Side Floating Output Voltage	V <sub>HO</sub>	V <sub>S</sub> -0.3 to V <sub>B</sub> +0.3	V
Offset Supply Voltage Transient	dV <sub>S</sub> /dt	50	V/ns
Low-Side Fixed Supply Voltage	V <sub>CC</sub>	-0.3 to +24	V
Low-Side Output Voltage	V <sub>LO</sub>	-0.3 to V <sub>CC</sub> +0.3	V
Logic Input Voltage (HIN and LIN*)	V <sub>IN</sub>	-0.3 to V <sub>CC</sub> +0.3	V

### Thermal Characteristics (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Power Dissipation Linear Derating Factor (Note 5)	P <sub>D</sub>	0.4	W
Thermal Resistance, Junction to Ambient (Note 5)	R <sub>θJA</sub>	64	°C/W
Thermal Resistance, Junction to Case (Note 5)	R <sub>θJC</sub>	42	°C/W
Operating Temperature	T <sub>J</sub>	+150	°C
Lead Temperature (Soldering, 10s)	T <sub>L</sub>	+300	
Storage Temperature Range	T <sub>STG</sub>	-55 to +150	

Note: 5. When mounted on a standard JEDEC 2-layer FR-4 board.

### Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
High Side Floating Supply Absolute Voltage	V <sub>B</sub>	V <sub>S</sub> + 10	V <sub>S</sub> + 20	V
High Side Floating Supply Offset Voltage	V <sub>S</sub>	(Note 6)	100	V
High Side Floating Output Voltage	V <sub>HO</sub>	V <sub>S</sub>	V <sub>B</sub>	V
Low Side Fixed Supply Voltage	V <sub>CC</sub>	10	20	V
Low Side Output Voltage	V <sub>LO</sub>	0	V <sub>CC</sub>	V
Logic Input Voltage (HIN and LIN*)	V <sub>IN</sub>	0	5	V
Ambient Temperature	T <sub>A</sub>	-40	+125	°C

Note: 6. Logic operation for V<sub>S</sub> of -5V to +100V. Logic state held for V<sub>S</sub> of -5V to -V<sub>BS</sub>.

## DC Electrical Characteristics

( $V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15V, @  $T_A$  = +25°C, unless otherwise specified.) (Note 7)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Logic "1" (HIN) & Logic "0" (LIN*) Input Voltage	$V_{IH}$	2.5	—	—	V	$V_{CC}$ = 10V to 20V
Logic "0" (HIN) & Logic "1" (LIN*) Input Voltage	$V_{IL}$	—	—	0.8	V	$V_{CC}$ = 10V to 20V
High Level Output Voltage, $V_{BIAS} - V_O$	$V_{OH}$	—	0.05	0.2	V	$I_O$ = 2mA
Low Level Output Voltage, $V_O$	$V_{OL}$	—	0.02	0.1	V	$I_O$ = 2mA
Offset Supply Leakage Current	$I_{LK}$	—	—	50	μA	$V_B = V_S = 100V$
Quiescent $V_{BS}$ Supply Current	$I_{BSQ}$	—	60	100	μA	$V_{IN}$ = 0V or 5V
Quiescent $V_{CC}$ Supply Current	$I_{CCQ}$	—	350	500	μA	$V_{IN}$ = 0V or 5V
Logic "1" Input Bias Current	$I_{IN+}$	—	3	10	μA	HIN = 5V, LIN* = 0V
Logic "0" Input Bias Current	$I_{IN-}$	—	—	5.0	μA	HIN = 0V, LIN* = 5V
$V_{CC}$ Supply Undervoltage Positive Going Threshold	$V_{CCUV+}$	7.4	8.5	9.6	V	—
$V_{CC}$ Supply Undervoltage Negative Going Threshold	$V_{CCUV-}$	7.1	7.8	8.8	V	—
$V_{BS}$ Supply Undervoltage Positive Going Threshold	$V_{BSUV+}$	5.5	6.5	7.5	V	—
$V_{BS}$ Supply Undervoltage Negative Going Threshold	$V_{BSUV-}$	5.3	6.3	7.3	V	—
Output High Short Circuit Pulsed Current	$I_{O+}$	130	290	—	mA	$V_O$ = 0V, PW ≤ 10μs
Output Low Short Circuit Pulsed Current	$I_{O-}$	270	600	—	mA	$V_O$ = 15V, PW ≤ 10μs

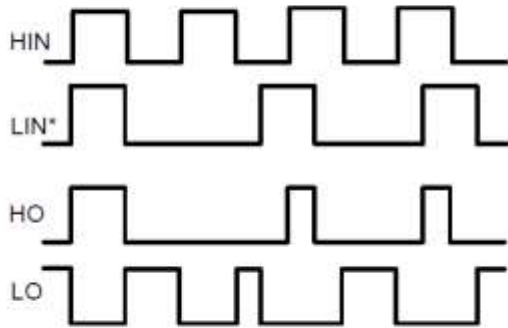
Note: 7. The  $V_{IN}$  and  $I_{IN}$  parameters are applicable to the two logic pins: HIN and LIN\*. The  $V_O$  and  $I_O$  parameters are applicable to the respective output pins: HO and LO.

## AC Electrical Characteristics

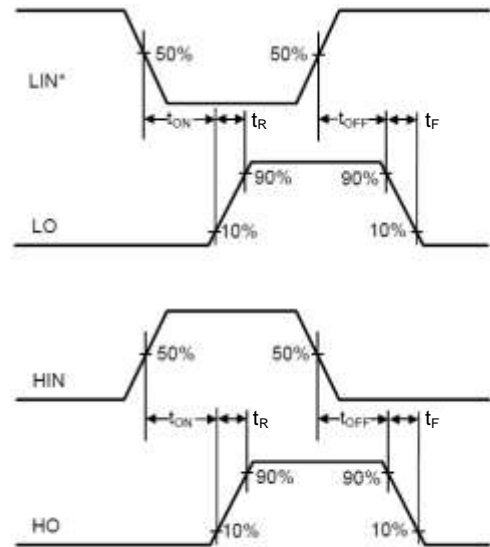
( $V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15V,  $C_L$  = 1000pF, @  $T_A$  = +25°C, unless otherwise specified.)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Turn-On Propagation Delay	$t_{ON}$	—	680	820	ns	$V_S$ = 0V
Turn-Off Propagation Delay	$t_{OFF}$	—	150	220	ns	$V_S$ = 100V
Delay Matching, HO & LO Turn-On/Turn-Off	$t_{DM}$	—	—	60	ns	—
Turn-On Rise Time	$t_R$	—	70	170	ns	$V_S$ = 0V
Turn-Off Fall Time	$t_F$	—	35	90	ns	$V_S$ = 0V
Deadtime: $t_{DT\ LO-HO}$ & $t_{DT\ HO-LO}$	$t_{DT}$	300	430	550	ns	—

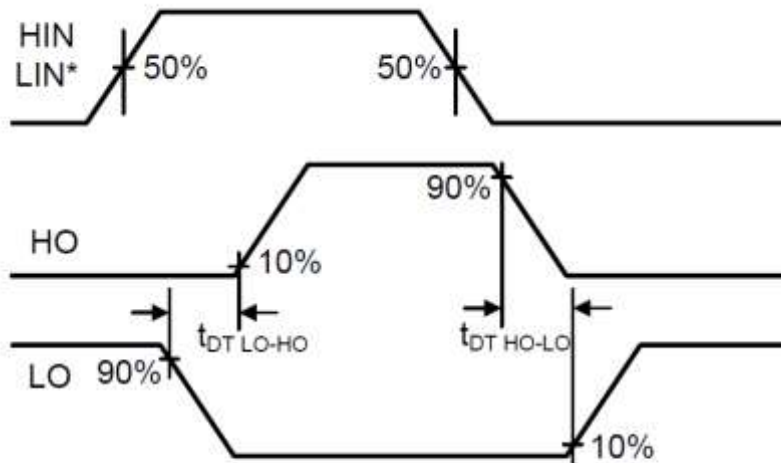
## Timing Waveforms



**Figure 1.** Input / Output Timing Diagram



**Figure 2.** Switching Time Waveform Definitions



**Figure 3.** Deadtime Waveform Definitions

## Typical Performance Characteristics (@T<sub>A</sub> = +25°C, unless otherwise specified.)

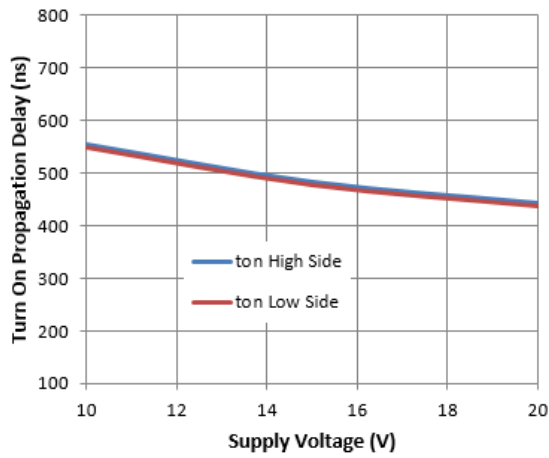


Figure 4. Turn-on Propagation Delay vs. Supply Voltage

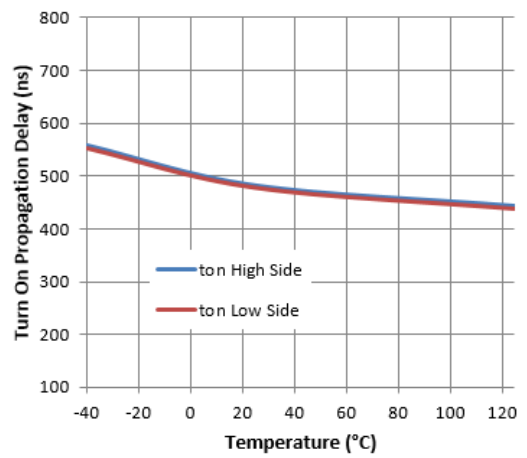


Figure 5. Turn-on Propagation Delay vs. Temperature

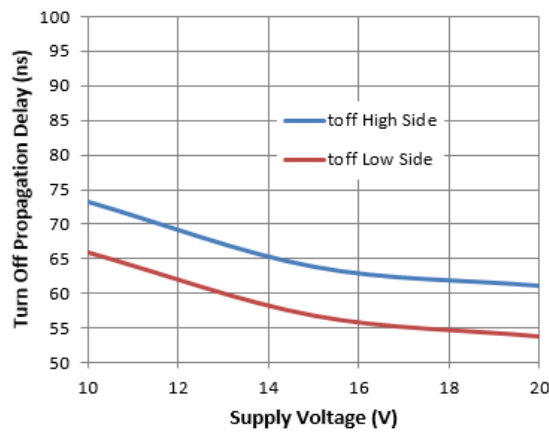


Figure 6. Turn-off Propagation Delay vs. Supply Voltage

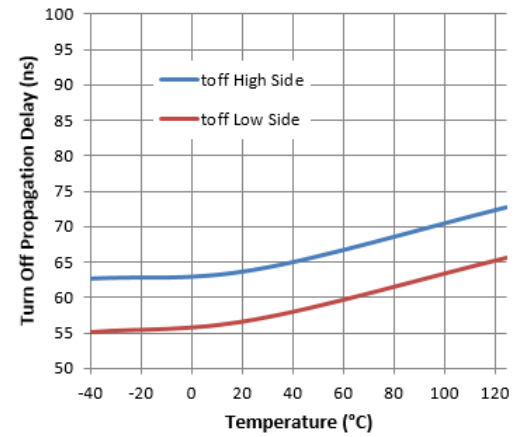


Figure 7. Turn-off Propagation Delay vs. Temperature

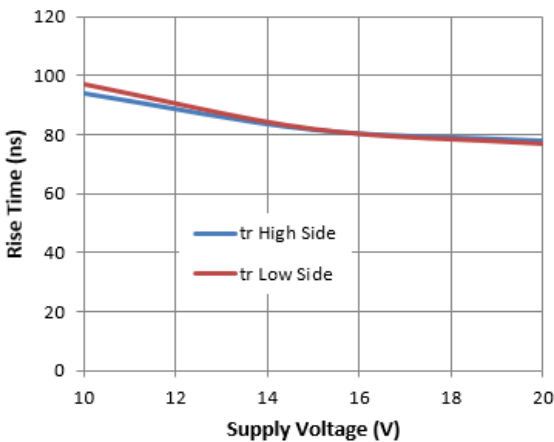


Figure 8. Rise Time vs. Supply Voltage

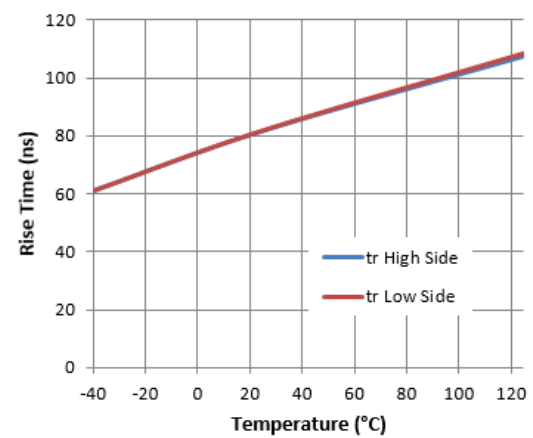


Figure 9. Rise Time vs. Temperature

## Typical Performance Characteristics (Continued)

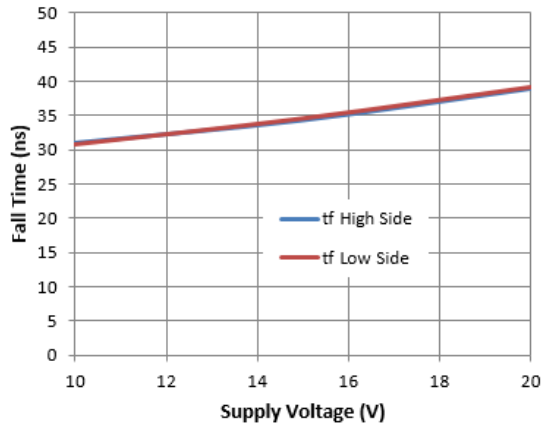


Figure 10. Fall Time vs. Supply Voltage

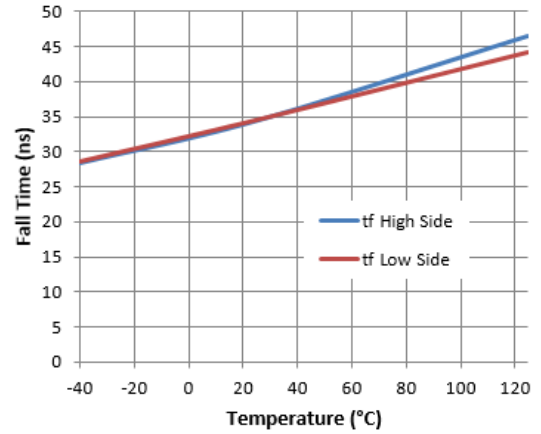


Figure 11. Fall Time vs. Temperature

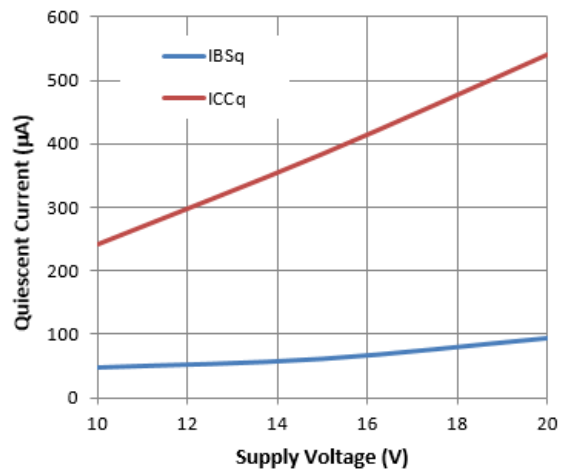


Figure 12. Quiescent Current vs. Supply Voltage

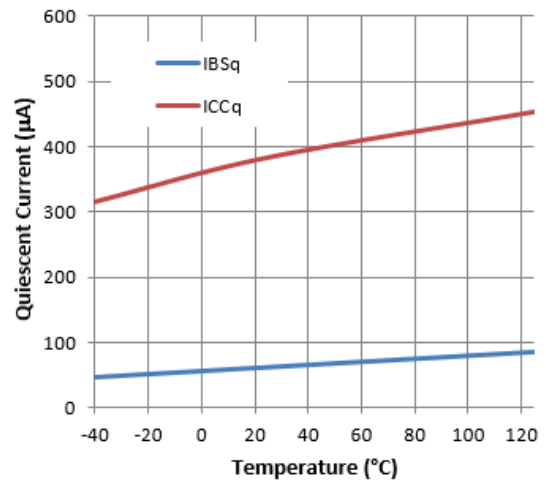


Figure 13. Quiescent Current vs. Temperature

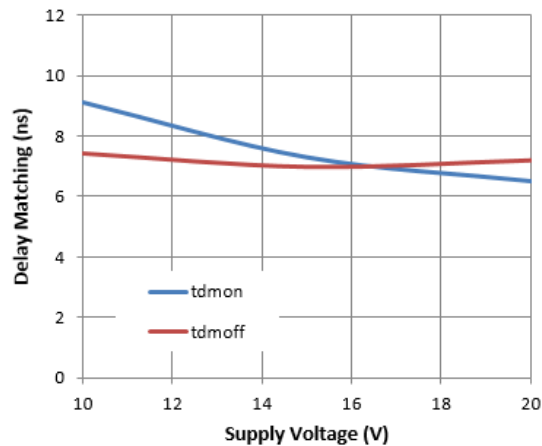


Figure 14. Delay Matching vs. Supply Voltage

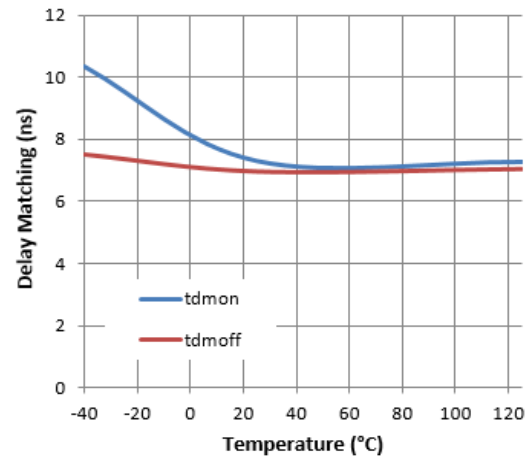


Figure 15. Delay Matching vs. Temperature

## Typical Performance Characteristics (Cont.)

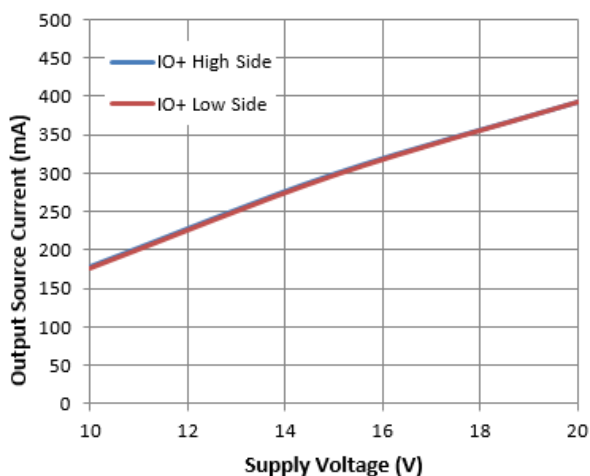


Figure 16. Output Source Current vs. Supply Voltage

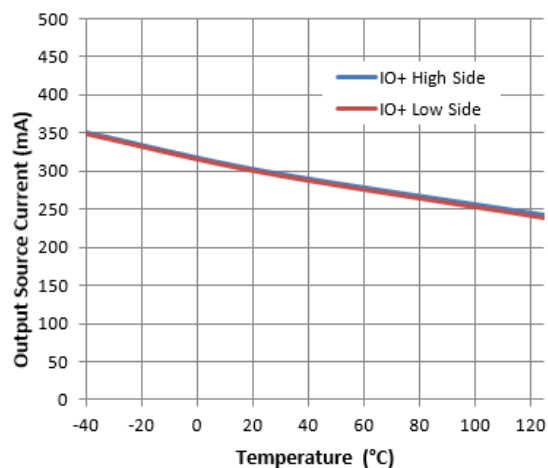


Figure 17. Output Source Current vs. Temperature

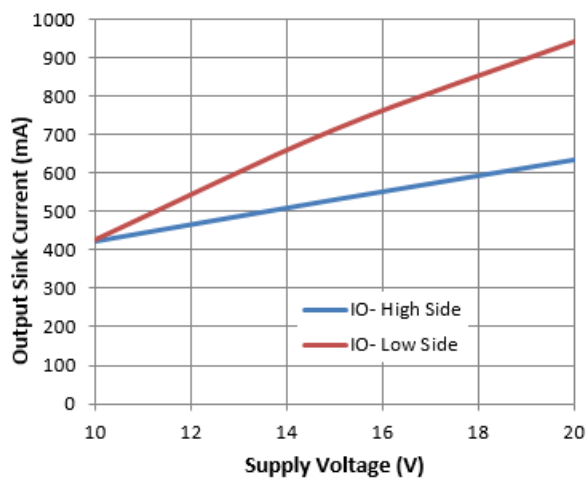


Figure 18. Output Sink Current vs. Supply Voltage

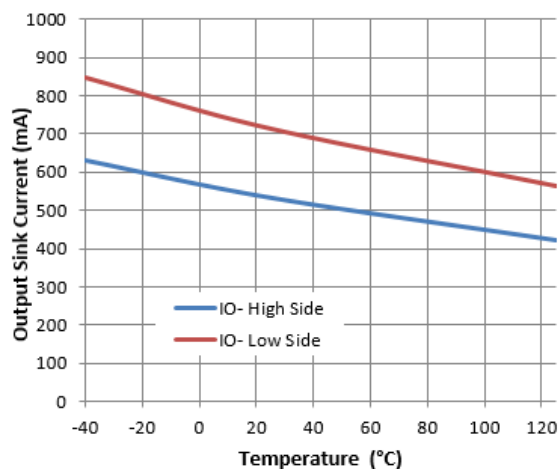


Figure 19. Output Sink Current vs. Temperature

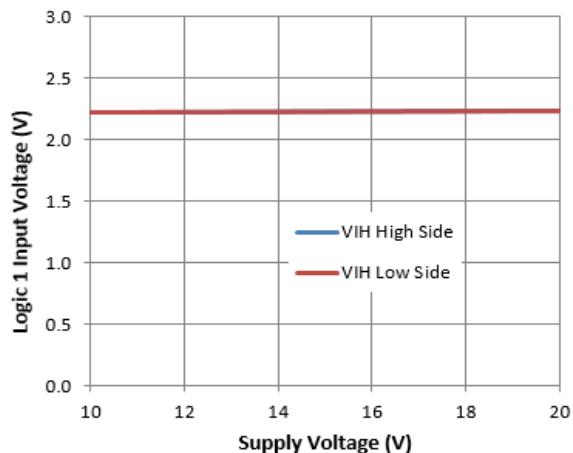


Figure 20. Logic 1 Input Voltage vs. Supply Voltage

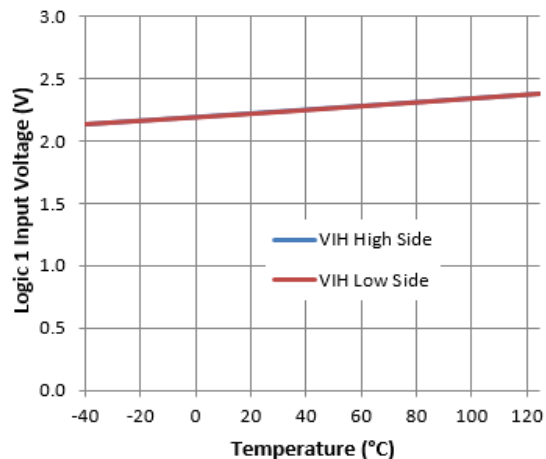


Figure 21. Logic 1 Input Voltage vs. Temperature

## Typical Performance Characteristics (Cont.)

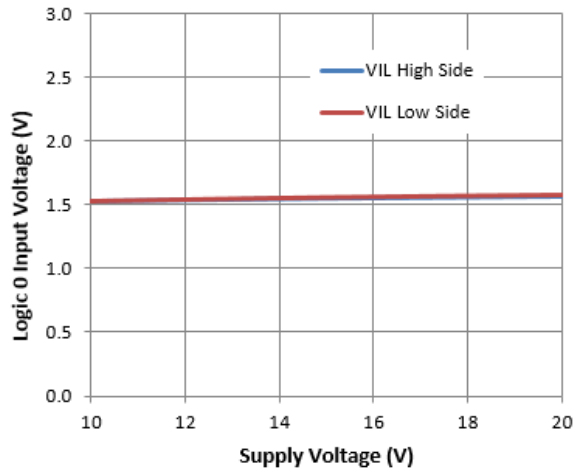


Figure 22. Logic 0 Input Voltage vs. Supply Voltage

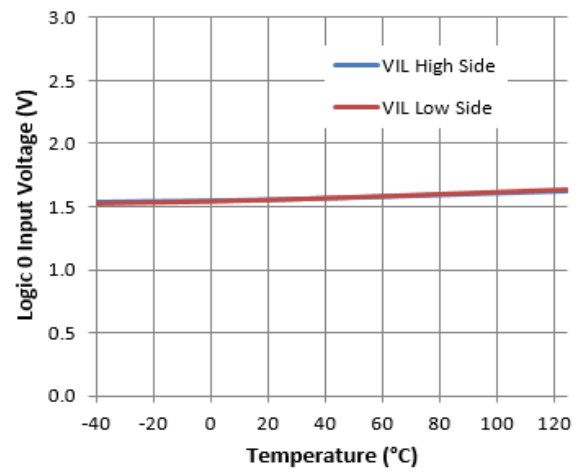


Figure 23. Logic 0 Input Voltage vs. Temperature

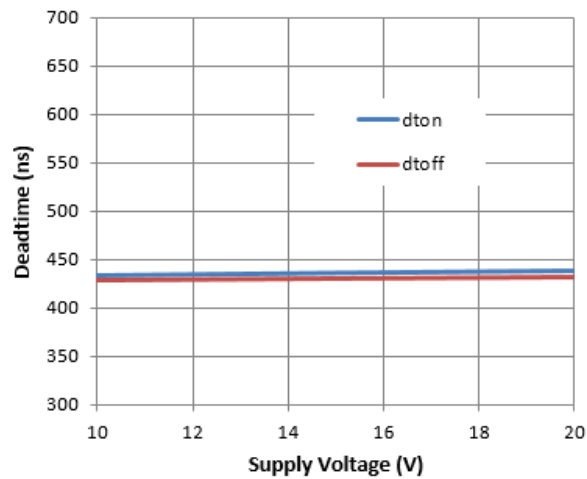


Figure 24. Deadtime vs. Supply Voltage

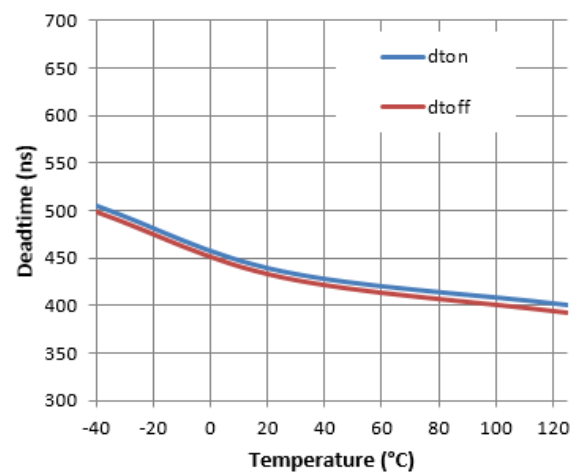


Figure 25. Deadtime vs. Temperature

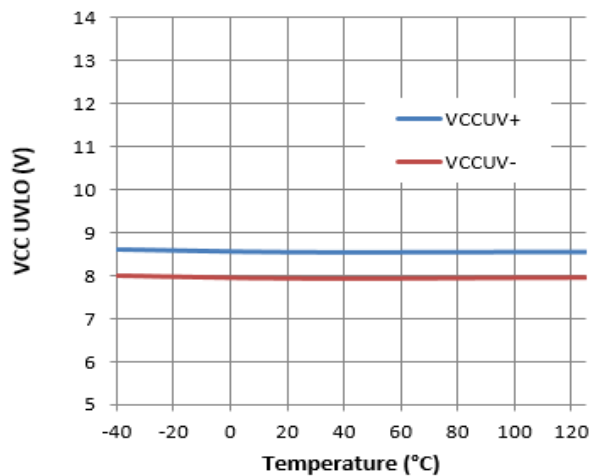


Figure 26. VCC UVLO vs. Temperature

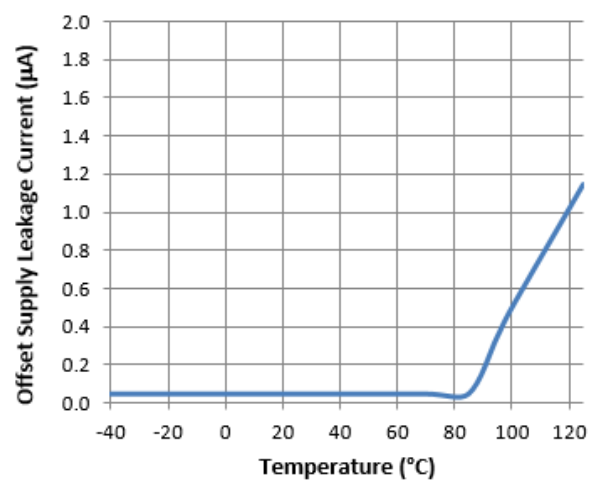
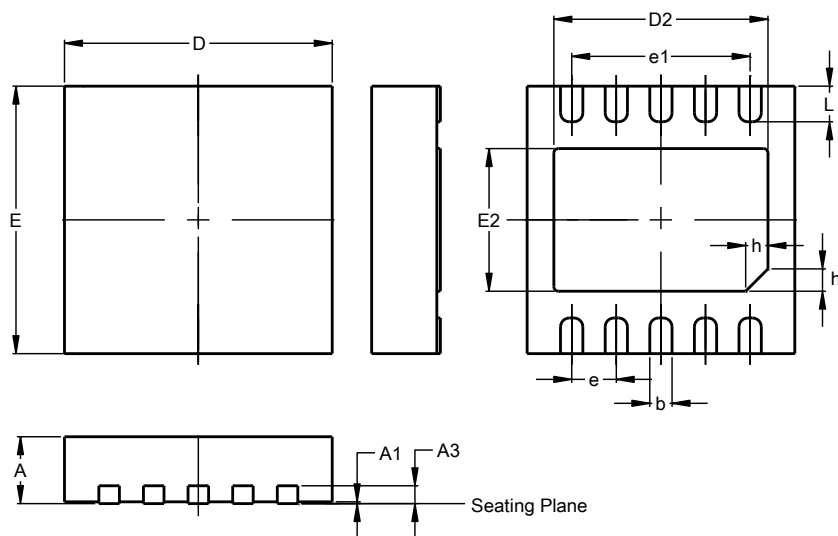


Figure 27. Offset Supply Leakage Current vs. Temperature

## Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

W-DFN3030-10 (Type TH)

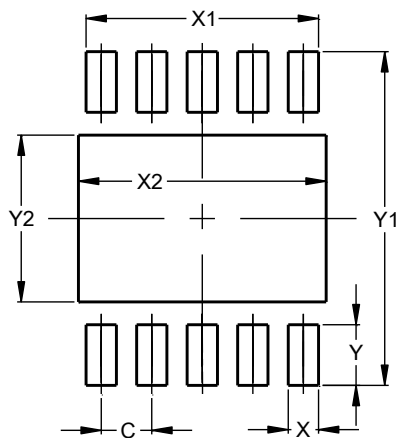


W-DFN3030-10 (Type TH)			
Dim	Min	Max	Typ
A	0.70	0.80	0.75
A1	--	0.05	0.02
A3	0.18	0.25	0.20
b	0.18	0.30	0.25
D	2.90	3.10	3.00
D2	2.40	2.60	2.50
e	0.50BSC		
e1	2.00BSC		
E	2.90	3.10	3.00
E2	1.45	1.65	1.55
h	0.20	0.30	0.25
L	0.30	0.50	0.40
All Dimensions in mm			

## Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

W-DFN3030-10 (Type TH)



Dimensions	Value (in mm)
C	0.500
X	0.300
X1	2.300
X2	2.600
Y	0.600
Y1	3.300
Y2	1.650

Note : For high voltage applications, the appropriate industry sector guidelines should be considered with regards to creepage and clearance distances between device Terminals and PCB tracking.

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