

## SINGLE-CELL LI-ION BATTERY- AND POWER-MANAGEMENT IC

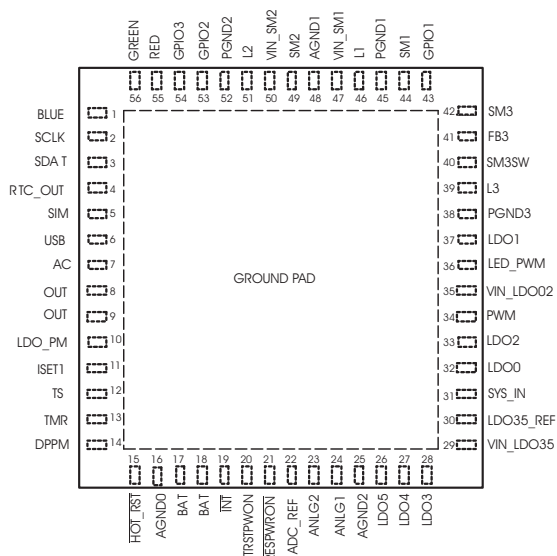
### FEATURES

- **BATTERY CHARGER**
  - Complete charge management solution for single Li-Ion/Li-Pol cell with thermal foldback, dynamic power management, and pack temperature sensing, supporting up to 1.5-A maximum charge current
  - Programmable charge parameters for AC adapter and USB port operation
- **INTEGRATED POWER SUPPLIES**
  - A total of 9 LDOs are integrated:
    - Six adjustable output LDOs (1.25-V to 3.3-V)
    - Two fixed-voltage LDOs (3.3-V)
    - One RTC backup supply with low leakage (3.1-V)
  - Two 600-mA, programmable dc/dc buck converters (0.6-V to 3.4-V) with enable, standby-mode operation, and automatic low-power mode setting
- **DISPLAY FUNCTIONS**
  - Two open-drain PWM outputs with programmable frequency and duty cycle. Can be used to control keyboard backlight, vibrator, or other external peripheral functions
  - RGB LED driver with programmable flashing period and individual R/G/B brightness control
  - Constant-current white LED driver, with programmable current level, brightness control, and overvoltage protection can drive up to 6 LEDs in series configuration
- **SYSTEM MANAGEMENT**
  - Dual input power path function with input current limiting and OV protection
  - POR function with programmable masking monitors all integrated supplies outputs
  - Software and hardware reset functions

- 8-channel integrated A/D samples system parameters with single conversion, peak detection, or averaging operating modes
- **HOST INTERFACE**
  - Host can set system parameters and access system status using I<sup>2</sup>C interface
  - Interrupt function with programmable masking signals system status modification to host
  - 3 GPIO ports, programmable as drivers, integrated A/D trigger or buck converters standby mode control

### APPLICATIONS

- PDAs
- Smart Phones
- MP3s
- Internet Appliances
- Handheld Devices



QFN 56-Pin, 8 x 8 mm Package  
(Top View - Not To Scale)



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## DESCRIPTION

The TPS65800 provides an easy to use, fully integrated solution for handheld devices, integrating charge management, multiple regulated power supplies, system management and display functions, in a small thermally-enhanced 8x8-mm package. The high level of integration enables typical board area space savings of 70% when compared to equivalent discrete solutions, while implementing a high-performance and flexible solution, portable across multiple platforms. If required, an external host may control the TPS65800 via I<sup>2</sup>C interface, with access to all integrated systems. The I<sup>2</sup>C enables setting output voltages, current thresholds, and operation modes. Internal registers have a complete set of status information, enabling easy diagnostics, and host-controlled handling of fault conditions. The TPS65800 can operate in stand-alone mode, with no external host control, if the internal power-up defaults are compatible with the system requirements

### AVAILABLE OPTIONS<sup>(1)</sup>

| T <sub>J</sub> | DEVICES <sup>(2)(3)(4)</sup> | MARKING  |
|----------------|------------------------------|----------|
| –40°C to 125°C | TPS65800RTQ                  | TPS65800 |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at [www.ti.com](http://www.ti.com).
- (2) The RTQ package is available in tape and reel. Add R suffix (TPS65800RTQR) to order quantities of 2000 parts per reel. Add T suffix (TPS65800RTQT) to order quantities of 250 parts per reel.
- (3) This product is RoHS compatible, including a lead concentration that does not exceed 0.1% of total product weight, and is suitable for use in specified lead-free soldering processes. In addition, this product uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.
- (4) Other power-up sequences and default power-up states for the supplies can be implemented upon request. Consult factory for available options.

## FUNCTIONAL BLOCK DIAGRAM

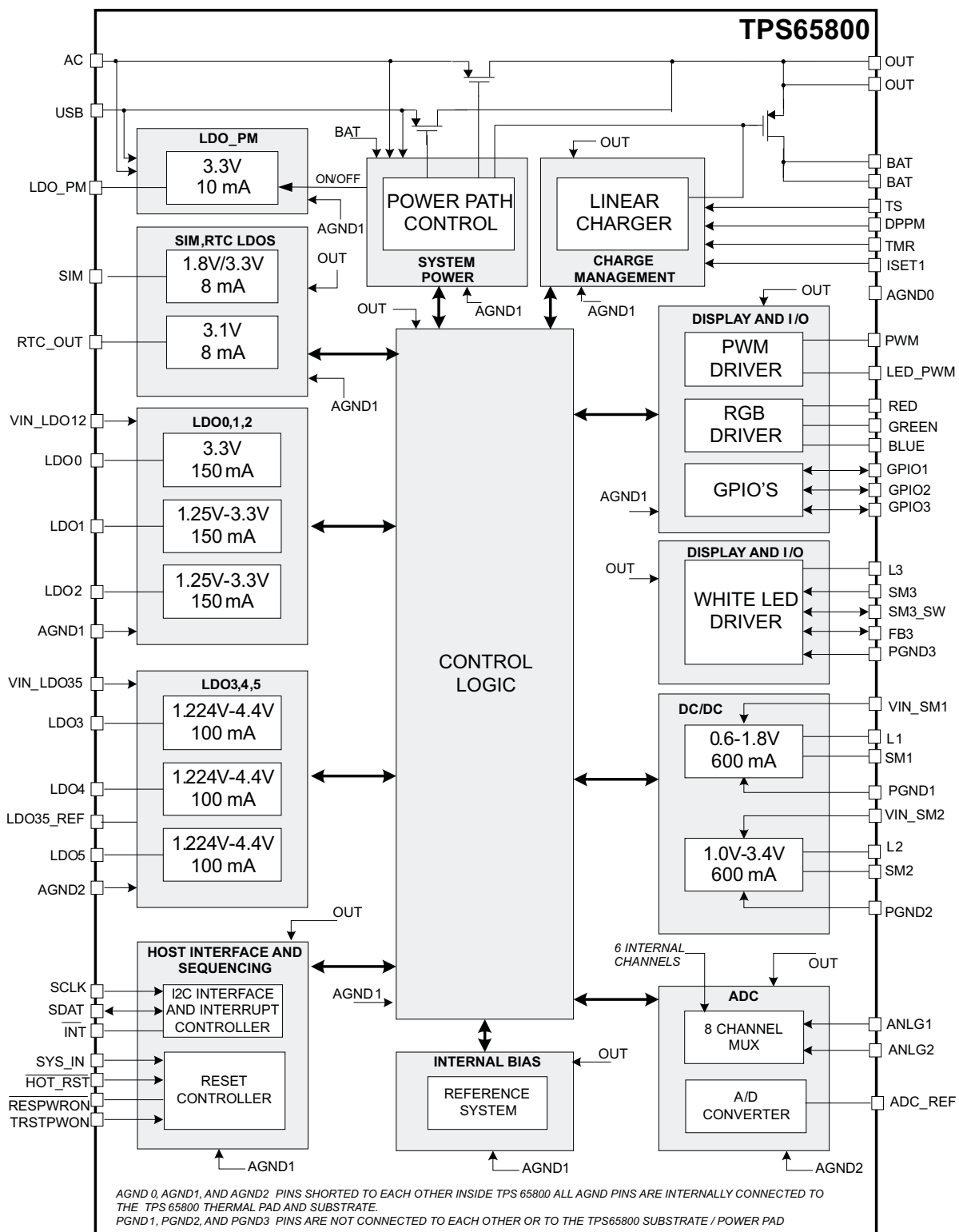


Figure 1. TPS65800 simplified block diagram

**ABSOLUTE MAXIMUM RATINGS**over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                                                              | VALUE                             | UNIT |
|--------------------------------------------------------------|-----------------------------------|------|
| AC and USB with respect to AGND1                             | –0.3 to 18                        | V    |
| ANLG1, ANLG2 with respect to AGND2                           | –0.3 to V(OUT)                    |      |
| V(OUT) with respect to AGND1                                 | 5                                 |      |
| VIN_LDO12, VIN_LDO35, LDO3, LDO4, LDO5 with respect to AGND2 | –0.3 to V(OUT)                    |      |
| LDO35_REF, ADC_REF with respect to AGND2                     | –0.3 to smaller of: 3.6 or V(OUT) |      |
| SIM, RTC_OUT with respect to AGND1                           | –0.3 to smaller of: 3.6 or V(OUT) |      |
| SM1, L1, VIN_SM1 with respect to PGND1                       | –0.3 to V(OUT)                    |      |
| SM2, L2, VIN_SM2 with respect to PGND2                       | –0.3 to V(OUT)                    |      |
| SM3, L3 with respect to PGND3                                | –0.3 to 29                        |      |
| SM3SW with respect to PGND3                                  | –0.3 to V(OUT)                    |      |
| FB3 with respect to PGND3                                    | –0.3 to 0.5                       |      |
| All other pins (except AGND and PGND), with respect to AGND1 | –0.3 to V(OUT)                    |      |
| AGND2, AGND0, PGND1, PGND2, PGND3 with respect to AGND1      | –0.3 to +0.3                      |      |
| Input Current, AC pin                                        | 2750                              | mA   |
| Input Current, USB pin                                       | 600                               |      |
| Output continuous current, OUT pin                           | 3000                              |      |
| Output continuous current, BAT pin                           | –3000                             |      |
| Continuous Current at L1, PGND1, L2, PGND2                   | 1800                              |      |
| T <sub>A</sub> Operating free-air temperature                | –40 to 85                         | °C   |
| T <sub>J</sub> Maximum junction temperature                  | 125                               |      |
| T <sub>STG</sub> Storage temperature                         | –65 to 150                        |      |
| Lead temperature 1,6 mm (1/16-inch) from case for 10 seconds | 260                               |      |
| ESD rating, all pins                                         | 1.5                               | kV   |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**DISSIPATION RATINGS**

| PACKAGE               | $\theta_{JA}$ | T <sub>A</sub> ≤ 55°C<br>POWER RATING | DERATING FACTOR<br>ABOVE T <sub>A</sub> = 55°C |
|-----------------------|---------------|---------------------------------------|------------------------------------------------|
| RTQ <sup>(1)(2)</sup> | 21.7°C/W      | 3.22 W                                | 0.046 W/°C                                     |

(1) This data is based on using the JEDEC High-K board and the exposed die pad is connected to a Cu pad on the board. This is connected to the ground plane by a via matrix.

(2) The RTQ package MSL level: HIR3 at 260°C

## RECOMMENDED OPERATING CONDITIONS

|                                                                         | MIN                                                                                                    | MAX                 | UNIT |
|-------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------|---------------------|------|
| AC and USB with respect to AGND1                                        | 4.35                                                                                                   | 16.5 <sup>(1)</sup> | V    |
| ANLG1, ANLG2 with respect to AGND2                                      | 0                                                                                                      | 2.6                 | V    |
| VIN_LDO35 with respect to AGND2                                         | Greater of: 3.6 V OR minimum input voltage required for LDO/converter operation outside dropout region | 4.7                 | V    |
| VIN_LDO12 with respect to AGND1                                         |                                                                                                        | 4.7                 |      |
| VIN_SM1 with respect to PGND1                                           |                                                                                                        | 4.7                 |      |
| VIN_SM2 with respect to PGND2                                           |                                                                                                        | 4.7                 |      |
| SM3 with respect to PGND3                                               |                                                                                                        | 28                  | V    |
| T <sub>A</sub> Operating free-air temperature                           | –40                                                                                                    | 85                  | °C   |
| T <sub>J(0p)</sub> Junction temperature, functional operation assured   | –40                                                                                                    | 125                 | °C   |
| T <sub>J</sub> Junction temperature, electrical characteristics assured | 0                                                                                                      | 125                 | °C   |

(1) Thermal operating restrictions are reduced or avoided if input voltage does not exceed 5 V.

## ELECTRICAL CHARACTERISTICS – I<sup>2</sup>C INTERFACE

Over recommended operating conditions (typical values at  $T_j = 25^\circ\text{C}$ ), application circuit as in figure (unless otherwise noted)

| PARAMETER                                    | TEST CONDITIONS                                                      | MIN | TYP  | MAX | UNIT          |
|----------------------------------------------|----------------------------------------------------------------------|-----|------|-----|---------------|
| <b>I<sup>2</sup>C TIMING CHARACTERISTICS</b> |                                                                      |     |      |     |               |
| $t_r$                                        | SCLK/SDATA rise time                                                 |     |      | 300 | ns            |
| $t_f$                                        | SCLK/SDATA fall time                                                 |     |      | 300 |               |
| $t_{w(H)}$                                   | SCLK pulse duration, high                                            | 600 |      |     |               |
| $t_{w(L)}$                                   | SCLK pulse duration, low                                             | 1.3 |      |     | $\mu\text{s}$ |
| $t_{\text{SU(STA)}}$                         | Setup time for START condition                                       | 600 |      |     | ns            |
| $t_{\text{H(STA)}}$                          | START condition hold time after which first clock pulse is generated | 600 |      |     |               |
| $t_{\text{SU(DAT)}}$                         | Data setup time                                                      | 100 |      |     |               |
| $t_{\text{H(DAT)}}$                          | Data hold time                                                       | 0   |      |     |               |
| $t_{\text{SU(STOP)}}$                        | Setup time for STOP condition                                        | 600 |      |     | $\mu\text{s}$ |
| $t_{\text{(BUF)}}$                           | Bus free time between START and STOP condition                       | 1.3 |      |     |               |
| F <sub>SCL</sub>                             | Clock frequency                                                      |     |      | 400 | kHz           |
| <b>I<sup>2</sup>C INTERFACE LOGIC LEVELS</b> |                                                                      |     |      |     |               |
| $V_{\text{IH}}$                              | High level input voltage                                             | 1.3 |      | 6   | V             |
| $V_{\text{IL}}$                              | Low level input voltage                                              | 0   |      | 0.4 |               |
| $I_{\text{H}}$                               | Input bias current                                                   |     | 0.01 |     | $\mu\text{A}$ |

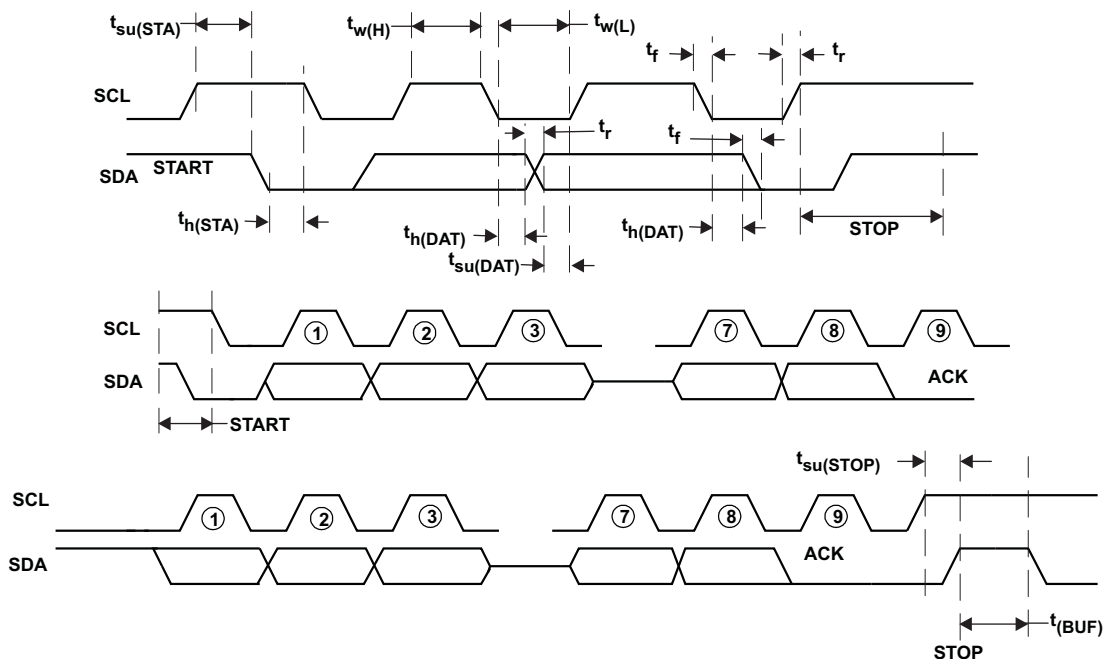


Figure 2. I<sup>2</sup>C Timing

## ELECTRICAL CHARACTERISTICS – SYSTEM SEQUENCING AND OPERATING MODES

Over recommended operating conditions (typical values at  $T_j = 25^\circ\text{C}$ ), application circuit as in [Figure 3](#) (unless otherwise noted).

| PARAMETER                                 |                                                | TEST CONDITIONS                                                                                                                                                          | MIN  | TYP  | MAX  | UNIT  |
|-------------------------------------------|------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|-------|
| QUIESCENT CURRENT                         |                                                |                                                                                                                                                                          |      |      |      |       |
| I <sub>BAT(SLEEP)</sub>                   | BAT pin current, sleep mode set                | Input power not detected, V(BAT) = 4.2 V, Sleep mode set                                                                                                                 |      | 370  |      | μA    |
| I <sub>BAT(DONE)</sub>                    | BAT pin current, charge terminated             | Charger function enabled by I <sup>2</sup> C, termination detected, input power detected and selected                                                                    |      | 3    |      |       |
| I <sub>BAT(CHGOFF)</sub>                  | BAT pin current, charge function OFF           | Charger function disabled by I <sup>2</sup> C, termination not detected, input power detected and selected                                                               |      | 3    |      |       |
| I <sub>INP(CHGOFF)</sub>                  | AC or USB pin current, charge function OFF     | Charger function disabled by I <sup>2</sup> C, termination not detected, input power detected and selected. All integrated supplies and drivers OFF, no load at OUT pin. |      |      | 200  |       |
| UNDERVOLTAGE LOCKOUT                      |                                                |                                                                                                                                                                          |      |      |      |       |
| V <sub>UVLO</sub>                         | Internal UVLO detection threshold              | NO POWER mode set at V(OUT) < V <sub>UVLO</sub> , V(OUT) decreasing                                                                                                      | −3%  | 2.5  | 3%   | V     |
| V <sub>UVLO_HYS</sub>                     | UVLO detection hysteresis                      | V(OUT) increasing                                                                                                                                                        |      | 120  |      | mV    |
| t <sub>DGL(UVLO)</sub>                    | UVLO detection deglitch time                   | Falling voltage only                                                                                                                                                     |      | 5    |      | ms    |
| SYSTEM LOW VOLTAGE THRESHOLD              |                                                |                                                                                                                                                                          |      |      |      |       |
| V <sub>LOW_SYS</sub>                      | Minimum system voltage detection threshold     | System voltage V(SYS_IN) decreasing, SLEEP mode set if V(SYS_IN) < V <sub>LOW_SYS</sub>                                                                                  | 0.97 | 1    | 1.03 | V     |
| V <sub>HYS(LOWSYS)</sub>                  | Minimum system voltage detection hysteresis    | V(SYS_IN) increasing                                                                                                                                                     |      | 50   |      | mV    |
| t <sub>DGL(LOWSYS)</sub>                  | Minimum system voltage detection deglitch time | V(SYS_IN) decreasing                                                                                                                                                     |      | 5    |      | ms    |
| THERMAL FAULT                             |                                                |                                                                                                                                                                          |      |      |      |       |
| T <sub>SHUT</sub>                         | Thermal shutdown                               | Increasing junction temperature                                                                                                                                          |      | 165  |      | °C    |
| T <sub>HYS(SHUT)</sub>                    | Thermal shutdown hysteresis                    | Decreasing junction temperature                                                                                                                                          |      | 30   |      |       |
| INTEGRATED SUPPLY POWER FAULT DETECTION   |                                                |                                                                                                                                                                          |      |      |      |       |
| V <sub>PGOOD</sub>                        | Power-good fault detection threshold           | Falling output voltage, applies to all integrated supply outputs. Referenced to the programmed output voltage value                                                      | 85%  | 90%  | 93%  |       |
| V <sub>HYS(PGOOD)</sub>                   | Power-good fault detection hysteresis          | Rising output voltage, applies to all integrated supply outputs. Referenced to V <sub>PGOOD</sub> threshold                                                              | 3%   | 5%   | 7%   |       |
| HOT RESET FUNCTION                        |                                                |                                                                                                                                                                          |      |      |      |       |
| V <sub>HRSTON</sub>                       | Low-level input voltage                        | RESET mode set at V(HOT_RESET) < V <sub>HRSTON</sub>                                                                                                                     |      |      | 0.4  | V     |
| V <sub>HRSTOFF</sub>                      | High level input voltage                       | HOT reset not active at V(HOT_RESET) > V <sub>HRSTOFF</sub>                                                                                                              | 1.3  |      |      |       |
| t <sub>DGL(HOTRST)</sub>                  | Hot reset input deglitch                       |                                                                                                                                                                          |      | 5    |      | ms    |
| SYSTEM RESET – OPEN DRAIN OUTPUT RESPWRON |                                                |                                                                                                                                                                          |      |      |      |       |
| V <sub>RSTLO</sub>                        | Low level output voltage                       | I <sub>L</sub> = 10 mA, V(RES PWON) < V <sub>RSTLO</sub>                                                                                                                 | 0    |      | 0.3  | V     |
| I <sub>TRSTPWON</sub>                     | Pullup current source                          | Internally connected to TRSTPWON pin                                                                                                                                     | 0.9  | 1.0  | 1.12 | μA    |
| K <sub>RESET</sub>                        | Reset timer constant                           | T <sub>RESET</sub> = K <sub>RESET</sub> × C <sub>TRSTPWON</sub>                                                                                                          |      | 1    |      | ms/nF |
| SEQUENCING DELAYS                         |                                                |                                                                                                                                                                          |      |      |      |       |
| t <sub>DLY(D1)</sub>                      | Sequencing delay                               | See sequencing timing diagram                                                                                                                                            |      | 0.24 |      | ms    |
| t <sub>DLY(D1)</sub>                      | Sequencing delay                               | See sequencing timing diagram                                                                                                                                            |      | 12   |      |       |

## ELECTRICAL CHARACTERISTICS – POWER PATH AND CHARGE MANAGEMENT

Over recommended operating conditions (typical values at  $T_j = 25^\circ\text{C}$ ), application circuit as in [Figure 3](#) (unless otherwise noted).

| PARAMETER                                     |                                                                 | TEST CONDITIONS                                                                                                                                       | MIN                    | TYP  | MAX  | UNIT  |
|-----------------------------------------------|-----------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------|------|------|-------|
| VOLTAGE DETECTION THRESHOLDS                  |                                                                 |                                                                                                                                                       |                        |      |      |       |
| V <sub>IN(DT)</sub>                           | Input Voltage detection threshold                               | AC detected at V(AC)– V(BAT) > V <sub>IN(DT)</sub> ;<br>USB detected at V(USB)– V(BAT) > V <sub>IN(DT)</sub>                                          | 190                    |      |      | mV    |
| V <sub>IN(NDT)</sub>                          | Input Voltage removal threshold                                 | AC not detected at V(AC)– V(BAT) < V <sub>IN(NDT)</sub> ;<br>USB not detected at V(USB)– V(BAT) < V <sub>IN(NDT)</sub>                                |                        |      | 125  |       |
| t <sub>DGL(NDT)</sub>                         | Power not detected deglitch                                     |                                                                                                                                                       |                        | 22.5 |      | ms    |
| V <sub>SUP(DT)</sub>                          | Supplement detection threshold                                  | Battery switch ON at V(BAT) – V(OUT) > V <sub>SUP(DT)</sub>                                                                                           |                        | 60   |      | mV    |
| V <sub>SUP(NDT)</sub>                         | Supplement not detected threshold                               | Battery switch OFF at V(BAT)– V(OUT) < V <sub>SUP(NDT)</sub>                                                                                          |                        | 20   |      |       |
| POWER PATH INTEGRATED MOSFETs CHARACTERISTICS |                                                                 |                                                                                                                                                       |                        |      |      |       |
| V <sub>ACDO</sub>                             | AC switch dropout voltage                                       | V <sub>ACDO</sub> = V(AC)– V(OUT); V(AC) = 4.75 V AC input current limit set to 2.75 A (typ), I <sub>O(OUT)</sub> = 1.0 A                             |                        | 350  | 375  | mV    |
| V <sub>USBDO</sub>                            | USB switch dropout voltage                                      | V <sub>USBDO</sub> = V(USB)– V(OUT); V(USB) = 4.6 V USB input current limit set to 2.75 A (typ)                                                       | I(OUT) + I(BAT)= 0.5 A | 175  | 190  |       |
|                                               |                                                                 |                                                                                                                                                       | I(OUT) + I(BAT)= 0.1 A | 35   | 45   |       |
| V <sub>BATDODCH</sub>                         | Battery switch dropout voltage, discharge                       | V(BAT): 3 V → V <sub>CH(REG)</sub> , I(BAT) = –1 A                                                                                                    |                        | 60   | 100  |       |
| V <sub>BATDOCH</sub>                          | Battery switch dropout voltage, charge                          | Charger on, V(BAT): 3 V → 4.2 V, I(BAT) = 1 A                                                                                                         |                        | 60   | 100  |       |
| POWER PATH INPUT CURRENT LIMIT                |                                                                 |                                                                                                                                                       |                        |      |      |       |
| I <sub>INP(LIM1)</sub>                        | Selected Input current limit, applies to USB input only         | Selected input switch not in dropout, I <sup>2</sup> C settings: ISET2 = LO, PSEL = LO                                                                |                        | 80   | 100  | mA    |
| I <sub>INP(LIM2)</sub>                        | Selected Input current limit, applies to USB input only         | Selected input switch not in dropout, I <sup>2</sup> C settings: ISET2 = HI, PSEL = LO                                                                |                        | 400  | 500  |       |
| I <sub>INP(LIM3)</sub>                        | Selected Input current limit, applies to either AC or USB input | Selected input switch not in dropout, I <sup>2</sup> C settings: ISET2 = HI OR LO, PSEL = HI                                                          |                        |      | 2.75 | A     |
| SYSTEM REGULATION VOLTAGE                     |                                                                 |                                                                                                                                                       |                        |      |      |       |
| V <sub>SYS(REG)</sub>                         | Output regulation voltage                                       | V <sub>SYS(REG)</sub> = V(OUT), DPPM loop not active, selected input current limit not reached. Selected input voltage (AC or USB) > 5.1 V            |                        | 4.6  | 4.7  | V     |
| POWER PATH PROTECTION AND RECOVERY FUNCTIONS  |                                                                 |                                                                                                                                                       |                        |      |      |       |
| V <sub>INOUTSH</sub>                          | Input-to-output short-circuit detection threshold               | AC and USB switches set to OFF if V(OUT) < V <sub>INOUTSH</sub>                                                                                       |                        | 0.6  |      | V     |
| R <sub>SH(USBSH)</sub>                        | OUT short circuit recovery pullup resistor                      | V(OUT) < 1 V, internal resistor connected from USB to OUT                                                                                             |                        | 500  |      | Ω     |
| R <sub>SH(ACSH)</sub>                         | OUT short circuit recovery pullup resistor                      | V(OUT) < 1 V, internal resistor connected from AC to OUT                                                                                              |                        | 500  |      |       |
| V <sub>OVP</sub>                              | Overvoltage detection threshold                                 | Rising voltage, overvoltage detected when V(AC) > V <sub>OVP</sub> or V(USB) > V <sub>OVP</sub>                                                       | 6                      | 6.5  | 6.8  | V     |
|                                               | Overvoltage detection hysteresis                                | Falling voltage, relative to detection threshold                                                                                                      |                        | 0.1  |      |       |
| V <sub>BATOUTSH</sub>                         | Battery to Output short circuit detection threshold             | BAT switch set to OFF if V(BAT)-V(OUT)> V <sub>BATOUTSH</sub>                                                                                         |                        | 200  |      | mV    |
| K <sub>BLK(SHBAT)</sub>                       | Battery-to-ouput short-circuit blanking time constant           | V(DPPM) < 1v, t <sub>BLK(SHBAT)</sub> = K <sub>BLK(SHBAT)</sub> × C <sub>DPPM</sub> , C <sub>DPPM</sub> capacitor is connected from DPPM pin to AGND1 |                        | 1    |      | ms/nF |
| I <sub>SH(BAT)</sub>                          | OUT short circuit recovery pullup current source                | V <sub>(BAT) – V<sub>(OUT)</sub></sub> > V <sub>BATOUTSH</sub> , internal current source connected between OUT and BAT                                |                        | 10   |      | mA    |
| R <sub>SH(BAT)</sub>                          | BAT short circuit recovery resistor                             | V <sub>(BAT)</sub> < 1 V, Internal resistor connected from OUT to BAT                                                                                 |                        | 1    |      | kΩ    |
| R <sub>DCH(BAT)</sub>                         | BAT pulldown resistor                                           | Internal resistor connected from BAT to AGND1 when battery is not detected by ANLG1                                                                   |                        | 500  |      | Ω     |



## ELECTRICAL CHARACTERISTICS – POWER PATH AND CHARGE MANAGEMENT (Continued)

Over recommended operating conditions (typical values at  $T_J = 25^\circ\text{C}$ ), application circuit as in [Figure 3](#) (unless otherwise noted).

| PARAMETER                                                                                                               |                                                       | TEST CONDITIONS                                                                                          |                                         | MIN                                       | TYP   | MAX   | UNIT |
|-------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------|----------------------------------------------------------------------------------------------------------|-----------------------------------------|-------------------------------------------|-------|-------|------|
| POWER PATH TIMING CHARACTERISTICS, DPPM AND THERMAL LOOPS NOT ACTIVE, R <sub>TMR</sub> = 50 kΩ                          |                                                       |                                                                                                          |                                         |                                           |       |       |      |
| t <sub>BOOT</sub>                                                                                                       | Boot-up time                                          | Measured from input power detection                                                                      |                                         | 120                                       | 200   | 300   | ms   |
| t <sub>SW(ACBAT)</sub>                                                                                                  | Switching from AC to BAT                              | No USB: measured from V(AC)– V(BAT) < V <sub>IN(NDT)</sub> , USB detected:CE=LO (after CE hold-off time) |                                         |                                           |       | 50    | μs   |
| t <sub>SW(USBBAT)</sub>                                                                                                 | Switching from USB to BAT                             | No AC: measured from V(USB)– V(BAT) < V <sub>IN(NDT)</sub> ,USB detected:CE=LO (after CE hold-off time)  |                                         |                                           |       | 50    |      |
| t <sub>SW(PSEL)</sub>                                                                                                   | Switching from USB to AC                              | Toggling I <sup>2</sup> C PSEL bit                                                                       |                                         |                                           |       | 50    |      |
| t <sub>SW(ACUSB)</sub>                                                                                                  | Switching from AC to USB or USB to AC                 | AC power removed or USB power removed                                                                    |                                         |                                           |       | 100   |      |
| BATTERY REMOVAL DETECTION                                                                                               |                                                       |                                                                                                          |                                         |                                           |       |       |      |
| V <sub>NOBATID</sub>                                                                                                    | Battery ID resistor detection                         | ID resistor not detected at V(OUT)– V(ANLG1) < V <sub>NOBATID</sub>                                      |                                         | 0.5                                       |       |       | V    |
| t <sub>DGL(NOBAT)</sub>                                                                                                 | Deglitch time for battery removal detection           |                                                                                                          |                                         | 0.6                                       |       | 1.2   | ms   |
| I <sub>O(ANLG1)</sub>                                                                                                   | ANLG1 pullup current                                  | Set via I <sup>2</sup> C bits (BATID1,BATID2) ADC_WAIT register                                          | 00, V <sub>(OUT)</sub> : 2.5 V to 4.4 V | $\frac{V(OUT) - 1.2}{500\text{ k}\Omega}$ |       |       | μA   |
|                                                                                                                         |                                                       |                                                                                                          | 01                                      | 10                                        |       |       |      |
|                                                                                                                         |                                                       |                                                                                                          | 10                                      | 50                                        |       |       |      |
|                                                                                                                         |                                                       |                                                                                                          | 11                                      | 60                                        |       |       |      |
|                                                                                                                         |                                                       |                                                                                                          | Total accuracy                          |                                           |       | 25%   |      |
| FAST CHARGE CURRENT, V(OUT) > V(BAT) + 0.1 V, V(BAT) > V <sub>Lowv</sub>                                                |                                                       |                                                                                                          |                                         |                                           |       |       |      |
| I <sub>O(BAT)</sub>                                                                                                     | Charge current range                                  | $I_{O(BAT)} = \frac{K_{(SET)} \times V_{(SET)}}{R_{SET}}$                                                |                                         | 100                                       |       | 1500  | mA   |
| V <sub>SET</sub>                                                                                                        | Battery charge current set voltage                    | V <sub>SET</sub> = V(SET1), (SET1_1, SET1_0) =                                                           | 11, 100% scaling                        | 2.475                                     | 2.500 | 2.525 | V    |
|                                                                                                                         |                                                       |                                                                                                          | 10, 75% scaling                         | 1.875                                     | 1.900 | 1.925 |      |
|                                                                                                                         |                                                       |                                                                                                          | 01, 50% scaling                         | 1.225                                     | 1.250 | 1.275 |      |
|                                                                                                                         |                                                       |                                                                                                          | 00, 25% scaling                         | 0.575                                     | 0.600 | 0.625 |      |
| K <sub>SET</sub>                                                                                                        | Battery charge current set factor                     | 100 mA < I <sub>O(BAT)</sub> ≤ 1 A                                                                       |                                         | 350                                       | 400   | 450   |      |
|                                                                                                                         |                                                       | 1 mA < I <sub>O(BAT)</sub> ≤ 100 mA                                                                      |                                         | 100                                       | 400   | 1000  |      |
| PRECHARGE CURRENT, V(OUT) > V(BAT) + 0.1 V, V <sub>BATSH</sub> < V(BAT) < V <sub>Lowv</sub> , t < t <sub>(PRECHG)</sub> |                                                       |                                                                                                          |                                         |                                           |       |       |      |
| I <sub>O(PRECHG)</sub>                                                                                                  | Precharge current range                               | $I_{O(PRECHG)} = \frac{V_{(PRECHG)} \times K_{(SET)}}{R_{SET}}$                                          |                                         | 10                                        |       | 150   | mA   |
| V <sub>PRECHG</sub>                                                                                                     | Precharge set voltage                                 | V <sub>PRECHG</sub> = V(SET1)                                                                            |                                         | 220                                       | 250   | 270   | mV   |
| V <sub>Lowv</sub>                                                                                                       | Precharge to fast-charge transition                   | Fast charge at V(BAT) > V <sub>Lowv</sub>                                                                |                                         | 2.8                                       | 3     | 3.2   | V    |
| t <sub>DGL(PRE)</sub>                                                                                                   | Deglitch time for fast charge to precharge transition | Decreasing battery voltage, R <sub>TMR</sub> = 50 kΩ                                                     |                                         |                                           | 22.5  |       | ms   |
| CHARGE REGULATION VOLTAGE, V(OUT) > V <sub>O(BATREG)</sub> + 0.1V                                                       |                                                       |                                                                                                          |                                         |                                           |       |       |      |
| V <sub>O(BATREG)</sub>                                                                                                  | Battery charge voltage                                | Voltage options, selection via I <sup>2</sup> C                                                          |                                         | 4.2                                       |       |       | V    |
|                                                                                                                         |                                                       |                                                                                                          |                                         | 4.356                                     |       |       |      |
|                                                                                                                         |                                                       | Accuracy, T <sub>A</sub> = 25°C                                                                          |                                         | –0.5%                                     |       | 0.5%  |      |
|                                                                                                                         |                                                       | Total accuracy                                                                                           |                                         | –1%                                       |       | 1%    |      |
| CHARGE TERMINATION, V(BAT) > V <sub>RCH</sub> , VOLTAGE REGULATION MODE SET                                             |                                                       |                                                                                                          |                                         |                                           |       |       |      |
| I <sub>TERM</sub>                                                                                                       | Charge termination current range                      | $I_{(TERM)} = \frac{V_{(TERM)} \times K_{(SET)}}{R_{SET}}$                                               |                                         | 10                                        |       | 150   | mA   |
| V <sub>TERM</sub>                                                                                                       | Battery termination detection set voltage             | V <sub>TERM</sub> = V(SET1), (SET1_1, SET1_0) =                                                          | 11, 100% scaling                        | 240                                       | 260   | 280   | mV   |
|                                                                                                                         |                                                       |                                                                                                          | 10, 75% scaling                         | 145                                       | 160   | 175   |      |
|                                                                                                                         |                                                       |                                                                                                          | 01, 50% scaling                         | 90                                        | 110   | 130   |      |
|                                                                                                                         |                                                       |                                                                                                          | 00, 25% scaling                         | 40                                        | 60    | 75    |      |
| t <sub>DGL(TERM)</sub>                                                                                                  | Deglitch time for termination detection               | V(SET1) < V <sub>TERM</sub> , R <sub>TMR</sub> = 50 kΩ                                                   |                                         |                                           | 22.5  |       | ms   |

**ELECTRICAL CHARACTERISTICS – POWER PATH AND CHARGE MANAGEMENT (Continued)**

Over recommended operating conditions (typical values at  $T_J = 25^\circ\text{C}$ ), application circuit as in [Figure 3](#) (unless otherwise noted).

| PARAMETER                         |                                                         | TEST CONDITIONS                                                                                                                          | MIN   | TYP                     | MAX   | UNIT |
|-----------------------------------|---------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------|-------|-------------------------|-------|------|
| BATTERY RECHARGE DETECTION        |                                                         |                                                                                                                                          |       |                         |       |      |
| V <sub>RCH</sub>                  | Recharge threshold voltage                              | New charge cycle starts if V(BAT) < V <sub>O(BATREG)</sub> – V <sub>RCH</sub> , after termination was detected                           | 80    | 100                     | 130   | mV   |
| t <sub>DGL(RCH)</sub>             | Deglintch time for recharge detection                   | R <sub>TMR</sub> = 50 kΩ                                                                                                                 |       | 22.5                    |       | ms   |
| DPPM FUNCTION                     |                                                         |                                                                                                                                          |       |                         |       |      |
| V <sub>DPPM</sub>                 | DPPM regulation point range                             | V <sub>(DPPM)</sub> = R <sub>DPPM</sub> × K <sub>DPPMM</sub> × I <sub>O(DPPM)</sub>                                                      | 2.6   |                         | 4.4   | V    |
| I <sub>O(DPPM)</sub>              | DPPM pin current source                                 | AC or USB Present                                                                                                                        | 95    | 100                     | 105   | μA   |
| K <sub>DPPM</sub>                 | DPPM scaling factor                                     |                                                                                                                                          | 1.139 | 1.15                    | 1.162 |      |
| t <sub>DGL(DPPM)</sub>            | DPPM de-glintch time                                    | Status bit set indicating DPPM loop active after deglintch time, R <sub>TMR</sub> = 50 kΩ                                                |       | 500                     |       | μs   |
| PACK TEMPERATURE SENSING          |                                                         |                                                                                                                                          |       |                         |       |      |
| V <sub>LTF</sub>                  | Low-temperure threshold                                 | Pack low temperature fault at V(TS) > V <sub>LTF</sub>                                                                                   | 2.465 | 2.5                     | 2.535 | V    |
| V <sub>HTF</sub>                  | High-temperure threshold                                | Pack low temperature fault at V(TS) < V <sub>HTF</sub>                                                                                   | 0.485 | 0.5                     | 0.515 |      |
| I <sub>O(TS)</sub>                | Temperature-sense current source                        | Thermistor bias current                                                                                                                  | 18.8  | 20                      | 21.2  | μA   |
| t <sub>DLG(TFAULT )</sub>         | Deglintch time for temperature fault detection          | R(TMR) = 50 kΩ, V(TS) > V <sub>LTF</sub> OR V(TS) < V <sub>HTF</sub>                                                                     |       | 22.5                    |       | ms   |
| CHARGE AND PRECHARGE SAFETY TIMER |                                                         |                                                                                                                                          |       |                         |       |      |
| t <sub>CHG</sub>                  | Charge safety timer programmed value                    | Safety timer range, thermal/DPPM loop not active, t <sub>CHG</sub> = R <sub>TMR</sub> × K <sub>TMR</sub>                                 | 3     | 5                       | 10    | h    |
| K <sub>TMR</sub>                  | Charge timer set factor                                 |                                                                                                                                          | 0.313 | 0.360                   | 0.414 | s/Ω  |
| t <sub>CHGADD</sub>               | Total elapsed time when DPPM or thermal loop are active | Fast charge on, t <sub>CHGADD</sub> is the maximum add-on time added to t <sub>CHG</sub>                                                 |       | 2 × t <sub>CHG</sub>    |       | h    |
| t <sub>PRECHG</sub>               | Precharge safety timer programmed value                 | Precharge safety timer range, thermal/DPPM loop not active, t <sub>PRECHG</sub> = K <sub>PRE</sub> × R <sub>TMR</sub> × K <sub>TMR</sub> | 18    | 30                      | 60    | min  |
| K <sub>PRE</sub>                  | Precharge timer set factor                              |                                                                                                                                          | 0.09  | 0.1                     | 0.11  |      |
| t <sub>PCHGADD</sub>              | Total elapsed time when DPPM or thermal loop are active | Precharge on, t <sub>PCHGADD</sub> is the maximum add-on time added to t <sub>PRECHG</sub>                                               |       | 2 × t <sub>PRECHG</sub> |       | h    |
| R <sub>TMR</sub>                  | External timer resistor limits                          |                                                                                                                                          | 30    |                         | 100   | kΩ   |
| R <sub>TMR(FLT)</sub>             | Timer fault recovery pullup resistor                    | Internal resistor connected from OUT to BAT after safety timer timeout                                                                   |       | 1                       |       | kΩ   |
| CHARGER THERMAL SHUTDOWN          |                                                         |                                                                                                                                          |       |                         |       |      |
| T <sub>THCHG</sub>                | Charger thermal shutdown                                | Charger turned off when T <sub>J</sub> > T <sub>THCHG</sub>                                                                              |       | 150                     |       | °C   |
| T <sub>THCHGHYS</sub>             | Charger thermal shutdown hystersis                      |                                                                                                                                          |       | 30                      |       |      |
| THERMAL REGULATION LOOP           |                                                         |                                                                                                                                          |       |                         |       |      |
| T <sub>THREG</sub>                | Temperature regulation limit                            | Charge current decreasesd and timer extended when T <sub>J</sub> > T <sub>THREG</sub>                                                    | 115   |                         | 135   | °C   |

## ELECTRICAL CHARACTERISTICS – LINEAR REGULATORS

Over recommended operating conditions (typical values at  $T_j = 25^\circ\text{C}$ ), application circuit as in [Figure 3](#) (unless otherwise noted).

| PARAMETER                                                  |                                                               | TEST CONDITIONS                                                                                          | MIN   | TYP                                                                                                   | MAX  | UNIT          |
|------------------------------------------------------------|---------------------------------------------------------------|----------------------------------------------------------------------------------------------------------|-------|-------------------------------------------------------------------------------------------------------|------|---------------|
| <b>SELECTABLE OUTPUT VOLTAGE LDOS: LDO1, LDO2</b>          |                                                               |                                                                                                          |       |                                                                                                       |      |               |
| $I_{Q(LDO12)}$                                             | Quiescent current, either LDO1 or LDO2 enabled, LDO0 disabled | $I_{Q(LDO12)} = I(VIN\_LDO02)$                                                                           |       | 15                                                                                                    |      | $\mu\text{A}$ |
|                                                            |                                                               | $I_{(LDO1,2)} = -1\text{ mA}$                                                                            |       |                                                                                                       |      |               |
|                                                            |                                                               | $I_{(LDO1,2)} = -150\text{ mA}$                                                                          |       | 160                                                                                                   |      |               |
| $I_{O(LDO1,2)}$                                            | Output current range                                          |                                                                                                          |       |                                                                                                       | 150  | mA            |
| $V_{O(LDO1,2)}$                                            | LDO1, LDO2 output voltage                                     | Output voltage, selectable via $I^2C$ .                                                                  |       | Available output voltages:<br>$V_{O(LDO1,2)TYP} = 1.25, 1.5, 1.8, 2.5, 2.85, 3, 3.2, 3.3$             |      | V             |
|                                                            |                                                               | Dropout voltage, 150 mA load                                                                             |       |                                                                                                       | 300  | mV            |
|                                                            |                                                               | Total accuracy, $V(VIN\_LDO02) = 3.65\text{ V}$                                                          | -3%   |                                                                                                       | 3%   |               |
|                                                            |                                                               | Line regulation, 100-mA load, $V(VIN\_LDO02): V_{(LDO1,2)TYP} + 0.5\text{ V} \rightarrow 4.7\text{ V}$   | -1%   |                                                                                                       | 1%   |               |
|                                                            |                                                               | Load regulation, load: 10 mA $\rightarrow$ 150 mA<br>$V(VIN\_LDO02) > V_{O(LDO1,2)TYP} + 0.5\text{ V}$   | -1.5% |                                                                                                       | 1.5% |               |
| $P_{SR(LDO12)}$                                            | PSRR at 20 kHz                                                | 150-mA load at output, $V(VIN\_LDO02) - V_{O(LDO1,2)} = 1\text{ V}$                                      |       | 40                                                                                                    |      | dB            |
| $I_{SC(LDO1,2)}$                                           | LDO1&2 short-circuit current limit                            | Output grounded                                                                                          |       | 300                                                                                                   |      | mA            |
| $R_{DCH(LDO1,2)}$                                          | Discharge resistor                                            | LDO disabled by $I^2C$ command                                                                           |       | 300                                                                                                   |      | $\Omega$      |
| $I_{LKG(LDO1,2)}$                                          | Leakage current                                               | LDO off                                                                                                  |       | 2                                                                                                     |      | $\mu\text{A}$ |
| $t_{SSLDO1,2}$                                             | Soft start ramp time                                          |                                                                                                          |       | 500                                                                                                   |      | $\mu\text{s}$ |
| $t_{SS\_DELAYDO1,2}$                                       | Startup delay                                                 | Measured from the time when the enable bit is set                                                        |       | 20                                                                                                    |      | $\mu\text{s}$ |
| <b>SIM LINEAR REGULATOR</b>                                |                                                               |                                                                                                          |       |                                                                                                       |      |               |
| $I_{Q(SIM)}$                                               | Quiescent current                                             | Internally connected to OUT pin                                                                          |       | 20                                                                                                    |      | $\mu\text{A}$ |
| $I_{O(SIM)}$                                               | Output current range                                          |                                                                                                          |       |                                                                                                       | 8    | mA            |
| $V_{O(SIM)}$                                               | SIM LDO output voltage                                        | Output voltage, selectable via $I^2C$ .                                                                  |       | Available output voltages:<br>$V_{O(SIM)TYP} = 1.8\text{ or }3$                                       |      | V             |
|                                                            |                                                               | Dropout voltage, 8-mA load                                                                               |       |                                                                                                       | 0.2  |               |
|                                                            |                                                               | Total accuracy, $V(OUT): 3.2\text{ V to }4.7\text{ V}, 8\text{ mA}$                                      | -5%   |                                                                                                       | 5%   |               |
|                                                            |                                                               | Load regulation, load: 1 mA $\rightarrow$ 8 mA,<br>$V(OUT) > V_{O(SIM)TYP} + 0.5\text{ V}$               | -3%   |                                                                                                       | 3%   |               |
|                                                            |                                                               | Line regulation, 5 mA load, $V(OUT):$<br>$V_{O(SIM)TYP} + 0.5\text{ V} \rightarrow 4.7\text{ V}$         | -2%   |                                                                                                       | 2%   |               |
| $I_{SC(SIM)}$                                              | Short Circuit current limit                                   | Output grounded                                                                                          |       | 20                                                                                                    |      | mA            |
| $I_{LKG(SIM)}$                                             | Leakage current                                               | LDO off                                                                                                  |       | 1                                                                                                     |      | $\mu\text{A}$ |
| <b>PROGRAMMABLE OUTPUT VOLTAGE LDO'S: LDO3, LDO4, LDO5</b> |                                                               |                                                                                                          |       |                                                                                                       |      |               |
| $I_{Q(LDO35)}$                                             | Quiescent current, only one of LDO3, LDO4, LDO5 is enabled    | $I_{Q(LDO35)} = I(VIN\_LDO35)$                                                                           |       | 70                                                                                                    |      | $\mu\text{A}$ |
| $I_{O(LDO35)}$                                             | Output current range                                          |                                                                                                          |       |                                                                                                       | 100  | mA            |
| $V_{O(LDO35)}$                                             | LDO3, LDO4, LDO5 output voltage                               | Output voltage, selectable via $I^2C$                                                                    |       | Available output voltages:<br>$V_{O(LDO35)TYP} = 1.224\text{ V to }4.46\text{ V}, 25\text{ mV steps}$ |      | V             |
|                                                            |                                                               | Dropout voltage, 100-mA load                                                                             |       |                                                                                                       | 240  | mV            |
|                                                            |                                                               | Total accuracy, 100-mA load $V(VIN\_LDO35) = 5\text{ V}$                                                 | -3%   |                                                                                                       | 3%   |               |
|                                                            |                                                               | Load regulation, $V(VIN\_LDO35) > V_{O(LDO35)TYP} + 0.5\text{ V}$                                        | -1%   |                                                                                                       | 1%   |               |
|                                                            |                                                               | Line regulation, 10 mA load,<br>$V(VIN\_LDO35): V_{O(LDO35)TYP} + 0.5\text{ V} \rightarrow 4.7\text{ V}$ | -1%   |                                                                                                       | 1%   |               |
| $I_{SC(LDO35)}$                                            | Short-circuit current limit                                   | Output grounded                                                                                          |       | 250                                                                                                   |      | mA            |
| $PSR_{(LDO35)}$                                            | PSRR at 10 kHz                                                | $V(VIN\_LDO35) > V_{O(LDO3,5)} + 1\text{ V}, 50\text{-mA load at output}$                                |       | 40                                                                                                    |      | dB            |
| $R_{DCH(LDO35)}$                                           | Discharge resistor                                            | LDO is disabled by $I^2C$ command                                                                        |       | 400                                                                                                   |      | $\Omega$      |
| $I_{LKG(LDO35)}$                                           | Leakage current                                               | LDO off                                                                                                  |       | 1                                                                                                     |      | $\mu\text{A}$ |
| $t_{SSLDO3,5}$                                             | Soft-start ramp time                                          |                                                                                                          |       | 120                                                                                                   |      | $\mu\text{s}$ |
| $t_{SS\_DELAYDO3,5}$                                       | Startup delay                                                 | Measured from the time when the enable bit is set                                                        |       | 70                                                                                                    |      | $\mu\text{s}$ |

**ELECTRICAL CHARACTERISTICS – LINEAR REGULATORS (continued)**

Over recommended operating conditions (typical values at  $T_J = 25^\circ\text{C}$ ), application circuit as in [Figure 3](#) (unless otherwise noted).

| PARAMETER                 |                               | TEST CONDITIONS                                                                |                       | MIN     | TYP | MAX  | UNIT |
|---------------------------|-------------------------------|--------------------------------------------------------------------------------|-----------------------|---------|-----|------|------|
| RTC_OUT LINEAR REGULATOR  |                               |                                                                                |                       |         |     |      |      |
| I <sub>Q(RTC_OUT)</sub>   | Quiescent current for RTC LDO | Internally connected to OUT pin                                                |                       | 20      |     |      | μA   |
| I <sub>O(RTC_OUT)</sub>   | Output current range          |                                                                                |                       | 8       |     |      | mA   |
| V <sub>O(RTC_OUT)</sub>   | RTC_OUT output voltage        | Fixed output voltage value                                                     |                       | 3.1     |     |      | V    |
|                           |                               | Dropout voltage, I(RTC_OUT) = −8 mA                                            |                       | 200     |     |      | mV   |
|                           |                               | Total accuracy, V(OUT): 2 V to 4.7 V, 8-mA load, sleep mode not set            |                       | −5%     |     | 5%   |      |
|                           |                               | Load regulation, load: 1 mA → 8 mA, 2 V < V(OUT) < 4.7 V                       |                       | −3%     |     | 3%   |      |
|                           |                               | Line regulation, 5-mA load, V(OUT): 2 V → 4.7 V                                |                       | −2%     |     | 2%   |      |
| I <sub>SH(RTC_OUT)</sub>  | Short circuit current limit   | V(RTC_OUT) = 0 V                                                               |                       | 20      |     |      | mA   |
| I <sub>LKG(RTC_OUT)</sub> | Leakage current               | V(RTC_OUT) = 1.5 V, V(OUT) = 0 V                                               | T <sub>J</sub> = 85°C | 880     |     |      | nA   |
|                           |                               |                                                                                | T <sub>J</sub> = 25°C | 250     |     |      |      |
| LDO0 LINEAR REGULATOR     |                               |                                                                                |                       |         |     |      |      |
| I <sub>Q(LDO0)</sub>      | Quiescent current             | Internally connected to VIN_LDO12 pin                                          | I(LDO0) = −1 mA       | 15      |     |      | μA   |
|                           |                               |                                                                                | I(LDO0) = −150 mA     | 160     |     |      |      |
| I <sub>O(LDO0)</sub>      | Output current range          |                                                                                |                       | 150     |     |      | mA   |
| V <sub>O(LDO0)</sub>      | Output voltage                | Fixed output voltage value                                                     |                       | 3.3     |     |      | V    |
|                           |                               | Dropout voltage, I(LDO0) = −150 mA                                             |                       | 300     |     |      | mV   |
|                           |                               | Total accuracy                                                                 |                       | −3%     |     | 3%   |      |
|                           |                               | Line regulation, V(OUT): V <sub>O(LDO0)</sub> + 0.5 → 4.7 V, I(LDO0) =− 100 mA |                       | −1%     |     | 1%   |      |
|                           |                               | Load regulation, I(LDO0) = −10 mA →− 150 mA                                    |                       | −1.5%   |     | 1.5% |      |
| PSR <sub>(LDO0)</sub>     | PSRR at 20 kHz                | 150 mA load at output, V(VIN_LDO12) − V <sub>O(LDO1,2)</sub> = 1 V             |                       | 40      |     |      | dB   |
| I <sub>SC(LDO0)</sub>     | Short-circuit current limit   | V(LDO0) = 0 V                                                                  |                       | 300     |     |      | mA   |
| I <sub>LKG(LDO0)</sub>    | Leakage current               | LDO off                                                                        |                       | 1       |     |      | μA   |
| T <sub>SSLD00</sub>       | Soft start ramp time          |                                                                                |                       | 500     |     |      | μs   |
| T <sub>SS_DELAYLDO0</sub> | Startup delay                 | Measured from the time when the enable bit is set                              |                       | 20      |     |      | μs   |
| LDO_PM LINEAR REGULATOR   |                               |                                                                                |                       |         |     |      |      |
| I <sub>Q(LD0_PM)</sub>    | Output current range          |                                                                                |                       | 20      |     |      | mA   |
| V <sub>O(LDO_PM)</sub>    | Output voltage                | Fixed output voltage value, V(OUT) > 4 V                                       |                       | 3.3     |     |      | V    |
|                           |                               | Dropout voltage, I(LDOPM) = −12 mA                                             |                       | 0.5 0.7 |     |      |      |
|                           |                               | Total accuracy                                                                 |                       | −5%     |     |      |      |
| I <sub>LKG(LDOPM)</sub>   | Leakage current               | LDO off                                                                        |                       | 1       |     |      | μA   |

## ELECTRICAL CHARACTERISTICS – SWITCHED MODE SM1 STEP DOWN CONVERTER

Over recommended operating conditions (typical values at  $T_J = 25^\circ\text{C}$ ),  $V_{O(\text{SM1})} = 1.24\text{ V}$ , application circuit as in [Figure 3](#) (unless otherwise noted).

| PARAMETER                 |                                | TEST CONDITIONS                                                                                                                          | MIN | TYP                                                                                           | MAX  | UNIT |
|---------------------------|--------------------------------|------------------------------------------------------------------------------------------------------------------------------------------|-----|-----------------------------------------------------------------------------------------------|------|------|
| I <sub>Q(SM1)</sub>       | Quiescent current for SM1      | I <sub>Q(SM1)</sub> = I(VIN_ SM1), no output load, not switching                                                                         |     | 10                                                                                            | 20   | μA   |
|                           |                                | SM1 OFF, set via I <sup>2</sup> C                                                                                                        |     | 0.1                                                                                           |      |      |
| I <sub>O(SM1)</sub>       | Output current range           |                                                                                                                                          |     |                                                                                               | 600  | mA   |
| V <sub>O(SM1)</sub>       | Output voltage, PWM mode       | Output voltage, selectable via I <sup>2</sup> C, standby OFF                                                                             |     | Available output voltages: V <sub>O(SM1)TYP</sub> = 0.6 V to 1.8 V, adjustable in 40-mV steps |      | V    |
|                           |                                | V <sub>O(SM1)</sub> = V <sub>SBY(SM1)</sub> , output voltage range, standby ON                                                           |     | Available output voltages: V <sub>SBY(SM1)</sub> = 0.6 V to 1.8 V, adjustable in 40-mV steps  |      |      |
|                           |                                | Total accuracy, V <sub>O(SM1)TYP</sub> = V <sub>SBY(SM1)</sub> = 1.24 V, V(VIN_ SM1) = 3 V to 4.7 V; 0 mA ≤ I <sub>O(SM1)</sub> ≤ 600 mA | −3% |                                                                                               | 3%   |      |
|                           |                                | Line regulation, V(VIN_ SM1): 3 → 4.7 V, I <sub>O(SM1)</sub> = 10 mA                                                                     |     | 0.027                                                                                         |      | %/V  |
|                           |                                | Load regulation, V(VIN_ SM1) = 4.7 V, I <sub>O(SM1)</sub> : 60 mA → 540 mA                                                               |     | 0.139                                                                                         |      | %/A  |
| R <sub>DS(ON)(PSM1)</sub> | P-channel MOSFET on-resistance | V(VIN_ SM1) = 3.6 V, 100% duty cycle set                                                                                                 |     | 310                                                                                           | 500  | mΩ   |
| I <sub>LKG(PSM1)</sub>    | P-channel leakage current      |                                                                                                                                          |     | 0.1                                                                                           |      | μA   |
| R <sub>DS(ON)(NSM1)</sub> | N-channel MOSFET on-resistance | V(VIN_ SM1) = 3.6 V, 0% duty cycle set                                                                                                   |     | 220                                                                                           | 330  | mΩ   |
| I <sub>LKG(NSM1)</sub>    | N-channel leakage current      |                                                                                                                                          |     | 5                                                                                             |      | μA   |
| I <sub>LIM(SM1)</sub>     | P- and N-channel current limit | 3 V < V(VIN_ SM1) < 4.7 V                                                                                                                | 900 | 1050                                                                                          | 1200 | mA   |
| f <sub>S(SM1)</sub>       | Oscillator frequency           | PWM mode set                                                                                                                             | 1.3 | 1.5                                                                                           | 1.7  | MHz  |
| EFF <sub>(SM1)</sub>      | Efficiency                     | V(VIN_ SM1) = 4.2 V, PWM mode, I <sub>O(SM1)</sub> = 300 mA, V <sub>O(SM1)</sub> = 3 V                                                   |     | 90%                                                                                           |      |      |
| t <sub>SS(SM1)</sub>      | Soft start ramp time           | Converter OFF→ON, V <sub>O(SM1)</sub> : 5% → 95% of target value                                                                         |     | 750                                                                                           |      | μs   |
| t <sub>DLY(SM1)</sub>     | Converter turn-on delay        | GPIO1 pin programmed as SM1 converter enable control. Measured from V(GPIO1): LO → HI                                                    |     | 170                                                                                           |      |      |

## ELECTRICAL CHARACTERISTICS – SWITCHED MODE SM2 STEP DOWN CONVERTER

Over recommended operating conditions (typical values at  $T_J = 25^\circ\text{C}$ ),  $V_{O(\text{SM}1)} = 1.24\text{ V}$ , application circuit as in [Figure 3](#) (unless otherwise noted).

| PARAMETER               |                                 | TEST CONDITIONS                                                                                                                                                                       | MIN                                                                                         | TYP   | MAX  | UNIT |
|-------------------------|---------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------|-------|------|------|
| I <sub>Q(SM2)</sub>     | Quiescent current for SM2       | I <sub>Q(SM2)</sub> = I(VIN_ SM2), no output load, not switching                                                                                                                      |                                                                                             | 10    | 20   | μA   |
|                         |                                 | SM2 OFF, set via I <sup>2</sup> C                                                                                                                                                     |                                                                                             | 0.1   |      |      |
| I <sub>O(SM2)</sub>     | Output current range            |                                                                                                                                                                                       |                                                                                             |       | 600  | mA   |
| V <sub>O(SM2)</sub>     | Output voltage                  | Output voltage, selectable via I <sup>2</sup> C, standby OFF                                                                                                                          | Available output voltages: V <sub>O(SM2)TYP</sub> = 1 V to 3.4 V, adjustable in 80 mV steps |       |      | V    |
|                         |                                 | V <sub>O(SM2)</sub> = V <sub>SBY(SM2)</sub> , output voltage range, standby ON                                                                                                        | Available output voltages: V <sub>SBY(SM2)</sub> = 1 V to 3.4 V, adjustable in 80-mV steps  |       |      |      |
|                         |                                 | Total accuracy, V <sub>O(SM2)TYP</sub> = V <sub>SM2(SBY)</sub> = 1.8 V, V(VIN_ SM2) = greater of [3 V or (V <sub>O(SM2)</sub> + 0.3 V)] to 4.7 V; 0 mA ≤ I <sub>O(SM2)</sub> ≤ 600 mA | -3%                                                                                         |       | 3%   |      |
|                         |                                 | Line regulation, V(VIN_ SM2) = greater of [3 V or (V <sub>O(SM2)</sub> + 0.3 V)] to 4.7 V; 0 mA ≤ I <sub>O(SM2)</sub> ≤ 600 mA                                                        |                                                                                             | 0.027 |      | %/V  |
|                         |                                 | Load regulation, V(VIN_ SM2) = 4.7 V, I <sub>O(SM2)</sub> : 60 mA → 540 mA                                                                                                            |                                                                                             | 0.139 |      | %/A  |
| R <sub>DSON(PSM2)</sub> | P-channel MOSFET on-resistance  | V(VIN_ SM2) = 3.6 V, 100% duty cycle set                                                                                                                                              |                                                                                             | 310   | 500  | mΩ   |
| I <sub>LKG(PSM2)</sub>  | P-channel leakage current       |                                                                                                                                                                                       |                                                                                             | 0.1   |      | μA   |
| R <sub>DSON(NSM2)</sub> | N-channel MOSFET on-resistance  | V(VIN_ SM2) = 3.6 V, 0% duty cycle set                                                                                                                                                |                                                                                             | 220   | 330  | mΩ   |
| I <sub>LKG(PSM2)</sub>  | N-channel leakage current       |                                                                                                                                                                                       |                                                                                             | 5     |      | μA   |
| I <sub>LIM(SM2)</sub>   | P- and N- channel current limit | 3 V < V(VIN_ SM2) < 4.7 V                                                                                                                                                             | 900                                                                                         | 1050  | 1200 | mA   |
| f <sub>S(SM2)</sub>     | Oscillator frequency            | PWM mode set                                                                                                                                                                          | 1.3                                                                                         | 1.5   | 1.7  | MHz  |
| EFF <sub>(SM2)</sub>    | Efficiency                      | V(VIN_ SM2) = 4.2 V, I <sub>O(SM2)</sub> = 300 mA, V <sub>O(SM2)</sub> = 3 V                                                                                                          |                                                                                             | 92%   |      |      |
| t <sub>SS(SM2)</sub>    | Soft start ramp time            | Converter OFF→ON, V <sub>O(SM2)</sub> : 5% → 95% of target value                                                                                                                      |                                                                                             | 750   |      | μs   |
| t <sub>DLY(SM2)</sub>   | Converter turn-on delay         | GPIO2 pin programmed as SM2 converter enable control. Measured from V(GPIO2): LO → HI                                                                                                 |                                                                                             | 170   |      |      |

## ELECTRICAL CHARACTERISTICS – GPIOs

Over recommended operating conditions (typical values at  $T_J = 25^\circ\text{C}$ ), application circuit as in [Figure 3](#) (unless otherwise noted).

| PARAMETER                     |                                         | TEST CONDITIONS                   | MIN | TYP | MAX | UNIT          |
|-------------------------------|-----------------------------------------|-----------------------------------|-----|-----|-----|---------------|
| <b>GPIO1–3</b>                |                                         |                                   |     |     |     |               |
| $V_{\text{OL}}$               | Low level output voltage GPIO0          | $I_{\text{OL}} = 20\text{ mA}$    |     |     | 0.5 | V             |
| $I_{\text{OGPIO}}$            | Low level sink current into GPIO1, 2, 3 | $V(\text{GPIO}n) = V(\text{OUT})$ | 20  |     |     | mA            |
| $V_{\text{IL}}$               | Low level input voltage                 |                                   |     |     | 0.4 | V             |
| $I_{\text{LKG}(\text{GPIO})}$ | Input leakage current                   | $V(\text{GPIO}n) = V(\text{OUT})$ |     | 1   |     | $\mu\text{A}$ |

## ELECTRICAL CHARACTERISTICS – ADC

Over recommended operating conditions (typical values at  $T_J = 25^\circ\text{C}$ ),  $V(\text{ADC\_REF}) = 2.535\text{V}$  if external reference voltage is used, application circuit as in [Figure 3](#) (unless otherwise noted).

| PARAMETER                  |                                                       | TEST CONDITIONS                                                                                                     |    | MIN       | TYP                         | MAX  | UNIT   |
|----------------------------|-------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------|----|-----------|-----------------------------|------|--------|
| ANALOG INPUTS              |                                                       |                                                                                                                     |    |           |                             |      |        |
| V <sub>RNG(CH1_5)</sub>    | Full-scale input range, Ch1 to Ch5                    | Positive inputs (active clamp), full scale ~ 2.535 V                                                                |    | 0         | V(ADC_REF)                  |      | V      |
| V <sub>RNG(CH6_8)</sub>    | Full-scale input range, Ch6 to Ch8                    | Positive inputs (active clamp), full scale ~4.7 V                                                                   |    | 0         | V <sub>INTREF</sub> × 1.854 |      |        |
| C <sub>IN(ADC)</sub>       | Input capacitance (all channels)                      |                                                                                                                     |    | 15        |                             |      | pF     |
| R <sub>INADC(CH1_5)</sub>  | Input resistance                                      | (Ch1 to Ch5)                                                                                                        |    | 1         |                             |      | MΩ     |
| I <sub>LKGADC(CH1_5)</sub> | Leakage current                                       | (Ch1 to Ch5)                                                                                                        |    |           |                             | 100  | nA     |
| R <sub>INADC(CH6_8)</sub>  | Input resistance                                      | (Ch6 to Ch8)                                                                                                        |    | 430       | 540                         |      | kΩ     |
| I <sub>LKGADC(CH6_8)</sub> | Leakage current                                       | (Ch6 to Ch8)                                                                                                        |    |           |                             | 10   | μA     |
| V <sub>CH5(ADC)</sub>      | Internal voltage proportional to junction temperature | T <sub>J</sub> = 25°C, ADC channel 5 input voltage                                                                  |    | 1.89<br>5 |                             |      | V      |
|                            |                                                       | Temperature coefficient                                                                                             |    | 6.5       |                             |      | mV/°C  |
| DC ACCURACY                |                                                       |                                                                                                                     |    |           |                             |      |        |
| RES <sub>(ADC)</sub>       | Resolution                                            | SAR ADC                                                                                                             |    | 10        |                             |      | Bits   |
| MCD <sub>(ADC)</sub>       | No missing codes                                      |                                                                                                                     |    | SPECIFIED |                             |      |        |
| INL <sub>(ADC)</sub>       | Integral linearity error                              |                                                                                                                     |    | ±3        |                             |      | LSB    |
| DNL <sub>(ADC)</sub>       | Differential non-linearity error                      |                                                                                                                     |    | ±1        |                             |      | LSB    |
| OFF <sub>ZERO(ADC)</sub>   | Offset error                                          | Difference between the first code transition (00...00 to 00...001) and the ideal AGND + 1 LSB                       |    |           |                             | 5    | LSB    |
| OFF <sub>CH(ADC)</sub>     | Offset error match between channels                   |                                                                                                                     |    |           |                             | 5    | LSB    |
| GAIN <sub>ADC</sub>        | Gain error                                            | Deviation in code from the ideal full scale code (11...111) for the full scale voltage                              |    | ±8        |                             |      | LSB    |
| GAIN <sub>CH(ADC)</sub>    | Gain error match                                      | Any two channels                                                                                                    |    | 2         |                             |      | LSB    |
| THROUGHPUT SPEED           |                                                       |                                                                                                                     |    |           |                             |      |        |
| ADC <sub>CLK</sub>         | Sampling clock                                        |                                                                                                                     |    | 650       | 750                         | 850  | kHz    |
| ADC <sub>TCONV</sub>       | Conversion time                                       | Sampling, conversion and setting R <sub>s</sub> ≤ 200 K for Ch1, Ch2, Ch3; R <sub>s</sub> ≤ 500 Ω for Ch6, Ch7, Ch8 |    | 44        | 59                          | 68   | μs     |
| REFERENCE VOLTAGES         |                                                       |                                                                                                                     |    |           |                             |      |        |
| V <sub>INTREF</sub>        | Internal ADC reference voltage                        | T <sub>A</sub> = 25°C, V(ADC_REF)=V <sub>INTREF</sub> when internal ADC reference is selected                       |    | 2.53      | 2.53<br>5                   | 2.54 | V      |
| I <sub>SHRT(INTREF)</sub>  | Internal reference short circuit limit                | V(ADC_REF)= AGND1, internal reference enabled via I <sup>2</sup> C                                                  |    | 6         |                             |      | mA     |
| V <sub>REF(DRIFT)</sub>    | ADC internal reference temperature drift              |                                                                                                                     |    | 50        |                             | 100  | ppm/°C |
| I <sub>Q(ADC)</sub>        | ADC Internal reference quiescent current              | Measured at OUT pin (internal reference) or ADC_REF pin (external reference)                                        |    | 40        |                             |      | μA     |
| I <sub>(ANLG2)</sub>       | ANLG2 pin internal pullup current source              | ADC channel 2 bias current, set via I <sup>2</sup> C register ADC_WAIT bits (ADC_CH2I_D1_1, ADC_CH2I_D2)            | 00 | 0         |                             | μA   |        |
|                            |                                                       |                                                                                                                     | 01 | 10        |                             |      |        |
|                            |                                                       |                                                                                                                     | 10 | 50        |                             |      |        |
|                            |                                                       |                                                                                                                     | 11 | 60        |                             |      |        |
|                            |                                                       | Total accuracy, relative to selected value                                                                          |    |           |                             | -25% | 25%    |

**ELECTRICAL CHARACTERISTICS – ADC (continued)**

Over recommended operating conditions (typical values at  $T_J = 25^\circ\text{C}$ ),  $V(\text{ADC\_REF}) = 2.535\text{V}$  if external reference voltage is used, application circuit as in [Figure 3](#) (unless otherwise noted).

| PARAMETER                            |                                          | TEST CONDITIONS                                                                                    |    | MIN                                               | TYP | MAX   | UNIT |
|--------------------------------------|------------------------------------------|----------------------------------------------------------------------------------------------------|----|---------------------------------------------------|-----|-------|------|
| I <sub>(ANLG1)</sub>                 | ANLG1 pin internal pullup current source | ADC channel 1 bias current, set via I <sup>2</sup> C register ADC_WAIT bits (BATIDI_D1, BATIDI_D2) | 00 | $\frac{V(\text{OUT}) - 1.2}{500 \text{ k}\Omega}$ |     |       | μA   |
|                                      |                                          |                                                                                                    | 01 | 10                                                |     |       |      |
|                                      |                                          |                                                                                                    | 10 | 50                                                |     |       |      |
|                                      |                                          |                                                                                                    | 11 | 60                                                |     |       |      |
|                                      |                                          | Total accuracy                                                                                     |    |                                                   | 10% |       | 10%  |
| INTERNAL REFERENCE POWER CONSUMPTION |                                          |                                                                                                    |    |                                                   |     |       |      |
| PD <sub>ACTIVE</sub>                 | Power dissipation                        | Conversion active                                                                                  |    | 2.3                                               |     |       | mW   |
| PD <sub>ARMED</sub>                  | Power dissipation                        | Not converting                                                                                     |    | 0.43                                              |     |       | mW   |
| TRIGGER TIMING CHARACTERISTICS       |                                          |                                                                                                    |    |                                                   |     |       |      |
| t <sub>DELAY(TRG)</sub>              | Trigger delay time accuracy              | Time range, set via I <sup>2</sup> C register ADC_DELAY                                            |    | 0                                                 |     | 750   | μS   |
|                                      |                                          | Relative to typical value set via I <sup>2</sup> C                                                 |    | −20%                                              |     | 20%   |      |
| t <sub>WAIT(TRG)</sub>               | Trigger wait time accuracy               | Time range, set via I <sup>2</sup> C register ADC_WAIT                                             |    | 0                                                 |     | 20.48 | mS   |
|                                      |                                          | Relative to typical value set via I <sup>2</sup> C                                                 |    | −20%                                              |     | 20%   |      |

**ELECTRICAL CHARACTERISTICS – LED AND PWM DRIVERS**

Over recommended operating conditions (typical values at  $T_J = 25^\circ\text{C}$ ), application circuit as in [Figure 3](#) (unless otherwise noted)

| PARAMETER                                                           | TEST CONDITIONS                                                                                                | MIN                                                                                      | TYP | MAX | UNIT          |
|---------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------|-----|-----|---------------|
| <b>SM3 BOOST CONVERTER, WHITE LED CONSTANT-CURRENT DRIVER</b>       |                                                                                                                |                                                                                          |     |     |               |
| $V_{\text{VIN(SM3)}}$ Input Voltage range                           | $V(\text{OUT}) = 3.3 \text{ V}$                                                                                | 3                                                                                        |     | 4.7 | V             |
| $V_{\text{OVP3}}$ Output overvoltage trip                           | OVP detected at $V(\text{SM3}) > V_{\text{OVP3}}$                                                              | 26.5                                                                                     | 29  | 30  | V             |
| $V_{\text{HYS(OVP3)}}$ Output overvoltage hysteresis                | OVP not detected at $V(\text{SM3}) < V_{\text{OVP3}} - V_{\text{HYS(OVP3)}}$                                   | 1.8                                                                                      |     |     | V             |
| $V_{\text{SM3REF}}$ LED current sense threshold                     | LED current below regulation point at $V(\text{FB3}) < V_{\text{SM3REF}}$                                      | 244                                                                                      | 252 | 260 | mV            |
| $I_{\text{O(SM3)}}$ LED current                                     | Current range, $V_{\text{in}} = 3.3 \text{ V}$ , $I_{\text{O(SM3)}} = \frac{V(\text{SM3REF})}{R_{\text{FB3}}}$ | 0.5                                                                                      |     | 25  | mA            |
|                                                                     | Total accuracy, $I_{\text{O(SM3)}} = 10\text{mA}$                                                              | –10% 10%                                                                                 |     |     |               |
| $D_{\text{SM3SW}}$ LED switch duty cycle                            | Duty cycle range                                                                                               | $D_{\text{SM3SW}} = 0\%$ to 99.6%, set via I <sup>2</sup> C, 256 steps 0.4% minimum step |     |     | --            |
| $f_{\text{REP\_SM3}}$ LED switch duty cycle pattern repetition rate | 256 pulses within repetition rate time                                                                         | SM3_LF_OSC = 0                                                                           |     | 122 | Hz            |
|                                                                     |                                                                                                                | SM3_LF_OSC = 1                                                                           |     | 183 |               |
| $R_{\text{DS(on)(SM3SW)}}$ LED switch MOSFET on-resistance          | $V(\text{OUT}) = 3.6 \text{ V}$ ; $I(\text{SM3SW}) = 20 \text{ mA}$                                            |                                                                                          | 1   | 2   | $\Omega$      |
| $I_{\text{LKG(SM3SW)}}$ LED switch MOSFET leakage                   |                                                                                                                |                                                                                          | 1   |     | $\mu\text{A}$ |
| $R_{\text{DS(on)(L3)}}$ Power stage MOSFET on-resistance            | $V(\text{OUT}) = 3.6 \text{ V}$ ; $I(\text{L3}) = 200 \text{ mA}$                                              |                                                                                          | 300 | 600 | m $\Omega$    |
| $I_{\text{LKG(L3)}}$ Power stage MOSFET leakage                     |                                                                                                                |                                                                                          | 1   |     | $\mu\text{A}$ |
| $I_{\text{MAX(L3)}}$ Power stage MOSFET current limit               | $3 \text{ V} < V(\text{OUT}) < 4.7 \text{ V}$                                                                  | 400                                                                                      | 500 | 600 | mA            |
| <b>PWM DRIVER, PWM OPEN DRAIN OUTPUT</b>                            |                                                                                                                |                                                                                          |     |     |               |
| $V_{\text{OL(PWM)}}$ Low level output voltage                       | $I(\text{PWM}) = 150 \text{ mA}$                                                                               |                                                                                          |     | 0.5 | V             |
| $f_{\text{PWM}}$ PWM driver frequency                               | Frequency range                                                                                                | Set via I <sup>2</sup> C, $f_{\text{PWM}} = 0.5/1/1.5/2/3/4.5/7.8/15.6$                  |     |     | Hz            |
|                                                                     | Total accuracy, relative to selected value                                                                     | – 20% 20%                                                                                |     |     |               |
| $t_{\text{RISE\_PWM}}$ Rise time PWM voltage                        | $I_{\text{OL\_PWM}} = 150 \text{ mA}$                                                                          | 0.2                                                                                      | 1   | 2.8 | $\mu\text{s}$ |

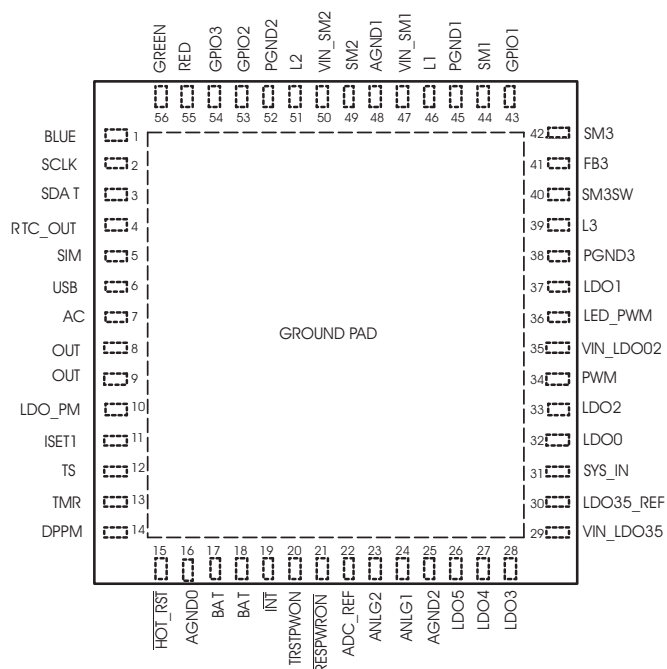


## ELECTRICAL CHARACTERISTICS – LED AND PWM DRIVERS (continued)

Over recommended operating conditions (typical values at  $T_J = 25^\circ\text{C}$ ), application circuit as in [Figure 3](#) (unless otherwise noted)

| PARAMETER                                     |                                                   | TEST CONDITIONS                                                         |                          | MIN                                                                                       | TYP | MAX  | UNIT |
|-----------------------------------------------|---------------------------------------------------|-------------------------------------------------------------------------|--------------------------|-------------------------------------------------------------------------------------------|-----|------|------|
| t <sub>FALL_PWM</sub>                         | Fall time PWM voltage                             | I <sub>OL_PWM</sub> = 150 mA                                            |                          | 0.2                                                                                       | 1   | 2.8  | μs   |
| D <sub>PWM</sub>                              | PWM driver duty cycle                             | Duty cycle range                                                        |                          | D <sub>PWM</sub> = 6.25% to 100%, set via I <sup>2</sup> C, 6.25% minimum step            |     |      | --   |
| LED_PWM DRIVER, LED_PWM OPEN DRAIN OUTPUT     |                                                   |                                                                         |                          |                                                                                           |     |      |      |
| D <sub>LEDPWM</sub>                           | LED_PWM driver duty cycle                         | Duty cycle range                                                        |                          | D <sub>LEDPWM</sub> = 0% to 99.6%, set via I <sup>2</sup> C, 256 steps 0.4% minimum step  |     |      |      |
| f <sub>REP(LEDPWM)</sub>                      | LED_PWM driver duty cycle pattern repetition rate | 256 pulses within repetition rate time                                  | SM3_LF_OSC = 0           | 122                                                                                       |     |      | Hz   |
|                                               |                                                   |                                                                         | SM3_LF_OSC = 1           | 180                                                                                       |     |      |      |
| V <sub>OL(LEDPWM)</sub>                       | Low level output voltage                          | I(LED_PWM) = 150 mA                                                     |                          | 0.5                                                                                       |     |      | V    |
| V <sub>OH(LEDPWM)</sub>                       | High level output voltage                         |                                                                         |                          | 6                                                                                         |     |      | V    |
| t <sub>RISE_LEDPWM</sub>                      | Rise time PWM voltage                             | I <sub>OL_LEDPWM</sub> = 150 mA                                         |                          | 0.2                                                                                       | 1   | 2.8  | μs   |
| t <sub>FALL_LEDPWM</sub>                      | Fall time PWM voltage                             | I <sub>OL_LEDPWM</sub> = 150 mA                                         |                          | 0.2                                                                                       | 1   | 2.8  | μs   |
| RGB DRIVER, RED/GREEN/BLUE OPEN DRAIN OUTPUTS |                                                   |                                                                         |                          |                                                                                           |     |      |      |
| t <sub>FLASH(RGB)</sub>                       | Flashing period                                   | Flashing period range                                                   |                          | t <sub>FLASH(RGB)</sub> = 1 to 8 s, set via I <sup>2</sup> C, 0.5 s minimum step, 8 steps |     |      | s    |
|                                               |                                                   | Total accuracy                                                          |                          | –20% 20%                                                                                  |     |      |      |
| t <sub>FLASH(ON)</sub>                        | Flash on time                                     | Flash on time range, value selectable by I <sup>2</sup> C               |                          | Set via I <sup>2</sup> C, t <sub>FLASH(ON)</sub> = 0.1/0.15/0.2/0.25/0.3/0.4/0.5/0.6 s    |     |      | s    |
|                                               |                                                   | Total accuracy, relative to selected value                              |                          | – 20% 20%                                                                                 |     |      |      |
| D <sub>RGB</sub>                              | Duty cycle                                        | Duty cycle range, value selectable via I <sup>2</sup> C                 |                          | D <sub>RGB</sub> = 0% to 99.98%, set via I <sup>2</sup> C, 3.23% minimum step             |     |      |      |
| I <sub>SINK(RGB)</sub>                        | RGB output sink current                           | V(RED) = V(GREEN) = V(BLUE) = 2 V, set via I <sup>2</sup> C RGB_ISET1,0 | 00 = (Driver set to OFF) |                                                                                           |     |      | mA   |
|                                               |                                                   |                                                                         | 01                       | 2.4                                                                                       | 4   | 5.6  |      |
|                                               |                                                   |                                                                         | 10                       | 4.8                                                                                       | 8   | 11.2 |      |
|                                               |                                                   |                                                                         | 11                       | 7                                                                                         | 12  | 16.6 |      |
| V <sub>OL(RGB)</sub>                          | Low level output voltage                          | Output low voltage, 8 mA load, RED/GREEN/BLUE PINS                      |                          | 0.3                                                                                       |     |      | V    |
| I <sub>LKG(RGB)</sub>                         | Output off leakage current                        | V(RED)=V(GREEN)=V(BLUE) = 4.7 V, all drivers disabled                   |                          | 1                                                                                         |     |      | μA   |
| t <sub>RISE_RGB</sub>                         | Voltage rise time                                 | 8-mA load                                                               |                          | 2                                                                                         | 5   | 8    | μs   |
| t <sub>FALL_RGB</sub>                         | Voltage fall time                                 | 8-mA load                                                               |                          | 2.4                                                                                       | 5   | 8    | μs   |

## PIN ASSIGNMENT



## PIN DESCRIPTION, REQUIRED EXTERNAL COMPONENTS

| NAME    | PIN    | I/O | DESCRIPTION                                                                                  | EXTERNAL REQUIRED COMPONENTS<br>(SEE APPLICATION DIAGRAM)                                                                                                                                                             |
|---------|--------|-----|----------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| AC      | 7      | I   | Adapter charge input voltage, connect to AC_DC adapter positive output terminal (dc voltage) | 1- $\mu$ F (minimum) capacitor to AGND1 pin to minimize overvoltage transients during AC power hot-plug events.                                                                                                       |
| ADC_REF | 22     | I/O | ADC internal reference filter or ADC external reference input                                | 4.7- $\mu$ F (minimum) to 10- $\mu$ F (maximum) capacitor connected to AGND2 pin                                                                                                                                      |
| AGND0   | 16     | –   | Analog ground connection                                                                     | Connect to analog ground plane                                                                                                                                                                                        |
| AGND1   | 48     | –   | Analog ground pin                                                                            | Connect to analog ground plane                                                                                                                                                                                        |
| AGND2   | 25     | –   | Analog ground pin                                                                            | Connect to analog ground plane                                                                                                                                                                                        |
| ANLG1   | 24     | I   | Analog input to ADC, programmable current source output                                      | Can be used to monitor additional system or pack parameters                                                                                                                                                           |
| ANLG2   | 23     | I   | Analog input to ADC, programmable current source output                                      | Can be used to monitor additional system or pack parameters                                                                                                                                                           |
| BAT     | 17, 18 | I/O | Battery power                                                                                | Connect to battery positive terminal. Connect 10- $\mu$ F capacitor (minimum) from BAT pin to AGND1 pin.                                                                                                              |
| BLUE    | 1      | O   | Programmable blue driver, open-drain output, current sink output when active.                | Connect to BLUE input of RGB LED                                                                                                                                                                                      |
| DPPM    | 14     | I   | Dynamic power path management set-point                                                      | External resistor from DPPM pin to AGND1 pin sets the DPPM regulation threshold. 1-nF (minimum) capacitor to from DPPM to AGND1 sets BAT to OUT short-circuit blanking delay when battery is hot-plugged into system. |
| FB3     | 41     | I/O | White LED duty cycle switch output, LED current setting                                      | External resistor from FB3 pin to PGND3 pin sets LED peak current. Connect 100-pF (minimum) filter capacitor to PGND3 pin.                                                                                            |
| GPIO1   | 43     | I/O | General purpose programmable I/O                                                             | Example: External Interrupt request to host ( $\overline{\text{INT}}\text{:HI}\rightarrow\text{LO}$ )                                                                                                                 |
| GPIO2   | 53     | I/O | General purpose programmable I/O                                                             | I/O Example: Set SM1 and SM2 converters in standby mode                                                                                                                                                               |
| GPIO3   | 54     | I/O | General purpose programmable I/O                                                             | Example: ADC conversion start trigger                                                                                                                                                                                 |
| GREEN   | 56     | O   | Programmable LED driver, open drain output, current sink output when active.                 | Connect to GREEN input of RGB LED                                                                                                                                                                                     |

**PIN ASSIGNMENT (continued)**

| NAME                         | PIN  | I/O | DESCRIPTION                                                                                                                    | EXTERNAL REQUIRED COMPONENTS<br>(SEE APPLICATION DIAGRAM)                                                                                                                                                   |
|------------------------------|------|-----|--------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| HOT_RST                      | 15   | I/O | Hardware reset input, reset generated when connected to ground                                                                 | Connect to an external push-button switch                                                                                                                                                                   |
| $\overline{\text{INT}}$      | 19   | O   | Interruption pin, open-drain output                                                                                            | Connect 100-k $\Omega$ external pullup resistor between $\overline{\text{INT}}$ and OUT. $\overline{\text{INT}}$ pin is LO when interrupt is requested by TPS65800.                                         |
| ISSET1                       | 11   | I   | Current set point when charging in auto mode with AC selected. Precharge and charge termination set point for all charge modes | External resistor from ISET1 pin to AGND1 pin sets charge current value                                                                                                                                     |
| L1                           | 46   | O   | SM1 synchronous buck converter power stage output                                                                              | 3.3- $\mu$ H inductor to SM1 pin                                                                                                                                                                            |
| L2                           | 51   | O   | SM2 synchronous buck converter power stage output                                                                              | 3.3- $\mu$ H inductor to SM2 pin                                                                                                                                                                            |
| L3                           | 39   | O   | Drain of the integrated boost power stage switch                                                                               | 4.7- $\mu$ H inductor to OUT pin, external Schottky diode to SM3 pin                                                                                                                                        |
| LDO0                         | 32   | O   | LDO0 output, fixed voltage                                                                                                     | 1- $\mu$ F (minimum) capacitor to AGND1                                                                                                                                                                     |
| LDO1                         | 37   | O   | LDO1 output                                                                                                                    | 1- $\mu$ F (minimum) capacitor to AGND1                                                                                                                                                                     |
| LDO2                         | 33   | O   | LDO2 output                                                                                                                    | 1- $\mu$ F (minimum) capacitor to AGND1                                                                                                                                                                     |
| LDO3                         | 28   | O   | LDO3 output                                                                                                                    | 2.2- $\mu$ F (minimum) capacitor to AGND2                                                                                                                                                                   |
| LDO4                         | 27   | O   | LDO4 output                                                                                                                    | 2.2- $\mu$ F (minimum) capacitor to AGND2                                                                                                                                                                   |
| LDO35_REF                    | 30   | I   | Linear regulators LDO3–5 reference filter                                                                                      | 100-nF capacitor to AGND2                                                                                                                                                                                   |
| LDO5                         | 26   | O   | LDO5 output                                                                                                                    | 2.2- $\mu$ F (minimum) capacitor to AGND2                                                                                                                                                                   |
| LDO_PM                       | 10   | O   | General-purpose LDO output                                                                                                     | 1- $\mu$ F (minimum) capacitor to AGND1 pin                                                                                                                                                                 |
| LED_PWM                      | 36   | O   | PWM driver output, open-drain                                                                                                  | Can be used to drive a keyboard backlight LED                                                                                                                                                               |
| OUT                          | 8, 9 | O   | Power path output. Connect to system main power rail (system power bus)                                                        | 10- $\mu$ F capacitor to AGND1 pin                                                                                                                                                                          |
| PGND1                        | 45   | –   | SM1 synchronous buck converter power ground                                                                                    | Connect to power ground plane                                                                                                                                                                               |
| PGND2                        | 52   | –   | SM1 synchronous buck converter power ground                                                                                    | Connect to power ground plane                                                                                                                                                                               |
| PGND3                        | 38   | –   | White LED driver power ground input.                                                                                           | Connect to a power ground plane                                                                                                                                                                             |
| PWM                          | 34   | O   | PWM driver output, open-drain                                                                                                  | Can be used to drive a vibrator or other external functions                                                                                                                                                 |
| RED                          | 55   | O   | Programmable LED driver, open drain output, current sink output when active.                                                   | Connect to RED input of RGB LED                                                                                                                                                                             |
| $\overline{\text{RESPWRON}}$ | 21   | O   | System reset, open-drain output                                                                                                | 100-k $\Omega$ external pullup resistor to OUT. $\overline{\text{RESPWRON}}$ pin is LO when TPS65800 is resetting the system.                                                                               |
| RTC_OUT                      | 4    | O   | Low-leakage LDO output. Can be connected to a super-capacitor or secondary cell, if used as a RTC backup output.               | 1- $\mu$ F (minimum) capacitor to AGND1 pin or supercapacitor                                                                                                                                               |
| SCLK                         | 2    | I   | I <sup>2</sup> C interface clock line                                                                                          | 2-k $\Omega$ pullup resistor to OUT pin                                                                                                                                                                     |
| SDAT                         | 3    | I/O | I <sup>2</sup> C interface data line                                                                                           | 2-k $\Omega$ pullup resistor to OUT pin                                                                                                                                                                     |
| SIM                          | 5    | O   | General-purpose LDO output                                                                                                     | 1- $\mu$ F (minimum) capacitor to AGND1 pin                                                                                                                                                                 |
| SM1                          | 44   | I   | SM1 synchronous buck converter output voltage sense                                                                            | LC filter: 10- $\mu$ F capacitor to PGND1 pin                                                                                                                                                               |
| SM2                          | 49   | I   | SM2 synchronous buck converter output voltage sense                                                                            | LC filter: 10- $\mu$ F capacitor to PGND2 pin                                                                                                                                                               |
| SM3                          | 42   | I   | White LED driver output overvoltage detection                                                                                  | Connect 1- $\mu$ F capacitor to PGND3 pin. Connect SM3 pin to the positive side of white LED ladder.                                                                                                        |
| SM3SW                        | 40   | I   | Integrated white LED duty cycle switch input                                                                                   | Connect to negative side of external LED ladder                                                                                                                                                             |
| SYS_IN                       | 31   | I   | System power bus low-voltage detection                                                                                         | External resistive divider sets minimum system operational voltage. TPS65800 enters sleep mode when voltage below minimum system voltage threshold is detected. 1 nF filter capacitor to AGND1 recommended. |

**PIN ASSIGNMENT (continued)**

| NAME                | PIN | I/O | DESCRIPTION                                                                                                                                                                                                                                                                                                                                               | EXTERNAL REQUIRED COMPONENTS<br>(SEE APPLICATION DIAGRAM)                                                           |
|---------------------|-----|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------|
| TMR                 | 13  | I   | Charge safety timer program input                                                                                                                                                                                                                                                                                                                         | External resistor from TMR pin to AGND1 pin sets the charge safety timer time-out value.                            |
| TRSTPWON            | 20  | I   | System reset pulse duration setting                                                                                                                                                                                                                                                                                                                       | 100-nF (minimum) capacitor to AGND1. External capacitor from TRSTPWON pin to AGND1 pin sets RESPWRON pulse duration |
| TS                  | 12  | I/O | Temperature sense input, current source output                                                                                                                                                                                                                                                                                                            | Connect to battery pack thermistor to sense battery pack temperature                                                |
| USB                 | 6   | I   | USB charge input voltage, connect to USB port positive power output                                                                                                                                                                                                                                                                                       | 1- $\mu$ F (minimum) capacitor to AGND1 pin, to minimize overvoltage transients during USB power hot-plug events.   |
| VIN_LDO35           | 29  | –   | Input to LDOs 3 to 5                                                                                                                                                                                                                                                                                                                                      | 1- $\mu$ F (minimum) decoupling capacitor to AGND2                                                                  |
| VIN_LDO02           | 35  | –   | Positive supply input for LDO0, LDO1, LDO2                                                                                                                                                                                                                                                                                                                | 1- $\mu$ F (minimum) decoupling capacitor to AGND1                                                                  |
| VIN_SM1             | 47  | –   | SM1 synchronous buck converter positive supply input                                                                                                                                                                                                                                                                                                      | 10- $\mu$ F capacitor to PGND1 pin                                                                                  |
| VIN_SM2             | 50  | –   | SM2 synchronous buck converter positive supply input                                                                                                                                                                                                                                                                                                      | 10- $\mu$ F capacitor to PGND2 pin                                                                                  |
| Exposed thermal pad | 57  | –   | There is an internal electrical connection between the exposed thermal pad and AGNDn pins of the IC. The exposed thermal pad must be connected to the same potential as the AGND1 pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the IC. AGNDn pins must be connected to a clean ground plane at all times. |                                                                                                                     |

## APPLICATION DIAGRAM

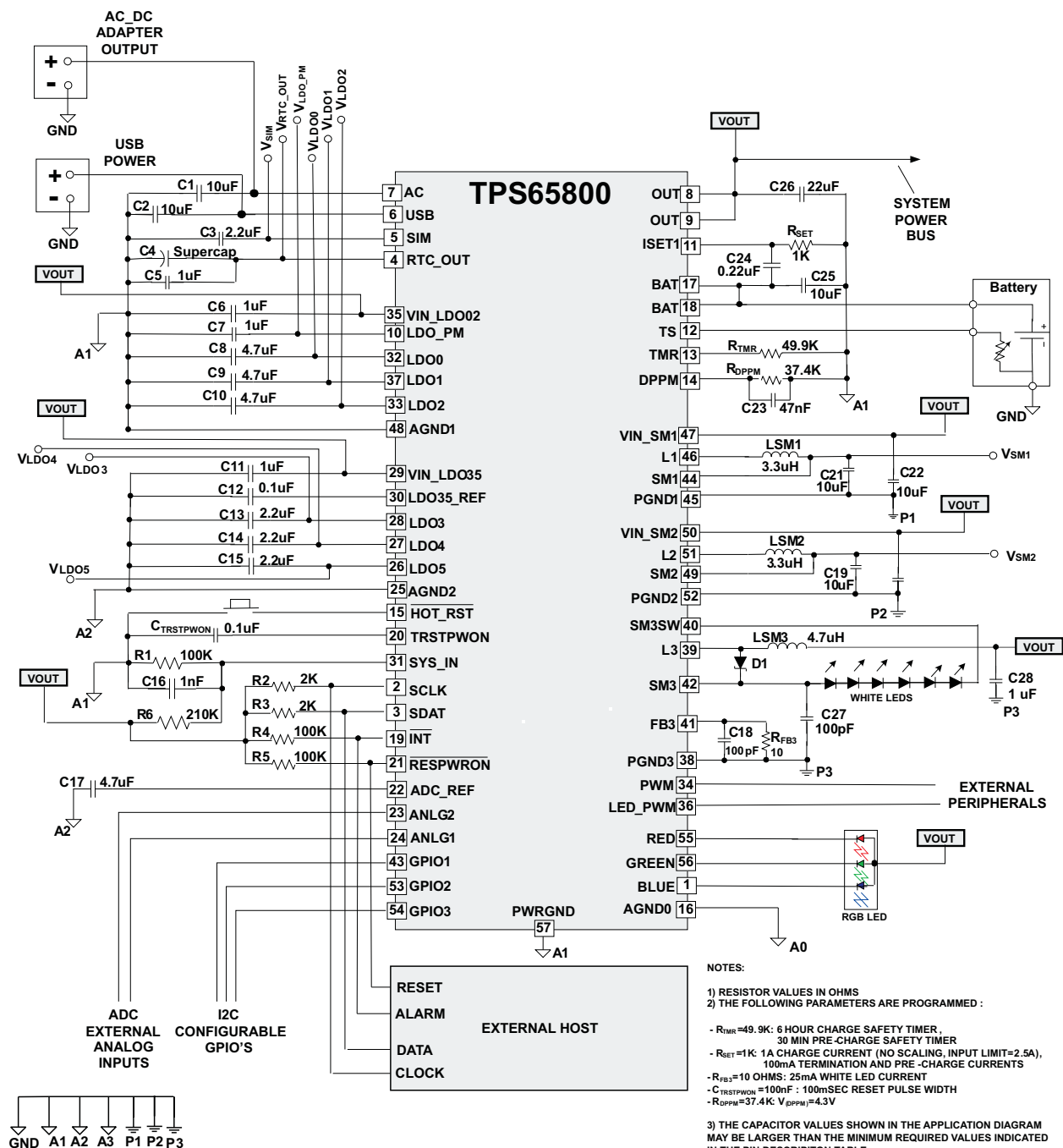


Figure 3. TPS65800 Application Diagram, Recommended External Components

## TYPICAL CHARACTERISTICS – POWER PATH MANAGEMENT

Measured with application circuit shown in [Figure 3](#), unless otherwise noted

**SWITCHING FROM AC TO BATTERY  
ON AC REMOVAL**

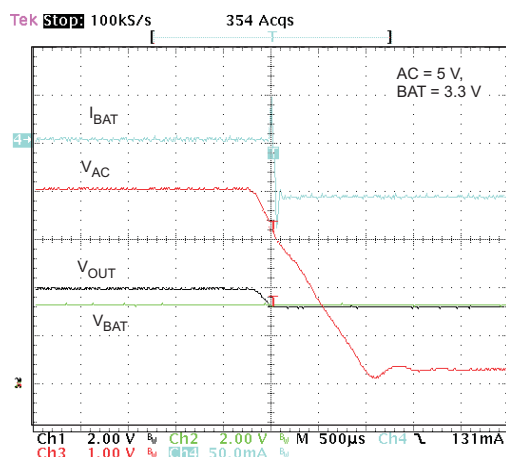


Figure 4.

**SWITCHING FROM USB TO BATTERY  
ON AC REMOVAL**

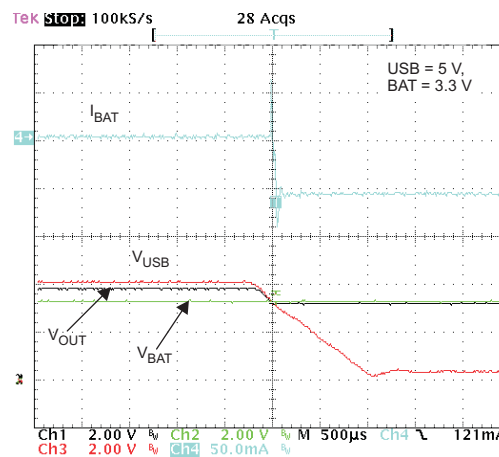


Figure 5.

## TYPICAL CHARACTERISTICS – LINEAR REGULATORS 0, 1, 2

Measured with application circuit shown in [Figure 3](#), unless otherwise noted

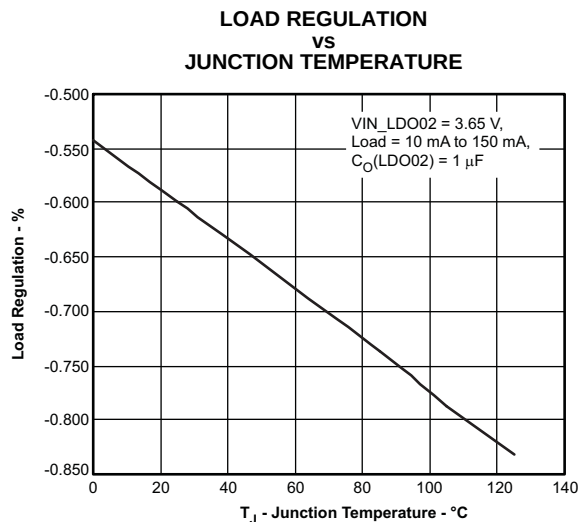


Figure 6.

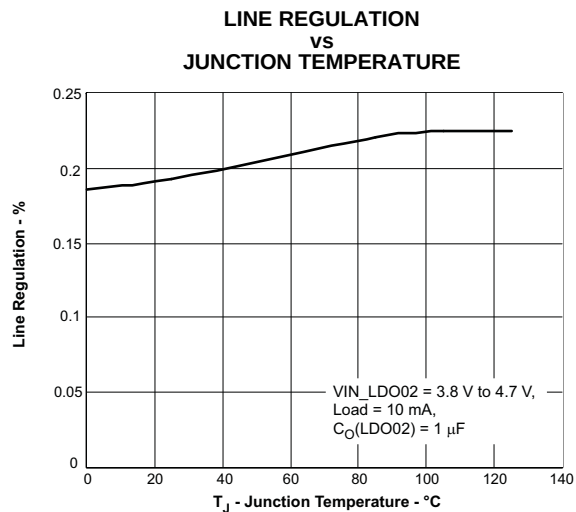


Figure 7.

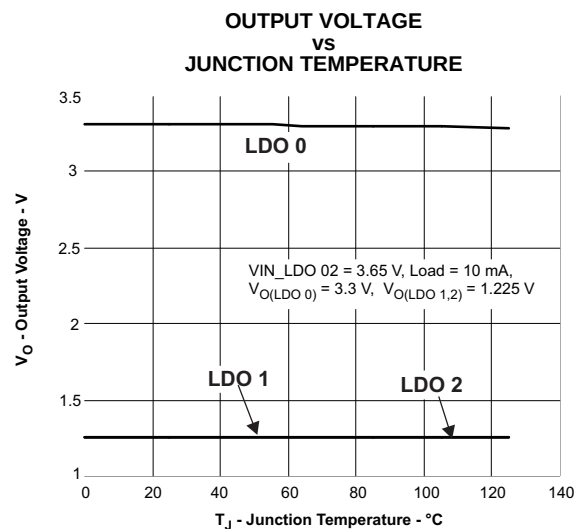


Figure 8.

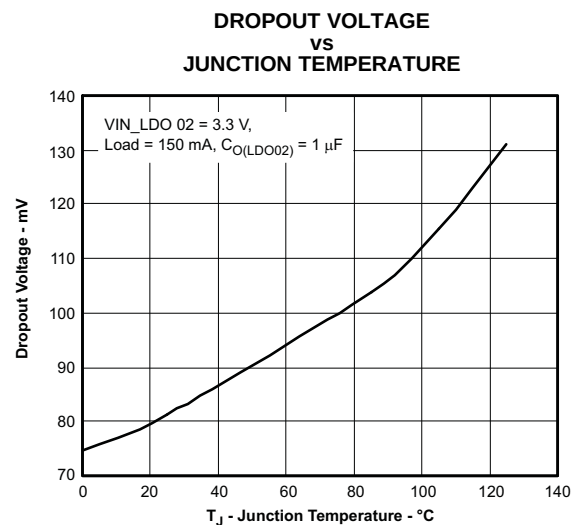


Figure 9.

## TYPICAL CHARACTERISTICS – LINEAR REGULATORS 3, 4, 5

Measured with application circuit shown in [Figure 3](#), unless otherwise noted

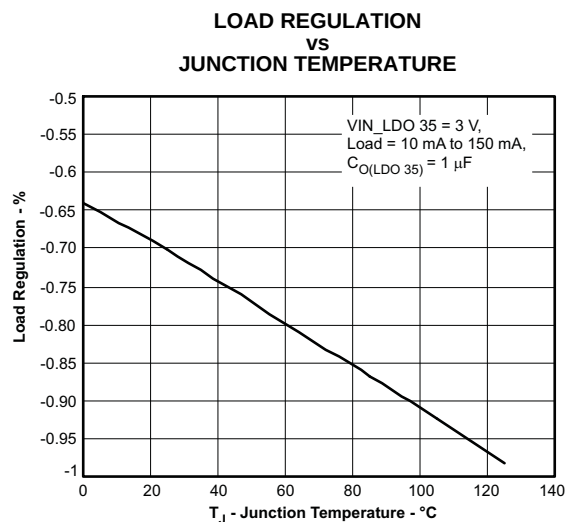


Figure 10.

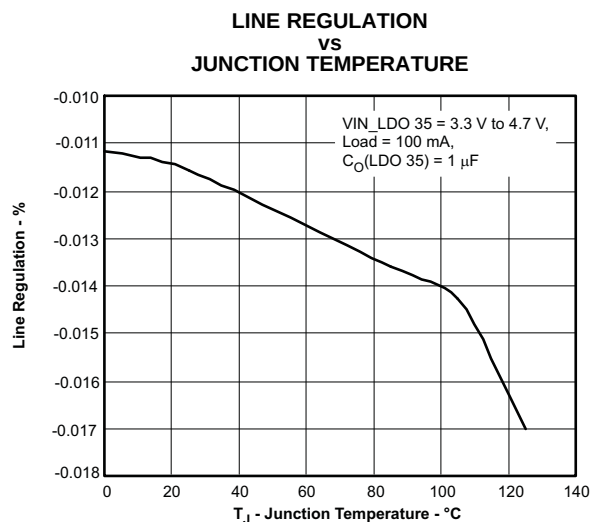


Figure 11.

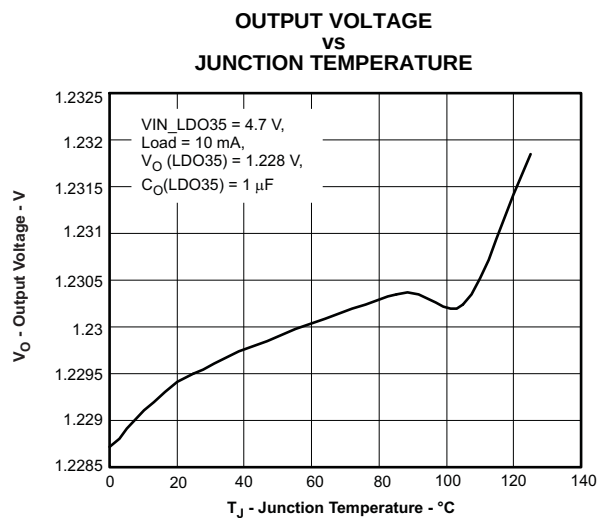


Figure 12.

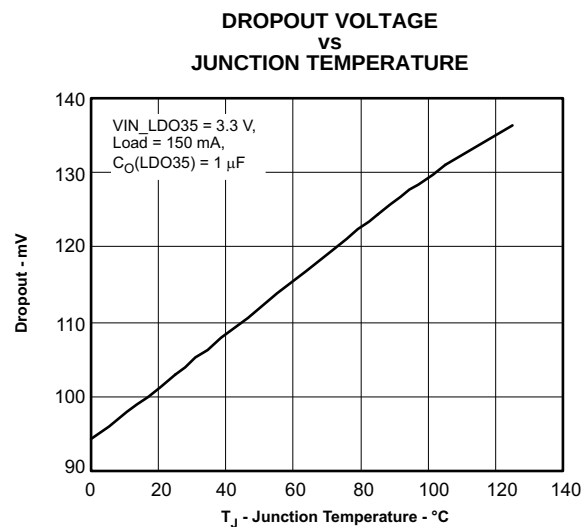


Figure 13.



## TYPICAL CHARACTERISTICS – SM1 AND SM2 BUCK CONVERTERS

Measured with application circuit shown in Figure 3, unless otherwise noted

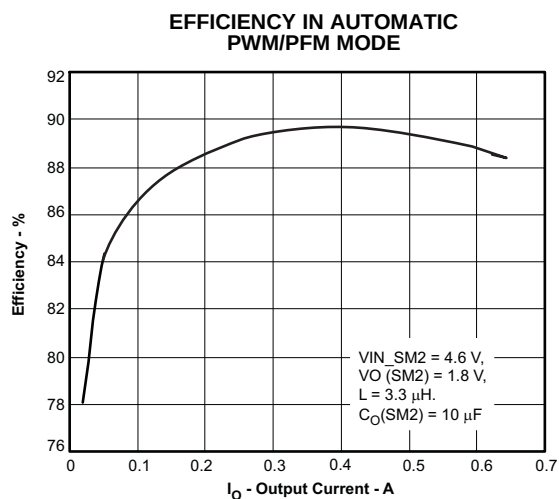


Figure 14.

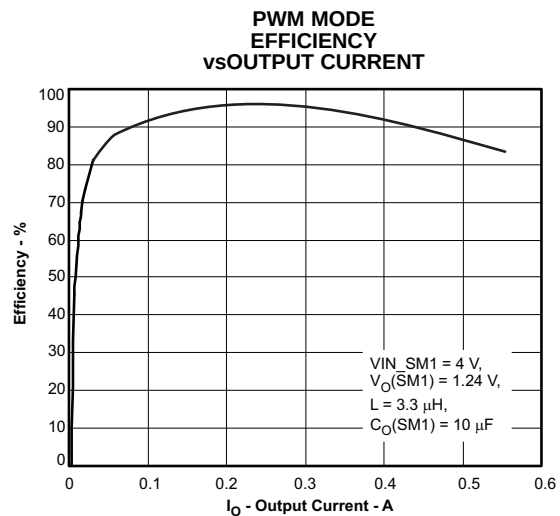


Figure 15.

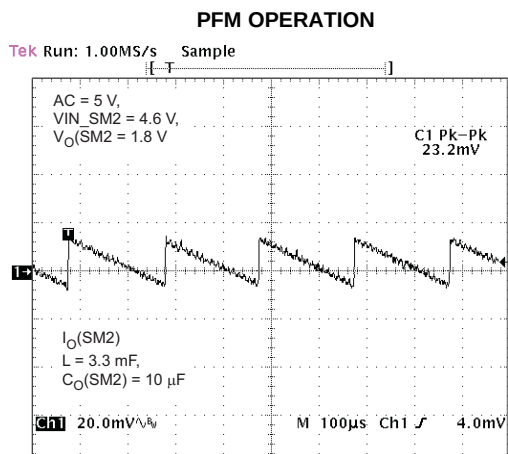


Figure 16.

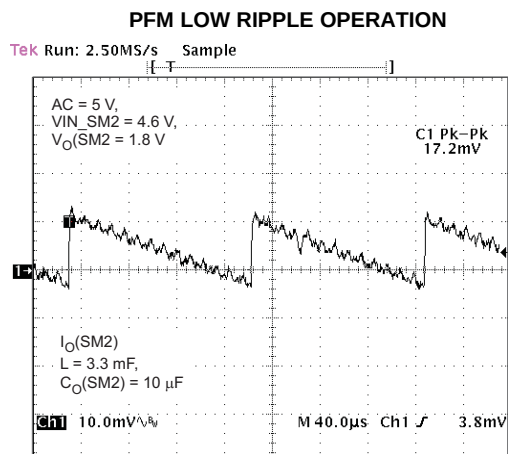


Figure 17.

## TYPICAL CHARACTERISTICS – DRIVERS

Measured with application circuit shown in Figure 3, unless otherwise noted

LINE TRANSIENT

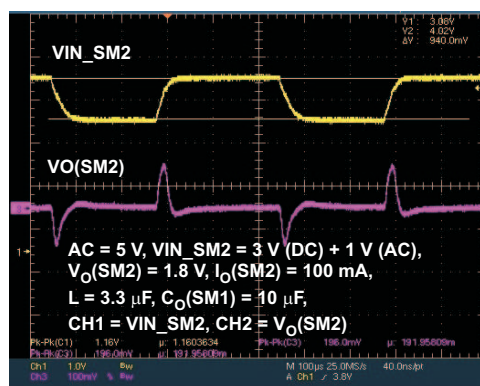


Figure 18.

LOAD TRANSIENT

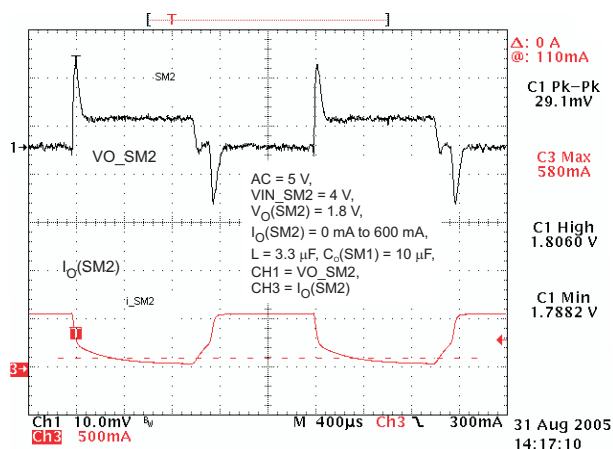


Figure 19.

TRANSIENT - SM1 STARTUP

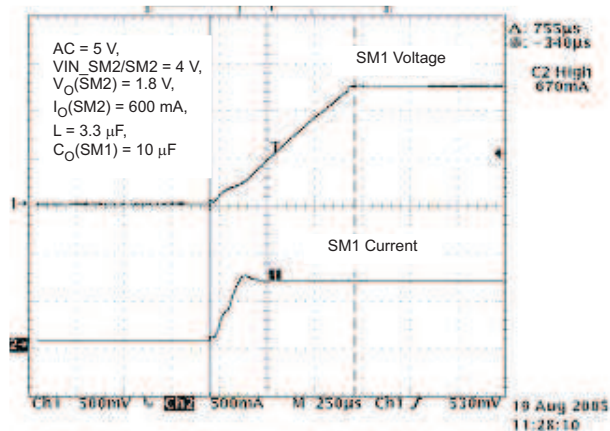


Figure 20.

TRANSIENT - SM2 STARTUP

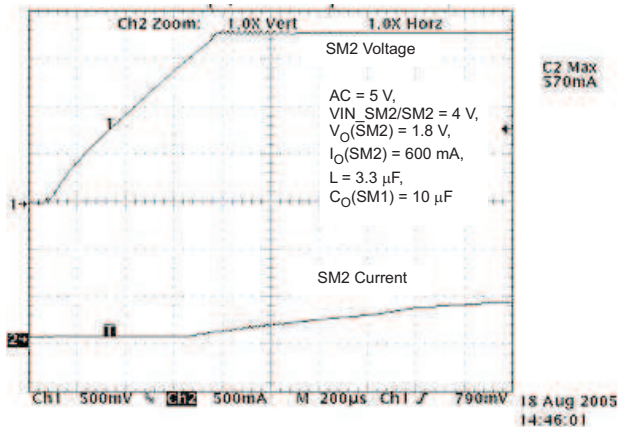


Figure 21.

## TYPICAL CHARACTERISTICS – DRIVERS (continued)

Measured with application circuit shown in [Figure 3](#), unless otherwise noted

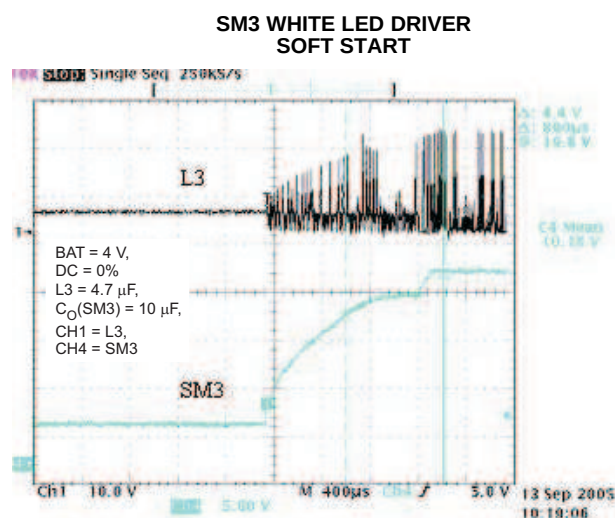


Figure 22.

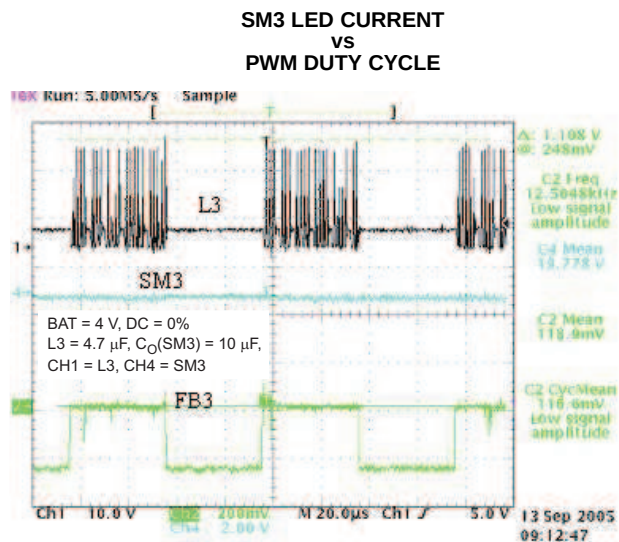


Figure 23.

## SERIAL INTERFACE

### Overview

The TPS65800 is compatible with a host-controlled environment, with internal parameters and status information accessible via an I<sup>2</sup>C interface. An I<sup>2</sup>C communication port provides a simple way for an I<sup>2</sup>C compatible host to access system status information and reset fault modes, functioning as a SLAVE port enabling I<sup>2</sup>C compatible hosts to WRITE to or to READ from internal registers. The TPS65800 I<sup>2</sup>C port is a 2-wire bidirectional interface using SCL (clock) and SDA (data) pins; the SDA pin is open drain and requires an external pullup. The I<sup>2</sup>C is designed to operate at SCL frequencies up to 400 kHz. The standard 8 bit command is supported, the CMD part of the sequence is the 8 bit register address to READ from or to WRITE to.

### Register Default Values

The internal TPS65800 registers are loaded during the initial power-up from an internal, non-volatile memory bank. The power-up default values are described in the sections detailing the registers functionality.

The register contents remain intact as long as OUT pin voltage remains above the internal UVLO threshold,  $V_{UVLO}$ . When the OUT pin voltage falls below the UVLO threshold all register bits are reset to the internal power up default.

### I<sup>2</sup>C Address

The I<sup>2</sup>C specification contains several global addresses, which the slaves on the bus are required to respond to. The TPS65800 only responds (ACK) to addresses 0x90 and 0x91 and does not respond (NACK) to any other address.

**Table 1. TPS65800 I<sup>2</sup>C Read/Write Address**

| BYTE                                    | BIT |    |    |    |    |    |    |     |
|-----------------------------------------|-----|----|----|----|----|----|----|-----|
|                                         | MSB | 6  | 5  | 4  | 3  | 2  | 1  | LSB |
| TPS65800 I <sup>2</sup> C WRITE ADDRESS | 1   | 0  | 0  | 1  | 0  | 0  | 0  | 0   |
| TPS65800 I <sup>2</sup> C READ ADDRESS  | 1   | 0  | 0  | 1  | 0  | 0  | 0  | 1   |
| I/O DATA BUS                            | B7  | B6 | B5 | B4 | B3 | B2 | B1 | B0  |

### Incremental Read

The TPS65800 does not support incremental read operations. Each register must be accessed in a single read operation.

### I<sup>2</sup>C Bus Release

The TPS65800 I<sup>2</sup>C engine does not create START or STOP states on the I<sup>2</sup>C bus during normal operation.

### Sleep Mode Operation

When the sleep mode is set SDAT is held LO by the TPS65800. The overall system operation is not affected, as in sleep mode all TPS65800 integrated supplies are disabled and no power is available for any external devices connected to the TPS65800 SDAT pin. When sleep mode ends the SDAT pin is released before the TPS65800 integrated regulated supplies are enabled. See section on [System Sequencing and TPS65800 Operating Modes](#) for additional details on sleep mode operation.

### I<sup>2</sup>C Bus Error Recovery

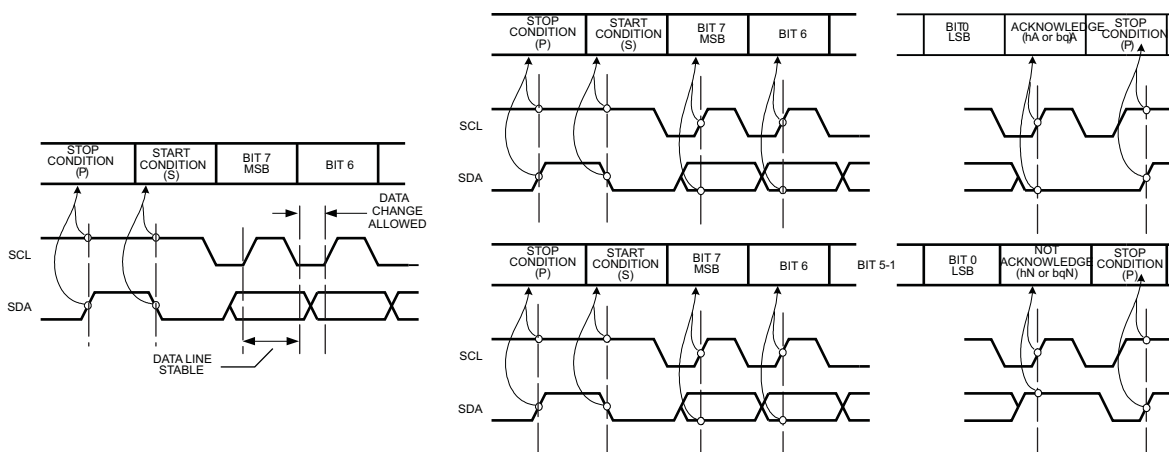
The I<sup>2</sup>C bus specification does not define a method to be used when recovering from a host side bus error. During a read operation, the SDA pin can be left in a LO state if the host has not sent enough SCL pulses to complete a transaction (i.e., host side bus error). The TPS65800 clears any SDA LO condition if 10 SCL pulses are sent by the host, enabling recovery from host side bus error events.

### I<sup>2</sup>C Communication Protocol

The following conventions are used when describing the communication protocol:

**Table 2. I<sup>2</sup>C Naming Conventions Used**

| CONDITION                                                                                               | CODE   |
|---------------------------------------------------------------------------------------------------------|--------|
| START sent from host                                                                                    | S      |
| STOP sent from host                                                                                     | P      |
| TPS65800 I <sup>2</sup> C slave address sent from host, bus direction set from host to TPS65800 (WRITE) | hA0    |
| TPS65800 register address sent from TPS65800, bus direction is from TPS65800 to host (READ)             | hA1    |
| Non-valid I <sup>2</sup> C slave address sent from host                                                 | hA_N   |
| Valid TPS65800 register address sent from host                                                          | HCMD   |
| Non-valid TPS65800 register address sent from host                                                      | HCMD_N |
| I/O data byte (8 bits) sent from host to TPS65800                                                       | hDATA  |
| I/O data byte (8 bits) sent from TPS65800 to host                                                       | bqDATA |
| Acknowledge (ACK) from host                                                                             | hA     |
| Not acknowledge (NACK) from host                                                                        | hN     |
| Acknowledge (ACK) from TPS65800                                                                         | bqA    |
| Not acknowledge (NACK) from TPS65800                                                                    | bqN    |



**Figure 24. I<sup>2</sup>C operation waveforms**

For normal data transfers, SDA is allowed to change only when SCL is low, and one clock pulse is used per bit of data. The SDA line must remain stable whenever the SCL line is high, as SDA changes when SCL is high are reserved for indicating the start and stop conditions. Each data transfer is initiated with a start condition and terminated with a stop condition.

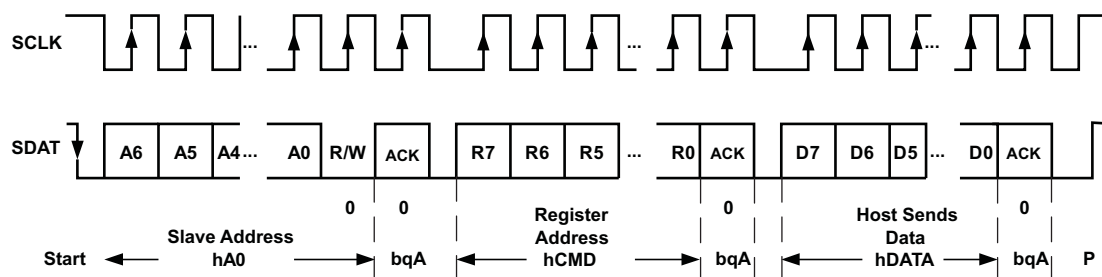
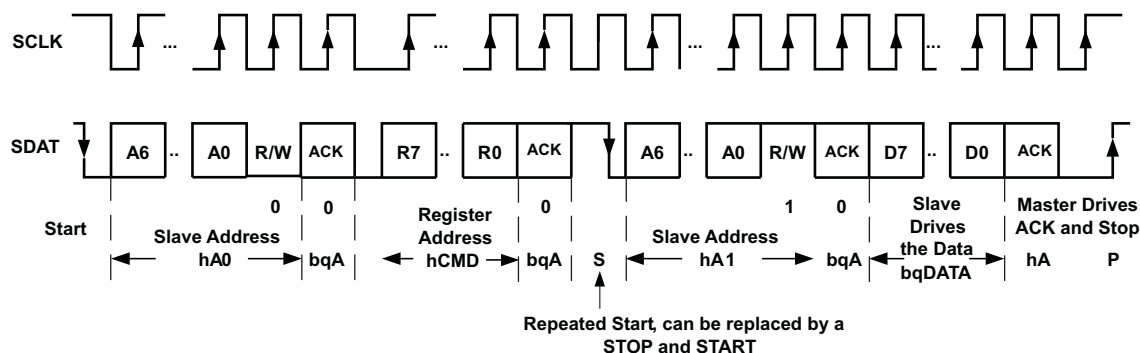
When addressed, the TPS65800 device generates an acknowledge bit after the reception of each byte by pulling the SDA line Low. The master device (microprocessor) must generate an extra clock pulse that is associated with the acknowledge bit. After the acknowledge/not acknowledge bit the TPS65800 leaves the data line high, enabling a STOP condition generation.

### I<sup>2</sup>C Read and Write Operations

The TPS65800 supports the standard I<sup>2</sup>C one byte Write. The basic I<sup>2</sup>C read protocol has the following steps:

- Host sends a start and sets TPS65800 I<sup>2</sup>C slave address in write mode.
- TPS65800 ACKs that this is a valid I<sup>2</sup>C address and that the bus is configured for write.
- Host sends TPS65800 register address.
- TPS65800 ACKs that this is a valid register and stores the register address to be read.
- Host sends a repeated start and TPS65800 I<sup>2</sup>C slave address, reconfiguring the bus for read.
- TPS65800 ACKs that this is a valid address and that bus is reconfigured.
- Bus is in read mode, TPS65800 starts sending data from selected register.

The I<sup>2</sup>C write protocol is similar to the read, without the need for a repeated start and bus being set in write mode. In a WRITE it is not necessary to end each 1 byte WRITE command with a STOP, a START has the same effect (repeated start).



**Figure 25. I<sup>2</sup>C read and write operations**

The host can complete a READ or a WRITE sequence with either a STOP or a START.

### Valid Write Sequences

The TPS65800 always ACKs its own address. If the CMD points to an allowable READ or WRITE address, bq writes the address into its RAM address register and sends an ACK. If the CMD points to a non-allowed address, bq does NOT write the address into its RAM address register and sends a NACK.

|   |     |     |        |     |
|---|-----|-----|--------|-----|
| S | hA0 | bqA |        |     |
| S | hA0 | bqA | hCMD   | bqA |
| S | hA0 | bqA | hCMD_N | bqN |

### One Byte Write

The data is written to the addressed register when the bq ACK ending the one byte write sequence is received. The host can cancel a WRITE by sending a STOP or START before the trailing edge of the bq ACK clock pulse.

|   |     |     |      |     |       |     |
|---|-----|-----|------|-----|-------|-----|
| S | hA0 | bqA | hCMD | bqA | hDATA | bqA |
|---|-----|-----|------|-----|-------|-----|

## Valid Read Sequences

The TPS65800 always ACKs its own address.

|   |     |     |
|---|-----|-----|
| S | hA1 | bqA |
|---|-----|-----|

Upon receiving hA1, TPS65800 starts at wherever the RAM address register is pointing. The START and the STOP both act as priority interrupts. If the host has been interrupted and is not sure where it left off it can send a STOP and reset the TPS65800 state machine to the WAIT state; once in WAIT state, the TPS65800 ignores all activity on the SCL and SDA lines until it receives a START. A repeated START and START in the I<sup>2</sup>C specification are both treated as a START.

|   |     |     |        |     |   |     |     |        |    |   |
|---|-----|-----|--------|-----|---|-----|-----|--------|----|---|
| S | hA0 | bqA | hCMD   | bqA | P |     |     |        |    |   |
| S | hA0 | bqA | hCMD   | bqA | S | hA1 | bqA | bqDATA | hN | P |
| S | hA1 | bqA | bqDATA | hN  | P |     |     |        |    |   |

## Non-Valid Sequences

### Incremental read sequences

|   |     |     |        |    |        |    |        |    |        |    |     |        |    |   |
|---|-----|-----|--------|----|--------|----|--------|----|--------|----|-----|--------|----|---|
| S | hA1 | bqA | bqDATA | hA | bqDATA | hA | bqDATA | hA | bqDATA | hA | ... | bqDATA | hA | P |
|---|-----|-----|--------|----|--------|----|--------|----|--------|----|-----|--------|----|---|

### START and non-hA0 or non-hA1 Address

A START followed by an address which is not bqA0 or bqA1 is NACKed.

|   |      |     |
|---|------|-----|
| S | hA_N | bqN |
|---|------|-----|

### Attempt to Specify Non-Allowed READ Address

If the CMD points to a non-allowed READ address (reserved registers), bq sends a NACK back to the host, and it does not load the address in the RAM address register. Note that TPS65800 NACKS whether a stop is sent or not.

|   |     |     |        |     |   |
|---|-----|-----|--------|-----|---|
| S | hA0 | bqA | hCMD_N | bqN | P |
| S | hA0 | bqA | hCMD_N | bqN |   |

### Attempt to Specify Non-Allowed WRITE Address

If the host attempts to WRITE to a READ-ONLY or non-accessible address TPS65800 ACKS the CMD containing the allowed READ address, loads the address into the address register and NACKS after the host sends the next data byte. After issuing the NACK TPS65800 returns to WAIT state. A subsequent hA1 READ could read this address.

|   |     |     |      |     |       |    |
|---|-----|-----|------|-----|-------|----|
| S | hA0 | bqA | hCMD | bqA | hDATA | bN |
|---|-----|-----|------|-----|-------|----|

**TPS65800 INTERNAL REGISTER MAP**

| hex | NAME            | DESCRIPTION                                                               | ADDITIONAL<br>DETAILS |
|-----|-----------------|---------------------------------------------------------------------------|-----------------------|
| 0   | RESERVED_01     | RESERVED                                                                  | FACTORY ONLY          |
| 1   | RESERVED_02     | RESERVED                                                                  | FACTORY ONLY          |
| 2   | PGOOD           | Output voltage status for linear regulators and dc/dc buck converters     |                       |
| 3   | INTMASK1        | Interrupt request masking settings                                        |                       |
| 4   | INTMASK2        | Interrupt request masking settings                                        |                       |
| 5   | INT_ACK1        | Masked interrupt request register, latched                                |                       |
| 6   | INT_ACK2        | Masked interrupt request register, latched                                |                       |
| 7   | PGOODFAULT_MASK | System Reset masking settings                                             |                       |
| 8   | SOFT_RESET      | Generates a software reset                                                |                       |
| 9   | CHG_CONFIG      | Battery charger configuration                                             |                       |
| A   | CHG_STAT        | Battery charger status                                                    |                       |
| B   | EN_LDO          | Linear regulator ON/OFF control                                           |                       |
| C   | LDO12           | LDO1 and LDO2 output voltage setting                                      |                       |
| D   | LDO3            | LDO3 output voltage settings                                              |                       |
| E   | LDO4            | LDO4 output voltage settings                                              |                       |
| F   | LDO5            | LDO5 output voltage settings                                              |                       |
| 10  | SM1_SET1        | SM1 Buck converter ON/OFF control and output voltage setting, normal mode |                       |
| 11  | SM1_SET2        | SM1 Buck converter configuration                                          |                       |
| 12  | SM1_STANDBY     | SM1 Buck converter standby mode ON/OFF and standby output voltage setting |                       |
| 13  | SM2_SET1        | SM2 Buck converter ON/OFF control and output voltage setting, normal mode |                       |
| 14  | SM2_SET2        | SM2 Buck converter configuration                                          |                       |
| 15  | SM2_STANDBY     | SM2 Buck converter standby mode ON/OFF and standby output voltage setting |                       |
| 16  | SM3_SET         | SM3 White LED driver ON/OFF control and settings                          |                       |
| 17  | RGB_FLASH       | Overall RGB driver timing settings                                        |                       |
| 18  | RGB_RED         | RGB driver: RED duty cycle and output current setting                     |                       |
| 19  | RGB_GREEN       | RGB driver: GREEN duty cycle and output current setting                   |                       |
| 1A  | RGB_BLUE        | RGB driver: BLUE duty cycle and output current setting                    |                       |
| 1B  | GPIO12          | GPIO1 and GPIO2 configuration                                             |                       |
| 1C  | GPIO3           | GPIO2 and GPIO3 configuration, battery charge voltage selection           |                       |
| 1D  | PWM             | PWM output configuration                                                  |                       |
| 1E  | ADC_SET         | ADC On/OFF control, ADC configuration                                     |                       |
| 1F  | ADC_reading_hi  | ADC data output                                                           |                       |
| 20  | ADC_reading_lo  | ADC data output                                                           |                       |
| 21  | DHILIM1         | ADC Maximum threshold setting                                             |                       |
| 22  | DHILIM2         | ADC Maximum threshold setting                                             |                       |
| 23  | DLOLIM1         | ADC Minimum threshold setting                                             |                       |
| 24  | DLOLIM2         | ADC Minimum threshold setting                                             |                       |
| 25  | ADC_DELAY       | ADC configuration: conversion delay                                       |                       |
| 26  | ADC_WAIT        | ADC configuration: wait and repeat operation                              |                       |
| 27  | LED_PWM         | LED_PWM configuration                                                     |                       |
| 2E  | RESERVED_03     | RESERVED                                                                  | FACTORY ONLY          |



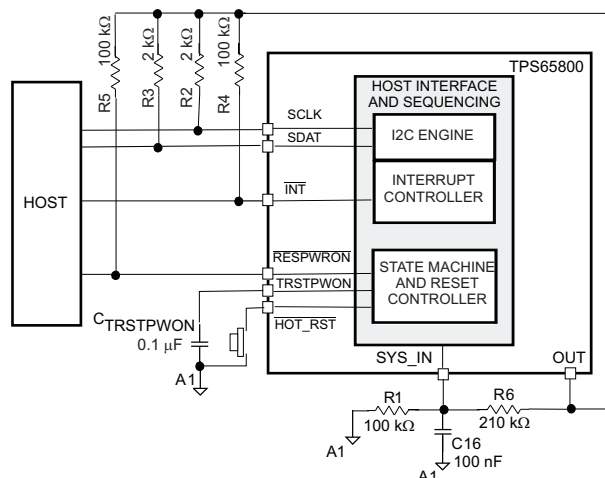
## FUNCTIONALITY REFERENCE GUIDE – HOST INTERFACE AND SYSTEM SEQUENCING

| INTERRUPT CONTROLLER, OPEN-DRAIN OUTPUT (INT)                                    |                                                                    |                                                                                            |                                                                                                    |                                                                                                  | Power up default                                  |
|----------------------------------------------------------------------------------|--------------------------------------------------------------------|--------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------|---------------------------------------------------|
| System Parameters Monitored by Interrupt Controller                              |                                                                    |                                                                                            |                                                                                                    |                                                                                                  |                                                   |
| Supply Output Power Good Fault Detection <sup>(1)</sup>                          | System Status Modification                                         | ADC status                                                                                 | Charger Status Transition                                                                          | Input and Output Power Transition                                                                |                                                   |
| SM1, SM2, SM3, LDO1, LDO2, LDO3, LDO4, LDO5                                      | Thermal Fault or GPIO 1,2 configured as external interrupt request | ADC conversion end<br>ADC Input out of range<br>External resistive load connected to ANLG1 | Charge: Pre↔ Fast ↔Done<br>DPPM:on ↔ off<br>Charge Suspend: on ↔ off<br>Thermal Foldback: on ↔ off | AC detected: yes ↔ no<br>USB detected: yes ↔ no<br>Input OVP: yes ↔ no<br>System Power: AC ↔ USB | All interrupt controller inputs set to non-masked |
| Can be masked Individually via I <sup>2</sup> C. Blanked during initial power up | Can be masked Individually via I <sup>2</sup> C                    |                                                                                            | Can be masked as a group via a single I <sup>2</sup> C mask register bit                           |                                                                                                  |                                                   |

- (1) For all supplies (except) for SM3 an output fault is detected if the output voltage is below 90% of the programmed regulation voltage. In the SM3 converter an output fault indicates that the output OVP threshold was reached.

| EVENTS TRIGGERING TPS65800 OPERATING MODE CHANGES |                                                                                                               |                                                        |                                                                                                                        |                                                                                                                  |
|---------------------------------------------------|---------------------------------------------------------------------------------------------------------------|--------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------|
| EVENT                                             | POWER GOOD FAULT DETECTION <sup>(1)</sup>                                                                     | THERMAL FAULT                                          | HARDWARE RESET                                                                                                         | SOFTWARE RESET                                                                                                   |
| How transition is triggered                       | Integrated regulator output voltage below target value: SM1, SM2, SM3, LDO1, LDO2, LDO3, LDO4, LDO5           | Internal IC junction temperature                       | Using $\overline{\text{HOT\_RST}}$ control pin                                                                         | I <sup>2</sup> C register control bit                                                                            |
| Operating mode change                             | Sets Sleep mode or starts a new power-up cycle when power good fault is detected (see state machine diagram). | Sets sleep mode when thermal fault is detected         | Generates external host reset pulse at pin $\overline{\text{RESPWON}}$ when $\overline{\text{HOT\_RST}} = \text{LO}$ . | Generates external host reset pulse at pin $\overline{\text{RESPWON}}$ when I <sup>2</sup> C control bit is set. |
|                                                   | Power good fault detection comparators are blanked during initial power-up.                                   | Input and battery power cycling required to exit sleep | Pulse duration set by external capacitor.                                                                              | Pulse duration set by external capacitor.                                                                        |
| Controls                                          | Can be masked Individually via I <sup>2</sup> C.                                                              | Fixed internal threshold                               | External Input                                                                                                         | Set via I <sup>2</sup> C                                                                                         |

- (1) For all supplies (except) for SM3 an output fault is detected if the output voltage is below 90% of the programmed regulation voltage. In the SM3 converter an output fault indicates that the output OVP threshold was reached.



**Figure 26. Required External Components, Recommended Values, External Connections**

## INTERRUPT CONTROLLER AND SYSTEM SEQUENCING

### Overview

The TPS65800 has two dedicated internal controllers that execute the host interface and system sequencing tasks: a sequencing controller and an interrupt controller.

The sequencing controller monitors internal and system parameters and defines the sequencing of the internal power supplies during power up and power down / power fault events, and executes specific internal power supply reset operations under external hardware control or host software commands.

The following parameters are monitored by the sequencing controller:

- System power bus voltage (at SYS\_IN pin), input supply voltage, battery pack voltage
- TPS65800 thermal fault status
- Integrated supply status

The interrupt controller monitors multiple system status parameters and signals to the host when one of the monitored parameters toggled, as a result of a system status change. The interrupt controller inputs include all the parameters monitored by the sequencing controller plus:

- Charger status
- Battery pack status
- ADC status

Internal I<sup>2</sup>C registers enable masking of all the monitored parameters. Using those registers the host can select which parameters trigger an interrupt or a power-good fault. Power good faults trigger a change in the TPS65800 operating mode, as detailed in the next sections.

A simplified block diagram for the TPS65800 sections that interface to the external host is shown in [Figure 27](#).

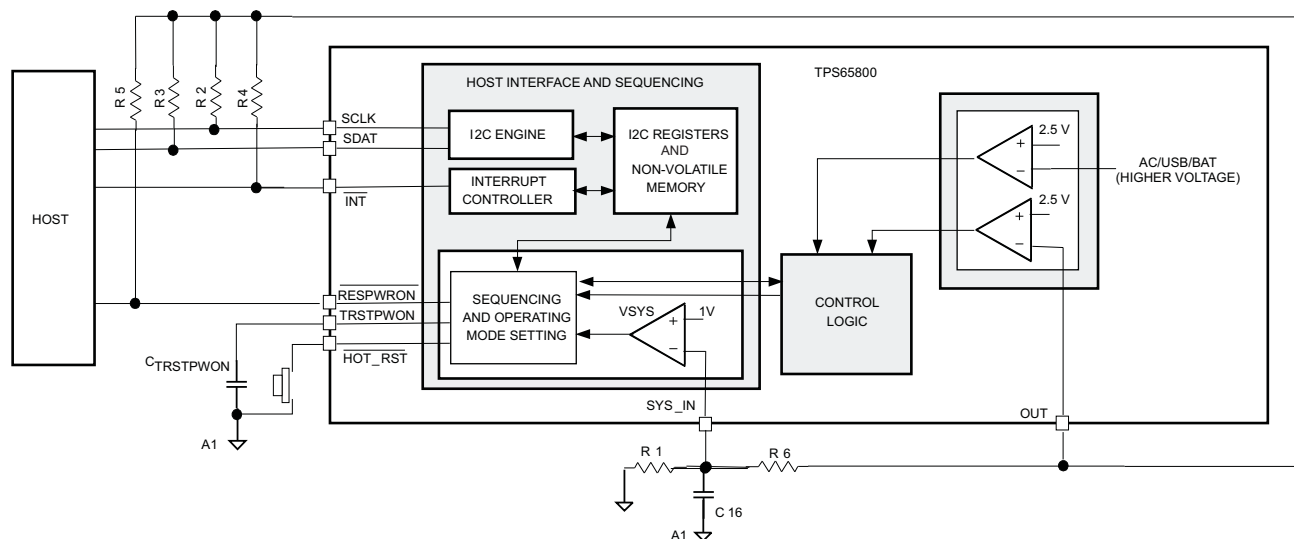


Figure 27. Simplified Block Diagram

## SYSTEM SEQUENCING AND TPS65800 OPERATING MODES

The TPS65800 has a state machine that controls the device power up and power down sequencing. The main operating modes are shown in the state diagram below:

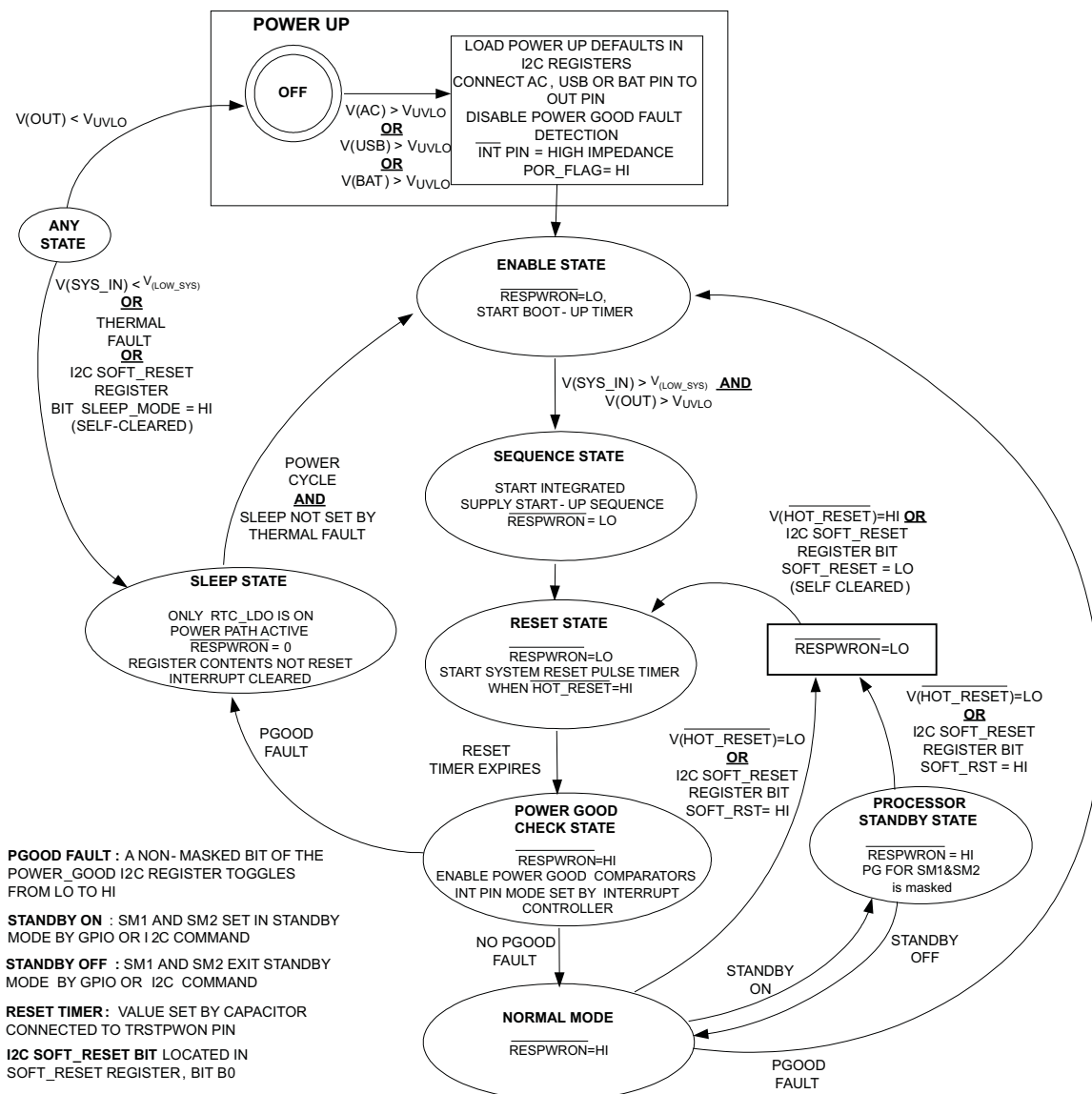


Figure 28. TPS65800 State Diagram

**POWER-UP**– If the AC, USB and BAT pin voltages are below the internal UVLO threshold  $V_{UVLO}$  (2.5 V typ) all IC blocks are disabled and the TPS65800 is not operational, with all functions OFF. When an external power source or battery with voltage greater than the  $V_{UVLO}$  voltage threshold is applied to AC/USB or BAT pins the internal TPS65800 references are powered up, biasing internal circuits. When all the main internal supply rails are active the TPS65800 I<sup>2</sup>C registers are set to the power-up default values, shown below:

**Table 3. Integrated Supply and Drivers Power-Up Defaults**

| SUPPLY  | POWER-UP DEFAULT        | OTHER BLOCKS    | POWER-UP DEFAULT |
|---------|-------------------------|-----------------|------------------|
| LDO0    | OFF, 3.3 V              | POWER PATH      | INPUT TO SYSTEM  |
| LDO1    | 2.85V, ON               | PWM             | OFF              |
| LDO2    | 3.3 V, ON               | PWM_LED         | OFF              |
| LDO3    | 1.25 V, ON              | GPIO1           | INPUT            |
| LDO4    | 2.75 V, ON              | GPIO2           | INPUT            |
| LDO5    | 2.81 V, ON              | GPIO3           | INPUT            |
| SIM     | 1.8 V, OFF              | ADC             | OFF              |
| RTC_OUT | ON, 3.1 V               | SM3 (WHITE LED) | OFF              |
| LDO_PM  | 3.3 V, ON @ OUT POWERED | RGB DRIVER      | OFF              |
| SM1     | ON, 1.24 V              | INTERRUPT MASK  | NONE MASKED      |
| SM2     | ON, 1.8 V               | POWER GOOD MASK | ALL MASKED       |
| CHARGER | ON                      |                 |                  |

After the internal I<sup>2</sup>C register power-up defaults are loaded the power path control logic is enabled, connecting the external power source to the OUT pin. A status flag (nRAMLOAD) is set to LO in the SOFT\_RESET register, indicating that the I<sup>2</sup>C registers were loaded with the power-up defaults, and the TPS65800 enters the ENABLE mode.

**ENABLE:** In the ENABLE mode the  $\overline{\text{RESPWRON}}$  output is set to the LO level, the  $\overline{\text{INT}}$  pin mode is set to high impedance and all the power good comparators that monitor the integrated supply outputs are disabled. The ENABLE mode is used by the TPS65800 to detect when the main system power rail (OUT pin) is powered and ready to be used on the internal supply power-up. The OUT pin voltage is sensed by an internal low system voltage comparator, which holds the IC in the ENABLE mode until the system power bus voltage (OUT pin) has reached a minimum operating voltage, defined by the user. The internal comparator senses the system voltage at pin SYS\_IN, and the threshold for the minimum system operating voltage at the OUT pin is set by the external divider connected from OUT pin to SYS\_IN pin. The threshold voltage is calculated as follows:

$$V(\text{OUT}) = V_{(\text{LOW\_SYS})} \times \left(1 + \frac{R6}{R1}\right):$$

where R6 and R1 are external resistors,  $V_{(\text{LOW\_SYS})} = 1 \text{ V}$  typical (1)

The minimum system operating voltage should always be set above the internal UVLO threshold  $V_{\text{UVLO}}$ . In normal application conditions the minimum system operating voltage is usually set to a value that assures that the TPS65800 integrated regulators are not operating in the dropout region.

When the voltage at the SYS\_IN pin exceeds the internal threshold  $V_{(\text{LOW\_SYS})}$  the TPS65800 is ready to start the system power sequencing, and the SEQUENCING mode is entered.

**SEQUENCING**– The sequencing state starts immediately after the enable state. In this mode of operation the integrated supplies are turned ON, according to the sequencing steps loaded from the internal non-volatile memory during the power-up phase. The TPS65800 sequencing timing diagram shown in figure details the internal timing delays and supply sequencing. At the end of the sequencing state the user-programmable reset timer is started, and the TPS65800 enters the reset state.

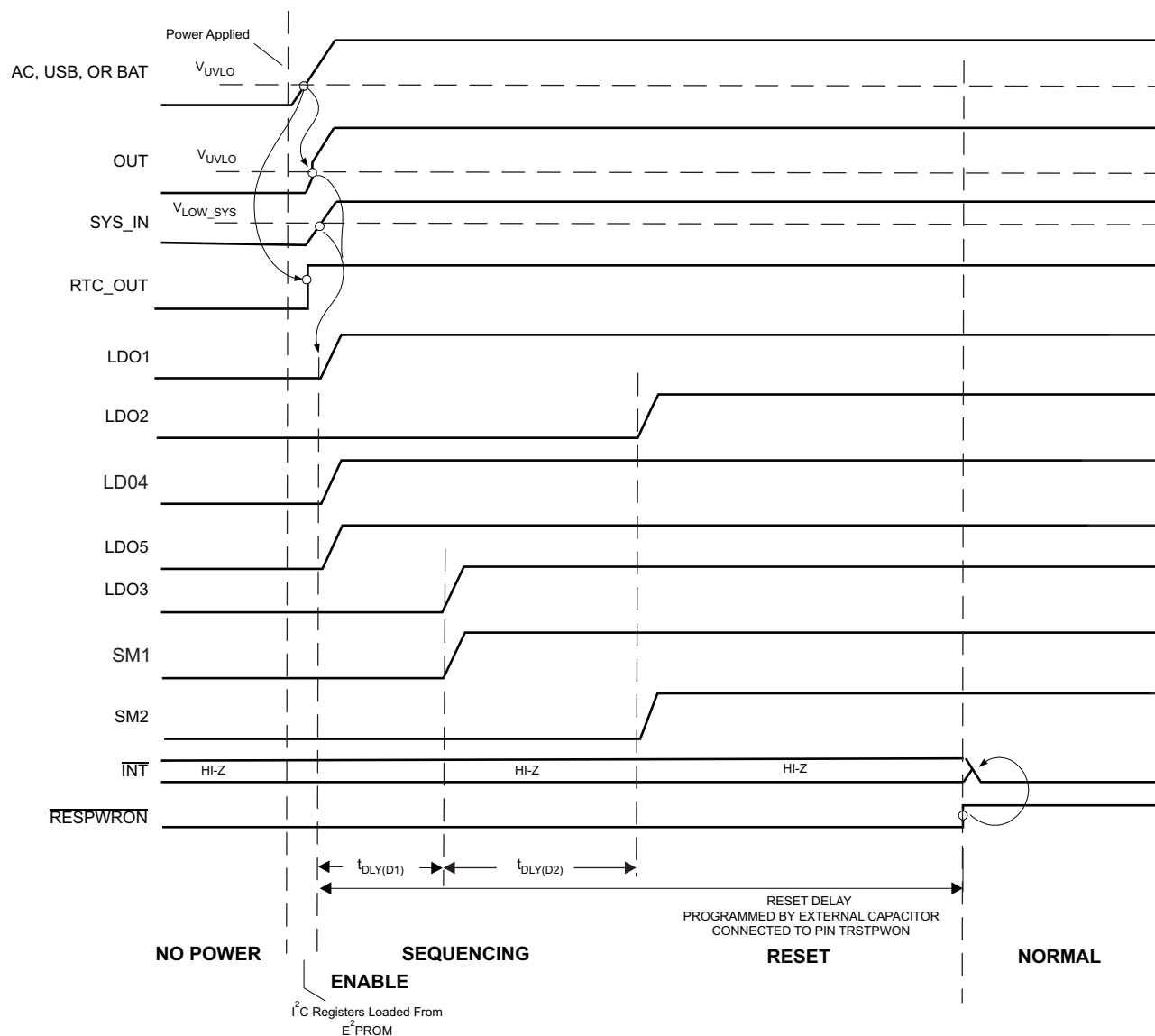


Figure 29. TPS65800 Supply Sequencing Timing

**RESET** – When the reset state starts the  $\overline{\text{RESPWRON}}$  output is LO. The user can program the reset timer value selecting the value of the external capacitor connected to pin TRSTPWON, as shown below:

$$T_{(\text{RESET})} = K_{\text{RESET}} \times C_{\text{TRSTPWON}}; \text{ where } K_{\text{RESET}} \text{ is the reset timer constant (1 ms/nF typ)}$$

The TPS65800  $\overline{\text{RESPWRON}}$  pin should be used to reset the external host. During the external host reset ( $\overline{\text{RESPWRON}} = \text{LO}$ ) the I<sup>2</sup>C SDA and SCL pins are not used to access TPS65800 internal registers. If a non-standard configuration is used to reset the system the SDA and SCL lines should not be used to communicate with the TPS65800 until  $\overline{\text{RESPWRON}} = \text{HI}$ , in order to avoid overwriting the integrated power supply internal power-up settings during the sequencing mode.

The power good comparators are masked during the reset mode. The reset mode ends when the reset timer expires, and the TPS65800 goes into the power good check mode.

The  $\overline{\text{RESPWRON}}$  signal set to a high level is the proper signal to use as an indicator that the device has transitioned out of the reset state. During the power-up sequence the  $\overline{\text{RESPWRON}}$  pin is asserted LOW until the RESET TIMER expires. The RESET TIME ( $t_{\text{reset}} = 1\text{ms/nF} \times C_{\text{TRSTPWON}}$ ) can be programmed via a capacitor between the TRSTPWON pin and ground.

When the RESPWRON signal is LO, all internal and external interrupts are ignored. As a result, the open-drain output that asserts the INT pin LO during a NORMAL MODE interrupt request is disabled. The INT pin is then asserted HI via a pullup resistor that is typically connected to VOUT. After the  $\overline{\text{RESPWRON}}$  signal goes HI, the interrupt controller is given control of the INT pin. Finally, the rising edge of the  $\overline{\text{RESPWRON}}$  pin should be used to indicate the PMIC has transitioned from the RESET STATE to the POWER GOOD CHECK STATE. At that point, the interrupt controller asserts an interrupt if necessary.

**POWER GOOD CHECK** – In the power good check mode the power good comparators are enabled, providing status on the integrated supplies output voltages. An output voltage is considered as out of regulation and generates a fault condition if the output voltage is below 90% of the target output voltage regulation value. If a power good fault is detected the SLEEP mode is set, if a power good fault is not detected the NORMAL mode is set.

The individual supply power good status can be masked via an I<sup>2</sup>C register PGOODFAULT\_MASK. Supplies that have their power-good fault status masked do not generate a power good fault. However, the status bit for the supply indicates that the output voltage is out of regulation.

The power good mask register bits default to masked upon power up.

**NORMAL MODE** – If a power good fault is not present at the end of the power good check mode the NORMAL mode starts. In this mode of operation the I<sup>2</sup>C registers define the TPS65800 operation, and the host has full control on operation modes, parameter settings, etc. The normal state operation ends if a thermal fault, system low voltage fault ( $V(\text{SYS\_IN}) < V_{\text{LOW\_SYS}}$ ) or power-good fault is detected. A thermal fault or system low voltage fault sets the SLEEP mode operation, a power good fault sets the NO POWER operation mode. From the normal mode the converters SM1 and SM2 can be set in the STANDBY mode, with reduced output voltages. In NORMAL mode either an I<sup>2</sup>C register bit (SOFT\_RESET register bit SOFT\_RST) or a hardware input ( $\overline{\text{HOT\_RESET}}$  pin set to LO) can trigger a transition to the RESET state, enabling implementation of a host reset function. In NORMAL mode an I<sup>2</sup>C register bit (SOFT\_RESET register bit SLEEP\_MODE) can trigger a transition to SLEEP mode.

**SLEEP MODE** – The SLEEP mode is set when a thermal fault or system low voltage fault is detected, under NORMAL operation mode set. This operation mode is also set when a power good fault is detected during the power good check state or via the I<sup>2</sup>C bit SLEEP\_MODE. In the SLEEP mode the  $\overline{\text{RESPWRON}}$  output is set to LO, and the I<sup>2</sup>C registers keep the same contents as in the state preceding SLEEP mode, with the exception of the following control bits, which are reset to the default power-up values:

1. LDO1, -2, -3, -4, -5, and RTC\_OUT are enabled, SIM LDO is disabled: EN\_LDO register set to default values
2. LDO0 disabled, all GPIO's with no control function assigned: GPIO12, GPIO3 registers set to default values
3. White LED driver is set to OFF: SM3\_SET register has all bits set to LO
4. RGB drivers are set to OFF: RGB\_FLASH, RGB\_RED, RGB\_GREEN, RGB\_BLUE registers are set to default values
5. PWM, PWM\_LED drivers OFF: PWM, LED\_PWM registers are set to default values
6. ADC engine reset to power up default: ADC\_SET, ADC\_DELAY, ADC\_WAIT registers are set to default values

***In SLEEP mode, the power path and main internal blocks are still active, but the internal integrated supply sequencing is disabled. As a result of that, during SLEEP mode ALL integrated supplies (ALL LDOs, ALL buck converters) are disabled.***

At the end of the SLEEP mode, the sequencer block uses the I<sup>2</sup>C control register values (which were reset to the default power-up values) to sequence the integrated power supplies. The SLEEP mode ends when one of the three following events happens:

1. *If SLEEP was set by thermal fault:* The SLEEP mode ends only when all external input supplies and battery pack are removed and a UVLO condition is detected by the TPS65800, setting the NO POWER mode.
2. *If SLEEP was set by a system low voltage detection, or I<sup>2</sup>C bit SLEEP\_MODE, only with battery present:* Input power must be connected, setting the TPS65800 in the ENABLE mode. If no input power is inserted, the battery discharges until the TPS65800 detects an UVLO condition and enters the NO POWER mode.

3. If sleep was set by a system low-voltage detection, power good fault or *SLEEP\_MODE*, with battery and input power present: all external input supplies connected to AC and USB pins must be removed, and then at least one of them reconnected to the system. The input power cycling triggers a transition from the SLEEP mode to the ENABLE mode.

**PROCESSOR STANDBY STATE**– This state is set using a I<sup>2</sup>C register or a GPIO configured as SM1/SM2 standby control. In standby mode operation the SM1 and SM2 voltages are set to value distinct than the normal mode output voltage, and SM1/SM2 are set to PFM mode. The standby output voltage is defined in I<sup>2</sup>C registers SM1\_STANDBY and SM2\_STANDBY.

## TPS65800 OPERATING MODE CONTROLS

**HARDWARE RESET:** A dedicated control pin, *HOT\_RESET*, enables implementation of a hardware reset function. The system reset pin *RESPWRON* is set to LO when *HOT\_RESET* = LO for a period longer than the internal deglitch (5 ms, typ). The RESET mode is started when the *HOT\_RESET* pin transitions from LO to HI, as shown in the state diagram.

**SOFTWARE RESET:** The external host can set the TPS65800 in RESET mode using the I<sup>2</sup>C register *SOFT\_RESET*, bit B0 (*SOFT\_RST*).

**SOFTWARE SLEEP:** The external host can set the TPS65800 in SLEEP mode using the I<sup>2</sup>C register *SOFT\_RESET*, bit B6 (*SLEEP\_MODE*).

A hardware or software reset does not affect the contents of the I<sup>2</sup>C registers.

## SEQUENCING AND OPERATING MODES – I<sup>2</sup>C REGISTERS

The I<sup>2</sup>C registers that control sequencing-related functions are shown below. The HEX address for each register is shown by the register name, together with the R or W functionality for the register bits. Shaded values indicate default initial power-up values.

| SOFT_RESET, ADDRESS=08, ALL BITS R/W, BITS B7/B6/B1/B0 APPLY TO SEQUENCING. |                                   |                                         |          |          |                                           |          |                         |                                         |
|-----------------------------------------------------------------------------|-----------------------------------|-----------------------------------------|----------|----------|-------------------------------------------|----------|-------------------------|-----------------------------------------|
|                                                                             | B7                                | B6                                      | B5       | B4       | B3                                        | B2       | B1                      | B0                                      |
| Bit name                                                                    | STBY MODE                         | SLEEP MODE                              | NOT USED | NOT USED | SM3_LF_OSc                                | NOT USED | nRAMLOAD                | SOFT RST                                |
| Function                                                                    | SET SM1 AND SM2 IN STANDBY MODE   | SET TPS65800 IN SLEEP MODE              | NOT USED | NOT USED | NOT RELATED TO SEQUENCING SEE SM3 SECTION | NOT USED | RAM RESET FLAG          | SOFTWARE RESET CONTROL                  |
| When 0                                                                      | NOT ACTIVE                        | NOT ACTIVE                              | NOT USED | NOT USED |                                           | NOT USED | RAM DEFAULTS LOADED     | NOT ACTIVE                              |
| When 1                                                                      | When 1 SET SM1 AND SM2 IN STANDBY | SET SLEEP MODE (reset to LO internally) | NOT USED | NOT USED |                                           | NOT USED | RAM DEFAULTS NOT LOADED | SET RESET MODE (reset to LO internally) |

Some host algorithms need to identify when the power-up defaults are loaded in the RAM, in order to start routines that initialize specific RAM registers. If that functionality is required the nRAMLOAD bit should be set to HI by the host when entering the NORMAL operation mode. The nRAMLOAD bit is reset to LO by the TPS65800 when the power-up defaults are loaded in the I<sup>2</sup>C registers (*V(OUT)* < *V<sub>UVLO</sub>* OR *PGOOD* fault detected), enabling the host algorithm to detect that the RAM registers require initialization.

The integrated supplies status is available in a dedicated register, shown below. The host can select which integrated supply outputs trigger a power-good fault condition using the *PGOODFAULT\_MASK* register.

When a non-masked power-good status register bit toggles state, the sequence controller generates a transition in the TPS65800 state machine, indicated as a *PGOOD FAULT* in the TPS65800 state diagram.

The power-good status register and mask register are shown below:

| SYSTEM STATUS MONITORED BY SEQUENCING CONTROLLER                                                     |                   |                   |                |                    |                    |                    |                    |                    |
|------------------------------------------------------------------------------------------------------|-------------------|-------------------|----------------|--------------------|--------------------|--------------------|--------------------|--------------------|
|                                                                                                      | B7                | B6                | B5             | B4                 | B3                 | B2                 | B1                 | B0                 |
| PGOOD, ADDRESS=02, ALL BITS READ ONLY - POWER UP DEFAULTS SHOW SYSTEM STATUS WHEN EXITING POWER DOWN |                   |                   |                |                    |                    |                    |                    |                    |
| Bit name                                                                                             | PGOOD SM1         | PGOOD SM2         | PGOOD SM3      | PGOOD LDO1         | PGOOD LDO2         | PGOOD LDO3         | PGOOD LDO4         | PGOOD LDO5         |
| Function                                                                                             | SM1 OUTPUT STATUS | SM2 OUTPUT STATUS | SM3 OVP STATUS | LDO1 OUTPUT STATUS | LDO2 OUTPUT STATUS | LDO3 OUTPUT STATUS | LDO4 OUTPUT STATUS | LDO5 OUTPUT STATUS |



| SYSTEM STATUS MONITORED BY SEQUENCING CONTROLLER |                         |                         |                         |                          |                          |                          |                          |                          |
|--------------------------------------------------|-------------------------|-------------------------|-------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|
|                                                  | B7                      | B6                      | B5                      | B4                       | B3                       | B2                       | B1                       | B0                       |
| When 0                                           | OK                      | OK                      | OK                      | OK                       | OK                       | OK                       | OK                       | OK                       |
| When 1                                           | FAULT                   | FAULT                   | FAULT                   | FAULT                    | FAULT                    | FAULT                    | FAULT                    | FAULT                    |
| PGOODFAULT_MASK, ADDRESS=07, ALL BITS R/W        |                         |                         |                         |                          |                          |                          |                          |                          |
| Bit name                                         | MASK_PSM1               | MASK_PSM2               | MASK_PSM3               | MASK_PLDO1               | MASK_PLDO2               | MASK_PLDO3               | MASK_PLDO4               | MASK_PLDO5               |
| Function                                         | MASK PGOOD FAULT BY SM1 | MASK PGOOD FAULT BY SM2 | MASK PGOOD FAULT BY SM3 | MASK PGOOD FAULT BY LDO1 | MASK PGOOD FAULT BY LDO2 | MASK PGOOD FAULT BY LDO3 | MASK PGOOD FAULT BY LDO4 | MASK PGOOD FAULT BY LDO5 |
| When 0                                           | UNMASKED                | UNMASKED                | UNMASKED                | UNMASKED                 | UNMASKED                 | UNMASKED                 | UNMASKED                 | UNMASKED                 |
| When 1                                           | MASKED                  | MASKED                  | MASKED                  | MASKED                   | MASKED                   | MASKED                   | MASKED                   | MASKED                   |

## INTERRUPT CONTROLLER

The TPS65800 has internal block and overall system status information stored in I<sup>2</sup>C status registers. The following subsystems and system parameters are monitored:

- External power supply status: AC or USB supply detected, AC or USB connected to system, AC/USB OVP
- Charger status: on/off/suspend, fast charge/precharge, termination detected, DPPM on, thermal loop ON
- Battery pack status: temperature, discharge on/off
- TPS65800 Thermal shutdown
- ADC status: conversion status, input out of range, ANLG1 high impedance detection
- Integrated supplies status: output out of regulation (power good fault)

The GPIO1 and GPIO2 pins can be configured as inputs, generating an interrupt request to the host ( $\overline{\text{INT}}:\text{HI} \rightarrow \text{LO}$ ) at the GPIO rising or falling edge. The host can use internal the INT\_MASK I<sup>2</sup>C registers to define which of the monitored status variables triggers an interrupt. When a non-masked system status bit toggles state, the interrupt controller issues an interrupt, following the steps below:

1. system status bits that caused the interruption are set to HI in registers INT\_ACK1 and INT\_ACK2
2. An interrupt is sent to the host ( $\overline{\text{INT}}:\text{HI} \rightarrow \text{LO}$ )

Once an interrupt is sent to the host,  $\overline{\text{INT}}$  is kept in the LO state and the INT\_ACK registers contents are latched, holding the system status that generated the currently issued interrupt request. When an interrupt request is active ( $\overline{\text{INT}} = \text{LO}$ ) additional changes in non-masked status registers and control signals are ignored, and the INT\_ACK registers are not updated.

The host must write a 0 to the INT\_ACK register bit that generated the interrupt in order to set  $\overline{\text{INT}} = \text{HI}$  and enable new updates to the INT\_ACK registers. If the host stops in the middle of a WRITE or READ operation, the  $\overline{\text{INT}}$  pin stays at the LO level. The TPS65800 has no reset timeout; it is assumed that the host does not leave  $\overline{\text{INT}} = \text{LO}$  and the status registers unread for a long time.

The non-masked I<sup>2</sup>C register bits and internal control signals generate a new interrupt only after  $\overline{\text{INT}}$  is set to HI. The non-masked power-good fault register bits generate a power-good fault when any of the non-masked bits detects that the monitored output voltage is out of regulation, independently of the  $\overline{\text{INT}}$  pin level.

## SYSTEM STATUS — I<sup>2</sup>C REGISTERS

The I<sup>2</sup>C registers that have system status data are shown below. The HEX address for each register is shown by the register name, together with the R or W functionality for the register bits. Those registers are valid, after an initial power up, when the TPS65800 enters the normal operation mode.

| SYSTEM STATUS MONITORED BY INTERRUPT CONTROLLER                                                      |                   |                   |                |                    |                    |                    |                    |                    |
|------------------------------------------------------------------------------------------------------|-------------------|-------------------|----------------|--------------------|--------------------|--------------------|--------------------|--------------------|
|                                                                                                      | B7                | B6                | B5             | B4                 | B3                 | B2                 | B1                 | B0                 |
| PGOOD, ADDRESS=02, ALL BITS READ ONLY - POWER UP DEFAULTS SHOW SYSTEM STATUS WHEN EXITING POWER DOWN |                   |                   |                |                    |                    |                    |                    |                    |
| Bit name                                                                                             | PGOOD SM1         | PGOOD SM2         | PGOOD SM3      | PGOOD LDO1         | PGOOD LDO2         | PGOOD LDO3         | PGOOD LDO4         | PGOOD LDO5         |
| Function                                                                                             | SM1 OUTPUT STATUS | SM2 OUTPUT STATUS | SM3 OVP STATUS | LDO1 OUTPUT STATUS | LDO2 OUTPUT STATUS | LDO3 OUTPUT STATUS | LDO4 OUTPUT STATUS | LDO5 OUTPUT STATUS |
| When 0                                                                                               | OK                | OK                | OK             | OK                 | OK                 | OK                 | OK                 | OK                 |
| When 1                                                                                               | FAULT             | FAULT             | FAULT          | FAULT              | FAULT              | FAULT              | FAULT              | FAULT              |



| SYSTEM STATUS MONITORED BY INTERRUPT CONTROLLER                                                                                                                                                 |                         |                             |                             |                       |                        |                                                              |       |                               |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------|-----------------------------|-----------------------------|-----------------------|------------------------|--------------------------------------------------------------|-------|-------------------------------|
|                                                                                                                                                                                                 | B7                      | B6                          | B5                          | B4                    | B3                     | B2                                                           | B1    | B0                            |
| CHG_STAT, ADDRESS=A, ALL BITS READ ONLY – POWER UP DEFAULTS SHOW SYSTEM STATUS WHEN EXITING POWER DOWN                                                                                          |                         |                             |                             |                       |                        |                                                              |       |                               |
| Bit name                                                                                                                                                                                        | BAT_STAT <sup>(1)</sup> | INPUT_PWR                   | THDPPM_ON                   | ACPG                  | USBPG                  | STAT1                                                        | STAT2 | INP_OV                        |
| Function                                                                                                                                                                                        | BATTERY DISCH STATUS    | SELECTED INPUT POWER STATUS | THERMAL FAULT AND DPPM MODE | AC INPUT POWER STATUS | USB INPUT POWER STATUS | CHARGE STATUS                                                |       | AC OR USB INPUT OVP DETECTION |
| When 0                                                                                                                                                                                          | NOT DISCHARGING         | AC INPUT SELECTED           | BOTH OFF                    | AC NOT DETECTED       | USB NOT DETECTED       | 00=FAULT/OFF/SUSPEND, 01=DONE, 10=FAST CHG ON, 11= PRECHARGE |       | NO OVP                        |
| When 1                                                                                                                                                                                          | When 1 DISCHARGING      | USB INPUT SELECTED          | DPPM ON OR THERMAL ON       | AC DETECTED           | USB DETECTED           |                                                              |       | OVP DETECTED                  |
| ADC STATUS                                                                                                                                                                                      |                         |                             |                             |                       |                        |                                                              |       |                               |
| REGISTER ADC_READING_HI, B7: CONVERSION COMPLETE;<br>INTERNAL STATUS BITS (NO I <sup>2</sup> C REGISTER BIT AVAILABLE: INPUT OUT OF RANGE (HI OR LO), ANLG1 PIN IMPEDANCE TO AGND2 EXCEEDS 1 mΩ |                         |                             |                             |                       |                        |                                                              |       |                               |
| OTHER SYSTEM STATUS: THERMAL FAULT DETECTED                                                                                                                                                     |                         |                             |                             |                       |                        |                                                              |       |                               |

(1) BAT\_STAT pin does not generate an interrupt, in order to avoid oscillatory behavior when battery supplement mode is set.

## INTERRUPT CONTROLLER – I<sup>2</sup>C REGISTERS

The I<sup>2</sup>C registers that control an interrupt generation (INT: HI→LO) are shown below. The HEX address for each register is shown by the register name, together with the R or W functionality for the register bits. Shaded values indicate default initial power-up values.

| INTERRUPT AND POWER GOOD FAULT MANAGEMENT REGISTERS |                                    |                                   |                                    |                                    |                                |                                    |                                      |                                      |
|-----------------------------------------------------|------------------------------------|-----------------------------------|------------------------------------|------------------------------------|--------------------------------|------------------------------------|--------------------------------------|--------------------------------------|
|                                                     | B7                                 | B6                                | B5                                 | B4                                 | B3                             | B2                                 | B1                                   | B0                                   |
| <b>INTMASK1, ADDRESS=03, ALL BITS R/W</b>           |                                    |                                   |                                    |                                    |                                |                                    |                                      |                                      |
| <b>Bit name</b>                                     | MASK_ISM1                          | MASK_ISM2                         | MASK_ISM3                          | MASK_ILDO1                         | MASK_ILDO2                     | MASK_ILDO3                         | MASK_ILDO4                           | MASK_ILDO5                           |
| <b>Function</b>                                     | MASK INT by SM1 PGOOD FAULT        | MASK INT by SM2 PGOOD FAULT       | MASK INT by SM3 PGOOD FAULT        | MASK INT by LDO1 PGOOD FAULT       | MASK INT by LDO2 PGOOD FAULT   | MASK INT by LDO3 PGOOD FAULT       | MASK INT by LDO4 PGOOD FAULT         | MASK INT by LDO5 PGOOD FAULT         |
| <b>When 0</b>                                       | UNMASKED                           | UNMASKED                          | UNMASKED                           | UNMASKED                           | UNMASKED                       | UNMASKED                           | UNMASKED                             | UNMASKED                             |
| <b>When 1</b>                                       | MASKED                             | MASKED                            | MASKED                             | MASKED                             | MASKED                         | MASKED                             | MASKED                               | MASKED                               |
| <b>INTMASK2, ADDRESS=04, ALL BITS R/W</b>           |                                    |                                   |                                    |                                    |                                |                                    |                                      |                                      |
| <b>Bit name</b>                                     | MASK_IADC                          | MASK_IANLG1                       | MASK_IGPIO2                        | MASK_IGPIO1                        | MASK_ITHSH UT                  | MASK_ICHG S T                      | MASK_IADC_H I                        | MASK_IADC_L O                        |
| <b>Function</b>                                     | MASKS INT BY ADC END OF CONVERSION | MASKS INT BY ANLG1 HIGH IMPEDANCE | MASKS INT BY GPIO2 EDGE TRANSITION | MASKS INT BY GPIO1 EDGE TRANSITION | MASKS INT BY THERMAL FAULT     | MASK INT BY CHG_STAT REGISTER BITS | MASK INT BY ADC INPUT ABOVE HI LIMIT | MASK INT BY ADC INPUT BELOW LO LIMIT |
| <b>When 0</b>                                       | UNMASKED                           | UNMASKED                          | UNMASKED                           | UNMASKED                           | UNMASKED                       | UNMASKED                           | UNMASKED                             | UNMASKED                             |
| <b>When 1</b>                                       | MASKED                             | MASKED                            | MASKED                             | MASKED                             | MASKED                         | MASKED                             | MASKED                               | MASKED                               |
| <b>INT_ACK1, ADDRESS=05, ALL BITS R/W</b>           |                                    |                                   |                                    |                                    |                                |                                    |                                      |                                      |
| <b>Bit name</b>                                     | ACK_SM1                            | ACK_SM2                           | ACK_SM3                            | ACK_LDO1                           | ACK_LDO2                       | ACK_LDO3                           | ACK_LDO4                             | ACK_LDO5                             |
| <b>Function</b>                                     | SM1 INT REQUEST                    | SM2 INT REQUEST                   | SM3 INT REQUEST                    | LDO1 INT REQUEST                   | LDO2 INT REQUEST               | LDO3 INT REQUEST                   | LDO4 INT REQUEST                     | LDO5 INT REQUEST                     |
| <b>When 0</b>                                       | CLEAR FLAG                         | CLEAR FLAG                        | CLEAR FLAG                         | CLEAR FLAG                         | CLEAR FLAG                     | CLEAR FLAG                         | CLEAR FLAG                           | CLEAR FLAG                           |
| <b>When 1</b>                                       | SM1 PGOOD FAULT GENERATED INT      | SM2 PGOOD FAULT GENERATED INT     | SM3 OVP FAULT GENERATED INT        | LDO1 PGOOD FAULT GENERATED INT     | LDO2 PGOOD FAULT GENERATED INT | LDO3 PGOOD FAULT GENERATED INT     | LDO4 PGOOD FAULT GENERATED INT       | LDO5 PGOOD FAULT GENERATED INT       |
| <b>INT_ACK2, ADDRESS=06, ALL BITS READ ONLY</b>     |                                    |                                   |                                    |                                    |                                |                                    |                                      |                                      |
| <b>Bit name</b>                                     | ACK_ADC                            | ACK_ANLG1                         | ACK_GPIO2                          | ACK_GPIO1                          | ACK_THSHUT                     | ACK_CHGSTA T                       | ACK_ADC_HI                           | ACK_ADC_LO                           |
| <b>Function</b>                                     | ADC INT REQUEST 1                  | ANLG1 COMPARATOR INT REQUEST      | GPIO2 INT REQUEST                  | GPIO1 INT REQUEST                  | THERMAL FAULT INT REQUEST      | CHARGER INT REQUEST                | ADC INT REQUEST 2                    | ADC INT REQUEST 3                    |
| <b>When 0</b>                                       | CLEAR FLAG                         | CLEAR FLAG                        | CLEAR FLAG                         | CLEAR FLAG                         | CLEAR FLAG                     | CLEAR FLAG                         | CLEAR FLAG                           | CLEAR FLAG                           |

| INTERRUPT AND POWER GOOD FAULT MANAGEMENT REGISTERS |                                |                                                      |                                  |                                  |                                     |                                             |                                                |                                                |
|-----------------------------------------------------|--------------------------------|------------------------------------------------------|----------------------------------|----------------------------------|-------------------------------------|---------------------------------------------|------------------------------------------------|------------------------------------------------|
|                                                     | B7                             | B6                                                   | B5                               | B4                               | B3                                  | B2                                          | B1                                             | B0                                             |
| <b>When 1</b>                                       | ADC DONE GENERATED INT REQUEST | ANLG1 HIGH IMPEDANCE DETECTION GENERATED INT REQUEST | GPIO2 EDGE GENERATED INT REQUEST | GPIO1 EDGE GENERATED INT REQUEST | THERMAL FAULT GENERATED INT REQUEST | CHARGER STATUS CHANGE GENERATED INT REQUEST | ADC INPUT ABOVE HI LIMIT GENERATED INT REQUEST | ADC INPUT BELOW LO LIMIT GENERATED INT REQUEST |
| <b>PGOODFAULT_MASK, ADDRESS=07, ALL BITS R/W</b>    |                                |                                                      |                                  |                                  |                                     |                                             |                                                |                                                |
| <b>Bit name</b>                                     | PGOOD SM1                      | PGOOD SM2                                            | PGOOD SM3                        | PGOOD LDO1                       | PGOOD LDO2                          | PGOOD LDO3                                  | PGOOD LDO4                                     | PGOOD LDO5                                     |
| <b>Function</b>                                     | MASK PGOOD FAULT BY SM1        | MASK PGOOD FAULT BY SM2                              | MASK PGOOD FAULT BY SM3          | MASK PGOOD FAULT BY LDO1         | MASK PGOOD FAULT BY LDO2            | MASK PGOOD FAULT BY LDO3                    | MASK PGOOD FAULT BY LDO4                       | MASK PGOOD FAULT BY LDO5                       |
| <b>When 0</b>                                       | UNMASKED                       | UNMASKED                                             | UNMASKED                         | UNMASKED                         | UNMASKED                            | UNMASKED                                    | UNMASKED                                       | UNMASKED                                       |
| <b>When 1</b>                                       | MASKED                         | MASKED                                               | MASKED                           | MASKED                           | MASKED                              | MASKED                                      | MASKED                                         | MASKED                                         |

## FUNCTIONALITY GUIDE — SYSTEM POWER AND CHARGE MANAGEMENT

| CHARGE MANAGEMENT                     |                                     |                     |                                    |                                           |                          |                   |                           |                  |
|---------------------------------------|-------------------------------------|---------------------|------------------------------------|-------------------------------------------|--------------------------|-------------------|---------------------------|------------------|
| Fast Charge <sup>(1)</sup>            |                                     | Precharge Current   | Termination                        |                                           | Charge Voltage           | Precharge Voltage | SafetyTimer Timeout       | Power Up Default |
| Charge Current Value                  | Charge Current Scaling              |                     | Current                            | Current Scaling                           |                          |                   |                           |                  |
| $I_{O(BAT)}$ , Programmable, 1.5A max | 25%, 50%, 75%, 100% of $I_{O(BAT)}$ | 10% of $I_{O(BAT)}$ | $I_{(TERM)}$ , 10% of $I_{O(BAT)}$ | 25%, 50%, 75%, 100% of $I_{(TERM)}$ value | 4.2 V or 4.36 V          | 3.0 V             | Programmable              | Charger ON       |
| Set via external resistor             | Set via I <sup>2</sup> C            | Fixed ratio         | Fixed ratio                        | Set via I <sup>2</sup> C                  | Set via I <sup>2</sup> C | Fixed             | Set via external resistor |                  |

(1) The input current limit (see system power management below ) regulates the input current, effectively limiting the charge current if the input current limit is lower than the fast charge current value programmed.

| POWER PATH MANAGEMENT        |                                       |                                                                                             |                                                               |                                                      |
|------------------------------|---------------------------------------|---------------------------------------------------------------------------------------------|---------------------------------------------------------------|------------------------------------------------------|
| INPUT CURRENT LIMIT          |                                       | INPUT CONNECTED TO OUT PIN                                                                  |                                                               | POWER UP DEFAULT                                     |
| AC PIN                       | USB PIN                               | INPUT POWER TO SYSTEM                                                                       | BATTERY TO SYSTEM                                             |                                                      |
| 2.5 A typ                    | 100 mA max or 500 mA max or 2.5 A typ | #1 – AC<br>#2 – USB<br>#3 – Battery (when AC pin power and USB pin power are not detected ) | Battery connected to system, independently of battery voltage | Input Power to System, USB mode selected, 100 mA max |
| Internal fixed current limit | Set via I <sup>2</sup> C              | Automatic internal algorithm                                                                | Set via I <sup>2</sup> C, overrides internal algorithm        |                                                      |

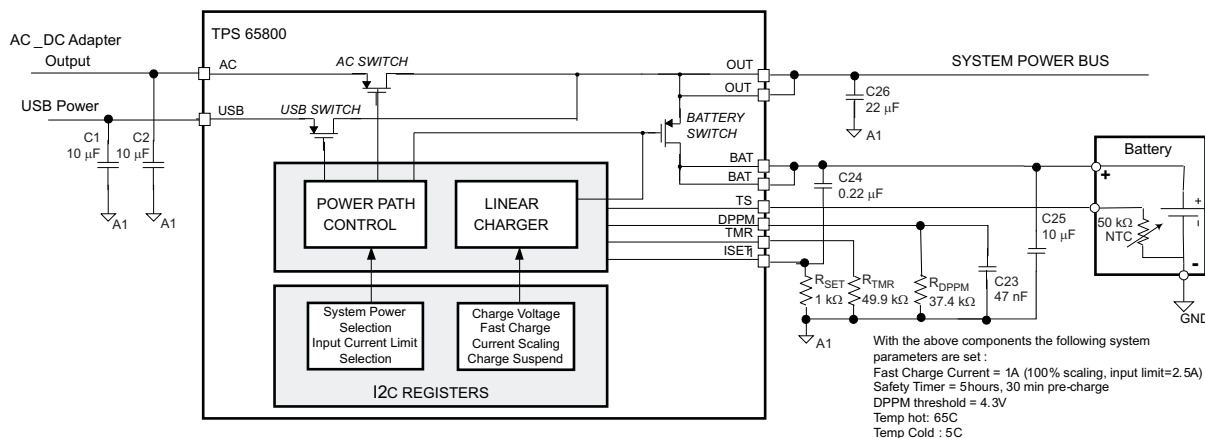


Figure 30. Required External Components, Recommended Values, External Connections

## POWER PATH AND CHARGE MANAGEMENT

### Overview

The TPS65800 has an integrated charger with power path integrated MOSFETs. This topology, shown in the simplified block diagram below, enables using an external input power to run the system and charge the battery simultaneously. The power path has dual inputs that can be used to select either an external AC\_DC adapter (AC pin) or an USB port power (USB pin) to power the end equipment main power rail (OUT pin, also referred to as the system power bus) and charge the battery pack (connected to BAT pin).

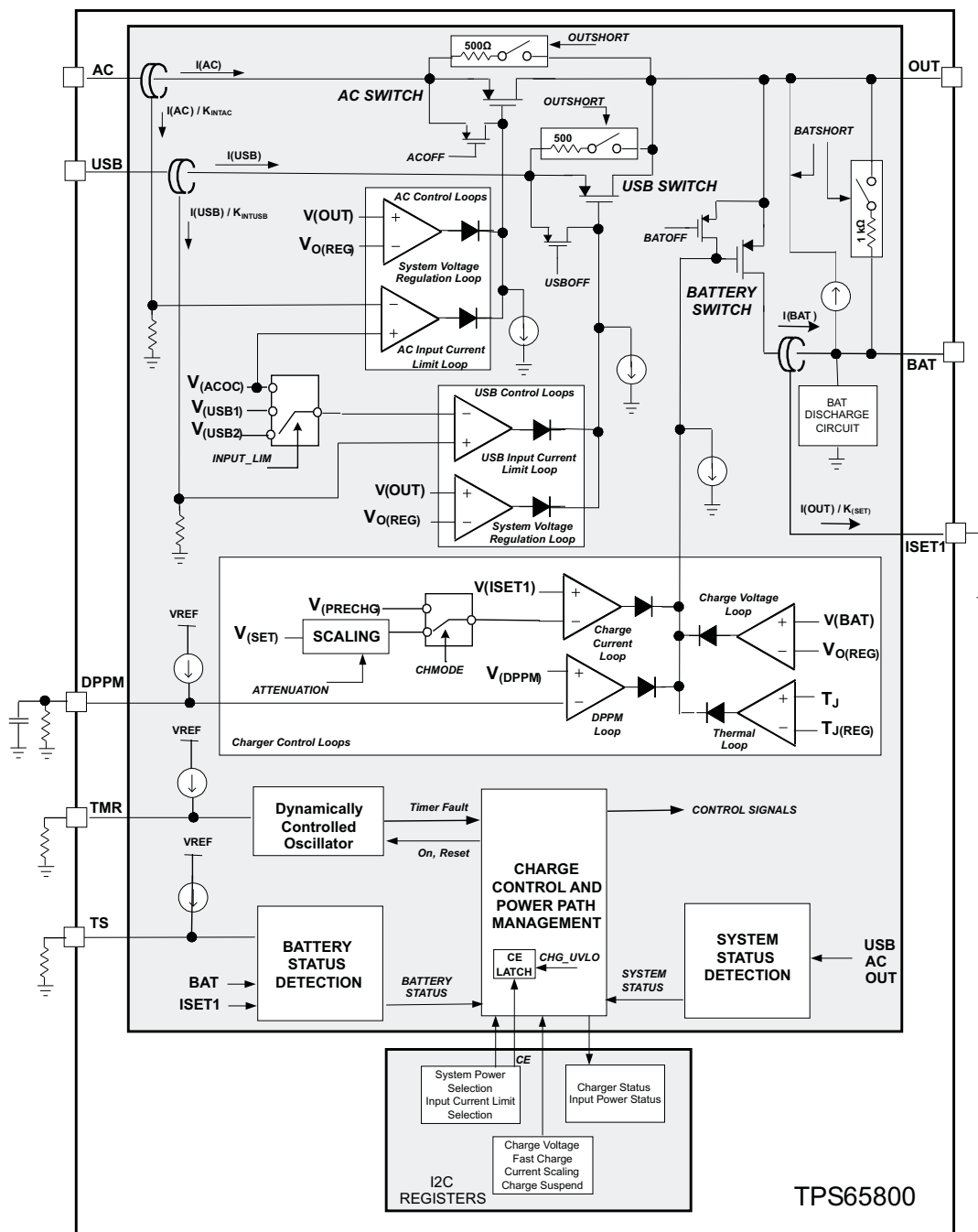


Figure 31. TPS65800 Charger and Power Path Section Simplified Block Diagram

The power path has three integrated power MOSFETs: the battery to system MOSFET (battery switch), the AC input to system MOSFET (AC switch) and the USB input to system MOSFET (USB switch). Each of those power MOSFETs can be operated either as an ON/OFF switch or as a linear pass element under distinct operating conditions, as defined by the control circuits that set the power MOSFET gate voltage.

The TPS65800 regulates the voltage at the OUT pin to 4.6 V when one of the external supplies connected to pins AC or USB is powering the OUT pin. The selected input (AC or USB pin) current is limited to a value defined by I<sup>2</sup>C register settings. The input current limit function assures compatibility with USB standard requirements, and also implements a protection function by limiting the maximum current supplied by an external AC\_DC adapter or USB port power terminal.

The AC power MOSFET and USB power MOSFET operating modes are set by integrated control loops. Each of the power MOSFETs is controlled by two loops: one system voltage regulation loop and one input current limiting loop. The integrated loops modulate the AC or USB power MOSFETs drain to source resistance to regulate either the OUT pin voltage or to limit the input current. If no input power is present (AC and USB input power not detected) the AC and USB power MOSFETs are turned OFF, and the battery MOSFET is turned ON, connecting the BAT pin to the OUT pin.

The battery switch is turned ON when the AC or USB input power is detected and the charger function is enabled, charging the battery pack. During charge the battery MOSFET switch operation mode is defined by the charger control loops. The battery MOSFET switch drain-to-source resistance is modulated by the charge current loop and charge voltage loop in order to implement the battery charging algorithm. In addition to that multiple safety functions are activated (thermal shutdown, safety timers, short circuit recovery), and additional functions (thermal loop and DPPM loop) optimize the charging process.

## POWER PATH MANAGEMENT FUNCTION

### Detecting the System Status

The power path and charge management block operate independently of the other TPS65800 circuits. Internal circuits check battery parameters (pack temperature, battery voltage, charge current) and system parameters (AC and USB voltage, battery voltage detection), setting the power path MOSFETs operating modes automatically. The TPS65800 has integrated comparators that monitor the battery voltage, AC pin voltage, USB pin voltage and the OUT pin voltage. The data generated by those comparators is used by the power path control logic to define which of the integrated power path switches is active. A simplified block diagram for the system status detection is shown below.

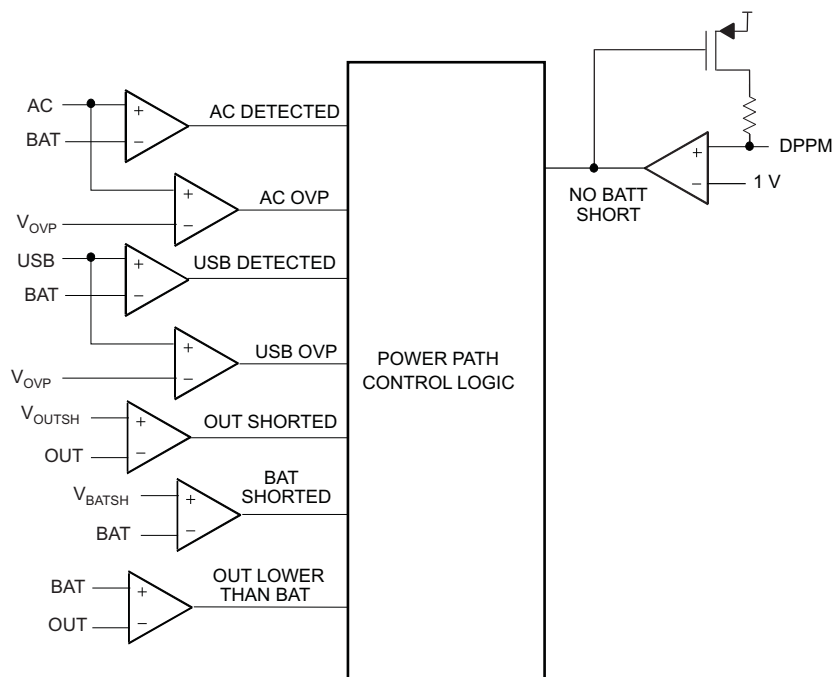


Figure 32. TPS65800 Systems Status Detection, Charger and Power Path Section

Table 4 lists the system power detection conditions.  $V_{IN(DT)}$ ,  $V_{OUTSH}$ ,  $V_{BATSH}$ ,  $V_{OVP}$  are TPS65800 internal references, refer to the electrical characteristics for additional details.

Table 4. System Status Detection, Charger and Power Path Section

|                                                    |                                  |
|----------------------------------------------------|----------------------------------|
| AC input voltage detected                          | $V(AC) - V(BAT) > V_{IN(DT)}$    |
| USB input voltage detected                         | $V(USB) - V(BAT) > V_{IN(DT)}$   |
| AC overvoltage detected                            | $V(AC) > V_{OVP}$                |
| USB overvoltage detected                           | $V(USB) > V_{OVP}$               |
| AC PIN TO OUT pin OR USB TO OUT PIN short detected | $V(OUT) < V_{INOUTSH}$           |
| BAT pin to OUT pin short detected                  | $V(BAT) - V(OUT) > V_{BATOUTSH}$ |
| Battery supplement mode need detected              | $V(BAT) - V(OUT) > V_{SUP}$      |
| Blank BAT to OUT short circuit detection           | $V(DPPM) < 1V$                   |

### Power Path Logic: Priority Algorithm

The system power bus supply is automatically selected by the power path control logic, following an internal algorithm. The power path function detects an external input power connection when the input voltage exceeds the battery pack voltage. It also detects a supplement mode need (battery switch must be turned ON) when the system voltage (OUT pin) is below the battery voltage. A connected and non-selected external supply or the battery is automatically switched to the system bus, following the priority algorithm, when the external supply currently selected is disconnected from the system.

The input power priority is hard-wired internally, with the AC input having the higher priority, followed by the USB input (2<sup>nd</sup>) and the battery pack (3<sup>rd</sup>). Using the I<sup>2</sup>C CHG\_CONFIG register control bit CE the user can override the power path algorithm, connecting the battery to the system power bus. Care must be taken when using the battery to system connection option, as the system power bus **is not** connected back to the AC or USB inputs (even if those are detected) when the battery is removed. Table 5 describes the priority algorithm.

**Table 5. Power Path Control Logic Priority Algorithm**

| CE BIT<br>(I <sup>2</sup> C CHG_CONFIG Register) | EXTERNAL SUPPLY<br>DETECTED |     | SWITCH MODE |     |                                                     | SYSTEM POWER<br>SOURCE |
|--------------------------------------------------|-----------------------------|-----|-------------|-----|-----------------------------------------------------|------------------------|
|                                                  | AC                          | USB | AC          | USB | Battery                                             |                        |
| HI                                               | YES                         | NO  | ON          | OFF | ON if Supplement mode is<br>required, OFF otherwise | AC                     |
|                                                  | NO                          | YES | OFF         | ON  |                                                     | USB                    |
|                                                  | YES                         | YES | ON          | OFF |                                                     | AC                     |
|                                                  | NO                          | NO  | OFF         | OFF |                                                     | BATTERY                |
| LO                                               | XX                          | XX  | OFF         | OFF | ON                                                  | BATTERY                |

The power path status is stored in register CHG\_STAT.

### Input Current Limit

The USB input current is limited to the maximum value programmed by the host, using the I<sup>2</sup>C interface. If the system current requirements exceed the input current limit, the output voltage collapses, the charge current is reduced, and finally the supplement mode is set. The input current limit value is set with the I<sup>2</sup>C charge control register bits PSEL and ISET2, and it is applied to the USB input ONLY. The AC input current limit is fixed to the internal short circuit limit value.

**Table 6. Charge Current Scaling via I<sup>2</sup>C**

| PSEL (I <sup>2</sup> C) | ISET2 (I <sup>2</sup> C) | INPUT CURRENT LIMIT |        |
|-------------------------|--------------------------|---------------------|--------|
|                         |                          | USB                 | AC     |
| LO                      | LO                       | 100 mA              | 2.75 A |
| LO                      | HI                       | 500 mA              | 2.75 A |
| HI                      | LO                       | 2.75 A              | 2.75 A |
| HI                      | HI                       | 2.75 A              | 2.75 A |

### System Voltage Regulation

The system voltage is regulated to a fixed voltage when one of the input power supplies is connected to the system. The system voltage regulation is implemented by a control loop that modulates the selected switch Rds(on).

The typical system regulation voltage is 4.6 V.

### Input Overvoltage Detection

The AC and USB input voltages are monitored by voltage comparators that identify an overvoltage condition. If an overvoltage condition is detected a status register bit is set, indicating a potential fault condition.

When an overvoltage condition is detected the AC or USB switches state is not modified. If any of those switches was ON, it is kept in the ON state. During overvoltage conditions, the system voltage still is regulated, and no major safety issues are observed when not modifying the input switch state.

If the input overvoltage condition results in excessive power dissipation, the thermal shutdown circuit is activated, the AC and USB switches are turned OFF, and the BAT switch is turned ON.

### Output Short-Circuit Detection

If the OUT pin voltage falls below an internal threshold  $V_{INOUTSH}$  the AC and USB switches are turned off and internal pullup resistors are connected from AC pin to OUT pin and USB pin to OUT pin. When the short circuit is removed those resistors enable the OUT pin voltage to rise above the  $V_{INOUTSH}$  threshold, returning the system to normal operation.

### Battery Short Circuit Detection

If the OUT pin voltage falls below the BAT pin voltage by more than an internal threshold  $V_{BATOUTSH}$  the battery switch is turned off and internal pullup resistor is connected between the OUT pin and the BAT pin. This resistor enables detection of the short removal, returning the system to normal operation.

## Boot-Up Algorithm

During the initial TPS65800 power-up the contents of the ISET2, CE and SUSPEND bits on the control register are ignored for a time period  $t_{BOOT}$ . During that time the charger is enabled, and the selected input current limit is set internally to 100 mA max. At the end of  $t_{BOOT}$  period the control register settings are implemented.

## No Battery Detection Circuit

The ANLG1 pin may be used to detect the connection of an external resistor that is embedded in a battery pack and is used as a pack ID function. The ANLG1 pin has an internal current source connected between OUT and ANLG1, which is enabled automatically when the TPS65800 is not in SLEEP mode. The current levels for ANLG1 pin can be programmed via I<sup>2</sup>C register ADC\_WAIT, bits BATID\_n, as shown below:

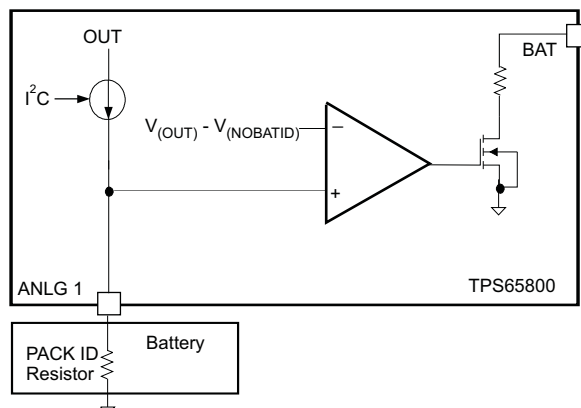


Figure 33. Battery Removal Detection, ANLG1 Pin

An internal comparator with a fixed deglitch time,  $t_{DGL(NO BAT)}$  monitors the ANLG1 pin voltage, if  $V(ANLG1) > V(OUT) - V_{NOBATID}$  a battery removed condition is detected and an internal discharge switch is activated, connecting an internal resistor from BAT pin to AGND1. Note that ANLG1 can also be used as an analog input for the ADC converter, in this case the voltage at pin ANLG1 must never exceed the  $V(OUT) - V_{NOBATID}$  threshold to avoid undesired battery discharge.

## Using the Input Power to Run the System and Charge the Battery Pack

The external supply connected to AC or USB pins must be capable of supplying the system power and the charger current. If the external supply power is not sufficient to run the system and charge the battery pack the TPS65800 executes a two-stage algorithm that prevents a low voltage condition at the system power bus:

1. The charge current is reduced, until the total (charger + system current) is at a level that can be supplied by the external input supply. This function is implemented by a dedicated charger control loop (see DPPM section in charger functional description for additional details).
2. The battery switch is turned ON if the charge current is reduced to zero and the input current is not enough to run the system. In this mode of operation both the battery and the external input power supply the system power ( supplement operation mode).

The supplement operation mode is automatically set by the TPS65800 when the input power is switched to the OUT pin, and the OUT pin voltage falls below the battery voltage.

## BATTERY CHARGE MANAGEMENT FUNCTION

### Operating Modes

The TPS65800 supports charging of single-cell Li-Ion or Li-Pol battery packs. The charge process is executed in three phases: precharge (or preconditioning), constant current and constant voltage.

The charge parameters are selectable via I<sup>2</sup>C interface and using external components. The charge process starts when an external input power is connected to the system, the charger is enabled by the I<sup>2</sup>C register CHG\_CONFIG bits CE=HI and CHGON=HI, and the battery voltage is below the recharge threshold,  $V_{(BAT)} < V_{(RCH)}$ . When the charge cycle starts a safety timer is activated. The safety timer timeout value is set by an external resistor connected to TMR pin.

When the charger is enabled two control loops modulate the battery switch drain to source impedance to limit the BAT pin current to the programmed charge current value (charge current loop) or to regulate the BAT pin voltage to the programmed charge voltage value (charge voltage loop). If  $V_{(BAT)} < 3\text{ V}$  (typ) the BAT pin current is internally set to 10% of the programmed charge current value. A typical charge profile is shown below, for an operation condition that does not cause the IC junction temperature to exceed 125°C (typ).

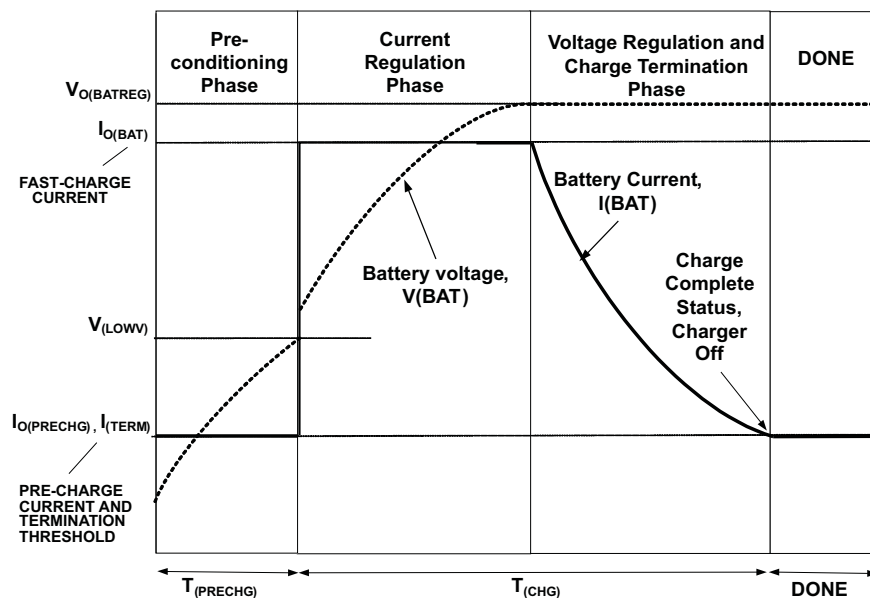
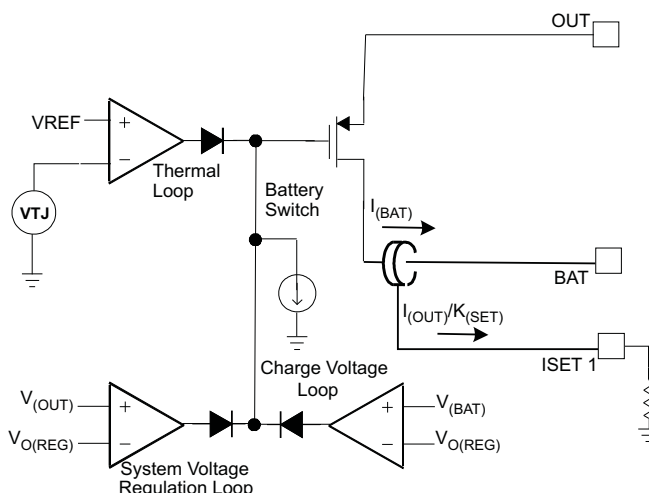


Figure 34. Typical Charge Cycle, Thermal Loop not Active

If the operating conditions cause the IC junction temperature to exceed 125°C the charge cycle is modified, with the activation of the integrated thermal control loop. The thermal control loop is activated when an internal voltage reference, which is inversely proportional to the IC junction temperature, is lower than a fixed, temperature stable internal voltage. The thermal loop overrides the other charger control loops and reduces the charge current until the IC junction temperature returns to 125°C, effectively regulating the IC junction temperature.





A modified charge cycle, with the thermal loop active, is shown here:

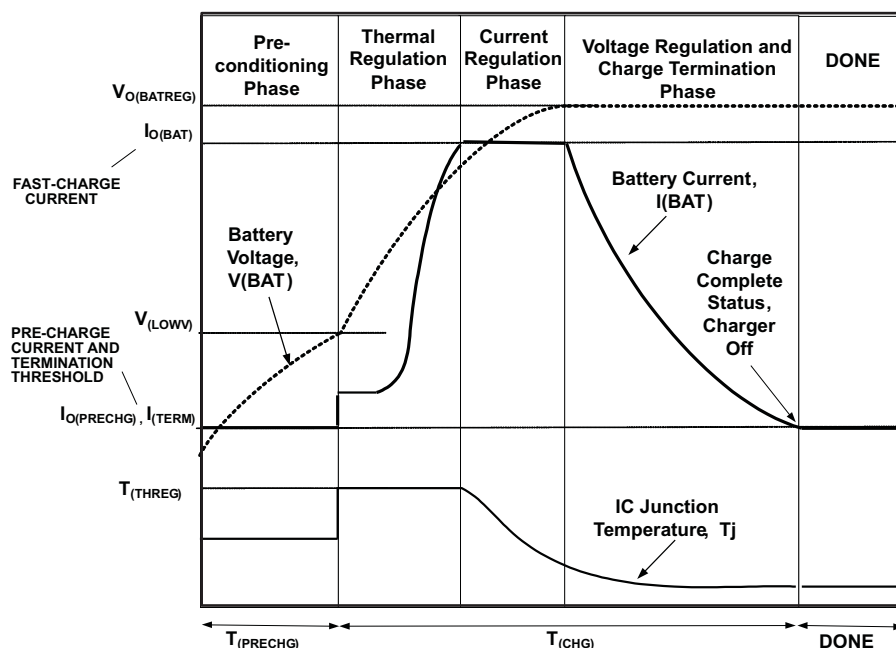


Figure 35. Typical Charge Cycle, Thermal Loop Active

### Battery Preconditioning

The TPS65800 applies a precharge current  $I_{O(PRECHG)}$  to the battery if the battery voltage is below the  $V_{(LOWV)}$  threshold, preconditioning deeply discharged cells. The charge current loop regulates the ISET1 pin voltage to an internal reference value,  $V_{PRECHG}$ . The resistor connected between the ISET1 and AGND pins,  $R_{SET}$ , determines the precharge rate.

The precharge rate programmed by  $R_{SET}$  is always applied to a deeply discharged battery pack, independently of the input power selection (AC or USB). The precharge current can be calculated as follows:

$$I_{O(PRECHG)} = \frac{V_{PRECHG} \times K_{SET}}{R_{SET}} \quad (2)$$

where:

$K_{SET}$  is the charge current scaling factor and  $V_{PRECHG}$  is the precharge set voltage.

### CONSTANT-CURRENT CHARGING

The constant charge current mode (fast charge) is set when the battery voltage is higher than the precharge voltage threshold. The charge current loop regulates the ISET1 pin voltage to an internal reference value,  $V_{SET}$ . The fast charge current regulation point is defined by the external resistor connected to the ISET1 pin,  $R_{SET}$ , as shown in the following:

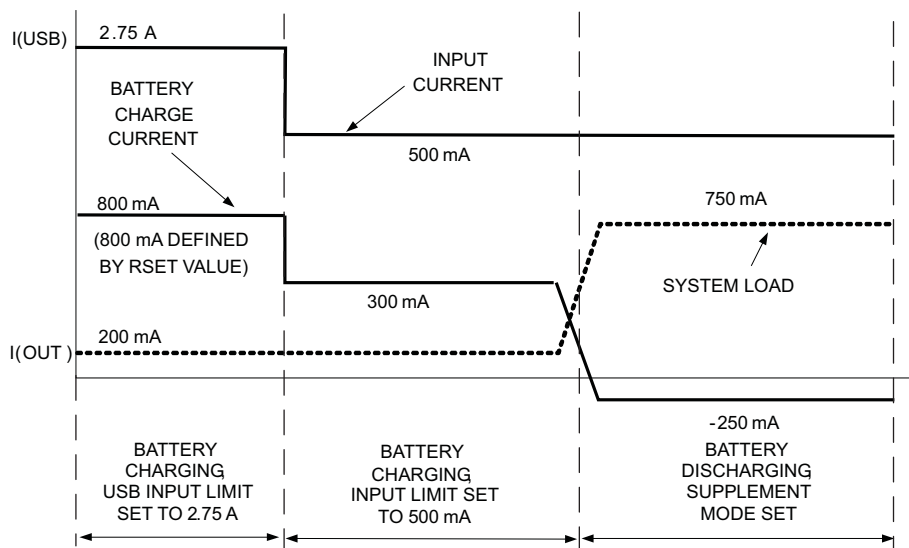
$$I_{O(BAT)} = \frac{V_{SET} \times K_{SET}}{R_{SET}} \quad (3)$$

where:

$V_{SET}$  (2.5 V typ) is the voltage at ISET1 pin during charge current regulation and  $K_{SET}$  = Charge Current Scaling Factor.

The reference voltage  $V_{SET}$  can be reduced via I<sup>2</sup>C register CHG\_CONFIG bits ISET1\_1 and ISET1\_0.  $V_{SET}$  can be selected as a percentage (75%, 50% or 25%) of the original 2.5 V typ, non-attenuated  $V_{SET}$  value, effectively scaling down the charge current.

The ISET1 resistor always sets the maximum charge current, if the AC input is selected. When the USB input is selected, the maximum charge current is defined by the USB input current limit and the programmed charge current. If the USB input current limit is lower than the  $I_{O(OUT)}$  value, the battery switch is set in the dropout region and the charge current is defined by the input current limit value and system load, as shown in the following curves:



**Figure 36. Input Current Limit Impact on Effective Charge Current**

## CHARGE TERMINATION AND RECHARGE

The TPS65800 monitors the charging current during the voltage regulation phase. Charge is terminated when the charge current is lower than an internal threshold, set to 10% (typ) of the fast charge current rate. The termination point applies to both AC and USB charging, and it can be calculated as follows:

$$I_{TERM} = \frac{V_{TERM} \times K_{SET}}{R_{SET}} \quad (4)$$

where

$V_{TERM}$  is the termination detection voltage reference.

The voltage at ISET1 pin is monitored to detect termination, and termination is detected when  $V(SET1) < V_{TERM}$  (0.25 V typ). The voltage reference  $V_{TERM}$  is internally set to 10% of the  $V_{SET}$  reference voltage, and it is modified if the reference voltage  $V_{SET}$  is scaled via I<sup>2</sup>C register CHG\_CONFIG bits ISET1\_1 and ISET1\_0.  $V_{TERM}$  is reduced by the same percentage used to scale down  $V_{SET}$ .

The table below shows charge current and termination thresholds for a 1-A charge current set (1-kΩ resistor connected to ISET1 pin), with the selected input current limit set to a value higher than the programmed charge current. The termination current is scaled for all charge current modes (AC or USB), as it is always set by the ISET1 pin external resistor value.

**Table 7. Charge Current and Termination Threshold Selection Example**

| Charge Control Register Bits |         | Charge Current, (% of typical value programmed by ISET1 resistor) | Vset (V) | Vterm (mV) | Charge Current (A) | Termination Current (mA) |
|------------------------------|---------|-------------------------------------------------------------------|----------|------------|--------------------|--------------------------|
| ISET1_1                      | ISET1_0 |                                                                   |          |            |                    |                          |
| 0                            | 0       | 25%                                                               | 0.6      | 60         | 0.24               | 20                       |
| 0                            | 1       | 50%                                                               | 1.25     | 115        | 0.5                | 40                       |
| 1                            | 0       | 75%                                                               | 1.9      | 160        | 0.78               | 60                       |
| 1                            | 1       | 100%                                                              | 2.5      | 250        | 1                  | 100                      |

Once termination is detected, a new charge cycle starts if the voltage on the BAT pin falls below the  $V_{(RCH)}$  threshold. A new charge start is also triggered if the charger is enabled/disabled/enabled via I<sup>2</sup>C (CHG\_CONFIG register bits CE or CHGON), or if both AC and USB input power are removed and then at least one of them is re-inserted.

The termination is disabled when the thermal loop OR DPPM loop are active, and during supplement mode.

## BATTERY VOLTAGE REGULATION, CHARGE VOLTAGE

The voltage regulation feedback is implemented by sensing the BAT pin voltage, which is connected to the positive side of the battery pack. The TPS65800 monitors the battery-pack voltage between the BAT and AGND1 pins, when the battery voltage rises to the  $V_{O(REG)}$  threshold the voltage regulation phase begins and the charging current tapers down.

The charging voltage can be selected as 4.2 V or 4.365 V (typ). The default power-up voltage is 4.2 V. As a safety measure the 4.365 V charge voltage is programmed only if two distinct bits are set via I<sup>2</sup>C: VCHG = HI in the CHG\_CONFIG, and CHG\_VLTG=LO in the GPIO3 register.

## TEMPERATURE QUALIFICATION

The TPS65800 continuously monitors battery temperature by measuring the voltage between the TS and AGND1 pins. An internal current source provides the bias for a negative-temperature coefficient thermistor (NTC), and the TS pin voltage is compared to the window set by internal thresholds  $V_{LTF}$  and  $V_{HTF}$  to determine if charging is allowed. A voltage outside the  $V_{LTF}$  to  $V_{HTF}$  window is considered a temperature fault, and charge is suspended. Charge resumes when the temperature returns to the valid window range.

With a 50-k $\Omega$  (at 25°C) thermistor, the valid temperature window is set between 0°C to 45°C. The temperature window can be enlarged by adding external resistors to the TS pin application circuit.

## DYNAMIC POWER PATH MANAGEMENT

Under normal operating conditions, the OUT pin voltage is regulated when the AC or USB pin is powering the OUT pin and the battery pack is being charged. If the total (system + charge current) exceeds the available input current, the system voltage drops below the regulation value.

The dynamic power path management function monitors the system output voltage. A condition where the external input supply rating has been exceeded or the input current limit has been reached is detected when the OUT pin voltage drops below an user-defined threshold,  $V_{DPPM}$ :

$$V_{DPPM} = R_{DPPM} \times K_{DPPM} \times I_{DPPM} \quad (5)$$

where:

$R_{DPPM}$  = external resistor connected to DPPM pin

$K_{DPPM}$  = DPPM scaling factor

$I_{DPPM}$  = DPPM pin internal current source

To correct this situation the DPPM loop reduces the charge current, regulating the OUT pin voltage to the user-defined  $V_{DPPM}$  threshold. The DPPM loop effectively identifies the maximum current that can be delivered by the selected input and dynamically adjusts the charge current to guarantee that the end equipment is always powered. In order to minimize OUT voltage ripple during DPPM operation the  $V_{DPPM}$  threshold should be set just below the system regulation voltage.

If the charge current is reduced to zero by the DPPM and the input current is still lower than the OUT pin load, the output voltage falls below the DPPM threshold, decreasing until the battery supplement mode is set [ $V(OUT) = V(BAT) - V_{SUP(DT)}$ ].

## CHARGER OFF MODE

The TPS65800 charger circuitry enters the low-power OFF mode if both AC and USB power are not detected. This feature prevents draining the battery during the absence of input supply.

## PRECHARGE SAFETY TIMER

The TPS65800 activates an internal safety timer during the battery preconditioning phase. The precharge safety timer time-out value is set by the external resistor connected to TMR pin, RTMR, and the timeout constants  $K_{PRE}$  and  $K_{TMR}$ :

$$T_{PRECHG} = K_{PRE} \times R_{TMR} \times K_{TMR}$$

The  $K_{PRE}$  constant typical value is 0.1, setting the precharge timer value to 10% of the charge safety timer value.

When the charger is in suspend mode, set via I<sup>2</sup>C register CHG\_CONFIG bit CHGON or set by a pack temperature fault, the precharge safety timer is put on hold (i.e., charge safety timer is not reset). Normal operation resumes when the charger exits the suspend mode. If V(BAT) does not reach the internal voltage threshold  $V_{PRECHG}$  within the precharge timer period a fault condition is detected and the charger is turned off.

If the TMR pin is left floating and internal resistor, 50K $\Omega$  typ, is used to generate the timebase used to set the precharge timeout value. The typical precharge timeout value can be then calculated as:

$$T_{PRECHG} = K_{PRE} \times 50K \times K_{TMR}$$

## CHARGE SAFETY TIMER

As a safety mechanism the TPS65800 has a user-programmable timer that measures the total fast charge time. This timer (charge safety timer) is started at the end of the preconditioning period. The safety charge timeout value is set by the value of an external resistor connected to the TMR pin ( $R_{TMR}$ ). The charge safety timer time-out value is calculated as follows:

$$T_{CHG} = K_{TMR} \times R_{TMR}$$

When the charger is in suspend mode, set via I<sup>2</sup>C register CHG\_CONFIG bit CHGON or set by a pack temperature fault, the charge safety timer is put on hold (i.e., charge safety timer is not reset). Normal operation resumes when the charger exits the suspend mode. If charge termination is not reached within the timer period a fault condition is detected, and the charger is turned off.

The charge safety timer is held in reset if the TMR pin is left floating. Under this mode of operation an internal resistor, 50K $\Omega$  typ, sets the internal charger and power path deglitch and delay times, as well as the precharge safety timer timeout value.

## TIMER FAULT RECOVERY

The TPS65800 provides a recovery method to deal with timer fault conditions. The following summarizes this method:

- Condition 1: Charge voltage above recharge threshold,  $V_{RCH}$ , and timeout fault occurs.

**Recovery method:** The IC waits for the battery voltage to fall below the recharge threshold. This could happen as a result of a load on the battery, self-discharge or battery removal. Once the battery falls below the recharge threshold, the IC clears the fault and starts a new charge cycle.

- Condition 2: Charge voltage below recharge threshold,  $V_{(RCH)}$ , and timeout fault occurs.

**Recovery method:** Under this scenario, the IC connects an internal pullup resistor from OUT pin to Bat pin. This pullup resistor is used to detect a battery removal condition and remains on as long as the battery voltage stays below the recharge threshold. If the battery voltage goes above the recharge threshold, the IC disables the pullup resistor connection and executes the recovery method described for condition 1.

All timers are reset and all timer fault conditions are cleared when a new charge cycle is started either via I<sup>2</sup>C (toggling CHG\_CONFIG bits CE, CHGON) or by cycling the input power. All timers are reset and all timer fault conditions are cleared when the TPS65800 enters the UVLO mode.

## DYNAMIC TIMER FUNCTION

The charge and precharge safety timers are programmed by the user to detect a fault condition if the charge cycle duration exceeds the total time expected under normal conditions. The expected total charge time is usually calculated based on the fast charge current rate.

When the thermal loop or the DPPM loops are activated the charge current is reduced, and a false safety timer fault can be observed if this mode of operation is active for a long periods. To avoid this undesirable fault condition the TPS65800 activates the dynamic timer function when the DPPM and thermal loops are active. The dynamic timer function slows down the safety timers clock, effectively adding an extra time to the programmed timeout value as follows:

1. If the battery voltage is below the battery depleted threshold: the precharge timer value is modified while the thermal loop or the DPPM loop are active
2. If the battery voltage is above the precharge threshold: the safety timer value is modified if the DPPM or the thermal loop are active AND the battery voltage is below the recharge threshold.

The TPS65800 dynamic timer function circuit monitors the voltage at pin ISET1 during precharge and fast charge. When the charger is regulating the charge current, the voltage at pin ISET1 is regulated by the control loops to either  $V_{SET}$  or  $V_{PRECHG}$ . If the thermal loop or DPPM loops are active, the voltage at pin ISET1 is lower than  $V_{SET}$  or  $V_{PRECHG}$ , and the dynamic timer control circuit changes the safety timers clock period based on the  $V_{SET}/V(ISET1)$  ratio (fast charge) or  $V_{PRECHG}/V(ISET1)$  ratio (precharge).

The maximum *clock period* is internally limited to twice the value of the programmed clock period, which is defined by the resistor connected to TMR pin, as shown in the following figure:

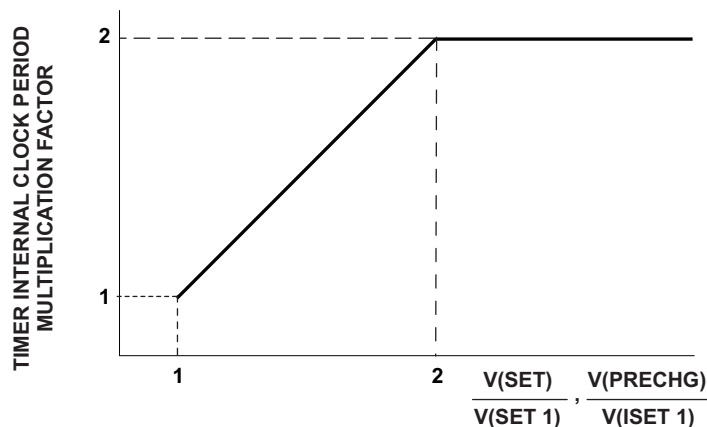


Figure 37. Safety Timer Internal Clock Slowdown

The effective charge safety timer value can then be expressed as follows:

$$\text{Effective precharge timeout} = t_{(PRECHG)} + t_{(PCHGADD)}$$

$$\text{Effective charge safety timeout} = t_{(CHG)} + t_{(CHGADD)}$$

Where the *added* timeout values,  $t_{(PCHGADD)}$ ,  $t_{(CHGADD)}$ , are equal to the sum of all time periods when either the thermal loop or DPPM loops were active. The *maximum added* timeout value is internally limited to  $2 \times t_{(CHG)}$  or  $2 \times t_{(PRECHG)}$

## CHARGE AND SYSTEM POWER MANAGEMENT — I<sup>2</sup>C REGISTERS

The I<sup>2</sup>C registers that control charger and power path related functions are shown below. The HEX address for each register is shown by the register name, together with the R or W functionality for the register bits. Shaded values indicate default initial power-up values. Note that the CHG\_STAT register contents are valid only when either AC or USB power are applied to the TPS65800. The output of linear regulator LDO\_PM can be used as an indicator of external input power detection; if LDO\_PM is in regulation the CHG\_STAT register contents are valid.

| CHG_CONFIG, ADDRESS=9, ALL BITS R/W |                          |                  |          |                                                                                                                     |          |                   |                                    |                                      |
|-------------------------------------|--------------------------|------------------|----------|---------------------------------------------------------------------------------------------------------------------|----------|-------------------|------------------------------------|--------------------------------------|
|                                     | B7                       | B6               | B5       | B4                                                                                                                  | B3       | B2                | B1                                 | B0                                   |
| Bit name                            | VCHG                     | CHGON            | NOT USED | ISSET1_1                                                                                                            | ISSET1_0 | ISSET2            | PSEL                               | CE <sup>(1)</sup>                    |
| Function                            | CHARGE VOLTAGE SELECTION | SUSPEND CHARGE   | NOT USED | CHARGE CURRENT SCALING FACTOR                                                                                       |          | USB CURRENT LIMIT | SELECTED INPUT CURRENT LIMIT       | SYSTEM POWER SELECTION               |
| When 0                              | 4.36 V                   | CHARGE SUSPENDED | NOT USED | 00= 0.25   10=0.75<br>01= 0.5   11= 1<br>Note: Relative to Charge Current Programmed by external ISET pin resistor. |          | 100 mA            | USE USB CURRENT LIMIT              | BATTERY TO SYSTEM                    |
| When 1                              | 4.2 V                    | CHARGE ON        | NOT USED |                                                                                                                     |          | 500 mA            | INPUT CURRENT LIMIT SET TO MAXIMUM | INPUT POWER TO SYSTEM <sup>(1)</sup> |

- (1) The CE bit state is latched inside the charger control logic (CE latch) during an OUT pin UVLO event, prior to resetting the charge control register bit CE to its power up default value. The charger CE latch controls the charger and power path state as long as the TPS65800 is in UVLO mode and an external supply is connected to the charger block. The CE latch is reset to its power-up value (CE=HI) only when the input power is removed from the charger block. The CE latch is disabled and the CE charge control register bit sets the charger and power path MOSFETs state when the TPS65800 exits the UVLO mode. This feature avoids a host software *loop* when the host algorithm requires a depleted (or absent) battery to be connected to the system bus while input power is present.

| GPIO3, ADDRESS = 1C, ALL BITS R/W. NOTE: ONLY BIT B4 CONTROLS CHARGER-RELATED FUNCTIONALITY. |                              |                              |                              |                                     |          |                              |                              |                              |
|----------------------------------------------------------------------------------------------|------------------------------|------------------------------|------------------------------|-------------------------------------|----------|------------------------------|------------------------------|------------------------------|
|                                                                                              | B7                           | B6                           | B5                           | B4                                  | B3       | B2                           | B1                           | B0                           |
| Bit name                                                                                     | GPIO3i/O                     | GPIO3_LEVEL                  | LDO0_ENABLE                  | CHARGE_VLTG                         | NOT USED | GPIO2_INTSRC                 | GPIO1_INTSRC                 | GPIO2_SM2                    |
| Function                                                                                     | SEE <a href="#">Table 15</a> | SEE <a href="#">Table 15</a> | SEE <a href="#">Table 15</a> | CHARGE VOLTAGE SELECTION SAFETY BIT | NOT USED | SEE <a href="#">Table 15</a> | SEE <a href="#">Table 15</a> | SEE <a href="#">Table 15</a> |
| When 0                                                                                       |                              |                              |                              | 4.2 V                               |          |                              |                              |                              |
| When 1                                                                                       |                              |                              |                              | 4.36 V                              |          |                              |                              |                              |

| CHG_STAT, ADDRESS = A, ALL BITS READ ONLY. POWER-UP DEFAULTS SHOW SYSTEM STATUS WHEN EXITING POWER DOWN. |                                |                             |                              |                       |                        |                                            |       |                               |
|----------------------------------------------------------------------------------------------------------|--------------------------------|-----------------------------|------------------------------|-----------------------|------------------------|--------------------------------------------|-------|-------------------------------|
|                                                                                                          | B7                             | B6                          | B5                           | B4                    | B3                     | B2                                         | B1    | B0                            |
| Bit name                                                                                                 | BAT_STAT <sup>(1)(2)</sup>     | INPUT_PWR                   | THDPPM_ON                    | ACPG <sup>(3)</sup>   | USBPG <sup>(3)</sup>   | STAT1                                      | STAT2 | INP_OV                        |
| Function                                                                                                 | BATTERY SUPPLEMENT MODE STATUS | SELECTED INPUT POWER STATUS | THERMAL LOOP AND DPPM STATUS | AC INPUT POWER STATUS | USB INPUT POWER STATUS | CHARGE STATUS                              |       | AC OR USB INPUT OVP DETECTION |
| When 0                                                                                                   | SUPPLEMENT MODE OFF            | AC INPUT SELECTED           | BOTH OFF                     | AC NOT DETECTED       | USB NOT DETECTED       | 00 = FAULT/OFF/SUSPEND<br>01 = CHARGE DONE |       | NO OVP                        |
| When 1                                                                                                   | SUPPLEMENT MODE ON             | USB INPUT SELECTED          | DPPM ON OR THERMAL ON        | AC DETECTED           | USB DETECTED           | 10 = FAST CHARGE ON<br>11 = PRECHARGE ON   |       | OVP DETECTED                  |

- (1) The battery supplement is entered when  $V_{(BAT)} - V_{(OUT)} > 60$  mV (typ), and it ends when  $V_{(BAT)} - V_{(OUT)} < 20$  mV. When the system power bus current exceeds the input current limit or the external supply current capability, the supplement mode is set. An oscillatory behavior for BAT\_STAT bit can happen if the battery switch dropout voltage is less than 20 mV (typ) when in supplement mode.
- (2) The BAT\_STAT is always masked internally, and does not generate interrupts.
- (3) The ACPG and USBPG bits have valid data only when  $V_{(LDO\_PM)} > 2.0$  V.

## FUNCTIONALITY GUIDE — LINEAR REGULATORS

| SELECTABLE OUTPUT VOLTAGE LDO |                               |                                   |                                              |                                 |             |       |                  |  |
|-------------------------------|-------------------------------|-----------------------------------|----------------------------------------------|---------------------------------|-------------|-------|------------------|--|
| Supply                        | ON/OFF Control                | Output Discharge Switch           | OUTPUT VOLTAGE (V), set via I <sup>2</sup> C |                                 | IO Max (mA) | Acc % | Power Up Default |  |
|                               |                               |                                   | # of Steps                                   | Available Values (V)            |             |       |                  |  |
| LDO1                          | Yes, set via I <sup>2</sup> C | Yes, enabled via I <sup>2</sup> C | 8                                            | 1.25/1.5/1.8/2.5/2.85/3/3.2/3.3 | 150         | 3     | ON, 2.85 V       |  |
| LDO2                          | Yes, set via I <sup>2</sup> C | Yes, enabled via I <sup>2</sup> C | 8                                            | 1.25/1.5/1.8/2.5/2.85/3/3.2/3.3 | 150         | 3     | ON, 3.3 V        |  |
| SIM                           | Yes, set via I <sup>2</sup> C | No                                | 2                                            | 1.8 / 3                         | 8           | 2     | OFF, 1.8 V       |  |

| PROGRAMMABLE OUTPUT VOLTAGE LDO |                               |                                   |                                              |            |          |             |       |                  |
|---------------------------------|-------------------------------|-----------------------------------|----------------------------------------------|------------|----------|-------------|-------|------------------|
| Supply                          | ON/OFF Control                | Output Discharge Switch           | OUTPUT VOLTAGE (V), set via I <sup>2</sup> C |            |          | IO Max (mA) | Acc % | Power Up Default |
|                                 |                               |                                   | Range                                        | # of Steps | Min Step |             |       |                  |
| LDO3                            | Yes, set via I <sup>2</sup> C | Yes, enabled via I <sup>2</sup> C | 1.224–4.46                                   | 128        | 25 mV    | 100         | 3     | ON, 1.25 V       |
| LDO4                            | Yes, set via I <sup>2</sup> C | Yes, enabled via I <sup>2</sup> C | 1.224–4.46                                   | 128        | 25 mV    | 100         | 3     | ON, 2.75 V       |
| LDO5                            | yes, set via I <sup>2</sup> C | Yes, enabled via I <sup>2</sup> C | 1.224–4.46                                   | 128        | 25 mV    | 100         | 3     | ON, 2.81 V       |

| FIXED OUTPUT VOLTAGE LDO'S |                           |                    |             |       |                                |
|----------------------------|---------------------------|--------------------|-------------|-------|--------------------------------|
| Supply                     | ON/OFF Control            | OUTPUT VOLTAGE (V) | IO Max (mA) | Acc % | Power Up Default               |
| RTC_OUT                    | Yes, via I <sup>2</sup> C | 3.1, fixed         | 8           | 5     | ON                             |
| LDC0                       |                           | 3.3, fixed         | 150         | 3     | OFF                            |
| LDO_PM                     | NO, enabled internally    | 3.3, fixed         | 20          | 5     | ON if AC or USB power detected |

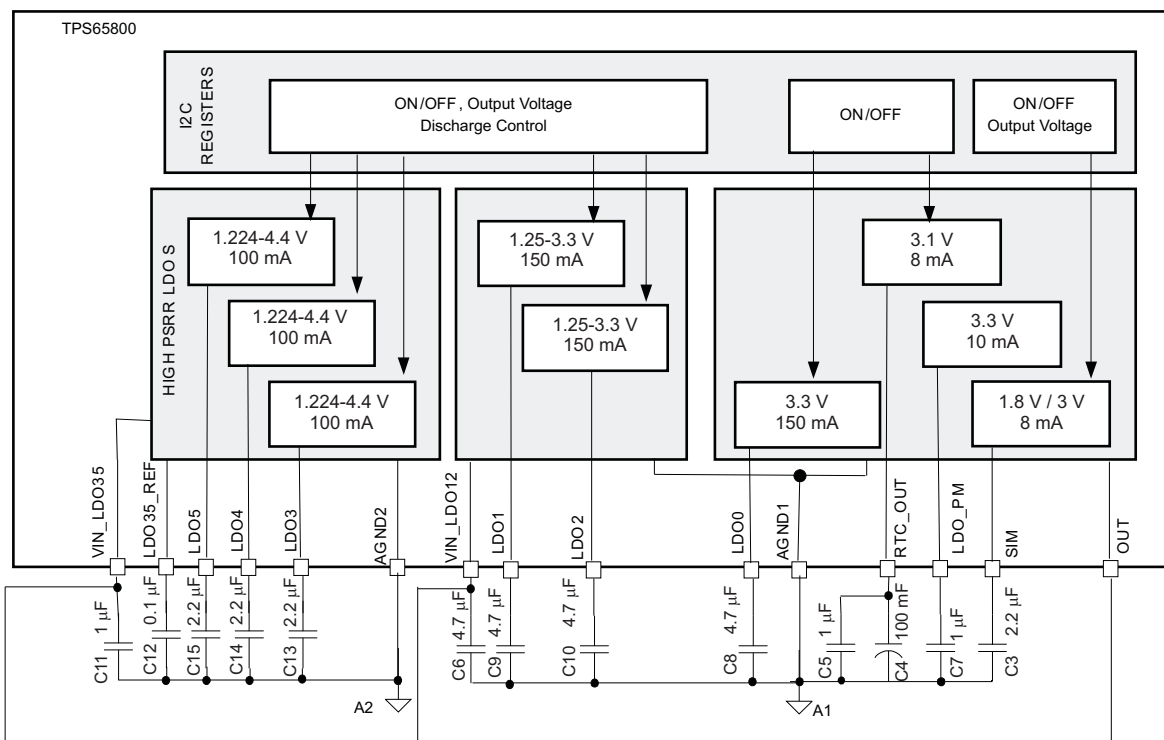


Figure 38. Required External Components, Recommended Values, External Connections



## LINEAR REGULATORS — FUNCTIONAL DESCRIPTION

The TPS65800 offers nine integrated linear regulators, designed to be stable over the operating load range with use of external ceramic capacitors, as long as the recommended filter capacitor values (see application diagram and pinout description) are used. The output voltage can be programmed via I<sup>2</sup>C (LDO0-2, LDO3-5) or have a fixed output voltage.

### Simplified Block Diagram

A simplified block diagram for the LDOs is shown in [Figure 39](#).

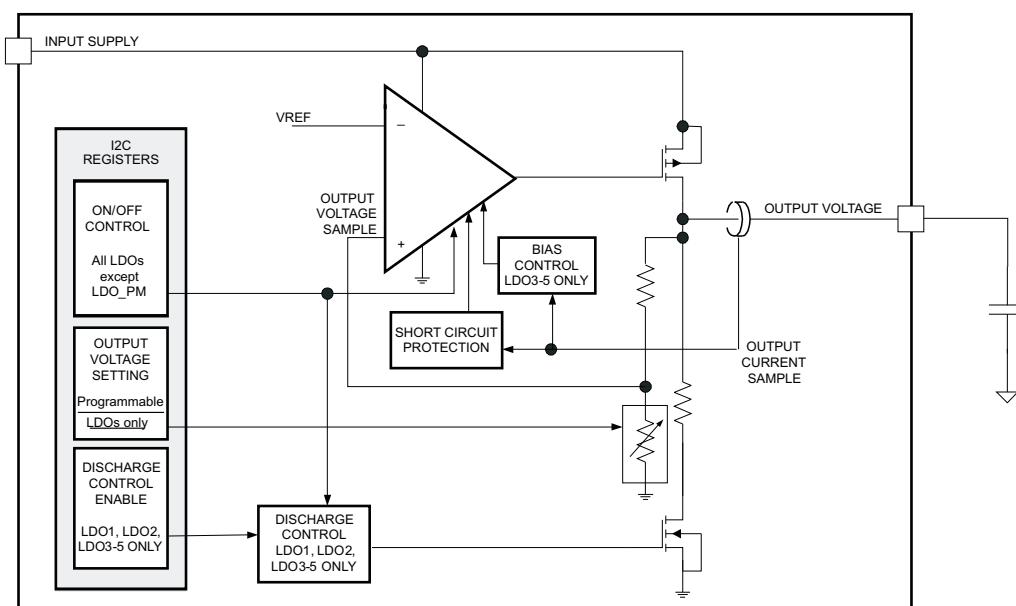


Figure 39. Simplified Block Diagram

### Connecting the LDO Input Supply

Both LDO1-2 and LDO3-5 have uncommitted input power supply pins (VIN\_LDO12, VIN\_LDO35), which should be externally connected to the OUT pin. Optionally the LDO0-2 and LDO3-5 input supplies can be connected to the output of the available buck converters SM1 or SM2, as long as the resulting overall power-up sequence meets the system requirements.

The RTC\_OUT, SIM, LDO0 and LDO\_PM linear regulators are internally connected to the OUT pin.

### ON/OFF Control

All the LDO's, with exception of LDO\_PM LDO, have a ON/OFF control which can be set via I<sup>2</sup>C commands, facilitating host management of the distinct system power rails. The LDO\_PM LDO On/OFF control is internally hard-wired, and it is set to ON when either the AC or USB input power is detected.

### Output Discharge Switch

LDO1, LDO2 AND LDO3-5 have integrated switches that discharge each output to ground when the LDO is set to OFF by an I<sup>2</sup>C command. The output discharge switch function can be disabled by using I<sup>2</sup>C register control bits. The discharge switches are enabled after the initial power-up

### Special Functions

The RTC\_OUT, SIM (Subscriber line interface module) and LDO\_PM linear regulators are designed to support lower load currents. The SIM and RTC\_LDO have low leakage in OFF mode, with the input pin voltage above or below the output pin voltage. The LDO\_PM can be used for USB enumeration, or a status indication of input power connection.



## Output Voltage Monitoring

Internal power good comparators monitor the LDO outputs and detect when the output voltage is below 90% of the programmed value. This information is used by the TPS65800 to generate interrupts or to trigger distinct operating modes, depending on specific I<sup>2</sup>C register settings. See interrupt and sequencing controller section for additional details.

## LINEAR REGULATORS — I<sup>2</sup>C REGISTERS

The I<sup>2</sup>C registers that control LDO-related functions are shown below. The HEX address for each register is shown by the register name, together with the R or W functionality for the register bits. Shaded values indicate default initial power-up values.

|                                                                                         | B7                                  | B6                                                                              | B5                                                   | B4                                                                | B3                                  | B2                                                         | B1                                                            | B0                     |
|-----------------------------------------------------------------------------------------|-------------------------------------|---------------------------------------------------------------------------------|------------------------------------------------------|-------------------------------------------------------------------|-------------------------------------|------------------------------------------------------------|---------------------------------------------------------------|------------------------|
| EN_LDO: ADDRESS = B, ALL BITS R/W                                                       |                                     |                                                                                 |                                                      |                                                                   |                                     |                                                            |                                                               |                        |
| Bit name                                                                                | LDO1_EN                             | LDO2_EN                                                                         | LDO3_EN                                              | LDO4_EN                                                           | LDO5_EN                             | SIM_SET                                                    | SIM_EN1                                                       | RTC_EN                 |
| Function                                                                                | LDO1...5 ON/OFF CONTROL             |                                                                                 |                                                      |                                                                   |                                     | SIM LDO output voltage                                     | SIM/RTC ON/OFF CONTROL                                        |                        |
| When 0                                                                                  | OFF                                 | OFF                                                                             | OFF                                                  | OFF                                                               | OFF                                 | 3.0 V                                                      | OFF                                                           | OFF                    |
| When 1                                                                                  | ON                                  | ON                                                                              | ON                                                   | ON                                                                | ON                                  | 1.80 V                                                     | ON                                                            | ON                     |
| LDO12: ADDRESS = C, ALL BITS R/W                                                        |                                     |                                                                                 |                                                      |                                                                   |                                     |                                                            |                                                               |                        |
| Bit name                                                                                | LDO1_DISCH                          | LDO1_2 SET                                                                      | LDO1_1 SET                                           | LDO1_0 SET                                                        | LDO2_DISCH                          | LDO2_2 SET                                                 | LDO2_1 SET                                                    | LDO2_0 SET             |
| Function                                                                                | LDO1 output discharge switch enable | LDO1 OUTPUT VOLTAGE SETTING                                                     |                                                      |                                                                   | LDO2 Output discharge switch enable | LDO2 OUTPUT VOLTAGE SETTING                                |                                                               |                        |
| When 0                                                                                  | OFF                                 | 000 = 1.25 V<br>010 = 1.8 V<br><b>100 = 2.85 V</b><br>110 = 3.2 V               | 001 = 1.5 V<br>011 = 2.5 V<br>110 = 3 V<br>111 = 3.3 | <b>Default = 2.85 V</b>                                           | OFF                                 | 000 = 1.25 V<br>010 = 1.8 V<br>100 = 2.85 V<br>110 = 3.2 V | 001 = 1.5 V<br>011 = 2.5 V<br>110 = 3 V<br><b>111 = 3.3 V</b> | <b>Default = 3.3 V</b> |
| When 1                                                                                  | ON                                  |                                                                                 |                                                      |                                                                   | ON                                  |                                                            |                                                               |                        |
| LDO3, ADDRESS = D, ALL BITS R/W                                                         |                                     |                                                                                 |                                                      |                                                                   |                                     |                                                            |                                                               |                        |
| Bit name                                                                                | LDO3_DISCH                          | LDO3_6 SET                                                                      | LDO3_5 SET                                           | LDO3_4 SET                                                        | LDO3_3 SET                          | LDO3_2 SET                                                 | LDO3_1 SET                                                    | LDO3_0 SET             |
| Function                                                                                | LDO3 output discharge switch enable | LDO3 OUTPUT VOLTAGE SETTING                                                     |                                                      |                                                                   |                                     |                                                            |                                                               |                        |
| When 0                                                                                  | OFF                                 | SeeTable 8 for LDO3-5 output voltage setting, <b>power-up default = 1.25 V</b>  |                                                      |                                                                   |                                     |                                                            |                                                               |                        |
| When 1                                                                                  | ON                                  |                                                                                 |                                                      |                                                                   |                                     |                                                            |                                                               |                        |
| LDO4, ADDRESS = E, ALL BITS R/W                                                         |                                     |                                                                                 |                                                      |                                                                   |                                     |                                                            |                                                               |                        |
| Bit name                                                                                | LDO4_DISCH                          | LDO4_6 SET                                                                      | LDO4_5 SET                                           | LDO4_4 SET                                                        | LDO4_3 SET                          | LDO4_2 SET                                                 | LDO4_1 SET                                                    | LDO4_0 SET             |
| Function                                                                                | LDO4 output discharge switch enable | LDO4 OUTPUT VOLTAGE SETTING                                                     |                                                      |                                                                   |                                     |                                                            |                                                               |                        |
| When 0                                                                                  | OFF                                 | See Table 8 for LDO3-5 output voltage setting, <b>power-up default = 2.75 V</b> |                                                      |                                                                   |                                     |                                                            |                                                               |                        |
| When 1                                                                                  | ON                                  |                                                                                 |                                                      |                                                                   |                                     |                                                            |                                                               |                        |
| LDO5, ADDRESS = F, ALL BITS R/W                                                         |                                     |                                                                                 |                                                      |                                                                   |                                     |                                                            |                                                               |                        |
| Bit name                                                                                | LDO5_DISCH                          | LDO5_6 SET                                                                      | LDO5_5 SET                                           | LDO5_4 SET                                                        | LDO5_3 SET                          | LDO5_2 SET                                                 | LDO5_1 SET                                                    | LDO5_0 SET             |
| Function                                                                                | LDO5 output discharge switch enable | LDO5 OUTPUT VOLTAGE SETTING                                                     |                                                      |                                                                   |                                     |                                                            |                                                               |                        |
| When 0                                                                                  | OFF                                 | See Table 8 for LDO3-5 output voltage setting, <b>power-up default = 2.81 V</b> |                                                      |                                                                   |                                     |                                                            |                                                               |                        |
| When 1                                                                                  | ON                                  |                                                                                 |                                                      |                                                                   |                                     |                                                            |                                                               |                        |
| GPIO3, ADDRESS = 1C, ALL BITS R/W. NOTE: ONLY BIT B5 CONTROLS LDO-RELATED FUNCTIONALITY |                                     |                                                                                 |                                                      |                                                                   |                                     |                                                            |                                                               |                        |
| Bit name                                                                                | GPIO3i/O                            | GPIO3 LEVEL                                                                     | LDO0 ENABLE                                          | CHARGE_VLTG                                                       | NOT USED                            | GPIO2_INTSRC                                               | GPIO1_INTSRC                                                  | GPIO2_SM2              |
| Function                                                                                | SEE Table 15                        | SEE Table 15                                                                    | LDO0 ON/OFF CONTROL                                  | SEE CHARGER SECTION<br>Battery Voltage Regulation, Charge Voltage | NOT USED                            | SEE Table 15                                               | SEE Table 15                                                  | SEE Table 15           |
| When 0                                                                                  |                                     |                                                                                 | LDO0 OFF                                             |                                                                   |                                     |                                                            |                                                               |                        |
| When 1                                                                                  |                                     |                                                                                 | LDO0 ON                                              |                                                                   |                                     |                                                            |                                                               |                        |

**Table 8. LDO 3–5 Programming Step Values**

| Step | B6–B0    | Vset  | Step | B6–B0    | Vset  | Step | B6–B0    | Vset  | Step | B6–B0    | Vset  |
|------|----------|-------|------|----------|-------|------|----------|-------|------|----------|-------|
| 0    | 000 0000 | 1.224 | 32   | 010 0000 | 2.040 | 64   | 100 0000 | 2.015 | 96   | 110 0000 | 2.856 |
| 1    | 000 0001 | 1.250 | 33   | 010 0001 | 2.066 | 65   | 100 0001 | 2.040 | 97   | 110 0001 | 2.882 |
| 2    | 000 0010 | 1.275 | 34   | 010 0010 | 2.091 | 66   | 100 0010 | 2.907 | 98   | 110 0010 | 3.723 |
| 3    | 000 0011 | 1.301 | 35   | 010 0011 | 2.117 | 67   | 100 0011 | 2.933 | 99   | 110 0011 | 3.749 |
| 4    | 000 0100 | 1.326 | 36   | 010 0100 | 2.142 | 68   | 100 0100 | 2.958 | 100  | 110 0100 | 3.774 |
| 5    | 000 0101 | 1.352 | 37   | 010 0101 | 2.168 | 69   | 100 0101 | 2.984 | 101  | 110 0101 | 3.800 |
| 6    | 000 0110 | 1.377 | 38   | 010 0110 | 2.193 | 70   | 100 0110 | 3.009 | 102  | 110 0110 | 3.825 |
| 7    | 000 0111 | 1.403 | 39   | 010 0111 | 2.219 | 71   | 100 0111 | 3.035 | 103  | 110 0111 | 3.851 |
| 8    | 000 1000 | 1.428 | 40   | 010 1000 | 2.244 | 72   | 100 1000 | 3.060 | 104  | 110 1000 | 3.876 |
| 9    | 000 1001 | 1.454 | 41   | 010 1001 | 2.270 | 73   | 100 1001 | 3.086 | 105  | 110 1001 | 3.902 |
| 10   | 000 1010 | 1.479 | 42   | 010 1010 | 2.295 | 74   | 100 1010 | 3.111 | 106  | 110 1010 | 3.927 |
| 11   | 000 1011 | 1.505 | 43   | 010 1011 | 2.321 | 75   | 100 1011 | 3.137 | 107  | 110 1011 | 3.953 |
| 12   | 000 1100 | 1.530 | 44   | 010 1100 | 2.346 | 76   | 100 1100 | 3.162 | 108  | 110 1100 | 3.978 |
| 13   | 000 1101 | 1.556 | 45   | 010 1101 | 2.372 | 77   | 100 1101 | 3.188 | 109  | 110 1101 | 4.004 |
| 14   | 000 1110 | 1.581 | 46   | 010 1110 | 2.397 | 78   | 100 1110 | 3.213 | 110  | 110 1110 | 4.029 |
| 15   | 000 1111 | 1.607 | 47   | 010 1111 | 2.423 | 79   | 100 1111 | 3.239 | 111  | 110 1111 | 4.055 |
| 16   | 001 0000 | 1.632 | 48   | 011 0000 | 2.448 | 80   | 101 0000 | 3.264 | 112  | 111 0000 | 4.080 |
| 17   | 001 0001 | 1.658 | 49   | 011 0001 | 2.474 | 81   | 101 0001 | 3.290 | 113  | 111 0001 | 4.106 |
| 18   | 001 0010 | 1.683 | 50   | 011 0010 | 2.499 | 82   | 101 0010 | 3.315 | 114  | 111 0010 | 4.131 |
| 19   | 001 0011 | 1.709 | 51   | 011 0011 | 2.525 | 83   | 101 0011 | 3.341 | 115  | 111 0011 | 4.157 |
| 20   | 001 0100 | 1.734 | 52   | 011 0100 | 2.550 | 84   | 101 0100 | 3.366 | 116  | 111 0100 | 4.182 |
| 21   | 001 0101 | 1.760 | 53   | 011 0101 | 2.576 | 85   | 101 0101 | 3.392 | 117  | 111 0101 | 4.208 |
| 22   | 001 0110 | 1.785 | 54   | 011 0110 | 2.601 | 86   | 101 0110 | 3.417 | 118  | 111 0110 | 4.233 |
| 23   | 001 0111 | 1.811 | 55   | 011 0111 | 2.627 | 87   | 101 0111 | 3.443 | 119  | 111 0111 | 4.259 |
| 24   | 001 1000 | 1.836 | 56   | 011 1000 | 2.652 | 88   | 101 1000 | 3.468 | 120  | 111 1000 | 4.284 |
| 25   | 001 1001 | 1.862 | 57   | 011 1001 | 2.678 | 89   | 101 1001 | 3.494 | 121  | 111 1001 | 4.310 |
| 26   | 001 1010 | 1.887 | 58   | 011 1010 | 2.703 | 90   | 101 1010 | 3.519 | 122  | 111 1010 | 4.335 |
| 27   | 001 1011 | 1.913 | 59   | 011 1011 | 2.729 | 91   | 101 1011 | 3.545 | 123  | 111 1011 | 4.361 |
| 28   | 001 1100 | 1.938 | 60   | 011 1100 | 2.754 | 92   | 101 1100 | 3.570 | 124  | 111 1100 | 4.386 |
| 29   | 001 1101 | 1.964 | 61   | 011 1101 | 2.780 | 93   | 101 1101 | 3.596 | 125  | 111 1101 | 4.412 |
| 30   | 001 1110 | 1.989 | 62   | 011 1110 | 2.805 | 94   | 101 1110 | 3.621 | 126  | 111 1110 | 4.437 |
| 31   | 001 1111 | 2.015 | 63   | 011 1111 | 2.831 | 95   | 101 1111 | 3.647 | 127  | 111 1111 | 4.463 |

## FUNCTIONALITY GUIDE — SWITCHED MODE STEP-DOWN CONVERTERS

| BUCK CONVERTERS, I <sup>2</sup> C PROGRAMMABLE OUTPUT VOLTAGE |                                                    |                                                        |                                                                                            |            |          |         |             |                                                                      |                                            |            |          |                                                             |
|---------------------------------------------------------------|----------------------------------------------------|--------------------------------------------------------|--------------------------------------------------------------------------------------------|------------|----------|---------|-------------|----------------------------------------------------------------------|--------------------------------------------|------------|----------|-------------------------------------------------------------|
| Supply                                                        | PFM Mode                                           | Standby Mode                                           | OUTPUT VOLTAGE (V), Set via I <sup>2</sup> C, Separate Settings for Normal or Standby Mode |            |          |         | IO Max (mA) | PWM Freq and Phase                                                   | SLEW RATE, mV/μS, Set via I <sup>2</sup> C |            |          | Power Up Default                                            |
|                                                               |                                                    |                                                        | Range                                                                                      | # of Steps | Min Step | Acc (%) |             |                                                                      | Range                                      | # of Steps | Min Step |                                                             |
| SM1                                                           | PFM/PWM with automatic mode selection or PWM only. | Standby mode with distinct voltage available           | 0.6-1.8                                                                                    | 32         | 40 mV    | 3       | 600         | 1.5MHz, 0°                                                           | 0, 0.24 to 15.36                           | 8          | 0.24     | ON, skip mode off, PWM only, 1.24 V(on/sby), 15.36mV/μS     |
| SM2                                                           | Mode of operation set via I <sup>2</sup> C         | Standby mode set via I <sup>2</sup> C or with GPIO pin | 1.0-3.4                                                                                    | 32         | 80mV     | 3       | 600         | 1.5MHz, 0/90/180 270°, with respect to SM1, set via I <sup>2</sup> C | 0, 0.48-30.72                              | 8          | 0.48     | ON, skip mode on, PWM/PFM, 1.8 V (on/sby), 180°, 30.72mV/μS |

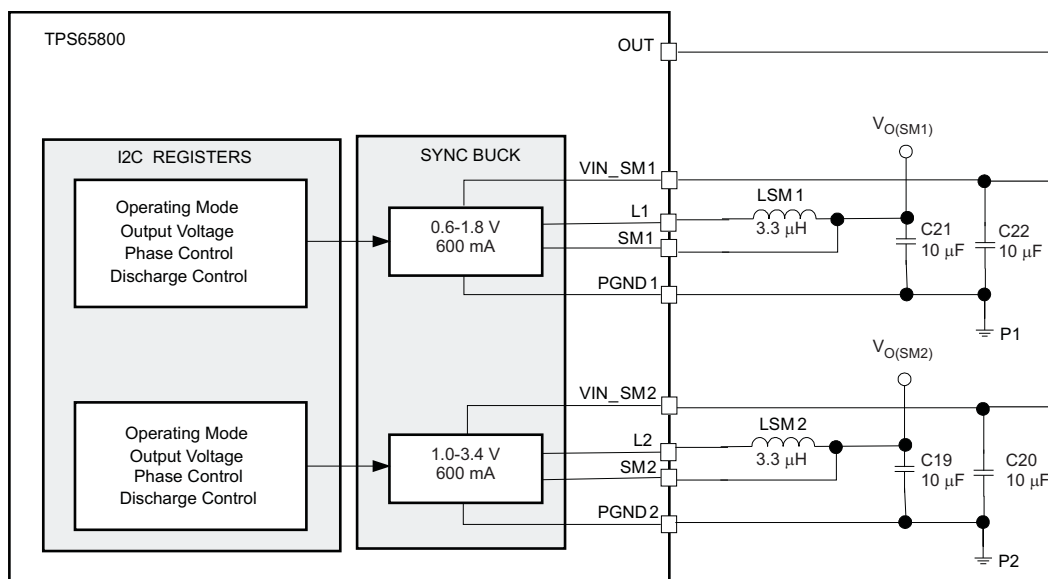


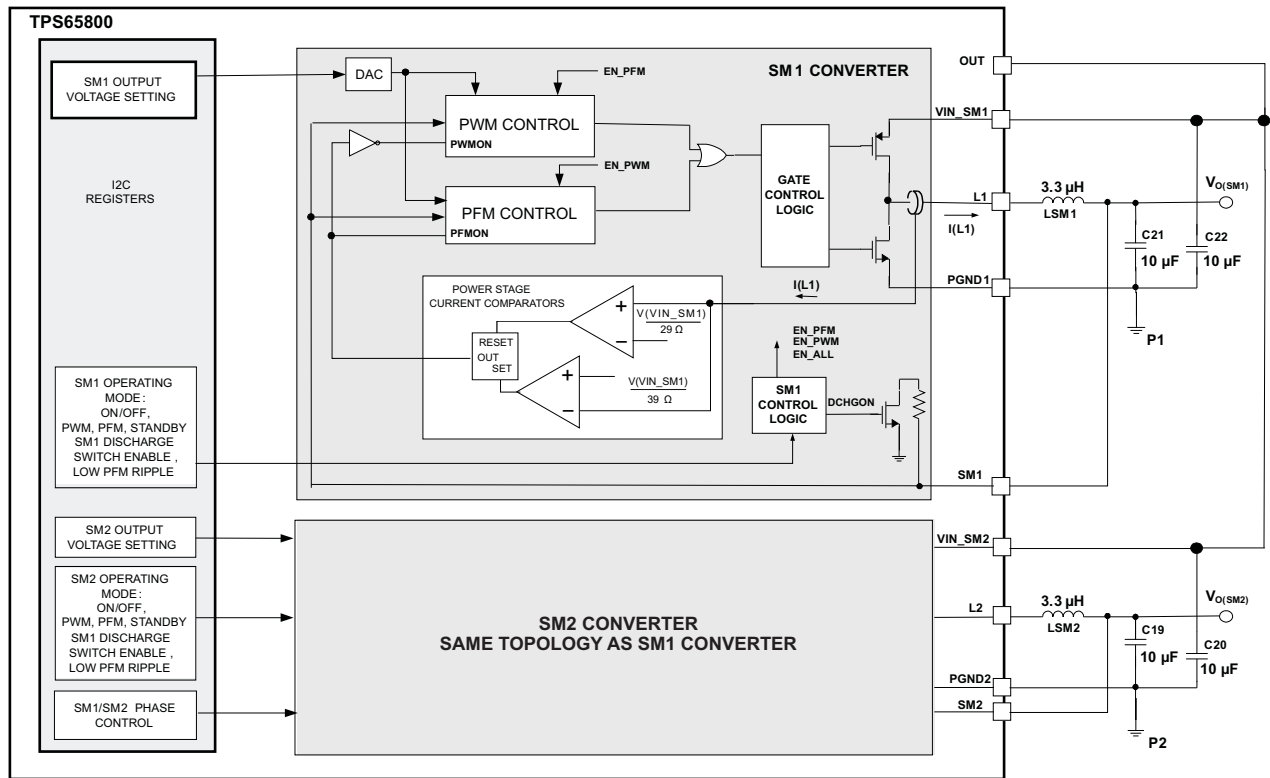
Figure 40. Required External Components, Recommended Values, External Connections

### STEP-DOWN SWITCHED MODE CONVERTERS: SM1 and SM2

The TPS65800 has two highly efficient step down synchronous converters. The integration of the power stage switching MOSFETs reduces the external component count, and only the external output inductor and filter capacitor are required. The integrated power stage supports 100% duty cycle operation. Multiple operation modes are available, enabling optimization of the overall system performance under distinct load conditions.

The converters have two modes of operation: a 1.5 MHz fixed frequency pulse width modulation (PWM) mode at moderate to heavy loads, and a pulse frequency modulation (PFM) mode at light loads. The converter output voltage is programmable via I<sup>2</sup>C registers SM1\_SET1 and SM2\_SET1.

When the SM1/SM2 converters are disabled an integrated switch automatically discharges the converter output capacitor. The discharge switch function can be disabled by setting the control bits DISCHSM1 and DISCHSM2 to LO, in I<sup>2</sup>C registers SM1\_SET2 and SM2\_SET2.



**Figure 41. SM1/SM2 Converter**

The TPS65800 SM1 and SM2 buck converters can be set to operate only in PWM mode or to switch automatically between PFM and PWM modes. The average load current is monitored, and the PFM mode is set if the average load current is below the threshold  $I_{PFM(ENTER)}$ . When in PFM mode the load current is also monitored, and the PWM mode is set when the load current exceeds the threshold  $I_{PFM(LEAVE)}$ . The thresholds for automatic PFM/PWM switching are calculated as shown in Equation 6 for the SM1 converter, the same thresholds apply to the SM2 converter by replacing  $VIN\_SM1$  by  $VIN\_SM2$ :

$$I_{PFM(LEAVE)} = \frac{V(VIN\_SM3)}{29\ \Omega}, \quad I_{PFM(ENTER)} = \frac{V(VIN\_SM3)}{39\ \Omega} \quad (6)$$

The automatic switching mode is enabled via the control bits PFM\_SM1 and PFM\_SM2 on I<sup>2</sup>C registers SM1\_SET1 and SM2\_SET1.

### Output Voltage Slew Rate

I<sup>2</sup>C registers enable setting the output voltage slew rate, when transitioning from one programmed voltage to a new programmed voltage value. These events can be triggered by a new output voltage selection or by switching from a low power mode (standby) to a normal operating mode. During a transition, the output voltage is stepped from the currently programmed voltage to the new target voltage. The slew rate from the initial voltage to the final voltage can be selected using I<sup>2</sup>C registers, SM1\_SET2 and SM2\_SET2, ranging from 0.24 mV/μs to 15.36 mV/μs for the SM1 converter and 0.48 to 30.72 mV/μs for the SM2 converter. If the slew rate is set to OFF, the output voltage goes from the current value to the programmed value in a single step.

During the transition to standby mode the Power Good comparators are disabled.

## Soft Start

SM1 and SM2 have an internal soft start circuit that limits the inrush current during start-up. An initial delay (170  $\mu$ s typ) from the converter enabled command to the converter effectively being operational is required, to assure that the internal circuits of the converter are properly biased. At the end of that initial delay the soft start is initiated, and the internal compensation capacitor is charged with a low value current source. The soft start time is typically 750  $\mu$ s, with the output voltage ramping from 5% to 95% of the final target value.

## Dropout Operation at 100% Duty Cycle

The TPS65800 buck converters offer a low input to output voltage difference while still maintaining operation when the duty cycle is set to 100%. In this mode of operation the P-channel switch is constantly turned on, enabling operation with a low input voltage. Dropout operation starts if:

$$V(VIN\_SM1) \leq V(SM1) + I(L1)(R_{DS(on)(PSM1)} + R_L) \quad (7)$$

Where:

$I(L1)$  = Output current plus inductor ripple current.

$R_L$  = DC resistance of the inductor

Equation 7 can be also used for the SM2 converter, replacing SM1 by SM2 and L1 by L2.

## Output Voltage Monitoring

The output voltage of converters SM1 and SM2 is monitored by internal comparators, and an output low voltage condition is detected when the output voltage is below 90% of the programmed value. The power good status for SM1 and SM2 is accessible via I<sup>2</sup>C, see interrupt controller section for more details.

The power good comparators for SM1 and SM2 are disabled during the transition to standby mode operation. They are enabled when the transition to standby mode is complete.

## Standby Mode

Using the I<sup>2</sup>C SM1 and SM2 can be set in stand-by mode. In STANDBY mode the PFM operation mode is set and the output voltage is defined by I<sup>2</sup>C registers SM1\_STANDBY and SM2\_STANDBY, and it can be set to a value different than the normal mode output regulation voltage. The standby mode can also be set by the GPIO pins, if those are configured as control pins that define the SM1/SM2 operating mode.

## PWM Operation

During PWM operation the converters use a fast response voltage mode controller scheme with input voltage feed-forward, enabling the use of small ceramic input and output capacitors. At the beginning of each clock cycle the P-channel MOSFET switch is turned on, and the oscillator starts the voltage ramp. The inductor current ramps up until the ramp voltage reaches the error amplifier output voltage, when the comparator trips and the p-channel MOSFET switch is turned off. Internal adaptive break-before-make circuits turn on the integrated n-channel MOSFET switch after an internal, fixed dead-time delay, and the inductor current ramps down, until the next cycle is started. When the next cycle starts the ramp voltage is reset to its low value and the p-channel MOSFET switch is turned on again.

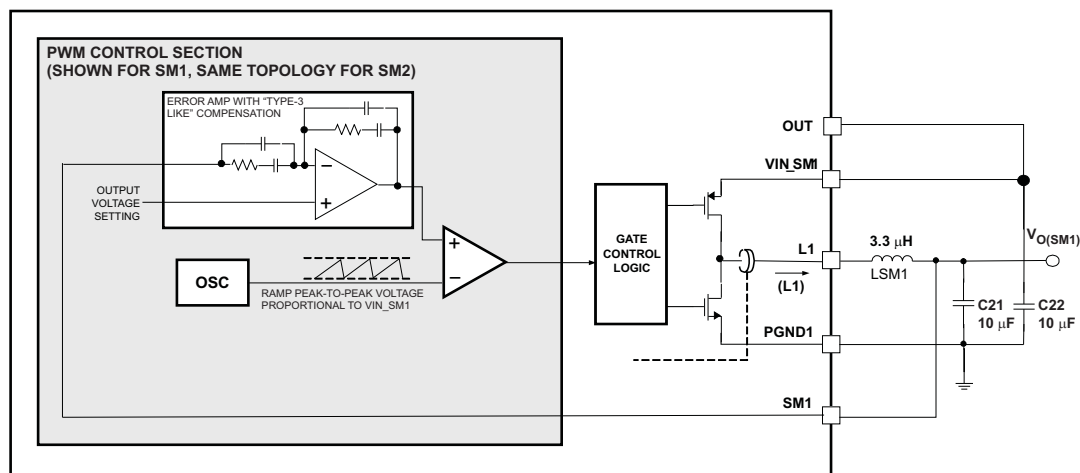


Figure 42. PWM Operation

The integrated power MOSFETs current is monitored at all times and the power MOSFET is turned off if its internal short circuit current limit is reached.

### Phase Control in PWM Mode

The SM1 and SM2 converters operate synchronized to each other when both are in PWM mode, with converter SM1 as the master. I<sup>2</sup>C control register bits S1S2PHASE in register SM1\_SET2 enables delaying the SM2 PWM clock with respect to SM1 PWM clock, selecting a phase shift from 0 to 270 degrees. The out-of-phase operation reduces the average current at the input node, enabling use of smaller input filter capacitors when both converters are connected to the same input supply.

### PFM Mode Operation

Using the I<sup>2</sup>C interface the SM1 and SM2 converters can have the automatic power saving PFM mode enabled. When the PFM mode is set the switching frequency is reduced and the internal bias currents are decreased, optimizing the converter efficiency under light load conditions.

In PFM mode the output voltage is monitored by a voltage comparator, which regulates the output voltage to the programmed value  $V_{O(SM1)}$ . If the output voltage is below  $V_{O(SM1)}$  the PFM control circuit turns on the power stage, applying a burst of pulses to increase the output voltage. When the output voltage exceeds the target regulation voltage  $V_{O(SM1)}$ , the power stage is disabled, and the output voltage drops until it is below the regulation voltage target, when the power stage is enabled again.

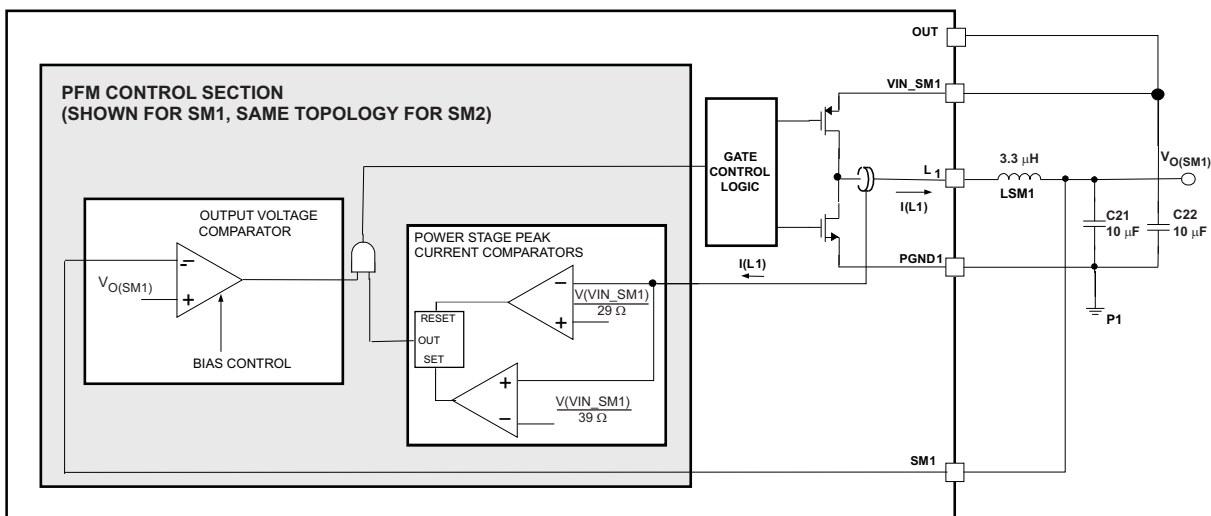


Figure 43. PFM Mode Operation

During burst operation two current comparators control the power stage integrated MOSFETs. These comparators monitor the instantaneous inductor current and compare it to the internal thresholds  $I_{PFM(ENTER)}$  and  $I_{PFM(LEAVE)}$ , turning the p-channel switch on if the inductor current is less than  $I_{PFM(LEAVE)}$  and turning it off if the inductor current exceeds  $I_{PFM(ENTER)}$ . The n-channel switch is turned on when the p-channel MOSFET is off.

The PFM output voltage comparator quiescent current may be reduced using the I<sup>2</sup>C register bits PFM\_RPL1 and PFM\_RPL2 in registers SM1\_SET and SM2\_SET. The voltage comparator quiescent current is reduced if PFM\_RPL1 and PFM\_RPL2 bits are set to LO, and the comparator response time ( $t_{COMP}$ , see Figure 44) increases. A reduction in quiescent current increases the converter efficiency at light loads, at the expense of a larger output voltage ripple when in PFM mode.

The ripple is minimized if PFM\_RPL1 and PFM\_RPL2 bits are set to HI, at the expense of reduced efficiency under light loads. The operation under low and high ripple settings is described in Figure 44.

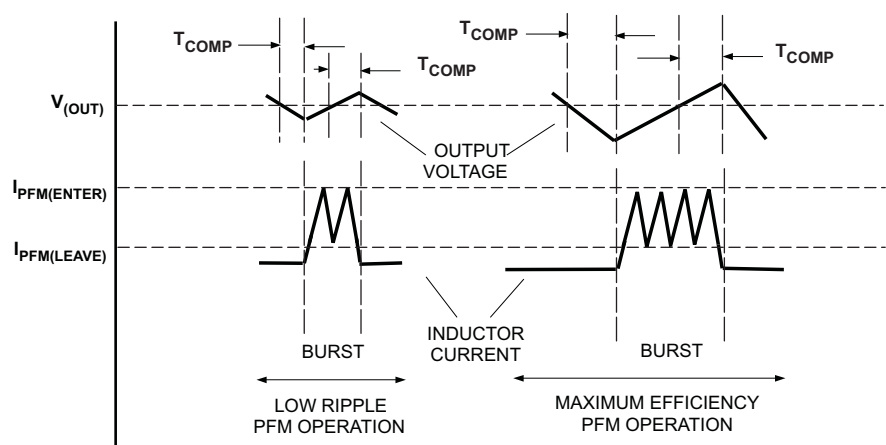
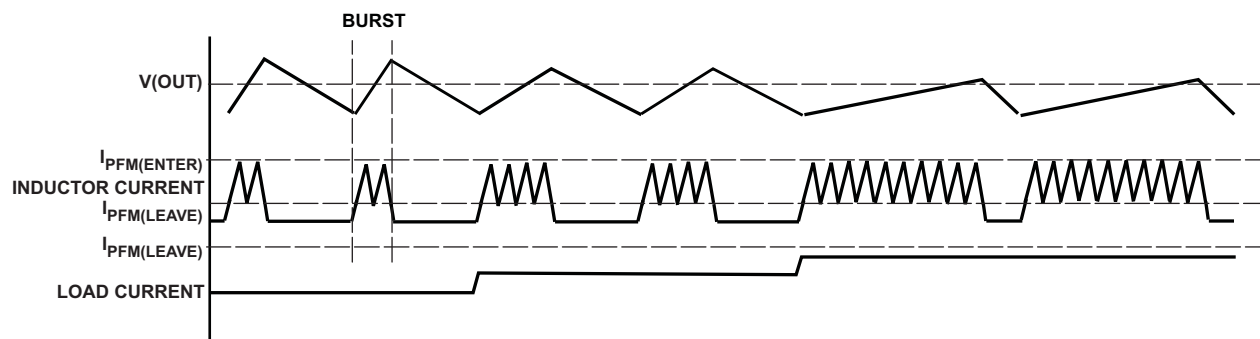


Figure 44. PFM mode operation waveforms

When a burst of pulses is generated, the PFM current comparators control the power stage MOSFETs to limit the inductor current to a value between the thresholds  $I_{PFM(LEAVE)}$  and  $I_{PFM(ENTER)}$ . The number of pulses in a burst cycle is proportional to the load current, and the average current is always below  $I_{PFM(LEAVE)}$  once PFM operation is set. The typical burst operation in PFM mode is shown in Figure 45.



**Figure 45. Typical Burst Operation in PFM Mode**

The PFM operation is disabled and PWM operation set if one of the following events happen during PFM operation:

1. The total burst operation time exceeds 10  $\mu$ s, typ.
2. The output voltage falls below 2% of the target regulation voltage.

The PFM mode can be disabled through the serial interface to force the individual converters to stay in fixed frequency PWM mode.



## SWITCHED MODE STEP-DOWN CONVERTERS — I<sup>2</sup>C REGISTERS

The I<sup>2</sup>C registers that control buck converter-related functions are shown below. The HEX address for each register is shown by the register name, together with the R or W functionality for the register bits. Shaded values indicate default initial power-up values.

|                                                     | B7                 | B6                         | B5                                 | B4                                                                                       | B3          | B2                                                                                                                                                            | B1          | B0          |
|-----------------------------------------------------|--------------------|----------------------------|------------------------------------|------------------------------------------------------------------------------------------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|-------------|
| SM1_SET1, ADDRESS=10, ALL BITS R/W                  |                    |                            |                                    |                                                                                          |             |                                                                                                                                                               |             |             |
| Bit name                                            | SM1 EN             | PFM_RPL1                   | PFM_SM1                            | SetV4_SM1                                                                                | SetV3_SM1   | SetV2_SM1                                                                                                                                                     | SetV1_SM1   | SetV0_SM1   |
| Function                                            | SM1 ON/OFF CONTROL | SM1 PFM FUNCTION OPERATION | SM1 PFM MODE ON/OFF CTRL           | SM1 OUTPUT VOLTAGE REGULATION VALUE, STANDBY MODE NOT SET                                |             |                                                                                                                                                               |             |             |
| When 0                                              | OFF                | MAXIMIZE EFFICIENCY        | PWM/PFM                            | See <a href="#">Table 9</a> for SM1, SM2 voltage setting, <b>Power up default=1.24 V</b> |             |                                                                                                                                                               |             |             |
| When 1                                              | ON                 | MINIMIZE OUTPUT RIPPLE     | Only PWM                           |                                                                                          |             |                                                                                                                                                               |             |             |
| SM1_SET2, ADDRESS=11, ALL BITS R/W                  |                    |                            |                                    |                                                                                          |             |                                                                                                                                                               |             |             |
| Bit name                                            | NOT USED           | STANDBY_SM1                | DISCHSM1                           | S1S2PHASE_1                                                                              | S1S2PHASE_0 | SLEWSM1_2                                                                                                                                                     | SLEWSM1_1   | SLEWSM1_0   |
| Function                                            | NOT USED           | SM1 STANDBY MODE ON        | SM1 output discharge switch enable | SM2 PWM CLOCK DELAY, WITH RESPECT TO SM1 PWM CLOCK                                       |             | SM1 OUTPUT SLEW RATE SETTING                                                                                                                                  |             |             |
| When 0                                              | NOT USED           | OFF                        | OFF                                | 00 = 0 <b>10 = 180</b><br>01 = 90    11 = 270<br>Units: degrees <b>Default= 180</b>      |             | 000 = 0.24    010 = 0.96    100 = 5.84 <b>110 = 15.36</b><br>001 = 0.48    011 = 1.92    101 = 7.68    111 = IMMEDIATE<br>Unit: mV/μs <b>Default= 15.36</b>   |             |             |
| When 1                                              | NOT USED           | ON                         | ON                                 |                                                                                          |             |                                                                                                                                                               |             |             |
| SM1_STANDBY, ADDRESS=12, B4-B0 R/W, B7-B5 READ ONLY |                    |                            |                                    |                                                                                          |             |                                                                                                                                                               |             |             |
| Bit name                                            | NOT USED           | NOT USED                   | NOT USED                           | SetV4_SM1SL                                                                              | SetV3_SM1SL | SetV2_SM1SL                                                                                                                                                   | SetV1_SM1SL | SetV0_SM1SL |
| Function                                            | NOT USED           | NOT USED                   | NOT USED                           | SM1 OUTPUT VOLTAGE REGULATION VALUE, STANDBY MODE SET                                    |             |                                                                                                                                                               |             |             |
| When 0                                              | NOT USED           | NOT USED                   | NOT USED                           | See <a href="#">Table 9</a> for SM1, SM2 voltage setting, <b>Power up default=1.24 V</b> |             |                                                                                                                                                               |             |             |
| When 1                                              | NOT USED           | NOT USED                   | NOT USED                           |                                                                                          |             |                                                                                                                                                               |             |             |
| SM2_SET1, ADDRESS=13, ALL REGISTER BITS R/W         |                    |                            |                                    |                                                                                          |             |                                                                                                                                                               |             |             |
| Bit name                                            | SM2 EN             | PFM_RPL2                   | PFM_SM2                            | SetV4_SM2                                                                                | SetV3_SM2   | SetV2_SM2                                                                                                                                                     | SetV1_SM2   | SetV0_SM2   |
| Function                                            | SM2 ON/OFF CONTROL | SM2 PFM FUNCTION OPERATION | SM2 PFM MODE ON/OFF CTRL           | SM2 OUTPUT VOLTAGE REGULATION VALUE, STANDBY MODE NOT SET                                |             |                                                                                                                                                               |             |             |
| When 0                                              | OFF                | MAXIMIZE EFFICIENCY        | PWM/PFM                            | See <a href="#">Table 9</a> for SM1, SM2 voltage setting, <b>Power up default=1.80 V</b> |             |                                                                                                                                                               |             |             |
| When 1                                              | ON                 | MINIMIZE OUTPUT RIPPLE     | ONLY PWM                           |                                                                                          |             |                                                                                                                                                               |             |             |
| SM2_SET2, ADDRESS=14, ALL REGISTER BITS R/W         |                    |                            |                                    |                                                                                          |             |                                                                                                                                                               |             |             |
| Bit name                                            | NOT USED           | STANDBY_SM2                | DISCHSM2                           | NOT USED                                                                                 | NOT USED    | SLEWSM2_2                                                                                                                                                     | SLEWSM2_1   | SLEWSM2_0   |
| Function                                            | NOT USED           | SM2 STANDBY MODE ON        | SM2 output discharge switch enable | NOT USED                                                                                 | NOT USED    | SM2 OUTPUT SLEW RATE SETTING                                                                                                                                  |             |             |
| When 0                                              | NOT USED           | OFF                        | OFF                                | NOT USED                                                                                 | NOT USED    | 000 = 0.48    010 = 1.92    100 = 7.68<br><b>110 = 30.72</b> 001 = 0.096    011 = 3.84<br>101 = 15.36    111 = IMMEDIATE<br>Unit: mV/μs <b>Default= 30.72</b> |             |             |
| When 1                                              | NOT USED           | ON                         | ON                                 | NOT USED                                                                                 | NOT USED    |                                                                                                                                                               |             |             |
| SM2_STANDBY, ADDRESS=15, ALL REGISTER BITS R/W      |                    |                            |                                    |                                                                                          |             |                                                                                                                                                               |             |             |
| Bit name                                            | NOT USED           | NOT USED                   | NOT USED                           | SetV4_SM2SL                                                                              | SetV3_SM2SL | SetV2_SM2SL                                                                                                                                                   | SetV1_SM2SL | SetV0_SM2SL |
| Function                                            | NOT USED           | NOT USED                   | NOT USED                           | SM1 OUTPUT VOLTAGE REGULATION VALUE, STANDBY MODE SET                                    |             |                                                                                                                                                               |             |             |
| When 0                                              | NOT USED           | NOT USED                   | NOT USED                           | See <a href="#">Table 9</a> for SM1, SM2 voltage setting, <b>Power up default=1.8 V</b>  |             |                                                                                                                                                               |             |             |
| When 1                                              | NOT USED           | NOT USED                   | NOT USED                           |                                                                                          |             |                                                                                                                                                               |             |             |

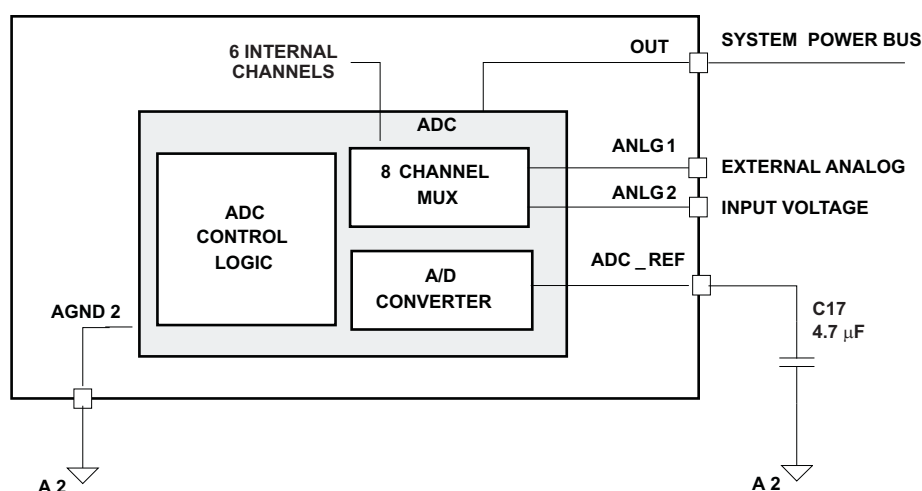
**Table 9. Programmable Settings for SM1 and SM2 (Including STANDBY)**

| SetV4_ SM | SetV3_ SM | SetV2_ SM | SetV1_ SM | SetV0_ SM | Vset SM1 | Vset SM2 | SetV4_ SM | SetV3_ SM | SetV2_ SM | SetV1_ SM | SetV0_ SM | Vset SM1 | Vset SM2 |
|-----------|-----------|-----------|-----------|-----------|----------|----------|-----------|-----------|-----------|-----------|-----------|----------|----------|
| 0         | 0         | 0         | 0         | 0         | 0.6      | 1        | 1         | 0         | 0         | 0         | 0         | 1.24     | 2.28     |
| 0         | 0         | 0         | 0         | 1         | 0.64     | 1.08     | 1         | 0         | 0         | 0         | 1         | 1.28     | 2.36     |
| 0         | 0         | 0         | 1         | 0         | 0.68     | 1.16     | 1         | 0         | 0         | 1         | 0         | 1.32     | 2.44     |
| 0         | 0         | 0         | 1         | 1         | 0.72     | 1.24     | 1         | 0         | 0         | 1         | 1         | 1.36     | 2.52     |
| 0         | 0         | 1         | 0         | 0         | 0.76     | 1.32     | 1         | 0         | 1         | 0         | 0         | 1.4      | 2.6      |
| 0         | 0         | 1         | 0         | 1         | 0.8      | 1.4      | 1         | 0         | 1         | 0         | 1         | 1.44     | 2.68     |
| 0         | 0         | 1         | 1         | 0         | 0.84     | 1.48     | 1         | 0         | 1         | 1         | 0         | 1.48     | 2.76     |
| 0         | 0         | 1         | 1         | 1         | 0.88     | 1.56     | 1         | 0         | 1         | 1         | 1         | 1.52     | 2.84     |
| 0         | 1         | 0         | 0         | 0         | 0.92     | 1.64     | 1         | 1         | 0         | 0         | 0         | 1.56     | 2.92     |
| 0         | 1         | 0         | 0         | 1         | 0.96     | 1.72     | 1         | 1         | 0         | 0         | 1         | 1.6      | 3        |
| 0         | 1         | 0         | 1         | 0         | 1        | 1.8      | 1         | 1         | 0         | 1         | 0         | 1.64     | 3.08     |
| 0         | 1         | 0         | 1         | 1         | 1.04     | 1.88     | 1         | 1         | 0         | 1         | 1         | 1.68     | 3.16     |
| 0         | 1         | 1         | 0         | 0         | 1.08     | 1.96     | 1         | 1         | 1         | 0         | 0         | 1.72     | 3.24     |
| 0         | 1         | 1         | 0         | 1         | 1.12     | 2.04     | 1         | 1         | 1         | 0         | 1         | 1.76     | 3.32     |
| 0         | 1         | 1         | 1         | 0         | 1.16     | 2.12     | 1         | 1         | 1         | 1         | 0         | 1.8      | 3.4      |
| 0         | 1         | 1         | 1         | 1         | 1.2      | 2.2      | 1         | 1         | 1         | 1         | 1         | 0.6      | 1        |

| SM1, SM2 PHASE |             |       | SMX_SLEW RATE, SMX = SM1 OR SM2 |         |         |           |           |
|----------------|-------------|-------|---------------------------------|---------|---------|-----------|-----------|
| S1S2_PHASE1    | S1S2_PHASE0 | PHASE | SLEWX_2                         | SLEWX_1 | SLEWX_0 | SM1 mV/μs | SM2 mV/μs |
| 0              | 0           | 0°    | 0                               | 0       | 0       | 0.24      | 0.48      |
| 0              | 1           | 90°   | 0                               | 0       | 1       | 0.48      | 0.96      |
| 1              | 0           | 180°  | 0                               | 1       | 0       | 0.96      | 1.92      |
| 1              | 1           | 270°  | 0                               | 1       | 1       | 1.92      | 3.84      |
|                |             |       | 1                               | 0       | 0       | 3.84      | 7.68      |
|                |             |       | 1                               | 0       | 1       | 7.68      | 15.36     |
|                |             |       | 1                               | 1       | 0       | 15.36     | 30.72     |
|                |             |       | 1                               | 1       | 1       | Immediate |           |

## FUNCTIONALITY GUIDE – ANALOG TO DIGITAL CONVERTER

| 10 BIT SUCCESSIVE APPROXIMATION ADC                                                                            |                                 |                                        |                                 |                                                 |                                 |                                 |                                                                                                |                  |
|----------------------------------------------------------------------------------------------------------------|---------------------------------|----------------------------------------|---------------------------------|-------------------------------------------------|---------------------------------|---------------------------------|------------------------------------------------------------------------------------------------|------------------|
| ADC Input Channels                                                                                             |                                 | Trigger Mode                           | Conversion Count                | Converter Mode                                  | Trigger Delay                   |                                 | Wait Time, Multiple Conversions                                                                | Power Up Default |
| Internal                                                                                                       | External                        |                                        |                                 |                                                 | Range                           | Min Step                        |                                                                                                |                  |
| Charge Current, Thermistor temperature, IC junction temperature, RTC_OUT voltage, OUT voltage, Battery voltage | ANLG1 and ANLG2 voltages        | GPIOB, I <sup>2</sup> C driven, Repeat | 1, 4, 8, 16, 32, 64, 128, 256   | Single, Average, Find max value, Find min value | 0-750 $\mu$ s, 16 steps         | 50 $\mu$ s                      | $\mu$ s: 20, 40, 60, 80, 160, 240, 320, 640<br>ms: 1.28, 1.92, 2.56, 5.12, 10.24, 15.36, 20.48 | ADC off          |
| Fixed internally                                                                                               | Selectable via I <sup>2</sup> C | Selectable via I <sup>2</sup> C        | Selectable via I <sup>2</sup> C | Selectable via I <sup>2</sup> C                 | Selectable via I <sup>2</sup> C | Selectable via I <sup>2</sup> C | Selectable via I <sup>2</sup> C                                                                |                  |



**Figure 46. Required External Components, Recommended Values, External Connections**

## ANALOG-TO-DIGITAL CONVERTER

### Overview

The TPS65800 has a 10 bit integrated successive approximation A/D, capable of running A/D conversions on eight distinct channels in a variety of modes. Two of the eight channels are connected to uncommitted pins ANLG1 and ANLG2, and can be used to convert external voltages. The other six channels monitor system parameters which are critical to the overall system monitoring. The channel selection is set via I<sup>2</sup>C.

A dedicated set of I<sup>2</sup>C registers enables configuration of the ADC to perform a conversion cycle with either a single conversion or a multiple conversions. The ALU generates a data set containing maximum value detection, minimum value detection and average value calculation for each conversion cycle. Each cycle can be performed a single time or multiple times.

### Input Channels

The following channels are available for selection via the I<sup>2</sup>C register ADC\_SET bits CHSEL\_SET bits:

Table 10. ADC input channel overview

| Channel | Connection                    | Parameter Sampled                               | Voltage Range Under Normal Operating Conditions       | Special Features                                                                     | Full Scale Reading (Internal reference selected ) | LSB value                      |
|---------|-------------------------------|-------------------------------------------------|-------------------------------------------------------|--------------------------------------------------------------------------------------|---------------------------------------------------|--------------------------------|
| CH1     | ANLG1 pin                     | User defined                                    | User defined                                          | Internal pullup current source programmable via I <sup>2</sup> C: 0/10/50/60 $\mu$ A | 2.535 V                                           | Full scale reading $\div$ 1023 |
| CH2     | ANLG2 pin                     |                                                 |                                                       |                                                                                      | 2.535 V                                           |                                |
| CH3     | ISSET1 pin                    | Voltage proportional to charge current          | 0 V (charger off) to 2.525 V (fast charge)            | —                                                                                    | 2.535 V                                           |                                |
| CH4     | TS pin                        | Voltage proportional to pack temperature        | 0 V (short) to 4.7v (no thermistor)                   | Internal 20- $\mu$ A pullup current source (ON only when AC/USB are present)         | 2.535 V                                           |                                |
| CH5     | Internal junction temperature | Voltage proportional to IC junction temperature | 1.85 V at T <sub>J</sub> = 25°C, –6.5 mV/°C slope typ | —                                                                                    | 2.535 V                                           |                                |
| CH6     | RTC_OUT pin                   | Internal LDO output voltage                     | 0 V to 3.3 V                                          | —                                                                                    | 4.7 V                                             |                                |
| CH7     | OUT pin                       | System Power bus voltage                        | 0 V to 4.4 V                                          | —                                                                                    | 4.7 V                                             |                                |
| CH8     | BAT pin                       | Battery pack positive terminal voltage          | 0 V to 4.4 V                                          | —                                                                                    | 4.7 V                                             |                                |

## FUNCTIONAL OVERVIEW

The TPS65800 ADC can be subdivided in four sections:

1. **Input selection:** The input selection section has two major blocks, the input bias control and an 8 channel MUX. The input bias control provides the bias currents that are applied to pins ANLG1 and ANLG2 and pin TS. The TS pin bias current is fixed (20  $\mu$ A typ), and the bias currents for pins ANLG1 and ANLG2 are set on I<sup>2</sup>C register ADC\_WAIT.

The TS and ANLG1 pin current sources are automatically enabled when the input power is detected, providing the required setup to measure a pack thermistor temperature (TS pin) or a battery ID resistor (ANLG1 pin). ANLG1 and ANLG2 can be used to measure external resistive loads or analog voltages. The bias current sources are always connected to the OUT pin internally.

The internal MUX connects one of the monitored analog inputs to the ADC engine, following the selection defined on register ADC\_SET.

2. **ADC engine:** The ADC engine uses an internal or external voltage reference, as defined by the ADC\_REF bit on the ADC\_SET control register. If the internal reference is selected ADC\_REF is connected to an internal LDO that regulates the ADC\_REF pin voltage to generate the ADC supply and internal voltage reference. The internal LDO maximum output current is 6 mA typical, and a conversion should be started only after the external capacitor is fully charged.

If an external reference is used it should be connected to the ADC\_REF pin. When an external reference is selected the internal LDO connected to ADC\_REF is disabled. Care must be taken when selecting an external reference as the ADC reference voltage, as it affects the ADC LSB absolute value.

3. **Trigger control and synchronization:** The ADC engine starts a conversion of the selected input when the trigger control circuit sends a start command. The trigger control circuit starts the ADC conversion and transfers the ADC output data to the arithmetic logic unit (ALU) at the end of the conversion. It also synchronizes the data transfer from the ALU to the I<sup>2</sup>C ADC\_READING register at the end of a conversion cycle, and generates the ADC status information sent to the ADC registers.

An ADC engine conversion is triggered by the TPS65800 trigger control circuit using either an internal trigger or an external trigger. The internal trigger is automatically generated by the TPS65800 at the end of each ADC engine conversion, following the timing parameters set on I<sup>2</sup>C registers ADC\_SET, ADC\_DELAY and ADC\_WAIT.

The GPIO3 pin can be used as an external trigger if the bit ADC\_TRG\_GPIO3 is set HI, in the I<sup>2</sup>C register ADC\_DELAY. In the external trigger mode a new conversion is started after the GPIO3 pin has an edge transition, following the timing parameters set on I<sup>2</sup>C registers ADC\_SET, ADC\_DELAY and ADC\_WAIT.

4. **Arithmetic Logic Unit (ALU):** The ALU performs mathematical operations on the ADC output data as defined by the I<sup>2</sup>C ADC\_READING registers. It executes average calculations or minimum /maximum detection. The result of the calculations is stored in a 11 bit accumulator register (1 bit allocated for carry-over). The accumulator value is transferred to the I<sup>2</sup>C data register at the end of a conversion cycle.

A simplified block diagram for the ADC is shown in Figure 47.

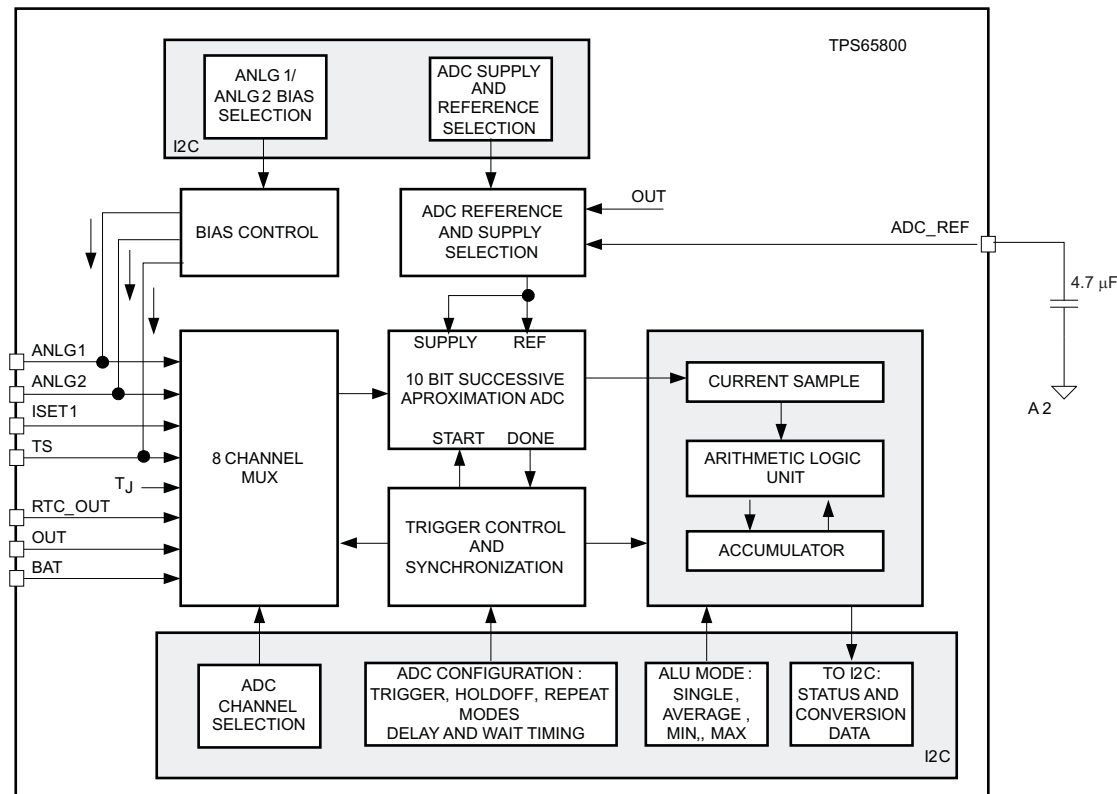


Figure 47. ADC Simplified Block Diagram

### ADC Conversion Cycle

A conversion cycle includes all the steps required to successfully sample the selected input signal and transfer the converted data to the I<sup>2</sup>C, generating an interrupt request to the host ( pin: HI→LO). The number of individual conversions (samples) in a conversion cycle is defined by the I<sup>2</sup>C ADC\_SET register bits READ\_MODE settings, and can range from a single sample to 256 samples. The conversion cycle settings for the ALU is defined by register ADC\_READING and it can be set to average, maximum value detection, minimum value detection or no processing (ADC engine output loaded in the accumulator directly).

The conversion cycle starts with the first sampling and ends when:

- The required ALU operations are performed on the final sample, and
- The ALU accumulator data is transferred to the I<sup>2</sup>C ADC\_READING register, and
- The register bit ADC\_STATUS in the ADC\_READING register is set to LO.

A conversion cycle is always started by the external host when the ADC\_EN bit in the ADC\_SET register is toggled from LO to HI by a I<sup>2</sup>C write operation. Resetting the ADC\_EN bit to LO before the current conversion cycle ends (INT: LO → HI, ADC\_STATUS bit set to LO) is not recommended, as the ADC keeps its current configuration until the current conversion cycle ends.

At the end of a conversion cycle the output data is stored at registers in the ALU block. The ADC\_STATUS bit is set to LO ( DONE ) and an interrupt is generated (INT pin: HI→LO ) if the ADC\_STATUS bit is unmasked, at the interrupt masking registers INT\_MASK. It should be noted that the minimum, maximum and average values are ALWAYS calculated by the ALU for each conversion cycle.

The value loaded in the I<sup>2</sup>C registers ADC\_READING\_HI and ADC\_READING\_LO at the end of a conversion cycle is defined by control bits ADC\_READ0 and ADC\_READ1 in register ADC\_READING\_HI. The average, minimum, maximum and last sample values for a conversion cycle can be read if the external host executes an I<sup>2</sup>C write operation, changing the values of bits ADC\_READ0 and ADC\_READ1, followed by an I<sup>2</sup>C read operation on registers ADC\_READING\_HI and ADC\_READING\_LO. The minimum, maximum, average, and last values have the same value if a conversion cycle with only one sample is executed.

The ADC\_READ0 and ADC\_READ1 bits *can not be modified* during the execution of a conversion cycle. A new conversion cycle should be started *only after* the current conversion cycle is completed, by toggling the ADC\_EN bit from HI to LO and HI again.

### External Trigger Operation

The trigger control circuit can be programmed to use an external signal to start a conversion. The TPS65800 GPIO3 input is configurable as an ADC trigger, with ADC conversion starting on either a rising edge or falling edge. When using an external trigger the trigger delay, trigger wait time delay and trigger holdoff mode can be programmed using I<sup>2</sup>C registers.

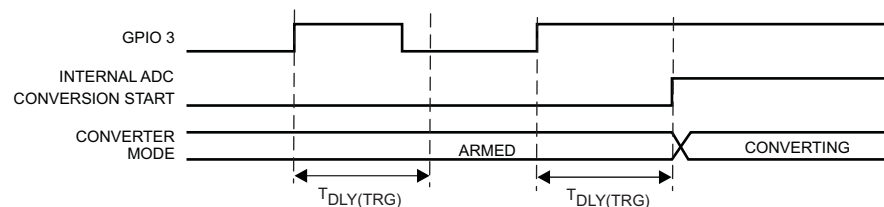
The procedure to start an externally-triggered conversion cycle has the following steps:

1. Verify that the current conversion cycle has ended (ADC\_STATUS=LO, I<sup>2</sup>C register ADC\_READING\_HI)
2. Set ADC\_EN=LO
3. Configure ADC sampling mode, ALU mode, trigger parameters, etc.
4. Set ADC\_EN=HI

After step 4 the ADC is armed, waiting for an external trigger detection to start a conversion cycle. Similarly to the non-triggered mode, the ADC configuration *should not be modified until the current conversion cycle ends*. Note that in the external trigger mode the current cycle does not end if the converter is armed and an external trigger is not detected.

### Detecting an External Trigger Event

An external trigger event is detected when the GPIO3 input has an edge that matches the edge detection programmed in the EDGE bit, at the I<sup>2</sup>C register ADC\_DELAY. The internal ADC trigger can be delayed with respect to the external trigger signal edge. The delay time value is set by the ADC\_DELAY register bits DELAY\_n, and can range from 0  $\mu$ s (no delay) to 750  $\mu$ s. A conversion is started only if the external trigger remains at its active level when the delay time expires, as shown in Figure 48. In a positive-edge detection the active trigger level is HI; in a negative-edge detection the active trigger level is LO.



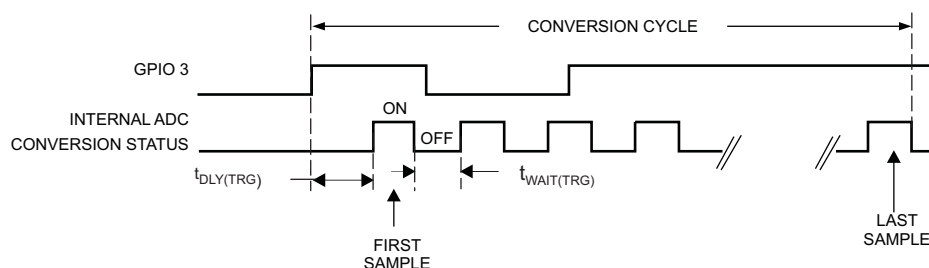
**Figure 48. ADC Conversion Triggered by GPIO3 Positive-Edge-Triggered Active-Level HI**

### Executing Multiple-Sample Cycles With an External Trigger

When executing conversion cycles that require multiple samples it may be desirable to synchronize the input signal conversion using either an external trigger that has a periodic repetition rate or an external asynchronous trigger that indicates when the external input signal being converted is valid. The TPS65800 has additional operating modes and timing parameters that can be programmed using the I<sup>2</sup>C to configure multiple sample conversion cycles.

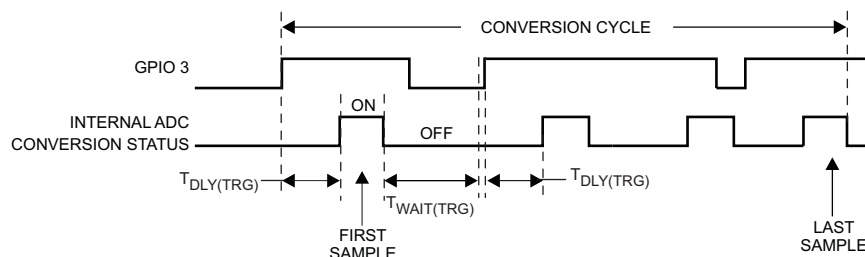
In multiple sample cycles the host can select the wait time between samples using the bits WAITn in the ADC\_WAIT register to set the wait time between samples. The wait time is measured between the end of a conversion and the start of a new conversion.

With the default power-up settings (HOLDOFF=LO, ADC\_DELAY register), the TPS65800 executes a multiple-sample conversion cycle if the first sample is taken when the trigger is at its active level. Subsequent samples are converted at the end of the wait time, even if the trigger returns to the non-active level. The external trigger level edge is ignored until the current conversion cycle ends.



**Figure 49. ADC Conversion Triggered by GPIO3 Positive Edge-Triggered Active-Level HI, Holdoff = LC**

If the sample conversion needs to be synchronized with an external trigger, during multiple sample conversion cycles, the control bit HOLDOFF should be set to HI. When the holdoff mode is active, the internal trigger starts a sample conversion only if the external trigger was detected and is at its active level at the end of the wait time, as shown in Figure 50.



**Figure 50. ADC Conversion Triggered by GPIO3 Positive Edge-Triggered Active-Level HI; Holdoff = HI, Four Sample Cycles**

When the multiple sample cycles are executed the host must configure the maximum and minimum limits for the ADC output using registers DLOLIM1, DLOLIM2, DHILIM1 and DHILIM2. A conversion cycle ends if any individual conversion result exceeds the maximum limit value or is below the minimum limit value. When an out of limit conversion is detected an interrupt is sent to the host, and the ADC\_STATUS bit on register ADC\_READING\_HI is set to DONE.

### Continuous Conversion Operation (Repeat Mode)

The TPS65800 ADC can be set to operate in a continuous conversion mode, with back-to-back conversion cycles executed. The REPEAT mode is targeted at applications where an input is continuously monitored for a period of time, and the host must be informed if the monitored input is out of the range set by I<sup>2</sup>C registers DLOLIM1, DLOLIM2, DHILIM1 and DHILIM2. In REPEAT mode each conversion is started when the ADC trigger (internal or external) is detected, and a new conversion cycle is started when the current conversion cycle ends. All the trigger and sampling modes available for normal conversion cycles are available in repeat mode. Executing I<sup>2</sup>C read operations to get the ADC readings for average, minimum, maximum and last sample values is possible in REPEAT mode. However, this is not a recommended operation, as the REPEAT mode does not generate a DONE status flag making it difficult to synchronize the ADC data reading to the end of a conversion cycle.

The recommended use of the REPEAT mode is:

1. Configure the ADC conversion cycle: trigger mode, sample mode, select input signal, etc.
2. Configure the HI and LO limits for the ADC readings
3. Set the ADC\_DELAY register bit REPEAT to HI
4. Toggle ADC\_DELAY register bit ADC\_EN bit from LO to HI

5. Monitor the INT pin. An interrupt triggered by ADC\_STATUS=LO indicates that the selected input signal is out of range

To exit the continuous mode the host must follow the steps below, if external trigger mode was set:

1. Exit external trigger mode
2. Set REPEAT bit to LO, effectively terminating the repeat mode. This generates an additional conversion; at the end of this conversion the ADC is ready for a new configuration.
3. Set ADC\_EN to LO, after on-going conversion ends

To exit the continuous mode the host must follow the steps below, if internal trigger mode was set:

1. Set REPEAT bit to LO, effectively terminating the repeat mode.
2. Set ADC\_EN to LO, after on-going conversion ends

### **ADC Input Signal Range Setting**

The registers DHILIMn and DLOLIMn can be used by the host to set maximum and minimum limits for the DAC engine output. At the end of each conversion the ADC output is checked for the maximum and minimum limits, and a status flag is set if the converted data exceeds the high limit or is under the low limit. In multiple sample operation the converted data range is checked when all programmed samples have been converted.

The host can mask or unmask interrupts caused by the ADC range status bits using the INT\_MASKn registers.



## ADC State Machine

The ADC state machine with all the trigger and operation modes is shown in Figure 51.

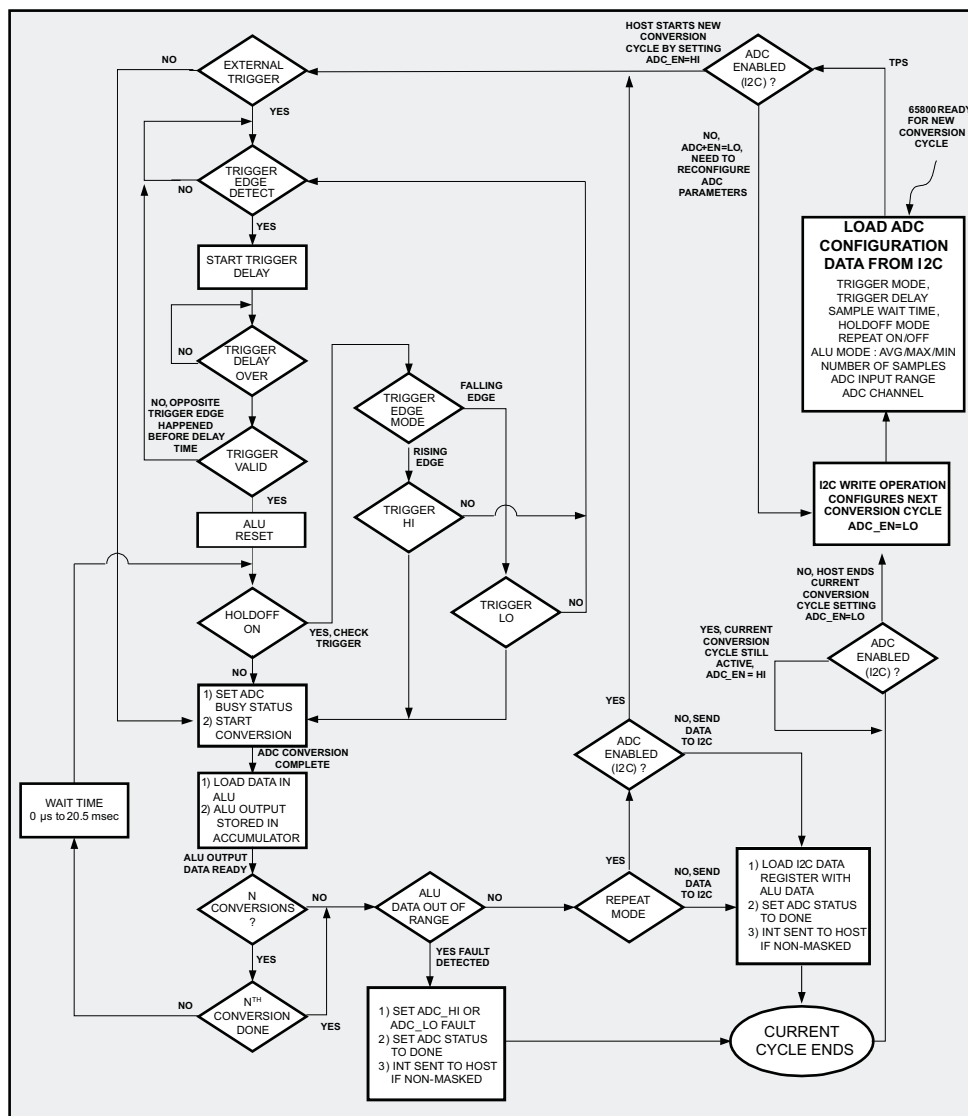


Figure 51. Trigger and Operation Modes for the ADC State Machine

## BATTERY DETECTION CIRCUIT

The ANLG1 pin has an internal current source connected between OUT and ANLG1, which is turned on automatically when the OUT pin voltage exceeds the minimum system voltage set by the SYS\_IN pin external resistive divider. The current levels for ANLG1 pin can be programmed via I<sup>2</sup>C register ADC\_WAIT, bits BATID\_n. An integrated switch discharges the BAT pin to AGND1 when  $V(\text{ANLG1}) > V(\text{OUT}) - V_{(\text{NOBATID})}$ , enabling implementation of a battery removal function if an external pack resistor ID is connected between ANLG1 and ground.

The ANLG1 pin may be used to monitor other parameters than a pack ID resistor. When ANLG1 pin is used as a generic ADC analog input  $V(\text{ANLG1})$  should never exceed  $V(\text{OUT}) - V_{(\text{NOBATID})}$ , to avoid undesired battery discharge caused by activation of the battery pin discharge circuit.

## ADC – I<sup>2</sup>C REGISTERS

The I<sup>2</sup>C registers that control ADC-related functions are shown below. The HEX address for each register is shown by the register name, together with the R or W functionality for the register bits. Default, initial power-up values are shown in bold. In the timing equations, replace Bn with 1 for HI state, and 0 for LO state.

|                                                                        | B7                                                                                                                                                                                                                             | B6                      | B5                                                        | B4                                                               | B3                                                                                  | B2                                         | B1                                                      | B0                                    |
|------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------|-----------------------------------------------------------|------------------------------------------------------------------|-------------------------------------------------------------------------------------|--------------------------------------------|---------------------------------------------------------|---------------------------------------|
| ADC_SET, ADDRESS = 1E, ALL BITS R/W                                    |                                                                                                                                                                                                                                |                         |                                                           |                                                                  |                                                                                     |                                            |                                                         |                                       |
| Bit Name                                                               | ADC_ENABLE                                                                                                                                                                                                                     | ADC_REF_EN              | CHSEL2_SET                                                | CHSEL1_SET                                                       | CHSEL0_SET                                                                          | READ_MODE2                                 | READ_MODE1                                              | READ_MODE0                            |
| Function                                                               | ADC ON/OFF CONTROL                                                                                                                                                                                                             | ADC REFERENCE SELECTION | ADC CHANNEL SELECTION                                     |                                                                  |                                                                                     | ADC SAMPLING SETTINGS                      |                                                         |                                       |
| When 0                                                                 | OFF                                                                                                                                                                                                                            | Internal                | 000 = ANLG1<br>001 = ANLG2<br>010 = V(ISET1)              | 011 = V(TS)<br>100 = Tj<br>101 = V(RTC_OUT)                      | 110 = V(OUT)<br>111 = V(BAT)<br>Default = ANLG1                                     | 000 = 1<br>001 = 4<br>010 = 8              | 011 = 16<br>100 = 32<br>101 = 64                        | 110 = 128<br>111 = 256<br>Default = 1 |
| When 1                                                                 | ON                                                                                                                                                                                                                             | External                |                                                           |                                                                  |                                                                                     |                                            |                                                         |                                       |
| ADC READING_HI, ADDRESS = 1F, BITS B3/B4 R/W, ALL OTHER BITS READ ONLY |                                                                                                                                                                                                                                |                         |                                                           |                                                                  |                                                                                     |                                            |                                                         |                                       |
| Bit Name                                                               | ADC_STATUS                                                                                                                                                                                                                     | NOT USED                | NOT USED                                                  | ADC_READ1                                                        | ADC_READ0                                                                           | D10                                        | D9_MSB                                                  | D8                                    |
| Function                                                               | CURRENT CONVERSION STATUS                                                                                                                                                                                                      | NOT USED                | NOT USED                                                  | ALU OUTPUT DATA SELECTION                                        |                                                                                     | ADC AVERAGE CARRYOVER BIT                  | ADC CONVERSION OUTPUT BITS                              |                                       |
| When 0                                                                 | DONE                                                                                                                                                                                                                           | NOT USED                | NOT USED                                                  | 00=LAST 10 = MAXIMUM<br>01=AVERAGE 11 = MINIMUM<br>Default= LAST |                                                                                     |                                            | VALID ONLY AFTER ADC CONVERSION ENDS SEE ADC_READING_LO |                                       |
| When 1                                                                 | BUSY                                                                                                                                                                                                                           | NOT USED                | NOT USED                                                  |                                                                  |                                                                                     |                                            |                                                         |                                       |
| ADC READING_LO, ADDRESS = 20, READ ONLY                                |                                                                                                                                                                                                                                |                         |                                                           |                                                                  |                                                                                     |                                            |                                                         |                                       |
| Bit Name                                                               | D7                                                                                                                                                                                                                             | D6                      | D5                                                        | D4                                                               | D3                                                                                  | D2                                         | D1                                                      | D0_LSB                                |
| Function                                                               | ADC CONVERSION OUTPUT BITS, VALID ONLY AFTER ADC CONVERSION ENDS                                                                                                                                                               |                         |                                                           |                                                                  |                                                                                     |                                            |                                                         |                                       |
| Value                                                                  | VALUE=[B10*512 + B9*256 + B8*128 + B7*64 + B6*32 + B5*16 + B4*8 + B3*4 + B2*2 + B1] * [ VRNG(CHn) / 1023]; Unit=Volts, The LSB bit value is proportional to the ADC reference voltage - See VRNG(CHn) in electrical parameters |                         |                                                           |                                                                  |                                                                                     |                                            |                                                         |                                       |
| DHILIM1, ADDRESS = 21, ALL BITS R/W                                    |                                                                                                                                                                                                                                |                         |                                                           |                                                                  |                                                                                     |                                            |                                                         |                                       |
| Bit Name                                                               | NOT USED                                                                                                                                                                                                                       | NOT USED                | NOT USED                                                  | NOT USED                                                         | NOT USED                                                                            | DHILIM10                                   | DHILIM9                                                 | DHILIM8                               |
| Function                                                               | RESERVED                                                                                                                                                                                                                       |                         |                                                           |                                                                  |                                                                                     | ADC MAX INPUT LIMIT RANGE SETTING (3 MSBs) |                                                         |                                       |
| DHILIM2, ADDRESS = 22, ALL BITS R/W                                    |                                                                                                                                                                                                                                |                         |                                                           |                                                                  |                                                                                     |                                            |                                                         |                                       |
| Bit Name                                                               | DHILIM7                                                                                                                                                                                                                        | DHILIM6                 | DHILIM5                                                   | DHILIM4                                                          | DHILIM3                                                                             | DHILIM2                                    | DHILIM1                                                 | DHILIM0_LSB                           |
| Function                                                               | ADC MAX INPUT LIMIT RANGE SETTING (8 LSBs)                                                                                                                                                                                     |                         |                                                           |                                                                  |                                                                                     |                                            |                                                         |                                       |
| DLOLIM1, ADDRESS = 23, ALL BITS R/W                                    |                                                                                                                                                                                                                                |                         |                                                           |                                                                  |                                                                                     |                                            |                                                         |                                       |
| Bit Name                                                               | NOT USED                                                                                                                                                                                                                       | NOT USED                | NOT USED                                                  | NOT USED                                                         | NOT USED                                                                            | DLOLIM10                                   | DLOLIM9                                                 | DLOLIM8                               |
| Function                                                               | RESERVED                                                                                                                                                                                                                       |                         |                                                           |                                                                  |                                                                                     | ADC MIN INPUT LIMIT RANGE SETTING (3 MSBs) |                                                         |                                       |
| DLOLIM2, ADDRESS = 24, ALL BITS R/W                                    |                                                                                                                                                                                                                                |                         |                                                           |                                                                  |                                                                                     |                                            |                                                         |                                       |
| Bit Name                                                               | DLOLIM7                                                                                                                                                                                                                        | DLOLIM6                 | DLOLIM5                                                   | DLOLIM4                                                          | DLOLIM3                                                                             | DLOLIM2                                    | DLOLIM1                                                 | DLOLIM0_LSB                           |
| Function                                                               | ADC MIN INPUT LIMIT RANGE SETTING (8 LSBs)                                                                                                                                                                                     |                         |                                                           |                                                                  |                                                                                     |                                            |                                                         |                                       |
| ADC_DELAY, ADDRESS = 25,ALL BITS R/W                                   |                                                                                                                                                                                                                                |                         |                                                           |                                                                  |                                                                                     |                                            |                                                         |                                       |
| Bit Name                                                               | ADC_TRG_GPIO3                                                                                                                                                                                                                  | EDGE_GPIO3              | HOLDOFF                                                   | REPEAT                                                           | Delay_3                                                                             | Delay_2                                    | Delay_1                                                 | Delay_0                               |
| Function                                                               | USE GPIO3 AS ADC TRIGGER                                                                                                                                                                                                       | GPIO3 TRIGGER MODE      | ADC HOLDOFF ON/OFF CONTROL                                | REPEAT MODE ON/OFF                                               | ADC EXTERNAL TRIGGER DELAY SETTING                                                  |                                            |                                                         |                                       |
| When 0                                                                 | OFF                                                                                                                                                                                                                            | Falling Edge            | OFF                                                       | OFF                                                              | t <sub>DLY(TRIG)</sub> = B4*400 + B3 * 200 + B2*100 + B1* 50, Units=μs Default=0 μs |                                            |                                                         |                                       |
| When 1                                                                 | ON                                                                                                                                                                                                                             | Rising Edge             | ON                                                        | ON                                                               |                                                                                     |                                            |                                                         |                                       |
| ADC_WAIT, ADDRESS = 26, ALL BITS R/W                                   |                                                                                                                                                                                                                                |                         |                                                           |                                                                  |                                                                                     |                                            |                                                         |                                       |
| Bit Name                                                               | ADC_CH2I_D1                                                                                                                                                                                                                    | ADC_CH2I_D0             | BATIDI_D1                                                 | BATIDI_D0                                                        | WAIT_D3                                                                             | WAIT_D2                                    | WAIT_D1                                                 | WAIT_LSB                              |
| Function                                                               | ANLG2 PULLUP CURRENT SOURCE VALUE                                                                                                                                                                                              |                         | ANLG1 PULLUP CURRENT SOURCE VALUE                         |                                                                  | ADC SAMPLE WAIT TIME, MULTIPLE SAMPLES MODE                                         |                                            |                                                         |                                       |
| When 0                                                                 | 11:60 μA, 10:50 μA, 01:10 μA, 00: 0 Default= 00                                                                                                                                                                                |                         | 11:60 μA, 10:50 μA, 01:10 μA, 00: WEAK PULLUP Default: 00 |                                                                  | 0000 = 0                                                                            | 0100 = 0.08                                | 1000 = 0.64                                             | 1100 = 5.12                           |
| When 1                                                                 |                                                                                                                                                                                                                                |                         |                                                           |                                                                  | 0001 = 0.02                                                                         | 0101 = 0.16                                | 1001 = 1.28                                             | 1101 = 10.24                          |
|                                                                        |                                                                                                                                                                                                                                |                         |                                                           |                                                                  | 0010 = 0.04                                                                         | 0110 = 0.24                                | 1010 = 1.92                                             | 1110 = 15.36                          |
|                                                                        |                                                                                                                                                                                                                                |                         |                                                           |                                                                  | 0011 = 0.06                                                                         | 0111 = 0.32                                | 1011 = 2.56                                             | 1111 = 20.48                          |
|                                                                        |                                                                                                                                                                                                                                |                         |                                                           |                                                                  | Units = ms                                                                          |                                            |                                                         | Default = 0                           |

## FUNCTIONALITY GUIDE — LED AND PERIPHERAL DRIVERS

| WHITE LED CONSTANT CURRENT DRIVER |                                                      |            |                |                          |       |         |         |                  |
|-----------------------------------|------------------------------------------------------|------------|----------------|--------------------------|-------|---------|---------|------------------|
| Driver                            | PWM                                                  |            | Output Voltage | LED Current              |       |         | Eff (%) | Power Up Default |
|                                   | Duty Cycle Range                                     | # of Steps |                | Io(Typ)                  | Max   | Acc (%) |         |                  |
| SM3                               | Off (0%),<br>0.4% -99.6%<br>Set via I <sup>2</sup> C | 256        | 5 V–25 V       | Set by external resistor | 25 mA | 25      | 80      | Off (0%)         |

| OPEN DRAIN PWM DRIVERS |                                                         |                                                       |            |          |            |                  |
|------------------------|---------------------------------------------------------|-------------------------------------------------------|------------|----------|------------|------------------|
| Driver                 | PWM Freq (kHz)                                          | PWM Duty Cycle                                        |            |          | Io(max) mA | Power Up Default |
|                        |                                                         | Range                                                 | # of Steps | Min Step |            |                  |
| PWM                    | 0.5/1/1.5/2/3/ 4.5/7.8/15.6<br>Set via I <sup>2</sup> C | Off (0%),<br>6.25% to 100<br>Set via I <sup>2</sup> C | 8          | 6.25%    | 150        | Off(0%)          |
| LED_PWM                | 15.625 or 23.4 , set via I <sup>2</sup> C               | Off(0%),<br>0.4% to 99.6%<br>Set via I <sup>2</sup> C | 256        | 0.4%     | 150        | Off (0%)         |

| RGB OPEN DRAIN LED DRIVER |                                                   |            |          |                                       |            |          |                                                            |            |           |          |                                                       |
|---------------------------|---------------------------------------------------|------------|----------|---------------------------------------|------------|----------|------------------------------------------------------------|------------|-----------|----------|-------------------------------------------------------|
| Driver                    | Flash Period (same for RGB)                       |            |          | Flash On time (same for RGB)          |            |          | Brightness (Individual R/G/B Control)                      |            |           | Io mA    | Power Up Default                                      |
|                           | Range                                             | # of Steps | Min Step | Range                                 | # of Steps | Min Step | Duty (%)                                                   | # of Steps | Min Steps |          |                                                       |
| RED,<br>GREEN,<br>BLUE    | No flash,<br>or 1–8 s<br>Set via I <sup>2</sup> C | 16         | 0.5 s    | 0.1–0.6 s<br>Set via I <sup>2</sup> C | 8          | 0.1 s    | Off (0%),<br>3.125 to<br>96.87<br>Set via I <sup>2</sup> C | 32         | 3.125%    | 0/4/8/12 | Flash Off, 0<br>mA,<br>0%<br>brightness<br>duty cycle |

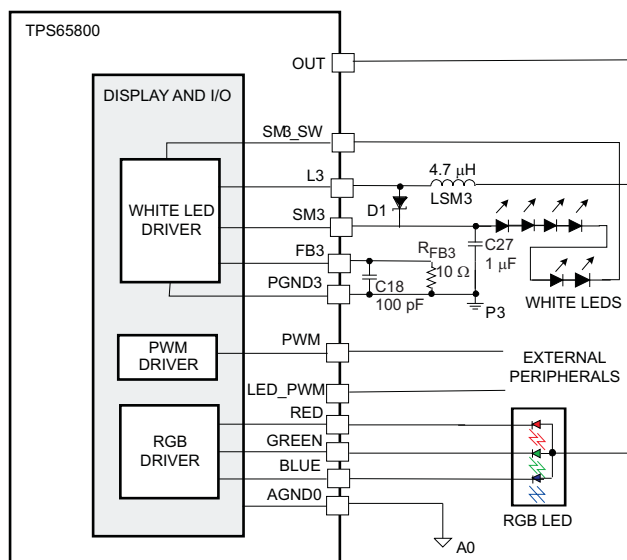
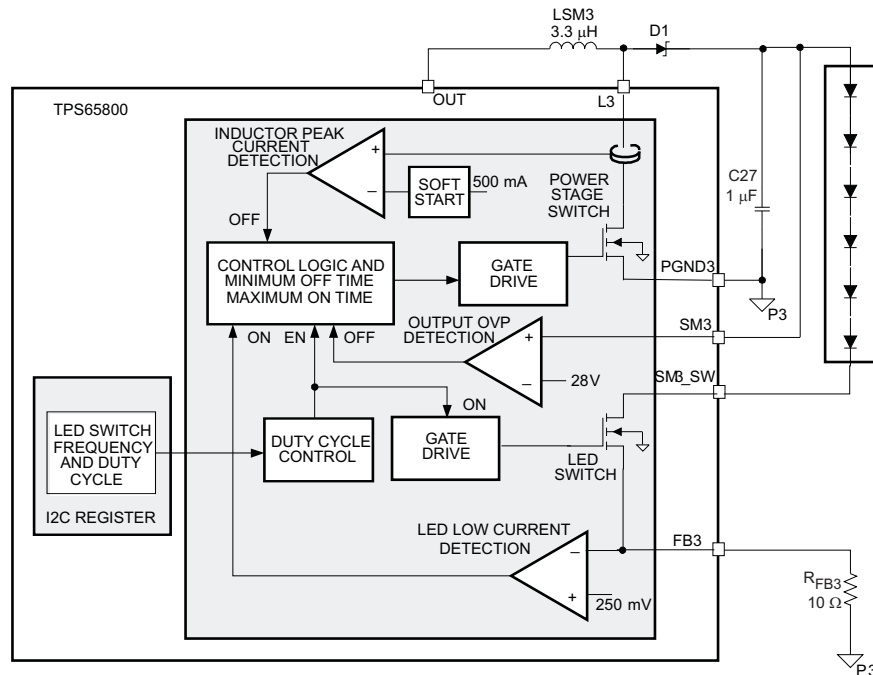


Figure 52. Required External Components, Recommended Values, External Connections

## WHITE LED CONSTANT CURRENT DRIVER

The TPS65800 has an integrated boost converter (SM3) that is optimized to drive white LEDs connected in a series configuration. Up to six series white LEDs can be driven, with programmable current and duty cycle adjustable via a dedicated I<sup>2</sup>C register.

The SM3 boost converter (SM3) has a 30-V, 500-mA, low-side integrated power stage switch that drives the external inductor. Another integrated 30-V, 25-mA switch (LED switch) is used to modulate the brightness of the external white LEDs. A simplified block diagram is shown in [Figure 53](#)



**Figure 53. Simplified Block Diagram**

The SM3 converter operates like a standard boost converter. The LED current is defined by the value of the external resistor  $R_{FB3}$ , connected from pin FB3 to AGND1. The integrated power stage switch control monitors the LED switch current (FB3) and the integrated power stage switch current, implementing a topology that effectively regulates the LED current independently of the input voltage and number of LEDs connected. The high voltage rating of the integrated switches enables driving up to six white LEDs, connected in a series configuration.

The internal LED switch, in series with the external LEDs, disconnects the LEDs from ground during shutdown. In addition, the LED switch is driven by a PWM signal that sets the duty cycle, enabling adjustment to the average LED current by modifying the settings of the I<sup>2</sup>C register SM3\_SET. With this control method, the LED brightness depends on the LED switch duty cycle only, and is independent of the PWM control signal.

The duty cycle control used in the SM3 converter LED switch is implemented by generating a burst of high frequency pulses, with a pattern that is repeated periodically. For a duty cycle of 50%, all of the high frequency pulses have a 50% duty cycle. The duty cycle control sets individual pulses to 100% duty cycle when increasing the LED\_PWM output duty cycle; for decreasing LED\_PWM output duty cycles, individual pulses are set to 0% duty cycle. An example of distinct duty cycles is shown in [Figure 54](#), the sum of the individual pulses on/off time over the repetition period are equivalent to the duty cycle obtained with traditional single-pulse duty cycle circuits.

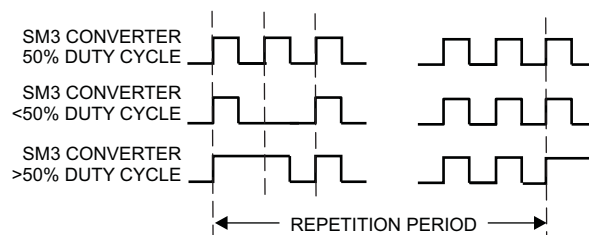


Figure 54. Example of Distinct Duty Cycles

The repetition period can be set using the register `SOFT_RESET` control bit `SM3_LF_OSC` to either 180 Hz (HI) or 122 Hz (LO). Each repetition period has a total of 256 pulses, enabling a resolution of 0.4% when programming the duty cycle.

### SM3 Control Logic Overview

The SM3 boost converter operates in a pulse frequency modulation (PFM) scheme with constant peak current control. This control scheme maintains high efficiency over the entire load current range and enables the use of small external components, as the switching frequency can reach up to 1 MHz depending on the load conditions. The LED current ripple is defined by the external inductor size.

The converter monitors the sense voltage at pin FB3, and turns on the integrated power stage switch when  $V_{(FB3)}$  is below the 250-mV (typ) internal reference voltage and the LED Switch is ON, starting a new cycle. The integrated power switch turns off when the inductor current reaches the internal 500-mA (typ) peak current limit, or if the switch is on for a period longer than the maximum on-time of 6  $\mu$ s (typ). The integrated power switch also turns off when the LED switch is set to OFF. As the integrated power switch is turned off, the external Schottky diode is forward biased, delivering the stored inductor energy to the output. The main switch remains off until the FB3 pin voltage is below the internal 250-mV reference voltage and the LED switch is turned ON, when it is turned on again.

This PFM peak current control scheme sets the converter in discontinuous conduction mode (DCM), and the switching frequency depends on the inductor, input/output voltage and LED current. Lower LED currents reduce the switching frequency, with high efficiency over the entire LED current range. This regulation scheme is inherently stable, allowing a wide range for the selection of the inductor and output capacitor.

### Peak Current Control (Boost Converter)

The SM3 integrated power stage switch is turned on until the inductor current reaches the DC current limit  $I_{MAX(L3)}$  (500 mA, typ). Due to internal delays, typically around 100 ns, the actual current exceeds the DC current limit threshold by a small amount. The typical peak current limit can be calculated as shown in [Equation 8](#)

$$I_{P(typ)} = I_{MAX(L3)} + \frac{V(OUT)}{L} \times 100 \text{ ns}, \text{ or } I_{P(typ)} = 500 \text{ mA} + \frac{V(OUT)}{L} \times 100 \text{ ns} \quad (8)$$

The current overshoot is directly proportional to the input voltage, and inversely proportional to the inductor value.

### Soft Start

All inductive step-up converters exhibit high in-rush current during start-up. If no special precautions are taken, voltage drops can be observed at the input supply rail during start-up, with unpredictable results in the overall system operation.

The SM3 boost converter limits the inrush current during start-up by increasing the current limit in three steps:

1. 125 mA (typ),
2. 250 mA (typ) and
3. 500 mA (typ)

The two initial steps (125 mA and 250 mA) are active for 256 power stage switching cycles.

### Enabling the SM3 Converter

The SM3\_SET I<sup>2</sup>C register controls the SM3 LED switch duty cycle. If the register is set to all zeros SM3 is set to OFF mode. When the host writes a value other than 00 in SM3\_SET the SM3 converter is enabled, entering the soft start phase and then normal operation. The SM3 converter can operate with duty cycles varying from 0.4% to 99.6%, with LED switch frequencies of 122 Hz or 180 Hz. The LED switch operating frequency is set by bit SM3\_LF, in the SOFT\_RESET register.

### Overvoltage Protection

The output voltage of the boost converter is sensed at pin SM3, and the integrated power stage switch is turned OFF when  $V(\text{SM3})$  exceeds the internal overvoltage threshold  $V_{\text{OVP3}}$ . The converter returns to normal operation when  $V(\text{SM3}) < V_{\text{OVP3}} - V_{\text{HYS}(\text{OVP3})}$ .

### Under Voltage Lockout Operation

When the TPS65800 enters the UVLO mode, the SM3 converter is set to OFF mode with the power stage MOSFET switch and the LED switch open (off).

### Thermal Shutdown Operation

When the TPS65800 enters the thermal shutdown mode, the SM3 converter is set to OFF mode with the power stage MOSFET switch and the LED switch open (off).

## PWM DRIVERS

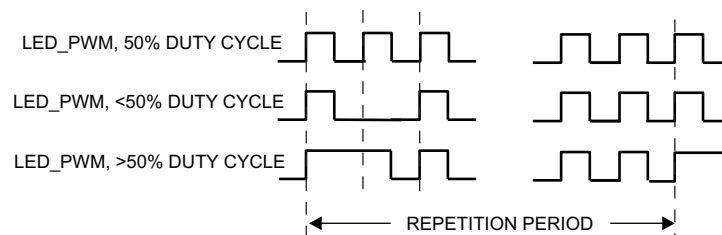
### PWM Pin Driver

The TPS65800 offers one low-frequency, open-drain PWM driver, capable of driving up to 150 mA. The PWM frequency and duty cycle are defined by the PWM I<sup>2</sup>C register settings. The PWM parameters are set in I<sup>2</sup>C register PWM. Available frequency values range from 500 Hz to 15 kHz, with 8 frequency values and 16 duty cycle options (6.25% each).

### LED\_PWM Pin Driver

The TPS65800 has another PWM driver output (pin LED\_PWM), which is optimized to drive a backlight LED. The LED\_PWM driver controls the external LED current intensity using a pulse-width control method, with duty cycle being set by the I<sup>2</sup>C register LED\_PWM.

The pulse width method implemented generates a burst of high frequency pulses, with a pattern that is repeated periodically. For a duty cycle of 50%, all of the high -frequency pulses have a 50% duty cycle. The duty cycle control sets individual pulses to 100% duty cycle when increasing the LED\_PWM output duty cycle; for decreasing LED\_PWM output duty cycles individual pulses are set to 0% duty cycle. An example of distinct duty cycles is shown in Figure 55; the sum of the individual pulses on/off time over the repetition period is equivalent to the duty cycle obtained with traditional single-pulse duty cycle circuits.



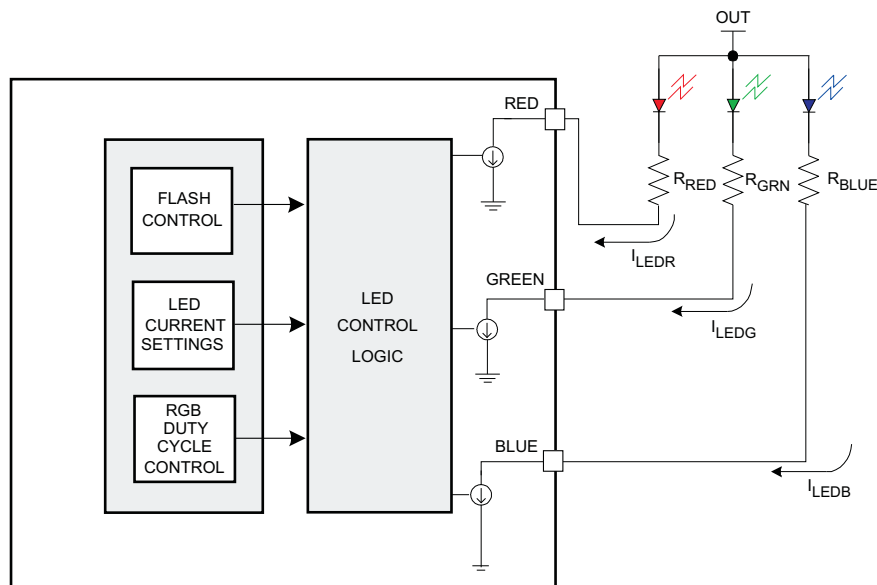
**Figure 55. Example of Distinct Duty Cycles**

The repetition period can be set using the register SOFT\_RESET control bit SM3\_LF\_OSC to either 183 Hz (HI) or 122 Hz (LO). Each repetition period has a total of 256 pulses, enabling a resolution of 0.4% when programming the duty cycle. The LED\_SET register enables control of the duty cycle via I<sup>2</sup>C, with duty cycle ranging from 0.4% to 99.6%. Setting the LED\_SET register to all zeros forces the LED\_PWM pin to 0% duty cycle (OFF).

## RGB Driver

The TPS65800 has a dedicated driver for an RGB external LED. Three outputs are available (pins RED, GREEN, BLUE), with common settings for operation mode (flash on/off, flash period, flash on time), LED current and phase delay between outputs. The TPS65800 RGB driver continually flashes the external LEDs connected to the RED, GREEN and BLUE pins using the flash operation parameters defined in register RGB\_FLASH.

The currents for the external LEDs can be programmed via I<sup>2</sup>C, and external resistors are not required to limit the LED current. However, they can be added to set the LED current if the available I<sup>2</sup>C values are not compatible with the current application, as shown in the circuit below:



**Figure 56. Limiting the External LED Current**

The flashing-mode parameters defined in register RGB\_FLASH enable setting the flashing period from 1 to 8 seconds in 0.5-s steps, or to continuous operation. Flashing operation is enabled by setting the FLASH\_EN bit in register RGB\_FLASH to HI. This bit must be set HI to enable the RGB current-sink channels.

Each driver has an individual duty cycle control. The duty cycle modulation method used is similar to the PWM\_LED duty cycle control, with high frequency pulses being generated when the driver (RED, GREEN, or BLUE pins) is ON. The repetition period for the RGB drivers has a total of 32 pulses, enabling a 3.125% resolution when programming the individual RED, GREEN and BLUE drivers duty cycles. The duty cycles for each driver can be set individually using control bits on registers RGB\_RED, RGB\_GREEN and RGB\_BLUE.

The RGB drivers can be programmed to sink 4, 8, or 12 mA, with no external current limiting resistor.

## White LED, PWM Drivers — I<sup>2</sup>C Registers

The I<sup>2</sup>C registers that control LED AND PWM driver related functions are shown below. The HEX address for each register is shown by the register name, together with the R or W functionality for the register bits. Shaded values indicate default initial power-up values. In the equations replace Bn with 1 for HI state, and 0 for LO state.

|                                      | B7                                                                                 | B6                                                                        | B5                                  | B4                                                                           | B3                                                                          | B2         | B1         | B0         |
|--------------------------------------|------------------------------------------------------------------------------------|---------------------------------------------------------------------------|-------------------------------------|------------------------------------------------------------------------------|-----------------------------------------------------------------------------|------------|------------|------------|
| SM3_SET, ADDRESS=16, ALL BITS R/W    |                                                                                    |                                                                           |                                     |                                                                              |                                                                             |            |            |            |
| Bit Name                             | SM3_I7 set                                                                         | SM3_I6 set                                                                | SM3_I5 set                          | SM3_I4 set                                                                   | SM3_I3 set                                                                  | SM3_I2 set | SM3_I1 set | SM3_I0 set |
| Function                             | SM3 DUTY CYCLE CONTROL                                                             |                                                                           |                                     |                                                                              |                                                                             |            |            |            |
| Value                                | See <a href="#">Table 11</a> for SM3 duty cycle settings, <b>default = 0 (OFF)</b> |                                                                           |                                     |                                                                              |                                                                             |            |            |            |
| RGB_FLASH, ADDRESS= 17, ALL BITS R/W |                                                                                    |                                                                           |                                     |                                                                              |                                                                             |            |            |            |
| Bit Name                             | FLASH_EN                                                                           | FLASH_ON2                                                                 | FLASH_ON1                           | FLASH_ON0                                                                    | FLASH_PER3                                                                  | FLASH_PER2 | FLASH_PER1 | FLASH_PER0 |
| Function                             | FLASH MODE ON/OFF CTRL                                                             | FLASH MODE ON TIME                                                        |                                     |                                                                              | FLASH MODE PERIOD                                                           |            |            |            |
| When 0                               | OFF                                                                                | See <a href="#">Table 12</a> for RGB ON TIME settings, <b>default=0.1</b> |                                     |                                                                              | See <a href="#">Table 12</a> for RGB FLASH settings, <b>default = 1</b>     |            |            |            |
| When 1                               | ON                                                                                 |                                                                           |                                     |                                                                              |                                                                             |            |            |            |
| RGB_RED, ADDRESS=18, ALL BITS R/W    |                                                                                    |                                                                           |                                     |                                                                              |                                                                             |            |            |            |
| Bit Name                             | RGB_ISET1                                                                          | RGB_ISET0                                                                 | PHASE                               | PWMR_D4                                                                      | PWMR_D3                                                                     | PWMR_D2    | PWMR_D1    | PWMR_D0    |
| Function                             | RGB LED CURRENT SETTINGS                                                           |                                                                           | PHASE CONTROL                       | REG DRIVER DUTY CYCLE CONTROL                                                |                                                                             |            |            |            |
| When 0                               | 00= 0    10= 8 mA<br>01= 4 mA    11=12 mA                                          |                                                                           | GREEN out of $\Phi$ with RED & BLUE | See <a href="#">Table 12</a> for RGB_RED DUTY settings, <b>default = 0</b>   |                                                                             |            |            |            |
| When 1                               |                                                                                    |                                                                           | BLUE out of $\Phi$ with RED & GREEN |                                                                              |                                                                             |            |            |            |
| RGB_GREEN, ADDRESS=19, ALL BITS R/W  |                                                                                    |                                                                           |                                     |                                                                              |                                                                             |            |            |            |
| Bit Name                             | NOT USED                                                                           | NOT USED                                                                  | NOT USED                            | PWMG_D4                                                                      | PWMG_D3                                                                     | PWMG_D2    | PWMG_D1    | PWMG_D0    |
| Function                             | NOT USED                                                                           | NOT USED                                                                  | NOT USED                            | GREEN DRIVER DUTY CYCLE CONTROL                                              |                                                                             |            |            |            |
| Value                                | NOT USED                                                                           | NOT USED                                                                  | NOT USED                            | See <a href="#">Table 12</a> for RGB_GREEN DUTY settings, <b>default = 0</b> |                                                                             |            |            |            |
| RGB_BLUE, ADDRESS=1A, ALL BITS R/W   |                                                                                    |                                                                           |                                     |                                                                              |                                                                             |            |            |            |
| Bit Name                             | NOT USED                                                                           | NOT USED                                                                  | NOT USED                            | PWMB_D4                                                                      | PWMB_D3                                                                     | PWMB_D2    | PWMB_D1    | PWMB_D0    |
| Function                             | NOT USED                                                                           | NOT USED                                                                  | NOT USED                            | BLUE DRIVER DUTY CYCLE CONTROL                                               |                                                                             |            |            |            |
| Value                                | NOT USED                                                                           | NOT USED                                                                  | NOT USED                            | See <a href="#">Table 12</a> for RGB_BLUE DUTY settings, <b>default = 0</b>  |                                                                             |            |            |            |
| PWM, ADDRESS=1D, ALL BITS R/W        |                                                                                    |                                                                           |                                     |                                                                              |                                                                             |            |            |            |
| Bit Name                             | PWM_EN                                                                             | PWM1_F2                                                                   | PWM_F1                              | PWM_F0                                                                       | PWM_D3                                                                      | PWM_D2     | PWM_D1     | PWM_D0     |
| Function                             | PWM ON/OFF CONTROL                                                                 | PWM DRIVER FREQUENCY SETTINGS                                             |                                     |                                                                              | PWM DRIVER DUTY CYCLE SETTINGS                                              |            |            |            |
| When 0                               | Disabled                                                                           | 000 = 15.6 kHz                                                            | 011 = 3 kHz                         | 110 = 1 kHz                                                                  | See <a href="#">Table 13</a> for PWM DUTY settings, <b>default = 0.0625</b> |            |            |            |
| When 1                               | Enabled                                                                            | 001 = 7.8 kHz<br>010 = 4.5 kHz                                            | 100 = 2 kHz<br>101 = 1.5 kHz        | 111 = 500 Hz<br><b>Default = 15.6 kHz</b>                                    |                                                                             |            |            |            |
| LED_PWM, ADDRESS=27, ALL BITS R/W    |                                                                                    |                                                                           |                                     |                                                                              |                                                                             |            |            |            |
| Bit Name                             | LPWM_7 set                                                                         | LPWM_6 set                                                                | LPWM_5 set                          | LPWM_4 set                                                                   | LPWM_3 set                                                                  | LPWM_2 set | LPWM_1 set | LPWM_0 set |
| Function                             | LED_PWM DRIVER DUTY CYCLE CONTROL                                                  |                                                                           |                                     |                                                                              |                                                                             |            |            |            |
| Value                                | See <a href="#">Table 11</a> for LED_PWM DUTY settings, <b>default=0 (OFF)</b>     |                                                                           |                                     |                                                                              |                                                                             |            |            |            |



**Table 11. SM3 Duty Cycle Settings**

| Dec | B7-B0     | Dcpu  | Dec | B7-B0     | Dcpu  | Dec | B7-B0     | Dcpu  | Dec | B7-B0     | Dcpu  | Dec | B7-B0     | Dcpu  |
|-----|-----------|-------|-----|-----------|-------|-----|-----------|-------|-----|-----------|-------|-----|-----------|-------|
| 0   | 0000 0000 | –     | 52  | 0011 0100 | 0.203 | 104 | 0110 1000 | 0.406 | 156 | 1001 1100 | 0.609 | 208 | 1101 0000 | 0.813 |
| 1   | 0000 0001 | 0.004 | 53  | 0011 0101 | 0.207 | 105 | 0110 1001 | 0.410 | 157 | 1001 1101 | 0.613 | 209 | 1101 0001 | 0.816 |
| 2   | 0000 0010 | 0.008 | 54  | 0011 0110 | 0.211 | 106 | 0110 1010 | 0.414 | 158 | 1001 1110 | 0.617 | 210 | 1101 0010 | 0.820 |
| 3   | 0000 0011 | 0.012 | 55  | 0011 0111 | 0.215 | 107 | 0110 1011 | 0.418 | 159 | 1001 1111 | 0.621 | 211 | 1101 0011 | 0.824 |
| 4   | 0000 0100 | 0.016 | 56  | 0011 1000 | 0.219 | 108 | 0110 1100 | 0.422 | 160 | 1010 0000 | 0.625 | 212 | 1101 0100 | 0.828 |
| 5   | 0000 0101 | 0.020 | 57  | 0011 1001 | 0.223 | 109 | 0110 1101 | 0.426 | 161 | 1010 0001 | 0.629 | 213 | 1101 0101 | 0.832 |
| 6   | 0000 0110 | 0.023 | 58  | 0011 1010 | 0.227 | 110 | 0110 1110 | 0.430 | 162 | 1010 0010 | 0.633 | 214 | 1101 0110 | 0.836 |
| 7   | 0000 0111 | 0.027 | 59  | 0011 1011 | 0.230 | 111 | 0110 1111 | 0.434 | 163 | 1010 0011 | 0.637 | 215 | 1101 0111 | 0.840 |
| 8   | 0000 1000 | 0.031 | 60  | 0011 1100 | 0.234 | 112 | 0111 0000 | 0.438 | 164 | 1010 0100 | 0.641 | 216 | 1101 1000 | 0.844 |
| 9   | 0000 1001 | 0.035 | 61  | 0011 1101 | 0.238 | 113 | 0111 0001 | 0.441 | 165 | 1010 0101 | 0.645 | 217 | 1101 1001 | 0.848 |
| 10  | 0000 1010 | 0.039 | 62  | 0011 1110 | 0.242 | 114 | 0111 0010 | 0.445 | 166 | 1010 0110 | 0.648 | 218 | 1101 1010 | 0.852 |
| 11  | 0000 1011 | 0.043 | 63  | 0011 1111 | 0.246 | 115 | 0111 0011 | 0.449 | 167 | 1010 0111 | 0.652 | 219 | 1101 1011 | 0.855 |
| 12  | 0000 1100 | 0.047 | 64  | 0100 0000 | 0.250 | 116 | 0111 0100 | 0.453 | 168 | 1010 1000 | 0.656 | 220 | 1101 1100 | 0.859 |
| 13  | 0000 1101 | 0.051 | 65  | 0100 0001 | 0.254 | 117 | 0111 0101 | 0.457 | 169 | 1010 1001 | 0.660 | 221 | 1101 1101 | 0.863 |
| 14  | 0000 1110 | 0.055 | 66  | 0100 0010 | 0.258 | 118 | 0111 0110 | 0.461 | 170 | 1010 1010 | 0.664 | 222 | 1101 1110 | 0.867 |
| 15  | 0000 1111 | 0.059 | 67  | 0100 0011 | 0.262 | 119 | 0111 0111 | 0.465 | 171 | 1010 1011 | 0.668 | 223 | 1101 1111 | 0.871 |
| 16  | 0001 0000 | 0.063 | 68  | 0100 0100 | 0.266 | 120 | 0111 1000 | 0.469 | 172 | 1010 1100 | 0.672 | 224 | 1110 0000 | 0.875 |
| 17  | 0001 0001 | 0.066 | 69  | 0100 0101 | 0.270 | 121 | 0111 1001 | 0.473 | 173 | 1010 1101 | 0.676 | 225 | 1110 0001 | 0.879 |
| 18  | 0001 0010 | 0.070 | 70  | 0100 0110 | 0.273 | 122 | 0111 1010 | 0.477 | 174 | 1010 1110 | 0.680 | 226 | 1110 0010 | 0.883 |
| 19  | 0001 0011 | 0.074 | 71  | 0100 0111 | 0.277 | 123 | 0111 1011 | 0.480 | 175 | 1010 1111 | 0.684 | 227 | 1110 0011 | 0.887 |
| 20  | 0001 0100 | 0.078 | 72  | 0100 1000 | 0.281 | 124 | 0111 1100 | 0.484 | 176 | 1011 0000 | 0.688 | 228 | 1110 0100 | 0.891 |
| 21  | 0001 0101 | 0.082 | 73  | 0100 1001 | 0.285 | 125 | 0111 1101 | 0.488 | 177 | 1011 0001 | 0.691 | 229 | 1110 0101 | 0.895 |
| 22  | 0001 0110 | 0.086 | 74  | 0100 1010 | 0.289 | 126 | 0111 1110 | 0.492 | 178 | 1011 0010 | 0.695 | 230 | 1110 0110 | 0.898 |
| 23  | 0001 0111 | 0.090 | 75  | 0100 1011 | 0.293 | 127 | 0111 1111 | 0.496 | 179 | 1011 0011 | 0.699 | 231 | 1110 0111 | 0.902 |
| 24  | 0001 1000 | 0.094 | 76  | 0100 1100 | 0.297 | 128 | 1000 0000 | 0.500 | 180 | 1011 0100 | 0.703 | 232 | 1110 1000 | 0.906 |
| 25  | 0001 1001 | 0.098 | 77  | 0100 1101 | 0.301 | 129 | 1000 0001 | 0.504 | 181 | 1011 0101 | 0.707 | 233 | 1110 1001 | 0.910 |
| 26  | 0001 1010 | 0.102 | 78  | 0100 1110 | 0.305 | 130 | 1000 0010 | 0.508 | 182 | 1011 0110 | 0.711 | 234 | 1110 1010 | 0.914 |
| 27  | 0001 1011 | 0.105 | 79  | 0100 1111 | 0.309 | 131 | 1000 0011 | 0.512 | 183 | 1011 0111 | 0.715 | 235 | 1110 1011 | 0.918 |
| 28  | 0001 1100 | 0.109 | 80  | 0101 0000 | 0.313 | 132 | 1000 0100 | 0.516 | 184 | 1011 1000 | 0.719 | 236 | 1110 1100 | 0.922 |
| 29  | 0001 1101 | 0.113 | 81  | 0101 0001 | 0.316 | 133 | 1000 0101 | 0.520 | 185 | 1011 1001 | 0.723 | 237 | 1110 1101 | 0.926 |
| 30  | 0001 1110 | 0.117 | 82  | 0101 0010 | 0.320 | 134 | 1000 0110 | 0.523 | 186 | 1011 1010 | 0.727 | 238 | 1110 1110 | 0.930 |
| 31  | 0001 1111 | 0.121 | 83  | 0101 0011 | 0.324 | 135 | 1000 0111 | 0.527 | 187 | 1011 1011 | 0.730 | 239 | 1110 1111 | 0.934 |
| 32  | 0010 0000 | 0.125 | 84  | 0101 0100 | 0.328 | 136 | 1000 1000 | 0.531 | 188 | 1011 1100 | 0.734 | 240 | 1111 0000 | 0.938 |
| 33  | 0010 0001 | 0.129 | 85  | 0101 0101 | 0.332 | 137 | 1000 1001 | 0.535 | 189 | 1011 1101 | 0.738 | 241 | 1111 0001 | 0.941 |
| 34  | 0010 0010 | 0.133 | 86  | 0101 0110 | 0.336 | 138 | 1000 1010 | 0.539 | 190 | 1011 1110 | 0.742 | 242 | 1111 0010 | 0.945 |
| 35  | 0010 0011 | 0.137 | 87  | 0101 0111 | 0.340 | 139 | 1000 1011 | 0.543 | 191 | 1011 1111 | 0.746 | 243 | 1111 0011 | 0.949 |
| 36  | 0010 0100 | 0.141 | 88  | 0101 1000 | 0.344 | 140 | 1000 1100 | 0.547 | 192 | 1100 0000 | 0.750 | 244 | 1111 0100 | 0.953 |
| 37  | 0010 0101 | 0.145 | 89  | 0101 1001 | 0.348 | 141 | 1000 1101 | 0.551 | 193 | 1100 0001 | 0.754 | 245 | 1111 0101 | 0.957 |
| 38  | 0010 0110 | 0.148 | 90  | 0101 1010 | 0.352 | 142 | 1000 1110 | 0.555 | 194 | 1100 0010 | 0.758 | 246 | 1111 0110 | 0.961 |
| 39  | 0010 0111 | 0.152 | 91  | 0101 1011 | 0.355 | 143 | 1000 1111 | 0.559 | 195 | 1100 0011 | 0.762 | 247 | 1111 0111 | 0.965 |
| 40  | 0010 1000 | 0.156 | 92  | 0101 1100 | 0.359 | 144 | 1001 0000 | 0.563 | 196 | 1100 0100 | 0.766 | 248 | 1111 1000 | 0.969 |
| 41  | 0010 1001 | 0.160 | 93  | 0101 1101 | 0.363 | 145 | 1001 0001 | 0.566 | 197 | 1100 0101 | 0.770 | 249 | 1111 1001 | 0.973 |
| 42  | 0010 1010 | 0.164 | 94  | 0101 1110 | 0.367 | 146 | 1001 0010 | 0.570 | 198 | 1100 0110 | 0.773 | 250 | 1111 1010 | 0.977 |
| 43  | 0010 1011 | 0.168 | 95  | 0101 1111 | 0.371 | 147 | 1001 0011 | 0.574 | 199 | 1100 0111 | 0.777 | 251 | 1111 1011 | 0.980 |
| 44  | 0010 1100 | 0.172 | 96  | 0110 0000 | 0.375 | 148 | 1001 0100 | 0.578 | 200 | 1100 1000 | 0.781 | 252 | 1111 1100 | 0.984 |
| 45  | 0010 1101 | 0.176 | 97  | 0110 0001 | 0.379 | 149 | 1001 0101 | 0.582 | 201 | 1100 1001 | 0.785 | 253 | 1111 1101 | 0.988 |
| 46  | 0010 1110 | 0.180 | 98  | 0110 0010 | 0.383 | 150 | 1001 0110 | 0.586 | 202 | 1100 1010 | 0.789 | 254 | 1111 1110 | 0.992 |
| 47  | 0010 1111 | 0.184 | 99  | 0110 0011 | 0.387 | 151 | 1001 0111 | 0.590 | 203 | 1100 1011 | 0.793 | 255 | 1111 1111 | 0.996 |
| 48  | 0011 0000 | 0.188 | 100 | 0110 0100 | 0.391 | 152 | 1001 1000 | 0.594 | 204 | 1100 1100 | 0.797 |     |           |       |
| 49  | 0011 0001 | 0.191 | 101 | 0110 0101 | 0.395 | 153 | 1001 1001 | 0.598 | 205 | 1100 1101 | 0.801 |     |           |       |
| 50  | 0011 0010 | 0.195 | 102 | 0110 0110 | 0.398 | 154 | 1001 1010 | 0.602 | 206 | 1100 1110 | 0.805 |     |           |       |
| 51  | 0011 0011 | 0.199 | 103 | 0110 0111 | 0.402 | 155 | 1001 1011 | 0.605 | 207 | 1100 1111 | 0.809 |     |           |       |

**Table 12. RGB Duty Cycle Control Settings**

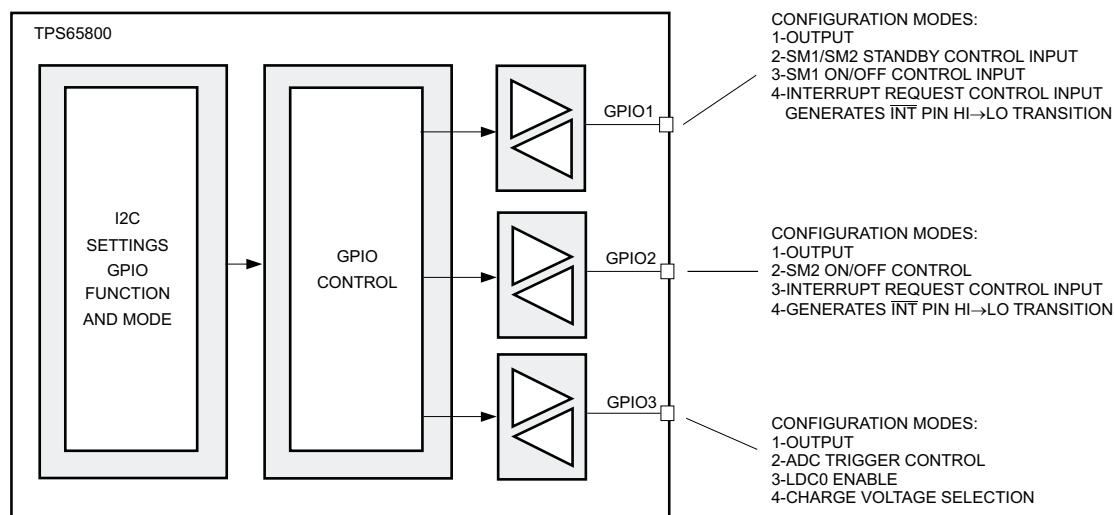
| RGB_D4 | RGB_D3 | RGB_D2 | RGB_D1 | RGB_D0 | DC(%) | FLASH_PER3 | FLASH_PER2 | FLASH_PER1 | FLASH_PER0 | P(s)        |
|--------|--------|--------|--------|--------|-------|------------|------------|------------|------------|-------------|
| 0      | 0      | 0      | 0      | 0      | 0.00  | 0          | 0          | 0          | 0          | 1           |
| 0      | 0      | 0      | 0      | 1      | 3.23  | 0          | 0          | 0          | 1          | 1.5         |
| 0      | 0      | 0      | 1      | 0      | 6.45  | 0          | 0          | 1          | 0          | 2           |
| 0      | 0      | 0      | 1      | 1      | 9.68  | 0          | 0          | 1          | 1          | 2.5         |
| 0      | 0      | 1      | 0      | 0      | 12.90 | 0          | 1          | 0          | 0          | 3           |
| 0      | 0      | 1      | 0      | 1      | 16.13 | 0          | 1          | 0          | 1          | 3.5         |
| 0      | 0      | 1      | 1      | 0      | 19.35 | 0          | 1          | 1          | 0          | 4           |
| 0      | 0      | 1      | 1      | 1      | 22.58 | 0          | 1          | 1          | 1          | 4.5         |
| 0      | 1      | 0      | 0      | 0      | 25.80 | 1          | 0          | 0          | 0          | 5           |
| 0      | 1      | 0      | 0      | 1      | 29.03 | 1          | 0          | 0          | 1          | 5.5         |
| 0      | 1      | 0      | 1      | 0      | 32.25 | 1          | 0          | 1          | 0          | 6           |
| 0      | 1      | 0      | 1      | 1      | 35.48 | 1          | 0          | 1          | 1          | 6.5         |
| 0      | 1      | 1      | 0      | 0      | 38.70 | 1          | 1          | 0          | 0          | 7           |
| 0      | 1      | 1      | 0      | 1      | 41.93 | 1          | 1          | 0          | 1          | 7.5         |
| 0      | 1      | 1      | 1      | 0      | 45.15 | 1          | 1          | 1          | 0          | 8           |
| 0      | 1      | 1      | 1      | 1      | 48.38 | 1          | 1          | 1          | 1          | Continuous  |
| 1      | 0      | 0      | 0      | 0      | 51.60 |            |            |            |            |             |
| 1      | 0      | 0      | 0      | 1      | 54.83 |            |            |            |            |             |
| 1      | 0      | 0      | 1      | 0      | 58.05 |            | FLASH_ON2  | FLASH_ON1  | FLASH_ON0  | ON_TIME (s) |
| 1      | 0      | 0      | 1      | 1      | 61.23 |            | 0          | 0          | 0          | 0.1         |
| 1      | 0      | 1      | 0      | 0      | 64.50 |            | 0          | 0          | 1          | 0.15        |
| 1      | 0      | 1      | 0      | 1      | 67.73 |            | 0          | 1          | 0          | 0.2         |
| 1      | 0      | 1      | 1      | 0      | 70.95 |            | 0          | 1          | 1          | 0.25        |
| 1      | 0      | 1      | 1      | 1      | 74.18 |            | 1          | 0          | 0          | 0.3         |
| 1      | 1      | 0      | 0      | 0      | 77.40 |            | 1          | 0          | 1          | 0.4         |
| 1      | 1      | 0      | 0      | 1      | 80.63 |            | 1          | 1          | 0          | 0.5         |
| 1      | 1      | 0      | 1      | 0      | 83.85 |            | 1          | 1          | 1          | 0.6         |
| 1      | 1      | 0      | 1      | 1      | 87.08 |            |            |            |            |             |
| 1      | 1      | 1      | 0      | 0      | 90.30 |            |            |            |            |             |
| 1      | 1      | 1      | 0      | 1      | 93.53 |            |            |            |            |             |
| 1      | 1      | 1      | 1      | 0      | 96.75 |            |            |            |            |             |
| 1      | 1      | 1      | 1      | 1      | 99.98 |            |            |            |            |             |

**Table 13. PWM Frequency and Duty Cycle Settings**

| PWM FREQUENCY TABLE |        |        |        | PWM_D DUTY CYCLE |         |         |         |              |
|---------------------|--------|--------|--------|------------------|---------|---------|---------|--------------|
| PWM_F2              | PWM_F1 | PWM_F0 | F (Hz) | PWM2_D3          | PWM2_D2 | PWM2_D1 | PWM2_D0 | D_cycle (pu) |
| 0                   | 0      | 0      | 15600  | 0                | 0       | 0       | 0       | 0.0625       |
| 0                   | 0      | 1      | 7800   | 0                | 0       | 0       | 1       | 0.125        |
| 0                   | 1      | 0      | 4500   | 0                | 0       | 1       | 0       | 0.1875       |
| 0                   | 1      | 1      | 3000   | 0                | 0       | 1       | 1       | 0.25         |
| 1                   | 0      | 0      | 2000   | 0                | 1       | 0       | 0       | 0.3125       |
| 1                   | 0      | 1      | 1500   | 0                | 1       | 0       | 1       | 0.375        |
| 1                   | 1      | 0      | 1000   | 0                | 1       | 1       | 0       | 0.4375       |
| 1                   | 1      | 1      | 500    | 0                | 1       | 1       | 1       | 0.5          |
|                     |        |        |        | 1                | 0       | 0       | 0       | 0.5625       |
|                     |        |        |        | 1                | 0       | 0       | 1       | 0.625        |
|                     |        |        |        | 1                | 0       | 1       | 0       | 0.6875       |
|                     |        |        |        | 1                | 0       | 1       | 1       | 0.75         |
|                     |        |        |        | 1                | 1       | 0       | 0       | 0.8125       |
|                     |        |        |        | 1                | 1       | 0       | 1       | 0.875        |
|                     |        |        |        | 1                | 1       | 1       | 0       | 0.9375       |
|                     |        |        |        | 1                | 1       | 1       | 1       | 1            |

**FUNCTIONALITY GUIDE – GENERAL PURPOSE INPUTS/OUTPUTS**

| GPIO3 FUNCTIONS                                |               |                                                                                                                                                                        |                                                                                                                                   |                                                                                                                                                    |                            |
|------------------------------------------------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|
| CONFIGURED AS OUTPUT                           |               | CONFIGURED AS INPUT                                                                                                                                                    |                                                                                                                                   | POWER-UP<br>DEFAULT                                                                                                                                |                            |
| OUTPUT LEVEL                                   | Io(max)<br>mA | A/D CONVERSION START TRIGGER                                                                                                                                           |                                                                                                                                   |                                                                                                                                                    |                            |
| HI or LO at output set<br>via I <sup>2</sup> C | 5             | Falling or rising edge selected via I <sup>2</sup> C                                                                                                                   |                                                                                                                                   | Input, no mode<br>selected                                                                                                                         |                            |
| GPIO2 FUNCTIONS                                |               |                                                                                                                                                                        |                                                                                                                                   |                                                                                                                                                    |                            |
| CONFIGURED AS OUTPUT                           |               | CONFIGURED AS INPUT                                                                                                                                                    |                                                                                                                                   | POWER-UP<br>DEFAULT                                                                                                                                |                            |
| OUTPUT LEVEL                                   | Io(max)<br>mA | HOST INTERRUPT<br>REQUEST                                                                                                                                              | SM2 ENABLE                                                                                                                        |                                                                                                                                                    |                            |
| HI or LO at output set<br>via I <sup>2</sup> C | 5             | Set $\overline{\text{INT}}$ pin to LO via I <sup>2</sup> C<br>when GPIO2 pin edge is<br>detected. Rising or falling<br>edge detection selected via<br>I <sup>2</sup> C | GPIO2 level sets SM2 converter ON/OFF operation.<br>GPIO2 pin level (HI or LO) for ON operation<br>selected via I <sup>2</sup> C  | Input, no mode<br>selected                                                                                                                         |                            |
|                                                |               | The host interrupt request and SM2 enable GPIO2 functions are mutually exclusive,<br>and they should NOT be configured simultaneously                                  |                                                                                                                                   |                                                                                                                                                    |                            |
| GPIO1 FUNCTIONS                                |               |                                                                                                                                                                        |                                                                                                                                   |                                                                                                                                                    |                            |
| CONFIGURED AS OUTPUT                           |               | CONFIGURED AS INPUT                                                                                                                                                    |                                                                                                                                   |                                                                                                                                                    | POWER-UP<br>DEFAULT        |
| OUTPUT LEVEL                                   | Io(max)<br>mA | HOST INTERRUPT<br>REQUEST                                                                                                                                              | SM1 ENABLE                                                                                                                        | SM1 AND SM2 STANDBY<br>CONTROL                                                                                                                     |                            |
| HI or LO at output set<br>via I <sup>2</sup> C | 5             | Set $\overline{\text{INT}}$ pin to LO via I <sup>2</sup> C<br>when GPIO1 pin edge is<br>detected. Rising or falling<br>edge detection set via I <sup>2</sup> C         | GPIO1 level sets SM1<br>converter ON/OFF<br>operation. GPIO2 pin<br>level (HI or LO) for ON<br>operation set via I <sup>2</sup> C | GPIO1 level sets SM2 and<br>SM1 converters in standby<br>mode. GPIO1 pin level (HI<br>or LO) for standby mode<br>set selected via I <sup>2</sup> C | Input, no mode<br>selected |
|                                                |               | The host interrupt request, SM1 enable and SM1/SM2 standby control GPIO1<br>functions are mutually exclusive, and they should NOT be configured<br>simultaneously.     |                                                                                                                                   |                                                                                                                                                    |                            |

**Figure 57. Required External Components, Recommended Values, External Connections**

## General Purpose I/Os — GPIO 1, 2, 3

The TPS65800 integrates 3 general purpose open drain ports (GPIOs) that can be configured as selectable inputs or outputs. When configured as outputs the output level can be set to LO or HI via I<sup>2</sup>C commands. When the GPIOs are configured as inputs the action to be taken when a transition or HI/LO level is detected at the GPIO pin is selectable via I<sup>2</sup>C.

When configured as inputs the GPIOs can be set in the following modes:

1. Interrupt request: In this mode of operation, a transition at the GPIO pin generates an interrupt request at the interrupt controller. The GPIO interrupt request can be masked at the INT\_MASK register. This operation mode is available for GPIO's 1 and 2.
2. SM1 and SM2 control: The GPIO's can be used to turn the converters SM1 and SM2 ON/OFF, as well as setting them in standby mode. This control mode is available for GPIO1 (SM1 on/off and SM1/SM2 standby) and GPIO2 (SM2 on/off control).
3. ADC trigger: GPIO3 can be configured as an external ADC trigger. The GPIO3 trigger configuration bit is located at the ADC register ADC\_DELAY.

## GPIOs Input Level Configuration

When using I<sup>2</sup>C commands, the GPIO1 and GPIO2 pins can be configured as logic output signals or as level-controlled inputs which enables (or disables) the switch mode converters SM1 and/or SM2. These pins may also be configured as rising- or falling-edge-triggered inputs to externally control the generation of an interrupt signal ( $\overline{\text{INT}}$ ), if desired.

The GPIO3 pin may be used as an external trigger source to start an A/D conversion cycle or as a logic output.

See Figure 58 for a description of the logic used for GPIO1 and GPIO2 inputs when configured for edge-triggered interrupt generation. The signal from the GPIO pin input is double-latched before being sent to the interrupt controller logic. The inversion of the Q output from the first flip-flop must be HI to allow the output latch to be cleared when a READ command occurs. On the initial edge of the GPIO signal, the Q output of the flip-flop is set (HI). The  $\overline{\text{INT}}$  line is asserted (LO) after the initial selected edge from the GPIO pin. On the next falling (or rising) edge of the GPIO pin, the interrupt can again be cleared (which allows the  $\overline{\text{INT}}$  pin to go back high). The  $\overline{\text{INT}}$  signal is cleared (set back HI) after an I<sup>2</sup>C READ operation is performed.

Thus, two successive edges of the GPIO signal, followed by an I<sup>2</sup>C READ command, are required to clear the  $\overline{\text{INT}}$  pin output. If no I<sup>2</sup>C READ commands occur, repeatedly applying edges to the GPIO pin does not toggle the state of the  $\overline{\text{INT}}$  pin output.

In addition to an I<sup>2</sup>C READ command after two GPIO edges, a UVLO event or reconfiguration of the GPIO pins as outputs also de-asserts the  $\overline{\text{INT}}$  signal.

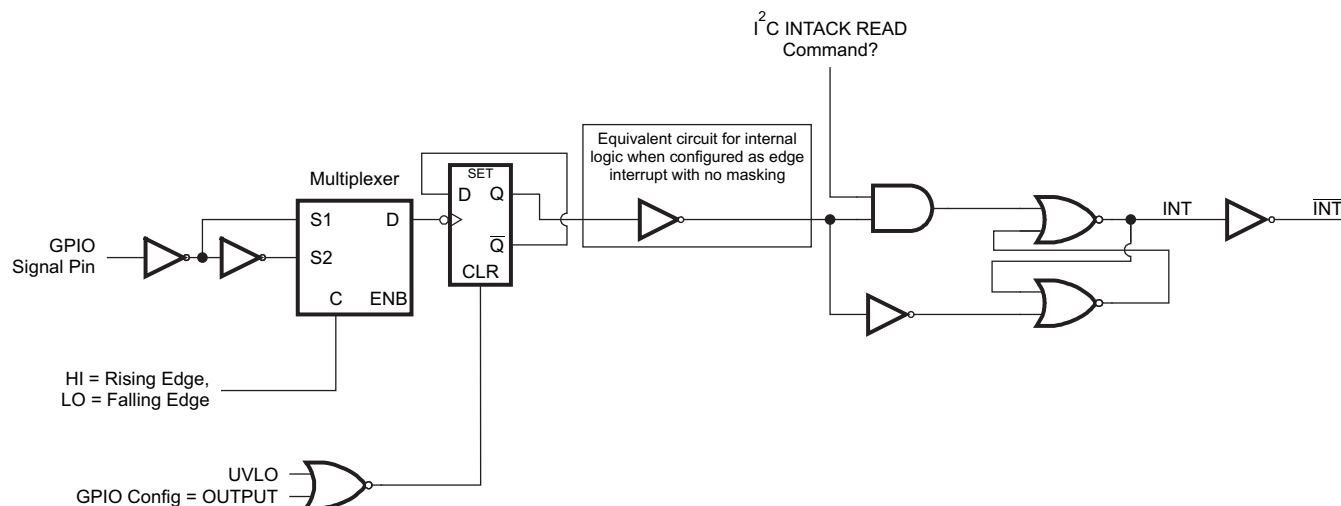


Figure 58. GPIO 1 or GPIO2 Configured as an Interrupt Request Input

## Function Implementation: I<sup>2</sup>C Commands × GPIO Commands

Some of the GPIO SM1/SM2 control functions overlap I<sup>2</sup>C register control functions. [Table 14](#) describes the TPS65800 action when the GPIO's command and I<sup>2</sup>C registers commands are not compatible with each other.

**Table 14. GPIO Commands and I<sup>2</sup>C Registers Commands**

| SM1 AND SM2 ON/OFF I <sup>2</sup> C COMMAND  | GPIO COMMAND       | SM1 OR SM2 MODE SET |
|----------------------------------------------|--------------------|---------------------|
| CONVERTER DISABLED                           | DON'T CARE         | DISABLED            |
| CONVERTER ENABLED                            | CONVERTER ENABLED  | ENABLED             |
| DON'T CARE                                   | CONVERTER DISABLED | DISABLED            |
| SM1 AND SM2 STANDBY I <sup>2</sup> C COMMAND | GPIO COMMAND       | SM1 OR SM2 MODE SET |
| DO NOT SET STANDBY                           | DON'T CARE         | NORMAL              |
| SET STANDBY                                  | SET STANDBY        | STANDBY             |
| DON'T CARE                                   | DO NOT SET STANDBY | NORMAL              |

## GPIO Configuration Table

Table 15 describes the I<sup>2</sup>C register settings required to program the available GPIO modes.

**Table 15. Recommended GPIO Configuration Procedure**

| GPIO MODE                                       | I <sup>2</sup> C REGISTERS | I <sup>2</sup> C REGISTER BIT SETTING                                               | ADDITIONAL DETAILS                                               |
|-------------------------------------------------|----------------------------|-------------------------------------------------------------------------------------|------------------------------------------------------------------|
| GPIO3 = OUTPUT                                  | GPIO3                      | GPIO3I/O=HI AND GPIO3OUT=HI                                                         | GPIO3 PIN SET TO HIGH IMPEDANCE MODE                             |
|                                                 |                            | GPIO3I/O=HI AND GPIO3OUT=LO                                                         | V(GPIO3) = V <sub>OL</sub>                                       |
| GPIO3 =INPUT<br>ADC CONVERSION<br>START TRIGGER | GPIO3 AND<br>ADC_DELAY     | GPIO3I/O=LO AND ADC_TRG_GPIO3=HI AND<br>EDGE_GPIO3=HI                               | GPIO3 pin rising edge triggers ADC<br>conversion                 |
|                                                 |                            | GPIO3I/O=LO AND ADC_TRG_GPIO3=HI AND<br>EDGE_GPIO3=LO                               | GPIO3 pin falling edge triggers ADC<br>conversion                |
| GPIO2 = OUTPUT                                  | GPIO12                     | GPIO2I/O=HI AND GPIO2OUT=HI                                                         | GPIO2 PIN SET TO HIGH IMPEDANCE<br>MODE                          |
|                                                 |                            | GPIO2I/O=HI AND GPIO2OUT=LO                                                         | V(GPIO2) = V <sub>OL</sub>                                       |
| GPIO2=INPUT,<br>HOST INTERRUPT<br>REQUEST       | GPIO12 AND<br>GPIO3        | GPIO2I/O=LO AND GPIO2INT=HI AND<br>GPIO2LVL=HI AND GPIO2SM2=LO                      | $\overline{\text{INT}}$ pin HI→LO→HI at V(GPIO2) falling<br>edge |
|                                                 |                            | GPIO2I/O=LO AND GPIO2INT=HI AND<br>GPIO2LVL=HI AND GPIO2SM2=LO                      | $\overline{\text{INT}}$ pin HI→LO→HI at V(GPIO2) rising<br>edge  |
| GPIO2=INPUT,<br>SM2 ENABLE                      | GPIO12 AND<br>GPIO3        | GPIO2I/O=LO AND GPIO2INT=LO AND<br>GPIO2LVL=HI AND GPIO2SM2=HI                      | SM2 converter ON at V(GPIO2) = HI                                |
|                                                 |                            | GPIO2I/O=LO AND GPIO2INT=LO AND<br>GPIO2LVL=LO AND GPIO2SM2=HI                      | SM2 converter ON at V(GPIO2) = LO                                |
| GPIO1 = OUTPUT                                  | GPIO12                     | GPIO1I/O=HI AND GPIO1OUT=HI                                                         | GPIO1 PIN SET TO HIGH IMPEDANCE<br>MODE                          |
|                                                 |                            | GPIO1I/O=HI AND GPIO1OUT=LO                                                         | V(GPIO1) = V <sub>OL</sub>                                       |
| GPIO1=INPUT,<br>HOST INTERRUPT<br>REQUEST       | GPIO12 AND<br>GPIO3        | GPIO1I/O=LO AND GPIO1INT=HI AND<br>GPIO1LVL=HI AND GPIO1SM1=LO AND<br>GPIO1SMSBY=LO | $\overline{\text{INT}}$ pin HI→LO→HI at V(GPIO1) falling<br>edge |
|                                                 |                            | GPIO1I/O=LO AND GPIO1INT=HI AND<br>GPIO1LVL=LO AND GPIO1SM1=LO AND<br>GPIO1SMSBY=LO | $\overline{\text{INT}}$ pin HI→LO→HI at V(GPIO1) rising<br>edge  |
| GPIO1=INPUT,<br>SM1 ENABLE                      | GPIO12 AND<br>GPIO3        | GPIO1I/O=LO AND GPIO1INT=LO AND<br>GPIO1LVL=HI AND GPIO1SM1=HI AND<br>GPIO1SMSBY=LO | SM1 converter ON at V(GPIO1) = HI                                |
|                                                 |                            | GPIO1I/O=LO AND GPIO1INT=LO AND<br>GPIO1LVL=LO AND GPIO1SM1=HI AND<br>GPIO1SMSBY=LO | SM1 converter ON at V(GPIO1) = LO                                |
| GPIO1=INPUT,<br>SM1/SM2 STANDBY<br>CONTROL      | GPIO12 AND<br>GPIO3        | GPIO1I/O=LO AND GPIO1INT=LO AND<br>GPIO1LVL=HI AND GPIO1SM1=LO AND<br>GPIO1SMSBY=HI | SM1/SM2 converter standby set at<br>V(GPIO1) = HI                |
|                                                 |                            | GPIO1I/O=LO AND GPIO1INT=LO AND<br>GPIO1LVL=LO AND GPIO1SM1=LO AND<br>GPIO1SMSBY=HI | SM1/SM2 converter standby set at<br>V(GPIO1) = LO                |

## GPIOs — I<sup>2</sup>C Registers

The I<sup>2</sup>C registers that control GPIO-related functions are shown below. The HEX address for each register is shown by the register name, together with the R or W functionality for the register bits. Shaded values indicate default initial power-up values.

|                                         | B7         | B6                            | B5                            | B4                            | B3                             | B2                             | B1                                         | B0                        |
|-----------------------------------------|------------|-------------------------------|-------------------------------|-------------------------------|--------------------------------|--------------------------------|--------------------------------------------|---------------------------|
| <b>GPIO12, ADDRESS=1B, ALL BITS R/W</b> |            |                               |                               |                               |                                |                                |                                            |                           |
| <b>Bit Name</b>                         | GPIO2I/O   | GPIO1I/O                      | GPIO2OUT                      | GPIO1OUT                      | GPIO2LVL                       | GPIO1LVL                       | GPIO1SMSBY                                 | GPIO1SM1                  |
| <b>Function</b>                         | GPIO2 MODE | GPIO1 MODE                    | SET GPIO2 LEVEL (OUTPUT ONLY) | SET GPIO1 LEVEL (OUTPUT ONLY) | GPIO2 EDGE AND LEVEL DETECTION | GPIO1 EDGE AND LEVEL DETECTION | GPIO 1 CONTROLS SM1 AND SM2 STANDBY ON/OFF | GPIO1 CONTROLS SM1 ON/OFF |
| <b>When 0</b>                           | INPUT      | INPUT                         | LOW                           | LOW                           | RISING EDGE, LO LEVEL          | RISING EDGE, LO LEVEL          | DISABLED                                   | DISABLED                  |
| <b>When 1</b>                           | OUTPUT     | OUTPUT                        | HIGH                          | HIGH                          | FALLING EDGE, HI LEVEL         | FALLING EDGE, HI LEVEL         | ENABLED                                    | ENABLED                   |
| <b>GPIO3, ADDRESS=1C, ALL BITS R/W</b>  |            |                               |                               |                               |                                |                                |                                            |                           |
| <b>Bit Name</b>                         | GPIO3I/O   | GPIO3OUT                      | LDO0_EN                       | CHG_VOLT                      | NOT USED                       | GPIO2 INT                      | GPIO1 INT                                  | GPIO2SM2                  |
| <b>Function</b>                         | GPIO3 MODE | SET GPIO3 LEVEL (OUTPUT ONLY) | LDO0 ON/OFF CONTROL           | CHARGE VOLTAGE SAFETY BIT     | NOT USED                       | GPIO2 TRIGGERS INT:HI→LO       | GPIO1 TRIGGERS INT:HI→LO                   | SM2 ON/OFF CONTROL        |
| <b>When 0</b>                           | INPUT      | LOW                           | OFF                           | 4.20 V                        | NOT USED                       | DISABLED                       | DISABLED                                   | DISABLED                  |
| <b>When 1</b>                           | OUTPUT     | HIGH                          | ON                            | 4.36 V                        | NOT USED                       | ENABLED                        | ENABLED                                    | ENABLED                   |



## APPLICATION INFORMATION

### INDUCTOR AND CAPACITOR SELECTION — CONVERTERS SM1 AND SM2

SM1 and SM2 are designed with internal voltage mode compensation and the stabilization is based on choosing an LC filter that has a corner frequency around 27 kHz. It is not recommended to use LC values that would be outside the range of 13 kHz to 40 kHz.

Equation 9 calculates the corner frequency of the output LC filter. The standard recommended LC values are 3.3  $\mu$ H and 10  $\mu$ F.

$$F = \frac{1}{2\pi\sqrt{LC}} = 27.7 \text{ kHz} \quad (\text{a) for } L = 3.3 \mu\text{H and } C = 10 \mu\text{F} \quad (9)$$

The inductor value, along with the input voltage  $V_{IN}$ , output voltage  $V_{OUT}$  and switching frequency  $f$  define the ripple current. Typically the ripple current target is 30% of the full load current. At light loads it is desirable for ripple current to be less than 150% of the light load current.

The inductor should be chosen with a rating to handle the peak ripple current., if an inductor's current gets higher than its rated saturation level (DCR), the inductance starts to fall off, and the inductor's ripple current increases exponentially. The DCR of the inductor plays an important role in efficiency and size of the inductor. Larger diameter wire has less DCR but may increase the size of the inductor

Equation 10 calculates the target inductor value. If an inductor value has already been chosen, Equation 11, calculates the inductor's ripple current under static operating conditions. The ripple amplitude can be calculated during the on time (positive ramp) or during the off time (negative ramp). It is easiest to calculate the ripple using the off time, because the inductor's voltage is the output voltage.

$$I_{\text{target}} = \frac{V_{\text{OUT}}}{0.3 \times I_{\text{OUT\_MAX}}} \left( 1 - \frac{V_{\text{OUT}}}{V_{\text{IN\_MAX}}} \right) \frac{1}{f} \quad (10)$$

$$\Delta I_L = \frac{V_L}{L} \times \Delta t = \frac{V_{\text{OUT}}}{L} \left( 1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}} \right) \frac{1}{f} \quad (11)$$

Equation 12 calculates the peak current due to the output load and ripple current

$$I_{L\text{max}} = I_{\text{OUTmax}} + \frac{\Delta I_L}{2} \quad (12)$$

For a faster transient response, a lower inductor and higher capacitance allows the output current to ramp faster, while the addition capacitance holds up the output longer (a 2.2- $\mu$ H inductor in combination with a 22- $\mu$ F output capacitor are recommended).

The highest inductor current occurs at the maximum input voltage. The peak inductor current during a transient may be higher than the steady state peak current and should be considered when choosing an inductor. Monitoring the inductor current for non-saturation operation during a transient of  $1.2 \times I_{\text{loadmax}}$  at  $V_{\text{in\_max}}$  ensures adequate saturation margin.

**Table 16. Inductors for Typical Operation Conditions**

| DEVICE          | INDUCTOR VALUE | TYPE              | COMPONENT SUPPLIER |
|-----------------|----------------|-------------------|--------------------|
| DCDC3 converter | 3.3 $\mu$ H    | CDRH2D14NP-3R3    | Sumida             |
|                 | 3.3 $\mu$ H    | PDS3010-332       | Coilcraft          |
|                 | 3.3 $\mu$ H    | VLF4012AT-3R3M1R3 | TDK                |
|                 | 2.2 $\mu$ H    | VLF4012AT-2R2M1R5 | TDK                |
|                 | 2.2 $\mu$ H    | NR3015T2R2        | Taoup-Uidem        |

**APPLICATION INFORMATION (continued)****Table 16. Inductors for Typical Operation Conditions (continued)**

| DEVICE          | INDUCTOR VALUE | TYPE              | COMPONENT SUPPLIER |
|-----------------|----------------|-------------------|--------------------|
| DCDC2 converter | 3.3 µH         | CDRH2D18/HPNP-3R3 | Sumida             |
|                 | 3.3 µH         | VLF4012AT-3R3M1R3 | TDK                |
|                 | 2.2 µH         | VLCF4020-2R2      | TDK                |
| DCDC1 converter | 3.3 µH         | CDRH3D14/HPNP-3R2 | Sumida             |
|                 | 3.3 µH         | CDRH4D28C-3R2     | Sumida             |
|                 | 3.3 µH         | MSS5131-332       | Coilcraft          |
|                 | 2.2 µH         | VLCF4020-2R2      | TDK                |

**OUTPUT CAPACITOR SELECTION, SM1, SM2 CONVERTERS**

The advanced fast response voltage mode control scheme of the SM1, SM2 converters implemented in the TPS65020 allow the use of small ceramic capacitors with a typical value of 10 µF for a 3.3-µH inductor, without having large output voltage under and overshoots during heavy load transients.

Ceramic capacitors having low ESR values have low output voltage ripple, and recommended values and manufacturers are listed in [Table 1](#). Often, due to the low ESR, the ripple current rating of the ceramic capacitor is adequate to meet the inductor's currents requirements.

The RMS ripple current is calculated as:

$$I_{\text{RMSOut}} = \frac{1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}}}{2 \times L \times f} \times \frac{1}{\sqrt{3}} \quad (13)$$

At nominal load current, the inductive converters operate in PWM mode. The overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor: The output voltage ripple is maximum at the highest input voltage  $V_{\text{IN}}$ .

$$V_{\text{RMSOut}} = \frac{1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}}}{L \times f} \times \left( \frac{1}{8 \times C_{\text{out}} \times f} + \text{ESR} \right) \quad (14)$$

At light load currents, the converters operate in PFM and the output voltage ripple is dependent on the output capacitor value. The output voltage ripple is set by the internal PFM output voltage comparator delay and the external capacitor. The typical output voltage ripple is less than 1% of the nominal output voltage.

**Table 17. Input/Output Capacitors for Typical Operation Conditions**

| CAPACITOR VALUE | CASE SIZE | COMPONENT SUPPLIER        | COMMENTS |
|-----------------|-----------|---------------------------|----------|
| 22 µF           | 1260      | TDK C3216X5R0J226M        | Ceramic  |
| 22 µF           | 1260      | Taiyo Yuden JMK316BJ226ML | Ceramic  |
| 10 µF           | 0805      | Taiyo Yuden JMK212BJ106M  | Ceramic  |
| 10 µF           | 0805      | TDK C2012X5R0J106M        | Ceramic  |
| 22 µF           | 0805      | TDK C2012X5R0J226MT       | Ceramic  |
| 22 µF           | 0805      | Taiyo Yuden JMK212BJ226MG | Ceramic  |

## INPUT CAPACITOR SELECTION, SM1, SM2 CONVERTERS

Buck converters have a pulsating input current that can generate high input voltage spikes at  $V_{IN}$ . A low ESR input capacitor is required to filter the input voltage, minimizing the interference with other circuits connected to the same power supply rail. Each dc-dc converter requires a 10- $\mu$ F ceramic input capacitor on its input pin.

## OUTPUT VOLTAGE SELECTION, SM1, SM2 CONVERTERS

Typically the output voltage is programmed by the I<sup>2</sup>C. An external divider can be added to raise the output voltage, if the available I<sup>2</sup>C values do not meet the application requirements. Care must be taken with this special option, because this external divider (gain factor) would apply to any selected I<sup>2</sup>C output voltage value for this converter.

Equation 16 calculates R1, Let R2 = 20 k $\Omega$ :

$$R1 = \left[ \frac{V_{SMxOUT}}{V_{FB}} - 1 \right] R2 \quad (16)$$

Where  $V_{FB}$  is the I<sup>2</sup>C selected voltage, is the desired output voltage and R1/R2 is the feedback divider.

## DESIGN EXAMPLES

### SM1, SM2 CONVERTER DESIGN EXAMPLE

#### Design Conditions and Parametrs for SM1 or SM2:

Vin\_SM1/2: 4.6V typical (May be less if input source is limited).

Vout\_SM1/2: 1.24 V

Iout\_max: 0.6 A

fsw = 1500 kHz

fc = 25 kHz

$$L_{target} = \frac{V_{OUT}}{0.3 \times I_{OUT\_MAX}} \left[ 1 - \frac{V_{OUT}}{V_{IN\_MAX}} \right] \frac{1}{f_{sw}} = 3.35 \mu H, \text{ 3.3 } \mu H \text{ is a good target.} \quad (17)$$

$$C = \frac{1}{L[2 \times \pi \times f_c]^2} = 10.5 \mu F \text{ 10 } \mu F \text{ is a good target.} \quad (18)$$

### CHARGER DESIGN EXAMPLE

#### Design Conditions and Parameters for Charger:

Vout: 4.6 V; (OUT pin is input to charger)

Fast-charge current, I<sub>PGM</sub>: 1 A

DPPM-OUT threshold: 4.3 V; (charging current reduces when OUT falls to this level)

Safety timer: 5 h

Battery short circuit delay, t<sub>DELAY</sub>: 47  $\mu$ s; (Delays BAT short circuit during hot plug of battery)

TS temperature range: disabled

K<sub>SET</sub>=400; V<sub>SET</sub>=2.5 V; K<sub>DPPM</sub> = 1.15; I<sub>DPPM</sub> = 100  $\mu$ A; K<sub>TMR</sub>=0.36 s/ $\Omega$

#### Program Fast-Charge Current Level:

$$R_{ISET} = \frac{K_{SET} \times V_{SET}}{I_{PGM}} = 1 \text{ k}\Omega \quad (19)$$

#### Program DPPM\_OUT Voltage Level (Level at Which Charging Current Reduces)

$$R_{DPPM} = \frac{V_{DPPM\_OUT}}{K_{DPPM} \times I_{DPPM}} = 3.74 \text{ k}\Omega \quad (20)$$

**Program BAT Short-Circuit Delay (Used for Inserting Battery)**

$$C_{\text{DPPM}} = t_{\text{DELAY}} \times I_{\text{DPPM}} = 4.7 \text{ Nf} \quad (21)$$

**Program 5-Hour Safety Timer**

$$R_{\text{TMR}} = \frac{t_{\text{SAFETY-HR}} \times 3600 \text{ sec/hr}}{K_{\text{TMR}}} = 50 \text{ k}\Omega \quad (22)$$

**Disable/Program TS**

$R_{\text{TS}} = 49.9 \text{ k}\Omega$ – fixed resistor to disable TS input.

$$V_{\text{TS}} = I_{\text{TS}} \times R_{\text{TS}} = 20 \mu\text{A} \times 49.9 \text{ k}\Omega = 0.998 \text{ V}$$

The TS pin has a 20- $\mu\text{A}$  current source output that biases the resistor or thermistor. If  $V_{\text{TS}}$  is within the 0.5- to 2.5-V window, normal operation is allowed. If a 503AT thermistor is used, the typical range is 4°C to 41°C.

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS65800RTQR     | ACTIVE        | QFN          | RTQ                | 56   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -40 to 85    | TPS<br>65800            | <a href="#">Samples</a> |
| TPS65800RTQRG4   | ACTIVE        | QFN          | RTQ                | 56   |                | TBD                        | Call TI                 | Call TI              | -40 to 85    |                         | <a href="#">Samples</a> |
| TPS65800RTQT     | ACTIVE        | QFN          | RTQ                | 56   | 250            | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -40 to 85    | TPS<br>65800            | <a href="#">Samples</a> |
| TPS65800RTQTG4   | ACTIVE        | QFN          | RTQ                | 56   |                | TBD                        | Call TI                 | Call TI              | -40 to 85    |                         | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

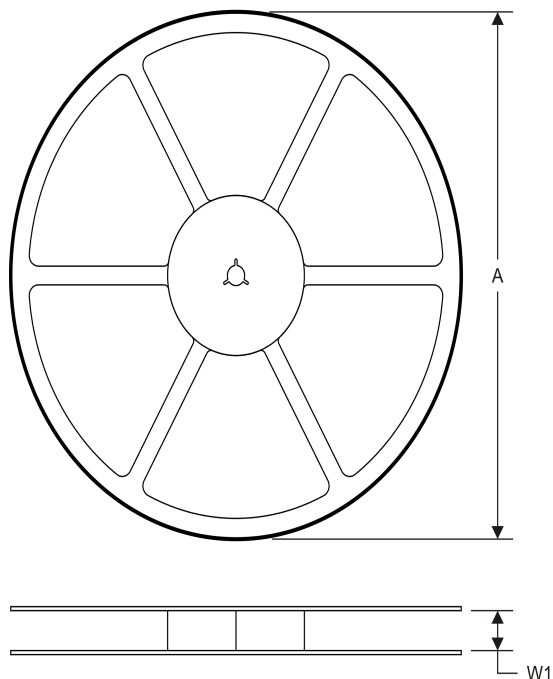
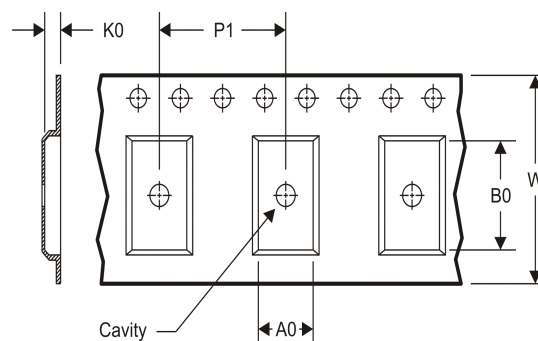
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


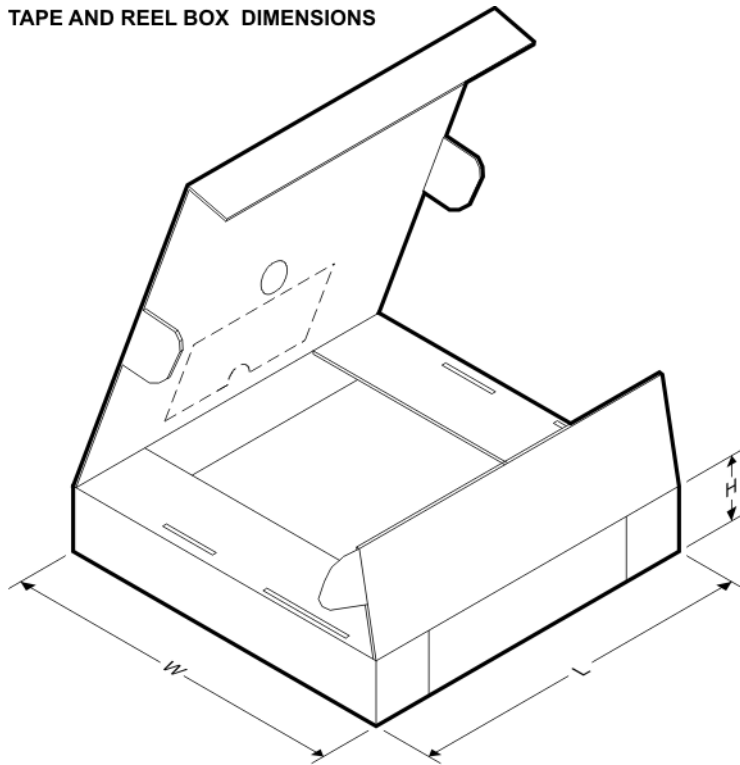
|    |                                                           |
|----|-----------------------------------------------------------|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS65800RTQR | QFN          | RTQ             | 56   | 2000 | 330.0              | 16.4               | 8.3     | 8.3     | 2.25    | 12.0    | 16.0   | Q2            |
| TPS65800RTQT | QFN          | RTQ             | 56   | 250  | 180.0              | 16.4               | 8.3     | 8.3     | 2.25    | 12.0    | 16.0   | Q2            |

## TAPE AND REEL BOX DIMENSIONS



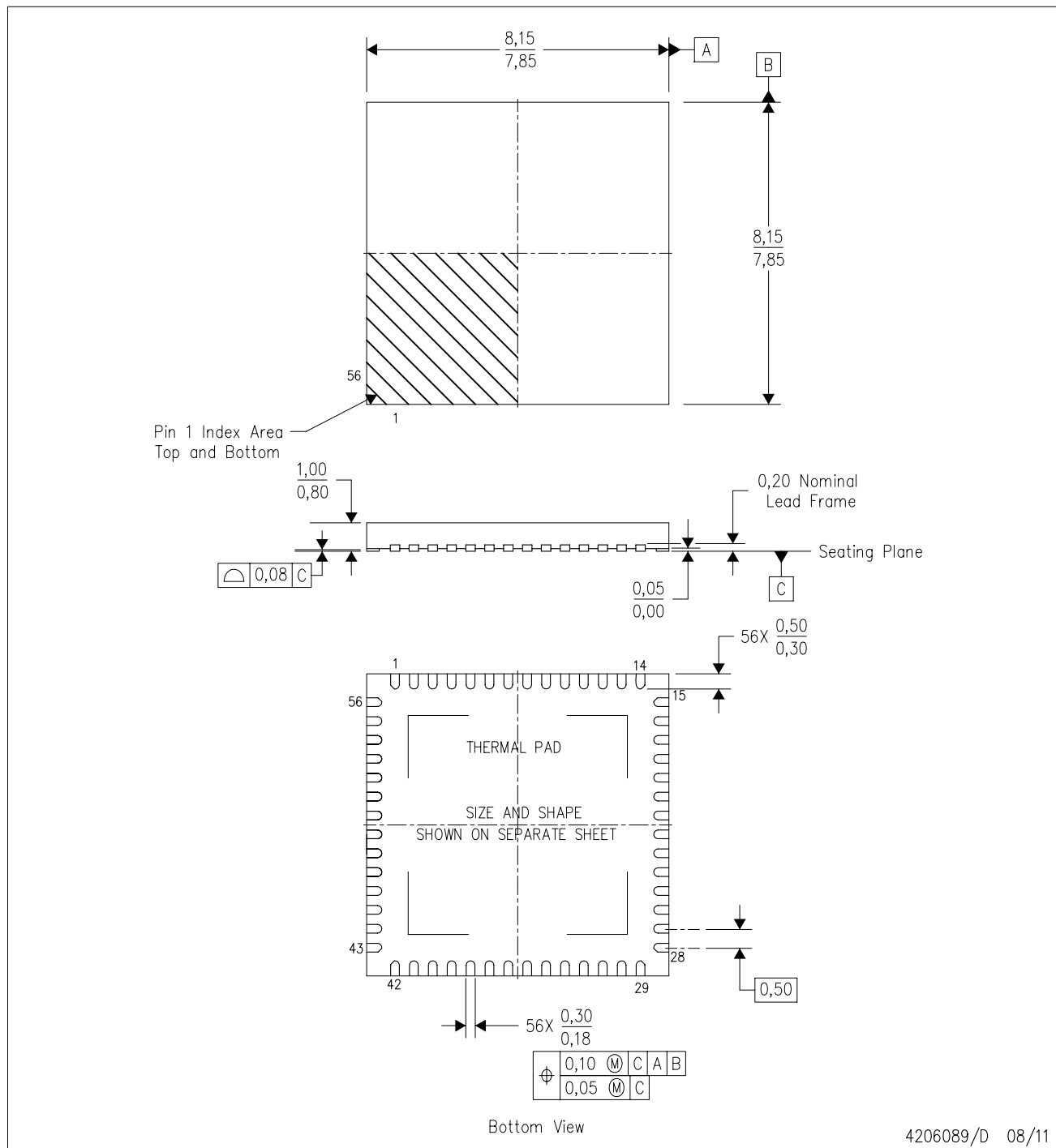
\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS65800RTQR | QFN          | RTQ             | 56   | 2000 | 367.0       | 367.0      | 38.0        |
| TPS65800RTQT | QFN          | RTQ             | 56   | 250  | 210.0       | 185.0      | 35.0        |



RTQ (S-PVQFN-N56)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) Package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F. Package complies to JEDEC MO-220.

RTQ (S-PVQFN-N56)

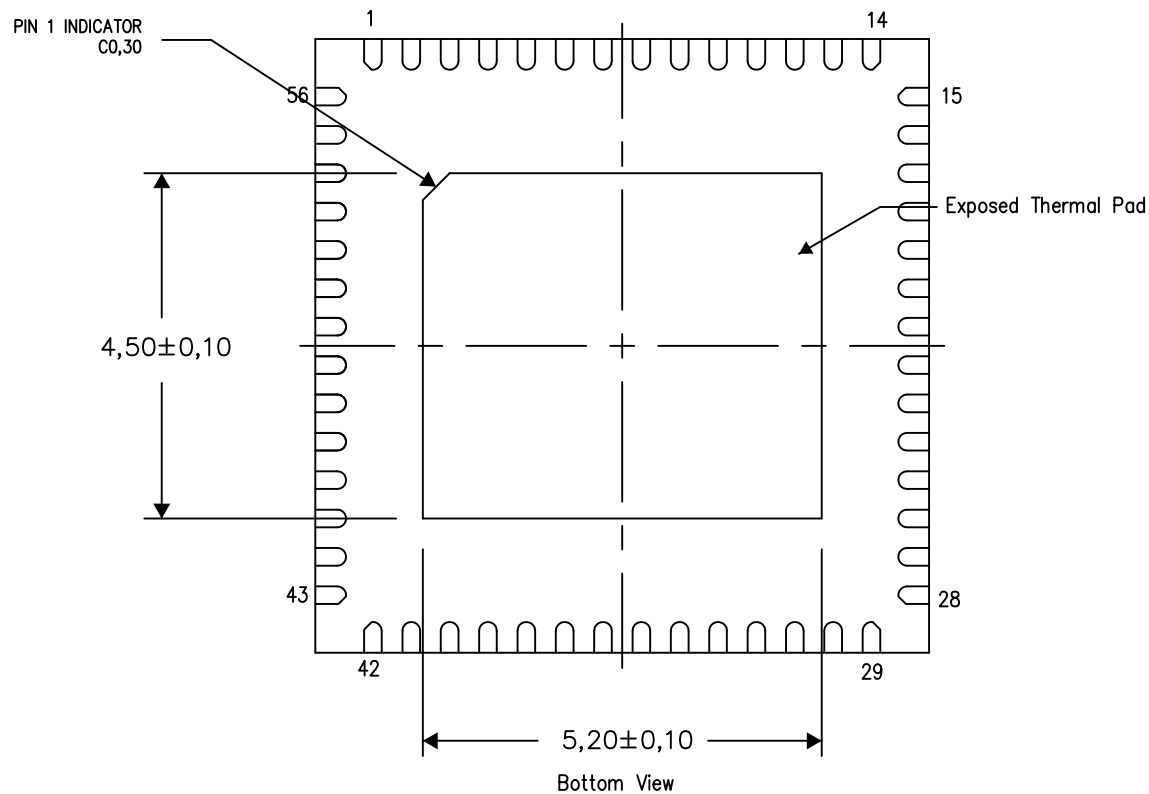
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206252-2/P 10/13

NOTE: All linear dimensions are in millimeters

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