

EB51F5G30DV-10.000M

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REGULATORY COMPLIANCE (Data Sheet downloaded on Mar 1, 2017)



ITEM DESCRIPTION

Temperature Compensated Quartz Crystal Clock Oscillators TCXO HCMOS (CMOS) 5.0Vdc 14-Pin DIP Metal Thru-Hole 10.000MHz $\pm 1.0\text{ppm}$ Maximum $\pm 3.0\text{ppm}$ Maximum -30°C to $+75^{\circ}\text{C}$

ELECTRICAL SPECIFICATIONS

Nominal Frequency	10.000MHz
Initial Tolerance	$\pm 1.0\text{ppm}$ Maximum (Measured at Nominal Vdd and Vc)
Frequency Stability	$\pm 3.0\text{ppm}$ Maximum
Frequency Stability vs. Input Voltage	$\pm 0.3\text{ppm}$ Maximum (Vdd $\pm 5\%$)
Frequency Stability vs. Load	$\pm 0.2\text{ppm}$ Maximum ($\pm 10\%$)
Frequency Stability vs. Aging	$\pm 1\text{ppm/Year}$ Maximum (at 25°C)
Operating Temperature Range	-30°C to $+75^{\circ}\text{C}$
Supply Voltage	5.0Vdc $\pm 5\%$
Input Current	15mA Maximum (Measured at Steady State at 25°C)
Output Voltage Logic High (Voh)	Vdd-0.5Vdc Minimum
Output Voltage Logic Low (Vol)	0.5Vdc Maximum
Rise/Fall Time	6nSec Maximum (Measured at 20% to 80% of waveform)
Duty Cycle	50% $\pm 5\%$ (Measured at 50% of waveform)
Load Drive Capability	30pF HCMOS Load Maximum
Output Logic Type	CMOS
Control Voltage	2.5Vdc $\pm 2.0\text{Vdc}$
Control Voltage Range	0.0Vdc to Vdd
Frequency Deviation	$\pm 7\text{ppm}$ Minimum, $\pm 20\text{ppm}$ Maximum (Referenced to Fo at Vc=2.5Vdc; Vdd=5.0Vdc)
Linearity	$\pm 10\%$ Maximum
Internal Trim	$\pm 3\text{ppm}$ Minimum (at 25°C , Top Access)
Input Impedance	10kOhms Typical
Phase Noise	-70dBc/Hz at 10Hz Offset, -100dBc/Hz at 100Hz Offset, -130dBc/Hz at 1kHz Offset, -140dBc/Hz at 10kHz Offset, -145dBc/Hz at 100kHz Offset (Typical Values at 19.440MHz)
Storage Temperature Range	-55°C to $+125^{\circ}\text{C}$

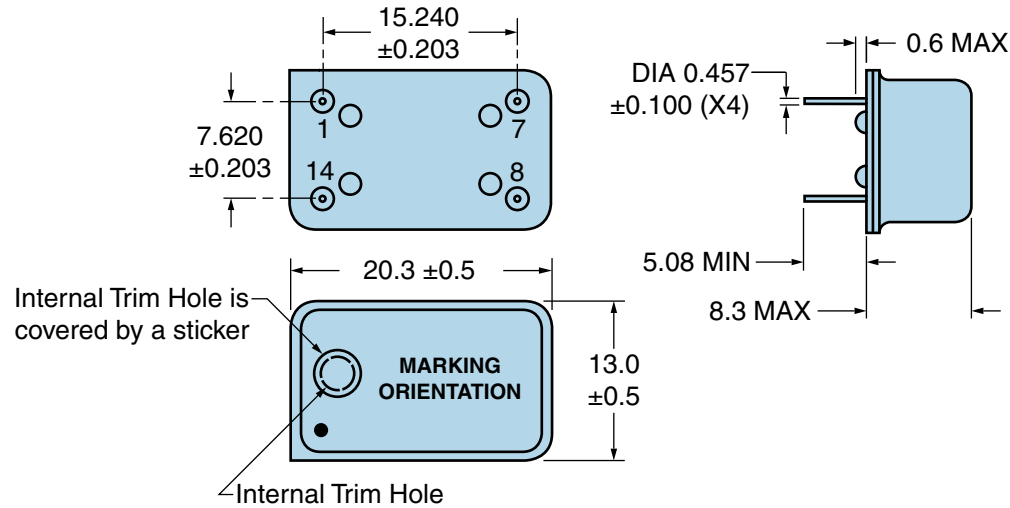
ENVIRONMENTAL & MECHANICAL SPECIFICATIONS

Fine Leak Test	MIL-STD-883, Method 1014 Condition A (Internal Crystal Only)
Gross Leak Test	MIL-STD-883, Method 1014 Condition C (Internal Crystal Only)
Lead Integrity	MIL-STD-883, Method 2004
Mechanical Shock	MIL-STD-202, Method 213 Condition C
Resistance to Soldering Heat	MIL-STD-202, Method 210
Resistance to Solvents	MIL-STD-202, Method 215
Solderability	MIL-STD-883, Method 2003
Temperature Cycling	MIL-STD-883, Method 1010
Vibration	MIL-STD-883, Method 2007 Condition A

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MECHANICAL DIMENSIONS (all dimensions in millimeters)



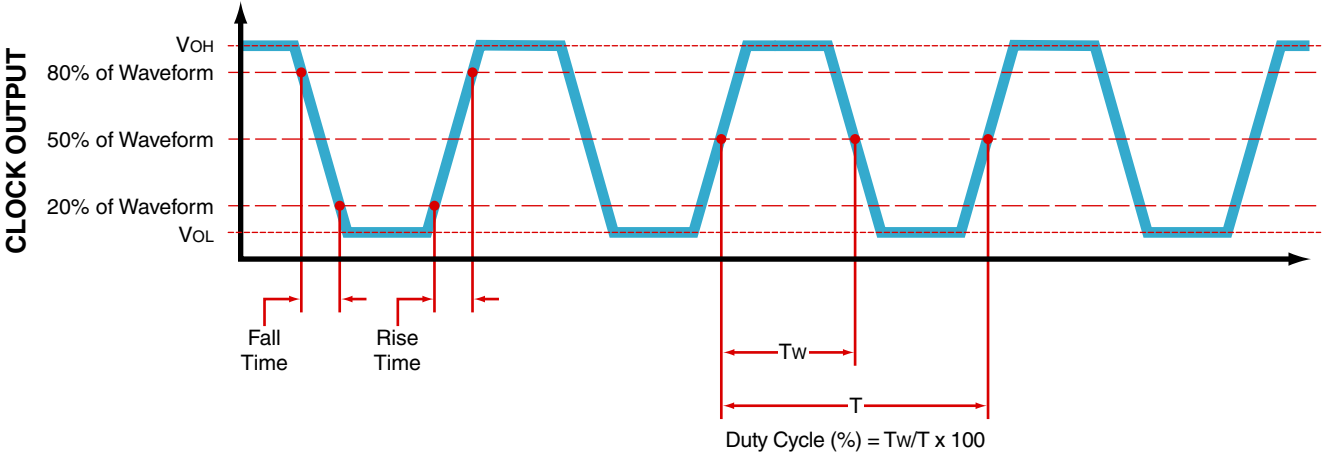
PIN	CONNECTION
1	Voltage Control
7	Case Ground
8	Output
14	Supply Voltage

LINE	MARKING
1	ECLIPTEK
2	10.000M
3	XXYYZZ XX=Ecliptek Manufacturing Code Y=Last Digit of the Year ZZ=Week of the Year

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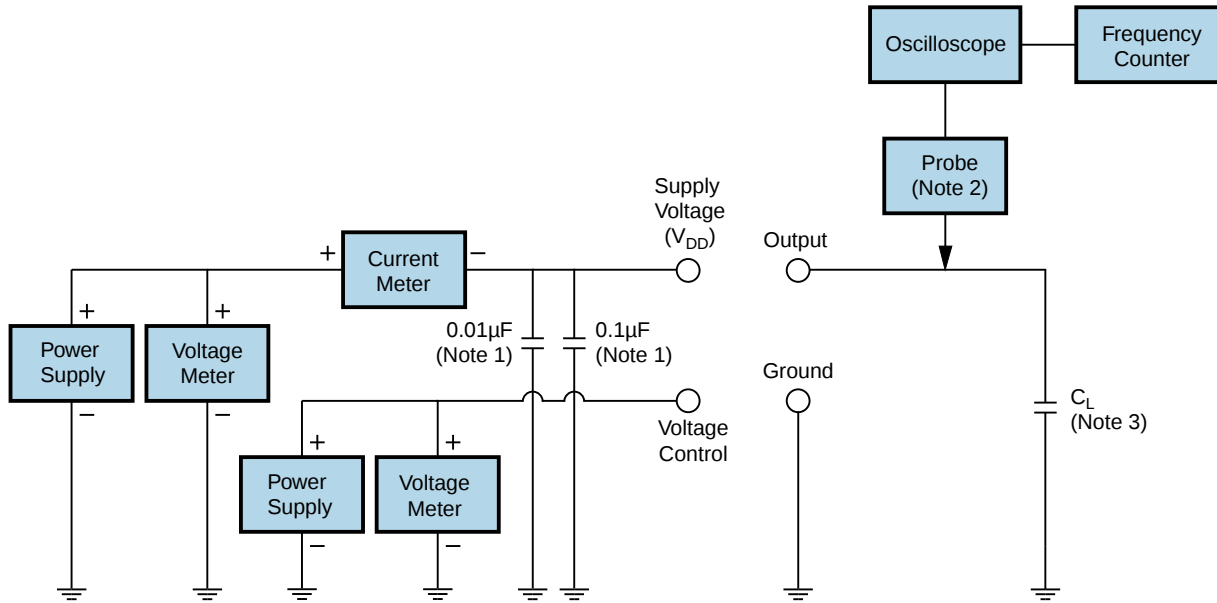
OUTPUT WAVEFORM



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Test Circuit for Voltage Control Option



Note 1: An external $0.1\mu\text{F}$ low frequency tantalum bypass capacitor in parallel with a $0.01\mu\text{F}$ high frequency ceramic bypass capacitor close to the package ground and V_{DD} pin is required.

Note 2: A low capacitance ($<12\text{pF}$), 10X attenuation factor, high impedance ($>10\text{Mohms}$), and high bandwidth ($>300\text{MHz}$) passive probe is recommended.

Note 3: Capacitance value C_L includes sum of all probe and fixture capacitance.

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Recommended Solder Reflow Methods



Low Temperature Solder Bath (Wave Solder)

TS MAX to TL (Ramp-up Rate)	5°C/Second Maximum
Preheat	
- Temperature Minimum (TS MIN)	N/A
- Temperature Typical (TS TYP)	150°C
- Temperature Maximum (TS MAX)	N/A
- Time (ts MIN)	30 - 60 Seconds
Ramp-up Rate (TL to TP)	5°C/Second Maximum
Time Maintained Above:	
- Temperature (TL)	150°C
- Time (tL)	200 Seconds Maximum
Peak Temperature (TP)	245°C Maximum
Target Peak Temperature (TP Target)	245°C Maximum 1 Time / 235°C Maximum 2 Times
Time within 5°C of actual peak (tP)	5 Seconds Maximum 1 Time / 15 Seconds Maximum 2 Times
Ramp-down Rate	5°C/Second Maximum
Time 25°C to Peak Temperature (t)	N/A
Moisture Sensitivity Level	Level 1

Low Temperature Manual Soldering

185°C Maximum for 10 Seconds Maximum, 2 times Maximum.

High Temperature Manual Soldering

260°C Maximum for 5 Seconds Maximum, 2 times Maximum.