

# HD74HC259

## 8-bit Addressable Latch

# HITACHI

ADE-205-480 (Z)  
1st. Edition  
Sep. 2000

### Description

The HD74HC259 has a single data input (D), 8 latch outputs ( $Q_0$ - $Q_7$ ), 3 address inputs (A, B, and C), a common enable input (E), and a common clear input. To operate this device as an addressable latch, data is held on the D input, and the address of the latch into which the data is to be entered is held on the A, B and C inputs. When enable is taken low the data flows through to the addressed output. The data is stored when enable transitions from low to high. All unaddressed latches will remain unaffected. With enable in the high state the device is deselected, and all latches remain in their previous state, unaffected by changes on the data or address inputs. To eliminate the possibility of entering erroneous data into the latches, the enable should be held high (inactive) while the address lines are changing.

If enable is held high and clear is taken low all eight latches are cleared to a low state. If enable is low all latches except the addressed latch will be cleared. The addressed latch will instead follow the D input, effectively implementing a 3-to-8 line decoder.

### Features

- High Speed Operation:  $t_{pd}$  (Data to Output) = 16 ns typ ( $C_L = 50$  pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage:  $V_{CC} = 2$  to 6 V
- Low Input Current: 1  $\mu$ A max
- Low Quiescent Supply Current:  $I_{CC}$  (static) = 4  $\mu$ A max ( $T_a = 25^\circ\text{C}$ )

### Function Table

Inputs				
Clear	G	Output of Addressed Latch	Each Other Output	Function
H	L	D	$Q_{io}$	Addressable latch
H	H	$Q_{io}$	$Q_{io}$	Memory
L	L	D	L	8-line demultiplexer
L	H	L	L	Clear

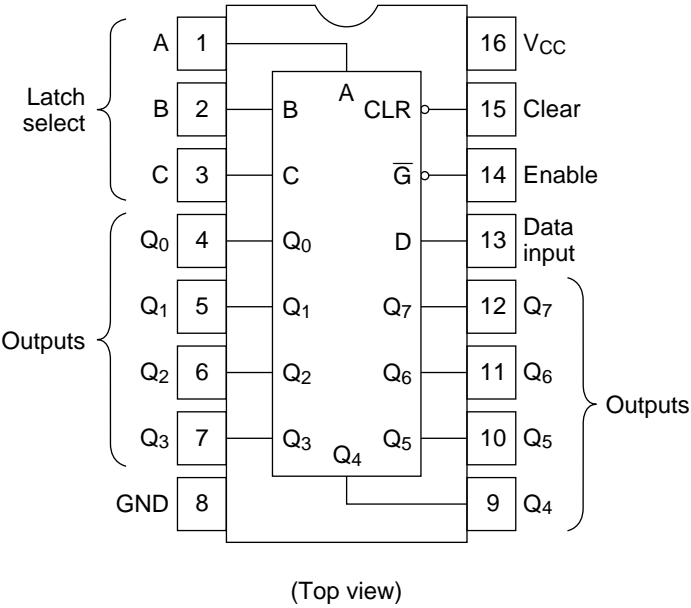
# HD74HC259

## Select Inputs

C	B	A	Latch Addressed
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

- Notes:
1. D: the level at the data input
  2. Q<sub>i</sub>: the level of Q<sub>i</sub> (i = 0, 1, ..., 7, as appropriate) before the indicated steady-state input conditions were established.

## Pin Arrangement



## DC Characteristics

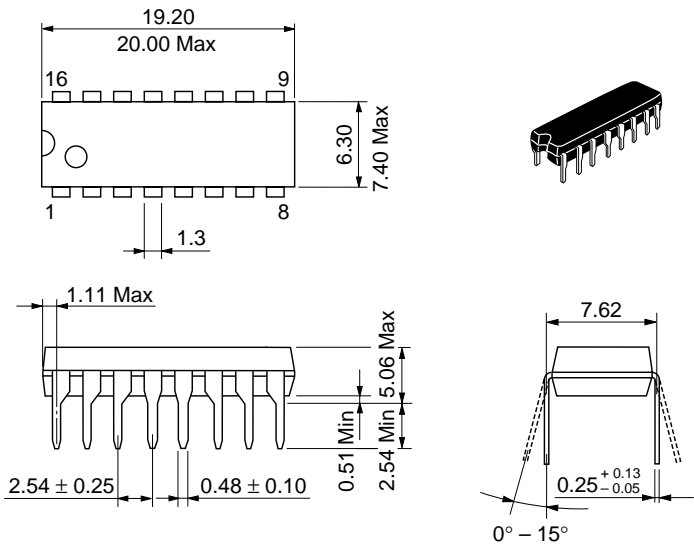
Item	Symbol	V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V <sub>IH</sub>	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V <sub>IL</sub>	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V <sub>OH</sub>	2.0	1.9	2.0	—	1.9	—	V	Vin = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = -20 μA	
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			I <sub>OH</sub> = -4 mA
		6.0	5.68	—	—	5.63	—			I <sub>OH</sub> = -5.2 mA
	V <sub>OL</sub>	2.0	—	0.0	0.1	—	0.1	V	Vin = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 20 μA	
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			I <sub>OL</sub> = 4 mA
		6.0	—	—	0.26	—	0.33			I <sub>OL</sub> = 5.2 mA
Input current	I <sub>in</sub>	6.0	—	—	±0.1	—	±1.0	μA	Vin = V <sub>CC</sub> or GND	
Quiescent supply current	I <sub>CC</sub>	6.0	—	—	4.0	—	40	μA	Vin = V <sub>CC</sub> or GND, I <sub>out</sub> = 0 μA	

AC Characteristics (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Item	Symbol	V <sub>cc</sub> (V)	Ta = 25°C		Ta = -40 to +85°C		Unit	Test Conditions
			Min	Typ	Max	Min		
Propagation delay time	t <sub>PHL</sub>	2.0	—	—	185	—	ns	Data to output
		4.5	—	16	37	—		
		6.0	—	—	31	—		
	t <sub>PLH</sub>	2.0	—	—	215	—		Latch select to output
		4.5	—	20	43	—		
		6.0	—	—	37	—		
		2.0	—	—	200	—		Enable to output
		4.5	—	17	40	—		
		6.0	—	—	34	—		
		6.0	—	—	34	—		
	t <sub>PHL</sub>	2.0	—	—	155	—	ns	Clear to output
		4.5	—	15	31	—		
		6.0	—	—	26	—		
Pulse width	t <sub>w</sub>	2.0	80	—	—	100	ns	Clear, Enable
		4.5	16	6	—	20		
		6.0	14	—	—	17		
Setup time	t <sub>su</sub>	2.0	100	—	—	125	ns	Latch select or data to enable
		4.5	20	5	—	25		
		6.0	17	—	—	21		
Hold time	t <sub>h</sub>	2.0	5	—	—	5	ns	Latch select or data to enable
		4.5	5	-1	—	5		
		6.0	5	—	—	5		
Output rise/fall time	t <sub>TLH</sub>	2.0	—	—	75	—	ns	
	t <sub>THL</sub>	4.5	—	5	15	—		
		6.0	—	—	13	—		
Input capacitance	C <sub>in</sub>	—	—	5	10	—	10	pF

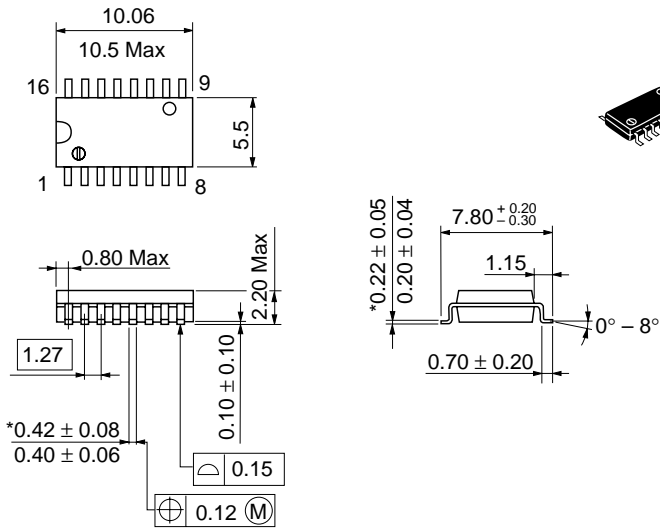
Package Dimensions

Unit: mm



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	1.07 g

Unit: mm



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.24 g

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**Hitachi, Ltd.**

Semiconductor & Integrated Circuits.  
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan  
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL	North America	: <a href="http://semiconductor.hitachi.com/">http://semiconductor.hitachi.com/</a>
	Europe	: <a href="http://www.hitachi-eu.com/hel/ecg">http://www.hitachi-eu.com/hel/ecg</a>
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**For further information write to:**

Hitachi Semiconductor  
(America) Inc.  
179 East Tasman Drive,  
San Jose, CA 95134  
Tel: <1> (408) 433-1990  
Fax: <1> (408) 433-0223

Hitachi Europe GmbH  
Electronic Components Group  
Dornacher Straße 3  
D-85622 Feldkirchen, Munich  
Germany  
Tel: <49> (89) 9 9180-0  
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.  
Electronic Components Group.  
Whitebrook Park  
Lower Cookham Road  
Maidenhead  
Berkshire SL6 8YA, United Kingdom  
Tel: <44> (1628) 585000  
Fax: <44> (1628) 585160

Hitachi Asia Ltd.  
Hitachi Tower  
16 Collyer Quay #20-00,  
Singapore 049318  
Tel: <65>-538-6533/538-8577  
Fax: <65>-538-6933/538-3877  
URL: <http://www.hitachi.com.sg>

Hitachi Asia Ltd.  
(Taipei Branch Office)  
4/F, No. 167, Tun Hwa North Road,  
Hung-Kuo Building,  
Taipei (105), Taiwan  
Tel: <886>-(2)-2718-3666  
Fax: <886>-(2)-2718-8180  
Telex: 23222 HAS-TP  
URL: <http://www.hitachi.com.tw>

Hitachi Asia (Hong Kong) Ltd.  
Group III (Electronic Components)  
7/F., North Tower,  
World Finance Centre,  
Harbour City, Canton Road  
Tsim Sha Tsui, Kowloon,  
Hong Kong  
Tel: <852>-(2)-735-9218  
Fax: <852>-(2)-730-0281  
URL: <http://www.hitachi.com.hk>

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