



STEVAL-PCC011V1

ST802RT1B Ethernet PHY demonstration board

Data brief

Features

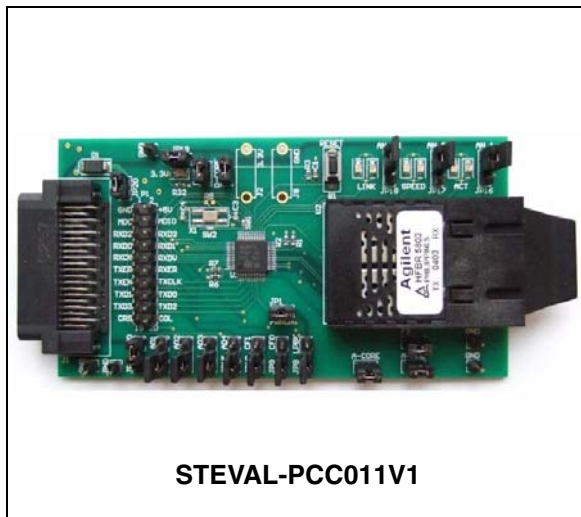
- ST802RT1B fast Ethernet physical layer transceiver
- On-board 3.3 V LDO regulator
- On-board 25 MHz crystal
- 12 jumpers for boot-strap configuration (MII address, auto-negotiation, loopback, power down, MII/RMII configuration)
- GND test points and jumpers for power consumption measurement
- Connectors:
 - 20-pin full pitch header connector for debugging (compatible with STM32F107 controller board)
 - 40-pin connector compatible with the Spirent Communications SmartBits 200/2000 (SMB-200/ SMB-2000) analysis system
 - Optical transceiver connector
- RoHS compliant

Description

The STEVAL-PCC011V1 demonstration board is designed as an evaluation platform for the ST802RT1B, Fast Ethernet physical layer (PHY) interface supporting 100BASE-FX applications. The PHY provides a media independent interface (MII) and reduced media independent interface (RMII) for easy attachment to 10/100 media access controllers (MAC).

Many jumpers, test points and connectors on the demonstration board allow testing of the features provided by the ST802RT1B Ethernet PHY.

An additional header connector allows connection to the STM32F107 controller demonstration board (not included with the STEVAL-PCC011V1), providing the capability for quick evaluation of the complete application – microcontroller and the physical layer.



STEVAL-PCC011V1

The controller board is pre-Flashed with a web server demonstration.

The STM32F107 controller demonstration board is available separately through order code STEVAL-PCC010V1.

1 Schematic diagrams

Figure 1. ST802RT1 FX mode Ethernet PHY demonstration board schematic - part 1

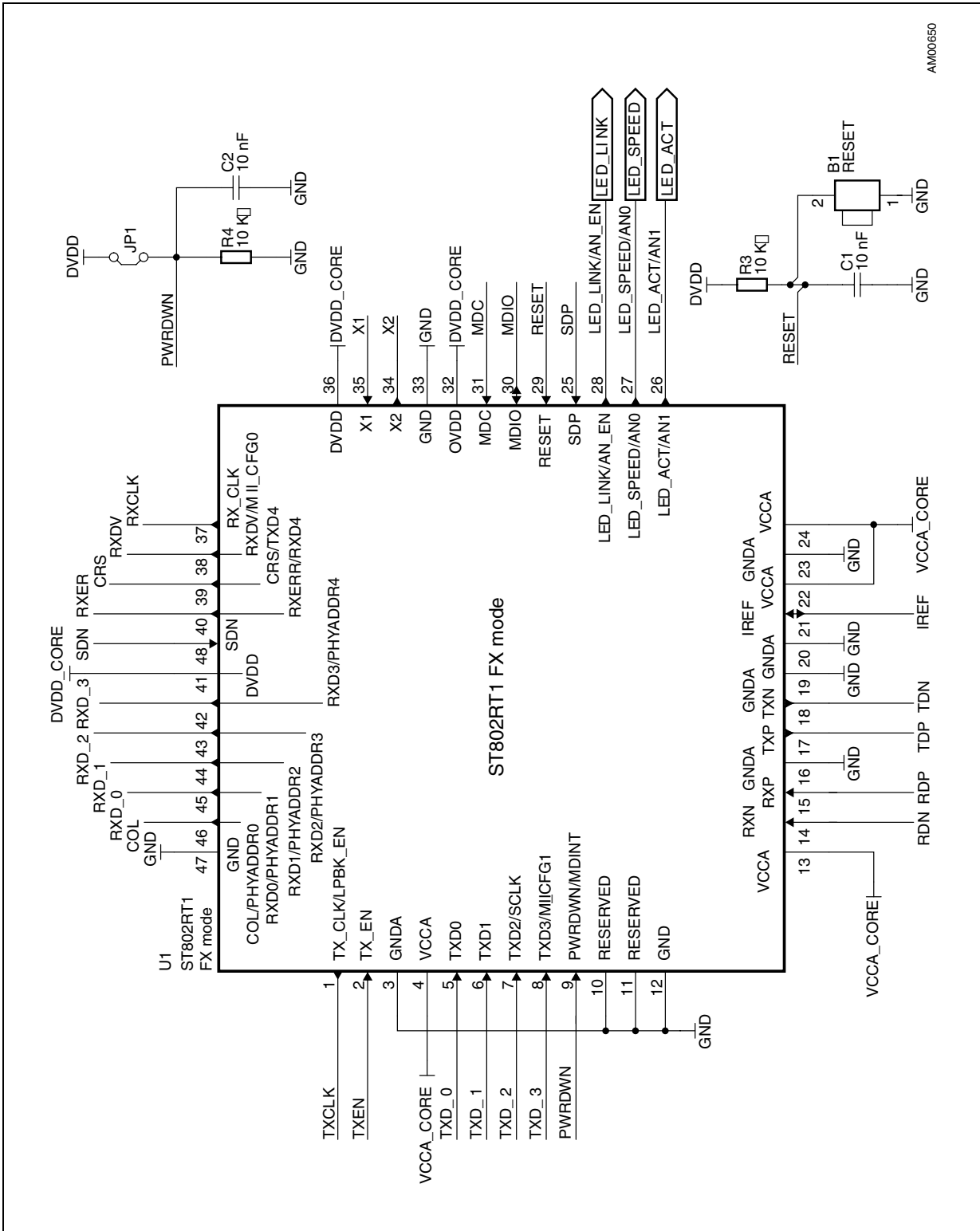
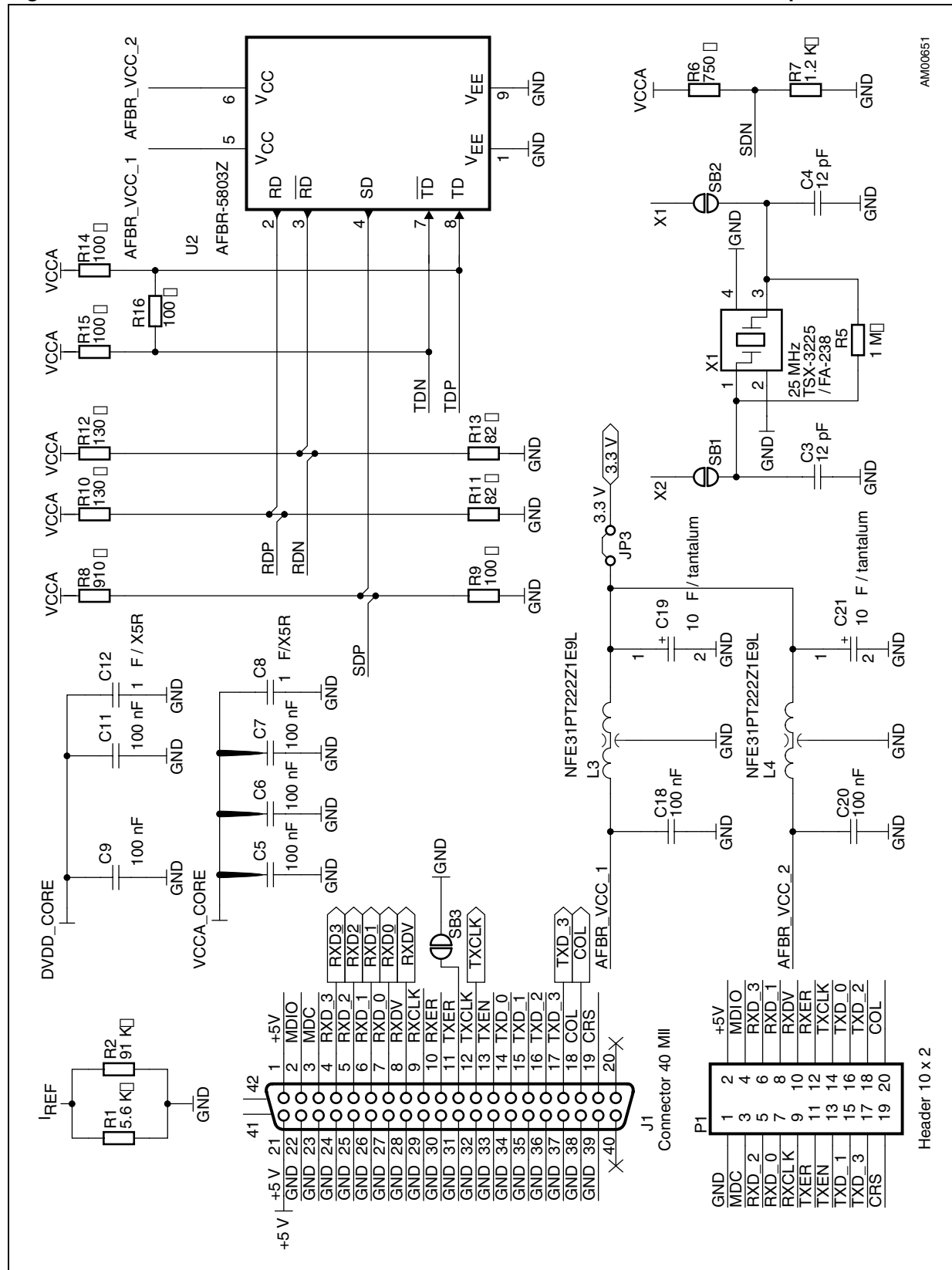


Figure 2. ST802RT1 FX mode Ethernet PHY demonstration board schematic - part 2



The schematic diagram illustrates the internal circuitry of the AM00646 module, organized into several functional blocks:

- Power Input and Regulation:** A +5V input is connected to a diode (D1) and a 10F/6.3V tantalum capacitor (C13). The signal passes through a 2-pin header (JP20) to the V_{IN} pin of a voltage regulator (U3, LD1117S33). The regulator's output (V_{OUT}) is filtered by a 100nF capacitor (C14) and a 10F/6.3V tantalum capacitor (C15) before reaching the 3.3V LDO (JP19).
- 3.3V LDO and Filtering:** The 3.3V LDO output is connected to a 3.3V pin header (JP19) and a 10F/6.3V tantalum capacitor (C16).
- LEDs and Status Indicators:** Three LEDs (LED1, LED2, LED3) are connected to the 3.3V LDO output through current-limiting resistors (R26, R27, R28). LED1 is labeled "Yellow", LED2 "Red", and LED3 "Green". Each LED is connected to a 2-pin header (JP16, JP17, JP18) and a 3.3V pin header (JP19).
- Signal Processing and Control:** The module includes several signal pins (TXCLK, TXDV, TXD_3, TXD_2, TXD_1, TXD_0, RXDV, RXD_3, RXD_2, RXD_1, RXD_0, COL, LED_LINK, LED_LINK_EN, LED_SPEED, LED_SPEED_AN0, LED_ACT, LED_ACT_AN1) connected to various components like resistors (R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32), capacitors (C13, C14, C15, C16), and headers (JP1, JP2, JP3, JP4, JP5, JP6, JP7, JP8, JP9, JP10, JP11, JP12, JP13, JP14, JP15, JP16, JP17, JP18, JP19, JP20).
- Grounding and Power Distribution:** The module is powered by a 3.3V supply connected to a 3.3V pin header (JP19). The ground (GND) is connected to a GND pin header (JP20).

2 Revision history

Table 1. Document revision history

Date	Revision	Changes
22-Feb-2010	1	Initial release.

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