M61532FP

8ch Electronic Volume with 9 Input Selector

REJ03F0041-0100Z
Rev.1.0
Sep.19.2003

Feature

FUNCTION	FEATURE
Electric Volume	8channel independent Electric Volume with High Voltage Transistor. (0~-99.0dB/0.5dBstep,-∞dB)
Twin Input Selector	Front L/R channel has twin 9 Input Selector.(Main & Sub)
Multi Channel Input Selector	Every channel has 2 Input Selector and Input Gain Control
Input Gain Control	Input Gain Control (0/+6/+12/+18dB)
REC Output	2 Lines REC Output (Both L and R channels)
Output Gain Control	Output Gain Control (0/+6/+12/+18dB)
Output for ADC	Built-in Single-end output (for ADC)
Input ATT	Input ATT (for ADC:0/-6/-12/-18dB)

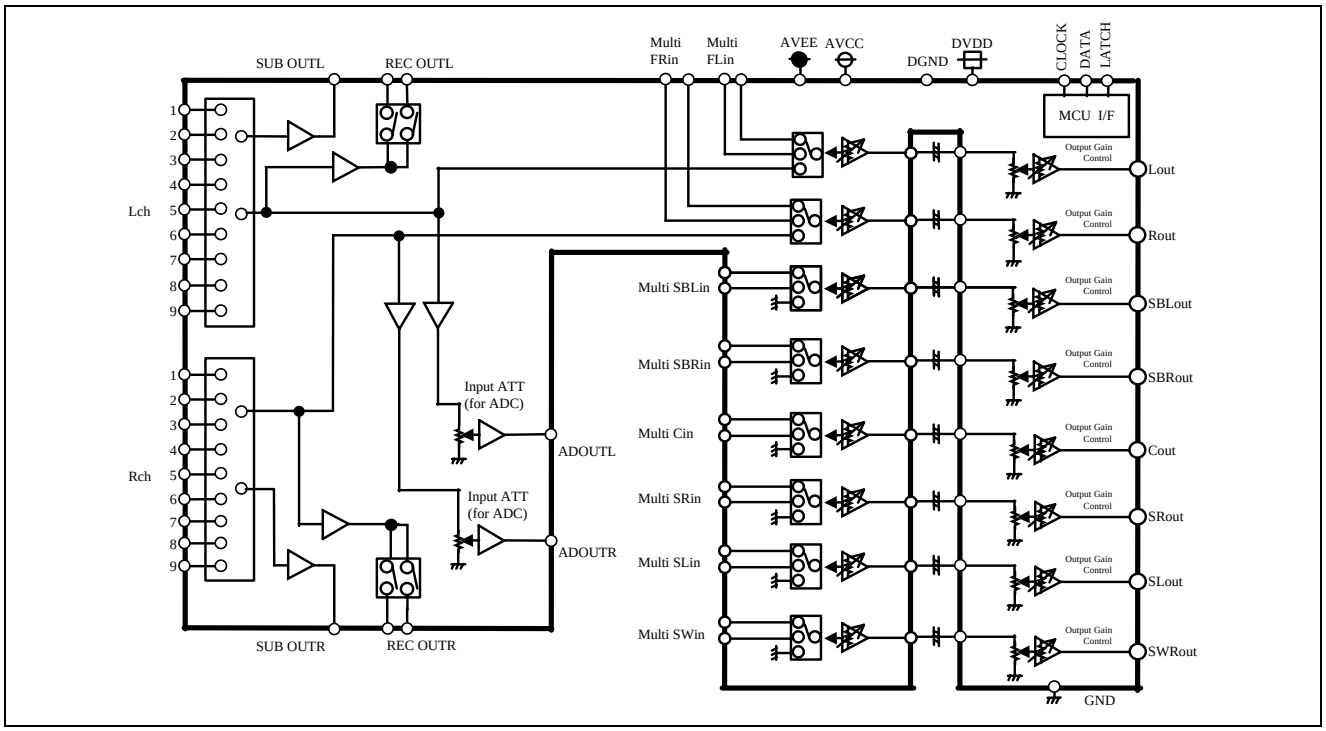
Application

Receiver,AV Amp,Mini Stereo etc.

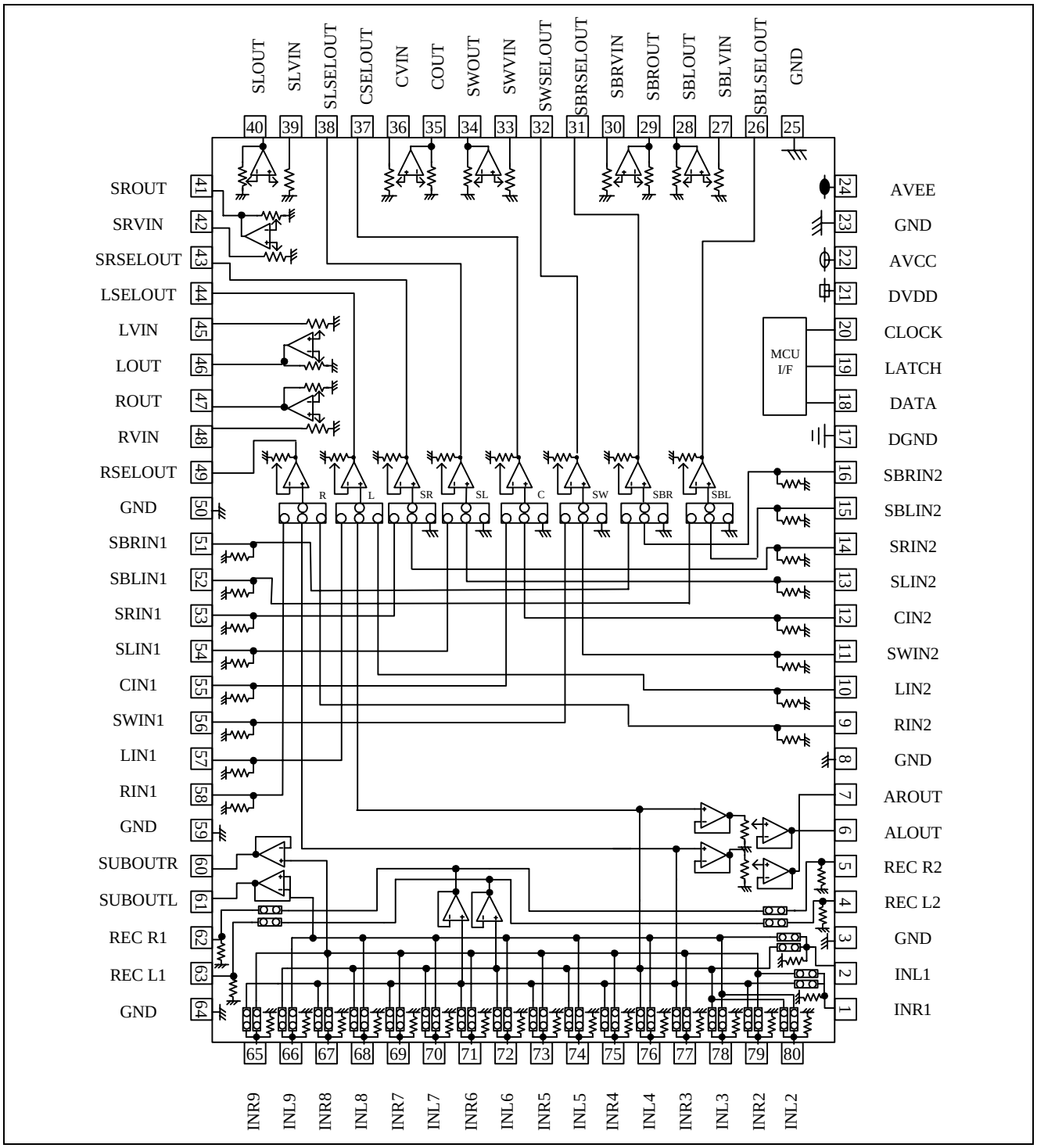
Recommended Operating Condition

Supply Voltage Range AVCC=7.0V(typ) , AVEE=-7.0V(typ) , DVDD=2.7~5.5V

System Block Diagram



Block Diagram and Pin Configuration (Top View)

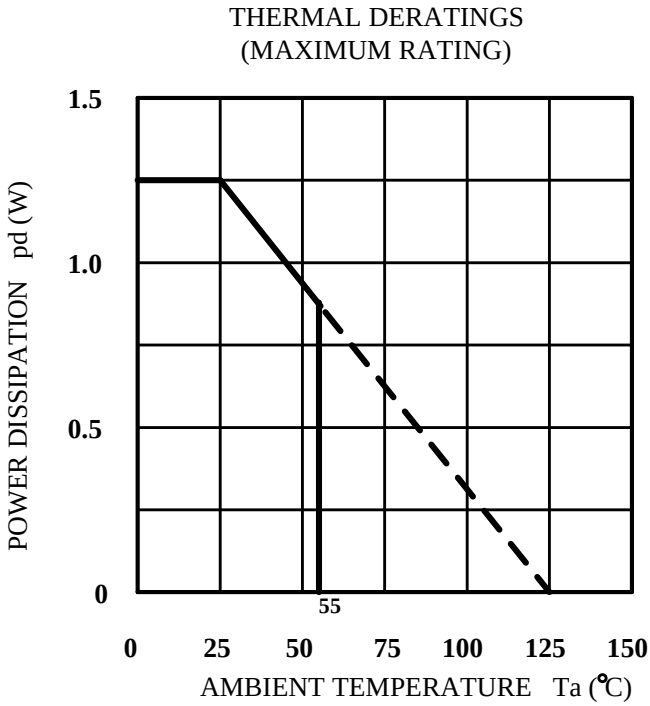


Pin Description

PIN No.	Name	Function
2,80,78,76,74,72,70,68,66,	INL1,2,3,4,5,6,7,8,9	Input pin of L channel (Input Selector)
1,79,77,75,73,71,69,67,65	INR1,2,3,4,5,6,7,8,9	Input pin of R channel (Input Selector)
3,8,23,25,50,59,64	GND1,2,3,4,5,6,7,	Analog Ground
63,4,62,5	REC L1/L2/R1/R2	Output pin of REC L/R
6	ALOUT	Output pin of L channel for ADC(Single ended)
7	AROUT	Output pin of R channel for ADC(Single ended)
9	RIN2	Input pin of R channel
10	LIN2	Input pin of L channel
11	SWIN2	Input pin of SW channel
12	CIN2	Input pin of C channel
13	SLIN2	Input pin of SL channel
14	SRIN2	Input pin of SR channel
15	SBLIN2	Input pin of SBL channel
16	SBRIN2	Input pin of SBR channel
17	DGND	Ground of internal logic circuit
18	DATA	Input pin of Control Data
19	LATCH	Input pin of Control Trigger
20	CLOCK	Input pin of Control Clock
21	DVDD	Power supply to internal logic circuit
22	AVCC	Positive power supply to internal analog circuit
24	AVEE	Negative power supply to internal analog circuit
26	SBLSELOUT	Output pin of SBL channel volume input selector
27	SBLVIN	Input pin of SBL channel volume
28	SBLOUT	Output pin of SBL channel
29	SBROUT	Output pin of SBR channel
30	SBRVIN	Input pin of SBR channel volume
31	SBRSELOUT	Output pin of SBR channel volume input selector
32	SWSELOUT	Output pin of SW channel volume input selector
33	SWVIN	Input pin of SW channel volume
34	SWOUT	Output pin of SW channel
35	COUT	Output pin of C channel
36	CVIN	Input pin of C channel volume
37	CSELOUT	Output pin of C channel volume input selector
38	SLSELOUT	Output pin of SL channel volume input selector
39	SLVIN	Input pin of SL channel volume
40	SLOUT	Output pin of SL channel
41	SROUT	Output pin of SR channel
42	SRVIN	Input pin of SR channel volume
43	SRSELOUT	Output pin of SR channel volume input selector
44	LSELOUT	Output pin of L channel volume input selector
45	LVIN	Input pin of L channel volume
46	LOUT	Output pin of L channel
47	ROUT	Output pin of R channel
48	RVIN	Input pin of R channel volume
49	RSELOUT	Output pin of R channel volume input selector
51	SBRIN1	Input pin of SBR channel
52	SBLIN1	Input pin of SBL channel
53	SRIN1	Input pin of SR channel
54	SLIN1	Input pin of SL channel
55	CIN1	Input pin of C channel
56	SWIN1	Input pin of SW channel
57	LIN1	Input pin of L channel
58	RIN1	Input pin of R channel
60	SUBOUTR	Sub Output pin of R channel
61	SUBOUTL	Sub Output pin of L channel

Absolute Maximum Ratings

Symbol	Parameter	Condition	Ratings	Unit
Supply voltage	Power supply	AVCC-AVEE	±8.0	V
		DVDD-GND	6.0	
Pd	Power dissipation	Ta≤25°C	1250	mW
Kθ	Thermal derating	Ta>25°C	12.5	mW/°C
Topr	Operating temperature		-20~+55	°C
Tstg	Storage temperature		-40~+125	°C



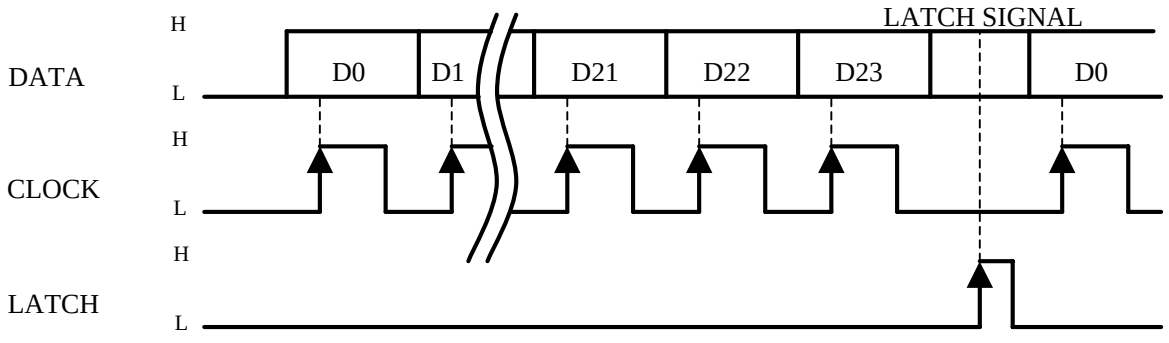
Recommended Operating Conditions

(Ta=25°C, unless otherwise noted)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Analog supply voltage (Positive)	AVCC		4.5	7.0	7.5	V
Analog supply voltage (Negative)	AVEE		-7.5	-7.0	-4.5	V
Digital supply voltage	DVDD		2.7	3.3	5.5	V
Logic “H” level input voltage	VIH	DGND reference	DVDD x 0.7	—	DVDD	V
Logic “L” level input voltage	VIL	DGND reference	DGND	—	DVDD x 0.2	V

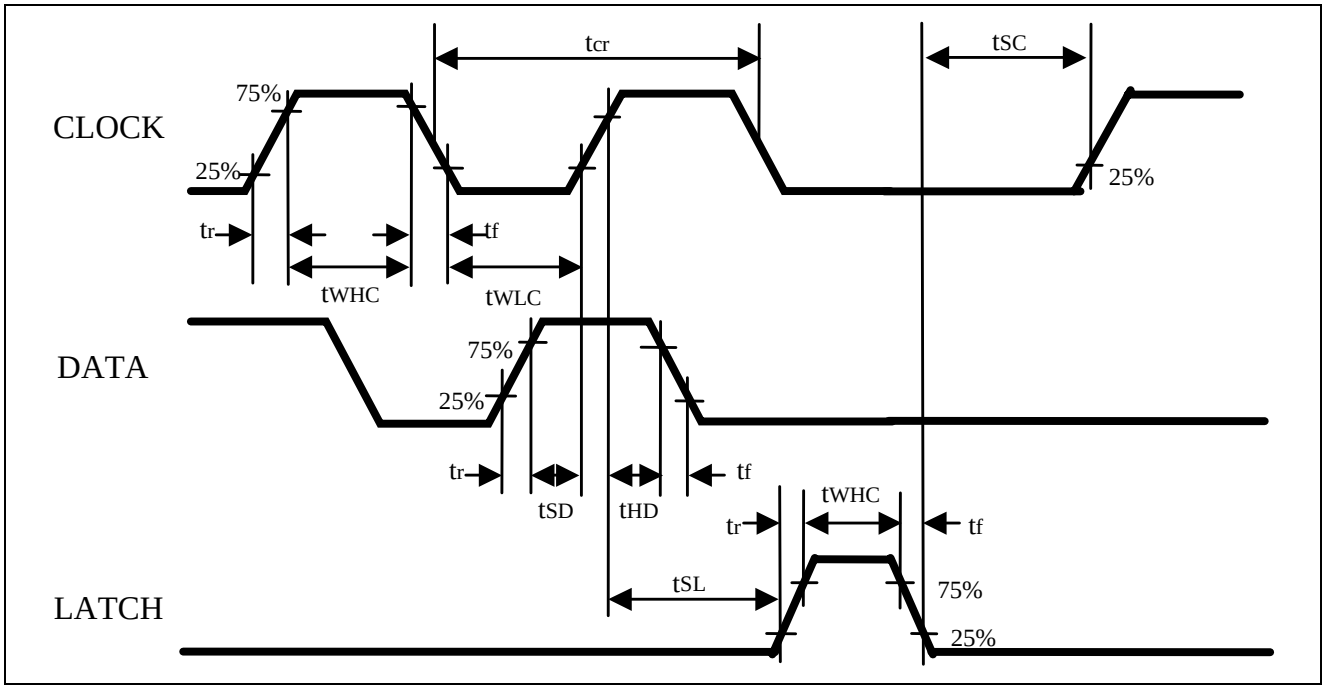
Note:VEE≤DGND≤VDD≤VCC

Relationship Between Data and Clock



DATA signal is read at the rising edge of CLOCK.
Serial data (D0 – D23) is loaded at the rising edge of the LATCH signal.

Clock and Data Timings

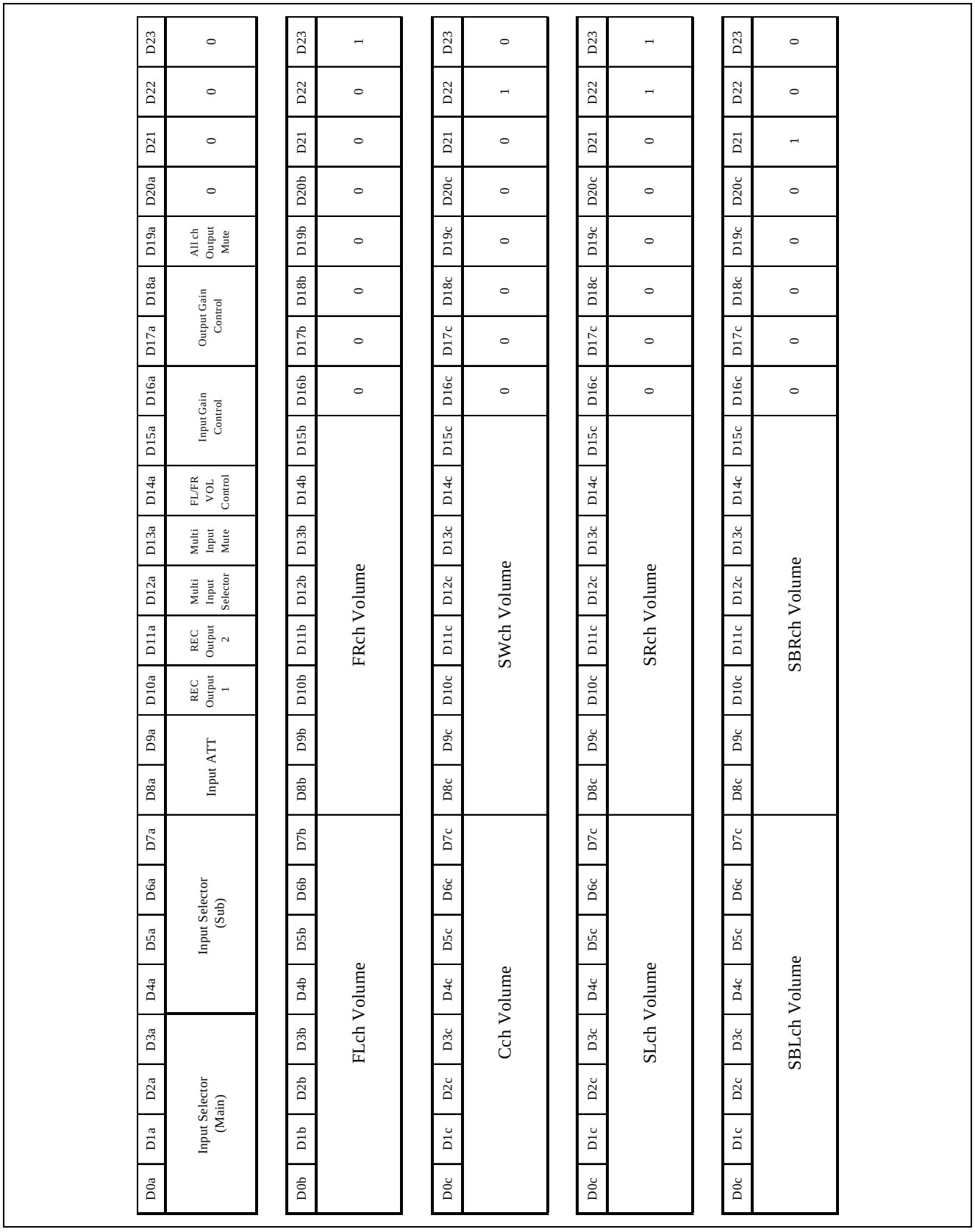


Timing Definition of Digital Block

		Limits			
Symbol	**Parameter**	**Min**	**typ**	**Max**	**Unit**
tcr	Clock cycle time	4	—	—	µsec
tWHC	Clock pulse width (“H” level)	1.6	—	—	
tWLC	Clock pulse width (“L” level)	1.6	—	—	
tr	Rising time of clock,data and latch	—	—	0.4	
tf	Falling time of clock,data and latch	—	—	0.4	
tSD	Data setup time	0.8	—	—	
tHD	Data hold time	0.8	—	—	
tSL	Latch setup time	1	—	—	
tWHL	Latch pulse width	1.6	—	—	
tSC	Clock setup time	4	—	—	

Data Control Specification

Initialize all data of the 5 formats when Digital Power supply (DVDD) turn on.



Setting Code

(1) Input Selector

Setting	Main	D0a	D1a	D2a	D3a
	Sub	D4a	D5a	D6a	D7a
ALL OFF		0	0	0	0
IN1		0	0	0	1
IN2		0	0	1	0
IN3		0	0	1	1
IN4		0	1	0	0
IN5		0	1	0	1
IN6		0	1	1	0
IN7		0	1	1	1
IN8		1	0	0	0
IN9		1	0	0	1

(2) Input ATT

Setting	D8a	D9a
0dB	0	0
-6dB	0	1
-12dB	1	0
-18dB	1	1

(3) REC Output

REC Output	REC1	REC2
Setting	D10a	D11a
OFF	0	0
ON	1	1

(4) Multi Input

Setting	D12a
Multi In1	0
Multi In2	1

(5) Multi Input Mute (Except For FL/FR)

Setting	D13a
Mute OFF depend on (4) Multi Input	0
Mute ON	1

(6) FL/FR VOL Input

Setting	D14a
Bypass	0
Multi Input	1

(7) Input Gain Control

Setting	D15a	D16a
0dB	0	0
+6dB	0	1
+12dB	1	0
+18dB	1	1

(8) Output Gain Control

Setting	D17a	D18a
0dB	0	0
+6dB	0	1
+12dB	1	0
+18dB	1	1

(9) All Ch Output Mute

Setting	D19a
Mute off	0
Mute on	1

It's initial setting when power is turned on.

(9)6 channel Volume

ATT		D0b	D1b	D2b	D3b	D4b	D5b	D6b	D7b
	FLch	D0b	D1b	D2b	D3b	D4b	D5b	D6b	D7b
	FRch	D8b	D9b	D10b	D11b	D12b	D13b	D14b	D15b
	Cch	D0c	D1c	D2c	D3c	D4c	D5c	D6c	D7c
	SWch	D8c	D9c	D10c	D11c	D12c	D13c	D14c	D15c
	SLch	D0d	D1d	D2d	D3d	D4d	D5d	D6d	D7d
	SRch	D8d	D9d	D10d	D11d	D12d	D13d	D14d	D15d
	SBLch	D0e	D1e	D2e	D3e	D4e	D5e	D6e	D7e
	SBRch	D8e	D9e	D10e	D11e	D12e	D13e	D14e	D15e
- 0.0 dB		0	0	0	0	0	0	0	0
- 0.5 dB		0	0	0	0	0	0	0	1
- 1.0 dB		0	0	0	0	0	0	1	0
- 1.5 dB		0	0	0	0	0	0	1	1
- 2.0 dB		0	0	0	0	0	1	0	0
- 2.5 dB		0	0	0	0	0	1	0	1
- 3.0 dB		0	0	0	0	0	1	1	0
- 3.5 dB		0	0	0	0	0	1	1	1
- 4.0 dB		0	0	0	0	1	0	0	0
- 4.5 dB		0	0	0	0	1	0	0	1
- 5.0 dB		0	0	0	0	1	0	1	0
- 5.5 dB		0	0	0	0	1	0	1	1
- 6.0 dB		0	0	0	0	1	1	0	0
•					•				
•					•				
- 50.0 dB		0	1	1	0	0	1	0	0
- 50.5 dB		0	1	1	0	0	1	0	1
- 51.0 dB		0	1	1	0	0	1	1	0
- 51.5 dB		0	1	1	0	0	1	1	1
- 52.0 dB		0	1	1	0	1	0	0	0
•					•				
•					•				
- 95.0 dB		1	0	1	1	1	1	1	0
- 95.5 dB		1	0	1	1	1	1	1	1
- 96.0 dB		1	1	0	0	0	0	0	0
- 96.5 dB		1	1	0	0	0	0	0	1
- 97.0 dB		1	1	0	0	0	0	1	0
- 97.5 dB		1	1	0	0	0	0	1	1
- 98.0 dB		1	1	0	0	0	1	0	0
- 98.5 dB		1	1	0	0	0	1	0	1
- 99.0 dB		1	1	0	0	0	1	1	0
- ∞ dB		1	1	1	1	1	1	1	1

It's initial setting when power is turned on.

Electrical Characteristics

Unless otherwise noted, Ta=25°C,AVCC=7V,AVEE=-7V,DVDD=3.3V,f=1kHz, Volume=0dB, Input Selector=IN1,Input ATT=0dB,Input Gain Control=0dB,Output Gain Control=0dB, L/R Volume Input=Bypass,Multi Input Selector=Multi IN1 setting

(1) Power supply characteristics

Parameter	Symbol	Test condition	Limits min	Limits typ	Limits max	Unit
Analog positive power circuit current	AIcc	With AVCC=7V and AVEE=-7V Pin22 pin current, when no signal is provided	—	50	70	mA
Analog negative power Circuit current	AIee	With AVCC=7V and AVEE=-7V Pin24 pin current, when no signal is provided	-70	-50	—	mA
Digital power circuit current	DIdd	With DVDD=3.3V, Pin21 pin current, when no signal is provided	—	3	6	mA

(2) Input/Output characteristics (OVER ALL)

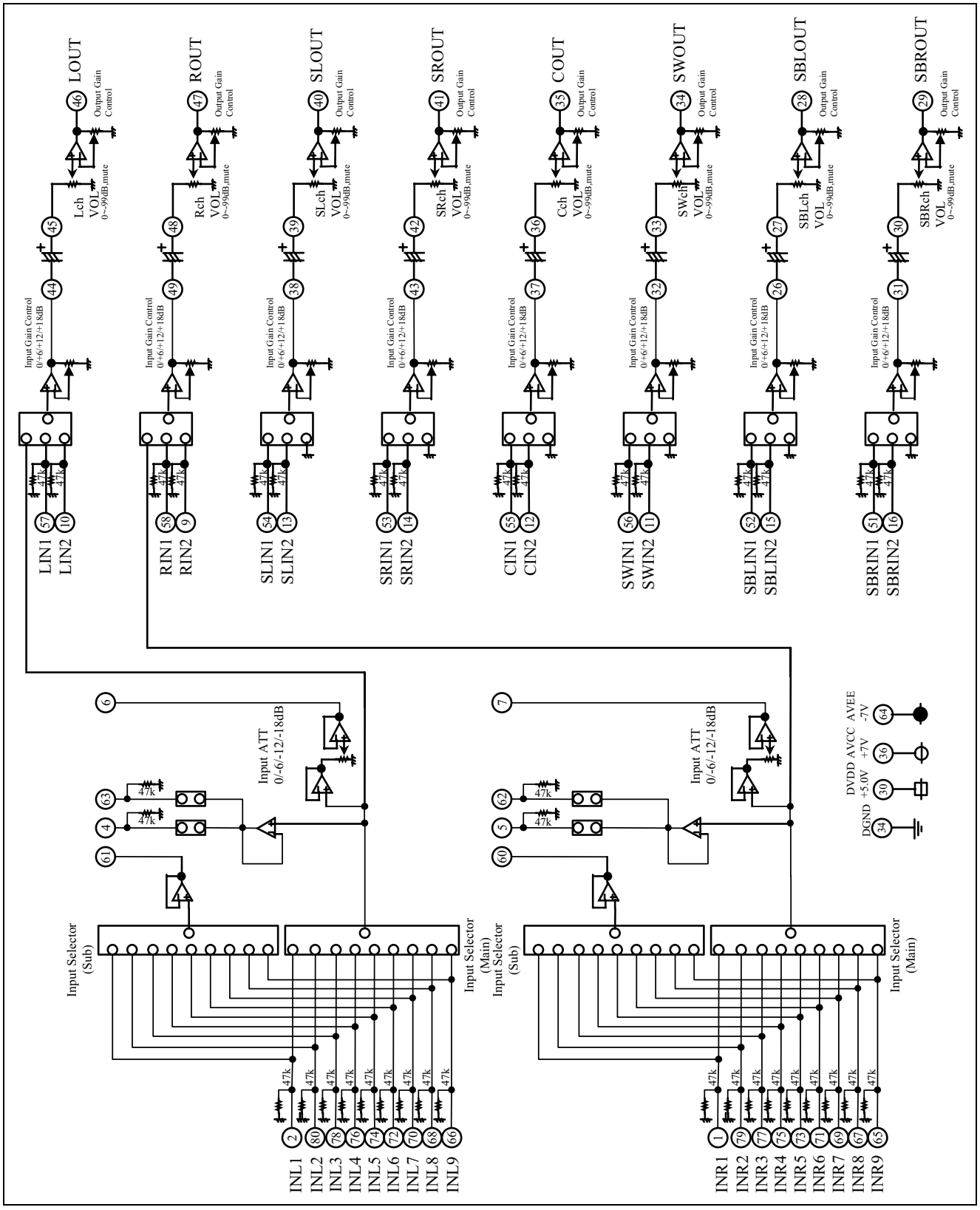
Parameter	Symbol	Test Condition		Limits min	Limits typ	Limits max	Unit
Input resistance	Rin	65-80pin when each selector chooses a terminal concerned		35	47	65	kΩ
Maximum output voltage	VOM	(1,2,51,5253,54,55,56) pin input, (47,46,29,28,41,40,35,34) pin output, THD=1%, RL=10kΩ Output Gain Control =+12dB setting		3.6	4.2	—	Vrms
Pass gain	Gv	(1,2,51,5253,54,55,56) pin input, (47,46,29,28,41,40,35,34) pin output, Vi=0.3Vrms,FLAT		-2.0	0	2.0	dB
Distortion	THD1	(1,2,51,5253,54,55,56) pin input, (47,46,29,28,41,40,35,34) pin output, BW:400Hz~30kHz f=1kHz , Vo=0.3Vrms , RL=10kΩ		—	0.005	0.05	%
	THD2	(1,2,51,5253,54,55,56) pin input, (47,46,29,28,41,40,35,34) pin output, BW:400Hz~30kHz f=1kHz , Vo=2Vrms , RL=10kΩ		—	0.03	0.1	%
Channels balance	CBAL	(1,2)pin input,(47,46)pin output, Vi=0.3Vrms , JIS-A		-0.5	0	0.5	dB
Output noise voltage	Vono (VOL =-∞dB)	JIS-A , (1,2,51,5253,54,55,56) pin: Rg=0Ω, (47,46,29,28,41,40,35,34) pin output, Volume=-∞dB setting	Output Gain Control=0dB	—	1.5	6	μVrms
			Output Gain Control=+12dB	—	9	20	μVrms
	Vono (VOL=0dB)	JIS-A , (1,2)pin : Rg=0Ω, (47,46)pin output, Volume=0dB setting	Output Gain Control=0dB	—	2.5	8	μVrms
			Output Gain Control=+12dB	—	12	25	μVrms
	Vonodac (dac out)	JIS-A , (1,2)pin:Rg=0Ω (5.4)pin output		—	3	9	μVrms

Parameter	Symbol	Test Condition	Limits min	typ	max	Unit
Input/Multi selector channel separation	CS1	<Input selector> (47,46)pin output, Vo=1Vrms , Rg=0Ω, RL=10kΩ, JIS-A	—	-90	-70	dB
	CS2	<Multi channel selector> (47,46,29,28,41,40,35,34) pin output, Vo=1Vrms , Rg=0Ω, RL=10kΩ, JIS-A, FL/FR VOL Input=Multi input	—	-90	-70	dB
Cross talk between channels	CT1 (L/R)	(1,2) pin input, (47,46) pin output, Vo=1Vrms , Rg=0Ω, RL=10kΩ, JIS-A	—	-90	-70	dB
	CT2 (Multi Input)	(51,52,10,53,54,55,56,57,58) pin input, (29,28,41,40,35,34,47,46) pin output, Vo=1Vrms , Rg=0Ω, RL=10kΩ, JIS-A, L/R VOL Input=Multi input	—	-90	-70	dB

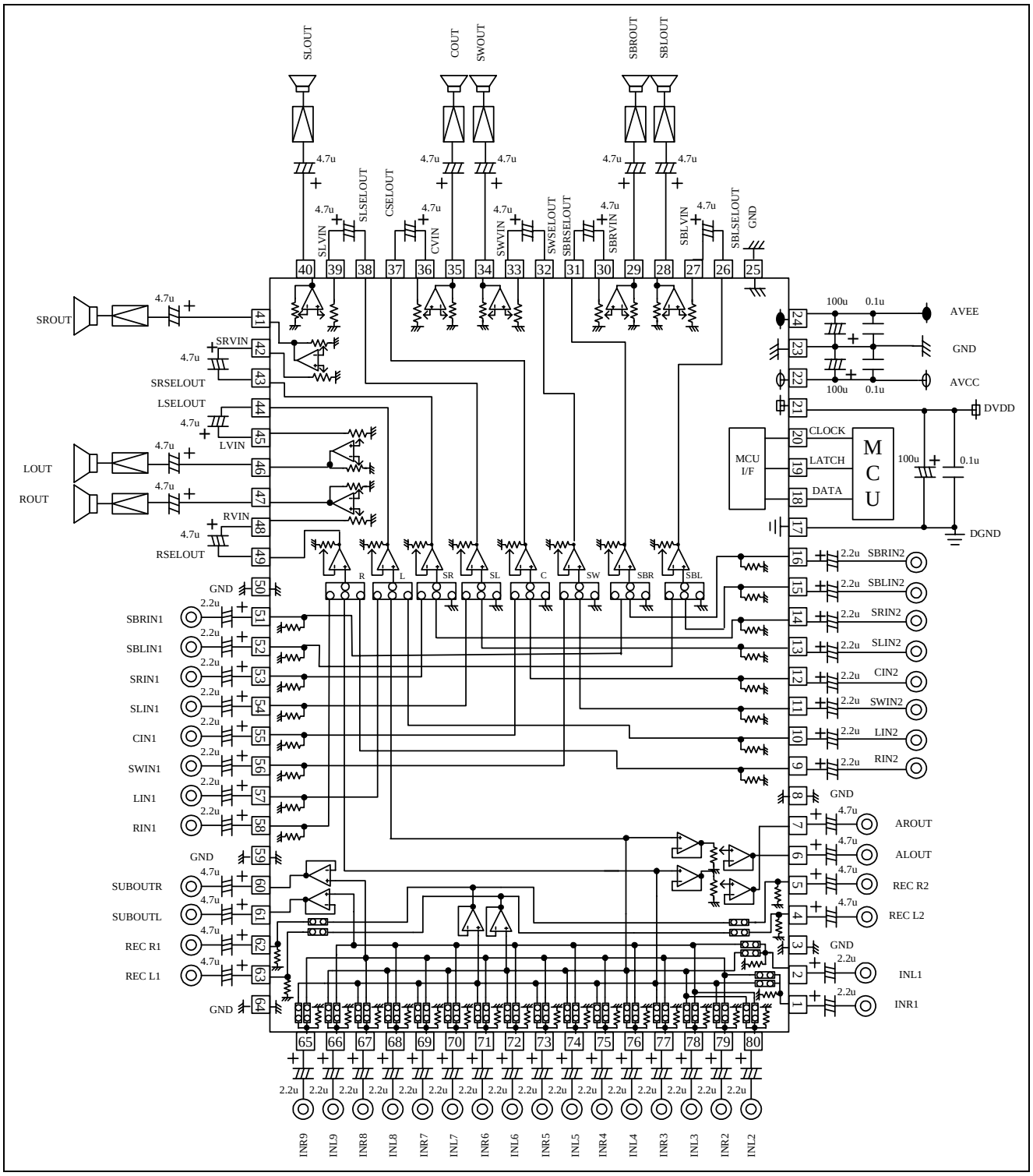
(3) 8 channel Volume characteristics

Parameter	Symbol	Test condition	Limits min	typ	max	Unit
Maximum attenuation	ATTmax	(47,46,29,28,41,40,35,34) pin output, Vi=2Vrms,JIS-A,VOL=-∞	—	-100	-95	dB
Volume gain Between channels	Dvol	(47,46,29,28,41,40,35,34) pin output, Volume=0dB setting	-0.5	0	+0.5	dB

Internal Block Diagram



Application Example



Package Dimensions

Plastic 80pin 14X20mm body QFP

80P6N-A (MMP)

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP80-P-1420-0.80	—	1.58	Alloy 42

Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	3.05
A_1	0	0.1	0.2
A_2	—	2.8	—
b	0.3	0.35	0.45
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e	—	0.8	—
H_D	16.5	16.8	17.1
H_E	22.5	22.8	23.1
L	0.4	0.6	0.8
L_1	—	1.4	—
x	—	—	0.2
y	—	—	0.1
θ	0°	—	10°
b_2	—	0.5	—
l_2	1.3	—	—
M_D	—	14.6	—
M_E	—	20.6	—

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