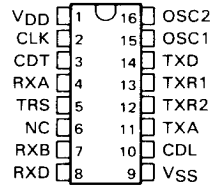
D2866, AUGUST 1985—REVISED FEBRUARY 1986

NOT RECOMMENDED FOR NEW DESIGN

For new design, refer to TCM3105

J
DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TCM3101 is a single-chip asynchronous Frequency Shift Keying (FSK) modem that uses silicon gate CMOS technology to implement a switched capacitor architecture. It is pin selectable (TXR1, TXR2, and TRS inputs) for a wide range of transmit/receive baud rates and is compatible with the applicable Bell 202 or CCITT V23 specifications. Operation is fully reversible, thereby allowing both forward and backward channels to be used simultaneously.

The transmitter is a programmable frequency synthesizer that provides two output frequencies (on TXA), representing the 'marks' and 'spaces' of the digital signal present on the TXD input.

The receive section is responsible for the demodulation of the analog signal appearing at the RXA input and is based on the principle of frequency to voltage conversion. This section contains a group delay equalizer (to correct phase distortion), automatic gain control, carrier detect level adjustment, and bias distortion adjustment, thereby optimizing performance and giving the lowest possible bit error rate.

Carrier-detect information is given to the system by means of the carrier-detect circuits, which set a flag on the CDT output if the level of received in-band energy falls below a value set on the CDL input for a specified minimum duration.

Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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PIN NO.	PIN NAME	DESCRIPTION
1	V_{DD}	Positive supply voltage
2	CLK	Output for a continuous clock signal output at 19.11 kHz (9.56 kHz for CCITT V23 600 baud)
3	CDT	Carrier Detect Output, a low-level output that indicates carrier failure
4	RXA	Receive Analog Input to which the received line signal must be ac coupled
5	TRS	Transmit/Receive Standard Select Input, which, with TXR1 and TXR2, sets the standard bit rates and mark/space frequencies
6	NC	No internal connection
7	RXB	Receive Bias Adjust for external adjustment of the decision threshold of the final comparator to minimize bias distortion
8	RXD	Receiver Digital Output for the demodulated received data in positive logic. The high logic level is a mark and the low logic level is a space.
9	V_{SS}	Supply voltage (normally ground), connected to substrate
10	CDL	Carrier Detect Level Adjust for external adjustment of carrier detect threshold
11	TXA	Transmit Analog Output for the modulated signal, which must be ac coupled
12	TXR2	Bit Rate Select 2 input, which, along with TXR1 and TRS, sets the bit rates and mark/space frequencies
13	TXR1	Bit Rate Select 1 input, which, along with TXR2 and TRS, sets the bit rates and mark/space frequencies
14	TXD	Transmit Digital Input for input data to the transmitter in positive logic. The high logic level is a mark and the low logic level is a space. The data can be accepted at any speed from zero to the selected speed and may be totally asynchronous.
15	OSC1	Oscillator connections. The crystal (typically 4.4336 MHz) is connected to these pins. If an external clock is used, OSC1 is left open and the clock is connected to OSC2.
16	OSC2	

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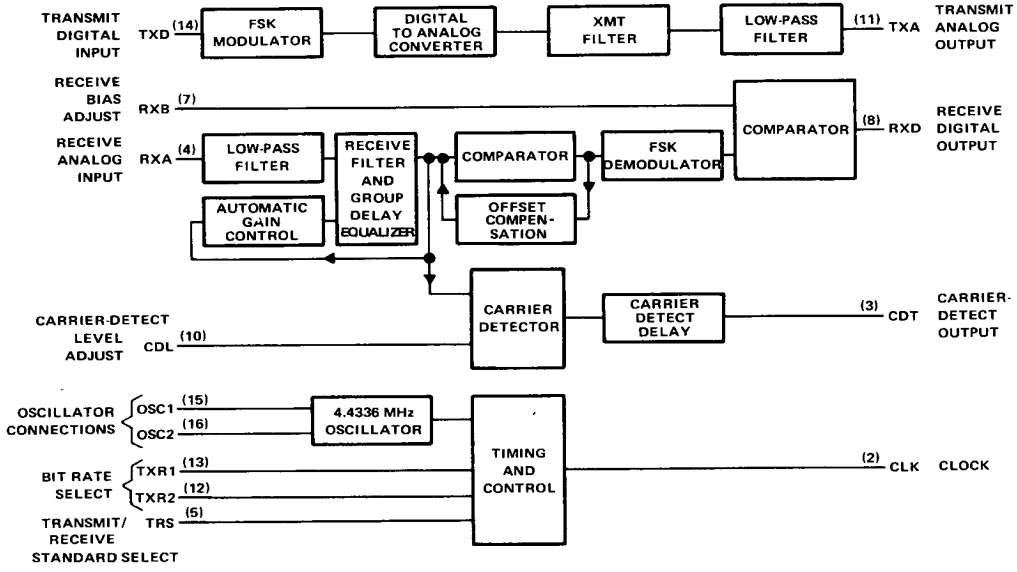
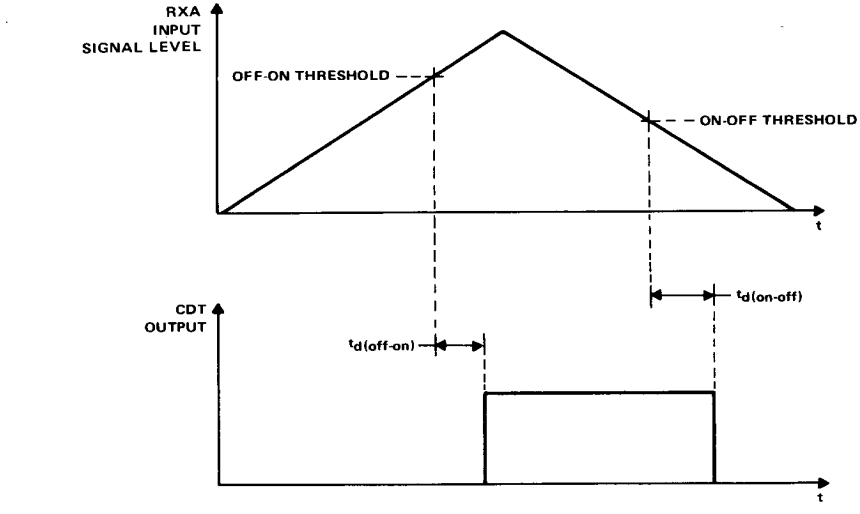
functional block diagram



timing diagram



absolute maximum ratings over free-air operating temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . −0.3 V to 10 V
Input voltage, V_I (any input) . . . . . −0.3 to V_{DD}
Operating free-air temperature range . . . . . −10°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Clock frequency, f_{clock}	4.4334	4.4336	4.4338	MHz
Supply voltage, V_{DD}	4	5	5.5	V
High-level input voltage, V_{IH}	2		V_{DD}	V
Low-level input voltage, V_{IL}	0		0.8	V
Analog input level, peak-to-peak (ac coupled)		0.3	0.78	V
Analog load impedance at TXA	50			kΩ
Operating free-air temperature range, T_A	−10		70	°C

2 Telecommunications Circuits

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-Level output voltage	RXD, CDT, CLK	I_{OH} = −100 μA, V_{DD} = 5 V		2.4		V_{DD}	V
V_{OL}	Low-level output voltage	RXD, CDT, CLK	I_{OL} = 1.6 mA, V_{DD} = 5 V		V_{SS}		0.4	V
	Analog output voltage level, peak-to-peak		V_{DD} = 4 V	R_L = 50 kΩ, C_L = 100 pF		1.3		V
			V_{DD} = 5 V		1.4	1.6	2	
			V_{DD} = 5.5 V			1.75		
	Adjust voltage	RXB	V_{DD} = 5 V		2.5	2.7	3	V
		CDL			2	3.2	4	
	Analog output dc offset					$V_{DD}/2$		V
	Digital input current		V_I = 0 to V_{DD}				±1	μA
	Analog input current						±15	μA
	Bias input current	RXB, CDL				100	150	μA
I_{DD}	Supply current		V_{DD} = 4 V			2	4	mA
			V_{DD} = 5 V			4	6	
			V_{DD} = 5.5 V			6	8	
C_i	Input capacitance, all inputs		f = 1 MHz			10		pF
C_o	Output capacitance, all outputs		f = 1 MHz			10		pF
	Phase jitter						200	μs
	Bias distortion†						15%	
	Carrier detect threshold, off-on‡				−45.5		−43	dBm
	Carrier detect threshold, on-off‡				−48		−45.5	dBm
	Carrier detect hysteresis				2.5	2.8		dBm
$t_{d(off-on)}$	Carrier detect delay time		RX = 600 or 1200 bps		12		25	ms
$t_{d(on-off)}$	Carrier detect delay time				12		20	ms

†Bias distortion is the departure from a 50% duty cycle when a series of alternating mark and space tones are received.
‡This is the threshold with the CDL input properly adjusted.

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PRINCIPLES OF OPERATION

The TCM3101 FSK modem is made up of four functional circuits. The circuits are the transmitter, the receiver, a carrier detector, and control and timing (See Figure 1).

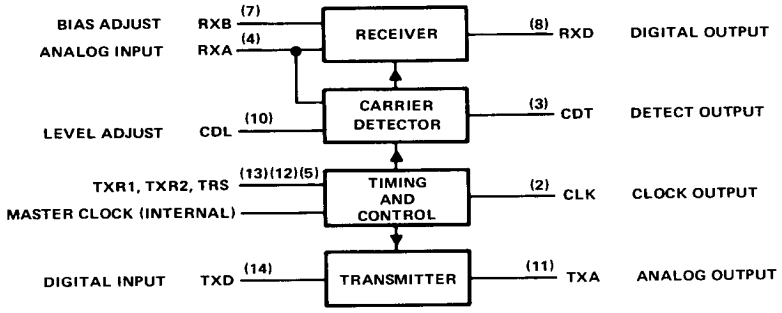

FIGURE 1. TCM3101 SYSTEM PARTITIONING

transmitter

The transmitter comprises a phase coherent FSK modulator, a transmit filter, and a transmit amplifier. The modulator is a programmable frequency synthesizer that derives the output frequencies by variable division of the oscillator frequency (4.4336 MHz). The division ratio is set by the states of the Transmit/Receive Standard input (TRS), the Bit Rate Select inputs (TXR1 and TXR2), and the Digital Data input (TXD).

The transmit frequency assignments are given in Table 1. The data convention is that a high logic level equals a mark and a low logic level equals a space.

TABLE 1. TRANSMIT FREQUENCY ASSIGNMENTS

TRS	STANDARD	TXR1	TXR2	TRANSMITTER BIT RATE	TXD	TX FREQUENCY (Hz)	
L or H	CCITT V23	H	L	75	H	M	390
					L	S	450
		L	H	600	H	M	1300
					L	S	1700
		L	L	1200	H	M	1300
					L	S	2100
CLK	BELL 202	H	L	150	H	M	387
					L	S	487
		L	X	1200	H	M	1200
					L	S	2200
X		H	H	0	X	TRANSMITTER DISABLED	

A switched-capacitor low-pass filter limits the harmonics and noise outside the transmit band and the characteristics of this filter are set by the frequency select inputs as previously described. The harmonics introduced by the transmit filter clock are removed by a continuous low-pass filter.

The transmitter output level varies with power supply voltage and so must be compensated in the 2-wire to 4-wire converter to give a constant output level to the line.

receiver

A continuous low-pass anti-aliasing filter is followed by the receive amplifier, which automatically controls the gain to give a constant output level from the receive filter. The receive filter limits the bandwidth of the signal presented to the demodulator, reducing out-of-band interference, and has very high rejection of 75- and 150-baud backward channel frequencies. These are typically present at much higher levels than the received signal. The receiver bit rate assignments are given in Table 2.

TABLE 2. RECEIVER BIT RATE ASSIGNMENTS

TRS	STANDARD	RECEIVE BIT RATE	CLK FREQUENCY (kHz)
H	CCITT V23	600	9.56
L	CCITT V23	1200	19.11
CLK	BELL 202		

The group delay equalizer is a switched-capacitor network that compensates the delay introduced by the receive filter and the network. The output from the equalizer is then limited to give an FSK modulated squarewave that is presented to the demodulator.

The demodulator is an edge-triggered multivibrator that triggers off positive- and negative-going edges. The output of the demodulator is, therefore, a stream of constant-length pulses at a frequency that is double the frequency of the limited input signal. The dc component of this signal is proportional to the received frequency and is extracted by a switched-capacitor, low-pass, post-demodulator filter.

The variation of dc level with received frequency is presented to a comparator that slices at a level externally fixed by the RXB bias adjustment pin. This voltage depends on received bit rate and internal offsets. The comparator output is then the received data at the RXD output.

carrier detect

The carrier detect circuits comprise an energy detector and digital delay. The energy detector compares the total signal level at the output of the receive filter to an externally set threshold level on the CDL input. The comparator has a 2.5-dB hysteresis and a delay to allow for momentary signal loss and to prevent oscillation. The output of the detector is available on the CDT pin where a high level indicates that a carrier is present.

control and timing

An on-chip oscillator runs from an external 4.4336-MHz crystal connected between the OSC1 and OSC2 pins or an external signal driving OSC1. A clock signal equal to 16 times the selected receive bit rate is available on the CLK output.

The single-supply rail means that all analog functions are referenced to an internally generated reference. All analog inputs and output must be ac coupled.

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TYPICAL APPLICATION INFORMATION

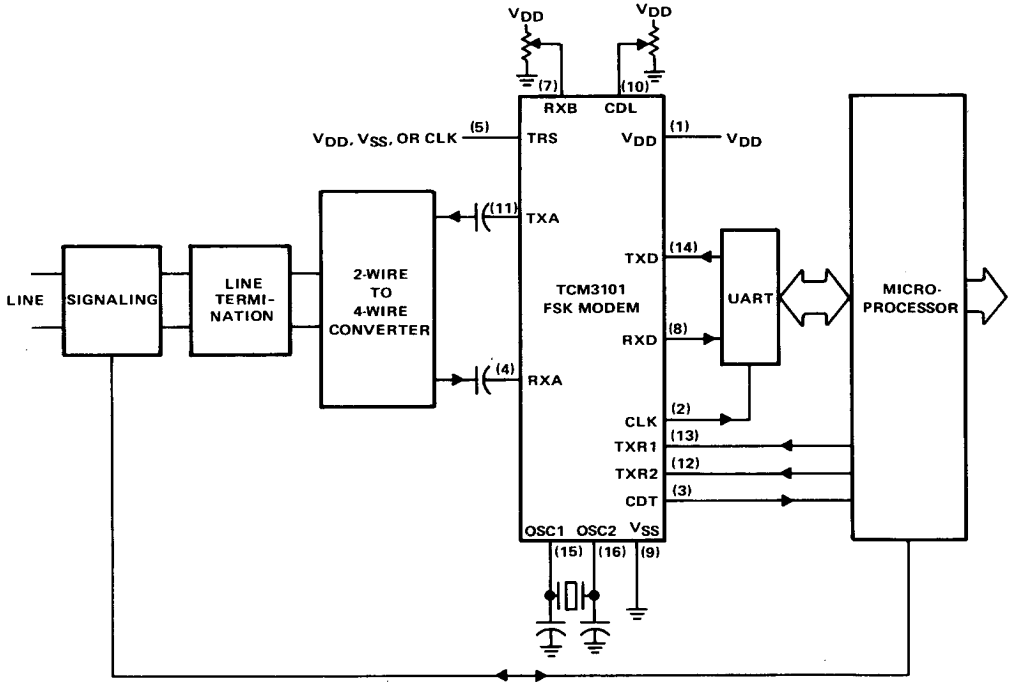

FIGURE 2. TYPICAL SYSTEM CONFIGURATION

TYPICAL APPLICATION INFORMATION

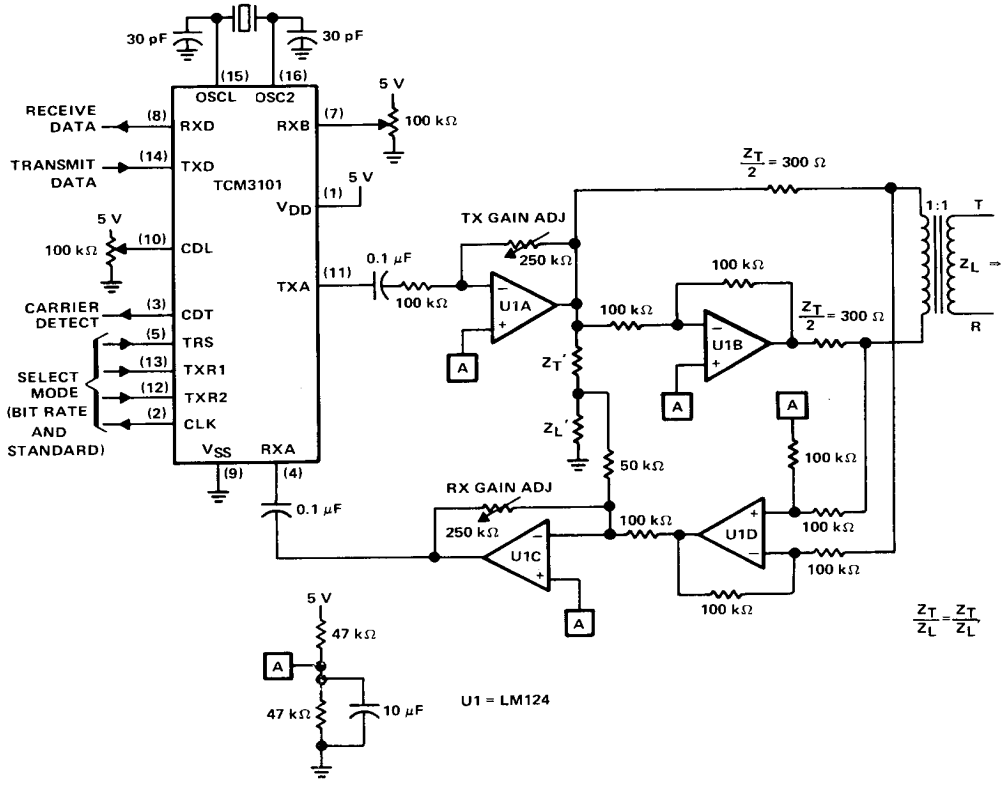

FIGURE 3. TELEPHONE LINE INTERFACE CIRCUIT

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TYPICAL APPLICATION INFORMATION

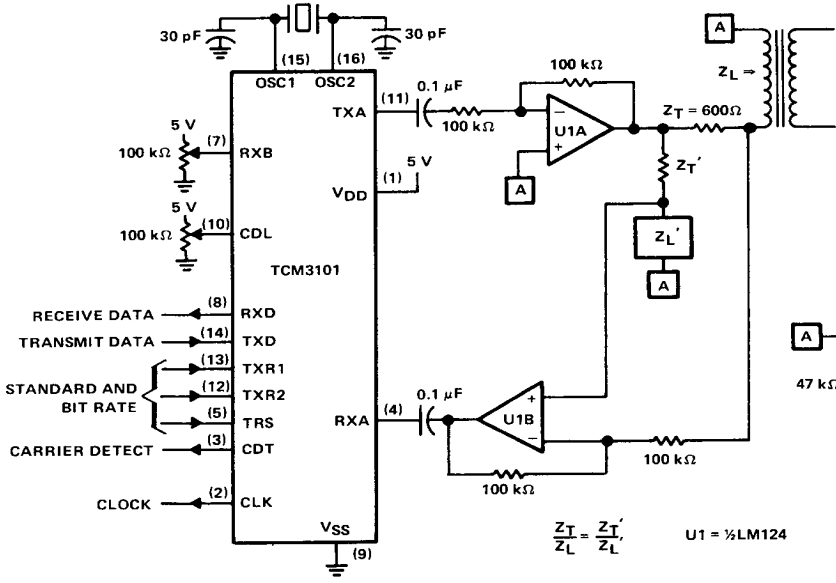

FIGURE 4. SIMPLIFIED TELEPHONE LINE INTERFACE CIRCUIT