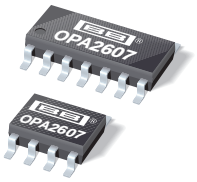
BURR - BROWN®



OPA2607

For most current data sheet and other product information, visit www.burr-brown.com

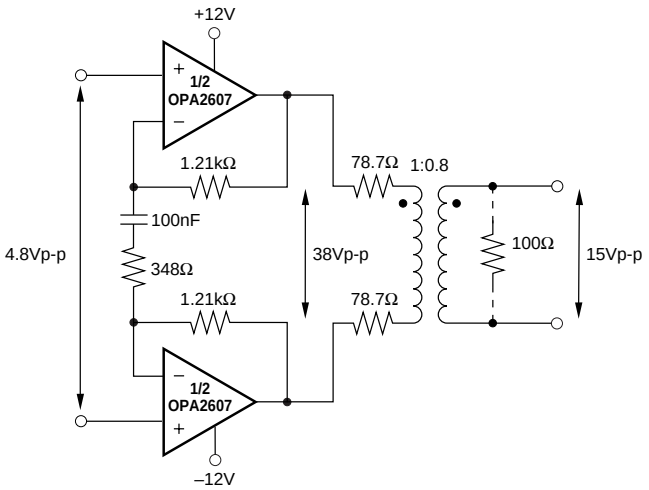
SpeedPLUS™ Dual, High Output, Current-Feedback OPERATIONAL AMPLIFIER

FEATURES

- WIDEBAND ±12V OPERATION: 25MHz (G = +8)
- UNITY GAIN STABLE: 35MHz (G = +1)
- HIGH OUTPUT CURRENT: 250mA
- OUTPUT VOLTAGE SWING: ±10.5V (V_S = ±12V)
- HIGH SLEW RATE: 600V/µs
- LOW SUPPLY CURRENT: 8mA/channel
- FLEXIBLE POWER CONTROL (SO-14)
- ±6V TO ±16V SUPPLY RANGE
- SO-COOL™ POWER PACKAGING

APPLICATIONS

- xDSL LINE DRIVER
- LOW-NOISE ADSL RECEIVER
- LOW-COST VIDEO DA
- LOW-COST UPGRADE TO LT1207/AD812



Low Turns Ratio ADSL Upstream Driver

DESCRIPTION

The OPA2607 provides a high output voltage swing and low distortion required for low turns ratio ADSL upstream driver applications. Operating on a ±12V supply, the OPA2607 consumes a low 8.0mA/channel quiescent current to deliver a very high 250mA peak output current. Guaranteed output current of 180mA supports even the most demanding ADSL CPE requirements with low harmonic distortion. Differential driver applications will deliver < –75dBc distortion at the peak upstream power levels of full rate ADSL. Using a differential driver design, as shown below, the OPA2607 can deliver a high 38Vp-p voltage swing into a 1:0.8 step-down transformer to meet the ADSL CPE upstream power requirements. This low turns ratio actually provides a step up to the much weaker downstream signal arriving on the line side of this transformer, extending the DSL modem's reach.

Power control features are included in the SO-14 package version to allow system power to be minimized. Two logic control lines allow four quiescent power settings. These include full power, power cutback for short loops, idle state for no signal transmission but line match maintenance, and shutdown for power off with a high impedance output. An additional I_{ADJ} pin allows the maximum supply current to be adjusted ±25% from the nominal value. Connecting this pin to $+V_{CC}$ will increase the full power quiescent to 20mA, increasing the peak output current available, while connecting this pin to $–V_{CC}$ will decrease the full power quiescent to 12mA where a lower peak output current is required. The digital control lines continue to scale the total quiescent current from these new maximum levels in the same proportional steps as before.

The OPA2607 is available in three package styles. For power driver applications, a thermally enhanced SO-COOL™ package with a heat slug is available in both SO-8 and SO-14 pinouts. For lower power receiver applications, a standard SO-8 package is available.

OPA2607 RELATED PRODUCTS

SINGLES	DUALS	TRIPLES	NOTES
OPA681	OPA2681	OPA3681	Single +12V Capable
—	OPA2677	—	Single +12V Capable

International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111
Twx: 910-952-1111 • Internet: http://www.burr-brown.com/ • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS: $V_S = \pm 12V$

$R_F = 1.21k\Omega$, $R_L = 100\Omega$, and G = +8, unless otherwise noted.

PARAMETER	CONDITIONS	OPA2607H, U, N TYP +25°C	GUARANTEED +25°C[2]	GUARANTEED 0°C to 70°C[3]	GUARANTEED –40°C to +85°C[3]	UNITS	MIN/ MAX	TEST LEVEL[1]
AC PERFORMANCE (see Figure 1)								
Small-Signal Bandwidth (V_O = 0.5Vp-p)	G = +1, R_F = 1.50kΩ	35				MHz	typ	C
	G = +2, R_F = 1.43kΩ	28				MHz	typ	C
	G = +4, R_F = 1.37kΩ	25				MHz	typ	C
	G = +8, R_F = 1.21kΩ	25	19	18	17	MHz	min	B
Bandwidth for 0.1dB Gain Flatness	G = +8, V_O = 0.5Vp-p	6				MHz	typ	C
Large-Signal Bandwidth	G = +8, V_O = 20Vp-p	13	10.6	9.0	7.9	MHz	min	B
Slew Rate	G = +8, V_O = 20V Step	600	470	400	350	V/µs	min	B
Rise/Fall Time	G = +8, V_O = 0.5V Step	14	18	20	21	ns	min	B
Spurious Free Dynamic Range[4]	V_O = 2Vp-p, 1MHz, R_L = 100Ω	77	66	60	57	dB	min	B
	V_O = 20Vp-p, 150kHz, R_L = 150Ω	75	70	58	57	dB	min	B
Input Voltage Noise		1.7	2.0	2.6	2.7	nV/√Hz	max	B
Non-Inverting Input Current Noise		11	13	13	13	pA/√Hz	max	B
Inverting Input Current Noise		15	17	17	17	pA/√Hz	max	B
Differential Gain	NTSC, G = +2, R_L = 150Ω	0.01				%	typ	C
Differential Phase	NTSC, G = +2, R_L = 150Ω	0.01				degrees	typ	C
Channel-to-Channel Crosstalk	f = 1MHz	–60				dB	typ	C
DC PERFORMANCE[5]								
Open-Loop Transimpedance Gain	V_O = 0V, R_L = 100Ω	950	440	390	310	kΩ	min	A
Input Offset Voltage	V_{CM} = 0V	±1.5	±7	±8	±8.5	mV	max	A
Average Offset Voltage Drift	V_{CM} = 0V			–20	–25	µV/°C	max	B
Non-Inverting Input Bias Current	V_{CM} = 0V	±3	±12	±15	±20	µA	max	A
Average Non-Inverting Input Bias Current Drift	V_{CM} = 0V			–70	–100	nA/°C	max	B
Inverting Input Bias Current	V_{CM} = 0V	±4	±40	±58	±70	µA	max	A
Average Inverting Input Bias Current Drift	V_{CM} = 0V			–380	–425	nA/°C	max	B
INPUT								
Common-Mode Input Range (CMIR)		±10.3	±10.0	±9.9	±9.8	V	min	A
Common-Mode Rejection Ratio (CMRR)	V_{CM} = 0V	64	53	52	51	dB	min	A
Non-Inverting Input Impedance		250 || 4				kΩ || pF	typ	C
Inverting Input Resistance	Open-Loop	33				Ω	typ	C
OUTPUT								
Voltage Output Swing	No Load, Hard Limit	±11.2	±10.9	±10.8	±10.7	V	min	A
	R_L = 100Ω, Hard Limit	±10.5	±9.9	±9.8	±9.7	V	min	A
	R_L = 150Ω, SFDR > 67dB, 150kHz	±10.2				V	typ	C
Current Output, Sourcing	V_O = 0	310	210	175	140	mA	min	A
Current Output, Sinking	V_O = 0	250	180	150	110	mA	min	A
Closed-Loop Output Impedance	G = +8, f ≤ 10kHz	0.02				Ω	typ	C
Power Control (SO-14 only)	**DIG_REF = Gnd**							
Maximum Logic 0	A0, A1	0.8				V	max	C
Minimum Logic 1	A0, A1	2				V	min	C
Logic Input Current	0V to 4.5V	60				µA	max	C
Supply Current at Full Power	A0 = 1, A1 = 1, I_{ADJ} = open	16				mA	typ	C
Supply Current at Power Cutback	A0 = 0, A1 = 1, I_{ADJ} = open	13				mA	typ	C
Supply Current at Idle Power	A0 = 1, A1 = 0, I_{ADJ} = open	3.8				mA	typ	C
Supply Current at Shutdown	A0 = 0, A1 = 0, I_{ADJ} = open	1.3				mA	typ	C
Output Impedance in Idle Power	Closed-Loop, f < 1MHz	0.7				Ω	typ	C
Output Impedance in Shutdown		350 || 17				kΩ || pF	typ	C
Shutdown Isolation	G = +8, 1MHz	75				dB	typ	C
Maximum Adjusted Quiescent Current	A0 = 1, A1 = 1, I_{ADJ} at $+V_S$	20				mA	typ	C
Minimum Adjusted Quiescent Current	A0 = 1, A1 = 1, I_{ADJ} at $-V_S$	12				mA	typ	C
POWER SUPPLY								
Minimum Operating Voltage			±6	±6	±6	V	min	B
Specified Operating Voltage		±12				V	typ	C
Maximum Operating Voltage			±16	±16	±16	V	max	A
Maximum Quiescent Current	Total Both Channels, Full Power	16	16.8	17	17.5	mA	max	A
Minimum Quiescent Current	Total Both Channels, Full Power	16	15.2	13.8	13.3	mA	min	A
Power Supply Rejection Ratio (PSRR)	f ≤ 10kHz	68	61	59	57	dB	min	A
TEMPERATURE RANGE								
Specification: H, U, N		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}	Junction-to-Ambient							
H PSO-8 Power Package[6]		50				°C/W	typ	C
U SO-8		125				°C/W	typ	C
N PSO-14 Power Package[6]		45				°C/W	typ	C

NOTES: (1) Test Levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (2) Junction temperature = ambient for 25°C guaranteed specifications. (3) Junction temperature = ambient at low temperature limit: junction temperature = ambient +40°C at high temperature limit for over temperature guaranteed specifications. (4) Single amplifier SFDR limited by 2nd Harmonic. Differential SFDR will be limited by 3rd Harmonic and will be > 15dB higher. (5) Current is considered positive out of node. V_{CM} is the input common-mode voltage. (6) Slug in power package connected to $-V_S$ plane at least 2" x 2" (50mm x 50mm) in size. See the Board Layout Guidelines Section.

ABSOLUTE MAXIMUM RATINGS

Power Supply	±16.5V_{DC}
Internal Power Dissipation[1]	See Thermal Information
Differential Input Voltage	±5V
Input Voltage Range	±V_S
Storage Temperature Range: U, N	–40°C to +125°C
Lead Temperature (soldering, 10s)	+260°C
Junction Temperature (T_J)	+175°C
ESD Rating (Human Body Model)	4000V
(Machine Model)	300V

NOTE: (1) Packages must be derated based on specified θ_{JA}. Maximum T_J must be observed.

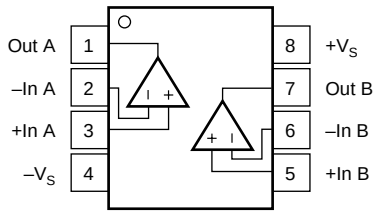
ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

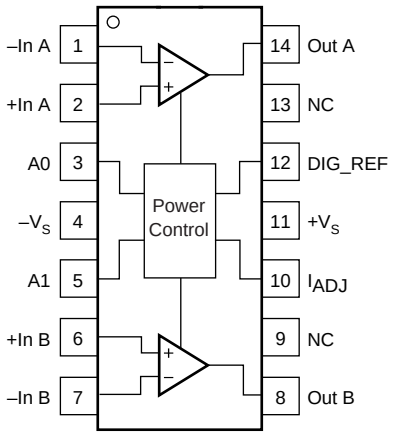
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PIN CONFIGURATIONS

Top View



SO-8, PSO-8



PSO-14

NC = No Connection

PACKAGE/ORDERING INFORMATION

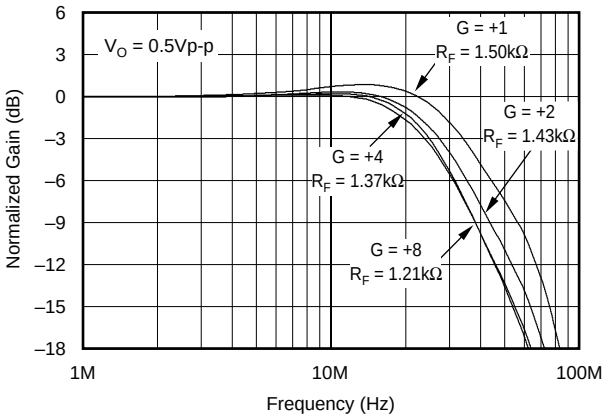
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER[1]	TRANSPORT MEDIA
OPA2607H	PSO-8	182-1	–40°C to +85°C	OPA2607H	OPA2607H	Rails
"	"	"	"	"	OPA2607H/2K5	Tape and Reel
OPA2607U	SO-8	182	"	OPA2607U	OPA2607U	Rails
"	"	"	"	"	OPA2607U/2K5	Tape and Reel
OPA2607N	PSO-14	235-1	"	OPA2607N	Contact Factory	Rails
"	"	"	"	"	Contact Factory	Tape and Reel

NOTE: (1) Models with a slash (/) are available only as Tape and Reel in the quantity indicated after the slash (e.g. /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of the OPA2607U/2K5 will get a single 2500-piece Tape and Reel.

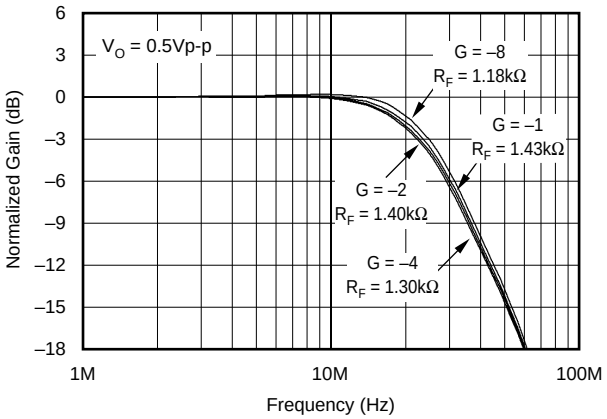
TYPICAL PERFORMANCE CURVES: $V_S = \pm 12V$

At T_A = +25°C, G = +8, R_F = 1.21kΩ, and R_L = 100Ω, unless otherwise noted. See Figure 1 for AC performance only.

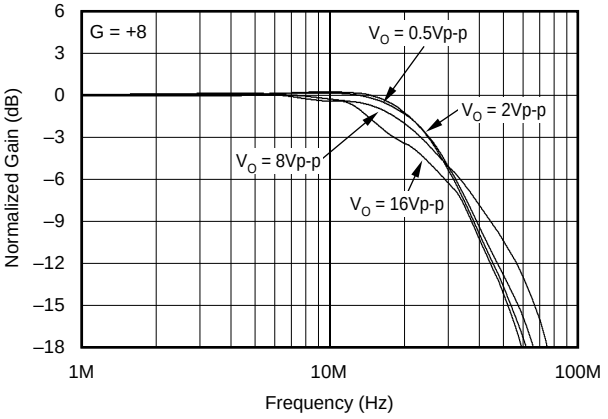
NON-INVERTING SMALL-SIGNAL FREQUENCY RESPONSE



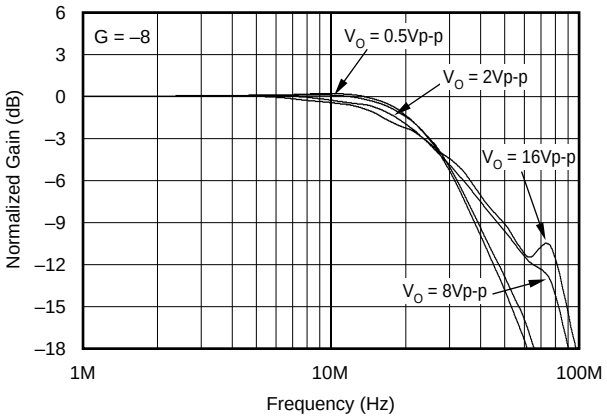
INVERTING SMALL-SIGNAL FREQUENCY RESPONSE



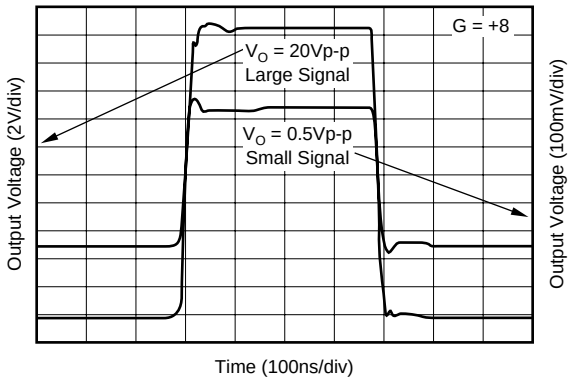
NON-INVERTING LARGE-SIGNAL FREQUENCY RESPONSE



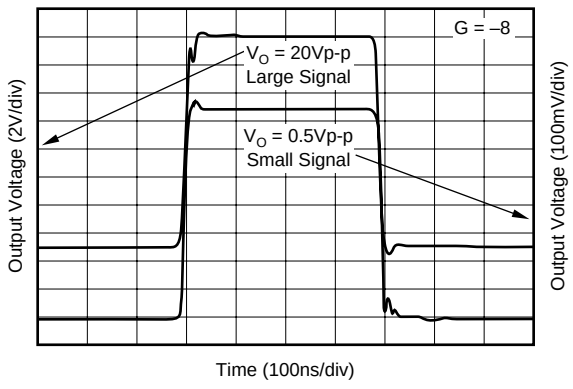
INVERTING LARGE-SIGNAL FREQUENCY RESPONSE



NON-INVERTING PULSE RESPONSE



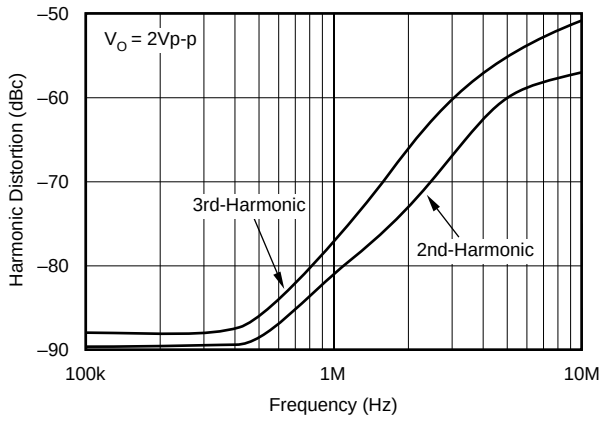
INVERTING PULSE RESPONSE



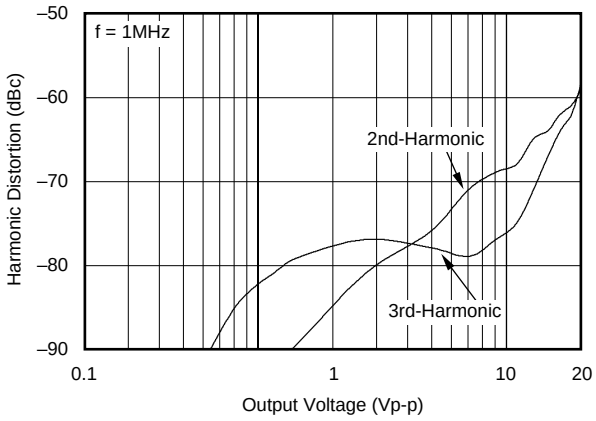
TYPICAL PERFORMANCE CURVES: $V_S = \pm 12V$ (Cont.)

At T_A = +25°C, G = +8, R_F = 1.21kΩ, and R_L = 100Ω, unless otherwise noted. See Figure 1 for AC performance only.

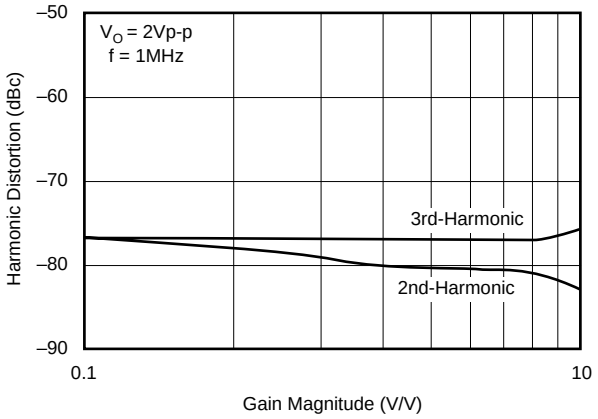
HARMONIC DISTORTION vs FREQUENCY



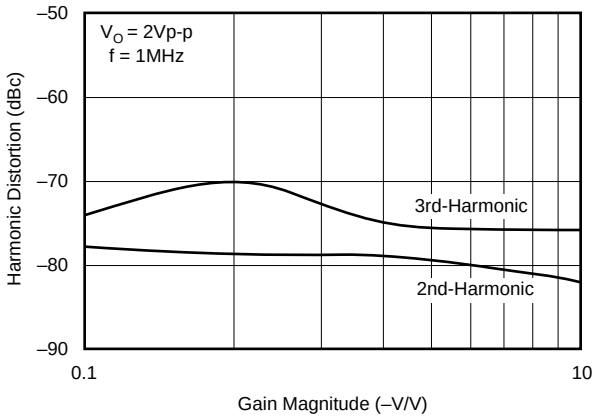
HARMONIC DISTORTION vs OUTPUT VOLTAGE



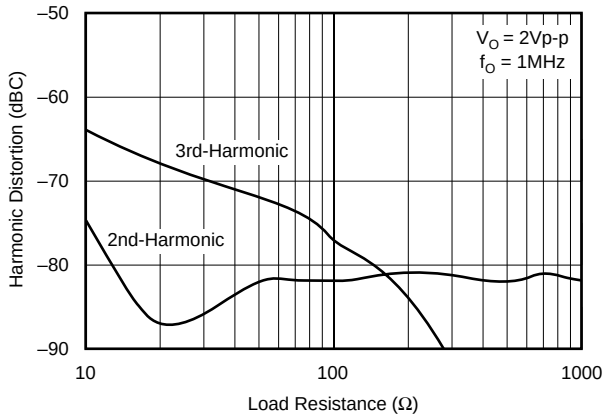
HARMONIC DISTORTION vs NON-INVERTING GAIN



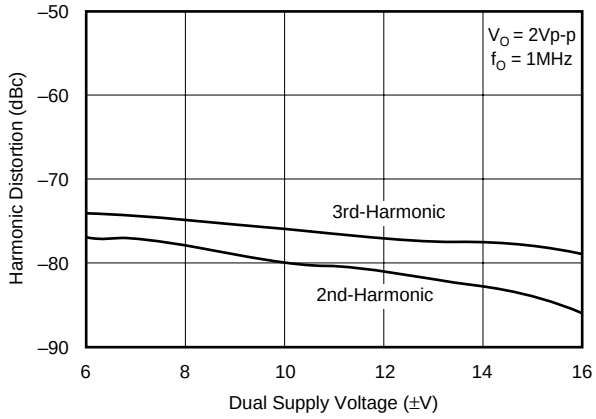
HARMONIC DISTORTION vs INVERTING GAIN



HARMONIC DISTORTION vs LOAD RESISTANCE

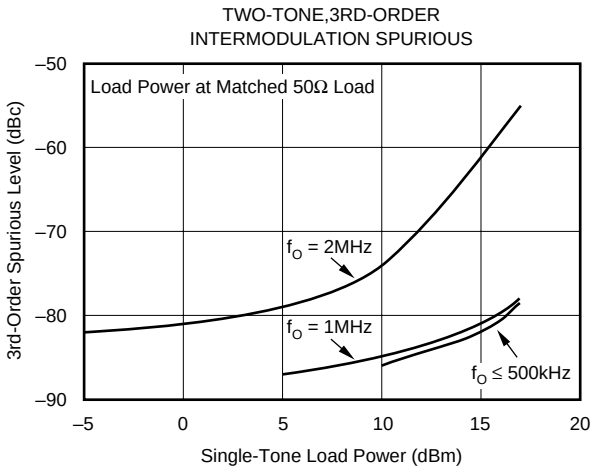


HARMONIC DISTORTION vs DUAL SUPPLY VOLTAGE



TYPICAL PERFORMANCE CURVES: $V_S = \pm 12V$ (Cont.)

At T_A = +25°C, G = +8, R_F = 1.21kΩ, and R_L = 100Ω, unless otherwise noted. See Figure 1 for AC performance only.



APPLICATIONS INFORMATION

WIDEBAND CURRENT FEEDBACK OPERATION

The OPA2607 gives the exceptional AC performance of a wideband current feedback op amp with a highly linear, high power output stage. Requiring only 8.0mA/chan quiescent current, the OPA2607 will swing to within 2V of either supply rail and deliver in excess of 180mA guaranteed at room temperature. This low output headroom requirement, along with supply-voltage independent biasing, gives remarkable single (+15V) supply operation. Previous boosted output stage amplifiers have typically suffered from very poor crossover distortion as the output current goes through zero. The OPA2607 achieves a comparable power gain with much better linearity. The primary advantage of a current-feedback op amp over a voltage-feedback op amp is that AC performance (bandwidth and distortion) is relatively independent of signal gain.

Figure 1 shows the DC-coupled, gain of +8, dual power-supply circuit configuration used as the basis of the ±12V Specifications and Typical Performance Curves. For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output impedance is set to 50Ω with a series output resistor. Voltage swings reported in the specifications are taken directly at the input and output pins while load powers (dBm) are defined at a matched 50Ω load. For the circuit of Figure 1, the total effective load will be 100Ω || 1379Ω = 93Ω.

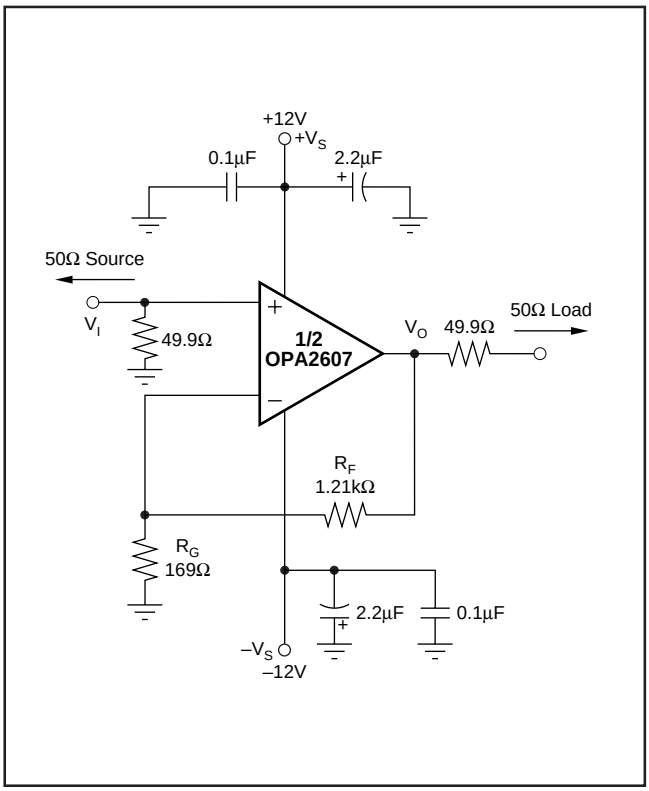


FIGURE 1. DC-Coupled, G = +8, Bipolar Supply, Specification and Test Circuit.

DESIGN-IN TOOLS

DEMONSTRATION BOARDS

Several PC boards are available to assist in the initial evaluation of circuit performance using the OPA2607 in its 3 package styles. All are available free as an unpopulated PC board delivered with descriptive documentation. The summary information for these boards is shown in Table I.

PRODUCT	PACKAGE	DEMO BOARD NUMBER	ORDERING NUMBER
OPA2607U	SO-8	DEM-OPA268xU	MKT-352
OPA2607N	SO-14 SO-Cool	DEM-OPA2607N	MKT-367
OPA2607H	SO-8 SO-Cool	DEM-OPA2607H	MKT-366

TABLE I.

Contact the Burr-Brown applications support line to request any of these boards.

MACROMODELS AND APPLICATIONS SUPPORT

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models for some op amps are available through the Burr-Brown web site (http://www.burr-brown.com). These models do a good job of predicting small-signal AC and transient performance under a wide variety of operating conditions. They do not do as well in predicting the harmonic distortion, dG/dP, or temperature characteristics. These models do not attempt to distinguish between the package types in their small-signal AC performance, nor do they attempt to simulate channel-to-channel coupling.

OPERATING SUGGESTIONS

SETTING RESISTOR VALUES TO OPTIMIZE BANDWIDTH

A current-feedback op amp like the OPA2607 can hold an almost constant bandwidth over signal gain settings with the proper adjustment of the external resistor values. This is shown in the Typical Performance Curves; the small-signal bandwidth decreases only slightly with increasing gain. Those curves also show that the feedback resistor has been changed for each gain setting. The resistor "values" on the inverting side of the circuit for a current-feedback op amp can be treated as frequency- response compensation elements while their "ratios" set the signal gain. Figure 2 shows the small-signal frequency-response analysis circuit for the OPA2607.

The key elements of this current feedback op amp model are:

$\alpha \rightarrow$ Buffer Gain from the Non-inverting Input to the Inverting Input

$R_I \rightarrow$ Buffer Output Impedance

$i_{ERR} \rightarrow$ Feedback Error Current Signal

$Z(s) \rightarrow$ Frequency Dependent Open Loop Transimpedance Gain from i_{ERR} to V_O

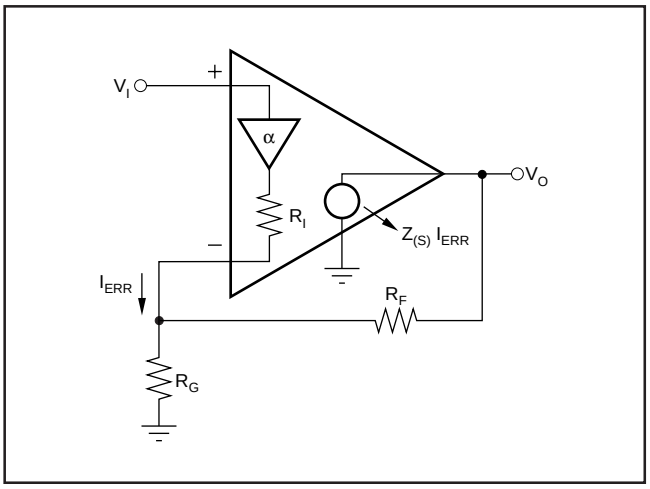


FIGURE 2. Current-Feedback Transfer Function Analysis Circuit.

The buffer gain is typically very close to 1.00 and is normally neglected from signal gain considerations. It will, however set the CMRR for a single op amp differential-amplifier configuration. For a buffer gain $\alpha < 1.0$, the CMRR = $-20 \cdot \log (1-\alpha)$ dB.

R_I, the buffer output impedance, is a critical portion of the bandwidth control equation. The OPA2607 has an R_I typically about 33Ω.

A current-feedback op amp senses an error current in the inverting node (as opposed to a differential input error voltage for a voltage-feedback op amp) and passes this on to the output through an internal frequency dependent transimpedance gain. The typical performance curves show this open-loop transimpedance response. This is analogous to the open-loop voltage gain curve for a voltage-feedback op amp. Developing the transfer function for the circuit of Figure 2 gives Equation 1:

$$\frac{V_O}{V_I} = \frac{\alpha\left(1+\frac{R_F}{R_G}\right)}{1+\frac{R_F + R_I\left(1+\frac{R_F}{R_G}\right)}{Z_{(S)}}} = \frac{\alpha\, NG}{1+\frac{R_F + R_I\, NG}{Z_{(S)}}} \qquad \left[NG \equiv \left(1+\frac{R_F}{R_G}\right)\right] \tag{1}$$

This is written in a loop-gain analysis format where the errors arising from a finite open-loop gain are shown in the denominator. If Z(s) were infinite over all frequencies, the denominator of Equation 1 would reduce to 1 and the ideal desired signal gain shown in the numerator would be achieved. The fraction in the denominator of Equation 1 determines the frequency response. Equation 2 shows this as the loop-gain equation:

$$\frac{Z_{(S)}}{R_F + R_I\, NG} = \text{Loop Gain} \tag{2}$$

If 20 • log (R_F + NG • R_I) were drawn on top of the open-loop transimpedance plot, the difference between the two would be the loop gain at a given frequency. Eventually, Z(s) rolls off to equal the denominator of Equation 2 at which point the loop gain has reduced to 1 (and the curves have intersected). This point of equality is where the amplifier's closed-loop frequency response given by Equation 1 will start to roll off, and is exactly analogous to the frequency at which the noise gain equals the open-loop voltage gain for a voltage-feedback op amp. The difference here is that the total impedance in the denominator of Equation 2 may be controlled somewhat separately from the desired signal gain (or NG).

The OPA2607 is internally compensated to give a maximally flat frequency response for R_F = 1.21kΩ at NG = 8 on ±12V supplies. Evaluating the denominator of Equation 2 (which is the feedback transimpedance) gives an optimal target of 1.44kΩ. As the signal gain changes, the contribution of the NG x R_I term in the feedback transimpedance will change, but the total can be held constant by adjusting R_F. Equation 3 gives an approximate equation for optimum R_F over signal gain:

$$R_F = 1441\Omega - NG\ R_I \qquad (3)$$

As the desired signal gain increases, this equation will eventually predict a negative R_F. A somewhat subjective limit to this adjustment can also be set by holding R_G to a minimum value of 20Ω. Lower values will load both the buffer stage at the input and the output stage if R_F gets too low—actually decreasing the bandwidth. Figure 3 shows the recommended R_F versus NG. The values for R_F versus Gain shown here are approximately equal to the values used to generate the typical performance curves. They differ in that the optimized values used in the typical performance curves are also correcting for board parasitics not considered in the simplified analysis leading to Equation 3. The values shown in Figure 3 give a good starting point for design where bandwidth optimization is desired.

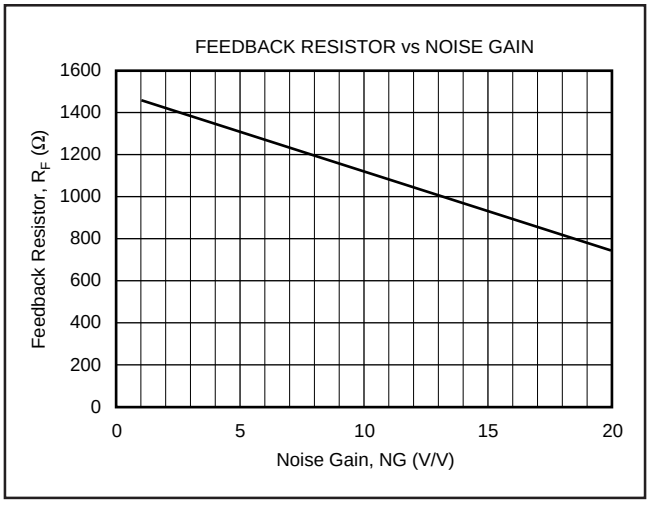


FIGURE 3. Recommended Feedback Resistor vs Noise Gain.

The total impedance going into the inverting input may be used to adjust the closed-loop signal bandwidth. Inserting a series resistor between the inverting input and the summing junction will increase the feedback impedance (denominator of Equation 2), decreasing the bandwidth. The internal buffer output impedance for the OPA2607 is slightly influenced by the source impedance looking out of the non-inverting input terminal. High-source resistors will have the effect of increasing R_I, decreasing the bandwidth. For those single-supply applications which develop a midpoint bias at the non-inverting input through high-valued resistors, the decoupling capacitor is essential for power-supply ripple rejection, non-inverting input-noise current shunting, and to minimize the high frequency value for R_I in Figure 2.

INVERTING AMPLIFIER OPERATION

Since the OPA2607 is a wideband, current-feedback op amp, most of the familiar op amp application circuits are available to the designer. Those dual op amp applications that require considerable flexibility in the feedback element (e.g. integrators, transimpedance, some filters) should consider the unity gain stable voltage-feedback OPA2680, since the feedback resistor is the compensation element for a current-feedback op amp. Wideband inverting operations (and especially summing) are particularly suited to the OPA2607. Figure 4 shows a typical inverting configuration where the I/O impedances are 50Ω.

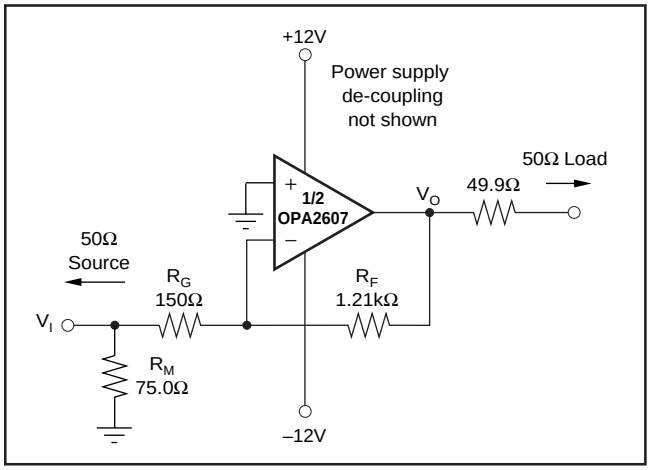


FIGURE 4. Inverting Gain of –8 with Impedance Matching.

In the inverting configuration, two key design considerations must be noted. The first is that the gain resistor (R_G) becomes part of the signal-channel input impedance. If input impedance matching is desired (which is beneficial whenever the signal is coupled through a cable, twisted pair, long PC board trace, or other transmission line conductor), it is normally necessary to add an additional matching resistor (R_M) to ground. R_G by itself is normally not set to the required input impedance since its value, along with the desired gain, will determine an R_F which may be non-optimal from a frequency response standpoint. The total input impedance for the source becomes the parallel combination of R_G and R_M.

The second major consideration, touched on in the previous paragraph, is that the signal-source impedance becomes part of the noise-gain equation and will have slight effect on the bandwidth through Equation 1. The values shown in Figure 4 have accounted for this by slightly decreasing R_F to re-optimize the bandwidth for the noise gain. In the example of Figure 4, the R_M value combines in parallel with the external 50Ω source impedance, yielding an effective driving impedance of 50Ω || 75Ω = 30.0Ω. This impedance is added in series with R_G for calculating the noise gain, which gives NG = 7.72 (instead of NG = 9.00 with a 0Ω source). This value, along with the R_F of Figure 3 and the inverting input impedance of 33Ω, are inserted into Equation 3 to get R_F = 1186Ω.

Note that the non-inverting input in this bipolar-supply inverting application is connected directly to ground. It is often suggested that an additional resistor be connected to ground on the non-inverting input to achieve bias-current error cancellation at the output. The input bias currents for a current-feedback op amp are not generally matched in either magnitude or polarity. Connecting a resistor to ground on the non-inverting input of the OPA2607 in the circuit of Figure 4 will actually provide additional gain for that input's bias and noise currents, but will not decrease the output DC error since the input bias currents are not matched.

OUTPUT CURRENT AND VOLTAGE

The OPA2607 provides outstanding output voltage and current capabilities. Under no-load conditions at 25°C, the output voltage typically swings within 0.8V of either supply rail; the guaranteed swing limit is within 1.1V of either rail. Into a 5Ω load (the minimum tested load), it is guaranteed to deliver more than ±180mA.

DISTORTION PERFORMANCE

The OPA2607 provides good distortion performance into a 100Ω load on ±12V supplies. Relative to alternative solutions, it provides exceptional performance into lighter loads. Increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network—in the non-inverting configuration (Figure 1) this is the sum of R_F + R_G, while in the inverting configuration it is just R_F. Also, providing an additional supply decoupling capacitor (0.1µF) between the supply pins (for bipolar operation) improves the 2nd-order distortion slightly (3 to 6dB).

In most op amps, increasing the output voltage swing increases harmonic distortion directly. As the typical performance curves show, the spurious intermodulation powers do not increase as predicted by a traditional intercept model. As the fundamental power level increases, the dynamic range does not decrease significantly. For 2 tones centered at 1MHz, with 10dBm/tone into a matched 50Ω load (i.e. 2Vp-p for each tone at the load, which requires 8Vp-p for the overall 2-tone envelope at the output pin), the typical performance curves show 85dBc difference between the test-tone power and the 3rd-order intermodulation spurious levels.

NOISE PERFORMANCE

Wideband current-feedback op amps generally have a higher output noise than comparable voltage-feedback op amps. The OPA2607 offers an excellent balance between voltage and current noise terms to achieve low output noise. The inverting current noise (15pA/√Hz) is significantly lower than competitive solutions, while the input voltage noise (1.7nV/√Hz) is lower than most unity gain stable, wideband, voltage-feedback op amps. This low input voltage noise was achieved at the price of higher non-inverting input current noise (11pA/√Hz). As long as the AC source impedance looking out of the non-inverting node is less than 100Ω, this current noise will not contribute significantly to the total output noise. The op amp input voltage noise and the two input current noise terms combine to give low output noise under a wide variety of operating conditions. Figure 5 shows the op amp noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

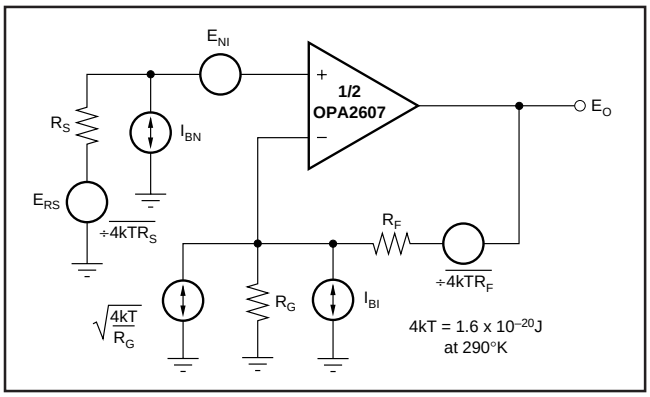


FIGURE 5. Op Amp Noise Analysis Model.

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 4 shows the general form for the output noise voltage using the terms shown in Figure 5.

(4)

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)NG^2 + \left(I_{BI}R_F\right)^2 + 4kTR_FNG}$$

Dividing this expression by the noise gain (NG = (1+R_F/R_G)) will give the equivalent input referred spot noise voltage at the non-inverting input as shown in Equation 5.

(5)

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}}$$

Evaluating these two equations for the OPA2607 circuit and component values shown in Figure 1 will give a total output spot noise voltage of 27nV/√Hz and a total equivalent input spot noise voltage of 3.4nV/√Hz. This total input referred spot noise voltage is higher than the 1.7nV/√Hz specifica-

tion for the op amp voltage noise alone. This reflects the noise added to the output by the inverting current noise times the feedback resistor. If the feedback resistor is reduced in high-gain configurations (as suggested previously), the total input referred voltage noise given by Equation 5 will approach just the 1.7nV/$\sqrt{Hz}$ of the op amp itself. For example, going to a gain of +20 using R_F = 750Ω will give a total input referred noise of 2.0nV/$\sqrt{Hz}$.

DC ACCURACY AND OFFSET CONTROL

A current-feedback op amp like the OPA2607 provides exceptional bandwidth in high gains, giving fast pulse settling but only moderate DC accuracy. The typical specifications show an input offset voltage comparable to high-speed voltage-feedback amplifiers. However, the two input bias currents are somewhat higher and are unmatched. Whereas bias current cancellation techniques are very effective with most voltage-feedback op amps, they do not generally reduce the output DC offset for wideband current-feedback op amps. Since the two input bias currents are unrelated in both magnitude and polarity, matching the source impedance looking out of each input to reduce their error contribution to the output is ineffective. Evaluating the configuration of Figure 1, using worst case +25°C input offset voltage and the two input bias currents, gives a worst case output offset range equal to:

$$\pm (NG \bullet V_{OS(MAX)}) \pm (I_{BN} \bullet R_S/2 \bullet NG) \pm (I_{BI} \bullet R_F)$$

where NG = non-inverting signal gain

$$= \pm (8 \bullet 7mV) \pm (12\mu A \bullet 25\Omega \bullet 8) \pm (40\mu A \bullet 1.21k\Omega)$$

$$= \pm 56.0mV \pm 2.4mV \pm 48.4mV$$

$$= \pm 107mV$$

THERMAL ANALYSIS

Maximum desired junction temperature will set the maximum allowed internal power dissipating. In no case should the maximum junction temperature exceed 175°C. The operating junction temperature is given by:

$$T_J = T_A + P_D \theta_{JA} \quad (6)$$

where T_A is the ambient temperature, P_D is the average power dissipation as calculated below, and θ_{JA} is the package thermal resistance shown in the specifications.

The total internal power dissipation of a single amplifier, assuming bipolar supplies ($\pm V_S$), is:

$$P_D = 2V_S I_Q + V_S I_{O(AVE)} - I^2_{O(RMS)} R_L \quad (7)$$

where I_Q is the quiescent supply current, $I_{O(AVE)}$ is the average output current, $I_{O(RMS)}$ is the root-mean-square output current, and R_L is the load seen by the output. Under absolute worst case conditions, with $V_O = V_S/2$, Equation 7 becomes:

$$P_D = 2V_S I_Q + V_S^2/(4R_L) \quad (8)$$

The ADSL Upstream Driver shown on the front page will be used as an example of these calculations. The ADSL (G.DMT) standard uses a spectrally-efficient coding technique, which produces a near-Gaussian output voltage distribution. Under these conditions, $I_{O(AVE)}$ = 0.8 $I_{O(RMS)}$. The maximum allowed crest factor in this standard is CF = 5.33Vpk/Vrms. We now calculate for each amplifier individually:

$$R_L = \left(78.7\Omega + \frac{100\Omega/2}{0.8^2}\right) \left\| \left(1.21k\Omega + \frac{348\Omega}{2}\right) \right. \quad (9)$$

$$= 141\Omega$$

$$I_{O(PK)} = \frac{V_{O(PK)}}{R_L} = \frac{38Vp-p/2}{141\Omega} = 135mA$$

$$I_{O(RMS)} = \frac{I_{O(PK)}}{CF} = \frac{135mA}{5.33} = 25.3mA$$

$$I_{O(AVE)} = 0.8\, I_{O(RMS)} = 20.2mA$$

Now calculate the typical junction temperature of both channels of the OPA2607H (PSO-8 SO-COOL™ Package) based on Equations 6 and 7:

$$P_D = 2 \bullet 12V \bullet 16mA + \quad (10)$$

$$2 \bullet (12V \bullet 20.2mA) - (25.3mA)^2 \bullet 141\Omega$$

$$= 0.69W$$

$$T_J = 85°C + 0.69W \bullet 50°C/W$$

$$= 120°C$$

The junction temperature of this example is well below 175°C absolute maximum because the PSO-8 power package has such a low thermal impedance when properly connected to the $-V_S$ power plane (see the Board Layout Guidelines section). To help illustrate this point, the regular SO-8 package (OPA2607U) gives T_J = 171°C under the same conditions.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high-frequency amplifier like the OPA2607 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability. On the non-inverting input it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the power supply pins to high frequency 0.1μF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power supply

connections (on pins 4 and 7) should always be decoupled with these capacitors. An optional supply decoupling capacitor across the two power supplies (for bipolar operation) will improve 2nd harmonic distortion performance. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

c) Careful selection and placement of external components will preserve the high-frequency performance of the OPA2607. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film and carbon composition axially leaded resistors can also provide good high-frequency performance. Again, keep their leads and PC board trace length as short as possible. Never use wirewound-type resistors in a high-frequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as non-inverting input termination resistors, should also be placed close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. The frequency response is primarily determined by the feedback resistor value as described previously. Increasing its value will reduce the bandwidth, while decreasing it will give a more peaked frequency response. The 1.21kΩ feedback resistor used in the typical performance specifications at a gain of +8 on ±12V supplies is a good starting point for design. Note that a 1.50kΩ feedback resistor, rather than a direct short, is recommended for the unity-gain follower application. A current-feedback op amp requires a feedback resistor even in the unity-gain follower configuration to control stability.

d) Connections to other wideband devices on the board may be made with short direct traces or through on-board transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of recommended "R_S vs Capacitive Load". Low parasitic capacitive loads (< 5pF) may not need an R_S since the OPA2607 is nominally compensated to operate with a 2pF parasitic load. If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched-impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary on board, and in fact a higher-impedance environment will improve distortion as shown in the "Distortion vs Load" plots. With a characteristic board-trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA2607 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device: this total effective impedance should be set to match the trace impedance. The high output voltage and current capability of the OPA2607 allows multiple destination devices to be handled as separate transmission lines, each with their own series and shunt terminations. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of "R_S vs Capacitive Load". This will not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) Do not socket a high speed part like the OPA2607. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA2607 onto the board.

f) Use the $-V_S$ plane to conduct heat out of the PSO-8 and PSO-14 Power Packages (OPA2607H and OPA2607N). These packages attach the die directly to a metal slug in its bottom, which you should solder to the board. This slug needs to be connected electrically to the negative supply plane, which must have a minimum area of 2" x 2" (50mm x 50mm) to produce the θ_{JA} values in the specifications table. More details will be found in the data sheets that accompany the demo boards described in the Demonstration Boards section of this data sheet.

INPUT AND ESD PROTECTION

The OPA2607 is built using a very high-speed complementary bipolar process. All device pins have ESD protection using internal diodes to the power supplies as shown in Figure 6. The OPA2607 has an ESD rating of 4000V human body model, and 300V machine model.

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (e.g. in systems with ±30V supply parts driving into the OPA2607), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response.

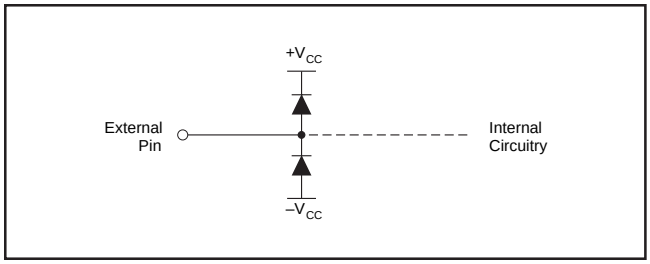


FIGURE 6. Internal ESD Protection.