

December 1993

CMOS Analog Multiplexers

Features

- Low Power Consumption
- TTL and CMOS Compatible Address and Enable Inputs
- 44V Maximum Power Supply Rating
- High Latch-Up Immunity
- Break-Before-Make Switching
- Alternate Source

Applications

- Data Acquisition Systems
- Communication Systems
- Signal Multiplexing/Demultiplexing
- Audio Signal Multiplexing

Description

The DG506A, DG507A, DG508A and DG509A are CMOS monolithic 16-channel/dual 8-channel and 8-channel/dual 4-channel analog multiplexers, which can also be used as demultiplexers. An enable input is provided. When the enable input is high, a channel is selected by the address inputs, and when low, all channels are off.

A channel in the ON state conducts current equally well in both directions. In the OFF state each channel blocks voltages up to the supply rails. The address inputs and the enable input are TTL and CMOS compatible over the full specified operating temperature range.

The DG506A, DG507A, DG508A and DG509A are pinout compatible with the industry standard devices.

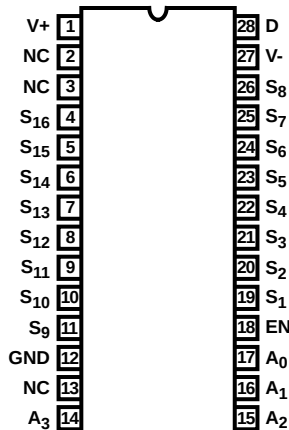
Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE
DG506AAK	-55°C to +125°C	28 Lead Ceramic DIP
DG506AAK/883B	-55°C to +125°C	28 Lead Ceramic DIP
DG506ABK	-25°C to +85°C	28 Lead Ceramic DIP
DG506ABY	-25°C to +85°C	28 Lead Plastic DIP
DG506ACJ	0°C to +70°C	28 Lead Plastic DIP
DG506ACK	0°C to +70°C	28 Lead Ceramic DIP
DG506ACY	0°C to +70°C	28 Lead SOIC
DG507AAK	-55°C to +125°C	28 Lead Ceramic DIP
DG507AAK/883B	-55°C to +125°C	28 Lead Ceramic DIP
DG507ABK	-25°C to +85°C	28 Lead Ceramic DIP
DG507ABY	-25°C to +85°C	28 Lead Plastic DIP
DG507ACJ	0°C to +70°C	28 Lead Plastic DIP
DG507ACK	0°C to +70°C	28 Lead Ceramic DIP
DG507ACY	0°C to +70°C	28 Lead SOIC

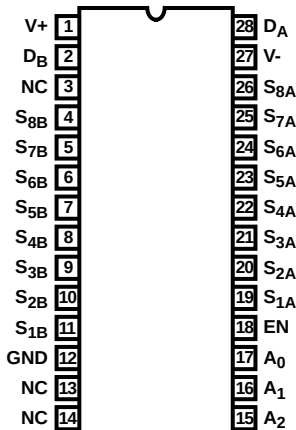
PART NUMBER	TEMP. RANGE	PACKAGE
DG508AAK	-55°C to +125°C	16 Lead Ceramic DIP
DG508AAK/883B	-55°C to +125°C	16 Lead Ceramic DIP
DG508ABK	-25°C to +85°C	16 Lead Ceramic DIP
DG508ABY	-25°C to +85°C	16 Lead Plastic DIP
DG508ACJ	0°C to +70°C	16 Lead Plastic DIP
DG508ACK	0°C to +70°C	16 Lead Ceramic DIP
DG508ACY	0°C to +70°C	16 Lead SOIC (W)
DG509AAK	-55°C to +125°C	16 Lead Ceramic DIP
DG509AAK/883B	-55°C to +125°C	16 Lead Ceramic DIP
DG509ABK	-25°C to +85°C	16 Lead Ceramic DIP
DG509ABY	-25°C to +85°C	16 Lead Plastic DIP
DG509ACJ	0°C to +70°C	16 Lead Plastic DIP
DG509ACK	0°C to +70°C	16 Lead Ceramic DIP
DG509ACY	0°C to +70°C	16 Lead SOIC (W)

Pinouts

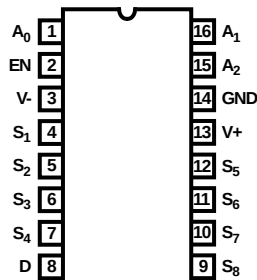
DG506A (PDIP, CDIP, SOIC)
TOP VIEW



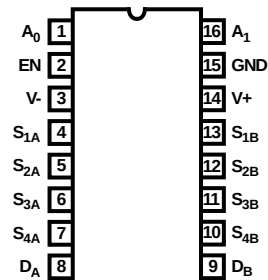
DG507A (PDIP, CDIP, SOIC)
TOP VIEW



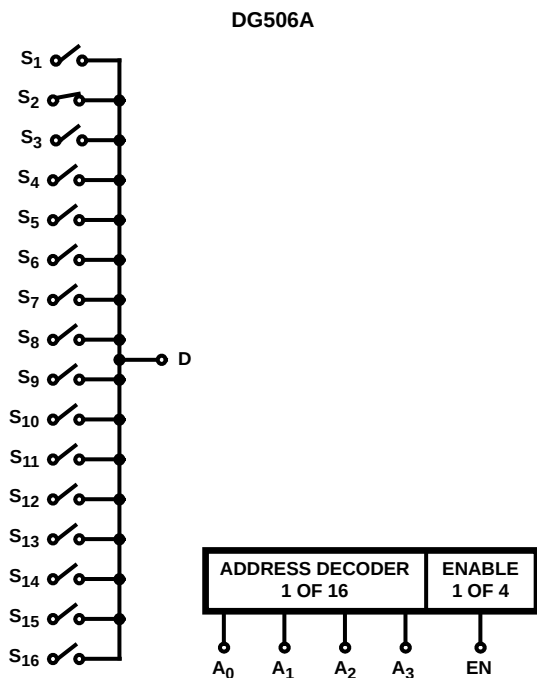
DG508A (PDIP, CDIP, SOIC)
TOP VIEW



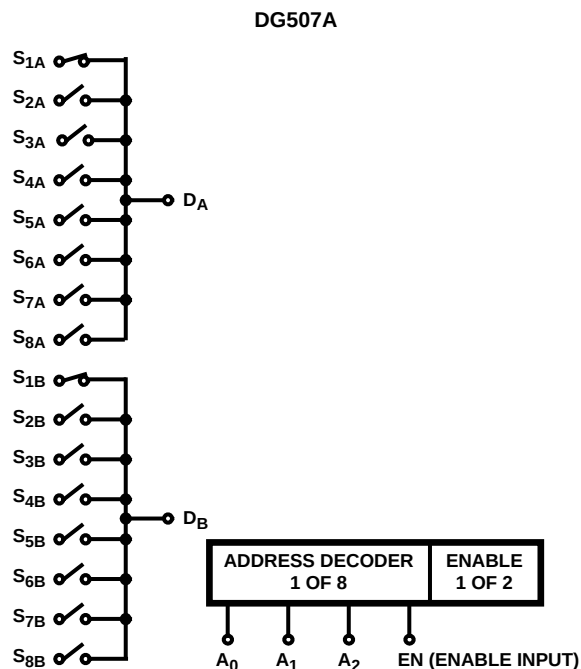
DG509A (PDIP, CDIP, SOIC)
TOP VIEW



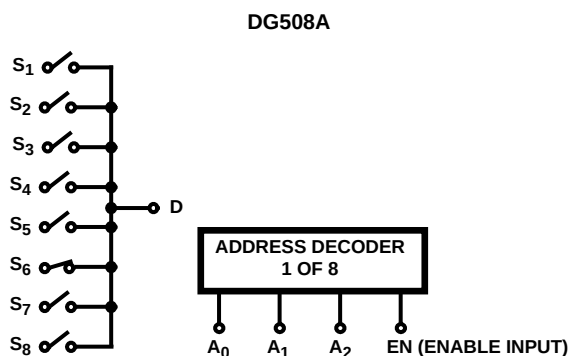
Functional Block Diagrams



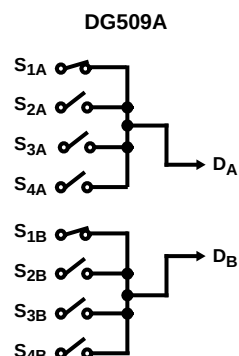
4 Line Binary Address Inputs
(0 0 0 1) and EN = 5V
Above example shows channel 2 turned ON.



3 Line Binary Address Inputs
(0 0 0) and EN = 5V
Above example shows channels 1_A and 1_B turned ON.

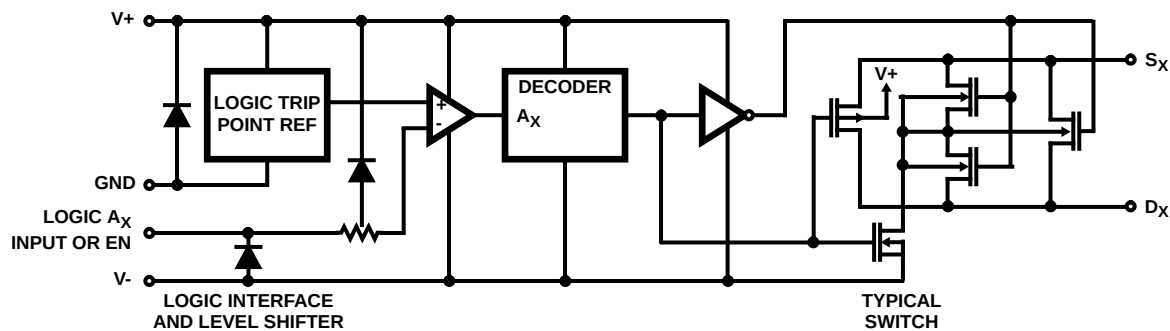


3 Line Binary Address Inputs
(1 0 1) and EN = 1
Above example shows channel 6 turned ON.



2 Line Binary Address Inputs
(0 0) and EN = 1
Above example shows channels 1_A and 1_B turned ON.

Schematic Diagram



Specifications DG506A, DG507A, DG508A, DG509A

Absolute Maximum Ratings

V+ to V-	44V
V- to Ground	-25V
V _{IN} to Ground (Note 1)	(V- -2V), (V+ +2V)
V _S or V _D to V+ (Note 1)	+2, (V- -2V)
V _S or V _D to V- (Note 1)	-2, (V+ +2V)
Current, any Terminal Except S or D	30mA
Continuous Current, S or D	20mA
Peak Current, S or D (Pulsed at 1ms, 10% Duty Cycle Max.)	40mA
Storage Temperature	
C Suffix	-65°C to +125°C
A & B Suffix	-65°C to +150°C
Lead Temperature (Soldering 10s)	+300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
16 Lead Ceramic DIP Package	77°C/W	23°C/W
28 Lead Ceramic DIP Package	55°C/W	17°C/W
16 Lead Plastic DIP Package	100°C/W	-
28 Lead Plastic DIP Package	60°C/W	-
16 Lead SOIC (W) Package	100°C/W	-
28 Lead SOIC Package	70°C/W	-
Operating Temperature Range		
C Suffix	0°C to +70°C	
B Suffix	-25°C to +85°C	
A Suffix	-55°C to +125°C	
Junction Temperature		
Ceramic DIP Package	+175°C	
Plastic DIP Package	+150°C	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $T_A = +25^\circ\text{C}$, V+ = +15V, V- = -15V, GND = 0V, V_{EN} = 2.4V, Unless Otherwise Specified

PARAMETERS	TEST CONDITIONS		DG506AA, DG507AA, DG508AA, DG509AA			DG506AB/C, DG507AB/C, DG508AB/C, DG509AB/C			UNITS
			MIN	(NOTE 2) TYP	MAX	MIN	(NOTE 2) TYP	MAX	
DYNAMIC CHARACTERISTICS									
Switching Time of Multi-plexer, t _{TRANSITION}	See Figure 3		-	0.6	1	-	0.6	-	μs
Break-Before-Make Interval, t _{OPEN}	See Figure 5		-	0.2	-	-	0.2	-	μs
Enable Turn-On Time, t _{ON(EN)}	See Figure 4		-	1	1.5	-	1	-	μs
Enable Turn-Off Time, t _{OFF(EN)}	See Figure 4		-	0.4	1.0	-	0.4	-	μs
Off Isolation, OIRR	V _{EN} = 0V, R _L = 1kΩ, C _L = 15pF, V _S = 7V _{RMS} , f = 500kHz (Note 4)		-	68	-	-	68	-	dB
Source Off Capacitance, C _{S(OFF)}	V _S = 0V, V _{EN} = 0V, f = 140kHz								
DG506A, DG507A			-	6	-	-	6	-	pF
DG508A, DG509A			-	5	-	-	5	-	pF
Drain Off Capacitance, C _{D(OFF)}	V _D = 0V, V _{EN} = 0V, f = 140kHz								
DG506A			-	45	-	-	45	-	pF
DG507A			-	23	-	-	23	-	pF
DG508A			-	25	-	-	25	-	pF
DG509A			-	12	-	-	12	-	pF
Charge Injection, Q	See Figure 6								
DG506A, DG507A			-	6	-	-	6	-	pC
DG508A, DG509A		-	4	-	-	4	-	pC	
INPUT									
Address Input Current, Input Voltage High, I _{AH}	V _A = 2.4V		-10	-0.002	-	-10	-0.002	-	μA
	V _A = 15V		-	0.006	10	-	0.006	10	μA
Address Input Current Input Voltage Low, I _{AL}	V _{EN} = 2.4V	V _A = 0V	-10	-0.002	-	-10	-0.002	-	μA
	V _{EN} = 0V		-10	-0.002	-	-10	-0.0002	-	μA

Specifications DG506A, DG507A, DG508A, DG509A

Electrical Specifications $T_A = +25^{\circ}\text{C}$, $V_+ = +15\text{V}$, $V_- = -15\text{V}$, $\text{GND} = 0\text{V}$, $V_{\text{EN}} = 2.4\text{V}$,
Unless Otherwise Specified **(Continued)**

PARAMETERS	TEST CONDITIONS		DG506AA, DG507AA, DG508AA, DG509AA			DG506AB/C, DG507AB/C, DG508AB/C, DG509AB/C			UNITS	
			MIN	(NOTE 2) TYP	MAX	MIN	(NOTE 2) TYP	MAX		
SWITCH										
Analog Signal Range, V _{ANALOG}	(Note 6)		-15	-	+15	-15	-	+15	V	
Drain Source On Resistance, R _{DS(ON)}	Sequence Each Switch On V _{AL} = 0.8V V _{AH} = 2.4V	I _S = -200μA, V _D = +10V	-	270	400	-	270	450	Ω	
		I _S = -200μA, V _D = -10V	-	230	400	-	230	450	Ω	
Greatest Change in Drain Source On Resistance Between Channels, ΔR _{DS(ON)}	-10V ≤ V _S ≤ +10V ΔR _{DS(ON)} = $\frac{R_{DS(ON)MAX} - R_{DS(ON)MIN}}{R_{DS(ON)AVG}}$		-	6	-	-	6	-	%	
Source Off Leakage Current, I _{S(OFF)}	V _{EN} = 0V	V _S = +10V, V _D = -10V	-1	0.002	1	-5	0.002	5	nA	
		V _S = -10V, V _D = +10V	-1	-0.005	1	-5	-0.005	5	nA	
Drain Off Leakage Current, I _{D(OFF)} DG506A	V _{EN} = 0V	V _S = -10V, V _D = +10V	-10	0.02	10	-20	0.02	20	nA	
		V _S = +10V, V _D = -10V	-10	-0.03	10	-20	-0.03	20	nA	
DG507A		V _S = -10V, V _D = +10V	-5	0.007	5	-10	0.007	10	nA	
V _S = +10V, V _D = -10V		-5	-0.015	5	-10	-0.015	10	nA		
DG508A		V _S = -10V, V _D = +10V	-	0.01	10	-	0.01	20	nA	
V _S = +10V, V _D = -10V		-10	-0.015	-	-20	-0.015	-	nA		
DG509A		V _S = -10V, V _D = +10V	-	0.005	10	-	0.005	20	nA	
V _S = +10V, V _D = -10V		-10	-0.008	-	-20	-0.008	-	nA		
Drain On Leakage Current, I _{D(ON)} DG506A	(Note 5) Sequence Each Switch On V _{AL} = 0.8V V _{AH} = 2.4V	V _D = V _{S(ALL)} = +10V	-10	0.03	10	-20	0.03	20	nA	
		V _D = V _{S(ALL)} = -10V	-10	-0.06	10	-20	-0.06	20	nA	
		DG507A	V _D = V _{S(ALL)} = +10V	-5	0.015	5	-10	0.015	10	nA
		V _D = V _{S(ALL)} = -10V	-5	-0.03	5	-10	-0.03	10	nA	
		DG508A	V _D = V _{S(ALL)} = +10V	-	0.015	10	-	0.015	20	nA
		V _D = V _{S(ALL)} = -10V	-10	-0.03	-	-20	-0.03	-	nA	
		DG509A	V _D = V _{S(ALL)} = +10V	-	0.007	10	-	0.007	20	nA
		V _D = V _{S(ALL)} = -10V	-10	-0.015	-	-20	-0.015	-	nA	
POWER SUPPLY CHARACTERISTICS										
Positive Supply Current, I ₊	V _{EN} = 5.0V, V _A = 0V		-	1.3	2.4	-	1.3	2.4	mA	
Negative Supply Current, I ₋	V _{EN} = 5.0V, V _A = 0V		-1.5	-0.7	-	-1.5	-0.7	-	mA	
Positive Supply Current, I ₊ Standby	V _{EN} = 0V, V _A = 0V		-	1.3	2.4	-	1.3	2.4	mA	
Negative Supply Current, I ₋ Standby	V _{EN} = 0V, V _A = 0V		-1.5	-0.7	-	-1.5	-0.7	-	mA	

Specifications DG506A, DG507A, DG508A, DG509A

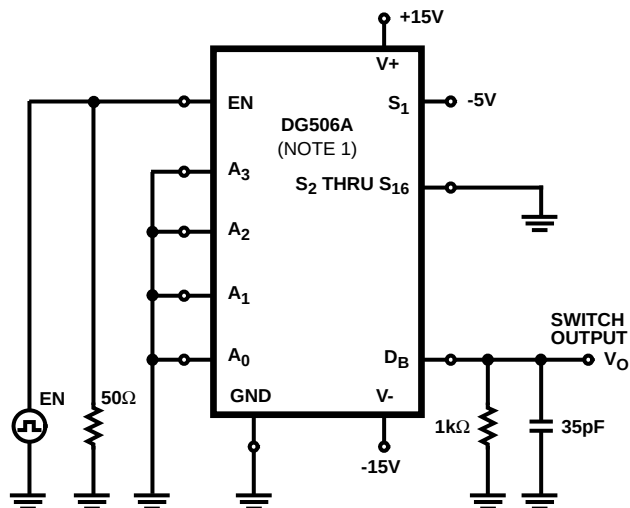
Electrical Specifications T_A = Over Operating Temperature Range, $V_+ = +15V$, $V_- = -15V$, $GND = 0V$, $V_{EN} = 2.4V$,
Unless Otherwise Specified

PARAMETERS	TEST CONDITIONS		DG506AA, DG507AA, DG508AA, DG509AA			DG506AB/C, DG507AB/C, DG508AB/C, DG509AB/C			UNITS
			MIN	(NOTE 2) TYP	MAX	MIN	(NOTE 2) TYP	MAX	
INPUT									
Address Input Current, Input Voltage High, I _{AH}	V _A = 2.4V		-30	-	-	-30	-	-	μA
	V _A = 15V		-	-	30	-	-	30	μA
Address Input Current Input Voltage Low, I _{AL}	V _{EN} = 2.4V	V _A = 0V	-30	-	-	-30	-	-	μA
	V _{EN} = 0V		-30	-	-	-30	-	-	μA
SWITCHING CHARACTERISTICS									
Analog Signal Range, V _{ANALOG}	(Note 6)		-15	-	+15	-15	-	+15	V
Drain Source On Resistance, R _{DS(ON)}	Sequence Each Switch On V _{AL} = 0.8V V _{AH} = 2.4V	I _S = -200μA, V _D = +10V	-	-	500	-	-	550	Ω
		I _S = -200μA, V _D = -10V	-	-	500	-	-	550	Ω
Source Off Leakage Current, I _{S(OFF)}	V _{EN} = 0V	V _S = +10V, V _D = -10V	-	-	50	-	-	50	nA
		V _S = -10V, V _D = +10V	-50	-	-	-50	-	-	nA
Drain Off Leakage Current, I _{D(OFF)} DG506A	V _{EN} = 0V	V _S = -10V, V _D = +10V	-	-	300	-	-	300	nA
		V _S = +10V, V _D = -10V	-300	-	-	-300	-	-	nA
DG507A		V _S = -10V, V _D = +10V	-	-	200	-	-	200	nA
		V _S = +10V, V _D = -10V	-200	-	-	-200	-	-	nA
DG508A		V _S = -10V, V _D = +10V	-	-	200	-	-	200	nA
		V _S = +10V, V _D = -10V	-200	-	-	-200	-	-	nA
DG509A		V _S = -10V, V _D = +10V	-	-	100	-	-	100	nA
		V _S = +10V, V _D = -10V	-100	-	-	-100	-	-	nA
Drain On Leakage Current, I _{D(ON)} DG506A	(Note 5) Sequence Each Switch On V _{AL} = 0.8V V _{AH} = 2.4V	V _D = V _{S(ALL)} = +10V	-	-	300	-	-	300	nA
		V _D = V _{S(ALL)} = -10V	-300	-	-	-300	-	-	nA
DG507A		V _D = V _{S(ALL)} = +10V	-	-	200	-	-	200	nA
		V _D = V _{S(ALL)} = -10V	-200	-	-	-200	-	-	nA
DG508A		V _D = V _{S(ALL)} = +10V	-	-	200	-	-	200	nA
		V _D = V _{S(ALL)} = -10V	-200	-	-	-200	-	-	nA
DG509A		V _D = V _{S(ALL)} = +10V	-	-	100	-	-	100	nA
		V _D = V _{S(ALL)} = -10V	-100	-	-	-100	-	-	nA

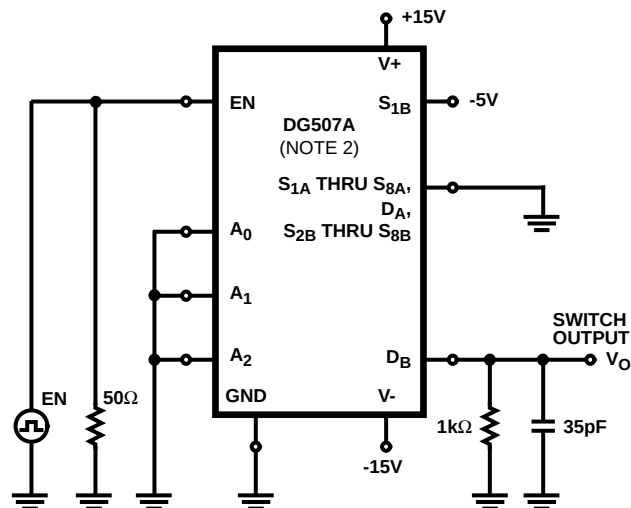
NOTES:

1. Signals on V_S , V_D or V_{IN} exceeding V_+ or V_- will be clamped by internal diodes. Limit diode forward current to maximum current ratings.
2. Typical values are for design aid only, not guaranteed and not subject to production testing.
3. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
4. Off isolation = $20\log |V_S|/|V_D|$, where V_S = input to Off switch, and V_D = output due to V_S .
5. $I_{D(ON)}$ is leakage from driver into "ON" switch.
6. Parameter not tested. Parameter guaranteed by design or characterization.

Typical Performance Curves (Continued)



NOTE: 1. Similar connections for DG508A



NOTE: 2. Similar connections for DG509A

FIGURE 4A. ENABLE t_{ON} and t_{OFF} SWITCHING TIME TEST CIRCUIT

FIGURE 4B. ENABLE t_{ON} and t_{OFF} SWITCHING TIME TEST CIRCUIT

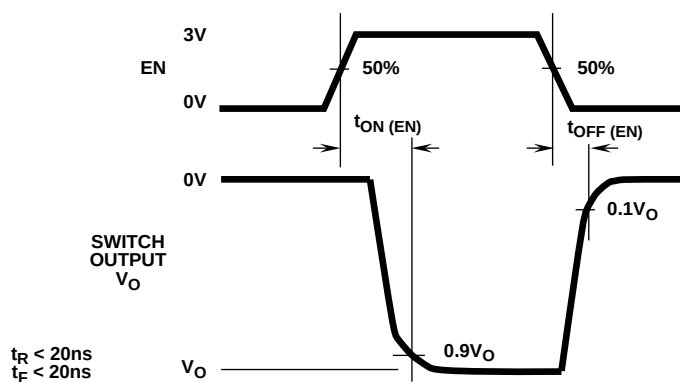
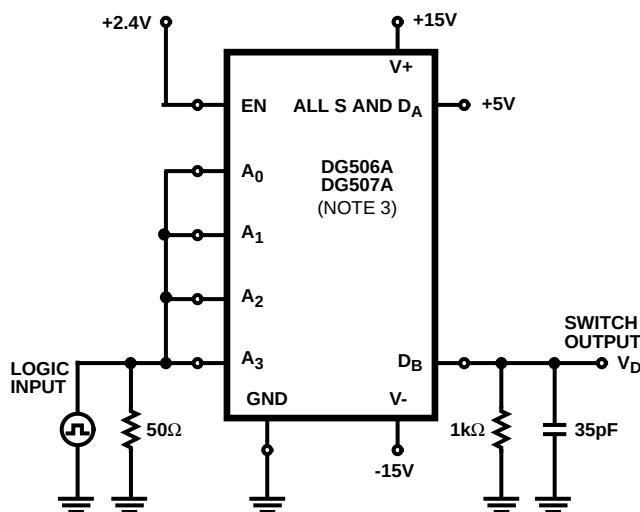


FIGURE 4C. ENABLE t_{ON} and t_{OFF} SWITCHING TIME WAVEFORMS



NOTE: 3. Similar connections for DG508A, DG509A.

FIGURE 5A. t_{OPEN} (BREAK-BEFORE-MAKE) SWITCHING TIME TEST CIRCUIT

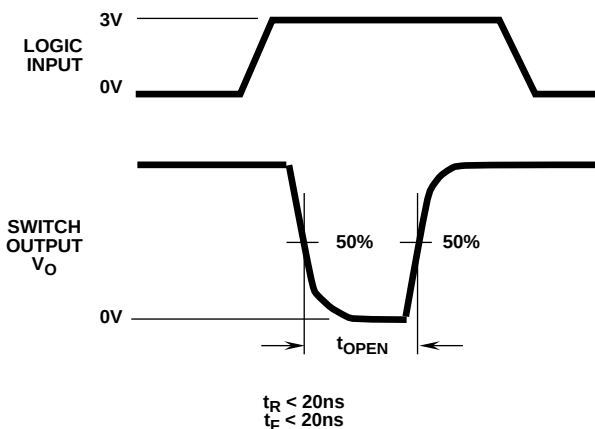
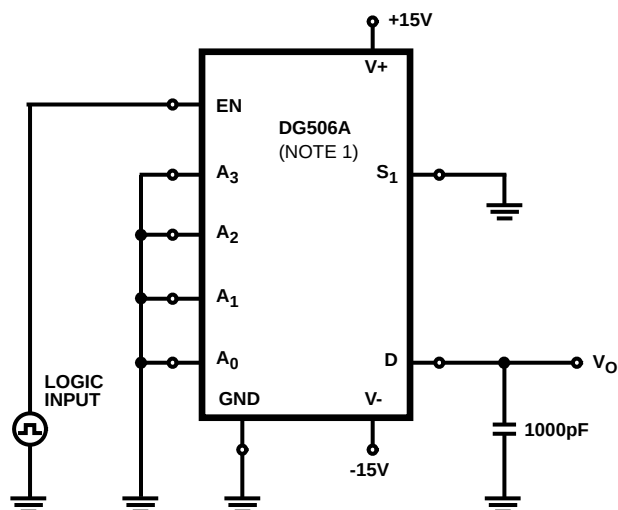


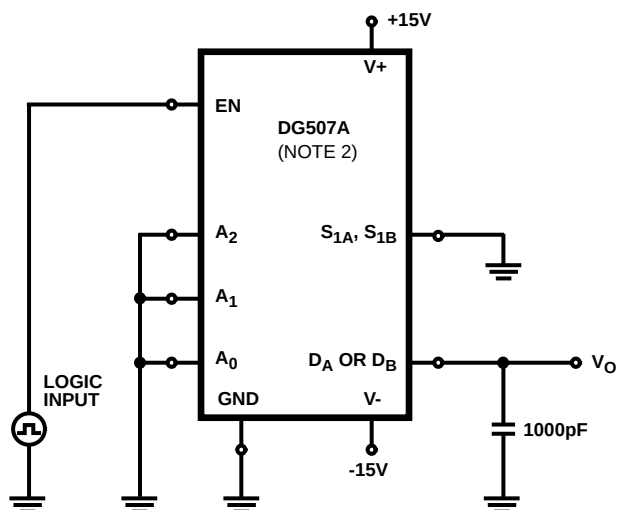
FIGURE 5B. t_{OPEN} (BREAK-BEFORE-MAKE) SWITCHING TIME WAVEFORMS

Typical Performance Curves (Continued)



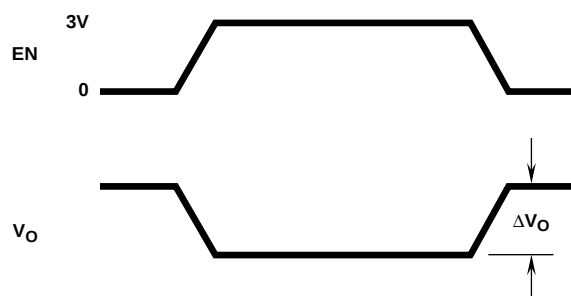
NOTE: 1. Similar connections for DG508A

FIGURE 6A. CHARGE INJECTION TEST CIRCUIT



NOTE: 2. Similar connections for DG509A

FIGURE 6B. CHARGE INJECTION TEST CIRCUIT



ΔV_O is the measured voltage error due to charge injection.
The error voltage in Coulombs is $Q = C_L \times \Delta V_O$.

FIGURE 6C. CHARGE INJECTION WAVEFORMS

DG506A, DG507A, DG508A, DG509A

Truth Tables

DG506A

A ₃	A ₂	A ₁	A ₀	EN	ON SWITCH
X	X	X	X	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

Logic "0" = V_{AL}, V_{ENL} ≤ 0.8V, Logic "1" = V_{AH}, V_{ENH} ≥ 2.4V.

DG507A

A ₂	A ₁	A ₀	EN	ON SWITCH
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic "0" = V_{AL}, V_{ENL} ≤ 0.8V, Logic "1" = V_{AH}, V_{ENH} ≥ 2.4V.

DG508A

A ₂	A ₁	A ₀	EN	ON SWITCH
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

A₀, A₁, A₂, EN
Logic "1" = V_{AH} ≥ 2.4V, Logic "0" = V_{AL} ≤ 0.8V

DG509A

A ₁	A ₀	EN	ON SWITCH
X	X	0	None
0	0	1	1A, 1B
0	1	1	2A, 2B
1	0	1	3A, 3B
1	1	1	4A, 4B

A₀, A₁, EN
Logic "1" = V_{AH} ≥ 2.4V, Logic "0" = V_{AL} ≤ 0.8V

Die Characteristics

DIE DIMENSIONS:

3810 μ m x 2770 μ m

METALLIZATION:

Type: Al

Thickness: 10k $\text{\AA}$ $\pm$ 1k $\text{\AA}$

GLASSIVATION:

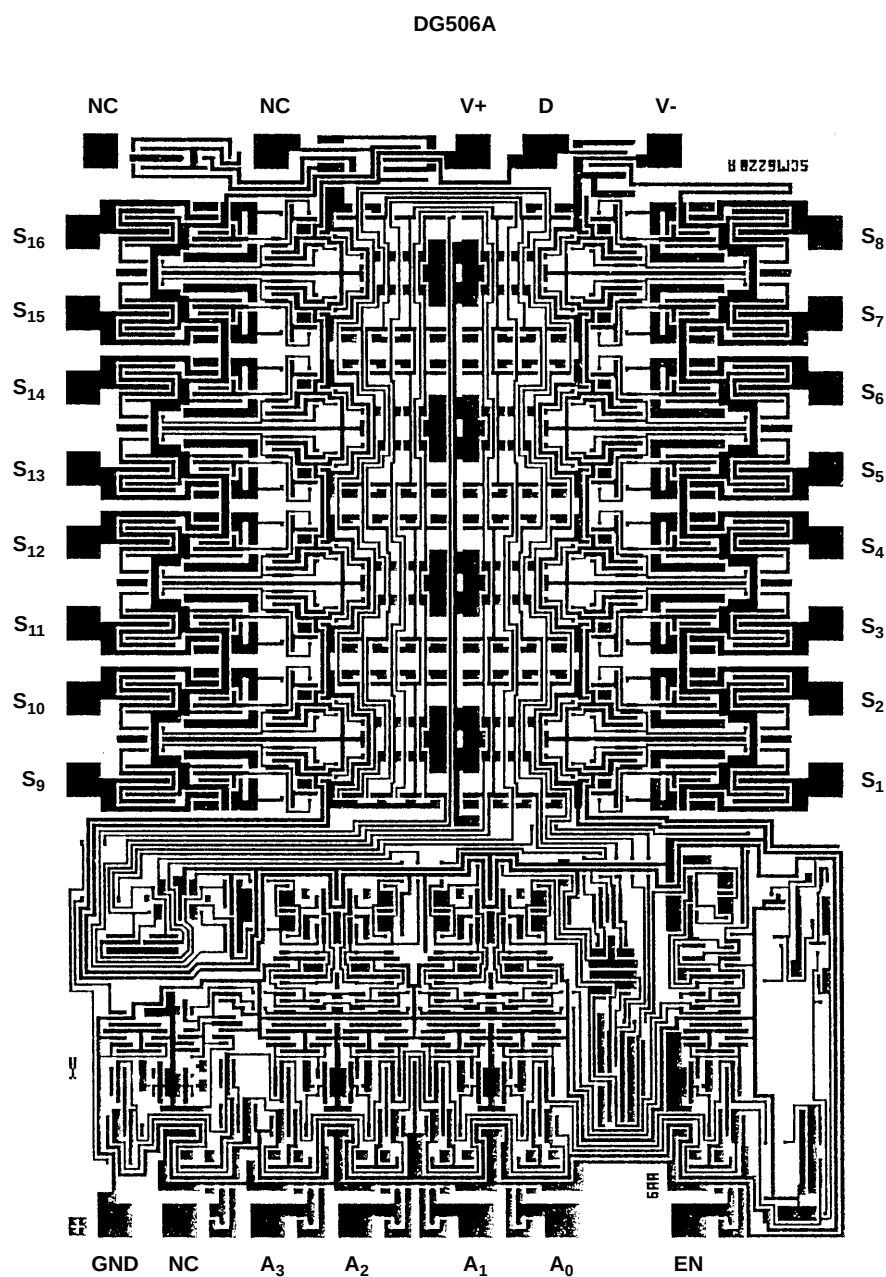
Type: PSG/Nitride

Thickness: PSG: 7k $\text{\AA}$ $\pm$ 1.4k $\text{\AA}$, Nitride: 8k $\text{\AA}$ $\pm$ 1.2k $\text{\AA}$

WORST CASE CURRENT DENSITY:

9.1 x 10⁴ A/cm²

Metallization Mask Layout



Die Characteristics

DIE DIMENSIONS:

3810 μ m x 2770 μ m

METALLIZATION:

Type: Al

Thickness: 10k $\text{\AA}$ $\pm$ 1k $\text{\AA}$

GLASSIVATION:

Type: PSG/Nitride

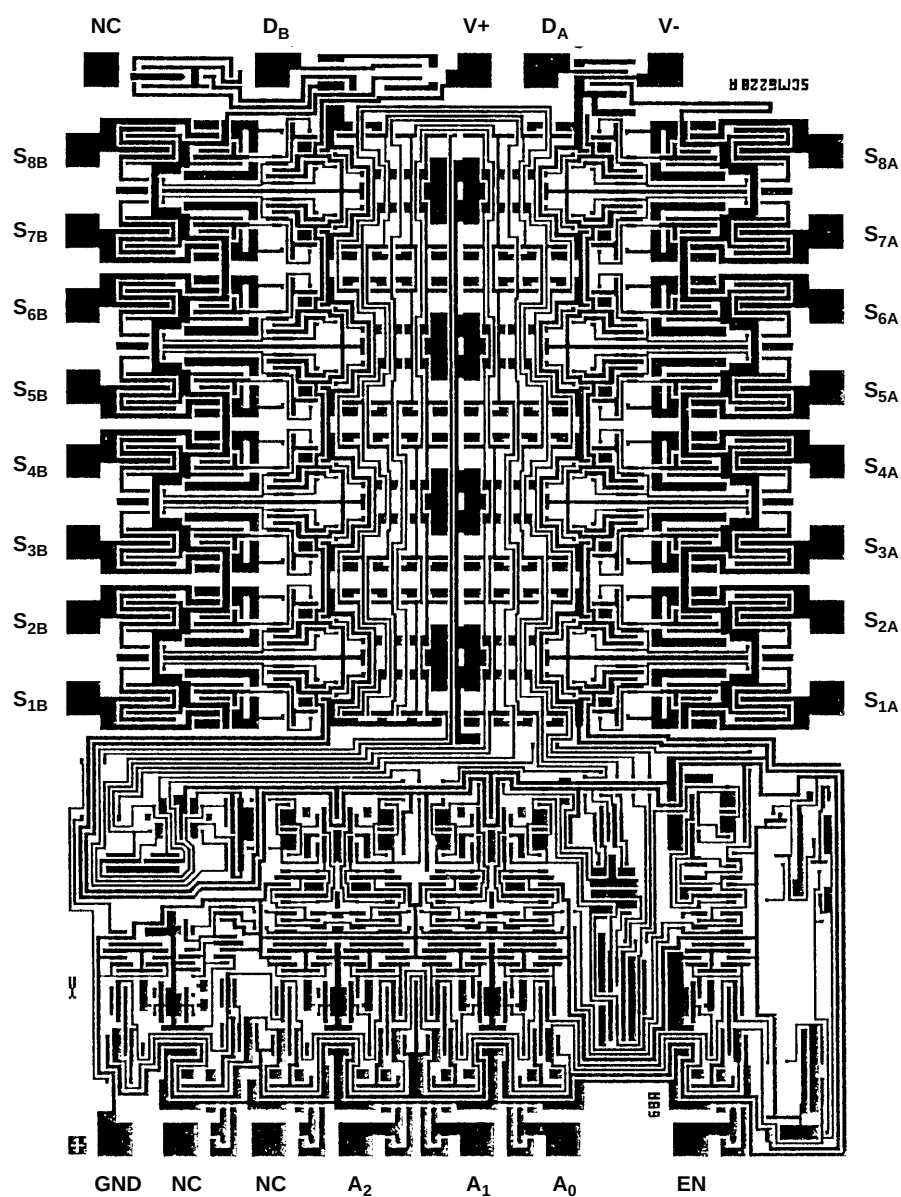
Thickness: PSG: 7k $\text{\AA}$ $\pm$ 1.4k $\text{\AA}$, Nitride: 8k $\text{\AA}$ $\pm$ 1.2k $\text{\AA}$

WORST CASE CURRENT DENSITY:

9.1 x 10⁴ A/cm²

Metallization Mask Layout

DG507A



Die Characteristics

DIE DIMENSIONS:

3100 μ m x 2083 μ m

METALLIZATION:

Type: Al

Thickness: 10k $\text{\AA}$ $\pm$ 1k $\text{\AA}$

GLASSIVATION:

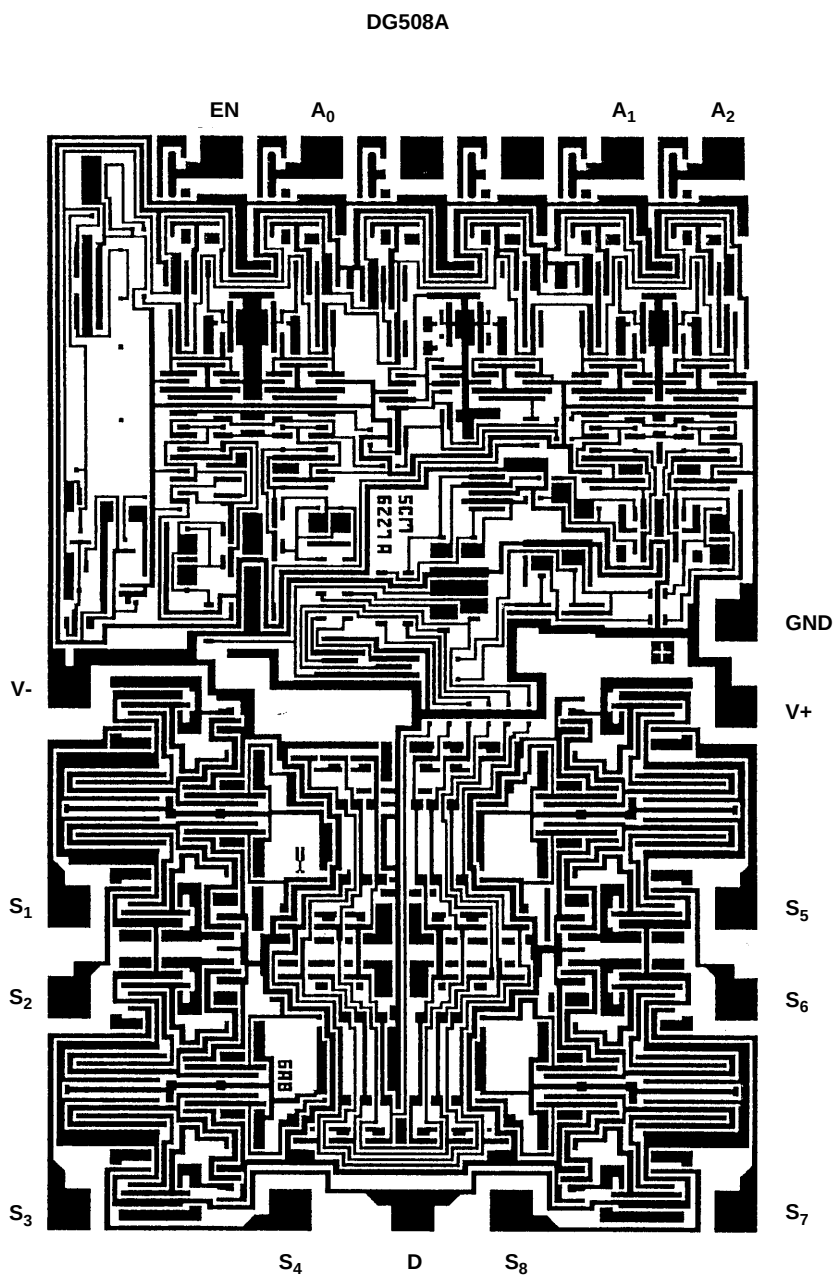
Type: PSG/Nitride

Thickness: PSG: 7k $\text{\AA}$ $\pm$ 1.4k $\text{\AA}$, Nitride: 8k $\text{\AA}$ $\pm$ 1.2k $\text{\AA}$

WORST CASE CURRENT DENSITY:

9.1 x 10⁴ A/cm²

Metallization Mask Layout



Die Characteristics

DIE DIMENSIONS:

3100μm x 2083μm

METALLIZATION:

Type: AI

Thickness: $10\text{k}\text{\AA} \pm 1\text{k}\text{\AA}$

GLASSIVATION:

Type: PSG/Nitride

Thickness: PSG: $7\text{k}\text{\AA} \pm 1.4\text{k}\text{\AA}$, Nitride: $8\text{k}\text{\AA} \pm 1.2\text{k}\text{\AA}$

WORST CASE CURRENT DENSITY:

 $9.1 \times 10^4 \text{ A/cm}^2$

Metallization Mask Layout

