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Jameco Part Number 1751367

FEATURES

- **SO-8 Package (LTC1595)**
- **DNL and INL: 1LSB Max**
- **Low Glitch Impulse: 1nV-s Typ**
- **Fast Settling to 1LSB: 2 μ s (with LT1468)**
- Pin Compatible with Industry Standard 12-Bit DACs: DAC8043 and DAC8143/AD7543
- 4-Quadrant Multiplication
- Low Supply Current: 10 μ A Max
- Power-On Reset
 - LTC1595/LTC1596: Resets to Zero Scale
 - LTC1596-1: Resets to Midscale
- 3-Wire SPI and MICROWIRE™ Compatible Serial Interface
- Daisy-Chain Serial Output (LTC1596)
- Asynchronous Clear Input
 - LTC1596: Clears to Zero Scale
 - LTC1596-1: Clears to Midscale

APPLICATIONS

- Process Control and Industrial Automation
- Software Controlled Gain Adjustment
- Digitally Controlled Filter and Power Supplies
- Automatic Test Equipment

DESCRIPTION

The LTC®1595/LTC1596/LTC1596-1 are serial input, 16-bit multiplying current output DACs. The LTC1595 is pin and hardware compatible with the 12-bit DAC8043 and comes in 8-pin PDIP and SO packages. The LTC1596 is pin and hardware compatible with the 12-bit DAC8143/AD7543 and comes in 16-pin PDIP and SO wide packages.

Both are specified over the industrial temperature range. Sensitivity of INL to op amp V_{OS} is reduced by five times compared to the industry standard 12-bit DACs, so most systems can be easily upgraded to true 16-bit resolution and linearity without requiring more precise op amps.

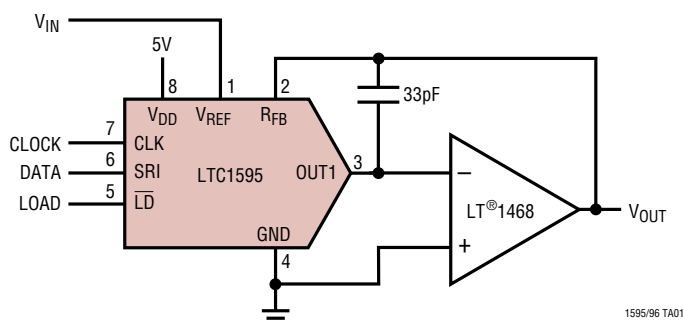
These DACs include an internal deglitching circuit that reduces the glitch impulse by more than ten times to less than 1nV-s typ.

The DACs have a clear input and a power-on reset. The LTC1595 and LTC1596 reset to zero scale. The LTC1596-1 is a version of the LTC1596 that resets to midscale.

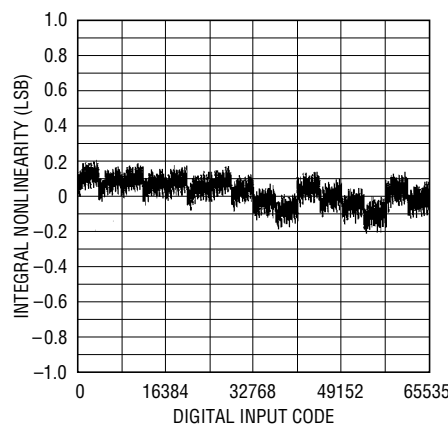
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TYPICAL APPLICATION

SO-8 Multiplying 16-Bit DAC Has Easy 3-Wire Serial Interface



Integral Nonlinearity



1595/96 TA02

LTC1595/LTC1596/LTC1596-1

ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{DD} to AGND	-0.5V to 7V	V_{OUT1}, V_{OUT2} to AGND	-0.5V to ($V_{DD} + 0.5V$)
V_{DD} to DGND	-0.5V to 7V	Maximum Junction Temperature	150°C
AGND to DGND	$V_{DD} + 0.5V$	Operating Temperature Range	
DGND to AGND	$V_{DD} + 0.5V$	LTC1595C/LTC1596C/LTC1596-1C	0°C to 70°C
V_{REF} to AGND, DGND	$\pm 25V$	LTC1595I/LTC1596I/LTC1596-1I	-40°C to 85°C
R_{FB} to AGND, DGND	$\pm 25V$	Storage Temperature Range	-65°C to 150°C
Digital Inputs to DGND	-0.5V to ($V_{DD} + 0.5V$)	Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION

TOP VIEW N8 PACKAGE 8-LEAD PDIP S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 150^{\circ}C, \theta_{JA} = 130^{\circ}C/W$ (N) $T_{JMAX} = 150^{\circ}C, \theta_{JA} = 190^{\circ}C/W$ (S)		TOP VIEW N PACKAGE 16-LEAD PDIP SW PACKAGE 16-LEAD PLASTIC SO WIDE $T_{JMAX} = 150^{\circ}C, \theta_{JA} = 100^{\circ}C/W$ (N) $T_{JMAX} = 150^{\circ}C, \theta_{JA} = 130^{\circ}C/W$ (SW)	
ORDER PART NUMBER		ORDER PART NUMBER	
LTC1595ACN8	LTC1595AIN8	LTC1596ACN	LTC1596AIN
LTC1595ACS8	LTC1595AIS8	LTC1596ACSW	LTC1596AISW
LTC1595BCN8	LTC1595BIN8	LTC1596BCN	LTC1596BIN
LTC1595BCS8	LTC1595BIS8	LTC1596BCSW	LTC1596BISW
LTC1595CCN8	LTC1595CIN8	LTC1596CCN	LTC1596CIN
LTC1595CCS8	LTC1595CIS8	LTC1596CCSW	LTC1596CISW
S8 PART MARKING		LTC1596-1ACN	LTC1596-1AIN
1595A	1595AI	LTC1596-1ACSW	LTC1596-1AISW
1595B	1595BI	LTC1596-1BCN	LTC1596-1BIN
1595C	1595CI	LTC1596-1BCSW	LTC1596-1BISW
		LTC1596-1CCN	LTC1596-1CIN
		LTC1596-1CCSW	LTC1596-1CISW

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

$V_{DD} = 5V \pm 10\%$, $V_{REF} = 10V$, $V_{OUT1} = V_{OUT2} = AGND = 0V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LTC1595A/96A/96-1A			LTC1595B/96B/96-1B			LTC1595C/96C/96-1C			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
Accuracy													
	Resolution		●	16			16			16			Bits
	Monotonicity		●	16			16			15			Bits
INL	Integral Nonlinearity	(Note 2) T _A = 25°C T _{MIN} to T _{MAX}	●	±0.25 ±1			±2			±4			LSB
				±0.35 ±1			±2			±4			LSB

ELECTRICAL CHARACTERISTICS

$V_{DD} = 5V \pm 10\%$, $V_{REF} = 10V$, $V_{OUT1} = V_{OUT2} = AGND = 0V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1595A/96A/96-1A			LTC1595B/96B/96-1B			LTC1595C/96C/96-1C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DNL	Differential Nonlinearity	$T_A = 25^\circ C$ T_{MIN} to T_{MAX}	●		± 0.2	± 1			± 1			± 2	LSB
					± 0.2	± 1			± 1			± 2	LSB
GE	Gain Error	(Note 3) $T_A = 25^\circ C$ T_{MIN} to T_{MAX}	●		2	± 16			± 16			± 32	LSB
					3	± 16			± 32			± 32	LSB

$V_{DD} = 5V \pm 10\%$, $V_{REF} = 10V$, $V_{OUT1} = V_{OUT2} = AGND = 0V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Gain Temperature Coefficient	(Note 4) $\Delta \text{Gain}/\Delta \text{Temperature}$	●		1	2	ppm/ $^\circ C$
$I_{LEAKAGE}$	OUT1 Leakage Current	(Note 5) $T_A = 25^\circ C$ T_{MIN} to T_{MAX}	●			± 3	nA
						± 15	nA
	Zero-Scale Error	$T_A = 25^\circ C$ T_{MIN} to T_{MAX}	●			± 0.2	LSB
						± 1	LSB
PSRR	Power Supply Rejection	$V_{DD} = 5V \pm 10\%$	●		± 1	± 2	LSB/V

Reference Input

R_{REF}	V_{REF} Input Resistance	(Note 6)	●	5	7	10	k Ω
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AC Performance

	Output Current Settling Time	(Notes 7, 8)			1		μs
	Mid-Scale Glitch Impulse	Using LT1122 Op Amp, $C_{FEEDBACK} = 33pF$			1		nV-s
	Digital-to-Analog Glitch Impulse	Full-Scale Transition, $V_{REF} = 0V$, Using LT1122 Op Amp, $C_{FEEDBACK} = 33pF$			2		nV-s
	Multiplying Feedthrough Error	$V_{REF} = \pm 10V$, 10kHz Sine Wave			1		mV _{P-P}
THD	Total Harmonic Distortion	(Note 9)			108		dB
	Equivalent DAC Thermal Noise Voltage Density	(Note 10) $f = 1kHz$			11		nV/ $\sqrt{Hz}$

Analog Outputs (Note 4)

C_{OUT}	Output Capacitance (Note 4)	DAC Register Loaded to All 1s C_{OUT1}	●		115	130	pF
		DAC Register Loaded to All 0s C_{OUT1}	●		70	80	pF

Digital Inputs

V_{IH}	Digital Input High Voltage		●	2.4			V
V_{IL}	Digital Input Low Voltage		●			0.8	V
I_{IN}	Digital Input Current		●		0.001	± 1	μA
C_{IN}	Digital Input Capacitance	(Note 4) $V_{IN} = 0V$	●			8	pF

Digital Outputs: SRO (LTC1596/LTC1596-1)

V_{OH}	Digital Output High Voltage	$I_{OH} = 200\mu A$	●	4			V
V_{OL}	Digital Output Low Voltage	$I_{OL} = 1.6mA$	●			0.4	V

$V_{DD} = 5V \pm 10\%$, $V_{REF} = 10V$, $V_{OUT1} = GND = 0V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Timing Characteristics (LTC1595)							
t_{DS}	Serial Input to CLK Setup Time		●	30	5		ns
t_{DH}	Serial Input to CLK Hold Time		●	30	5		ns

ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{SRI}	Serial Input Data Pulse Width		60			ns
t_{CH}	Clock Pulse Width High		60			ns
t_{CL}	Clock Pulse Width Low		60			ns
t_{LD}	Load Pulse Width		60			ns
t_{ASB}	LSB Clocked into Input Register to DAC Register Load Time		0			ns

$V_{DD} = 5V \pm 10\%$, $V_{REF} = 10V$, $V_{OUT1} = V_{OUT2} = AGND = 0V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Timing Characteristics (LTC1596/LTC1596-1)						
t_{DS1}	Serial Input to Strobe Setup Time	STB1 Used as the Strobe	30	5		ns
t_{DS2}		STB2 Used as the Strobe	20	-5		ns
t_{DS3}		STB3 Used as the Strobe	25	0		ns
t_{DS4}		STB4 Used as the Strobe	20	-5		ns
t_{DH1}	Serial Input to Strobe Hold Time	STB1 Used as the Strobe	30	5		ns
t_{DH2}		STB2 Used as the Strobe	40	15		ns
t_{DH3}		STB3 Used as the Strobe	35	10		ns
t_{DH4}		STB4 Used as the Strobe	40	15		ns
t_{SRI}	Serial Input Data Pulse Width		60			ns
t_{STB1} to t_{STB4}	Strobe Pulse Width	(Note 11)	60			ns
t_{STB1} to t_{STB4}	Strobe Pulse Width	(Note 12)	60			ns
t_{LD1} , t_{LD2}	LD Pulse Width		60			ns
t_{ASB}	LSB Strobed into Input Register to Load DAC Register Time		0			ns
t_{CLR}	Clear Pulse Width		100			ns
t_{PD1}	STB1 to SRO Propagation Delay	$C_L = 50pF$	30		150	ns
t_{PD}	STB2, STB3, STB4 to SRO Propagation Delay	$C_L = 50pF$	30		200	ns

Power Supply

V_{DD}	Supply Voltage		4.5	5	5.5	V
I_{DD}	Supply Current	Digital Inputs = 0V or V_{DD}		1.5	10	μA

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: $\pm 1LSB = \pm 0.0015\%$ of full scale = $\pm 15.3ppm$ of full scale.

Note 3: Using internal feedback resistor.

Note 4: Guaranteed by design, not subject to test.

Note 5: I_{OUT1} with DAC register loaded with all 0s.

Note 6: Typical temperature coefficient is 100ppm/C.

Note 7: OUT1 load = 100 Ω in parallel with 13pF.

Note 8: To 0.0015% for a full-scale change, measured from the falling edge of LD1, LD2 or LD.

Note 9: $V_{REF} = 6V_{RMS}$ at 1kHz. DAC register loaded with all 1s; op amp = LT1007.

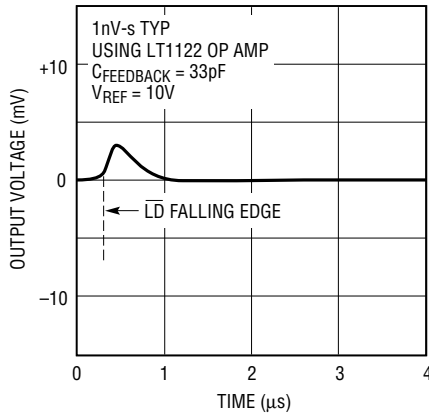
Note 10: Calculation from $e_n = \sqrt{4kTRB}$ where: k = Boltzmann constant (J/°K); R = resistance (Ω); T = temperature (°K); B = bandwidth (Hz).

Note 11: Minimum high time for STB1, STB2, STB4. Minimum low time for STB3.

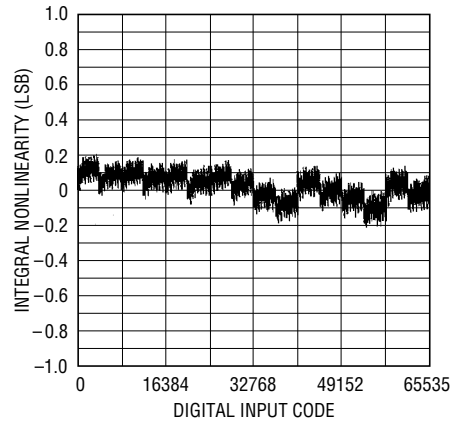
Note 12: Minimum low time for STB1, STB2, STB4. Minimum high time for STB3.

TYPICAL PERFORMANCE CHARACTERISTICS

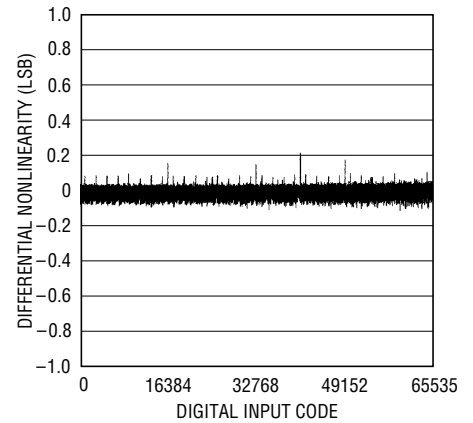
Mid-Scale Glitch Impulse



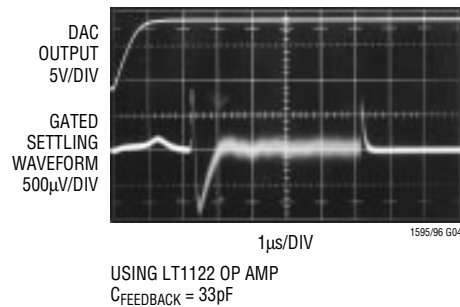
Integral Nonlinearity (INL)



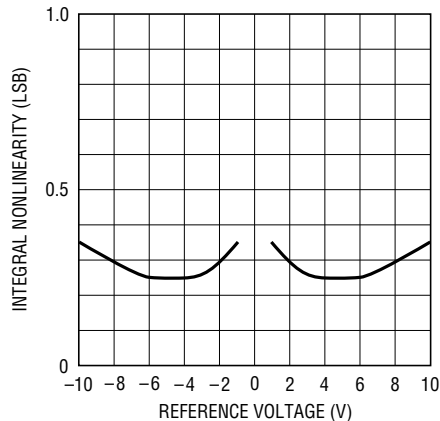
Differential Nonlinearity (DNL)



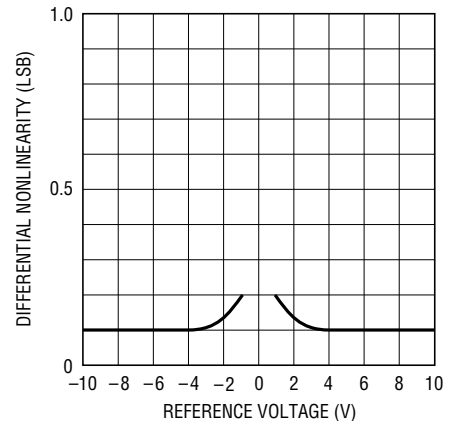
Full-Scale Settling Waveform



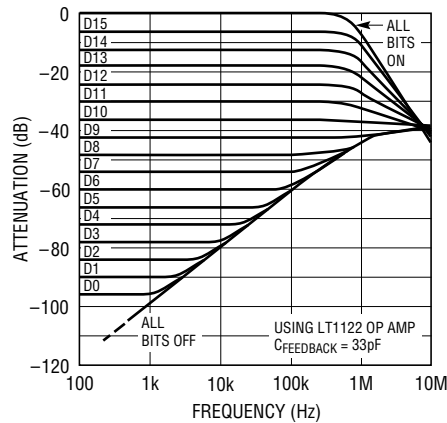
Integral Nonlinearity vs Reference Voltage



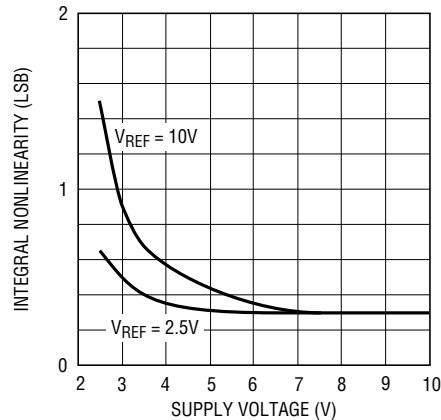
Differential Nonlinearity vs Reference Voltage



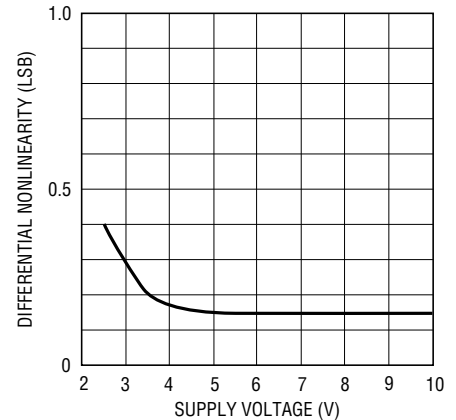
Multiplying Mode Frequency Response vs Digital Code



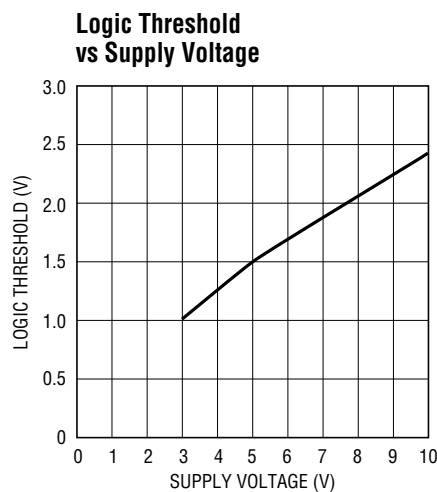
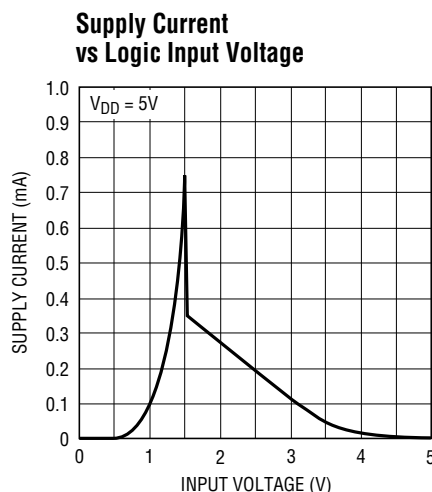
Integral Nonlinearity vs Supply Voltage



Differential Nonlinearity vs Supply Voltage



TYPICAL PERFORMANCE CHARACTERISTICS



PIN FUNCTIONS

LTC1595

V_{REF} (Pin 1): Reference Input.

R_{FB} (Pin 2): Feedback Resistor. Normally tied to the output of the current to voltage converter op amp.

OUT1 (Pin 3): Current Output Pin. Tie to inverting input of current to voltage converter op amp.

GND (Pin 4): Ground Pin.

LD (Pin 5): The Serial Interface Load Control Input. When LD is pulled low, data is loaded from the shift register into the DAC register, updating the DAC output.

SRI (Pin 6): The Serial Data Input. Data on the SRI pin is latched into the shift register on the rising edge of the serial clock. Data is loaded MSB first.

CLK (Pin 7): The Serial Interface Clock Input.

V_{DD} (Pin 8): The Positive Supply Input. $4.5V \leq V_{DD} \leq 5.5V$. Requires a bypass capacitor to ground.

LTC1596/LTC1596-1

OUT1 (Pin 1): True Current Output Pin. Tie to inverting input of current to voltage converter op amp.

OUT2 (Pin 2): Complement Current Output Pin. Tie to analog ground.

AGND (Pin 3): Analog Ground Pin.

STB1, STB2, STB3, STB4 (Pins 4, 8, 10, 11): Serial Interface Clock Inputs. STB1, STB2 and STB4 are rising edge triggered inputs. STB3 is a falling edge triggered input (see Truth Tables).

LD1, LD2 (Pins 5, 9): Serial Interface Load Control Inputs. When LD1 and LD2 are pulled low, data is loaded from the shift register into the DAC register, updating the DAC output (see Truth Tables).

SRO (Pin 6): The Output of the Shift Register. Becomes valid on the active edge of the serial clock.

SRI (Pin 7): The Serial Data Input. Data on the SRI pin is latched into the shift register on the active edge of the serial clock. Data is loaded MSB first.

DGND (Pin 12): Digital Ground Pin.

CLR (Pin 13): The Clear Pin for the DAC. Clears DAC to zero scale when pulled low on LTC1596. Clears DAC to midscale when pulled low on LTC1596-1. This pin should be tied to V_{DD} for normal operation.

V_{DD} (Pin 14): The Positive Supply Input. $4.5V \leq V_{DD} \leq 5.5V$. Requires a bypass capacitor to ground.

V_{REF} (Pin 15): Reference Input.

R_{FB} (Pin 16): Feedback Resistor. Normally tied to the output of the current to voltage converter op amp.

TRUTH TABLES

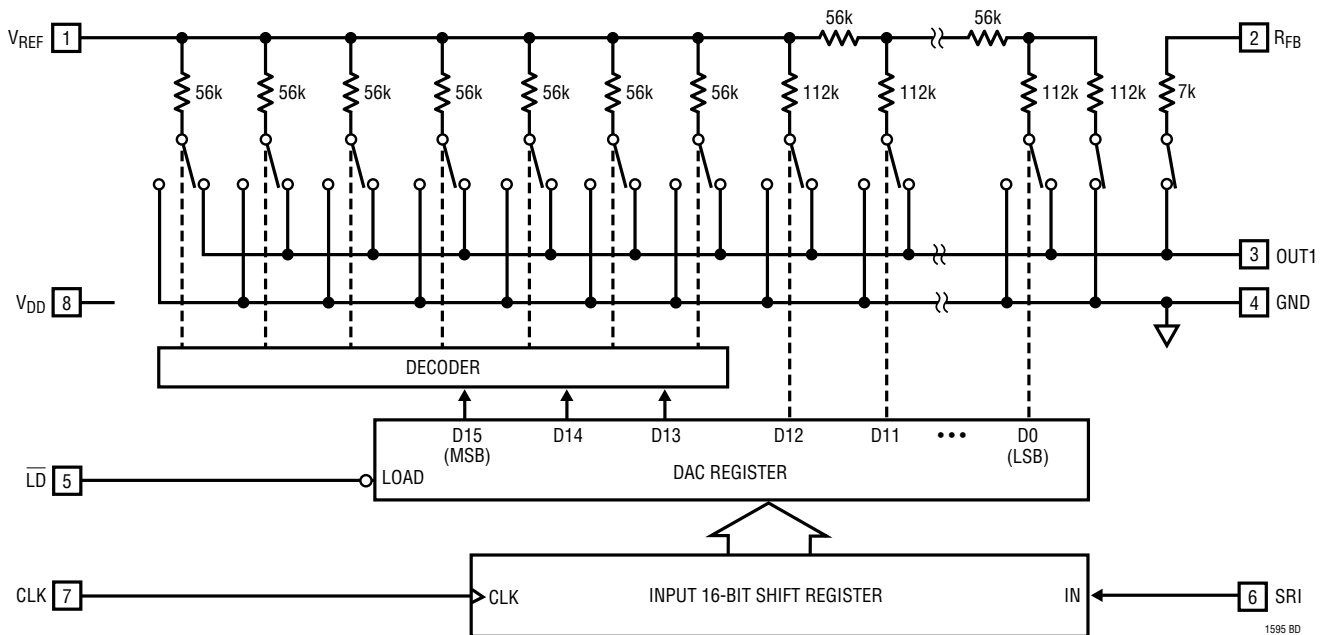
Table 1. LTC1596/LTC1596-1 Input Register

CONTROL INPUTS				Input Register and SRO Operation
STB1	STB2	STB3	STB4	
$\overline{\uparrow}$	0	1	0	Serial Data Bit on SRI Loaded into Input Register, MSB First
0	$\overline{\uparrow}$	1	0	Data Bit or SRI Appears on SRO Pin After 16 Clocked Bits
0	0	$\overline{\uparrow}$	0	
0	0	1	$\overline{\uparrow}$	
1	X	X	X	No Input Register Operation
X	1	X	X	No SRO Operation
X	X	0	X	
X	X	X	1	

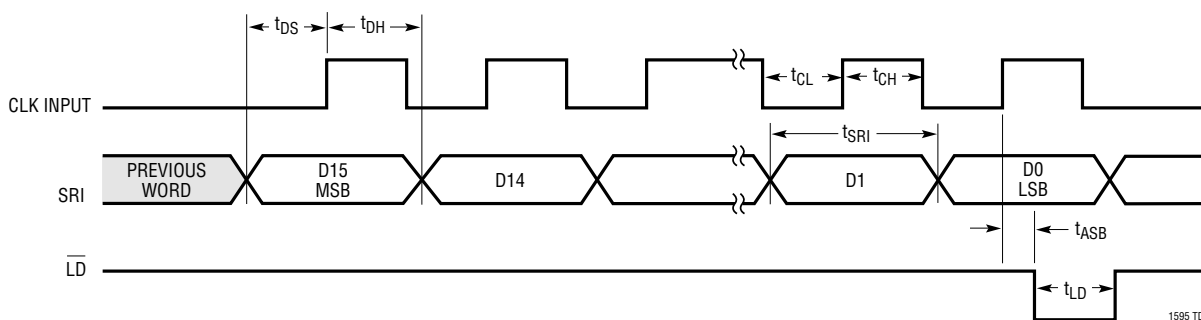
Table 2. LTC1596/LTC1596-1 DAC Register

CONTROL INPUTS			DAC Register Operation
CLR	$\overline{\text{LD1}}$	$\overline{\text{LD2}}$	
0	X	X	Reset DAC Register and Input Register to All 0s (LTC1596) or to Midscale (LTC1596-1) (Asynchronous Operation)
1	1	X	No DAC Register Operation
1	X	1	No DAC Register Operation
1	0	0	Load DAC Register with the Contents of Input Register

BLOCK DIAGRAM (LTC1595)



TIMING DIAGRAM (LTC1595)



BLOCK DIAGRAM (LTC1596/LTC1596-1)



APPLICATIONS INFORMATION

Description

The LTC1595/LTC1596 are 16-bit multiplying DACs which have serial inputs and current outputs. They use precision R/2R technology to provide exceptional linearity and stability. The devices operate from a single 5V supply and provide $\pm 10V$ reference input and voltage output ranges when used with an external op amp. These devices have a proprietary deglitcher that reduces glitch impulse to 1nV-s over a 0V to 10V output range.

Serial I/O

The LTC1595/LTC1596 have SPI/MICROWIRE compatible serial ports that accept 16-bit serial words. Data is accepted MSB first and loaded with a load pin.

The 8-pin LTC1595 has a 3-wire interface. Data is shifted into the SRI data input on the rising edge of the CLK pin. At the end of the data transfer, data is loaded into the DAC register by pulling the LD pin low (see LTC1595 Timing Diagram).

The 16-pin LTC1596 can operate in identical fashion to the LTC1595 but offers additional pins for flexibility. Four clock pins are available STB1, STB2, STB3 and STB4. STB1, STB2 and STB4 operate like the CLK pin of the LTC1595, capturing data on their rising edges. STB3 captures data on its falling edge (see Truth Table 1).

The LTC1596 has two load pins, $\overline{LD1}$ and $\overline{LD2}$. To load data, both pins must be taken low. If one of the pins is grounded, the other pin will operate identically to LTC1595's $\overline{LD}$ pin. An asynchronous clear input ($\overline{CLR}$) resets the LTC1596 to zero scale (and the LTC1596-1 to midscale) when pulled low (see Truth Table 2).

The LTC1596 also has a data output pin SRO that can be connected to the SRI input of another DAC to daisy-chain multiple DACs on one 3-wire interface (see LTC1596 Timing Diagram).

Unipolar (2-Quadrant Multiplying) Mode ($V_{OUT} = 0V$ to $-V_{REF}$)

The LTC1595/LTC1596 can be used with a single op amp to provide 2-quadrant multiplying operation as shown in Figure 1. With a fixed $-10V$ reference, the circuits shown give a precision unipolar 0V to 10V output swing.

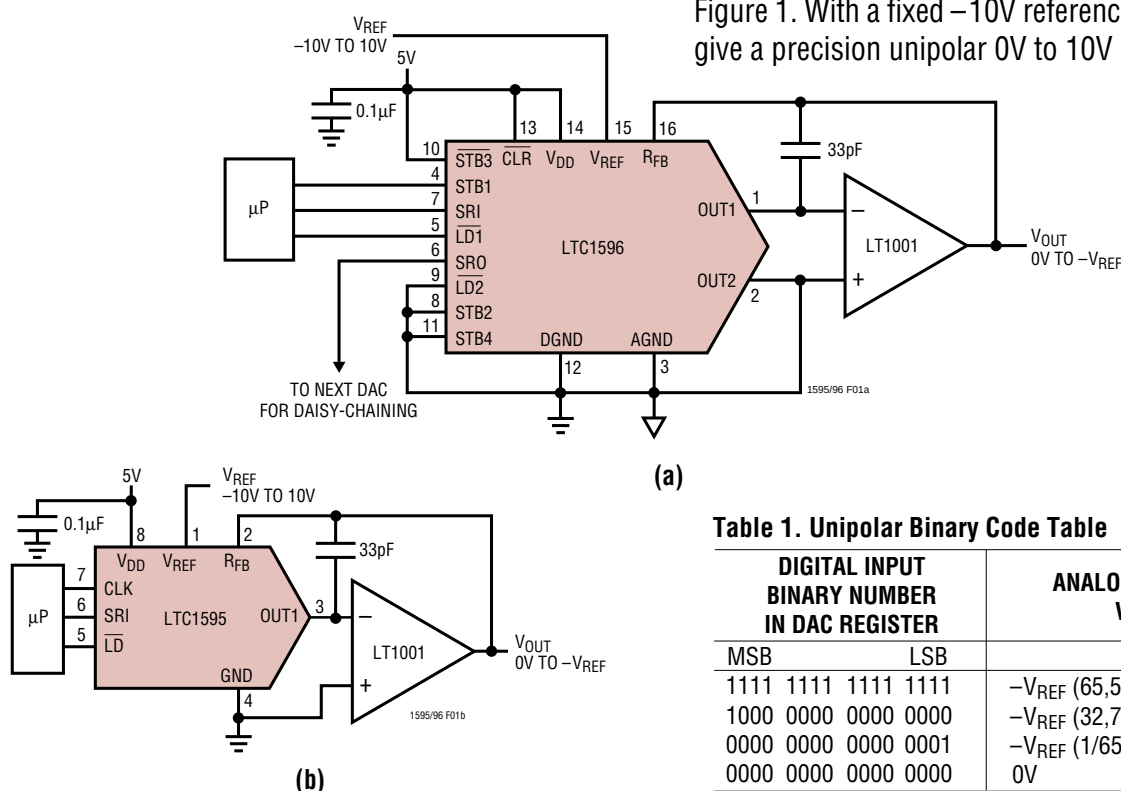


Table 1. Unipolar Binary Code Table

DIGITAL INPUT BINARY NUMBER IN DAC REGISTER		ANALOG OUTPUT V_{OUT}
MSB	LSB	
1111	1111	$-V_{REF}$ (65,535/65,536)
1000	0000	$-V_{REF}$ (32,768/65,536) = $-V_{REF}/2$
0000	0000	$-V_{REF}$ (1/65,536)
0000	0000	0V

Figure 1. Unipolar Operation (2-Quadrant Multiplication) $V_{OUT} = 0V$ to $-V_{REF}$

APPLICATIONS INFORMATION

Bipolar (4-Quadrant Multiplying) Mode ($V_{OUT} = -V_{REF}$ to V_{REF})

The LTC1595/LTC1596 can be used with a dual op amp and three external resistors to provide 4-quadrant multiplying operation as shown in Figure 2 (last page). With a fixed 10V reference, the circuits shown give a precision bipolar $-10V$ to $10V$ output swing. Using the LTC1596-1 will cause the power-on reset and clear pin to reset the DAC to midscale (bipolar zero).

Op Amp Selection

Because of the extremely high accuracy of the 16-bit LTC1595/LTC1596, thought should be given to op amp selection in order to achieve the exceptional performance of which the part is capable. Fortunately, the sensitivity of INL and DNL to op amp offset has been greatly reduced compared to previous generations of multiplying DACs.

Op amp offset will contribute mostly to output offset and gain and will have minimal effect on INL and DNL. For example, a $500\mu V$ op amp offset will cause about 0.55LSB

INL degradation and 0.15LSB DNL degradation with a 10V full-scale range. The main effects of op amp offset will be a degradation of zero-scale error equal to the op amp offset, and a degradation of full-scale error equal to twice the op amp offset. For example, the same $500\mu V$ op amp offset will cause a 3.3LSB zero-scale error and a 6.5LSB full-scale error with a 10V full-scale range.

Op amp input bias current (I_{BIAS}) contributes only a zero-scale error equal to $I_{BIAS}(R_{FB}) = I_{BIAS}(R_{REF}) = I_{BIAS}(7k)$. Table 2 shows a selection of LTC op amps which are suitable for use with the LTC1595/LTC1596. For a thorough discussion of 16-bit DAC settling time and op amp selection, refer to Application Note 74, "Component and Measurement Advances Ensure 16-Bit DAC Settling Time."

Grounding

As with any high resolution converter, clean grounding is important. A low impedance analog ground plane and star grounding should be used. I_{OUT2} (LTC1596) and GND (LTC1595) must be tied to the star ground with as low a resistance as possible.

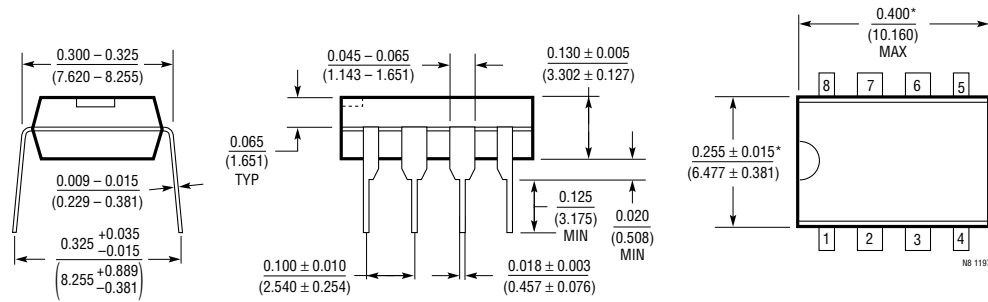
Table 2. 16-Bit Settling Time for Various Amplifiers Driven by the LT1595 DAC. LT1468 (Shaded) Offers Fastest Settling Time While Maintaining Accuracy Over Temperature

AMPLIFIER	CONSERVATIVE SETTling TIME AND COMPENSATION VALUE		COMMENTS
LT1001	120 μs	100pF	Good Low Speed Choice
LT1007	19 μs	100pF	I_B Gives ≈ 1 LSB Error at 25°C
LT1013	75 μs	150pF	≈ 1 LSB Error Due to V_{OS} over Temperature
LT1077	200 μs	100pF	
LT1097	120 μs	75pF	Good Low Speed Choice
LT1112	120 μs	100pF	Good Low Speed Choice Dual
LT1178	450 μs	100pF	Low Power Dual
LT1468	2.5 μs	30pF	Fastest Settling with 16-Bit Performance

PACKAGE DESCRIPTION

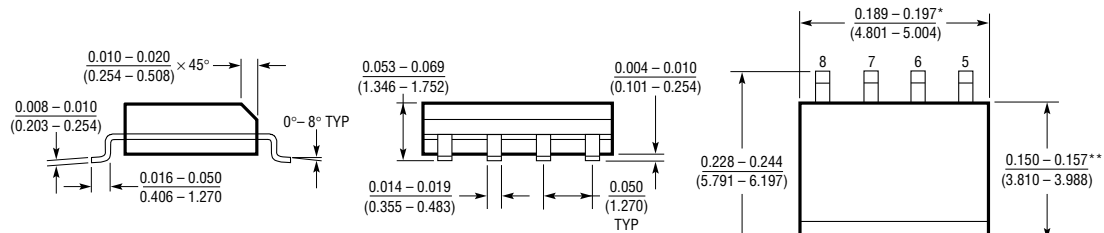
Dimensions in inches (millimeters) unless otherwise noted.

N8 Package 8-Lead PDIP (Narrow 0.300) (LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

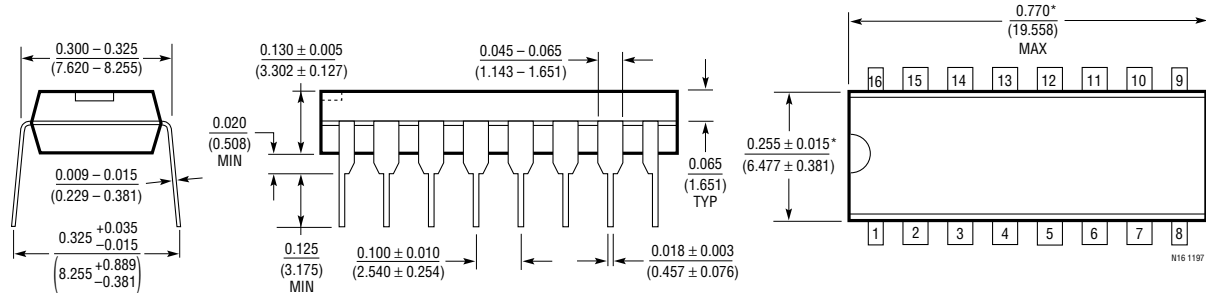
S8 Package 8-Lead Plastic Small Outline (Narrow 0.150) (LTC DWG # 05-08-1610)



DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006 (0.152mm) PER SIDE

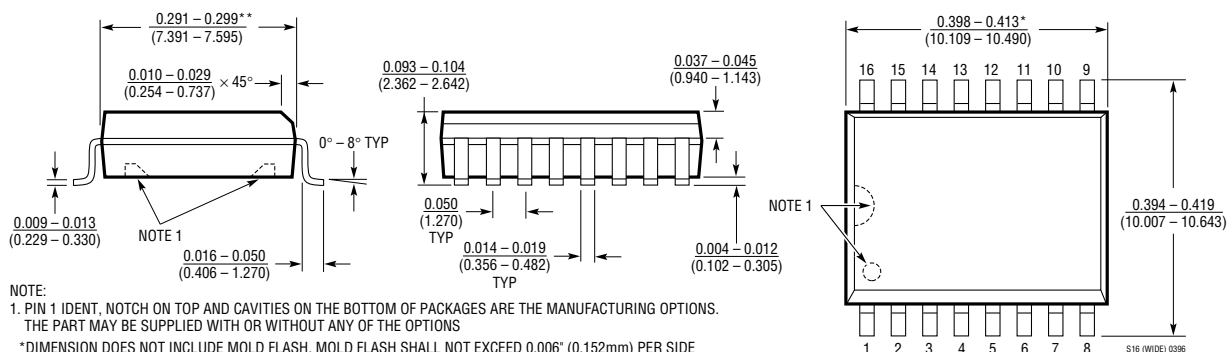
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010* (0.254mm) PER SIDE

N Package 16-Lead PDIP (Narrow 0.300) (LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

SW Package 16-Lead Plastic Small Outline (Wide 0.300) (LTC DWG # 05-08-1620)



NOTE:

1. PIN 1 IDENT. NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS

DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006 (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010* (0.254mm) PER SIDE

TYPICAL APPLICATIONS

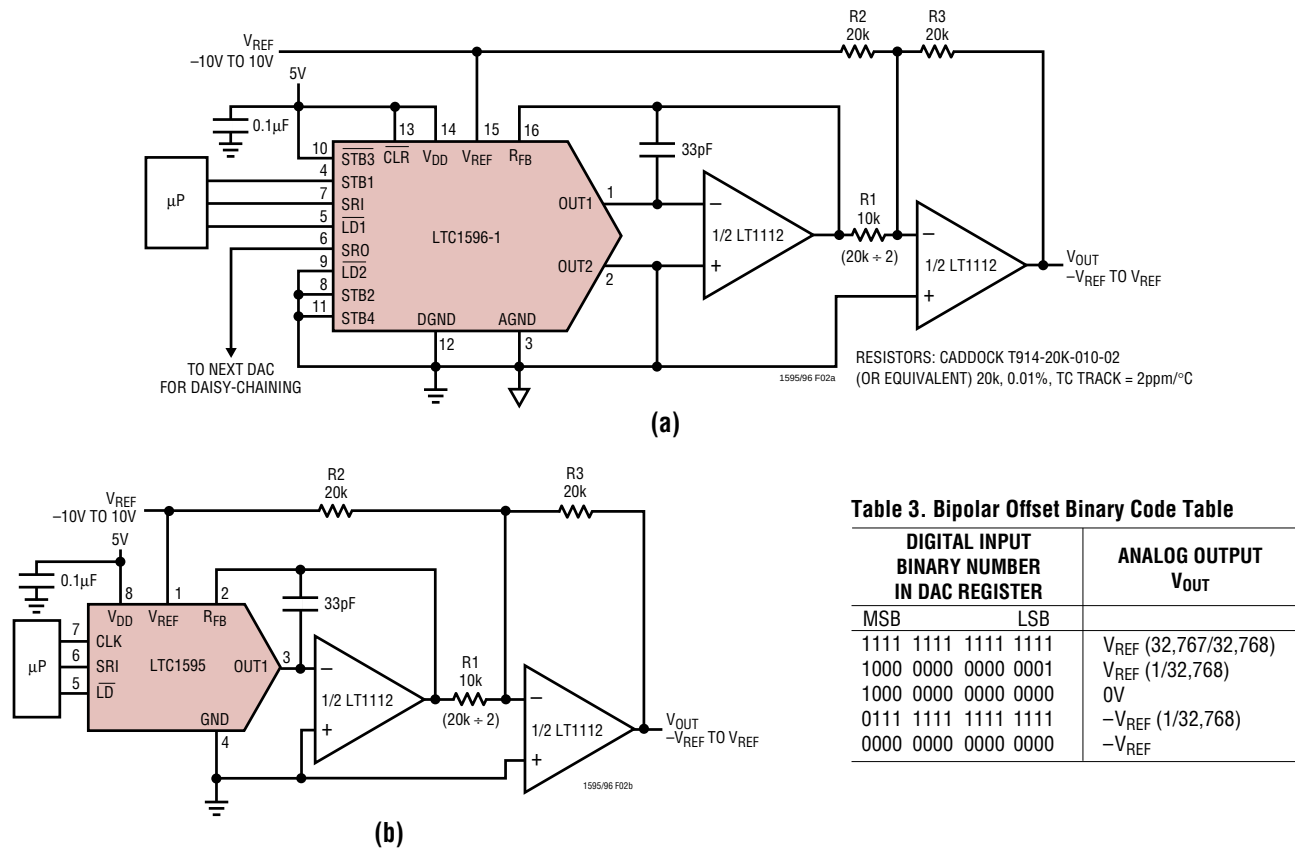


Figure 2. Bipolar Operation (4-Quadrant Multiplication) V_{OUT} = -V_{REF} to V_{REF}

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
DACs		
LTC1590	Dual Serial I/O Multiplying I _{OUT} 12-Bit DAC	16-Pin SO and PDIP, SPI Interface
LTC1597	Parallel 16-Bit Current Output DAC	Low Glitch, ±1LSB Maximum INL, DNL
LTC1650	Serial 16-Bit Voltage Output DAC	Low Noise and Glitch Rail-to-Rail V _{OUT}
LTC1658	Serial 14-Bit Voltage Output DAC	Low Power, 8-Lead MSOP Rail-to-Rail V _{OUT}
LTC7543/LTC8143/LTC8043	Serial I/O Multiplying I _{OUT} 12-Bit DACs	Clear Pin and Serial Data Output (LTC8143)
ADCs		
LTC1418	14-Bit, 200ksps 5V Sampling ADC	16mW Dissipation, Serial and Parallel Outputs
LTC1604	16-Bit, 333ksps Sampling ADC	±2.5V Input, SINAD = 90dB, THD = 100dB
LTC1605	Single 5V, 16-Bit 100ksps ADC	Low Power, ±10V Inputs
LTC2400	24-Bit, ΔΣ ADC in SO-8	1ppm (4ppm) Offset (Full Scale), Internal 50Hz/60Hz Notches
Op Amps		
LT1001	Precision Operational Amplifier	Low Offset, Low Drift
LT1112	Dual Low Power, Precision Picoamp Input Op Amp	Low Offset, Low Drift
LT1468	90MHz, 22V/μs, 16-Bit Accurate Op Amp	Precise, 1μs Settling to 0.0015%
References		
LT1236	Precision Reference	Ultralow Drift, 5ppm/°C, High Accuracy 0.05%
LT1634	Micropower Reference	Ultralow Drift, 10ppm/°C, High Accuracy 0.05%