

IR2131

3 HIGH SIDE AND 3 LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
Fully operational to +600V
Tolerant to negative transient voltage
dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for all channels
- Over-current shutdown turns off all six drivers
- Independent 3 high side & 3 low side drivers
- Matched propagation delay for all channels
- Outputs out of phase with inputs

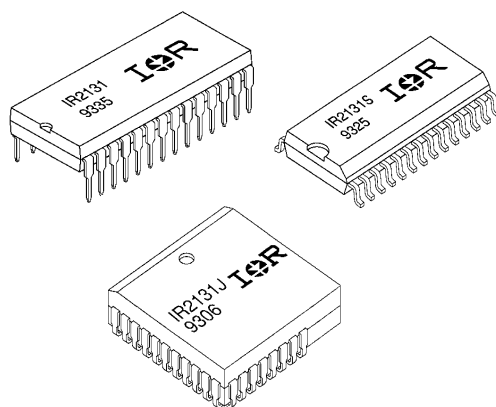
Description

The IR2131 is a high voltage, high speed power MOSFET and IGBT driver with three independent high and low side referenced output channels. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with 5V CMOS or LSTTL outputs. A current trip function which terminates all six outputs can be derived from an external current sense resistor. A shutdown input is provided for a customized shutdown function. An open drain FAULT signal is provided to indicate that any of the shutdowns has occurred. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channels can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operate up to 600 volts.

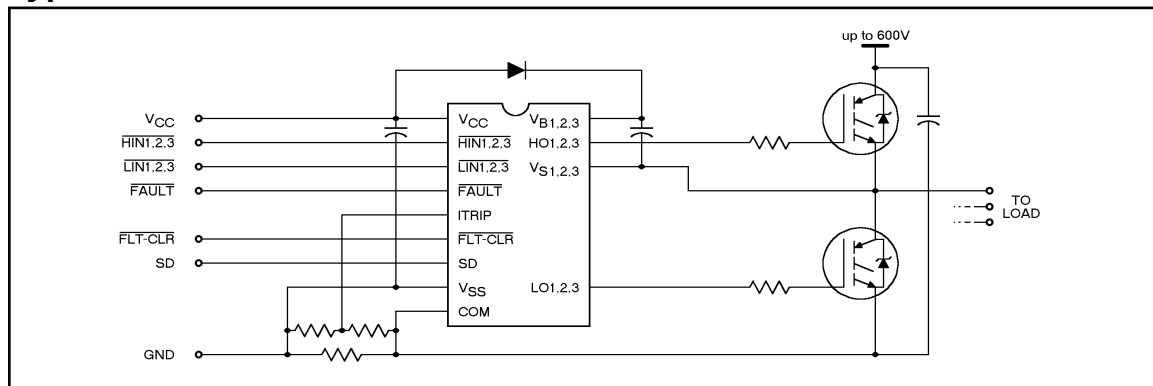
Product Summary

V_{OFFSET}	600V max.
$I_{\text{O+/-}}$	200 mA / 420 mA
V_{OUT}	10 - 20V
$t_{\text{on/off (typ.)}}$	1.3 & 0.6 μs
Deadtime (typ.)	700 ns

Packages



Typical Connection



Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions. Additional Information is shown in Figures 7 through 10.

Symbol	Parameter Definition	Value		Units
		Min.	Max.	
$V_{B1,2,3}$	High Side Floating Supply Voltage	-0.3	525	V
$V_{S1,2,3}$	High Side Floating Offset Voltage	$V_{B1,2,3} - 25$	$V_{B1,2,3} + 0.3$	
$V_{HO1,2,3}$	High Side Floating Output Voltage	$V_{S1,2,3} - 0.3$	$V_{B1,2,3} + 0.3$	
V_{CC}	Low Side and Logic Fixed Supply Voltage	-0.3	25	
V_{SS}	Logic Ground	$V_{CC} - 25$	$V_{CC} + 0.3$	
$V_{LO1,2,3}$	Low Side Output Voltage	-0.3	$V_{CC} + 0.3$	
V_{IN}	Logic Input Voltage ($HIN1,2,3$, $LIN1,2,3$, $FLT - CLR$, SD & $ITRIP$)	$V_{SS} - 0.3$	$V_{CC} + 0.3$	
V_{FLT}	FAULT Output Voltage	$V_{SS} - 0.3$	$V_{CC} + 0.3$	
dV_S/dt	Allowable Offset Supply Voltage Transient	—	50	V/ns
P_D	Package Power Dissipation @ $T_A \leq +25^\circ\text{C}$ (28 Lead DIP)	—	1.5	W
	(28 Lead SOIC)	—	1.6	
	(44 Lead PLCC)	—	2.0	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (28 Lead DIP)	—	83	$^\circ\text{C/W}$
	(28 Lead SOIC)	—	78	
	(44 Lead PLCC)	—	63	
T_J	Junction Temperature	—	150	$^\circ\text{C}$
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Parameter Definition	Value		Units
		Min.	Max.	
$V_{B1,2,3}$	High Side Floating Supply Voltage	$V_{S1,2,3} + 10$	$V_{S1,2,3} + 20$	V
$V_{S1,2,3}$	High Side Floating Offset Voltage	Note 1	600	
$V_{HO1,2,3}$	High Side Floating Output Voltage	$V_{S1,2,3}$	$V_{B1,2,3}$	
V_{CC}	Low Side and Logic Fixed Supply Voltage	10	20	
V_{SS}	Logic Ground	-5	5	
$V_{LO1,2,3}$	Low Side Output Voltage	0	V_{CC}	
V_{IN}	Logic Input Voltage ($HIN1,2,3$, $LIN1,2,3$, $FLT - CLR$, SD & $ITRIP$)	V_{SS}	$V_{SS} + 5$	
V_{FLT}	FAULT Output Voltage	V_{SS}	V_{CC}	
T_A	Ambient Temperature	-40	125	$^\circ\text{C}$

Note 1: Logic operational for V_S of -5V to +600V. Logic state held for V_S of -5V to $-V_{BS}$.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC} , $V_{BS1,2,3}$) = 15V, $V_{S1,2,3}$ = V_{SS} = COM, C_L = 1000 pF and T_A = 25°C unless otherwise specified. The dynamic electrical characteristics are defined in Figures 4 through 5.

Symbol	Parameter Definition	Value			Units	Test Conditions
		Min.	Typ.	Max.		
t_{on}	Turn-On Propagation Delay	0.6	1.3	2.0	μs	$V_{IN} = 0$ & 5V $V_{S1,2,3} = 0$ to 600V
t_{off}	Turn-Off Propagation Delay	0.2	0.6	1.0		
t_r	Turn-On Rise Time	—	80	150		
t_f	Turn-Off Fall Time	—	40	100		
t_{itrip}	ITRIP to Output Shutdown Propagation Delay	400	700	1000	ns	V_{IN} , $V_{ITRIP} = 0$ & 5V
t_{bl}	ITRIP Blanking Time	—	400	—		$V_{ITRIP} = 1V$
t_{flt}	ITRIP to FAULT Indication Delay	400	700	1000		V_{IN} , $V_{ITRIP} = 0$ & 5V
$t_{flt,in}$	Input Filter Time (All Six Inputs)	—	310	—		$V_{IN} = 0$ & 5V
t_{fltclr}	FLT-CLR to FAULT Clear Time	400	700	1000		V_{IN} , V_{IT} , $V_{FC} = 0$ & 5V
t_{sd}	SD to Output Shutdown Propagation Delay	400	700	1000		V_{IN} , $V_{SD} = 0$ & 5V
DT	Deadtime	400	700	1200		$V_{IN} = 0$ & 5V

Static Electrical Characteristics

V_{BIAS} (V_{CC} , $V_{BS1,2,3}$) = 15V, $V_{S1,2,3}$ = V_{SS} = COM and T_A = 25°C unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six logic input leads: $HIN1,2,3$ & $LIN1,2,3$. The V_O and I_O parameters are referenced to COM and $V_{S1,2,3}$ and are applicable to the respective output leads: $HO1,2,3$ or $LO1,2,3$.

Symbol	Parameter Definition	Value			Units	Test Conditions
		Min.	Typ.	Max.		
V_{IH}	Logic "0" Input Voltage (OUT = LO)	2.2	—	—	V	
V_{IL}	Logic "1" Input Voltage (OUT = HI)	—	—	0.8		
$V_{FCLR,IH}$	Logic "0" Fault Clear Input Voltage	2.2	—	—		
$V_{FCLR,IL}$	Logic "1" Fault Clear Input Voltage	—	—	0.8		
$V_{SD,TH+}$	Shutdown Input Positive Going Threshold	1.2	1.8	2.1		
$V_{SD,TH-}$	Shutdown Input Negative Going Threshold	0.9	1.5	1.8	mV	
$V_{IT,TH+}$	ITRIP Input Positive Going Threshold	250	485	600		
$V_{IT,TH-}$	ITRIP Input Negative Going Threshold	200	400	550		
V_{OH}	High Level Output Voltage, $V_{BIAS} - V_O$	—	—	100		$V_{IN} = 0V$, $I_O = 0A$
V_{OL}	Low Level Output Voltage, V_O	—	—	100		$V_{IN} = 5V$, $I_O = 0A$
I_{LK}	Offset Supply Leakage Current	—	—	50	μA	$V_B = V_S = 600V$
I_{OBS}	Quiescent V_{BS} Supply Current	—	30	100	mA	$V_{IN} = 0V$ or 5V
I_{OCC}	Quiescent V_{CC} Supply Current	—	3.0	4.5		$V_{IN} = 0V$ or 5V
I_{IN+}	Logic "1" Input Bias Current (OUT = HI)	—	190	300	μA	$V_{IN} = 0V$
I_{IN-}	Logic "0" Input Bias Current (OUT = LO)	—	50	100		$V_{IN} = 5V$
I_{ITRIP+}	"High" ITRIP Bias Current	—	75	150		ITRIP = 5V
I_{ITRIP-}	"Low" ITRIP Bias Current	—	—	100	nA	ITRIP = 0V
I_{FCLR+}	Logic "1" Fault Clear Bias Current	—	125	250	μA	FLT-CLR = 0V
I_{FCLR-}	Logic "0" Fault Clear Bias Current	—	75	150		FLT-CLR = 5V
I_{SD+}	Logic "1" Shutdown Bias Current	—	75	150		SD = 5V
I_{SD-}	Logic "0" Shutdown Bias Current	—	—	100	nA	SD = 0V

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Static Electrical Characteristics -- Continued

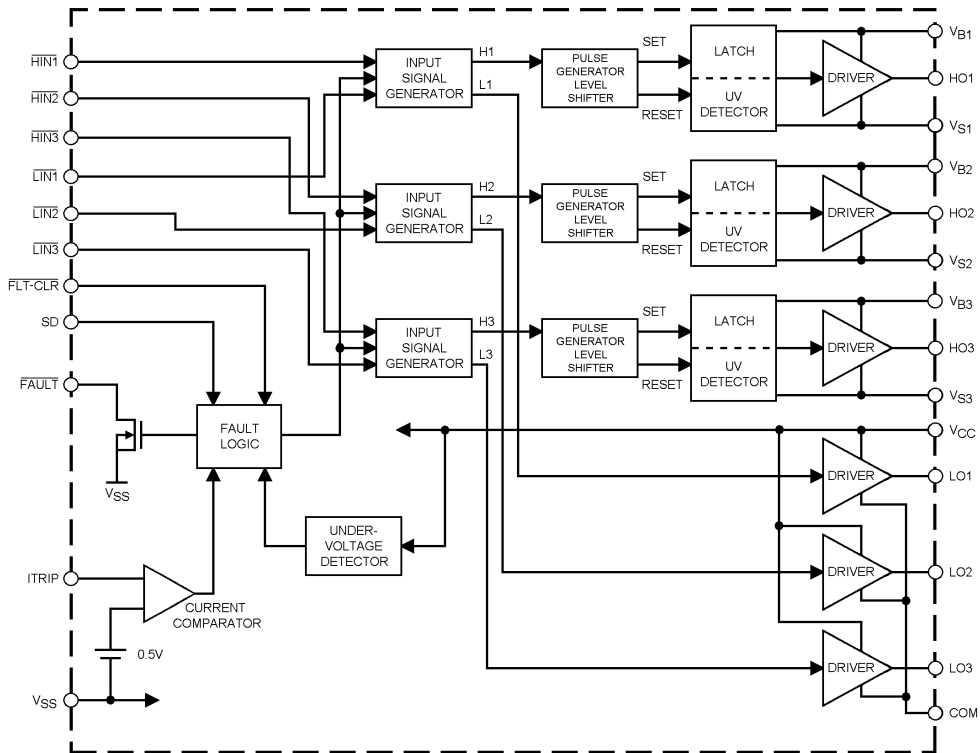
V_{BIAS} (V_{CC}, V_{BS1,2,3}) = 15V, V_{S1,2,3} = V_{SS} = COM and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six logic input leads: HIN1,2,3 & LIN1,2,3. The V_O and I_O parameters are referenced to COM and V_{S1,2,3} and are applicable to the respective output leads: HO1,2,3 or LO1,2,3.

Symbol	Parameter Definition	Value			Units	Test Conditions
		Min.	Typ.	Max.		
V _{BSUV+}	V _{BS} Supply Undervoltage Positive Going Threshold	8.2	8.7	9.2	V	
V _{BSUV-}	V _{BS} Supply Undervoltage Negative Going Threshold	7.8	8.3	8.8		
V _{CCUV+}	V _{CC} Supply Undervoltage Positive Going Threshold	8.2	8.7	9.2		
V _{CCUV-}	V _{CC} Supply Undervoltage Negative Going Threshold	7.8	8.3	8.8		
R _{on,FLT}	$\overline{\text{FAULT}}$ Low On-Resistance	—	55	75	Ω	
I _{O+}	Output High Short Circuit Pulsed Current	200	250	—	mA	V _O = 0V, V _{IN} = 0V PW ≤ 10 μs
I _{O-}	Output Low Short Circuit Pulsed Current	420	500	—		V _O = 15V, V _{IN} = 5V PW ≤ 10 μs

Lead Assignments

1 VCC VB1 28 2 HIN1 HO1 27 3 HIN2 VS1 26 4 HIN3 VB2 24 5 LIN1 HO2 23 6 LIN2 VS2 22 7 LIN3 VS2 21 8 $\overline{\text{FAULT}}$ VB3 20 9 ITRIP HO3 19 10 $\overline{\text{FLT-CLR}}$ VS3 18 11 SD VSS 17 12 VSS LO1 16 13 COM LO2 15 14 LO3 28 Lead DIP	HIN3 6 HIN2 5 HIN1 4 VCC 3 7 LIN1 8 LIN2 9 LIN3 10 11 FAULT 12 13 ITRIP 14 15 FLT-CLR 16 17 SD 18 VSS 19 COM 20 LO3 21 LO2 22 LO1 23 24 25 37 VB2 36 HO2 35 VS2 31 VB3 30 HO3 29 VS3 44 Lead PLCC w/o 12 Leads	1 VCC VB1 28 2 HIN1 HO1 27 3 HIN2 VS1 26 4 HIN3 VB2 24 5 LIN1 HO2 23 6 LIN2 VS2 22 7 LIN3 VS2 21 8 $\overline{\text{FAULT}}$ VB3 20 9 ITRIP HO3 19 10 $\overline{\text{FLT-CLR}}$ VS3 18 11 SD VSS 17 12 VSS LO1 16 13 COM LO2 15 14 LO3 28 Lead SOIC (Wide Body)
IR2131	IR2131J	IR2131S
Part Number		

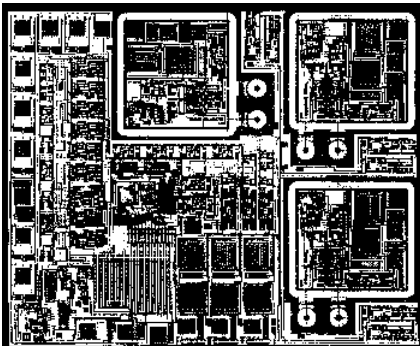
Functional Block Diagram



Lead Definitions

Lead	
Symbol	Description
HIN1,2,3	Logic inputs for high side gate driver outputs (HO1,2,3), out of phase
LIN1,2,3	Logic inputs for low side gate driver output (LO1,2,3), out of phase
FLT-CLR	Logic input for fault clear
SD	Logic input for shutdown
FAULT	Indicates over-current or undervoltage lockout (low side) has occurred, negative logic
VCC	Low side and logic fixed supply
ITRIP	Input for over-current shutdown
VSS	Logic ground
VB1,2,3	High side floating supplies
HO1,2,3	High side gate drive outputs
VS1,2,3	High side floating supply returns
LO1,2,3	Low side gate drive outputs
COM	Low side return

Device Information

Process & Design Rule		HVDCMOS 4.0 μm	
Transistor Count		700	
Die Size		167 X 141 X 26 (mil)	
Die Outline			
Thickness of Gate Oxide		800Å	
Connections	First Layer	Material	Poly Silicon
		Width	4 μm
		Spacing	6 μm
		Thickness	5000Å
	Second Layer	Material	Al - Si (Si: 1.0% ±0.1%)
		Width	6 μm
		Spacing	9 μm
		Thickness	20,000Å
Contact Hole Dimension		8 μm X 8 μm	
Insulation Layer	Material	PSG (SiO ₂)	
	Thickness	1.5 μm	
Passivation	Material	PSG (SiO ₂)	
	Thickness	1.5 μm	
Method of Saw		Full Cut	
Method of Die Bond		Ablebond 84 - 1	
Wire Bond	Method	Thermo Sonic	
	Material	Au (1.0 mil / 1.3 mil)	
Leadframe	Material	Cu	
	Die Area	Ag	
	Lead Plating	Pb : Sn (37 : 63)	
Package	Types	28 Lead PDIP & SOIC / 44 Lead PLCC	
	Materials	EME6300 / MP150 / MP190	
Remarks:			

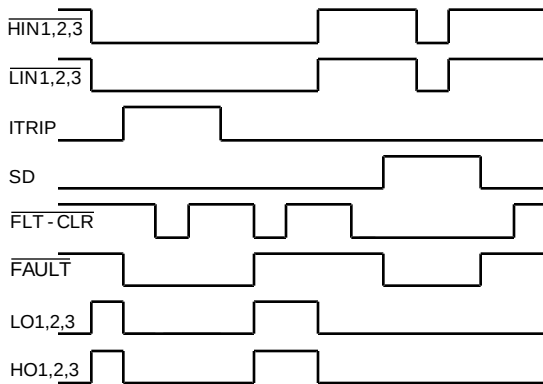


Figure 1. Input/Output Timing Diagram

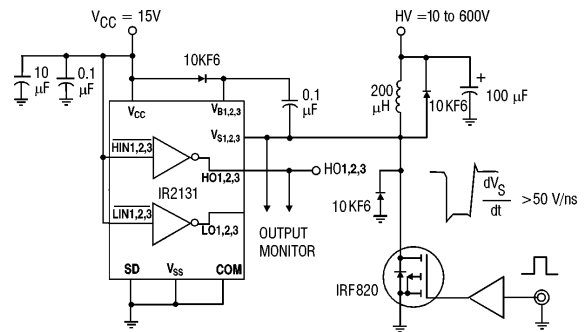


Figure 2. Floating Supply Voltage Transient Test Circuit

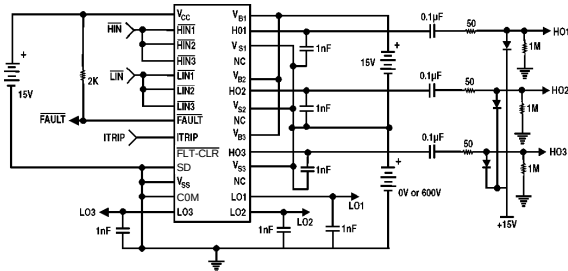


Figure 3. Switching Time Test Circuit

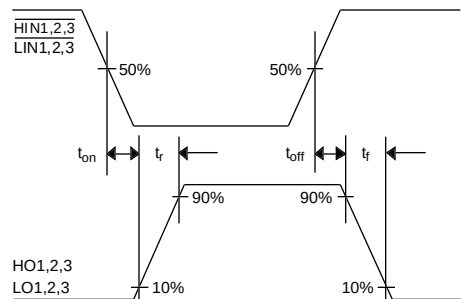


Figure 4. Switching Time Waveform Definitions

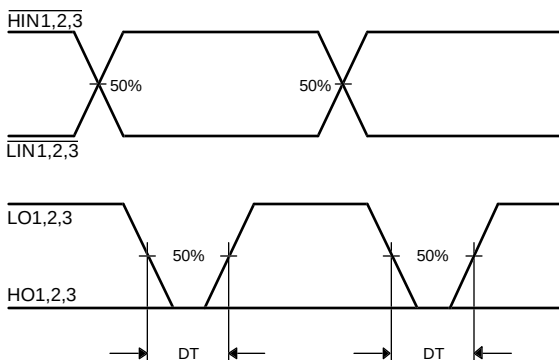


Figure 5. Deadtime Waveform Definitions

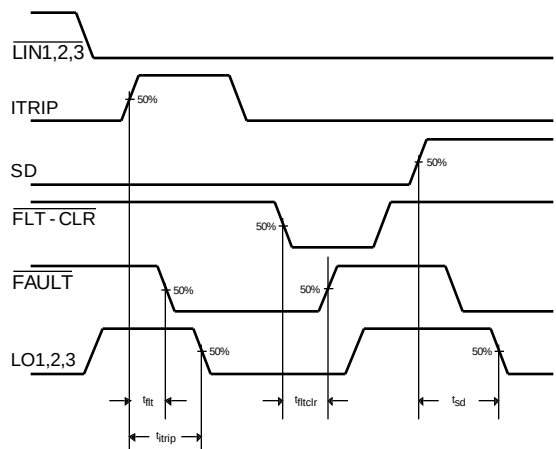


Figure 6. Shutdown Waveform Definitions

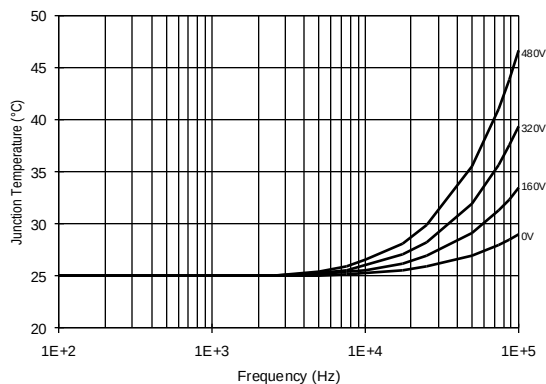


Figure 7. IR2131 T_j vs. Frequency (IRF820)
 $R_{\text{GATE}} = 33\Omega$, $V_{\text{CC}} = 15\text{V}$

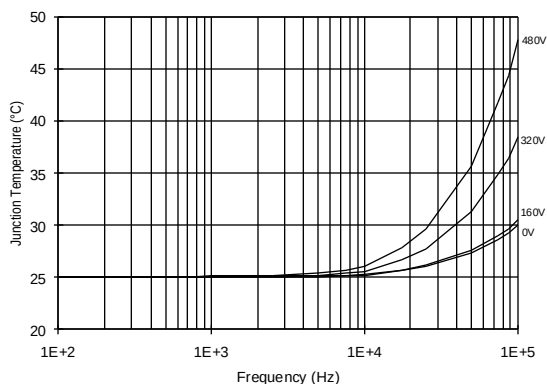


Figure 8. IR2131 T_j vs. Frequency (IRF830)
 $R_{\text{GATE}} = 20\Omega$, $V_{\text{CC}} = 15\text{V}$

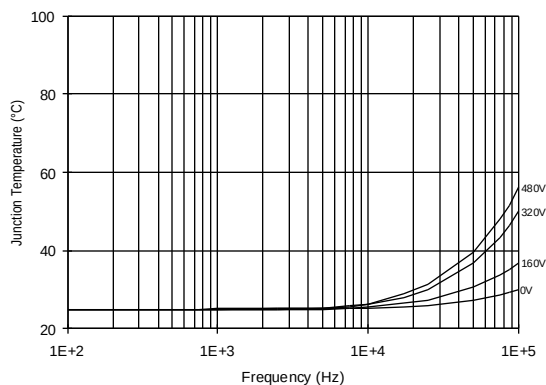


Figure 9. IR2131 T_j vs. Frequency (IRF840)
 $R_{\text{GATE}} = 15\Omega$, $V_{\text{CC}} = 15\text{V}$

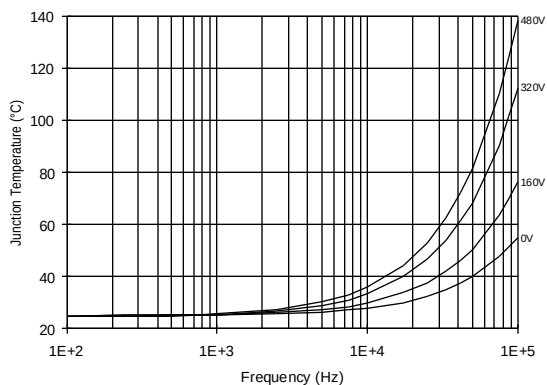


Figure 10. IR2131 T_j vs. Frequency (IRF450)
 $R_{\text{GATE}} = 10\Omega$, $V_{\text{CC}} = 15\text{V}$