Product Datasheet

MB86697A

FireStream™155 ATM 155Mbps SAR Device

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Version 2.3
/FML/NPD/FS155/DS/1973

The **FireStream™155** is a high performance ATM protocol controller which autonomously terminates ATM Adaptation Layer standard Type 5 (AAL5). ATM cells are received through a UTOPIA v2.01 compliant interface. Simultaneous segmentation and reassembly can be achieved at an average rate in excess of 155Mbps.

All ATM Forum traffic classes (ABR, VBR, CBR, UBR) are supported with traffic management to ATM Forum TM4.0 specification on up to 65536 virtual circuits (VCs).

The device is ideally suited to many ATM applications including ATM switches, access units, adaptor cards and multi-protocol hubs, bridges and routers.

PLASTIC PACKAGE
HQFP240

Features

- Broadband ISDN Adaptation Layer standard Type 5 (AAL5)
- Simultaneous segmentation and reassembly on up to 64K VCs
- ABR, VBR, UBR and CBR traffic classes with traffic management compliant to TM4.0
- Autonomous Resource Management (RM) cell handling
- 33MHz 32-bit PCI interface compliant to Revision 2.1
- Write-only interface for PDU handling with copy of SAR registers maintained in host memory
- Configuration through PCI slave port, PCI configuration optionally through serial EEPROM interface
- Transparent ATM cell and cell payload modes (AAL0) with support for Operations and Maintenance (OAM) cells
- 8/16-bit, up to 52MHz UTOPIA v2.01 level 1 and level 2 compliant cell stream interface with master/slave modes and optional HEC checking on receive
- Flexible routing tag append / remove mode for direct ATM Switch connection
- 32-bit Local memory port connects directly to SRAM
- JTAG compliant to IEEE1149.1
- Fabricated in CMOS technology with CMOS/TTL compatible 5V tolerant I/O and a 3.3V power supply

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1 Introduction

General

The **FireStream155** simultaneously supports autonomous segmentation and reassembly of user data packets on up to 64K virtual circuits (VCs). User data packets are transferred to and from shared data structure memory using a high speed 32-bit PCI bus and transferred to and from the network using a 8/16-bit UTOPIA interface.

Adaptation Layer Support

The **FireStream155** autonomously terminates the protocols involved in segmenting and reassembling data streams conforming to ATM Adaptation Layer (AAL) type5 to I.363. Streaming and Message Modes as defined for AAL5 are supported. In Message Mode, the Convergence Sublayer payload (Service Data Unit) is considered to be the user data transmitted from or received into a single entity - a single entity being regarded as one user data buffer or linked chain of user data buffers. In Streaming Mode, the Convergence Sublayer payload is considered to be the user data transmitted from or received into multiple entities separated in time. This allows a partial segmentation or reassembly. The device recognises OAM and RM cells and separates them from the data stream.

The **FireStream155** device supports two transparent modes (AAL0) with optional CRC-10 generation and checking. In transparent payload mode the 48 byte ATM cell payload is received or transmitted transparently into or from SAR Memory. In transparent cell mode the complete ATM cell, excluding the HEC, is received or transmitted transparently into or from SAR Memory.

Traffic Shaping

The **FireStream155** supports autonomous traffic shaping functions for ABR, VBR, UBR and CBR traffic. Traffic parameters are stored on a per-circuit basis in local memory. A calendar algorithm is used for traffic scheduling and has four priority levels which are independent of traffic type. ABR support includes autonomous handling of RM cells. Transmitted FRM cells are dropped into the data stream at the correct rate. Received BRM cells modify the associated VC's traffic parameters. Received FRM cells are stored locally and automatically rescheduled for transmission.

Local Memory

Control structures are initialised by the host and then copied by the **FireStream155** into local memory. These include circuit information such as VP/VC values and descriptor information such as data pointers and buffer lengths. The **FireStream155** then works on the local copy of these structures and hence does not consume any further system bandwidth. The local memory also contains static and dynamic traffic parameters and pointers for the traffic scheduling algorithm.

Cell Stream Interface

The **FireStream155** interfaces via a standard UTOPIA level 1 or level 2 interface. This 16-bit interface which operates at up to 52MHz can be configured as an ATM or a PHY (master or slave) device depending on the application. In routing tag modes the **FireStream155** adds a programmable length routing tag to the start of each ATM cell to allow connection to a switch matrix. The HEC is inserted on transmit and checked on receive. A 52-byte cell option is provided where the HEC is omitted.

PCI Master Interface

The **FireStream155** has a high performance 32-bit PCI master interface, conforming to v2.1 of the PCI specification. The programming interface has a “write-only” mode which minimizes PCI bus occupancy by removing the need for the Host to make slave read accesses.

PCI Slave Interface

A simple PCI slave control/status port is used to configure the device. Its function includes the initialization of the queue structures and the monitoring of cell and packet loss. An interrupt mechanism is implemented to indicate queue updates and exception conditions.

Circuit Initialization

Circuits are initialized for both transmit and receive by placing an entry on a high or low priority Transmit Pending Queue or onto an on-chip queue. This entry points to configuration information. A Status Queue is used to inform the user that the operation has been completed.

Transmit Operation

Transmit operation is initiated using a simple queue structure. A buffer containing part or all of a packet’s data is scheduled by placing a Transmit Descriptor pointer on the high or low priority Transmit Pending Queue. The **FireStream155** links queued descriptors for the same VC into a list. Data is then assembled under the control of the traffic scheduler into packets. The data pointer is contained in the Transmit Descriptor. When a buffer is exhausted it is returned to the host by putting the Transmit Descriptor pointer on a Release Queue.

Receive Operation

On receiving ATM cells the **FireStream155** takes a buffer from one of eight simple Buffer Free Pools. Each pool forms a linked list and buffers are allocated to the device by linking Receive Descriptors onto the list. Each pool may use a different buffer size. Receive Circuits can be allocated to one of these pools. Alternatively the device may be configured so that Receive Circuits use an initial buffer from one pool followed by subsequent buffers from another pool to reassemble a packet. This maximizes memory efficiency. Receive Circuits can have a low-priority discard mode where free buffers will not be allocated while the number of free entries is below a programmable threshold. This improves robustness of the system under heavy receive traffic loading by preventing the free pools under running. When buffers are completed they are returned to the host by putting the Receive Descriptor identifier on one of four Buffer Ready Queues.

JTAG

The **FireStream155** provides boundary scan test circuitry compliant with IEEE 1149.1 (JTAG). The **FireStream155** JTAG circuitry permits easier board level testing to be carried out by allowing the signal pins on the device to form a serial scan chain around the device. JTAG test modes are controlled by accessing an internal test access port controller via a standard JTAG test port.

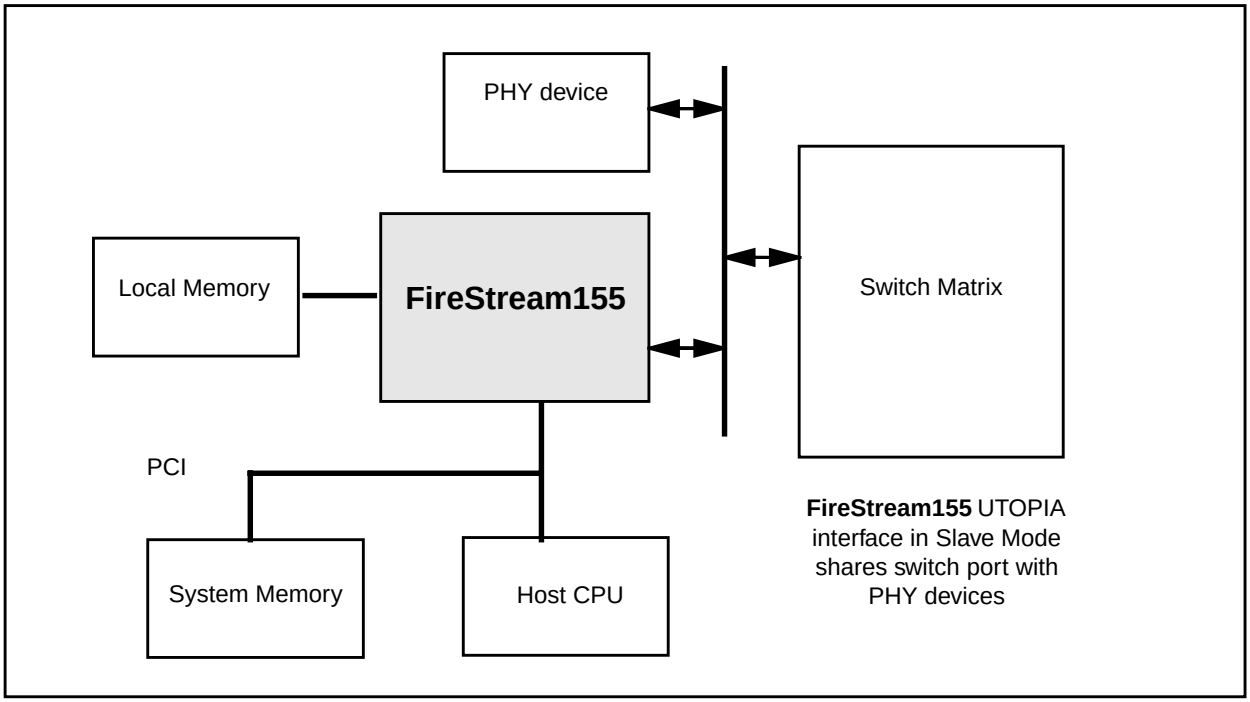

Figure 1 ATM Switch Port designed around the FireStream155

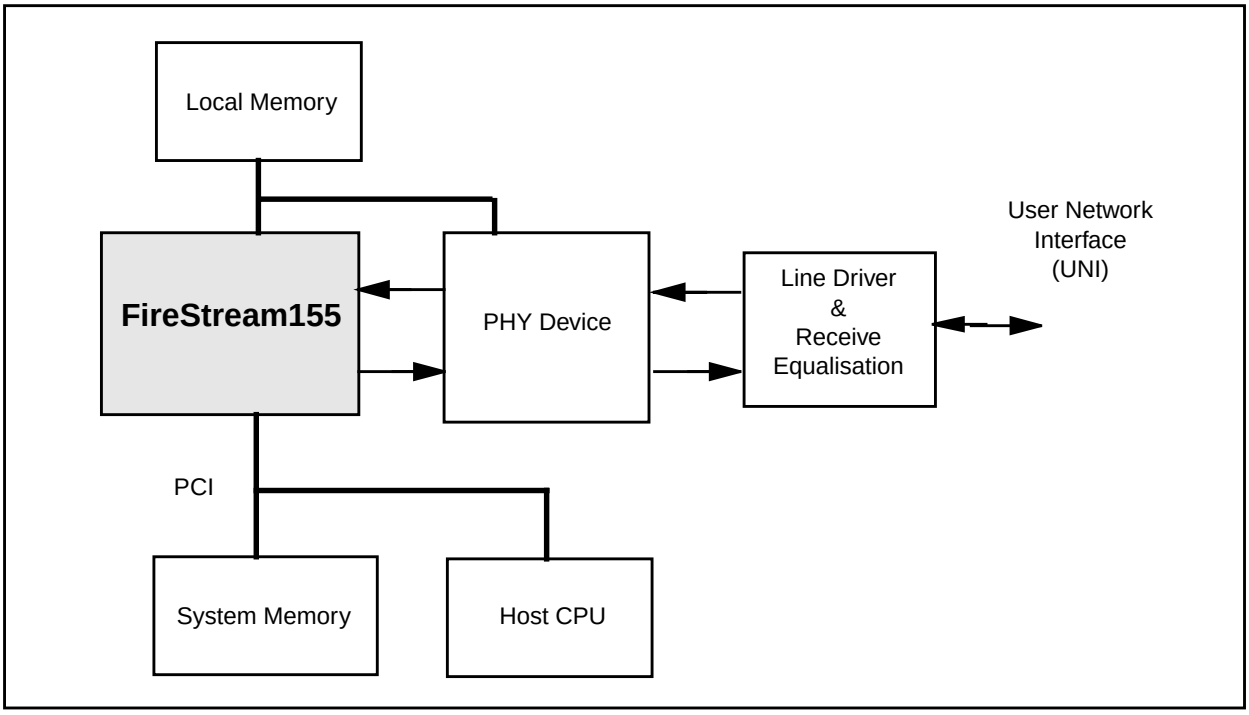

Figure 2 ATM Terminal Equipment based around the FireStream155

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2 External Interfaces

2.1 Logical Outline

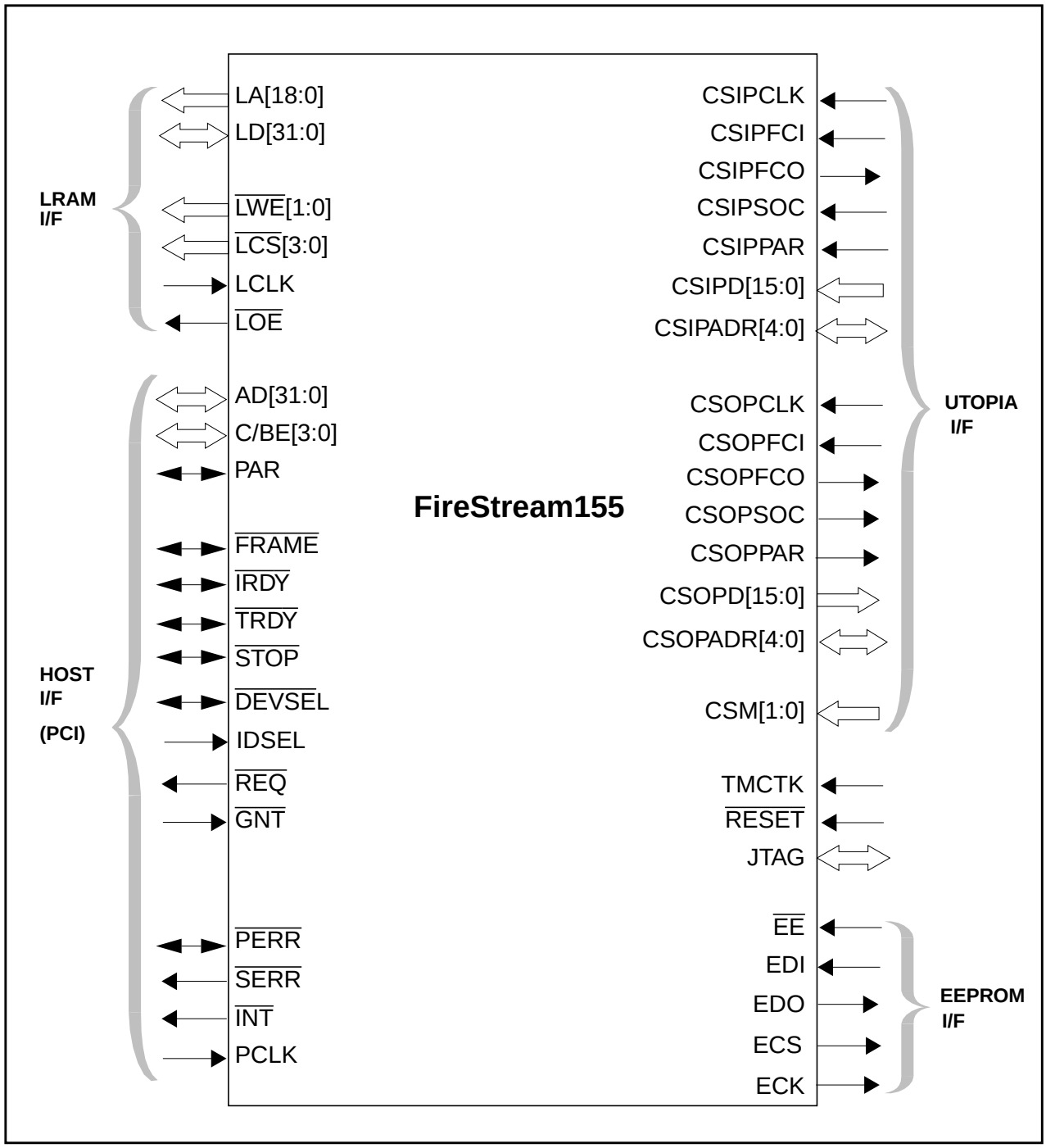

Figure 3 FireStream155 External Interfaces

2.2 Pin Descriptions

2.2.1 PCI Interface

This interface provides the **FireStream155** DMA controller with access to external system memory.

AD[31:0]
Bi-directional multiplexed address / data bus.

C/$\overline{\text{BE}}$[3:0]
Command / Byte Enables.

PAR
Even parity over AD[31:0] and C/$\overline{\text{BE}}$[3:0] buses.

$\overline{\text{FRAME}}$
Transaction frame signal.

$\overline{\text{IRDY}}$
Initiator ready to complete transfer.

$\overline{\text{TRDY}}$
Target ready to complete transfer.

$\overline{\text{STOP}}$
Transaction termination.

$\overline{\text{DEVSEL}}$
Slave device acknowledge.

IDSEL
Initialization device select.

$\overline{\text{REQ}}$
Bus request.

$\overline{\text{GNT}}$
Bus grant.

$\overline{\text{INT}}$
Interrupt output.

$\overline{\text{PERR}}$
Parity error.

$\overline{\text{SERR}}$
System error.

PCLK
PCI clock.

2.2.2 UTOPIA Interface

CSM[1:0]
UTOPIA mode pins.

CSOPD[15:0]
8/16-bit parallel output data.

CSOPPAR
Output parity.

CSOPSOC
Output start of cell signal.

CSOPADR[4:0]
Output address.

CSOPCLK
This signal is used to clock data out of the **FireStream155**.

CSOPFC I/O
See table 1 for the meaning of these flow control signals in the different UTOPIA configurations.

CSIPFC I/O
See table 1 for the meaning of these flow control signals in the different UTOPIA configurations.

CSIPD[15:0]
8/16-bit parallel input data.

CSIPPAR
Input parity.

CSIPSOC
Input start of cell signal.

CSIPADR[4:0]
Input address.

CSIPCLK
This signal is used to clock data into the **FireStream155**.

2.2.3 Local Memory Interface

LD[31:0]
Local Memory Data.

LA[18:0]
Local Memory address.

$\overline{\text{LOE}}$
Local Memory output enable.

$\overline{\text{LWE}}$[1:0]
Local Memory upper and lower word write enables.

$\overline{\text{LCS}}$[3:0]
Local Memory / Peripheral chip selects.

LCLK
Local Memory clock.

2.2.4 Miscellaneous Signals

$\overline{\text{RESET}}$
FireStream155 master reset (including PCI reset).

TMCTK
Traffic Manager calendar interval tick input.

TEST
Test input (tie to Vss for normal operation).

2.2.5 JTAG Test Port

TCK
JTAG test clock input.

$\overline{\text{TMS}}$
JTAG test mode input.

TDI
JTAG test data input.

TDO
JTAG test data output.

$\overline{\text{TRST}}$
JTAG reset.

2.2.6 Serial EEPROM Port

ECK
EEPROM clock output.

ECS
EEPROM chip select output.

EDI
Serial data in from EEPROM.

EDO
Serial data out to EEPROM.

$\overline{\text{EE}}$
EEPROM enable.

Pin Name	Direction	UTOPIA Interface Modes		
		Level 1 CSM[1:0] = 01	Level 2 ATM CSM[1:0] = 11	Level 2 PHY CSM[1:0] = 10
CSOPD[7:0]	Output	TXD[7:0]	TXD[7:0]	RXD[7:0]
CSOPD[15:8]	Output		TXD[15:8]	RXD[15:8]
CSOPSOC	Output	TXSOC	TXSOC	RXSOC
CSOPPAR	Output	TXPRTY	TXPRTY	RXPRTY
CSOPADR[4:0]	Bidirectional		TXADDR[4:0] (out)	RXADDR[4:0] (in)
CSOPFCO	Output	$\overline{\text{TXEN}}$	$\overline{\text{TXEN}}$	RXCLAV
CSOPFCI	Input	$\overline{\text{TXFULL}}$	TXCLAV	$\overline{\text{RXEN}}$
CSOPCLK	Input	TXCLK	TXCLK	RXCLK
CSIPD[7:0]	Input	RXD[7:0]	RXD[7:0]	TXD[7:0]
CSIPD[15:8]	Input		RXD[15:8]	TXD[15:8]
CSIPSOC	Input	RXSOC	RXSOC	TXSOC
CSIPPAR	Input	RXPRTY	RXPRTY	TXPRTY
CSIPADR[4:0]	Bidirectional		RXADDR[4:0] (out)	TXADDR[4:0] (in)
CSIPFCO	Output	$\overline{\text{RXEN}}$	$\overline{\text{RXEN}}$	TXCLAV
CSIPFCI	Input	$\overline{\text{RXEMPTY}}$	RXCLAV	$\overline{\text{TXEN}}$
CSIPCLK	Input	RXCLK	RXCLK	TXCLK

Table 1 FireStream155 UTOPIA modes

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3 Functional Description

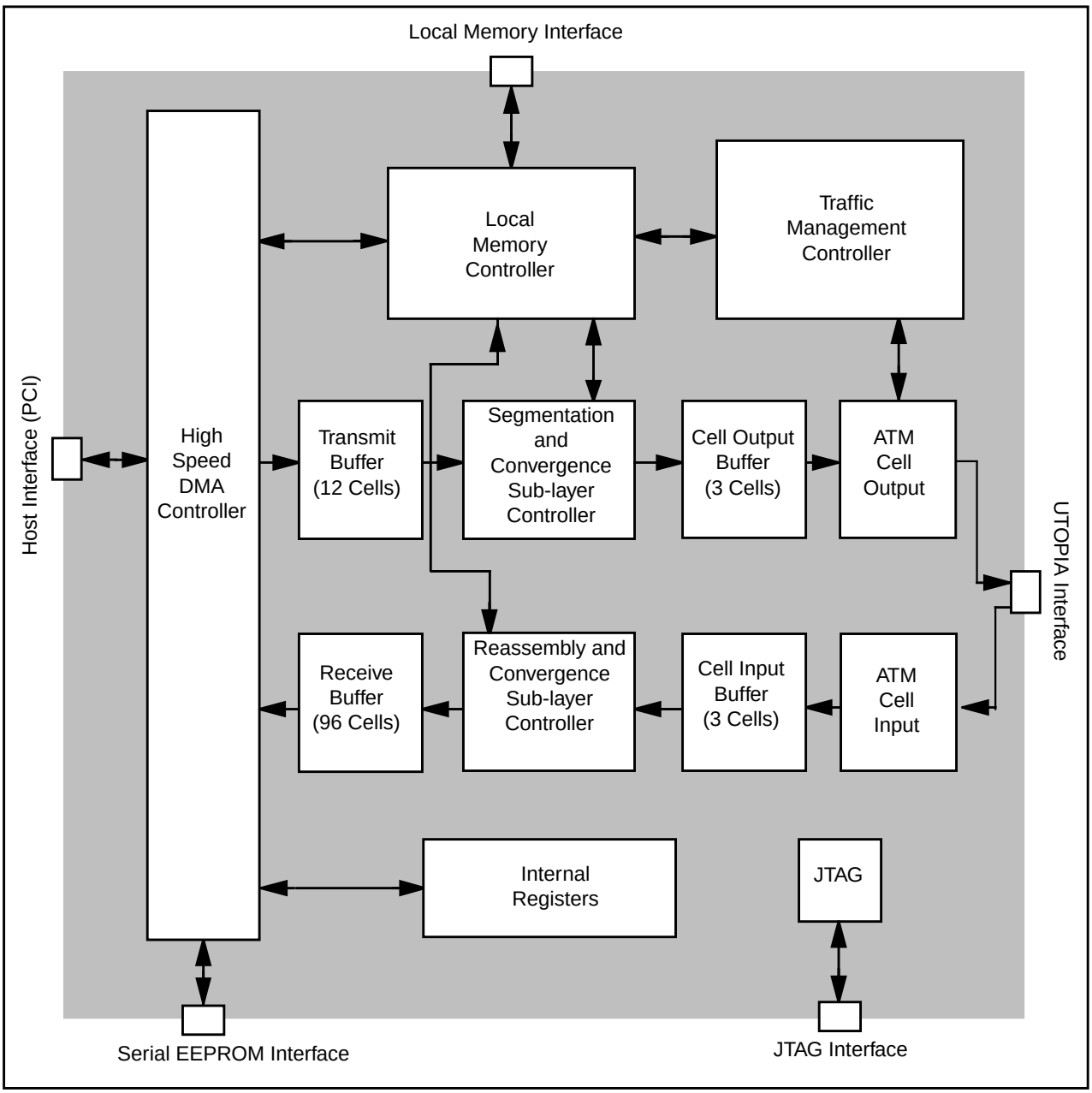

Figure 4 FireStream155 Block Diagram

3.1 Traffic Management Controller

The Traffic Management Controller communicates with the Reassembly Process, the Segmentation Process and the Local RAM (LRAM) interface. It is responsible for ensuring that the **FireStream155** conforms to the Traffic Management Specification v4.0 as devised by the ATM Forum, by managing the times at which cells are enabled to be sent. This process includes monitoring the traffic type (ABR, VBR, UBR or CBR) and the priority of the cells.

A cell scheduling process maintains a Calendar of locations representing a list of Virtual Circuits (VC) to be serviced in the order that they are to be processed. A Process Pointer keeps track of which location is being processed at any given time, and a Time Pointer keeps track of the current time. The Time Pointer is incremented by a pre-scaled version of either the Local clock or the TMCTK input. Both pointers step down the calendar and once the end is reached they return to the top. New cells which are to be scheduled are entered into the calendar with reference to the Time Pointer. Once a VC is serviced, the time it should be serviced next is calculated and a new entry is made in the calendar. Up to four calendars can be used each with a different priority. This feature can be used to allow CBR traffic to be sent in preference to other traffic types for example.

The overall traffic output of the **FireStream155** can be controlled by an additional leaky bucket traffic shaper.

RM cell handling is triggered by the Reassembly Interface once a Forward Resource Management (FRM) cell is received from the destination entity. The key elements of the FRM cell required to produce a Backward RM cell are stored in LRAM for the appropriate VC. A signal in the LRAM is set to indicate to the Scheduling Process that a BRM cell should be sent on this VC. After a BRM cell is received and before an FRM cell can be sent, the Traffic Manager triggers the Rate Calculation Process to determine the new rate for the VC. The new rate is used by the Traffic Manager to determine when the next cell should be scheduled. To control local congestion, the Host can program the **FireStream155** to behave as a congested destination and request the remote source to reduce its rate by adjusting the outgoing BRM cells.

GFC is implemented to ITU Specification I.361 section 4.1. Additionally the Host can program the **FireStream155** to report changes in GFC on a per circuit basis.

3.2 PCI Master DMA Controller

The PCI Master DMA Controller is responsible for enabling access to system memory. Within the DMA Controller accesses are shared between Transmit and Receive Buffer Managers. The **FireStream155** data-structures are defined to be highly efficient and keep the PCI bandwidth consumed to a minimum. A write-only interface for PDU handling may be implemented using registers shadowed in Host memory.

On transmit the Transmit Buffer Manager receives instructions to assemble cells from the Traffic Manager. It then makes a request to the DMA interface to transfer control information and ATM payload data. An example of control information might be to fetch, update or release a Transmit Descriptor. The Transmit Buffer Manager also processes the Transmit Pending Queues, the Status Queue and the Transmit Buffer Release Queue. It passes parameters from newly queued buffers to be stored in Local Memory.

The Receive Buffer Manager services requests for data transfer to memory for cells stored in the Rx DMA Cell Buffer. It also updates the Receive Buffer Ready queues on buffer completion and fetches

free buffers from the Buffer Free Pools for use with new data as required. Packet and Channel ageing functions are implemented in this module.

3.3 PCI Slave Interface

The **FireStream155** PCI Slave interface provides access to all the device's internal registers. It is also used to generate PCI interrupts.

3.3.1 Interrupts

Various sources of interrupt are generated by the **FireStream155** and can be signalled to PCI by asserting the PCI $\overline{\text{INT}}$ signal. The interrupt sources include:

- Transmit / Receive completion event
- Queue low fill level warning and queue underrun
- Statistics events / counter overflow
- Initialisation complete

3.4 Segmentation and Reassembly

The Segmentation Process receives user data from the Tx DMA Cell Buffer and circuit information from the Local Memory Interface. The circuit information includes the ATM header, any SAR-layer or Convergence-Sublayer information and possibly a routing tag. It carries out the appropriate SAR/CS processing on the data, appends the routing tag and ATM header and stores the cell in the ATM Cell Output Buffer. When the cell write is complete the Segmentation Process signals to the ATM Cell Output process that a cell is available for sending on the UTOPIA interface.

The Reassembly Process receives ATM cells from the UTOPIA Interface section via the Cell Input Buffer. A combination of bits from the UTOPIA address and the VP/VC fields are then used to identify the appropriate Receive Circuit Reference. Any selection of bits can be used from these fields. The data is stripped out by first removing the cell header (SAR layer) and then removing the data trailer (CS sublayer). The CRC32 check and the packet length measurement are computed at this point. The circuit information is stored in the local memory via the Local Memory Interface and the user data is sent to the system memory via the 96 Cell Receive Buffer.

3.5 Local Memory Controller

The Local Memory Controller module forms the interface between the local memory and the sections of the device requiring access to the memory. The data stored within the local memory comprises the traffic management parameters including the calendar table, cell headers, buffer parameters and other circuit information, used by both the Segmentation and Reassembly Processes. The interface also provides access via the Pending / Status Queue to enable circuit information to be accessed externally. Different numbers of VCs can be supported dependent on the amount of SRAM provided externally. For example 4x32Kx8 is enough SRAM to support 1K VCs full duplex and 4x128Kx8 is enough SRAM to support 4K VCs full duplex.

Peripherals, such as framers, which do not support PCI but can accept the SRAM interface timing, can be mapped into the LRAM address space and accessed using the Pending / Status Queue mechanism.

3.6 UTOPIA (Multi-PHY) Interface

The UTOPIA Multi-PHY interface implements the ATM Forum UTOPIA Level 1 and Level 2 interface specification with an 8/16-bit datapath. Refer to the UTOPIA Level 1/2 Specification for a detailed description of the UTOPIA interface operation and example timing diagrams. The optional TX/RXClav[3:1] signals are not supported by the **FireStream155**. The device can be configured as an ATM layer or PHY layer (master or slave) device and for level 1/2 operation by 2 mode pins.

3.6.1 ATM Layer (Master) Operation Transmit Direction

The **FireStream155** assembles cells for transmission in the Cell Output Buffer. These cells are tagged with the port address of the destination PHY device. When the **FireStream155** polls the PHY device (via the UTOPIA interface) the Cell Output Process transmits the complete cell on the UTOPIA interface if the PHY device indicates there is space for it. If no space is indicated, then the device does not transmit a cell but will continue to poll the device until such time that the cell can be accepted. The cumulative traffic queued for a given PHY port should not exceed its capacity to accept data or other PHY ports may suffer data starvation.

3.6.2 ATM Layer (Master) Operation Receive Direction

The **FireStream155** polls, selects and services enabled PHY devices on a “round-robin” basis (via the UTOPIA interface). When a selection has been made the **FireStream155** accepts a complete cell from the PHY device and stores it in the Cell Input Buffer. The Cell Input Buffer signals to the SAR/CS Receive Process block whenever there is a complete cell available. Once the SAR/CS Receive Process is ready to receive data, it empties the buffer.

3.6.3 PHY Layer (Slave) Operation Transmit Direction

When the **FireStream155** PHY port is polled by the ATM Layer (via the UTOPIA interface) the Cell Input Process signals back to the UTOPIA interface if there is space for a complete cell to be stored in its Cell Input Buffer. If no space is indicated, then it is the responsibility of the ATM layer not to transmit a cell. If a cell is erroneously sent under these conditions, it will be lost (no data will be over written in the Cell Input Buffer, and no indication is made via statistics or interrupts). The Cell Input Buffer signals to the SAR/CS Receive Process whenever there is a complete cell available. Once the SAR/CS Receive Process is ready to receive data, it empties the buffer.

3.6.4 PHY Layer (Slave) Operation Receive Direction

The SAR/CS Transmit Process waits until the Cell Output Buffer has room to accept a complete cell. It is therefore able to wait for the ATM layer device to poll, select and service the Cell Output Buffer (via the UTOPIA interface) - so this buffer will not overrun. On the UTOPIA side, if the Cell Output Buffer contains a cell ready for transfer, the Cell Output Process indicates this to the UTOPIA interface when polled.

3.6.5 Level 1 Operation

The **FireStream155** defaults to an ATM Layer device in level 1 operation. Octet level flow control is permitted during cell transmission from the PHY device. The **FireStream155** asserts its output flow

control signals on a cell boundary enabling interworking with devices implementing both cell and octet level flow control.

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4 Device Operation

4.1 Device Configuration and Start-up

4.1.1 Device Reset Sequence

On power-up (hard-reset) or after the application of a soft-reset, the **FireStream155** will carry out a reset of all control logic and internal registers and is able to execute both internal and external RAM tests. A serial EEPROM may be used to program appropriate sections of the PCI configuration space.

4.1.2 Device Configuration

Firstly the PCI configuration is completed. Then the **FireStream155** can be configured for operation by setting the appropriate bits in various control registers using the PCI slave interface. Static parameters, such as queue start and end pointers should be initialised followed by initial values of queue pointers.

4.1.3 Circuit Initialisation

Before data can be sent or received, circuit parameters for transmit and receive must be configured. These parameters are stored in Local Memory. The Pending Queues or the on-chip queue allow the user to pass parameters to the **FireStream155** using Commands. An initialisation command contains a Circuit Reference number, indicates the category of control access required and optionally points to an area of host memory where the parameters are stored or are required to be stored.

Commands are used for all control initialisation for both transmit and receive as well as setting up and modifying Traffic Management parameters and tearing down receive connections. The Status Queue provides an indication to the host that the commands placed on the control queue have been executed. An interrupt is available to flag the update of this queue.

4.1.4 Transmit Data Flow

A packet is passed to the **FireStream155** for segmentation by using the high or low priority Transmit Pending Queues. An entry on the queue points to a Transmit Descriptor and contains a Circuit Reference identifier which links it to an entry in the Local Memory. The Transmit Descriptor is associated with user data for a particular VC in host memory. The user data may form part of a packet (Chaining or Streaming modes) or an entire packet (Message mode). When a Transmit Descriptor is entered on the Transmit Pending Queue the Traffic Manager is informed that data exists for that circuit.

The Traffic Manager enters a marker for the data into one of its Calendars using the Circuit Reference identifier. When the calendar advances it searches for valid markers and, when it sees such a marker, it updates the calendar slot where the next cell should be sent using the appropriate traffic shaping parameters and requests to the Transmit Buffer Manager for a cell's worth of data for that circuit. The Transmit Buffer Manager fetches the data via the PCI DMA interface and performs any necessary buffer management, such as releasing a used buffer to the Transmit Buffer Release Queue or a chaining or streaming operation. The data is stored in the Transmit DMA buffer and is tagged with the

Circuit Reference. When a whole cell has been assembled in the buffer and there is also room for a cell's worth of data in the ATM Cell Output Buffer, the segmentation process fetches the ATM header, any SAR-layer or Convergence-Sublayer information and possibly a routing tag. It carries out the appropriate SAR/CS processing on the data, appends the routing tag and ATM header and stores the cell in the ATM Cell Output Buffer.

When the cell write is complete the Segmentation Process signals to the ATM Cell Output process that a cell is available. The cell is then output on the UTOPIA interface under the control of the UTOPIA flow control mechanisms with the HEC inserted and the CRC10 calculated as required.

4.1.5 Receive Data Flow

A cell arriving at the ATM Input Process is processed according to the UTOPIA flow control mechanisms. As it arrives it is buffered in the Cell Input Buffer. The cell is accepted if it passes the HEC and CRC10 checks as appropriate. The cell is then handed to the Reassembly Process. This process firstly maps the VP/VC onto a Receive Circuit Reference. This Circuit Reference is used as an address to look up circuit parameters in local memory. These parameters include SAR-layer and Convergence-Sublayer values and circuit status.

If the circuit is not activated, it may optionally be tagged as unknown and forwarded to the Host. If not, or if the packet is in discard mode after a protocol error or "packet too long detected", the cell will be dropped at this point. Otherwise the cell is stored in the Receive DMA Cell buffer with its Circuit Reference. When the Receive Buffer Manager sees a complete cell in the buffer it reads the appropriate buffer status information from Local Memory. If packet ageing is enabled and the packet is too old, reception is aborted and the host notified. If the circuit is active but no buffer is indicated and, for low priority circuits, enough free buffers are available, the Receive Buffer Manager will fetch a new buffer via the PCI DMA Interface from one of the pools of free buffers maintained by the Host.

The choice of which pool to use is determined by the mode of the circuit which is programmed by the Host. If the cell is the first in a packet then it might choose a buffer from a pool of small buffers, otherwise from a pool of large buffers. Alternatively there may be a fixed association between a VC and one of the pools. The cell is then transferred to host memory using the data pointer provided.

4.2 Test Modes

4.2.1 Loopback

A loopback path can be enabled within the **FireStream155**, as shown in Figure 5. This is a loopback path between the Utopia output path, and the Utopia input path. CSOPCLK and CSIPLCK do not need to be running during loopback testing and the UTOPIA interface will be idle.

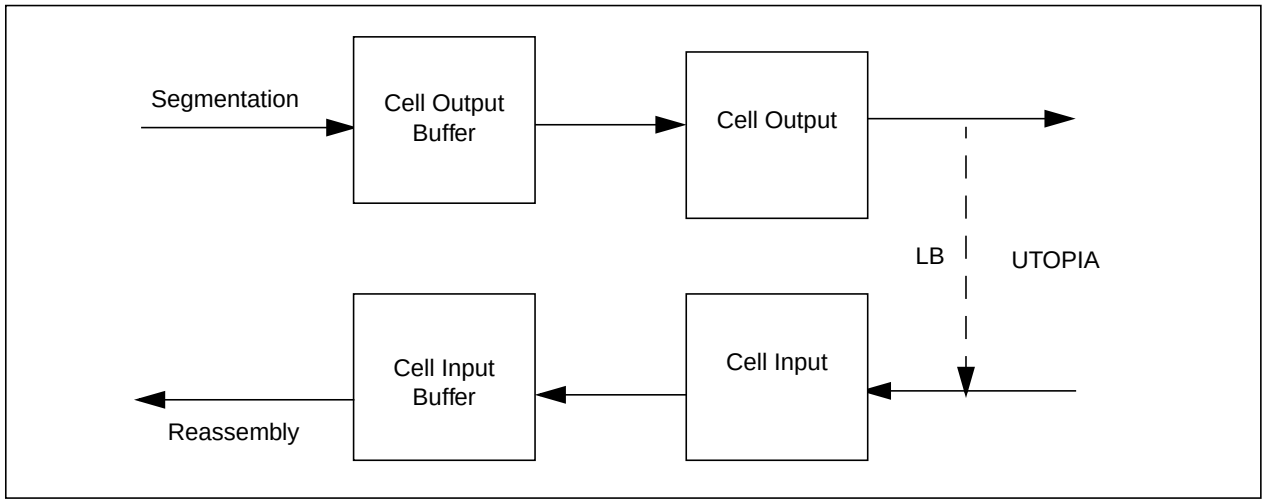

Figure 5 FireStream155 Loopback Mode

4.2.2 Local Memory

The **FireStream155** will automatically test the local memory on initialisation. Parameters in this memory are initialised by the Host and maintained by the device. For debugging purposes the user may use commands to obtain a dump of the contents of the local memory.

4.3 Clocks

The **FireStream155** requires up to 4 separate external clocks, PCLK, LCLK, CSOPCLK and CSIPCLK.

PCLK provides a clock for the PCI Interface. This Interface can run at any frequency up to 33MHz. LCLK provides a clock for the Local Memory Interface and can run at up to 33MHz. The CSOPCLK and CSIPCLK pins provide the clocks for the UTOPIA interface. The UTOPIA specification characterises the interface for clock speed of 25, 33 and 50MHz, but the interface may also be run at any frequency, up to 52MHz maximum for Level2 and 33MHz for Level1. The transmit and receive parts of the UTOPIA interface do not have to run at the same clock speed.

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5 Traffic Management

5.1 Calendar Algorithm

5.1.1 Principle of Operation

The calendar controller maintains a list of locations in LRAM representing calendars of channels to be serviced according to the time at which they are to be processed. A Process Pointer keeps track of which location is being processed at any given time, and a Time Pointer keeps track of the current time. Both pointers step down the calendar and once the end is reached they return to the top. New cells which are to be scheduled are entered into the calendar with reference to the Time Pointer, and ahead of the Time Pointer. If two or more channels should be scheduled in one location, then a linked list is formed in order to maintain the correct scheduling order.

Every cell period the Time Pointer always moves to the next location in the list but the progress of the Process Pointer depends on the entry at the current location. Where there are many operations scheduled in one location, the Process Pointer waits until all the channels for that location have been serviced and therefore falls behind the Time Pointer. However, any empty locations will be skipped by the Process Pointer and hence it will catch up with the Time Pointer.

Once a channel is serviced, the time it should be serviced next is calculated and a new entry is made in the calendar. The range of the calendar scheme is between 6 and 365,000 cells/sec or 2.37Kbits/sec to 155 Mbits/sec at a resolution of 1.56%.

5.1.2 Multiple Calendars

The Traffic Management module can maintain up to 4 calendars of descending priority. Therefore, different channels or traffic types can be prioritised by associating them to different calendars.

If the Process Pointer on a higher priority calendar should catch up with the Time Pointer on that calendar, then the Traffic Manager will service channels on the calendar of immediately lower priority. This process is illustrated in Figure 6 and Figure 7.

5.1.3 Controlling the calendars

The calendars are initialised by the **FireStream155** on power-up. The calendar entries are all cleared and the process pointer and time pointer are aligned. The calendars are enabled for operation by setting the calendar enable bits in the Traffic Management Configuration register.

The rate of processing for each calendar (cell interval) can be individually controlled by selecting between a programmably divided version of either the local clock (LCLK) or an asynchronous external calendar tick input (TMCTK).

5.1.4 Behaviour Under Extreme Traffic Overload

The process pointer will lag behind the current time pointer on the calendar if too much traffic is scheduled or if DMA bandwidth is insufficient to sustain the programmed bandwidth.

In this case the difference between the process pointer and the current time pointer is limited. This causes the time pointer to slow down. When process pointer catches up, the time pointer can advance at its usual rate.

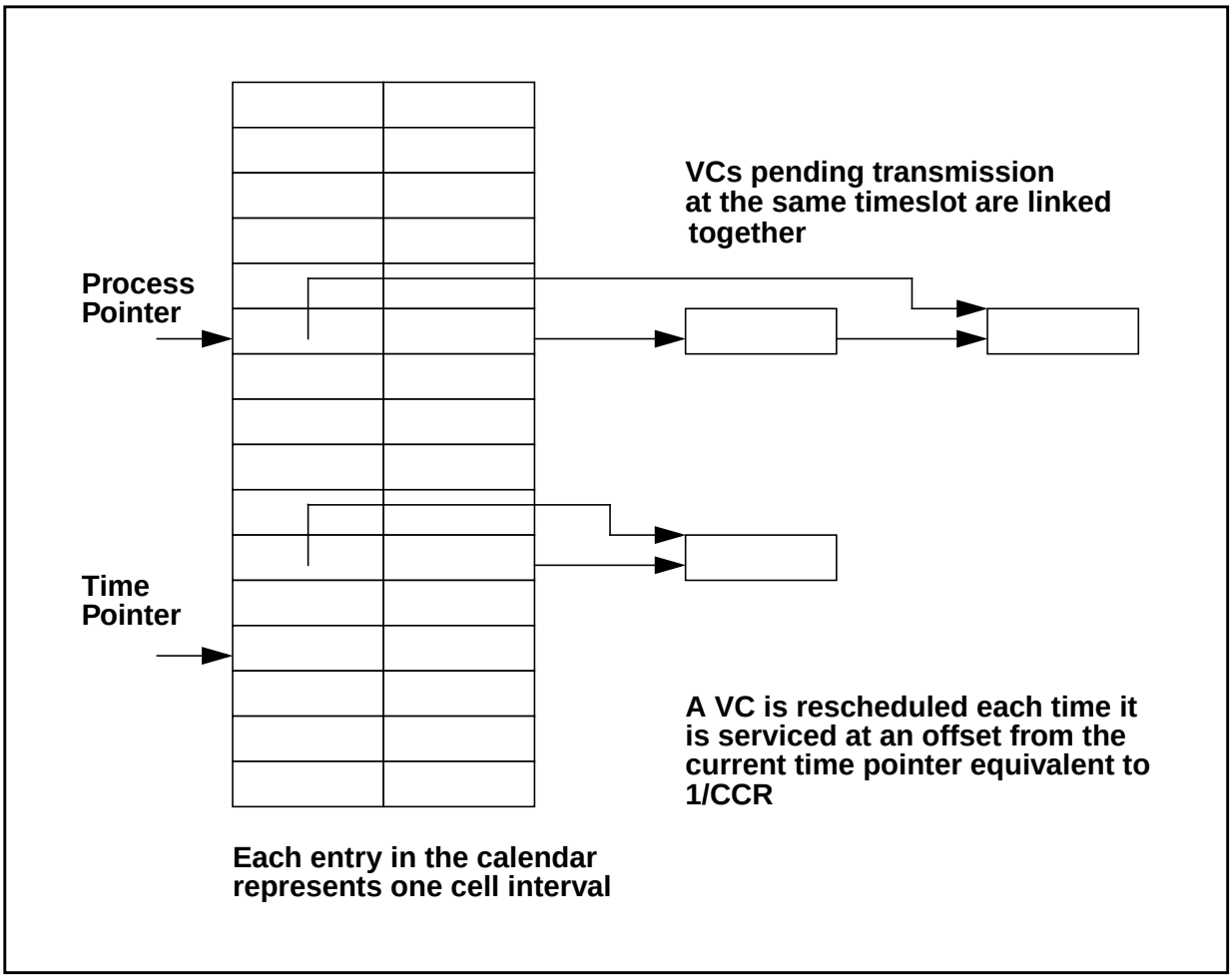

Figure 6 Calendar Algorithm

5.2 VBR & CBR Implementation

5.2.1 Leaky Bucket Algorithm

The VBR and CBR traffic types are dealt with using a leaky bucket algorithm. When a circuit is encountered in the calendar, the number of new tokens is computed, When tokens are available the next cell is scheduled at 1/PCR interval. If no tokens are available then the next cell is scheduled at 1/SCR interval.

CBR circuits are programmed in a similar way to VBR, but with PCR only defined. However, CBR circuits modify the calendar algorithm slightly. Instead of being rescheduled relative to the current time pointer, they are scheduled relative to the time when they should have been sent (subject to this

not being less than the current time). This ensures that the rate is maintained. Assigning these circuits to the highest priority calendar will ensure that the CDV is kept to a minimum.

When no further data is available on a VBR channel, the time of sending the last data cell is recorded and no new entry made in the calendar. If new data is queued at a later time, the current time and timestamp are compared to compute any new tokens and the circuit is scheduled back into the calendar.

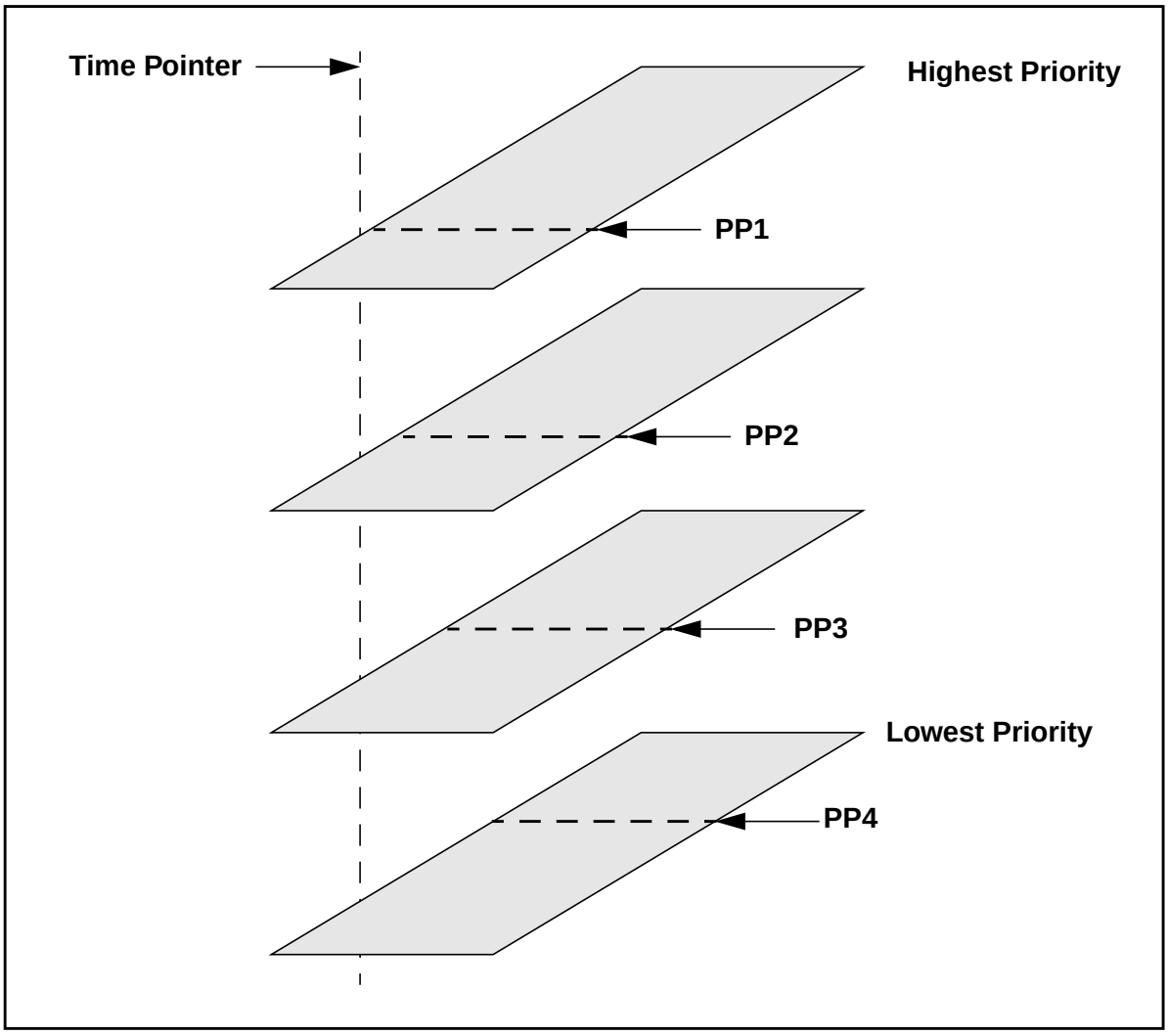

Figure 7 Calendar Priority Mechanism

5.3 ABR Implementation

5.3.1 Source Behaviour

The source behaviour conforms to the specification in TM 4.0 section 5.10.4. Cells are scheduled in the calendar using the current interval 1/CCR.

5.3.2 Transmission of FRM cells

The first cell to be transmitted on an ABR circuit is an FRM cell. FRM cells are composed autonomously by the **FireStream155** using the channel's parameters stored in local memory. FRM cells are then sent every Nrm cells or at Trm (typically10) cells/sec - whichever is the greater. The **FireStream155** keeps a count of data cells between FRM cells and also timestamps the last FRM transmission to make sure these rules are obeyed. Every time an FRM cell is sent the count of FRM cells since last BRM is incremented. If the circuit's CCR becomes zero then the FRM cells may be optionally sent out of rate with the CLP bit set. If the channel runs out of data, no further FRM cells are sent.

5.3.3 Reception of BRM cells

When a BRM cell is received it is examined to see if the NI or CI are set or if the ER is programmed. The transmission rate is adjusted accordingly. Also if BN = 0, the count of FRM cells sent on this ABR channel since the last BRM cell was received is reset.

5.3.4 No Data To Send

If a channel's data source is exhausted, the **FireStream155** marks the channel as being in a waiting state. During this period the ADTF timeout is monitored. If it expires then the channel becomes idle and returns to its initial state (the rate is reset to ICR). Otherwise if new data arrives it continues to be processed using existing parameters.

5.3.5 Destination Behaviour

The destination behaviour confirms to the specification in TM 4.0 section 5.10.5.

5.3.6 Reception of FRM cells

FRM cells received by the **FireStream155** are processed and the relevant parameters stored in local memory. FRM turnaround strategies 1, 2, 3 and 4 are supported.

Note that the **FireStream155** does not store the SN and QL fields of the RM cell. These fields are set to zero on outgoing FRM cells. However, the user can program the **FireStream155** to pass RM cells in Transparent Cell buffers to allow access to the received SN and QL fields.

5.3.7 Transmission of BRM cells

BRM cells are constructed from the parameters stored from a previous FRM cell reception but may be modified if the congested destination behaviour is enabled.

5.3.8 Congested Destination

The system environment of the **FireStream155** may be such that from time to time resources to handle receive traffic become scarce. In this case the Host can instruct the **FireStream155** to modify the BRM cells it sends out - either by use of the NI and CI bits or by modifying the Explicit Cell Rate by a factor of $1/2^n$. Each ABR channel can be assigned to one of eight groups so that only an

appropriate selection of channels are affected. This assignment may correspond with the association of channels with the 8 Buffer Free Pools.

5.3.9 Uni-directional Channel

The **FireStream155** may receive RM cells on a channel where there is no corresponding transmit channel. In this case the RM cell will be turned round immediately and sent back out-of-rate.

5.4 UBR Implementation

UBR traffic is implemented in a similar way to CBR in that it is always scheduled at its peak rate. It is recommended that the lowest priority calendar be used for this traffic type.

5.5 Overall Traffic Shaping

The overall rate of ATM cell transmission can be controlled by an additional leaky bucket process. The peak and average rates and the bucket size are all programmable via the Cell Output Shaping Configuration register.

5.6 Configuration and Performance Monitoring

5.6.1 Channel Initialisation

The **FireStream155** traffic management parameters are stored in local memory rather than host memory. As for all parameter initialisation, the Transmit Pending Queues or on chip queue are used to allow the user to pass the necessary values to the **FireStream155**.

5.6.2 Channel Parameter Modification

The **FireStream155** Pending Queues can be used during normal operation to pass commands to the device to modify the Traffic Management Parameters. This process can be immediate or linked to a particular place in the data stream (e.g. at the end of a packet).

5.6.3 Performance Monitoring

The **FireStream155** Commands can also be used during normal operation to report the status of the Traffic Management Parameters. The entire Traffic Management local storage can be dumped to Host memory.

5.7 GFC Support

Generic Flow Control (GFC) is a mechanism allowing a Controlling function to control the Traffic Output from a controlled device, using the 4-bit GFC field in ATM cell headers (GFC is applicable to UNI interfaces only). The GFC algorithm may be applied independently to each calendar. Each calendar may be ‘assigned’ to the GFC algorithm and may be ‘controlled’ or ‘uncontrolled’. (refer to ITU specification I.361).

A counter is set by the GFC fields of incoming cells and decremented when a cell is sent on a 'controlled' calendar.

In certain circumstances, a user may wish to be informed of changes in the GFC field, for example, when the GFC field is being used within a system to convey other status information. The **FireStream155** can optionally inform the Host via an RBRQ entry, of any change in the GFC field on a per channel basis.

5.8 Rate Parameters

The various rate parameters (e.g. PCR, SCR) are programmed using the binary floating point representation as described in TM 4.0 section 5.10.3.2. For example, a rate of 155Mbps equates to a PCR setting of `0x64C9`.

6 Programming Interface

6.1 Concepts

The Programming (Hardware-Software) Interface defines the bi-directional interface between the Host Processor Software and the **Firestream155**. Figure 8 shows the basic data structures used by the **Firestream155**. Communication between the Host and the device is achieved via **Firestream155**->Host and Host->**Firestream155** queue structures in an area of memory accessible by both the Host and the **Firestream155** (Shared Memory).

Payload data is transferred between the Host and the **Firestream155** via data buffers. Each data buffer has an associated descriptor. The descriptor contains a pointer to the data buffer, and may additionally provide limited control information about the data buffer. A descriptor is an area of memory containing the linked list control information associated with a data buffer.

6.1.1 Transmit Path

When data is to be transmitted an entry is placed on an appropriate Pending Queue. This entry contains a pointer to a single descriptor or pointers to the beginning and end of a linked list of descriptors, that in turn point to the buffers containing the data to be transmitted.

The **Firestream155** maintains a linked list of data to be transmitted for each channel, using descriptors. This is called the Channel Queue. When the Host passes new data for transmission, the **Firestream155** adds the linked list onto the end of the appropriate Channel Queue. The Channel Queue concept is shown in Figure 9. When the **Firestream155** has completed transmission of the User Data, used descriptors will be returned to the Host via a Transmit Buffer Release Queue entry.

6.1.2 Receive Path

When the **Firestream155** receives the first cell of a packet, it will obtain a new Receive Descriptor from a Buffer Free Pool. A Buffer Free Pool is a linked list of descriptors in Shared Memory which is constructed and maintained by the Host.

The **Firestream155** places the user data in the buffer pointed to by that descriptor. When a termination event (usually end of buffer or end of packet) is recognised by the **Firestream155**, an entry is placed upon an appropriate Buffer Ready Queue. This entry contains a pointer to the beginning (and optionally the end) of a linked list of descriptors, which in turn point to the received packet data. The Buffer Ready Queue entry also contains status information regarding the received data.

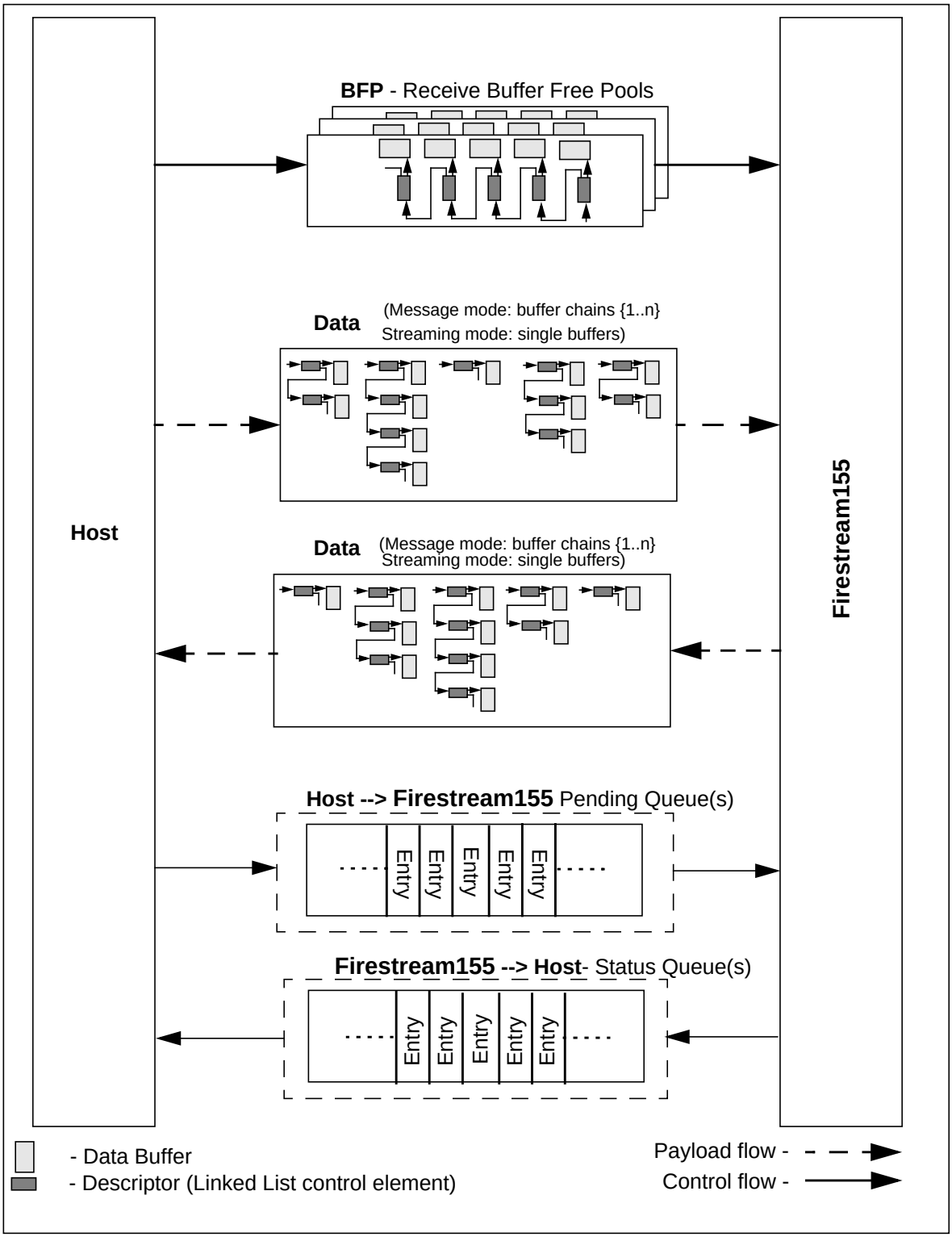

Figure 8 Firestream155 Basic Data Structures overview

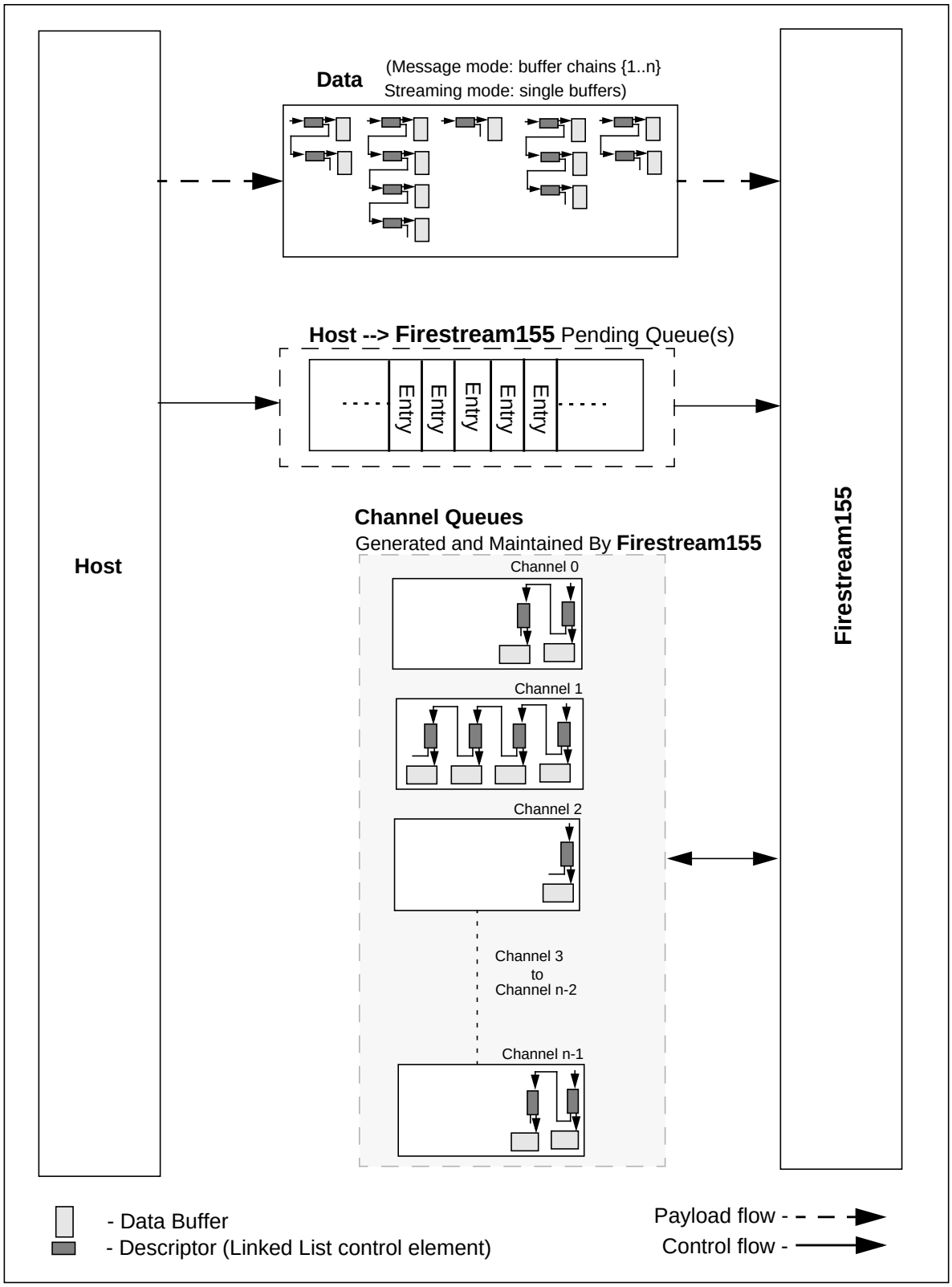

Figure 9 Transmit Path Overview

6.2 FireStream155 Modes of Operation

Four major modes of operation are supported by the **FireStream155**. Packet (Message) Mode, Streaming Mode, Store & Forward Mode and Position Mode. The latter two modes are derived from Streaming Mode and are used to maintain the position of OAM cells within a received cell stream.

6.2.1 Packet (Message) Mode

In Packet (Message) Mode, a complete AAL PDU is stored in one or more data buffers. The complete AAL PDU is passed between the Host and **FireStream155** in a linked list (or chain) of buffers.

In the transmit direction, pointers to the head and the tail of the chain of buffers are passed to the **FireStream155** using a Pending Queue entry.

In the Receive direction, data is only returned to the Host when a complete AAL PDU has been received into one (or more) buffers. A linked list (chain) of receive data buffers is formed in Shared Memory by the **FireStream155** as data is received. When a complete packet has been received, the linked list is passed to the Host via a Receive Buffer Ready Queue (RBRQ) entry. If OAM cells are mixed within the received cell stream, they are passed from the **FireStream155** to the Host via separate RBRQ entries.

Two distinct types of Packet (Message) Mode are specified: Packet Mode (Single Buffer) and Packet Mode (Multiple Buffers). In the former, a single buffer contains the whole AAL PDU, and in the latter the AAL PDU may be stored in one or more buffers. If a receive channel is programmed as packet Mode (Single Buffer) and the AAL PDU is too large to fit into a single buffer, packet re-assembly is aborted and the buffer is returned to the Host via a Buffer Ready Queue entry, which indicates the error status.

6.2.2 Streaming Mode

Streaming mode allows incomplete AAL PDU payload data to be transferred between the Host and **FireStream155**. On transmit, data can be passed to the **FireStream155** for transmission as part of an AAL PDU before the Host has compiled and buffered the complete AAL PDU.

Similarly on receive, data buffers can be passed to the Host for processing before the end of the AAL PDU is detected. When a data buffer becomes full, it is immediately passed to the Host via an RBRQ entry. No linked lists are formed by the **FireStream155** in Shared Memory.

Note that an OAM cell's position in the receive cell stream is not maintained in Streaming Mode but is provided on a separate queue entry.

6.2.3 Store & Forward Mode

The Store & Forward operation allows the **FireStream155** to be used as part of a simple switch or uplink station. Receive data may be passed from the RBRQ to a Transmit Pending Queue with minimal Host intervention.

Store & Forward mode is a modified form of Streaming Mode. The only difference is in the way Store & Forward Mode treats non-payload cells (e.g. OAM cells) in the receive cell stream. The position of OAM cells in the receive data stream is maintained by immediately terminating the current data buffer and placing the entry on the RBRQ followed by the OAM cell in a separate buffer. Note that in certain

circumstances, the number of payload bytes in a data buffer reported by the **FireStream155** may include pad bytes.

6.2.4 Position Mode

In certain applications, for example OAM based encryption or Cells in Frames, other than Store & Forward Mode, it is important to maintain the position of control cells (e.g. OAM cells) within a data stream. This is achieved using Position Mode. This mode is similar to Store & Forward Mode except that the current data buffer is not returned to the Host until the next data cell is received, The ensures that the correct packet length is always reported to the Host.

6.2.5 Transparent Payload

The Host or **FireStream155** provides multiple cell payloads (48 bytes) in data buffers.

In the transmit direction, the Host provides the data via a descriptor in a Transmit Pending Queue entry. Each 48 byte payload data has an ATM header added by the **FireStream155**, before being transmitted. No further AAL processing is performed. A CRC10 calculation may be performed on the cell payload. This 10-bit result overwrites the last 10-bits of each ATM cell payload.

In the receive direction, the **FireStream155** removes the ATM header from received data cells, prior to writing the 48 bytes of payload data to a data buffer. The **FireStream155** may also perform a CRC10 check on each incoming cell payload. If a CRC10 error occurs, the current buffer is returned to the Host via a Receive Buffer Ready Queue entry, which indicates the CRC10 failure. Further received data is placed in a new buffer.

6.2.6 Transparent Cell

The Host or **FireStream155** provide multiple ATM cells (48 payload bytes, plus default ATM header, but excluding the HEC byte). This 52 byte data is contiguous in the data buffer.

In the transmit direction, the Host provides the data via descriptors in a Transmit Pending Queue entry. As in Transparent Payload mode, an optional CRC10 calculation may be performed, with the 10-bit result overwriting the last 10 bits of each ATM cell payload.

In the receive direction, the **FireStream155** writes the complete cell (48 byte data plus ATM header, excluding HEC byte) into a data buffer. An optional CRC10 check may be performed, as in Transparent Payload mode.

Note that in the transmit data buffer, the ATM cell header must be written in little endian format. i.e. the first header byte of the cell should be in the most significant address. Similarly, the header will appear in this format for received data buffers.

6.2.7 OAM Cell Support

Any active receive channel may receive F4 or F5 OAM cells. The **FireStream155** does not autonomously process OAM cells. However there is a mechanism to allow the **FireStream155** to pass OAM cells to the Host using transparent cell mode. Each OAM cell uses a separate buffer and reception is indicated using special Receive Buffer Ready Queue entries. The forwarding of OAM cells to the Host can be configured on a per-channel basis. Alternatively, the **FireStream155** is able to extract and discard these cells.

6.3 Control Functions

6.3.1 Channel and Packet Ageing

Receive Packet Ageing

The **FireStream155** implements Receive Packet ageing. This is a mechanism by which the Host can specify a maximum time between receiving the first and last cell of a packet. The Receive Packet Ageing threshold value is programmable between 1ms and 30s. The Receive Packet Ageing function can be enabled or disabled independently for each receive channel. When a packet exceeds the maximum age, the **FireStream155** passes the existing data buffer(s) to the Host via a Receive Buffer Ready Queue entry with the Receive Packet Ageing Status code. All further data for that packet is discarded.

Receive Channel Ageing

The **FireStream155** implements Receive Channel ageing. This is a mechanism by which the Host can specify a maximum time between receiving packets. The Receive Channel Ageing threshold value is programmable between 4ms and 120s. The Receive Channel Ageing function can be enabled or disabled independently for each receive channel. When an idle period between packets exceeds the maximum age, the **FireStream155** passes a message to the Host via a Receive Buffer Ready Queue entry with the Receive Channel Ageing Status code. The Host may than take whatever action it deems necessary.

6.3.2 Interrupts

The **FireStream155** can generate an external interrupt in order to inform the Host of events. For example, the **FireStream155** may interrupt the Host when a write, or a number of writes, to a Receive Buffer Ready Queue takes place. This allows the Host to be designed to poll status/pointer registers in the **FireStream155**, or to be interrupt driven. Each interrupt event can be independently maskable and a global interrupt enable is provided.

There are several mechanisms defined for accessing the **FireStream155** Interrupt Status register and Re-Enabling Interrupts during interrupt servicing.

These mechanisms are:

- Read and Clear: when the Host reads the **FireStream155** Interrupt Status Register (ISR), the interrupt flags are cleared at completion of the bus read cycle.
- Read and No Clear: when the Host reads the **FireStream155** ISR, the interrupt flags are not cleared. Clearing the flags requires an separate write to the Interrupt Under Service Register (IUSR). Any bit set in the IUSR by the Host write, will clear the corresponding interrupt from the ISR.
- Read, Clear and Inhibit: when the Host reads the **FireStream155** ISR, the interrupt flags are cleared at completion of the bus read cycle. Additionally, **FireStream155** interrupt reporting is globally disabled. A write to the **FireStream155** is required to globally re-enable interrupt generation.
- Read, No Clear and Inhibit: when the Host reads the **FireStream155** ISR, the interrupt flags are not cleared, and **FireStream155** interrupt reporting is globally disabled. Clearing interrupt conditions requires a separate write to the IUSR. Any bit set in the IUSR by the Host write, will

clear the corresponding interrupt from the ISR. A separate write to the **FireStream155** is required to globally re-enable interrupt generation.

6.3.3 Register Access and Register Shadowing

All registers within the **FireStream155** are readable.

In Addition, the **FireStream155** can be configured to shadow queue pointers and status information in Host memory. This information is updated at a programmable interval provided that some change has occurred in one or more of the shadowed registers. This mechanism eliminates unnecessary PCI slave reads which are inefficient and reduce system performance.

The shadowing function is configured by programming a Shadow Base Address, a Shadow Update Period and the Shadow Select bit in the Shadow Configuration Register and by setting the value of INTMODE in SAR Mode Register 0. The shadowing function is enabled by setting the SHADEN bit in SAR Mode 0 Register.

All Shadowed registers are written to system memory when the programmed time interval expires provided that a change has occurred in at least one of the shadowed registers. If no change has occurred at this point then the next change immediately triggers an update. The hardware interrupt will not be driven until the shadow register update has been completed and must be explicitly cleared using the Interrupt Under Service Register (INTMODE `00` is not supported if using shadowing).

Further shadow updates may be inhibited until the IUSR has been accessed by setting the INTMODE field in SAR Mode Register 0 to Read, No Clear mode (`01`).

The registers that are shadowed are shown in Table 2 and Table 3.

Offset From Shadow Base Address (Hex)	Register	Register Offset (Hex)
00	Rx Buffer Ready Queue 3 Write Pointer	17C
04	Rx Buffer Ready Queue 2 Write Pointer	168
08	Rx Buffer Ready Queue 1 Write Pointer	154
0C	Rx Buffer Ready Queue 0 Write Pointer	140
10	Tx Buffer Release Queue Write Pointer	02C
14	HP Tx Pending Queue Read Pointer	008
18	LP Tx Pending Queue Read Pointer	018
1c	Status Queue Write Pointer	054
20	Buffer Free Pool Status	130
24	Interrupt Status Register	064

Table 2 Shadowed Registers (Shadow Select = 0)

Offset From Shadow Base Address (Hex)	Register	Register Offset (Hex)
00	Rx Buffer Ready Queue 3 Read Pointer	178
04	Rx Buffer Ready Queue 2 Read Pointer	164
08	Rx Buffer Ready Queue 1 Read Pointer	150
0C	Rx Buffer Ready Queue 0 Read Pointer	13C
10	Tx Buffer Release Queue Read Pointer	028
14	HP Tx Pending Queue Write Pointer	00C
18	LP Tx Pending Queue Write Pointer	01C
1c	Status Queue Read Pointer	050
20	Buffer Free Pool Status	130
24	Interrupt Status Register	064

Table 3 Shadowed Registers (Shadow Select = 1)

6.3.4 Low Priority Discard Modes

The **FireStream155** provides two mechanisms to allow graceful degradation of receive performance under heavy system loading and are designed to prevent loss of critical data.

Receive Buffer Manager LPD

If there is a scarcity of free receive buffers, this mechanism allows low priority traffic to be discarded. Each receive channel can be marked as low priority by clearing the Buffer Free Pool Priority bit if the receive configuration. A receive descriptor will only be allocated to a low priority channel if there is a minimum number of buffers available on the associated Buffer Free Pool. This minimum value is programmed by the host, and is the same value as that used for the Buffer Free Pool Nearly Empty interrupt (specified in the Buffer Free Pool Configuration registers). If a channel does not get a requested buffer, then the user is notified by an entry on the associated Receive Buffer Ready Queue and the rest of the packet is discarded.

Reassembly LPD

If the host PCI bus is saturated and the 96-cell receive buffer begins to fill, this mechanism allows low priority packets to be dropped at the ingress to this buffer. Each receive channel can be marked as low priority by setting the PRI bit in the receive configuration. The setting of the PRI_MODE bits in the Receive Address Select 0 register determines the discard behaviour based on the fill level of the buffer. This allows the user to tune the system to minimize cell loss.

6.3.5 Software Reset

The **FireStream155** implements two levels of Software Reset.

- Software Reset 0 has the same effect as a Hard Reset. All LRAM configuration data is lost.
- Software Reset 1 resets all **FireStream155** internal logic but leaves the LRAM data structures untouched.

6.3.6 Cell Loss Priority Control and Reporting

The Cell Loss Priority (CLP) bit within the ATM Cell header indicates the relative priority of the Cell. In the Transmit direction, the Host device has control over this bit (per channel) using the Set CLP and Reset CLP commands. By linking this command into the transmit data stream, the Host can control the CLP bit on a per buffer basis. The CLP of received data is reported via the CLP bit of the Receive Buffer Ready Queue. This bit is set if any of the cells within the packet associated with data buffer(s) for the queue entry were received with CLP=1.

6.3.7 Congestion Control and Reporting

Congestion within an ATM network is indicated via bit 1 of the PTI field in ATM cell header. In the Transmit direction, the Host device has control over this bit (per channel) using the Set Congestion and Reset Congestion commands. By linking this command into the transmit data stream, the Host can control the CLP bit on a per buffer basis. The Congestion state of received data is reported via the CI and CIL bits of the Receive Buffer Ready Queue. The CI bit is set if any of the cells within the data buffer(s) for the queue entry were received with PTI[1]=1, and the CIL bit reports the Congestion status of the last received cell of the packet.

6.3.8 Cells In Frames (CIF) Support

Position Mode can be used to aid the host in implementing Cells-In-Frames. On receive, any change in the cell header, or the reception of an OAM/RM cell can be used to terminate packet reception. On transmit, data and OAM/RM cells can be interleaved in the per-channel queue as can commands to alter the cell header.

6.3.9 LAN Emulation (LANE) Support

The Encapsulated Header function can be used to support LAN Emulation. This allows the Host to add a fixed header (of 1 to 12 bytes) onto each transmitted packet.

6.4 Data Buffer Management

Data buffers are used to transfer payload and control data between the Host and the **FireStream155**. Each data buffer has a descriptor associated with it. The descriptor formats are defined in paragraph 6.5 below.

6.4.1 Transmit Path Data Buffers

The Host may have limited control over transmit data buffers, therefore, there are few limitations placed upon these buffers. The minimum size of transmit data buffers is 1 byte and the maximum size is 65536 bytes.

There is no restriction on the memory alignment of Transmit data buffers (other than alignment on a byte boundary). Similarly there is no restriction on the size of data buffers other than those imposed on the AAL Packet length. This means that a single cell payload can straddle several buffers (up to a single buffer per byte). Note that a small buffer size will lead to a reduction in system performance, as will using buffers that are not D-Word aligned.

6.4.2 Receive Path Data Buffers

The Host generally has significant control of receive data buffers. A number of restrictions are defined to increase flexibility and reduce system performance impact. Receive data buffers are quad-word (8 byte) aligned and a multiple of 8 bytes. The minimum Receive data buffer size is 48 bytes and the maximum size is 65536 bytes. The **FireStream155** will only place an integer number of cells in a receive data buffer except for the last cell of a packet for which only the valid data is forwarded.

6.4.3 Buffer Free Pools

Buffer Free Pools are the mechanism by which the **FireStream155** obtains empty buffers on demand. A Buffer Free Pool is a linked list (in Shared Memory) of the descriptors associated with empty data buffers. The Host adds data buffers to the tail of the linked list when they become available, and the **FireStream155** removes buffers from the head of the linked list when required.

Receive data buffer sizes may be configured on a per pool basis. The **FireStream155** recognises the end of a Buffer Free Pool by comparing the Start and End addresses. The **FireStream155** supports two methods of indicating the fill level of a Buffer Free Pool. The first method of indicating the fill level uses the Nearly End of Linked List (NEOLL) bit in the descriptor control word to indicate that the Host should be alerted when the descriptor is being used by the **FireStream155**.

The second method of indicating the fill level uses count and update count registers to maintain the number of buffers in the Buffer Free Pool. When the Host adds to the Free Pool, it writes the number of buffers added to the Count Update register. The **FireStream155** increases the count register accordingly. When the **FireStream155** removes a buffer from the Buffer Free Pool, the count register is decremented. The method requires that the Host traverses chains to count the number of buffers before adding them to the Buffer Free Pool.

A Buffer Free Pool Underflow can occur when there are no available buffers available in a desired Buffer Free Pool. Where BFP Underflow occurs, the current packet is terminated, and passed to the Host via a Receive Buffer Ready Queue entry, indicating status of BFP Underflow. Where subsequent packets are discarded due to the BFP Underflow condition, an RBRQ entry is made for each packet discarded by the **FireStream155**.

The use of the Count/Count Update mechanism allows the Host to selectively discard data from low-priority channels when the number of buffers within a Free Pool falls below the programmed threshold.

The **FireStream155** implements a total of eight Buffer Free Pools. These Buffer Free Pools provide the system designer maximum flexibility, with respect to maximum memory efficiency, minimum bus utilization, and the ability to prioritize receive channels.

Free pools can be assigned to receive traffic in a flexible way so that memory and bus bandwidth efficiency maximized. Examples are given below:

- A single Buffer Free Pool could be set up containing buffers of 56 bytes. The **FireStream155** can then be programmed to place all OAM, Control and RM cells into data buffers from this Buffer Free Pool.
- The packet size profile may be known. i.e. 70% of packets contain less that 260 data bytes, and 30% are significantly larger. Two Buffer Free Pools may be set up, one containing buffers of size 280 bytes, and one containing significantly larger buffers. Each channel would then be programmed to write all data receive data to a 280 byte buffer, and if this overflows, then subsequent packet data is stored in a large buffer taken from a different Buffer Free Pool.
- Receive data can be targeted into different areas of host memory. If data received by the **FireStream155** is to be forwarded via a number of subsystems, each memory mapped into the main memory area, then the data can be sent direct to these systems.
- Two Buffer Free pools are allocated High and Low priority by the Host. The Host then ensures that the High Priority Buffer Free Pool always contains an adequate number of data buffers, possibly at the expense of the low priority pool. Each receive channel is allocated to the high or low priority Buffer Free Pool. If system resources become limited, the low priority Buffer Free Pool may become empty, and data may be lost on channels allocated to this pool.

6.5 Descriptor Format

A descriptor is an area of memory containing the linked list control information associated with a data buffer. Limited control information is also provided in the descriptor. A common descriptor format is defined, upon which the Transmit, Receive and Command descriptors are based.

The descriptor format is shown in Table 4. This common format allows easy re-use of descriptors between receive and transmit paths.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	CM			CD	EPI_CMOD	NEOLL	BPI					Reserved				Data Byte Count															
Next Descriptor Address																															
Buffer Start Address																															
AAL Control Field																Buffer Size															

Table 4 Descriptor Format

CM Cell Marker bits. Coded as shown in Table 5**.**

CM	Description
00	Normal Packet Data
01	RM Cell
10	OAM Cell (End to End)
11	OAM Cell (Segment)

Table 5 CM Coding

CD The Command / Data bit is set on transmit to indicate that the descriptor is associated with a command and cleared to indicate association with data.

EPI_CMOD End of Packet/Command Mode Indicator.

Data entries (CD reset), this is the End of Packet indicator. 0: Not End of Packet, 1: End of Packet.

Command entries (CD set), this is the Command Mode and defines the meaning of words 2 and 3. For CMOD set, the command(s) are within the data buffer defined by Buffer Start Address. For CMOD reset, the command entry is embedded within the descriptor. Further details can be found in the Command Descriptor Formats section.

NEOLL	**Receive Only** - Used by the Host on receive to mark the descriptor to generate an interrupt. This may be used to indicate that the Free Pool is nearly empty.
BPI	**Receive Only** - Buffer Pool Indicator. The Host may use this field as it remains unaltered by the **FireStream155** (except in Store and Forward mode). The field is commonly used to indicate to which Buffer Free Pool this descriptor belongs.
Data Byte Count	Range [1..65535] This field indicates the number of valid data bytes in the buffer pointed to by the descriptor. **Transmit** - In the transmit direction, this field always contains valid data. **Receive** - In Store & Forward mode, or in packet mode, where multiple buffers are required, the **FireStream155** writes to this field; Any previous value is overwritten.
Next Descriptor Address	This field is used by both the Host and the **FireStream155** device to generate linked lists of data buffers. The four LSB's are 0000 to ensure 16-byte alignment of descriptors. **Transmit** - The Host writes to this field to generate a linked list of data buffers, potentially for more than one AAL PDU, which is then passed to the **FireStream155** via a single Pending Queue entry. The **FireStream155** writes to this field to generate the Channel Queues when it is not used by the Host. **Receive** - In Packet mode, the **FireStream155** writes this field to generate a linked list of data buffers containing a single AAL PDU payload. In Streaming, Store & Forward and Position modes, the **FireStream155** does not write to this field as no linked lists are generated.
Buffer Start Address	This field points to the data buffer associated with the descriptor. This field is only written by the Host. For a receive or command descriptor, the 3 LSB's are 000 to ensure quad-word (8-byte) alignment of the receive data buffer.
AAL Control Field	The AAL control field is used to signal AAL specific control parameters to the **FireStream155**. This field contains the 16 bit AAL5 trailer control field and is written by the Host. The **FireStream155** inserts this field when transmitting (i.e. CPCS-UU and CPI bits). In Store & Forward mode, the **FireStream155** writes this field on receive. In other modes it does not write to this field.
Buffer Size	**Receive Only** - This field may be used to indicate the size of the data buffer to the **FireStream155** if the RBSVAL bit in the associated Buffer Free Pool Configuration register is not set.

6.5.1 Transmit Descriptor Format

The Transmit Descriptor is used to pass transmit data from the Host to the **FireStream155**. The CD bit is set to 0 to indicate a data buffer.

The Data Byte Count field is written by the Host to indicate the number of data bytes to be transmitted in the data buffer associated with the descriptor.

The Next Descriptor Address field is initially written by the Host in (multiple buffer) Packet mode. Where this field is unused by the Host (End of Packet, or Streaming), the **FireStream155** may write to it to form a Channel Queue.

The AAL Control Field is written by the Host only in certain circumstances. For an AAL5 channel, this field contains the AAL5 Control Field, which is inserted in the AAL5 PDU Trailer, and must contain valid data when this descriptor contains End of Packet indication i.e. the EPI_CMOD is set.

6.5.2 Command Descriptor Format

The Command Descriptor is a method of passing commands from the Host to the **FireStream155**. The CD bit is set to one to indicate that the descriptor relates to a command. If the CD bit is set, then the EPI_CMOD bit defines the Command Mode.

If the EPI_CMOD bit is set, the command is passed via a data buffer. The Data Byte Count is written by the Host, and defines the amount of valid data, and therefore the number of commands, in the Data Buffer. The Next Descriptor Address may be written by the Host device in order to pass a linked list of descriptors to the Host. The linked list may contain further command and/or data descriptors. This field may be written by the **FireStream155** whilst forming Channel Queues.

If the EPI_CMOD bit is reset, the command is embedded within the descriptor, as shown in Table 6. Words 2 and 3 of the descriptor are used to pass a reduced command entry (removing a level of indirection for linked commands). The format is suitable for commands with no or one parameter. The meaning of words 2 and 3 is as defined for Pending Queue entries. The next descriptor field may be used in the same way as described above.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	CM			CD	EPI_CMOD	NEOLL	BPI					Reserved				Data Byte Count															
Next Descriptor Address																															
Type		U		Control								Reserved				Channel Number															
Parameter 1																															

Table 6 Command-In-A-Descriptor Format

6.5.3 Receive Descriptor Format

Receive Descriptors are used by the **FireStream155** to pass received data to the Host.

The **FireStream155** obtains descriptors from one of the Buffer Free Pools, and writes receive data to the data buffer pointed to by the Receive Descriptor. The Receive Descriptor fields written to by the **FireStream155** depend upon the mode of operation.

The Data Byte Count field contains the number of valid bytes in the data buffer pointed to by the descriptor. It is only updated in Packet (Message) Mode (for all buffers except the last in a packet), and Store & Forward Mode. It is not written in Streaming Mode or Position Mode.

Therefore to minimize Host accesses, the **FireStream155** does not write any data to the Receive descriptor, apart from in Packet (Chaining) and Store & Forward modes.

The Next Descriptor Address is written only in Packet (Chaining) Mode, where a packet traverses more than one buffer.

The AAL Control Field is written by the **FireStream155** in Store & Forward Mode only.

A summary of write accesses to the receive descriptor is shown in Table 7.

Mode	Field	Validity
Packet - Single Buffer	Data Byte Count	Invalid - packet byte count in RBRQ entry
	Next Descriptor Address	Invalid
	AAL Control Field	Invalid - valid in RBRQ entry
Packet - Multiple Buffer	Data Byte Count	Valid for all except last buffer - indicates byte count for associated buffer
	Next Descriptor Address	Valid for all except last buffer
	AAL Control Field	Invalid - valid in RBRQ entry
Streaming, Position, CIF	Data Byte Count	Invalid - buffer byte count / packet byte count in RBRQ entry
	Next Descriptor Address	Invalid
	AAL Control Field	Invalid - valid in RBRQ entry
Store & Forward	Data Byte Count	Valid for all descriptors - indicates byte count for associated buffer.
	Next Descriptor Address	Invalid
	AAL Control Field	Valid

Table 7 Receive Descriptor Write Accesses

6.6 Command Management

6.6.1 Introduction

The Programming Interface defines a number of commands. There are a number of methods of passing and scheduling commands to the **FireStream155**, and of passing and returning command parameters.

Commands are passed to the **FireStream155** via a queue entry. The queue may be the High or Low priority Transmit Pending Queue, or the On-chip Transmit Pending Queue.

There are two scheduling mechanisms defined, Immediate and Linked (in-data sequence). Immediate Commands are executed as soon as they are encountered by the **FireStream155**. Linked Commands are added onto the appropriate Channel Queue by the **FireStream155** and are only executed when all data previously placed on the Channel Queue has been serviced.

Note that commands cannot be linked onto channels that are not enabled for transmit.

6.6.2 Passing Commands to the FireStream155

Commands are passed to the **FireStream155** via one of the Transmit Pending Queues, in the same manner in which transmit data is passed. The **FireStream155** will place an entry on the Command Status Queue (CSQ) for each queued command executed unless the NO_CSQ bit is set in the TPQ entry. If the command is passed using a Command Descriptor, the **FireStream155** makes two entries on the CSQ, one for the command itself, and one to return the pointer to the Command Descriptor to the Host.

Commands passed via the On-Chip Pending Queue are known as direct commands, and are treated in exactly the same way. Writing the 4th word into the On-Chip Pending Queue initiates command execution. The structures available to pass commands to the **FireStream155** are shown in Figure 10.

Command entries may be placed directly onto one of the Pending queues (Command-In-Queue). Alternatively, one or more commands maybe placed into a data buffer. The associated descriptor for the buffer is passed to the **FireStream155** via a pending queue entry (Command Via Descriptor). For commands with no or one parameter, the reduced command entry (8-bytes) maybe embedded in the descriptor (Command In a Descriptor).

6.6.3 Immediate Command Scheduling

Immediate Commands are executed as soon as they are encountered by the **FireStream155**. When the **FireStream155** encounters an Immediate Command, Pending Queue Processing is suspended until the command has been executed. Immediate commands may be passed to the **FireStream155** by any of the methods described above.

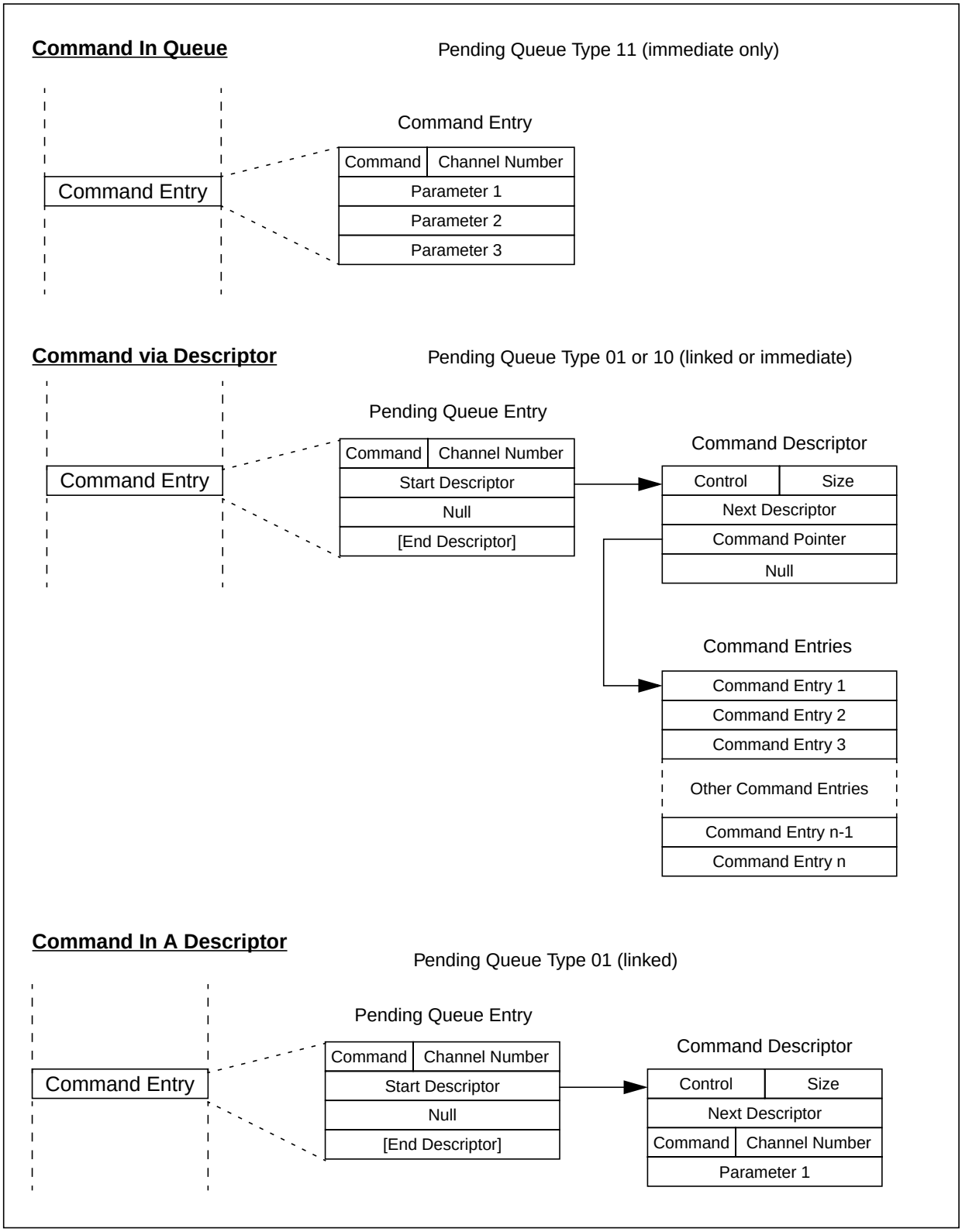

Figure 10 Passing Commands to the FireStream155

6.6.4 Linked Command Scheduling

Linked Commands are executed at a defined position with the Transmit Data sequence. When a Linked Command is encountered on a Transmit Pending Queue by the **FireStream155**, it is 'linked' onto the end of the Channel Queue for that channel. It will only be executed when all Transmit data and Commands previously scheduled for that channel have been actioned. Linked commands must be passed to the **FireStream155** via, or embedded within, a descriptor.

6.6.5 Command Parameters

Commands will generally have input and/or output parameters associated with them. Figure 11 shows two examples.

1 **Parameters In the Queue**. The Command Entry in the Transmit Pending Queue contains all command parameters.

2 **Parameters In Data Buffer**. In this case, one (or more) of the Command Parameters in the Command Entry is a pointer to a data buffer containing further parameters. The parameter data buffer must be 16-byte aligned.

These methods will also be used to pass return parameters from the **FireStream155** to the Host via a Status Queue entry.

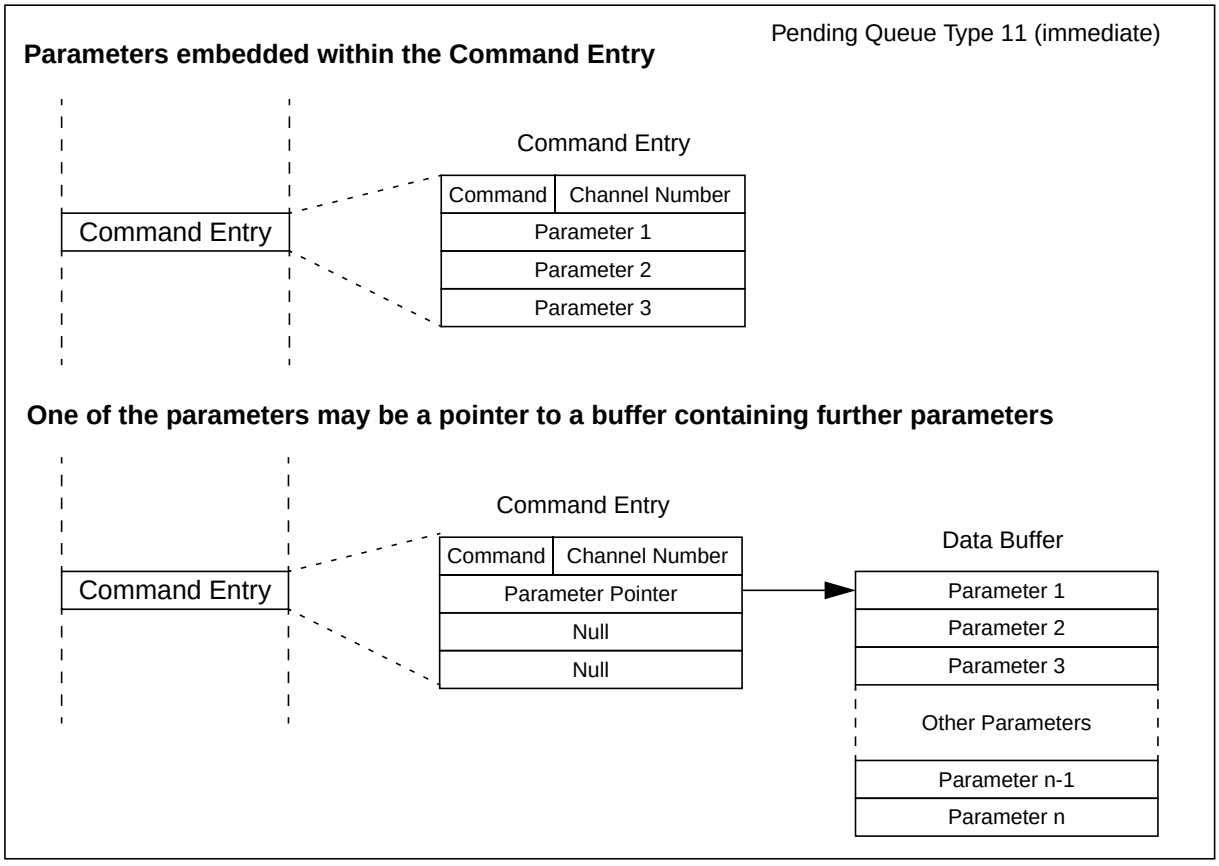

Figure 11 Passing Parameters to the FireStream155

6.7 Host -> FireStream155 Queue Formats

6.7.1 Introduction

A Host -> **FireStream155** queue is a FIFO structure that allows information to be passed from a Host to the **FireStream155**. The **FireStream155** supports two such queues to allow transmit data and commands to be passed from the Host to the **FireStream155**. They are a High Priority Transmit Pending Queue (HTPQ) and a Low Priority Transmit Pending Queue (LTPQ). The two priorities allow a Host device to ensure that high priority transmit data and commands are processed before and lower priority data or commands (e.g. CBR data vs UBR).

6.7.2 Common Transmit Pending Queue Entry Format

A common format for the pending queues is used, the format is shown in Table 8.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Type		T^1	U	Control						U		Reserved				Channel Number															
Type Specific Field #1																															
Type Specific Field #2																															
Type Specific Field #3																															

Table 8 Common Transmit Pending Queue Format

Type	This field defines the meanings of the type specific fields as described in Table 6 below.
T^1	Type Specific bit.
Control	This field is used for the Immediate and Command in Queue formats to indicate the command to be executed.
Channel Number	The channel number field indicates to which channel (if any) the entry relates.
Type Specific Fields	The contents of double-words 1 to 3 depend upon the value of the Type field and Control field in word 0. These are detailed in Table 6.

Type	Description	
00	**Transmit Data Entry**	
	T[1]	Unused
	Control	Unused
	Type Specific Field # 1	Start Descriptor Address
	Type Specific Field # 2	Reserved
	Type Specific Field # 3	End Descriptor Address
01	**Command Entry - Linked**	
	T[1]	Unused
	Control	Unused
	Type Specific Field # 1	Start Descriptor Address
	Type Specific Field # 2	Reserved
	Type Specific Field # 3	End Descriptor Address
10	**Command Entry - Immediate**	
	T[1]	Unused
	Control	Unused
	Type Specific Field # 1	Start Descriptor Address
	Type Specific Field # 2	Reserved
	Type Specific Field # 3	End Descriptor Address
11	**Command Parameters in Queue (immediate - parameters in entry)**	
	T[1]	No CSQ. When set this prevents a CSQ entry being generated when the command has completed.
	Control	Defines command to **FireStream155**
	Type Specific Field # 1	Command Parameter #1
	Type Specific Field # 2	Command Parameter #2
	Type Specific Field # 3	Command Parameter #3

Table 9 Transmit Pending Queue Entry Type and Type Specific Coding

6.7.3 Transmit Data Entry Queue Format

The Host adds a Transmit Data Entry onto a Pending Queue to schedule data for transmission. The Channel Number indicates the channel on which the data is to be scheduled. The Start Descriptor address points to the address of the first (or only) transmit descriptor to be scheduled. The End Descriptor Address points to the last Transmit Descriptor. Note that this field may be equal to the Start Descriptor Address which indicates a linked list of length 1. In Streaming Mode only the Start Descriptor Address is required.

6.7.4 Linked Command Entry Queue Format

The Host uses a Linked Command Entry to pass a Linked Command to the **FireStream155**. The Start Descriptor Address indicates the address of the start Command Descriptor. Linked Commands can be passed to the **FireStream155** as a linked list. The End Descriptor address field indicates the

address of the last descriptor in the linked list (and may be equal to the Start Descriptor Address). The linked list may contain other Linked Commands, and/or transmit data, but not Immediate Commands.

6.7.5 Immediate Command Entry Queue Format

The Host adds an Immediate Command Entry onto the Pending Queue to execute an Immediate Command, which resides in a buffer pointed to by a descriptor. The command is executed immediately by the **FireStream155**. The Channel Number field is not valid for some commands of this type. The Start Descriptor Address field points to the first Command Descriptor in a linked list, and the End Descriptor Address points to the last Command Descriptor in a linked list.

6.7.6 Immediate Command Entry Queue Format

The Host adds an Immediate Command Entry onto the Pending Queue to execute one or more Immediate Commands, which reside in a buffer pointed to by a descriptor. The command(s) is executed immediately by the **FireStream155**. The Channel Number field is not valid. The Start Descriptor Address field points to the first Command Descriptor in a linked list, and the End Descriptor Address points to the last Command Descriptor in a linked list.

6.7.7 Command In Queue

The command in queue format is used when a Host wishes to pass a single Immediate Command to the **FireStream155**. The number of valid parameters is implicit in the Command. Note that one (or more) of the parameters may be a data pointer, to a buffer containing further parameters.

6.7.8 NO_CSQ Operation

The NO_CSQ bit is valid for commands only. When set, the **FireStream155** will not generate a CSQ entry on completion of that command except where command completion fails.

6.8 FireStream155 -> Host Queues

6.8.1 Introduction

A **FireStream155** -> Host queue is a FIFO structure that allows information to be passed from the **FireStream155** to the Host. The **FireStream155** supports a Command Status Queue, a Transmit Buffer Release Queue and four Receive Buffer Ready Queues.

6.8.2 Common Status Queue Format

A common format for the status queues is used, the format is shown in Table 10.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Type		T^1	T^2	Status						T^3	Reserved					Channel Number															
Type Specific Field #1																															
Type Specific Field #2																															
Type Specific Field #3																															

Table 10 Common Status Queue Format

Type	This field defines the meanings of the Type Specific fields.
T^n	Type Specific bits.
Status	This field is used to indicate the status of the queue entry.
Channel Number	The channel number field indicates to which channel (if any) the entry relates.
Type Specific Fields	The contents of double-words 1 to 3 depend upon the value of the Type field and Status field in word 0. These are detailed in Table 11.

Type	Description	
01	**Command Status Entry - Parameters in entry**	
	T^1 - D	0 - Entry is returning command status
	T^2 - F	Set if command execution failed
	T^3	Unused
	Status	Status information
	Type Specific Field # 1	Return Parameter #1
	Type Specific Field # 2	Return Parameter #2
	Type Specific Field # 3	Return Parameter #3
	Command Status Entry - Parameters in data buffer	
	T^1 - D	0 - Entry is returning command status
	T^2 - F	Set if command execution failed
	T^3	Unused
	Status	Status information
	Type Specific Field # 1	Input Parameter Pointer
	Type Specific Field # 2	Output Parameter Pointer
	Type Specific Field # 3	Output / Input Parameter Data Buffer Byte Count
	Command Status Entry - Returning Command Descriptor	
	T^1 - D	1 - Entry is returning a descriptor
	T^2 - F	Set if command execution failed
	T^3	Unused
	Status	Status information
	Type Specific Field # 1	Command Descriptor Pointer
	Type Specific Field # 2	Null
	Type Specific Field # 3	Null
10	**Transmit Buffer Release Entry**	
	T^1	Unused
	T^2	Unused
	T^3	Unused
	Status	Status information
	Type Specific Field # 1	Start Descriptor Address
	Type Specific Field # 2	Byte Count
	Type Specific Field # 3	End Descriptor Address

Table 11 Status Queue Entry Type and Type Specific Coding

Type	Description	
11	**Receive Buffer Ready Entry**	
	T^1 - CI	The logical OR of the Congestion Indication bit of every cell in the received packet
	T^2 - CLP	The logical OR of the CLP bit of every cell in the received packet
	T^3 - CIL	The Congestion Indication bit of the last cell
	Status	Status information
	Type Specific Field # 1	Start Descriptor Address
	Type Specific Field # 2	AAL Specific / Byte Count
	Type Specific Field # 3	End Descriptor Address
00	Reserved	

Table 11 Status Queue Entry Type and Type Specific Coding

6.8.3 Command Status Queue Format

The **FireStream155** uses the Command Status Queue to pass status information, regarding executed commands, to the Host. There is a single Command Status Queue entry for every Command executed by the **FireStream155**, unless the NO_CSQ bit is set in the corresponding command entry. There will also be Command Status Queue entry for each command descriptor passed to the **FireStream155**. When the D bit is 0, the CSQ entry is providing Command Status and the F bit is valid. The Entry Status field defines the Command to which the CSQ entry relates, and will have the same coding as the Entry Control field for the Command.

6.8.4 Transmit Buffer Release Queue Format

The **FireStream155** uses the Transmit Buffer Release Queue (TBRQ) to pass transmit channel status information to the Host. There will be at least one TBRQ entry for each Transmit Data entry placed on the Pending Queues by the Host.

In Streaming mode, a TBRQ entry is made for each data buffer passed to the **FireStream155** via an entry on the Pending Queues. In Packet mode, a TBRQ entry is made for each AAL PDU passed to the **FireStream155** via an entry on the Pending Queues.

The Channel Number reports the channel on which data was transmitted, (or should have been transmitted). The Start Descriptor Address points to the descriptor of the data buffer which was transmitted, or to the descriptor of the first buffer of a linked list in packet mode.

The meaning of the Byte Count field varies with TBRQ entry status code. In Packet Mode, the value defines the total packet byte count, in Streaming Mode it defines the total number of bytes transmitted in this packet so far.

The End descriptor address is valid for Packet mode (End of Packet) only, and points to the last descriptor of the linked list.

The Transmit Status Queue Entry Status field is used in Transmit Buffer Release Queue entries and provides status information on transmitted data.

Transmit Status Code	Description
000000	Buffer sent OK - Streaming Mode - Not End of Packet
000001	Buffer sent OK - Streaming Mode - End of Packet
000010	Packet sent OK - Packet Mode - End of Single Buffer Packet
000011	Packet sent OK - Packet mode - End of Packet
000100	Cell sent OK - F5 OAM Cell Entry
000101	Reserved
000110	Cell sent OK - RM Cell Entry
000111	Reserved
001XXX	Reserved
010000	TX Packet Purged
010001	TX Channel Purged
010010	TX Packet Purged - No Descriptor
010011	TX Channel Purged - No Descriptor
010010 - 111111	Reserved

Table 12 Transmit Buffer Release Queue Entry Status

6.8.5 Receive Buffer Ready Queue Format

The **FireStream155** uses the Receive Buffer Ready Queues to pass received status information and data to the Host. The four Receive Buffer Ready Queues implemented on the **FireStream155** allow the Host to assign priority to receive data channels.

The Status field provides information regarding the data received, and also validates the contents of other fields within the structure. The Status codes are defined in Table 13. The Channel Number field defines which channel the data was received on. The Linked List Start Address field points to the Receive Descriptor associated with the receive data buffer(s).

For AAL5 channels, the AAL Specific field (which is the upper word of the Type Specific Field #2), contains the AAL5 Control field from the AAL5 CS-PDU trailer, and is only valid when the Status field indicates that this is the last entry for a packet.

The Byte count field (which is the lower word of the Type Specific Field #2), contains the number of bytes in the packet for Packet mode, and the number of bytes in the Receive Buffer in other modes.

The End Descriptor Address points to the Receive Descriptor pointing to the last data buffer of a packet, and is valid in packet mode only.

The CLP and CI bits are used to report the CLP and Congestion status of received data, and the CIL bit reports the CI bit of the last data cell.

The Receive Buffer Ready Queue Status Code is used in Receive Buffer Ready Queue Entries and provides Status information the received data associated with the entry.

6.8.6 Queue Overflow

If any of the **FireStream155** -> Host queues become full, any subsequent accesses to the queue will cause the last entry to be overwritten. To avoid loss of descriptors for receive data, the RBRQFI bit in the Statistics Configuration Register 0 can be set. This causes the Receive Buffer Manager to discard all cells that would cause an overflow write to a full RBRQ.

Receive Status Code	Description
000000	Buffer RX'ed OK - Streaming Mode, Not End of Packet
000001	Buffer RX'ed OK - Streaming Mode, End of Packet
000010	Buffer RX'ed OK - Packet Mode, Single Buffer Packet
000011	Buffer RX'ed OK - Packet Mode
000100	Buffer RX'ed OK - F4 OAM Cell (End to End)
000101	Buffer RX'ed OK - F4 OAM Cell (Segment)
000110	Buffer RX'ed OK - F5 OAM Cell (End to End)
000111	Buffer RX'ed OK - F5 OAM Cell (Segment)
001000	Buffer RX'ed OK - RM Cell
001001	Buffer RX'ed OK - TRANSP Cell
001010	Buffer RX'ed OK - TRANSPC Cell
001011	Unmatched Cell

Table 13 Receive Buffer Ready Queue Status Codes

Receive Status Code	Description
001100	Reserved
001101	Reserved
001110	Reserved
001111	Unrecognized Cell
010000	Reserved
010001	Re-assembly Abort - AAL5 Abort Cell RX'ed
010010	Packet Purged
010011	Packet Ageing Timeout
010100	Channel Ageing Timeout
010101	Calculated length Error
010110	Programmed length Limit Error
010111	AAL5 CRC32 Error
011000	OAM,TRANSP or TRANSPC CRC10 Error
011000	Reserved
011001	Reserved
011010	Reserved
011011	Reserved
011100	Reserved
011111	Re-assembly Abort - No buffers available
100000	Receive Buffer Overflow
100001	Change in GFC
100010	Receive buffer full
100011	Low priority discard - no receive descriptor
100100	Low priority discard - missing end of packet
100101-111111	Reserved

Table 13 Receive Buffer Ready Queue Status Codes

6.9 Command Descriptions

This section defines the operation and structure of all commands supported by the **FireStream155**.

In the following tables the following notation is used.

- U Indicates an unused bit. For the definition of unused see the Glossary (Appendix F).
- F in a status queue indicates PASS (Reset) or FAIL (Set) status of the command.
- All register numbers are offsets from the base address of the **FireStream155** in Host system memory.
- Reserved indicates a reserved bit. For the definition of reserved see the Glossary (Appendix F)

Number	Command	Overview	Code
1	C_NULL	NULL Command	000000
2	REG_RD	Register Read	000001
3	REG_RDM	Register Read Multiple	000010
4	REG_WR	Register Write	000011
5	REG_WRM	Register Write Multiple	000100
6	CONFIG_TX	Configure Transmit Channel	000101
7	CONFIG_RX	Configure Receive Channel	000110
8	PRP_RD	Peripheral (Expansion Port) Read	000111
9	PRP_RDM	Peripheral (Expansion Port) Read Multiple	101010
10	PRP_WR	Peripheral (Expansion Port) Write	001001
11	PRP_WRM	Peripheral (Expansion Port) Write Multiple	101011
12	RX_EN	Receive Channel Enable	001010
13	RX_PURGE	Receive Channel Purge	001011
14	RX_PURGE_INH	Receive Channel Purge and Inhibit	001100
15	TX_EN	Transmit Channel Enable	001101
16	TX_PURGE	Transmit Channel Purge	001110
17	TX_PURGE_INH	Transmit Channel Purge and Inhibit	001111
18	RST_CG	Reset Congestion Indication	010000
19	SET_CG	Set Congestion Indication	010001
20	RST_CLP	Reset Cell Loss Priority	010010
21	SET_CLP	Set Cell Loss Priority	010011
22	OVERRIDE	Override Packet Length	010100
23	ADD_BFP	Add to Buffer Free Pool	010101
24	DUMP_TX	Dump Transmit Channel Parameters	010110
25	DUMP_RX	Dump Receive Channel Parameters	010111
26	LRAM_RD	Local RAM Read	011000
27	LRAM_RDM	Local RAM Read Multiple	101000
28	LRAM_WR[a]	Local RAM Write	011001

Table 14 Firestream155 Command List

Number	Command	Overview	Code
29	LRAM_WRM[a]	Local RAM Write Multiple	101001
30	LRAM_BSET[a]	Local RAM Bit Set	011010
31	LRAM_BCLR[a]	Local RAM Bit Clear	011011
32	CONFIG_SEGM	Configure Segmentation Parameters	011100
33	READ_SEGM	Read Segmentation Parameters	011101
34	CONFIG_ROUT	Configure Routing Tag Parameters	011110
35	READ_ROUT	Read Routing Tag Parameters	011111
36	CONFIG_TM	Configure Traffic Manager Parameters	100000
37	READ_TM	Read Traffic Manager Parameters	100001
38	CONFIG_TXBM	Configure Transmit Buffer Manager Parameters	100010
39	READ_TXBM	Read Transmit Buffer Manager Parameters	100011
40	CONFIG_RXBM	Configure Receive Buffer Manager Parameters	100100
41	READ_RXBM	Read Receive Buffer Manager Parameters	100101
42	CONFIG_REAS	Configure Reassembly Parameters	100110
43	READ_REAS	Read Reassembly Parameters	100111

Table 14 Firestream155 Command List

a This command is inhibited and will return a 'fail' status unless the UNLOCK bit in SAR Mode Register 0 is set.

6.9.1 NULL Command

This command has no effect and no input or output parameters. It is used to test that the queuing mechanism is operational for debug purposes. A corresponding Status Queue entry is made when this command is encountered.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	U	U	NULL						U		Channel Number																			
Unused																															
Unused																															
Unused																															

Table 15 Null Command Pending Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	F	NULL						U		Channel Number																			
Unused																															
Unused																															
Unused																															

Table 16 Null Command Status Format

6.9.2 Register Read

This command performs a single register read. It takes a single input parameter, the register number of the register to be accessed. The register number and the register data are returned.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	U	U	Reg. Read						Unused																					
Register Number																															
Unused																															
Unused																															

Table 17 Register Read Command Pending Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	F	Reg. Read						Unused																					
Register Number																															
Register Data																															
Unused																															

Table 18 Register Read Command Status Format

6.9.3 Register Read Multiple

This command performs multiple register reads and has three input parameters. The 8-bit field Reads-1 specifies the number of register reads to perform. Setting this field to 0 causes a single read to occur. The Address Buffer Pointer parameter specifies a buffer that contains the register number of each of the registers to be read.

The format of the data in the Address Buffer is A_0,A_1,...$A_{(Reads-1)}$.

The Data Buffer Pointer parameter specifies a buffer where the read data from the register access is placed by the **FireStream155**. All parameters are returned to the Host. The data buffer contains the specified register contents. This data is contiguous in memory.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	U	U	Multiple Reg. Read						Unused														Reads-1							
Address Buffer Pointer																															
Data Buffer Pointer																															
Unused																															

Table 19 Register Read Multiple Command Pending Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	F	Multiple Reg. Read						Unused														Reads-1							
Address Buffer Pointer																															
Data Buffer Pointer																															
Unused																															

Table 20 Register Read Multiple Command Status Format

6.9.4 Register Write

This command performs a single register write. The command takes the register number of the register to be written, and the write data. The input parameters are returned.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	U	U	Reg. Write						Unused																					
Register Number																															
Register Data																															
Unused																															

Table 21 Register Write Command Pending Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	F	Reg Write						Unused																					
Register Number																															
Register Data																															
Unused																															

Table 22 Register Write Command Status Format

6.9.5 Register Write Multiple

This command performs multiple register writes and has two input parameters. The 8-bit field Writes-1 specifies the number of register writes to perform. Setting this field to 0 causes a single write to occur. The Address/Data Buffer Pointer parameter specifies a buffer that contains the register number of each of the registers to be written, and the 32-bit data to write.

The format of this data buffer is $A_0,D_0,A_1,D_1...A_{(Writes-1)},D_{(Writes-1)}$.

All parameters are returned to the Host.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	U	U	Multiple Reg. Write						Unused														Writes-1							
Address/Data Buffer Pointer																															
Unused																															
Unused																															

Table 23 Register Write Multiple Command Pending Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	F	Multiple Reg. Write						Unused														Writes-1							
Address/Data Buffer Pointer																															
Unused																															
Unused																															

Table 24 Register Write Multiple Command Pending Format

6.9.6 Transmit Configuration

This command completely configures a Transmit Channel. Input Parameters are passed via the Transmit Configuration parameter data buffer. The parameters are described below.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	U	U	Transmit Configure						U		Reserved				Channel Number															
Transmit Configuration Parameter Pointer																															
Unused																															
Unused																															

Table 25 Transmit Configuration Command Pending Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AAL			STR	ENC	Reserved	Reserved	Reserved	TTYPE		Calendar		Reserved	Reserved	Reserved	DLBM	Reserved										ATE	LP	CRC10	HV	Reserved	Reserved
ATM Header																															
TM Config 1																TM Config 0															
TM Config 3																TM Config 2															
TM Config 5																TM Config 4															
TM Config 7																TM Config 6															
Reserved								UTOPIA Address								HEC								UDF							
RTAG3								RTAG2								RTAG1								RTAG0							
RTAG7								RTAG6								RTAG5								RTAG4							
RTAG11								RTAG10								RTAG9								RTAG8							

Table 26 Transmit Configuration Data Buffer Format

Parameter	Description
AAL	AAL type. This 3-bit field that indicates the transmit channel AAL type. `000`: AAL5 `001`: Transparent Payload `010`: Transparent Cell `011`: Reserved `1XX`: Reserved

Table 27 Transmit Configuration Parameters

Parameter	Description	
STR	When set indicates that the channel is operating in Streaming Mode. When cleared, Packet Mode.	
ENC	Encapsulated Header (for values of TRTL > 0 only). When set indicates that an encapsulated header is to be placed at the beginning of the first cell of a packet. The size of the encapsulated header is given by the TRTL field of the SAR Mode 1 register.	
TType	Defines the Traffic Type. `00` : ABR `01` : CBR `10` : VBR `11` : UBR	
Calendar	Indicates which of the four calendars that the Channel is scheduled on. `00`: Calendar 0 `01`: Calendar 1 `10`: Calendar 2 `11`: Calendar 3	
ATE	Address Translation Enable (for use in Transparent Cell Mode only, also not available for use on ABR channels).If set indicates that the default (LRAM) ATM Cell header for the channel should be used for Transparent Cells in place of the ATM header field within the Transparent Cell data buffer.	
LP	LRAM PTI (for use in Transparent Modes only). If set specifies that the PTI field in Transmit Cells should be taken from the default cell header rather than derived by the **FireStream155**.	
CRC10	CRC-10 Enable (Transparent Modes only). If set specifies that last 10 bits of the payload data should be overwritten with a CRC-10 calculation.	
HV	HEC Valid. If set indicates that the default (LRAM) HEC value for the Channel should be used in Transmitted cells rather than the calculated HEC value.	
ATM Header	The default ATM Header (Excluding HEC) for the channel.	
TM Config 0	Traffic Manager Configuration 0. The meaning of this field is defined by the Traffic Type (TType) for the channel.	
	ABR This field represents the ICR	CBR, VBR, UBR This field represents the PCR

Table 27 Transmit Configuration Parameters

Parameter	Description	
TM Config 1	Traffic Manager Configuration 1. The meaning of this field is defined by the Traffic Type (TType) for the channel.	
	ABR Bit 15 : Unused Bits [14:12] : NRM Bit 11 : Unused Bits [10: 8] : MRM Bit 7 : Unused Bits [6: 4] : TRM Bits [3: 0] : Unused	VBR This field represents the SCR CBR, UBR This field is unused
TM Config 2	Traffic Manager Configuration 2. The meaning of this field is defined by the Traffic Type (TType) for the channel.	
	ABR Bits [15:12] : RDF Bits [11:10] : Unused Bits [9: 0] : ADTF	VBR Bits [15: 4] : Unused Bits [3: 0] : Binary fraction of SCR/PCR CBR, UBR This field is unused
TM Config 3	Traffic Manager Configuration 3. The meaning of this field is defined by the Traffic Type (TType) for the channel.	
	ABR This field is the MCR	VBR Bits [15: 8] : Unused Bits [7: 0] : Maximum Bucket Size CBR, UBR This field is unused
TM Config 4	Traffic Manager Configuration 4. The meaning of this field is defined by the Traffic Type (TType) for the channel.	
	ABR This field represents the PCR	VBR Bits [15: 8] : Unused Bits [7: 0] : Initial Bucket Fill Level CBR, UBR This field is unused
TM Config 5	Traffic Manager Configuration 5. The meaning of this field is defined by the Traffic Type (TType) for the channel.	
	ABR This field represents the RIFPCR (Product of RIF and PCR).	CBR, VBR, UBR This field is unused

Table 27 Transmit Configuration Parameters

Parameter	Description	
TM Config 6	Traffic Manager Configuration 6. The meaning of this field is defined by the Traffic Type (TType) for the channel.	
	ABR Bits [15: 8] : CRML (Lower 8-bits of CRM) Bits [7: 5] : CDF Bits [4: 3] : BRM generation strategy Bits [2: 0] : Group for congested destination	CBR, VBR, UBR This field is unused
TM Config 7	Traffic Manager Configuration 7. The meaning of this field is defined by the Traffic Type (TType) for the channel	
	ABR This field represents CRMU (Upper 16-bits of CRM field)	CBR, VBR, UBR This field is unused
For more detailed descriptions of the Traffic Manager parameters see section 7.4		
UTOPIA address	This defines the Transmit UTOPIA address in Level 2 ATM-layer Mode. This field is only used by the **FireStream155** if the DEF_HEC bit in SAR Mode Register 1 is set.	
UDF	This defines the UTOPIA User Defined Field.This field is only used by the **FireStream155** if the DEF_HEC bit in SAR Mode Register 1 is set.	
HEC	The defines the UTOPIA HEC byte. This field is only used by the **FireStream155** if the DEF_HEC bit in Mode Register 1 is set and the HV bit is set to 1.	
RTAG0-11	Defines the routing tag, or encapsulated header. The number of bytes is specified in the TRTL field of SAR Mode register 1.	

Table 27 Transmit Configuration Parameters

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	F	Transmit Configure						U		Reserved				Channel Number															
Transmit Configuration Parameter Pointer																															
Unused																															
Unused																															

Table 28 Transmit Configuration Command Status Format

6.9.7 Receive Configuration

This command configures a Receive Channel. The Receive Configure command format and parameters are shown below.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	U	U	Receive Configure						U		Reserved				Channel Number															
CRC10	HOAM	PRI	TRBRM	ML	AAL			TEP	TEVC	BFPP	BPS				RXBM_MODE	NAM	Reserved														
Unused																															
Unused																															

Table 29 Receive Configuration Command Pending Format

Parameter	Description
CRC10	CRC-10 Enable (transparent modes only). If set specifies that a CRC-10 calculation should be performed on received data cells.
HOAM	When set, indicates that OAM and RM cells should be forwarded to Host, otherwise they are discarded.
PRI	When set, indicates that this channel is eligible for discard if the fill level of the 96 cell buffer becomes greater than the allowable value (see Receive Address Select 0 Register)
TRBRM	This bit indicates that incoming FRM cells on this channel should be sent out as out of rate BRM cells by the Traffic Manager (TM). Used for uni-directional ABR channels (i.e. No corresponding Transmit channel configured). The RM cell is passed to the TM as a Transparent Cell, and the TM immediately forwards it for transmission.
ML	Maximum Length Enabled. When set this indicates that the maximum packet length check is to be performed for this channel. The maximum length is stored in the maximum packet length register.
AAL	Receive Channel AAL Type 000: AAL5 001: Transparent Payload 010: Transparent Cell 011: Reserved 1XX: Reserved

Table 30 Receive Configuration Parameters

Parameter	Description
TEP	Timeout Enable - Packet. If set enables the Receive packet ageing function. The current buffer is released if the packet is not received within the programmed time limit.
TEVC	Timeout Enable - Channel. If set enables the Receive channel ageing function. A buffer is released if the programmed inter-packet time interval is exceeded.
BFPP	Buffer Free Pool Priority. If set this indicates that the Channel is Low priority. This priority is used in Low Priority Discard Mode. In this mode a receive descriptor will only be allocated to the channel if there is a minimum number of buffers available.
BFPS	Buffer Free Pool Scheme. Defines which BFP is used by this channel. Table 31 shows the coding of this field.
RXBM_MODE	Receive Buffer Manager Mode 000: Packet, single buffer mode. 001: Cells in frames mode. 010: Packet, multiple buffer mode. 011: Reserved. 100: Streaming mode. 101: Reserved 110: Depending on PMS bit in SAR mode operation: 0: store and forward mode. 1: position mode. 111: Reserved
NAM	Non-Assured Mode (AAL5 only). If set, data from the last cell of a packet is provided to the host in the event of a CS trailer error, otherwise this data is discarded.

Table 30 Receive Configuration Parameters

BPS Code	Description	Receive Buffer Ready Queue
0000	Take buffers from BFP0.	0
0001	Take buffers from BFP1.	0
0010	Take buffers from BFP2.	1
0011	Take buffers from BFP3.	1
0100	Take buffers from BFP4.	2

Table 31 BPS Coding

BPS Code	Description	Receive Buffer Ready Queue
0101	Take buffers from BFP5.	2
0110	Take buffers from BFP6.	3
0111	Take buffers from BFP7.	3
1000	Take first buffer from BFP0, subsequent buffers from BFP1.	0
1001	Take first buffer from BFP2, subsequent buffers from BFP3.	1
1010	Take first buffer from BFP4, subsequent buffers from BFP5.	2
1011	Take first buffer from BFP6, subsequent buffers from BFP7.	3
1100	Take first buffer from BFP0, subsequent buffers from BFP7.	0
1101	Take first buffer from BFP2, subsequent buffers from BFP7.	1
1110	Take first buffer from BFP4, subsequent buffers from BFP7.	2
1111	Reserved	-

Table 31 BPS Coding

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	F	Receive Configure						U		Reserved				Channel Number															
Unused																															
Unused																															
Unused																															

Table 32 Receive Configuration Command Status Format

6.9.8 Read Peripheral

The **FireStream155** expansion port is configured such that the **FireStream155** can act as a bridge device between the Host System PCI Bus and a peripheral device (e.g. PHY device). These devices can be configured via the Read Peripheral and Write Peripheral Commands. This command reads a single word from the peripheral.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	U	U	Read Peripheral						Unused																					
FireStream155 Peripheral Address																															
Unused																															
Unused																															

Table 33 Read Peripheral Command Pending Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	F	Read Peripheral						Unused																					
FireStream155 Peripheral Address																															
Read Peripheral Data																															
Unused																															

Table 34 Read Peripheral Command Status Format

6.9.9 Read Peripheral Multiple

This command reads a specified number of words from the peripheral. It has three input parameters. The 8-bit field Reads-1 specifies the number of data words to read from the peripheral. Setting this field to 0 causes a single read to occur. These are read from contiguous locations starting at address **FireStream155** Peripheral Address. The read data is placed in the data buffer provided by Read Peripheral Data Buffer Pointer. All parameters are returned to the Host. The Read Peripheral Data buffer contains the Peripheral read data.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	U	U	Read Peripheral Multiple						Unused														Reads-1							
FireStream155 Peripheral Address																															
Read Peripheral Data Buffer Pointer																															
Unused																															

Table 35 Read Peripheral Multiple Command Pending Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	F	Read Peripheral Multiple						Unused														Reads-1							
FireStream155 Peripheral Address																															
Read Peripheral Data Buffer Pointer																															
Unused																															

Table 36 Read Peripheral Multiple Command Status Format

6.9.10 Write Peripheral

This command writes a single word to the **FireStream155** peripheral port. All parameters are returned to the Host.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	U	U	Write Peripheral						Unused																					
FireStream155 Peripheral Address																															
Write Peripheral Data																															
Unused																															

Table 37 Write Peripheral Command Pending Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	F	Write Peripheral						Unused																					
FireStream155 Peripheral Address																															
Write Peripheral Data																															
Unused																															

Table 38 Write Peripheral Command Status Format

6.9.11 Write Peripheral Multiple

This command writes a specified number of words to the **FireStream155** peripheral port. The Command has three input parameters. The 8-bit field Writes-1 specifies the number of words to write to the Peripheral. Setting this field to 0 causes a single write to occur. The data to be written is provided in a data buffer pointed to by the Write Peripheral Data Buffer Pointer. Data words are written into contiguous locations in the Peripheral starting at address **FireStream155** Peripheral Address. All parameters are returned to the Host.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	U	U	Write Peripheral Multiple						Unused														Writes-1							
FireStream155 Peripheral Address																															
Write Peripheral Data Buffer Pointer																															
Unused																															

Table 39 Write Peripheral Command Pending Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	F	Write Peripheral Multiple						Unused														Writes-1							
FireStream155 Peripheral Address																															
Write Peripheral Data Buffer Pointer																															
Unused																															

Table 40 Write Peripheral Command Status Format

6.9.12 Receive Enable

The Receive Enable command enables the specified Receive channel. It has a single parameter, the channel which should be enabled.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	U	U	Receive Enable						U		Reserved				Channel Number															
Unused																															
Unused																															
Unused																															

Table 41 Receive Enable Command Pending Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	F	Receive Enable						U		Reserved				Channel Number															
Unused																															
Unused																															
Unused																															

Table 42 Receive Enable Command Status Format

6.9.13 Receive Purge and Inhibit

The Receive Purge and Inhibit command purges and disables the specified Receive channel. All Receive buffers for that channel are returned to the Host via an RBRQ entry with status = purged. Any subsequent data received on that channel is discarded. The command has a single parameter, the channel which should be disabled. The Receive Purge and Inhibit Command has no return parameters.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	U	U	Receive Purge and Inhibit						U		Reserved				Channel Number																	
Unused																															
Unused																															
Unused																															

Table 43 Receive Purge and Inhibit Command Pending Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	F	Receive Purge and Inhibit						U		Reserved				Channel Number																	
Unused																															
Unused																															
Unused																															

Table 44 Receive Purge and Inhibit Command Status Format

6.9.14 Receive Purge

The Receive Purge command purges the current (if any) packet on the specified channel. All descriptors are immediately returned to the Host via a single RBRQ entry with status = purged. It has a single parameter, the Channel Number. This Command has no return parameters.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	U	U	Receive Purge						U		Reserved				Channel Number															
Unused																															
Unused																															
Unused																															

Table 45 Receive Purge Command Pending Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	F	Receive Purge						Reserved						Channel Number															
Unused																															
Unused																															
Unused																															

Table 46 Receive Purge Command Status Format

6.9.15 Transmit Enable

This command enables data transmission on the specified channel. The Transmit Enable command has a single parameter, the channel to be enabled. The Transmit Enable command has no return parameters.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	U	U	Transmit Enable						U		Reserved				Channel Number															
Unused																															
Unused																															
Unused																															

Table 47 Transmit Enable Command Pending Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	F	Transmit Enable						U		Reserved				Channel Number															
Unused																															
Unused																															
Unused																															

Table 48 Transmit Enable Command Status Format

6.9.16 Transmit Purge and Inhibit

A Per-Channel Transmit Purge and Inhibit. No further data is transmitted on the specified channel and all data and commands currently in the Channel Queue are discarded. All descriptors are returned to the Host via a single TBRQ entry with status = purged. An abort cell is transmitted if required. This command is used to close a channel and takes a single parameter, the channel number. It has no return parameters.

Note that there are special considerations required when using this command. Further details are provided in the **FireStream155** Frequently Asked Questions.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	U	U	Transmit Disable						U		Reserved				Channel Number															
Unused																															
Unused																															
Unused																															

Table 49 Transmit Purge and Inhibit Command Pending Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	F	Transmit Disable						U		Reserved				Channel Number															
Unused																															
Unused																															
Unused																															

Table 50 Transmit Purge and Inhibit Command Status Format

6.9.17 Transmit Purge

This command purges the specified Transmit channel. No further data for the current packet (if any) is transmitted, and the and descriptors are returned to the Host via a TBRQ entry with Status = Purged. Note that descriptors maybe returned one at a time (in Streaming Mode) or as a chain (in Packet Mode). An abort cell is transmitted if required. The Transmit Purge Command has a single parameter, the channel number. It has no return parameters.

Note that there are special considerations required when using this command. Further details are provided in the **FireStream155** Frequently Asked Questions.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	U	U	Transmit Purge						U		Reserved				Channel Number															
Unused																															
Unused																															
Unused																															

Table 51 Transmit Purge Command Pending Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	F	Transmit Purge						U		Reserved				Channel Number															
Unused																															
Unused																															
Unused																															

Table 52 Transmit Purge Command Status Format

6.9.18 Reset Congestion

This command sets the congestion bit (PTI[1]) to 0 on all cells transmitted on the specified channel. Note that this is the default case on power-up. The command has a single parameter, the Channel Number. It has no return parameters.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	U	U	Reset Congestion						U		Reserved				Channel Number															
Unused																															
Unused																															
Unused																															

Table 53 Reset Congestion Command Pending Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	F	Reset Congestion						U		Reserved				Channel Number															
Unused																															
Unused																															
Unused																															

Table 54 Reset Congestion Command Status Format

6.9.19 Set Congestion

This command sets the congestion bit (PTI[1]) to 1 on all cells transmitted on the specified channel. The command has a single parameter, the Channel Number. This Command has no return parameters.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	U	U	Set Congestion						U		Reserved				Channel Number															
Unused																															
Unused																															
Unused																															

Table 55 Set Congestion Command Pending Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	F	Set Congestion						U		Reserved				Channel Number															
Unused																															
Unused																															
Unused																															

Table 56 Set Congestion Command Status Format

6.9.20 Reset CLP

This command sets the CLP to 0 on all cells transmitted on the specified channel. Note that this is the default case on power-up. The command has a single parameter, the Channel Number. It has no return parameters.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	U	U	Reset CLP						U		Reserved				Channel Number															
Unused																															
Unused																															
Unused																															

Table 57 Reset CLP Command Pending Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	F	Reset CLP						U		Reserved				Channel Number															
Unused																															
Unused																															
Unused																															

Table 58 Reset CLP Command Status Format

6.9.21 Set CLP

This command sets the CLP bit to 1 on all cells transmitted on the specified channel. The command has a single parameter, the Channel Number. It has no return parameters.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	U	U	Set CLP						U		Reserved				Channel Number															
Unused																															
Unused																															
Unused																															

Table 59 Set CLP Command Pending Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	F	Set CLP						U		Reserved				Channel Number															
Unused																															
Unused																															
Unused																															

Table 60 Set CLP Command Status Format

6.9.22 Override Length

This command implements an override length function. This is used where the Host wishes to define the packet length field to be placed in the AAL Trailer, overriding the length parameter calculated by the **FireStream155**. This command has two input parameters, the Channel Number for which the Override length function is to be enabled, and the value for the Packet Length. This command has no return parameters

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	U	U	Override Length						U		Reserved				Channel Number															
Unused																Packet Length															
Unused																															
Unused																															

Table 61 Override Length Command Pending Format

.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	F	Override Length						U		Reserved				Channel Number															
Unused																															
Unused																															
Unused																															

Table 62 Override Length Command Status Format

6.9.23 Add Buffers to Free Pool

This command adds a number of buffers to the specified Buffer Free Pool, including updates to the count registers if required. The 16-bit field Count Update -1 specifies the number of buffers to be added. Setting this field to 0 causes a single buffer to be added. The command parameters are defined below. The command returns the total number of Buffers in the BFP. Note that this is only valid if the Host uses the **FireStream155** count update functionality.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	U	U	Add Buffers to BFP						BFP						Count Update -1															
New BFP End Address																															
Unused																															
Unused																															

Table 63 Add Buffers to Free Pool Command Pending Format

Parameter	Description
BFP	Defines the BFP to which buffers are to be added.
Count Update - 1	16-bit quantity defines the number of Buffers Added.
New BFP End Address	A pointer to the last descriptor in the BFP linked list.

Table 64 Add Buffers to Free Pool Parameters

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	F	Add Buffers to BFP						BFP						Count Update															
BFP Count																															
New BFP End Address																															
Unused																															

Table 65 Add Buffers to Free Pool Command Status Format

6.9.24 Dump Transmit Channel

This command dumps all LRAM data associated with a specified Transmit channel. All channel information is written to the data buffer provided by the Dump Channel data Buffer Pointer parameter. The Channel Dump information is written to the data buffer provided by Dump Channel Data Buffer Pointer. The format of data in this buffer is a snapshot of the LRAM data formed by the concatenation of the Segmentation, any relevant Routing Tags, TXBM, TM and LRAM parameters shown in Table 99, Table 100/Table 101, Table 96 and Table 102/Table 103.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	U	U	Dump Transmit Channel						U		Reserved				Channel Number															
Dump Channel Data Buffer Pointer																															
Unused																															
Unused																															

Table 66 Dump Transmit Channel Command Pending Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	F	Dump Transmit Channel						U		Reserved				Channel Number															
Dump Channel Data Buffer Pointer																															
Unused																															
Unused																															

Table 67 Dump Transmit Channel Command Status Format

6.9.25 Dump Receive Channel

This command dumps all LRAM data associated with a specified Receive channel. All channel information is written to the data buffer provided by the Dump Channel data Buffer Pointer parameter. The Channel Dump information is written to the data buffer provided by Dump Channel Data Buffer Pointer. The format of data in this buffer is a snapshot of the LRAM data formed by the concatenation of the RXBM and Reassembly LRAM parameters shown in Table 114 and Table 113.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	U	U	Dump Receive Channel						U		Reserved				Channel Number															
Dump Channel Data Buffer Pointer																															
Unused																															
Unused																															

Table 68 Dump Receive Channel Command Pending Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	F	Dump Receive Channel						U		Reserved				Channel Number															
Dump Channel Data Buffer Pointer																															
Unused																															
Unused																															

Table 69 Dump Receive Channel Command Status Format

6.9.26 Read LRAM

This command reads a single word from **FireStream155** LRAM.

Note that this command is a debug command only and should not be used under normal circumstances.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	U	U	Read LRAM						Unused																					
FireStream155 LRAM Address																															
Unused																															
Unused																															

Table 70 Read LRAM Command Pending Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	F	Read LRAM						Unused																					
FireStream155 LRAM Address																															
Read LRAM Data																															
Unused																															

Table 71 Read LRAM Command Status Format

6.9.27 Read LRAM Multiple

This command reads a specified number of words from **FireStream155** LRAM. The Command has three input parameters. The 8-bit field Reads-1 specifies the number of data words to read from LRAM. Setting this field to 0 causes a single read to occur. These are read from contiguous locations starting at address **FireStream155** LRAM Address. The read data is placed in the data buffer provided by Read LRAM Data Buffer Pointer. All parameters are returned to the Host. The Read LRAM Data Buffer now contains the LRAM read data

Note that this command is a debug command only and should not be used under normal circumstances.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	U	U	Read LRAM Multiple						Unused														Reads-1							
FireStream155 LRAM Address																															
Read LRAM Data Buffer Pointer																															
Unused																															

Table 72 Read LRAM Multiple Command Pending Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	F	Read LRAM Multiple						Unused														Reads-1							
FireStream155 LRAM Address																															
Read LRAM Data Buffer Pointer																															
Unused																															

Table 73 Read LRAM Multiple Command Status Format

6.9.28 Write LRAM

This command writes a single data word to **FireStream155** LRAM.

Note that as this command is a debug command only and should not be used under normal circumstances, it is disabled unless in Halt Mode or the UNLOCK bit is set.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	U	U	Write LRAM						Unused																					
FireStream155 LRAM Address																															
Write LRAM Data																															
Unused																															

Table 74 Write LRAM Command Pending Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	F	Write LRAM						Unused																					
FireStream155 LRAM Address																															
Write LRAM Data																															
Unused																															

Table 75 Write LRAM Command Status Format

6.9.29 Write LRAM Multiple

This command writes a number of data words to **FireStream155** LRAM. The Command has three input parameters. The 8-bit field Writes-1 specifies the number of words to write to LRAM. Setting this field to 0 causes a single write to occur. The data to be written is provided in a data buffer pointed to by the Write LRAM Data Buffer Pointer. Data words are written to contiguous locations in LRAM starting at address **FireStream155** LRAM Address. All parameters are returned to the Host.

Note that as this command is a debug command only and should not be used under normal circumstances, it is disabled unless in Halt Mode or the UNLOCK bit is set.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	U	U	Write LRAM Multiple						Unused														Writes-1							
FireStream155 LRAM Address																															
Write LRAM Data Buffer Pointer																															
Unused																															

Table 76: Write LRAM Multiple Command Pending Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	F	Write LRAM Multiple						Unused														Writes-1							
FireStream155 LRAM Address																															
Write LRAM Data Buffer Pointer																															
Unused																															

Table 77: Write LRAM Multiple Command Status Format

6.9.30 LRAM Bit Set

This command allows a user to set any bit(s) in **FireStream155** LRAM. The Command has two input parameters. The **FireStream155** LRAM Address is the address location on which the Bit Set operation is performed, and Data word defines which bits are set. The data is 'OR'ed with the current contents of the LRAM location specified. All parameters are returned to the Host.

Note that as this command is a debug command only and should not be used under normal circumstances, it is disabled unless in Halt Mode or the UNLOCK bit is set.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	U	U	LRAM Bit Set						Unused																					
FireStream155 LRAM Address																															
Data Word																															
Unused																															

Table 78 LRAM Bit Set Command Pending Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	F	LRAM Bit Set						Unused																					
FireStream155 LRAM Address																															
Unused																															

Table 79 LRAM Bit Set Command Status Format

6.9.31 LRAM Bit Clear

This command allows a user to Clear any bit(s) in **FireStream155** LRAM. The Command has two input parameters. The **FireStream155** LRAM Address is the address location on which the Bit Set operation is performed, and Data word defines which bits are cleared. The data is inverted and 'AND'ed with the current contents of the LRAM location specified. All parameters are returned to the Host.

Note that as this command is a debug command only and should not be used under normal circumstances, it is disabled unless in Halt Mode or the UNLOCK bit is set.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	U	U	LRAM Bit Clear						Unused																					
FireStream155 LRAM Address																															
Data Word																															
Unused																															

Table 80 LRAM Bit Clear Command Pending Format

.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	F	LRAM Bit Clear						Unused																					
FireStream155 LRAM Address																															
Data Word																															
Unused																															

Table 81 LRAM Bit Clear Command Status Format

6.9.32 Configure Segmentation

This command configures the Segmentation Parameters for the specified channel. This command has no return parameters. The format of data in this command is that of the LRAM data formed by the Segmentation LRAM parameters shown in Table 99.

Note that under most circumstances this command need not be used as all necessary parameters are set using the Transmit Configuration command.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	U	U	Config Segm						U		Reserved				Channel Number															
Packet Length																Reserved								SIP	ATE	LP	CRC10	HV	Reserved	Reserved	
CRC32																															
ATM Header																															

Table 82 Configure Segmentation Command Pending Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	F	Config Segm						U		Reserved				Channel Number															
Unused																															
Unused																															
Unused																															

Table 83 Configure Segmentation Command Status Format

6.9.33 Read Segmentation

This command reads Segmentation information for the specified channel. The Segmentation parameters are returned to the Host via Command-In-Queue format status entry.

6.9.34 Configure Routing Tag

This command configures the Routing Tag information for the specified channel. Up to 12 bytes of routing tag information are provided. This command has no return parameters. The format of data in this buffer is that of the LRAM data formed by the concatenation of the Routing Tag and Extended Routing Tag LRAM parameters shown in Table 100 and Table 101.

Note that under most circumstances this command need not be used as all necessary parameters are set using the Transmit Configuration command.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	U	U	Config Tag						U		Reserved				Channel Number															
Routing Parameter Data Buffer																															
Unused																															
Unused																															

Table 84 Configure Routing Tag Command Pending Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	F	Config Tag						U		Reserved				Channel Number															
Routing Parameter Data Buffer																															
Unused																															
Unused																															

Table 85 Configure Routing Tag Command Status Format

6.9.35 Read Routing Tag

This command reads the Routing Tag parameters for the specified channel. The command format is as for Configure Routing Tag command.

6.9.36 Configure Traffic Manager

This command configures the Traffic Manager (TM) parameters for the specified channel. The TM parameter data buffer is returned to the Host. The format of data in this buffer is that of the LRAM data formed by the Traffic Manager LRAM parameters shown in Table 102 or Table 111.

Note that under most circumstances this command need not be used as all necessary parameters are set using the Transmit Configuration command.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	U	U	Config TM						U		Reserved				Channel Number															
TM Parameter Data Buffer																															
Unused																															
Unused																															

Table 86 Configure TM Command Pending Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	F	Config TM						U		Reserved				Channel Number															
TM Parameter Data Buffer																															
Unused																															
Unused																															

Table 87 Configure TM Command Status Format

6.9.37 Read Traffic Manager

This command reads the Traffic Manager parameters for the specified channel. The command format is as for Configure Traffic Manager command.

6.9.38 Configure Transmit Buffer Manager

This command configures the Transmit Buffer Manager (TXBM) parameters for the specified channel. The TXBM Parameter data buffer is returned to the Host. The format of data in this buffer is that of the LRAM data formed by the Transmit Buffer Manager LRAM parameters shown in Table 96.

Note that under most circumstances this command need not be used as all necessary parameters are set using the Transmit Configuration command.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	U	U	Config TXBM						U		Reserved				Channel Number															
TXBM Parameter Data Buffer																															
Unused																															
Unused																															

Table 88 Configure Transmit Buffer Manager Command Pending Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	F	Config TXBM						U		Reserved				Channel Number															
TXBM Parameter Data Buffer																															
Unused																															
Unused																															

Table 89 Configure Transmit Buffer Manager Command Status Format

6.9.39 Read Transmit Buffer Manager

This command reads the Transmit Buffer Manager (TXBM) parameters for the specified channel. The command format is as for Configure TXBM command.

6.9.40 Configure Receive Buffer Manager

This command configures the Receive Buffer Manager (RXBM) parameters for the specified channel. The RXBM Parameter data buffer is returned to the Host. The format of data in this buffer is that of the LRAM data formed by the Receive Buffer Manager LRAM parameters shown in Table 114.

Note that under most circumstances this command need not be used as all necessary parameters are set using the Receive Configuration command.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	U	U	Config RXBM						U		Reserved				Channel Number															
RXBM Parameter Data Buffer																															
Unused																															
Unused																															

Table 90 Configure Receive Buffer Manager Command Pending Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	F	Config RXBM						U		Reserved				Channel Number															
RXBM Parameter Data Buffer																															
Unused																															
Unused																															

Table 91 Configure Receive Buffer Manager Command Status Format

6.9.41 Read Receive Buffer Manager

This command reads the Receive Buffer Manager (RXBM) Parameters for the specified channel. The command format is as for Configure RXBM command.

6.9.42 Configure Reassembly

This command configures the Reassembly Parameters for the specified channel. This command has no return parameters. The format of data in this command is that of the LRAM data formed by the Reassembly LRAM parameters shown in Table 113.

Note that under most circumstances this command need not be used as all necessary parameters are set using the Receive Configuration command.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	U	U	Config Reasm						U		Reserved				Channel Number															
CRC10	HOAM	PRI	ML	TRBRM	AAL			CE	DCD	RIP	EFCI	GFC				Packet Length															
CRC32																															
Unused																															

Table 92 Configure Reassembly Command Pending Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	F	Config Reasm						U		Reserved				Channel Number															
Unused																															
Unused																															
Unused																															

Table 93 Configure Reassembly Command Status Format

6.9.43 Read Reassembly

This command Reads Reassembly information for the specified channel. The Reassembly parameters are returned to the Host via Command-In-Queue format status entry. The command format is as for Configure Reassembly command.

7 Local Memory Organisation

The data in this section is provided for debug purposes and for detailed understanding of the local memory mapping. The user is not normally required to have an understanding of this information unless debugging using the memory dump commands is required.

7.1 Memory Organisation

Conceptually, all transmit, receive and traffic management parameters are stored together on a per channel basis. In reality, a more flexible way of storing the data is used. This allows different numbers of transmit and receive channels and optional storage for channels supporting ABR and for Routing Tags. This gives a more effective packing of data within the LRAM.

	Address	Storage Area
Base	0	Transmit Parameters
Index	cct *16	
Base	a = 16 * TXVCS	Receive parameters
Index	a + cct * 8	
Base	b = a + (8 * RXVCS)	ABR parameters
Index	b + cct * 4	
Base	c = b + (4 * ABRVCS)	Routing Tag parameters*
Index	c + cct * 2	
Base	d = c + (2 * TXVCS)	Extended Routing Tag parameters*
Index	c + cct * 2	
-	-	Some unused area
Base	w = x - (TXVCS / 32)	Slave Calendar Area
Index	x - (cct / 32)	
Base	x = y - (CALSUP * TXVCS / 32)	Master Calendar Area
Index	y - ((cal_no * TXVCS) + cct) / 32)	
Base	y = z - (CALSUP * TXVCS)	Calendar Pointers
Index	z - (cal_no * TXVCS) + cct	
Base	z = 2 ^ MEMSZ	Top of memory

Table 94 LRAM Organisation

where

- CCT is the channel number.
- TXVCS is the number of transmit channels supported. See SAR Mode Register 0 in Appendix B.
- ABRVCS is the number of ABR channels supported. See SAR Mode Register 0 in Appendix B.
- RXVCS is the number of receive channels supported. See SAR Mode Register 0 in Appendix B.
- CALSUP is the number of calendars used. See SAR Mode Register 0 in Appendix B.
- MEMSZ is the local memory size. See SAR Mode Register 0 in Appendix B.

* Note: The Routing Tag parameter storage area is optional and is dependent on the setting of TRTL and DEFHEC in SAR Mode Register 1.

Storage Area	Offset	Stored Parameter
Transmit Parameters	0-6	Transmit Buffer Manager (TXBM) parameters
	7-12	Traffic Manager (TM) parameters (except extra ABR)
	13-15	Segmentation (SEGM) parameters (except routing tag)
Receive Parameters	0-5	Receive Buffer Manager (RXBM) parameters
	6-7	Reassembly (REAS) parameters
ABR Parameters	0-3	Extra ABR parameters
Routing Tag Parameters	0-1	Routing Tag parameters
Extended Routing Tag Parameters	0-1	Extended Routing Tag parameters

Table 95 Mapping of Areas to Stored Parameters

7.2 Transmit Buffer Manager LRAM Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
End Descriptor Address																															
STATUS		OAM	AAL			STR	ENC	PV	S	M	OL	DCD	CLOSE	CLP	CI	CM or Buffer Length[15:14]		Buffer Length[13:0]													
Segmentation Pointer																															
Descriptor Address																															
AAL Control Field																Packet Length															
Next Descriptor Address																															
Packet Start Descriptor Address																															

Table 96 Transmit Buffer Manager LRAM Format

End Descriptor Address The field contains the address of the last descriptor on the current per-channel service queue. When new data is added to a channel, it is linked onto this descriptor by the TXBM, and this field is updated accordingly. This valid when the Channel Queue is not empty.

Status This two bit field indicates the Channel Queue Status. The coding of this field is defined in Table 97

STATUS code	Description
00	Empty Channel Queue. (End Descriptor, Descriptor and Next Descriptor Addresses invalid)
01	Channel Queue contains a single entry. (Descriptor and End valid, Next Invalid).
10	Channel Status Queue not empty (Descriptor and End valid, Next Invalid).

STATUS code	Description
11	Channel Status Queue not empty (Descriptor, Next and End valid).

Table 97 STATUS Coding

OAM This single bit field indicates whether the current descriptor (if any) is an OAM/RM cell (Set) or User Data (Reset).

When Set, the type of OAM field is defined by the top two bits of the Buffer Length field. The coding of these bits is as defined for the CM field in Table 5 and indicates whether the OAM cell is a RM cell, End to End OAM cell or Segment OAM cell

AAL AAL type. This 3-bit field that indicates the transmit channel AAL type. The coding of this field is defined in Table 98.

AAL Code	Description
000	AAL5
001	Transparent payload (TRANS)
010	Transparent cell (TRANSPC)
011	Reserved
100	Reserved
101	Reserved
110	Reserved
111	Reserved

Table 98 AAL Coding

STR When set indicates that the channel is operating in Streaming Mode. When reset, Packet Mode.

ENC Encapsulated Header (for values of TRTL > 0 only). When set indicates that an encapsulated header is to be placed at the beginning of the first cell of a packet. The size of the encapsulated header is given by the TRTL field of the SAR Mode 1 register.

PV	This single bit field indicates that the packet parameters for the current descriptor have been read form the Host and written to LRAM. The parameters validated by this bit are: • Buffer Length • OAM • M • Segmentation Pointer • AAL5 CNTL field
S	This bit indicates that segmentation has begun for the current packet. This bit is controlled by the TXBM.
M	If reset indicates that this is the last packet in streaming and chaining modes. If set indicates that there is further data to come. This bit is controlled by the TXBM.
OL	When set the Override Length bit indicates that the calculated packet length should not be used. Instead, the packet length is provided by the Host. This bit is set by the Override Length command, and the reset by the TXBM at the end of the current (or next in the case of an empty channel queue) packet.
DCD	When set, the TXBM will purge the current packet, and send an abort cell if required. This bit is set by the Transmit Purge command, and reset by the TXBM when it has been actioned.
Close	When set, the TXBM will purge all queued data, and send an abort cell if required. This bit is set by the Transmit Purge and Inhibit command, and reset by the TXBM when it has been actioned.
CLP	Defines the CLP bit of all cells transmitted on this channel. This bit is controlled by the set/clear CLP commands.
CI	Defines the Congestion Indication bit (PTI[1]) of all cells transmitted on this channel. This bit is controlled by the set/clear CI commands.
Buffer Length	For User Data, all 16 bits of this field indicate the number of valid data bytes in the current buffer. Initialized per packet, and updated by the TXBM every time a cell is transmitted. Note: For OAM cells (OAM Set), the bits 15 and 14 define the CM field. Bits 13 to 0 define the number of bytes in the data buffer associated with the current descriptor. Note that this implies that the maximum number of OAM cells that can be passed to the **FireStream155** in a single buffer is 341 (2^14/48).
Segmentation Pointer	This field is used by the TXBM to store the absolute address within the data buffer, from which the next cell of data is to be read.It is initialized to the Buffer Start Address (read from the Transmit Descriptor) when packet segmentation starts, and updated after every channel service.

Descriptor Address	This field contains the address of the current descriptor, and is valid when the channel is not empty.
Packet Length	This field is used to store the accumulated packet length calculation when OL reset, or the override packet length (provided by the Host) when OL set.
AAL5 Control Field	In AAL5 mode, this field contains the 16-bit AAL5 control field that is placed in the CS-PDU trailer. This data is defined on a per-packet basis form the Transmit Descriptor.
Next Descriptor Address	The field contains the address of the next descriptor on a per-channel service queue. This field is valid when the NV bit is set.
Packet Start Descriptor Address	This field contains the address of the first descriptor of a chain in Packet Mode. Unused in Streaming Mode.

7.3 Segmentation / Routing Tag LRAM Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Packet Length																Reserved								SIP	ATE	LP	CRC10	HV	Reserved	Reserved	
CRC32																															
ATM Header																															

Table 99 Segmentation LRAM Format

Packet Length The length of the current packet as calculated by the Segmentation Process. This field will be inserted in the CS-PDU trailer.

SIP Send In Progress. The length of the current packet as calculated by the Segmentation Process. This field will be inserted in the CS-PDU trailer.

ATE Address Translation Enable (Transparent Cell Mode only).If set indicates that the default (LRAM) ATM Cell header for the channel should be used for Transparent Cells in place of the ATM header field within the Transparent Cell data buffer.

LP LRAM PTI (Transparent Modes only). If set specifies that the PTI field in Transmit Cells should be taken from the default cell header rather than derived by the **FireStream155**.

CRC10 CRC-10 Enable (Transparent Modes only). If set specifies that last 10 bits of the payload data should be overritten with a CRC-10 calculation.

HV HEC Valid. If set indicates that the default (LRAM) HEC value for the Channel should be used in Transmitted cells rather than the calculated HEC value.

CRC32 In AAL5 mode, this field is used to store the partial CRC32 calculations for a packet.

ATM Header This field contains the ATM header data for the channel.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								UTOPIA ADDR								HEC								UDF							
RTAG0								RTAG1								RTAG2								RTAG3							

Table 100 Routing Tag LRAM Format

UTOPIA ADDR This defines the Transmit UTOPIA address in Level 2 ATM-layer Mode. This field is only used by the **FireStream155** if the DEF_HEC bit in SAR Mode Register 1 is set.

UDF This defines the UTOPIA User Defined Field.This field is only used by the **FireStream155** if the DEF_HEC bit in SAR Mode Register 1 is set.

HEC The defines the UTOPIA HEC byte. This field is only used by the **FireStream155** if the DEF_HEC bit in SAR Mode Register 1 is set and the HV bit is set to 1.

RTAG0 to RTAG3 Defines the routing tag, or encapsulated header. Defines the routing tag, or encapsulated header. The number of bytes is specified in the TRTL field of SAR Mode register 1. This field contains the routing tag data.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTAG4								RTAG5								RTAG6								RTAG7							
RTAG8								RTAG9								RTAG10								RTAG11							

Table 101 Extended Routing Tag LRAM Format

RTAG4 to RTAG11 Defines the routing tag, or encapsulated header. The number of bytes is specified in the TRTL field of SAR Mode register 1. This field contains the extended routing tag data.

7.4 Traffic Manager LRAM Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TType		Calendar		VCstate			Data_avl	Timed	TRM			BSent	BCount			LinkVC															
CCR																FRMTS															
Datats																Reserved	NRM			Reserved	MRM			NC							
MCR																RDF				Reserved	ADTF										
RIFPCR																PCR															
Reserved																ICR															

Table 102 Traffic Manager LRAM Format: ABR parameters.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRMU																CDF			Reserved												
CRML								NF																							
NI	CI	EFCI	Reserved								BMode	ERGroup	BRMCCR																		
BRMER																BRMCCR															

Table 103 Traffic Manager LRAM Format: Additional ABR parameters.

TTYPE Traffic type as shown in Table 104.

TTYPE	meaning
00	abr
01	cbr

Table 104 TTYPE encoding

TTYPE	meaning
10	vbr
11	ubr

Table 104 TTYPE encoding

Calendar Indicates in which of the four calendars the channel is entered.

VCState State of the channel which determines the behaviour of the TM during servicing/rescheduling.

Data_avl Data available. Set when the channel has received a new data indication. Cleared after reset or when the channel has become empty.

Timed True when the ADTF time period has elapsed since the last FRM cell was sent.

TRM ABR Variable - Time required to elapse after which an FRM cell must be sent if at least MRM (= 2) data cells have been sent. trm values are calculated against the upper 16 bits of the 22 bit TM timestamp. Since the lower 6 bits are not used, the inherent granularity is 2^6 *2.73u = 174us

TRM code	TRM value /ms	TRM code	TRM value /ms
000	0.78125	100	12.5
001	1.5625	101	25
010	3.125	110	50
011	6.25	111	100

Table 105 TRM Encoding

BSent Set if no BRM cell has been sent since the last in-rate FRM cell.

BCount A count recording the total number of BRM cells that have been sent out on this channel as a result of receiving an FRM cell to turnaround.

LinkVC Channel number of next entry in linked list in the calendar table.

CCR ABR Variable - Current Cell Rate. Indicates rate at which cells are to be scheduled on this channel.

FRMTS Time stamp from when the last in rate FRM cell was sent.

DataTS Time stamp to show when next cell should be sent or the fraction number of time slots remaining from the last scheduling (higher rate channels). Contains time that the channel was last serviced if the channel is waiting for a possible ADTF timeout.

NRM ABR Variable - Controls the number of cells allowed on a channel before an FRM cell must be sent.

NRM	Cells sent for every FRM cell	NRM	Cells sent for every FRM cell
000	2	100	32
001	4	101	64
010	8	110	128
011	16	111	256

Table 106 NRM Encoding

MRM Controls the minimum number of data cells that must be sent between consecutive FRM cells on a given channel

MRM	Minimum cells between FRM cells	MRM	Minimum cells between FRM cells
000	1	100	16
001	2	101	32
010	4	110	64
011	8	111	128

Table 107 MRM Encoding

NC Number of in-rate cells sent since last FRM (includes the FRM itself).

MCR ABR Variable - Minimum Cell Rate. Indicates lower bound on CCR.

RDF Rate decrease factor which determines the minimum factor decrease imposed on CCR after receiving a BRM cell.

RDF code	RDF value	RDF code	RDF value
0000	1	0101	1/32
0001	1/2	0110	1/64
0010	1/4	0111	1/128
0011	1/8	1000	1/256
0100	1/16	1001 - 1111	1/512 (mantissa accuracy limit)

Table 108 RDF Encoding

ADTF Timeout value. This time is compared to the subtraction of the TM timestamp - FRMTS. If the time indicated by the ADTF setting elapses between consecutive RM cells, the current cell rate will be reduced to initial cell rate (ICR).

RIFPCR The product of ABR parameters RIF and PCR which determines the permitted increase in CCR, after receiving a BRM cell.

PCR ABR Variable - Peak Cell Rate. This indicates upper bound on CCR.

ICR ABR Variable - Initial Cell Rate. This indicates rate at which cells are initially scheduled on this channel.

CRMU, CRML Upper and lower portions of the CRM timeout limit. This limit is an upper bound on the number of FRM cells that should be sent in the absence of a source generated BRM cell before a decrease on CCR is imposed.

CDF Cut-off decrease factor. This determines the minimum factor decrease imposed on CCR if required before an FRM is sent.

cdf code	CDF value	cdf code	CDF value
000	1	100	1/16
001	1/2	101	1/32
010	1/4	110	1/64
011	1/8	111	0 (No Reduction)

Table 109 CDF encoding

NF Number of NRM cells sent since last BRM with BN = 0 (i.e. from destination).

NI No increase bit from last BRM cell.

CI Congestion Indication bit received in last BRM cell.

EFCI EFCI state of most recent received data cell.

BMODE BRM mode - defines the method of FRM turnaround for this channel.

BMODE code	Turnaround operation on receiving an FRM
00	Schedules an in-rate (CLP=0) BRM with the new data. On sending BRM, bcount is reset to zero. [TM 4.0 Appendix I.7.1 behaviour 3]
01	Schedules an in-rate (CLP=0) BRM with the new data and increments bcount. On sending BRM, bcount is decremented by one. BRM's are sent until bcount = 0. [TM 4.0 Appendix I.7.1 behaviour 4]
10	Sends an out-of-rate (CLP=1) BRM cell with the new FRM data (this FRM cell). Schedules an in-rate (CLP=0) BRM with the new FRM cell data. On sending BRM, bcount is reset to zero. [TM 4.0 Appendix I.7.1 behaviour 1]
11	Sends an out-of-rate (CLP=1) BRM cell with the old FRM data from LRAM (last FRM cell). Schedules an in-rate (CLP=0) BRM with the new FRM cell data. On sending BRM, bcount is reset to zero. [TM 4.0 Appendix I.7.1 behaviour 2]

Table 110 BMODE Encoding

ERGroup Defines the group to which this channel belongs. The configuration of the ABR congested destination register determines the function of each group when turning around FRM cells. This determines the modification applied to the CI and NI bits and the BRMER fields in the BRM cell to be sent out on this channel.

BRMCCR Current cell rate to be inserted in next BRM cell.

BRMER Explicit cell rate ready to go in next BRM cell. Modified from the ER field in the received FRM cell, as defined by the value of ERGroup and ABR Congested Destination register setting.

BRMMCR Minimum cell rate to be inserted in next BRM cell.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TType		CNum		VCState			Reserved	MBS								LinkVC															
SCR																PCR															
Datats																Time Fraction				Token Fraction				Tokens							
Reserved																Reserved												CR Ratio			
Reserved																Reserved															
Reserved																Reserved															

Table 111 Traffic Manager LRAM Format: CBR/VBR/UBR traffic.

Variables as defined in Table 102 but with the following additions;

CR Ratio Cell rate ratio. Set by the user for VBR traffic and is the binary fraction of SCR/PCR to 4 significant figures. This is coded as the digits of a binary fraction after the point. The example in Table 112 shows a CR Ratio value of 1/4 + 1/8 = 3/8 (0.0110 in binary).

1/2	1/4	1/8	1/16
0	1	1	0

Table 112 cr_ratio coding example

SCR Sustainable Cell Rate. For CBR, SCR and PCR should be set at the same value.

MBS Maximum Bucket Size; For a VBR channel, indicates the maximum number of cells that can be held in the bucket. The burst size is determined by the MBS and cr_ratio settings.

Tokens (IBF) Current total of tokens accumulated on this channel. If set by the user using the IBF parameter, this value is used as the initial fill level of the VBR bucket.

Time Fraction	The fraction number of time slots that remained from the calculations last time the channel was scheduled.
Token Fraction	The fraction number of tokens remaining from the last time the channel was scheduled.

7.5 Reassembly LRAM Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC10	HOAM	PRI	ML	TRBRM	AAL			CE	DCD	RIP	EFCI	GFC				Packet Length															
CRC32																															

Table 113 Reassembly LRAM Format

CRC10 CRC-10 Enable (transparent modes only). If set specifies that a CRC-10 calculation should be performed on received data cells.

HOAM Host OAM. When Set, indicates that OAM and RM cells should be forwarded to the Host, otherwise they are discarded.

PRI Priority Discard. When set, indicates that this channel is eligible for discard if the fill level of the 96 cell buffer becomes greater than the allowable value (see Receive Address Select 0 Register)

ML Maximum Length Enabled. When set this indicates that the maximum packet length check is to be performed for this channel. The maximum length is stored in the maximum packet length register.

TRBRM Turnaround FRM. This bit indicates that FRM cells on this channel should be sent out as out of rate RM cells by the TM. It is used for unidirectional ABR channels (i.e. No corresponding TX channel setup). The RM cell is passed to the Traffic Manager as a Transparent Cell, and the TM immediately forwards it to the Segmentation Module.

AAL AAL Type. This indicates the AAL type for the channel. This field is coded as shown in Table 98

CE Channel Enable. This enables or disables data on the receive channel. When disabled, all receive data for this channel is discarded. This bit is set by the host via the Enable RX channel command. When set, the device will begin reassembly at the start of the next new packet.

DCD Discard Cells For Current Packet. When set indicates that data for the current packet should be discarded.

RIP Reassembly In Progress, This is used by the to indicate that reassembly is in progress for the current channel. This bit will be used whilst a channel is disabled to ensure a clean start-up (i.e. Reassembly begins at beginning of next packet).

EFCI Explicit Forward Congestion Indication. Stored value is that of the previous data cell. Allows the Reassembly Module to inform the Traffic Manager of changes in the EFCI bit in received cells for this channel.

GFC	Generic Flow Control. This field is used to store the GFC field of the previous cell. This allows the Host and/or the Traffic Manager to be notified of any changes in the GFC of received cells on the current channel.
Packet Length	This field is used by the reassembly process to keep a running total of the current packet length.
CRC32	In AAL5 mode, this field is used to store the partial CRC32 calculation between cells.

7.6 Receive Buffer Manager LRAM Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MODE			NAM	D	DCD	TEP	TEVC	DP	CI	CLP	BFPP	BFPS				Timestamp Value															
Buffer Size																Buffer Bytes Received														
Reassembly Pointer																															
Descriptor Address																															
Start Descriptor Address (Store and Forward Mode: Buffer Start Address)																															
Younger Channel																Older Channel														

Table 114 Receive Buffer Manager LRAM Format

MODE

The modes of operation are shown in Table 115. A brief summary of each mode is shown below:

- Packet, Single Buffer: a complete AAL PDU is stored in a single buffer and returned via a Status Queue entry. If it is too large to fit into the buffer, packet reassembly is aborted and the buffer is returned to the Host via a Status Queue entry, indicating and error status.
- Packet, Multiple Buffer: the data is returned to the host only when a complete AAL PDU is received. this may span multiple buffers that are linked together.
- In all modes, OAM cells are passed back to the host via separate Status Queue entries.
- Streaming: a Status Queue entry is made either when a buffer is full or a complete AAL PDU has been received.
- Store and Forward: similar to streaming mode except that the position of non-payload cells (e.g. OAM cells) is maintained within the receive stream. This is done by releasing the current (partial) packet to the host when an OAM cell is received. However because the data is released before the end of packet, the packet length may be incorrect as invalid bytes may have been counted in the released buffer.
- Position: similar to store and forward mode except that the payload data is only release upon the reception of the following cell. This ensures that the packet length is correct.
- Cells in Frames: this operates in the same way as store and forward mode except a Status Queue entry is made on a change in the header due to CLP, CI or GFC change (as well as upon the reception of an OAM and an RM cell).

MODE	Operation
000	packet, single buffer mode.
001	cells in frames mode.
010	packet, multiple buffer mode; start descriptor address invalid. (INITIAL SETTING)
011	packet, multiple buffer mode; start descriptor address valid.
100	streaming mode.
101	reserved
110	Depending on PMS bit in SAR mode operation: 0 - store and forward mode. 1 - position mode, last cell was not an OAM cell. (INITIAL SETTING)
111	PMS = 0: reserved PMS = 1: position mode, last cell was an OAM cell.

Table 115 Receive Modes Of Operation

NAM Non-Assured Mode (AAL5 only). If set, data from the last cell of a packet is provided to the host in the event of a CS trailer error, otherwise this data is discarded.

D Channel Discard. When set indicates that a purge inhibit command is being actioned. The RXBM will discard all unwanted data from the 96 cell Receive Buffer.

DCD Discard Cells for current packet bit is set by the RXBM to indicate that all further data for this packet is to be discarded. This bit is set either due to an error condition (e.g. packet ageing timeout) or the purge command.

TEP Timeout Enable - Packet. If set enables the Receive packet ageing function. The current buffer is released if the packet is not received within the programmed time limit.

TEVC Timeout Enable - Channel. If set enables the Receive channel ageing function. A buffer is released if the programmed inter-packet time interval is exceeded.

DP	Descriptor Present bit indicates that the reassembly pointer field contains valid data.The parameters validated by this bit are: • Buffer Size • Start Descriptor Address • Reassembly Pointer
CI	CI bit record for current packet. This bit is the current value of the 'OR' of all the CI bits received in the current packet.
CLP	CLP bit record for current packet. This bit is the current value of the 'OR' of all the CLP bits received in the current packet.
BFPP	Buffer Free Pool Priority. If clear this bit indicates that the Channel is Low priority. This priority is used in Low Priority Discard Mode. In this mode a receive descriptor will only be allocated to the channel if there is a minimum number of buffers available. This value is programmed by the host, and is the same value as that used for the Buffer Free Pool nearly empty interrupt (specified in the Buffer Free Pool Configuration register).
BFPS	Buffer Free Pool Scheme. Defines which BFP is used by this channel. Table 31shows the coding of this field. The coding 1XXX allows a user to implement a S(mall), M(edium), L(arge) buffer scheme.
Timestamp Value	This field is used to store a timestamp for use in the buffer/channel ageing functions.
Buffer Size	This field is used to store the size of the current buffer. It is set to the buffer length when a new Receive Descriptor is read, and is valid when the DP bit is set.
Buffer Bytes Received	This field is used to keep a track of bytes placed in the current buffer. It is initialized to zero when the RXBM acquires a new receive descriptor.
Reassembly Pointer	This field is used to store the current reassembly pointer. It is initialized to point to the beginning of a data buffer when a new receive descriptor is acquired, and updated when new data is added to the buffer.
Descriptor Address	This field contains the address of the current descriptor.
Start Descriptor Address	In Packet, Multiple Buffer mode it is used to store the address of the first descriptor in the chain. It is valid when DP is active. In Store and Forward mode it is used to store the address of the current buffer. This is the address that is written back to the Receive Descriptor when the payload data has been written to the host memory.

Younger Channel	Used for the Packet Ageing and VC Ageing functionality. This field contains the channel that is younger than this in the same queue (either the Packet Ageing queue or the VC Ageing queue).
Older Channel	Used for the Packet Ageing and VC Ageing functionality. This field contains the channel that is older than this in the same queue (either the Packet Ageing queue or the VC Ageing queue).

INTENTIONALLY

LEFT

BLANK

A Register Map

A.1 PCI Configuration Registers

Notes:

- All registers are accessed by PCI configuration cycles.
- Access type "E" denotes registers loadable using the EEPROM interface.

Number	Offset (Hex)	Description	Access
0	00	Device ID / Vendor ID	R/E
1	04	Status / Command	R/W
2	08	Class Code / Revision ID	R/E
3	0c	Header Type / Latency Timer / Cache Line Size	R/W[a]
4	10	Memory Base Address Register	R/W
5	14	Reserved	-
6	18	Reserved	-
7	1c	Reserved	-
8	20	Reserved	-
9	24	Reserved	-
10	28	Reserved	-
11	2c	Subsystem ID / Subsystem Vendor ID	R/E
12	30	Reserved	-
13	34	Reserved	-
14	38	Reserved	-
15	3c	Max_Lat / Min_Gnt / Interrupt Pin / Interrupt Line	R/E[b]
16	40	Retry / TRDY Timeout	R/W
17	44	User Programmable	R/E

Table 116 PCI Configuration Registers

a) Header Type sub-field is read or EEPROM programmable only
b) Interrupt Line sub-field is writable

A.2 Internal Registers

Notes:

- All registers may be accessed by word (16-bit) or d-word (32-bit) accesses. Byte (8-bit) accesses are not supported.
- All registers are cleared to 0 on a hardware or software reset except the buffer free pool registers (offset `0x90 - 0x12c`).

Number	Offset (Hex)	Register Name	Access
		Transmit Configuration Registers	
0	000	HP Tx Pending Queue Start Address	R/W[a]
1	004	HP Tx Pending Queue End Address	R/W[a]
2	008	HP Tx Pending Queue Read Pointer	R/W[ad]
3	00C	HP Tx Pending Queue Write Pointer	R/W
4	010	LP Tx Pending Queue Start Address	R/W[a]
5	014	LP Tx Pending Queue End Address	R/W[a]
6	018	LP Tx Pending Queue Read Pointer	R/W[ad]
7	01C	LP Tx Pending Queue Write Pointer	R/W
8	020	Tx Buffer Release Queue Start Address	R/W[a]
9	024	Tx Buffer Release Queue End Address	R/W[a]
10	028	Tx Buffer Release Queue Read Pointer	R/W
11	02C	Tx Buffer Release Queue Write Pointer	R/W[ad]
12	030	Tx Buffer Release Queue Configuration	R/W
13	034	Command Register 0	R/W
14	038	Command Register 1	R/W
15	03C	Command Register 2	R/W
16	040	Command Register 3	R/W
17	044	Reserved[b]	-
		Mode and Status Registers	
18	048	Status Queue Start Address	R/W[a]
19	04C	Status Queue End Address	R/W[a]
20	050	Status Queue Read Pointer	R/W
21	054	Status Queue Write Pointer	R/W[ad]
22	058	Status Queue Configuration	R/W
23	05C	SAR Mode 0	R/W
24	060	SAR Mode 1	R/W
25	064	Interrupt Status Register (ISR)	R/W[cd]
26	068	Interrupt Under Service Register (IUSR)	W
27	06C	Interrupt Mask Register (IMR)	R/W

Table 117 FireStream155 Register Map

Number	Offset (Hex)	Register Name	Access
28	070	Reserved[b]	-
29	074	Shadow Configuration Register	R/W
		Traffic Shaping	
30	078	Traffic Management Configuration	R/W
31	07C	Calendar Prescale	R/W
32	080	ABR Destination Congested	R/W
33	084	Cell Output Shaping Configuration	R/W
34	088	GFC Configuration	R/W
35	08C	Reserved[b]	-
		Receive Configuration Registers	
36	090	Rx Buffer Free Pool 0 Configuration	R/W
37	094	Rx Buffer Free Pool 0 Start Address	R/W[a]
38	098	Rx Buffer Free Pool 0 End Address	R/W
39	09C	Rx Buffer Free Pool 0 Count	R/W
40	0A0	Rx Buffer Free Pool 0 Count Update	R/W
41	0A4	Rx Buffer Free Pool 1 Configuration	R/W
42	0A8	Rx Buffer Free Pool 1 Start Address	R/W[a]
43	0AC	Rx Buffer Free Pool 1 End Address	R/W
44	0B0	Rx Buffer Free Pool 1 Count	R/W
45	0B4	Rx Buffer Free Pool 1 Count Update	R/W
46	0B8	Rx Buffer Free Pool 2 Configuration	R/W
47	0BC	Rx Buffer Free Pool 2 Start Address	R/W[a]
48	0C0	Rx Buffer Free Pool 2 End Address	R/W
49	0C4	Rx Buffer Free Pool 2 Count	R/W
50	0C8	Rx Buffer Free Pool 2 Count Update	R/W
51	0CC	Rx Buffer Free Pool 3 Configuration	R/W
52	0D0	Rx Buffer Free Pool 3 Start Address	R/W[a]
53	0D4	Rx Buffer Free Pool 3 End Address	R/W
54	0D8	Rx Buffer Free Pool 3 Count	R/W
55	0DC	Rx Buffer Free Pool 3 Count Update	R/W
56	0E0	Rx Buffer Free Pool 4 Configuration	R/W
57	0E4	Rx Buffer Free Pool 4 Start Address	R/W[a]
58	0E8	Rx Buffer Free Pool 4 End Address	R/W
59	0EC	Rx Buffer Free Pool 4 Count	R/W
60	0F0	Rx Buffer Free Pool 4 Count Update	R/W
61	0F4	Rx Buffer Free Pool 5 Configuration	R/W
62	0F8	Rx Buffer Free Pool 5 Start Address	R/W[a]
63	0FC	Rx Buffer Free Pool 5 End Address	R/W

Table 117 FireStream155 Register Map

Number	Offset (Hex)	Register Name	Access
64	100	Rx Buffer Free Pool 5 Count	R/W
65	104	Rx Buffer Free Pool 5 Count Update	R/W
66	108	Rx Buffer Free Pool 6 Configuration	R/W
67	10C	Rx Buffer Free Pool 6 Start Address	R/W[a]
68	110	Rx Buffer Free Pool 6 End Address	R/W
69	114	Rx Buffer Free Pool 6 Count	R/W
70	118	Rx Buffer Free Pool 6 Count Update	R/W
71	11C	Rx Buffer Free Pool 7 Configuration	R/W
72	120	Rx Buffer Free Pool 7 Start Address	R/W[a]
73	124	Rx Buffer Free Pool 7 End Address	R/W
74	128	Rx Buffer Free Pool 7 Count	R/W
75	12C	Rx Buffer Free Pool 7 Count Update	R/W
76	130	Rx Buffer Free Pool Status	R[d]
77	134	Rx Buffer Ready Queue 0 Start Address	R/W[a]
78	138	Rx Buffer Ready Queue 0 End Address	R/W[a]
79	13C	Rx Buffer Ready Queue 0 Read Pointer	R/W
80	140	Rx Buffer Ready Queue 0 Write Pointer	R/W[ad]
81	144	Rx Buffer Ready Queue 0 Configuration	R/W
82	148	Rx Buffer Ready Queue 1 Start Address	R/W[a]
83	14C	Rx Buffer Ready Queue 1 End Address	R/W[a]
84	150	Rx Buffer Ready Queue 1 Read Pointer	R/W
85	154	Rx Buffer Ready Queue 1 Write Pointer	R/W[ad]
86	158	Rx Buffer Ready Queue 1 Configuration	R/W
87	15C	Rx Buffer Ready Queue 2 Start Address	R/W[a]
88	160	Rx Buffer Ready Queue 2 End Address	R/W[a]
89	164	Rx Buffer Ready Queue 2 Read Pointer	R/W
90	168	Rx Buffer Ready Queue 2 Write Pointer	R/W[ad]
91	16C	Rx Buffer Ready Queue 2 Configuration	R/W
92	170	Rx Buffer Ready Queue 3 Start Address	R/W[a]
93	174	Rx Buffer Ready Queue 3 End Address	R/W[a]
94	178	Rx Buffer Ready Queue 3 Read Pointer	R/W
95	17C	Rx Buffer Ready Queue 3 Write Pointer	R/W[ad]
96	180	Rx Buffer Ready Queue 3 Configuration	R/W
97	184	Receive Packet / VC Timeout Interval	R/W
		Statistics	
98	188	Statistics Configuration Register 0	R/W
99	18C	Dropped Packets (No Buffers) Count	R
100	190	Dropped Packets (Low Priority) Count	R

Table 117 FireStream155 Register Map

Number	Offset (Hex)	Register Name	Access
101	194	Receive Timebase Counter	R
102	198	Reserved[b]	-
103	19C	~~Dropped Cell: Bad~~ HEC Error Counter	R
104	1A0	~~Dropped Cell:~~ CRC-10 Error Counter	R
105	1A4	~~Dropped Cell:~~ UTOPIA Long/Short Cell Error Counter	R
106	1A8	~~Dropped Cell:~~ UTOPIA Parity Error Counter	R
107	1AC	~~Dropped Cell: Channel~~ VP/VC Filter Mismatch Counter	R
108	1B0	Statistics Configuration Register 1	R/W
109	1B4	Reserved[b]	-
110	1B8	Maximum Received Packet Length	R/W
		Address Translation	
111	1BC	Receive Address Select 0	R/W
112	1C0	Receive Address Select 1	R/W
113	1C4	Receive Address Mask	R/W
114	1C8	Receive Address Compare	R/W
		DMA Mode	
115	1CC	DMA Mode Register	R/W

Table 117 FireStream155 Register Map

a. This is a CWRE controlled register. See description of SAR Mode Register 0.
b. The host should not access these areas during normal operation
c. The host should not write to this register during normal operation.
d. This register is shadowed in shared memory (if shadowing is enabled).

INTENTIONALLY

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B Register Descriptions

Register 0 - High Priority Transmit Pending Queue Start Address

This register is written by the host at initialisation.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HTPQSA																												0			

Bit(s)	Size	Name	Description
31-4	28	HTPQSA	Defines the upper 28-bits of the High Priority Pending Queue start address, by which the host passes high priority transmit requests and commands to the **FireStream155**.
3-0	4	0	Program to 0.

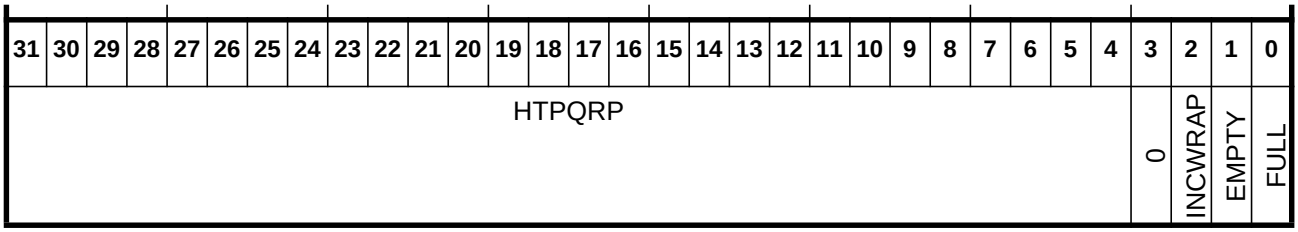
Register 1 - High Priority Transmit Pending Queue End Address

This register is written by the host at initialisation.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HTPQEA																												0			

Bit(s)	Size	Name	Description
31-4	28	HTPQEA	Defines the upper 28-bits of the High Priority Pending Queue end address.
3-0	4	0	Program to 0.

Register 2 - High Priority Transmit Pending Queue Read Pointer



Bit(s)	Size	Name	Description
31-4	28	HTPQRP	Defines the upper 28-bits of the High Priority Pending Queue read pointer. Used by the **FireStream155** to retrieve the next transmit request or command from the High Priority Transmit Pending Queue.
3	1	0	Program to 0.
2	1	INCWRAP	When set during a Host register access, the **FireStream155** will increment the value of the read pointer, irrespective of the HTPQRP field specified on the data bus. This bit is write only and reads 0.
1	1	EMPTY	When set, indicates that the High Priority Transmit Pending Queue contains no data. This bit is read only.
0	1	FULL	When set, indicates that the High Priority Transmit Pending Queue is full. This bit is read only.

Register 3 - High Priority Transmit Pending Queue Write Pointer

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HTPQWP																												0	INCWRAP	EMPTY	FULL

Bit(s)	Size	Name	Description
31-4	28	HTPQWP	Defines the upper 28-bits of the High Priority Pending Queue write pointer. Updated by the host when adding entries to the HTPQ.
3	1	0	Program to 0.
2	1	INCWRAP	When set during a Host register access, the **FireStream155** will increment the value of the write pointer, irrespective of the HTPQWP field specified on the data bus. This bit is write only and reads 0.
1	1	EMPTY	When set, indicates that the High Priority Transmit Pending Queue contains no data. This bit is read only.
0	1	FULL	When set, indicates that the High Priority Transmit Pending Queue is full. This bit is read only.

Register 4 - Low Priority Transmit Pending Queue Start Address

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTPQSA																												0			

Bit(s)	Size	Name	Description
31-4	28	LTPQSA	Defines the upper 28-bits of the Low Priority Pending Queue start address, by which the host passes low priority transmit requests and commands to the **FireStream155**.
3-0	4	0	Program to 0.

Register 5 - Low Priority Transmit Pending Queue End Address

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTPQEA																												0			

Bit(s)	Size	Name	Description
31-4	28	LTPQEA	Defines the upper 28-bits of the High Priority Pending Queue end address.
3-0	4	0	Program to 0.

Register 6 - Low Priority Transmit Pending Queue Read Pointer

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTPQRP																												0	INCWRAP	EMPTY	FULL

Bit(s)	Size	Name	Description
31-4	28	LTPQRP	Defines the upper 28-bits of the Low Priority Pending Queue read pointer. Used by the **FireStream155** to retrieve the next transmit request or command from the Low Priority Transmit Pending Queue.
3	1	0	Program to 0.
2	1	INCWRAP	When set during a Host register access, the **FireStream155** will increment the value of the write pointer, irrespective of the LTPQRP field specified on the data bus. This bit is write only and reads 0.
1	1	EMPTY	When set, indicates that the Low Priority Transmit Pending Queue contains no data. This bit is read only.
0	1	FULL	When set, indicates that the Low Priority Transmit Pending Queue is full. This bit is read only.

Register 7 - Low Priority Transmit Pending Queue Write Pointer

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTPQWP																												0	INCWRAP	EMPTY	FULL

Bit(s)	Size	Name	Description
31-4	28	LTPQWP	Defines the upper 28-bits of the Low Priority Pending Queue write pointer. Updated by the host when adding entries to the LTPQ.
3	1	0	Program to 0.
2	1	INCWRAP	When set during a Host register access, the **FireStream155** will increment the value of the write pointer, irrespective of the LTPQWP field specified on the data bus. This bit is write only and reads 0.
1	1	EMPTY	When set, indicates that the Low Priority Transmit Pending Queue contains no data. This bit is read only.
0	1	FULL	When set, indicates that the Low Priority Transmit Pending Queue is full. This bit is read only.

Register 8 - Transmit Buffer Release Queue Start Address

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBRQSA																												0			

Bit(s)	Size	Name	Description
31-4	28	TBRQSA	Defines the upper 28-bits of the Transmit Buffer Release Queue start address by which transmit status is passed to the Host, and used transmit buffers are returned to the Host.
3-0	4	0	Program to 0.

Register 9 - Transmit Buffer Release Queue End Address

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBRQEA																												0			

Bit(s)	Size	Name	Description
31-4	28	TBRQEA	Defines the upper 28-bits of the Transmit Buffer Release Queue end address.
3-0	4	0	Program to 0.

Register 10 - Transmit Buffer Release Queue Read Pointer

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBRQRP																												0	INCWRAP	EMPTY	FULL

Bit(s)	Size	Name	Description
31-4	28	TBRQRP	Defines the upper 28-bits of the Transmit Buffer Release Queue read pointer.
3	1	0	Program to 0.
2	1	INCWRAP	When set during Host register access, the **FireStream155** will increment the value of the read pointer, irrespective of the TBRQRP field specified on the data bus. This bit is write only and reads 0.
1	1	EMPTY	When set, indicates that the Transmit Buffer Release Queue contains no data. This bit is read only.
0	1	FULL	When set, indicates that the Transmit Buffer Release Queue is full. This bit is read only.

Register 11 - Transmit Buffer Release Queue Write Pointer

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBRQWP																												0	INCWRAP	EMPTY	FULL

Bit(s)	Size	Name	Description
31-4	28	TBRQWP	Defines the upper 28-bits of the Transmit Buffer Release Queue write pointer. Updated by the Host when adding entries to the TBRQ.
3	1	0	Program to 0.
2	1	INCWRAP	When set during Host register access, the **FireStream155** will increment the value of the read pointer, irrespective of the TBRQWP field specified on the data bus. This bit is write only and reads 0.
1	1	EMPTY	When set, indicates that the Transmit Buffer Release Queue contains no data. This bit is read only.
0	1	FULL	When set, indicates that the Transmit Buffer Release Queue is full. This bit is read only.

Register 12 - Transmit Buffer Release Queue Configuration

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0																TIME OUT		TBRIF			TBRWT										

Bit(s)	Size	Name	Description
31-16	10	0	Program to 0.
15-14	2	TIMEOUT	This value determines the maximum time before the Transmit Buffer Release Queue forces an interrupt. Only valid if TBRIF is not 0. 00 - 100us 01 - 1ms 10 - 10ms 11 - 100ms
13-11	3	TBRIF	Status Interrupt Frequency. This count specifies, in powers of 2, the frequency of transmit buffer release interrupts.
10-0	11	TBRWT	This 11-bit threshold value defines the number of free entries left on the queue below which the **TBR-NF** interrupt is generated.

Register 13 - Command Register 0

Command Register 0-3 together form the on-chip Transmit Pending Queue. The user submits Direct Commands to the **FireStream155** using these registers.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMND0																															

Bit(s)	Size	Name	Description
31-0	32	CMND0	Defines the first word of a direct command.

Register 14 - Command Register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMND1																															

Bit(s)	Size	Name	Description
31-0	32	CMND1	Defines the second word of a direct command.

Register 15 - Command Register 2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMND2																															

Bit(s)	Size	Name	Description
31-0	32	CMND2	Defines the third word of a direct command.

Register 16 - Command Register 3

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMND3																															

Bit(s)	Size	Name	Description
31-0	32	CMND3	Defines the fourth word of a direct command. Writing to this register causes the command to be initiated.

Register 17 - Reserved

Register 18 - Status Queue Start Address

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SQSA																												0			

Bit(s)	Size	Name	Description
31-4	28	SQSA	Defines the upper 28-bits of the Status Queue start address, which is used by the **FireStream155** to pass status information (in response to commands) to the Host.
3-0	4	0	Program to 0.

Register 19 - Status Queue End Address

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SQEA																												0			

Bit(s)	Size	Name	Description
31-4	28	SQEA	Defines the upper 28-bits of the Status Queue end address.
3-0	4	0	Program to 0.

Register 20 - Status Queue Read Pointer

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SQRP																												0	INCWRAP	EMPTY	FULL

Bit(s)	Size	Name	Description
31-4	28	SQRP	Defines the upper 28-bits of the Status Queue read pointer, which is used by the Host to retrieve Status Queue entries.
3	1	0	Program to 0.
2	1	INCWRAP	When set during a Host register access, the **FireStream155** will increment the value of the read pointer, irrespective of the SQRP field specified on the data bus. This bit is write only and reads 0.
1	1	EMPTY	When set, indicates that the Status Queue contains no data. This bit is read only.
0	1	FULL	When set, indicates that the Status Queue is full. This bit is read only.

Register 21 - Status Queue Write Pointer

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SQWP																												0	INCWRAP	EMPTY	FULL

Bit(s)	Size	Name	Description
31-4	28	SQWP	Defines the upper 28-bits of the Status Queue write pointer. Updated by the **FireStream155** when adding entries to the Status Queue.
3	1	0	Program to 0.
2	1	INCWRAP	When set during a Host register access, the **FireStream155** will increment the value of the read pointer, irrespective of the SQWP field specified on the data bus. This bit is write only and reads 0.
1	1	EMPTY	When set, indicates that the Status Queue contains no data. This bit is read only.
0	1	FULL	When set, indicates that the Status Queue is full. This bit is read only.

Register 22 - Status Queue Configuration

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0																TIME OUT		SIF			SQWT										

Bit(s)	Size	Name	Description
31-16	10	0	Program to 0.
15-14	2	TIMEOUT	This value determines the maximum time before the Status Queue forces an interrupt. Only valid if SIF is not 0. 00 - 100us 01 - 1ms 10 - 10ms 11 - 100ms
13-11	3	SIF	Status Interrupt Frequency. This count specifies, in powers of 2, the frequency of transmit buffer release interrupts.
10-0	11	SQWT	This 11-bit threshold value defines the number of free entries left on the queue below which the **SQ-NF** interrupt is generated.

Register 23 - SAR Mode 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHADEN	GINT	INTMODE		CWRE	UNLOCK	HALT	SRST1	SRST0	MEMSZ			MEMPS		MEMWT		PRPWT		CALSUP		RXVCS				ABRVCS				TXVCS			

Bit(s)	Size	Name	Description	
3-0	4	TXVCS	Transmit VCs Supported.	
			0000	None
			0001	1k
			0010	2k
			0011	4k
			0100	8k
			0101	16k
			0110	32k
			0111	64k
			1XXX	Reserved
7-4	4	ABRVCS	ABR VCs Supported. (This should be set to less than or equal to TXVCS)	
			0000	None
			0001	512
			0010	1k
			0011	2k
			0100	4k
			0101	8k
			0110	16k
			0111	32k
			1XXX	Reserved
11-8	4	RXVCS	Receive VCs Supported.	
			0000	None
			0001	1k
			0010	2k
			0011	4k
			0100	8k
			0101	16k
			0110	32k
			0111	64k
			1XXX	Reserved
13-12	2	CALSUP	Calendars Supported.	
			00	1
			01	2
			10	3
			11	4

Bit(s)	Size	Name	Description
15-14	2	PRPWT	Peripheral Wait States. 00 0 clocks 01 1 clocks 10 2 clocks 11 4 clocks
17-16	2	MEMWT	Local Memory Wait States. 00 0 clocks 01 1 clocks 10 2 clocks 11 4 clocks
19-18	2	MEMPS	Local Memory Page Size. 00 32k deep devices 01 128k deep devices 10 512k deep devices 11 Reserved
22-20	3	MEMSZ	Local Memory Size. 000 32k deep 001 64k deep 010 128k deep 011 256k deep 100 512k deep 101 1024k deep 110 2048k deep 111 Reserved
23	1	SRST0	**FireStream155** Master Software Reset. This bit is set to reset all internal **FireStream155** circuitry.
24	1	SRST1	**FireStream155** Software Reset. This bit is set to reset all internal **FireStream155** circuitry but does not reinitialise local memory.
25	1	RUN/$\overline{\text{HALT}}$	Puts the **FireStream155** into its halt mode (clear) / normal operation - run mode (set).
26	1	UNLOCK	If set this bit enables access to the debug local memory access commands. This prevents inadvertent alteration of local memory.
27	1	CWRE	**FireStream155** Host Queue Pointer Initialisation Enable. This bit is set to allow the Host to initialise Queue pointers and Free Pool Start Addesses. This bit should be cleared after initialisation for normal operation. CWRE controlled registers may be read at any time.

Bit(s)	Size	Name	Description	
29-28	2	INTMODE	Interrupt Mode.	
			00	Read and Clear Register: when the Host accesses the **FireStream155** ISR, the interrupt flags are implicitly cleared as part of the read process
			01	Read and No Clear Register: when the Host accesses the **FireStream155** ISR, the interrupt flags are not cleared. Clearing the flags requires an additional write to the Interrupt Under Service Register (IUSR)
			10	Read, No Clear and Inhibit: when the Host accesses the **FireStream155** ISR, the interrupt flags are not cleared, and **FireStream155** interrupt generation is globally disabled by clearing the GINT bit of SAR Mode 0. Clearing interrupt conditions requires an additional write to the IUSR. A write to set the **FireStream155** GINT bit of SAR Mode 0 is required to globally re-enable interrupt generation
			11	Read, Clear and Inhibit
30	1	GINT	Global Interrupt Enable. When set, enables **FireStream155** interrupt generation. When reset, no **FireStream155** interrupts will be generated (however the ISR will still be updated). Note that all interrupts are disabled at power-up.	
31	1	SHADEN	Shadow Register Enable. When set, enables the **FireStream155** shadow register function.	

Register 24 - SAR Mode 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	DEFHEC	TESTLP	DCRM	DCOAM	OAMCRC	DUMPE	GPLEN	GNAM	GVAS	GPAS	GPRI	PMS	0	0	GFCR	GFCE	UTPRTY	UT8BIT	HECM			TAGM	RRTL				TRTL			

Bit(s)	Size	Name	Description
3-0	4	TRTL	Transmit Routing Tag Length. This field specifies the length (if any) of the routing tag to be appended to all transmitted cells. Maximum length 12.
7-4	4	RRTL	Receive Routing Tag Length. This field specifies the length (if any) of the routing tag expected to be appended on received cells. Maximum length 12.
8	1	TAGM	Tag mode. defines whether the TAG space within the **FireStream155** should be used for a routing tag (clear) or as an encapsulated header (set) to be added on a per-packet basis. Note - if in encapsulated header mode then the ENC bit in the Transmit configuration must be set to enable this on a per circuit basis.
11-9	3	HECM	Header Error Check Mode. HEC2 specifies Mask = 0x55 (set) or Mask = 0x00 (clear). HEC1 specifies transmit cell header check byte included (53 byte cell) when set, or cell header check byte omitted (52 byte cell) when clear. HEC0 enables cell header error checking (set) or disables cell header error checking (clear).
12	1	UT8BIT	UTOPIA 8-bit bus when set.
13	1	UTPRTY	UTOPIA parity enabled when set.
14	1	GFCE	GFC Enable for the Traffic Manager and Reassembly.
15	1	GFCR	GFC mode in Reassembly module. 0: Per Chip GFC changes reported to Host. 1: Per Channel GFC changes reported to Host.
16	1	0	Program to 0.
17	1	0	Program to 0.
18	1	PMS	Position Mode Select. Selects either Store and forward (clear) or Position Important (set).
19	1	GPRI	Global enable for Receive Buffer Manager low priority discard mode. This overrides individual circuit settings.
20	1	GPAS	Global enable for packet ageing. This overrides individual circuit settings.

Bit(s)	Size	Name	Description
21	1	GVAS	Global enable for VC ageing. This overrides individual circuit settings.
22	1	GNAM	Global Enable for Non-Assured Mode. In this mode the contents of the final cell of AAL5 packets will be delivered to the host even if a CRC error or length error are detected.
23	1	GPLEN	Global enable for packet length check. This overrides individual circuit settings.
24	1	DUMPE	Dump enable. If set all received cells for non-activated channels are sent as transparent cells using buffers from free pool 6 and are reported on ready queue 3.
25	1	OAMCRC	Operation and Maintenance cyclic redundancy check enable (set) / disable (reset).
26	1	DCOAM	Discard Operation and Maintenance. If this bit is set the **FireStream155** will discard F5 OAM cells. If cleared all F5 OAM cells will use buffers from free pool 6 and report on ready queue 3.
27	1	DCRM	Discard Resource Management. If this bit is set the **FireStream155** will not forward RM cells to the Host. If cleared all RM cells will use buffers from free pool 6 and report on ready queue 3.
28	1	TSTLP	Test Loop Enable. When this bit is set the **FireStream155**'s loopback mode. Note: For loopback to function DEFHEC and TRTL should be set to 0.
29	1	DEFHEC	Define HEC etc. This bit should be set when the field in the Init TX area is used to define either HEC, UDF or UTOPIA address.
30	1	0	Program to 0.
31	1	0	Program to 0.

Register 25 - Interrupt Status

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							CSQ_NF	CSQ_W	PCI_FTL	GFC_C0	CTPQ_E	TBRQ_NF	TBRQ_W	HECO	CRCCO	VPFCO	UPECO	USCEO	INITERR	INIT	BFP_SC	RBRQ3_NF	RBRQ2_NF	RBRQ1_NF	RBRQ0_NF	RBRQ3_W	RBRQ2_W	RBRQ1_W	RBRQ0_W	DPCO	LPCO

Bit(s)	Size	Name	Description
0	1	LPCO	Low Priority Discard Count Overflow.
1	1	DPCO	Dropped Packet - No Buffers Count Overflow.
2	1	RBRQ0_W	Receive Buffer Ready Queue 0 Write.
3	1	RBRQ1_W	Receive Buffer Ready Queue 1 Write.
4	1	RBRQ2_W	Receive Buffer Ready Queue 2 Write.
5	1	RBRQ3_W	Receive Buffer Ready Queue 3 Write.
6	1	RBRQ0_NF	Receive Buffer Ready Queue 0 Nearly Full.
7	1	RBRQ1_NF	Receive Buffer Ready Queue 1 Nearly Full.
8	1	RBRQ2_NF	Receive Buffer Ready Queue 2 Nearly Full.
9	1	RBRQ3_NF	Receive Buffer Ready Queue 3 Nearly Full.
10	1	BFP_SC	Buffer Free Pool Status Change.
11	1	INIT	**FireStream155** Initialisation Complete.
12	1	INITERR	**FireStream155** Initialisation Fail. (local memory test fail)
13	1	USCEO	UTOPIA Short Cell Count Overflow.
14	1	UPECO	UTOPIA Parity Error Count Overflow.
15	1	VPFCO	VP/VC Filter Mismatch Count Overflow.
16	1	CRCCO	CRC-10 Count Overflow.
17	1	HECO	HEC Error Count Overflow.
18	1	TBRQ_W	Transmit Buffer Release Queue Write.
19	1	TBRQ_NF	Transmit Buffer Release Queue Nearly Full.
20	1	CTPQ_E	On-chip Pending Queue Ready.
21	1	GFC_C0	GFC Credit Counter Zero.
22	1	PCI_FTL	PCI Fatal Error. Non-recoverable PCI Error requires device reset.

Bit(s)	Size	Name	Description
23	1	CSQ_W	Command Status Queue Write.
24	1	CSQ_NF	Command Status Queue Nearly Full.

Register 26 - Interrupt Under Service

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							CSQ_NF	CSQ_W	PCI_FTL	GFC_C0	CTPQ_E	TBRQ_NF	TBRQ_W	HECO	CRCCO	VPFCO	UPECO	USCEO	INITERR	INIT	BFP_SC	RBRQ3_NF	RBRQ2_NF	RBRQ1_NF	RBRQ0_NF	RBRQ3_W	RBRQ2_W	RBRQ1_W	RBRQ0_W	DPCO	LPCO

- Each interrupt status bit in the ISR can be cleared independently. Writing a 1 clears the interrupt and writing a 0 leaves the interrupt pending.

Register 27 - Interrupt Mask

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							CSQ_NF	CSQ_W	PCI_FTL	GFC_C0	CTPQ_E	TBRQ_NF	TBRQ_W	HECO	CRCCO	VPFCO	UPECO	USCEO	INITERR	INIT	BFP_SC	RBRQ3_NF	RBRQ2_NF	RBRQ1_NF	RBRQ0_NF	RBRQ3_W	RBRQ2_W	RBRQ1_W	RBRQ0_W	DPCO	LPCO

- Within the IMR, a value of 1 indicates interrupt enabled, and a value of 0 masks that particular interrupt source.

Register 28 - Reserved

Register 29 - Shadow Configuration

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRBA																												SSEL	Timeout		

Bit(s)	Size	Name	Description	
2-0	3	Timeout	Shadow Register Update Period.	
			000	No Timer Function
			001	50 us
			010	100 us
			011	1 ms
			100	5 ms
			101	10 ms
			110	50 ms
			111	100 ms
3	1	Shadow Select	0	Select Normal Register List
			1	Select Alternate Register List
31-4	28	Address	Shadow Register Base Address.	

Register 30 - Traffic Management Configuration

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0																				FRMO_MASK	FCAL		TMCTS	C3TS	C2TS	C1TS	C0TS	C3EN	C2EN	C1EN	C0EN

Bit(s)	Size	Name	Description
0	1	C0EN	Calendar 0 Enable.
1	1	C1EN	Calendar 1 Enable.
2	1	C2EN	Calendar 2 Enable.
3	1	C3EN	Calendar 3 Enable.
4	1	C0TS	Calendar 0 Tick Source Select (0 = LCLK, 1 = TMCTK).
5	1	C1TS	Calendar 1 Tick Source Select (0 = LCLK, 1 = TMCTK).
6	1	C2TS	Calendar 2 Tick Source Select (0 = LCLK, 1 = TMCTK).
7	1	C3TS	Calendar 3 Tick Source Select (0 = LCLK, 1 = TMCTK).
8	1	TMCTS	If set, TMCTK is synchronised to LCLK on chip. If reset, the user should provide a synchronised input on TMCTK with a ‘high’ time equal to one clock period of LCLK.
10-9	2	FCAL	Fastest calendar. Set to indicate which calendar is fastest.
11	1	FRMO_MSK	FRM out-of-rate mask. If set, out-of-rate FRM cells are not sent from channels where the rate has fallen to zero.
31-12	20	0	Program to 0.

Register 31 - Calendar Prescale

Note: There is a minimum allowable number of four LCLK cycles per calendar tick. (i.e. If LCLK is selected as the calendar source, then the appropriate PCSL value should be set to a minimum of `0x04`.)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C3PSCL								C2PSCL								C1PSCL								C0PSCL							

Bit(s)	Size	Name	Description
7-0	8	C0PSCL	Calendar 0 Prescale. ~~If set to n, the selected Tick Source for Calendar 0 is divided by n+1.~~ If set to n, the calendar time pointer advances once evry n+1 LCLK cycles. This will usually equate to 1 cell lifetime.
15-8	8	C1PSCL	Calendar 1 Prescale. ~~If set to n, the selected Tick Source for Calendar 1 is divided by n+1.~~ If set to n, the calendar time pointer advances once evry n+1 LCLK cycles. This will usually equate to 1 cell lifetime.
23-16	8	C2PSCL	Calendar 2 Prescale. ~~If set to n, the selected Tick Source for Calendar 2 is divided by n+1.~~If set to n, the calendar time pointer advances once evry n+1 LCLK cycles. This will usually equate to 1 cell lifetime.
31-24	8	C3PSCL	Calendar 3 Prescale. ~~If set to n, the selected Tick Source for Calendar 3 is divided by n+1~~.If set to n, the calendar time pointer advances once evry n+1 LCLK cycles. This will usually equate to 1 cell lifetime.

Register 32 - ABR Congested Destination

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0							CDM	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0	MOD7		MOD6		MOD5		MOD4		MOD3		MOD2		MOD1		MOD0	

Bit(s)	Size	Name	Description
31-25	16	0	Program to 0.
24	1	CDM	Method of rate modification, Set = Binary mode; Clear = Explicit rate
23	1	EN7	Enable rate modification on channels in group 7
22	1	EN6	Enable rate modification on channels in group 6
21	1	EN5	Enable rate modification on channels in group 5
20	1	EN4	Enable rate modification on channels in group 4
19	1	EN3	Enable rate modification on channels in group 3
18	1	EN2	Enable rate modification on channels in group 2
17	1	EN1	Enable rate modification on channels in group 1
16	1	EN0	Enable rate modification on channels in group 0
15-14	2	MOD7	Rate Request modification for group 7 channels
13-12	2	MOD6	Rate Request modification for group 6 channels
11-10	2	MOD5	Rate Request modification for group 5 channels
9-8	2	MOD4	Rate Request modification for group 4 channels
7-6	2	MOD3	Rate Request modification for group 3 channels
5-4	2	MOD2	Rate Request modification for group 2 channels
3-2	2	MOD1	Rate Request modification for group 1 channels
1-0	2	MOD0	Rate Request modification for group 0 channels

Table 118 MOD Coding

Method	MOD bits	Operation
CDM = 0	00	reduce ER in outgoing BRM cells by a factor of 2
	01	reduce ER in outgoing BRM cells by a factor of 4
	10	reduce ER in outgoing BRM cells by a factor of 8
	11	reduce ER in outgoing BRM cells by a factor of 16
CDM = 1	00	No effect
	01	set NI in outgoing BRM cells
	10	set CI in outgoing BRM cells
	11	set both NI and CI bits outgoing BRM cells

Register 33 - Cell Output Shaping Configuration

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0			COTS	CEN	0	SC		COBS								COPK								COST							

Bit(s)	Size	Name	Description
31-29	3	0	Program to 0.
28	1	COTS	Cell Output Tick Source Select (0 = LCLK, 1 = TMCTK)
27	1	CEN	Enable for Cell Output Shaping. This bit is set to enable shaping of the total output traffic from the **FireStream155**. If cleared the traffic flow is unrestricted.
26	1	0	Program to 0.
25-24	2	SC	Contains the scaling factor by which the selected clock is divided when the Peak and Sustainable counters values are being decremented. `00:` divide by 1 `01:` divide by 2 `10:` divide by 4 `11:` divide by 8
23-16	8	COBS	Cell Output Bucket Size.
15-8	8	COPK	Value by which the Prescaled selected clock is divided by to increment the Peak Rate Counter.
7-0	8	COST	Value by which the Prescaled selected clock is divided by to increment the Sustainable Rate Counter.

Register 34 - GFC Configuration

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								GFCCON3	GFCCON2	GFCCON1	GFCCON0	GFCEN3	GFCEN2	GFCEN1	GFCEN0	GFCCR															

Bit(s)	Size	Name	Description
31-24	8	0	Program to 0.
23	1	GFCCON3	GFC Control for Calendar 3. If set in conjunction with GFCEN3, traffic on calendar 3 will be controlled. If reset, traffic is uncontrolled.
22	1	GFCCON2	GFC Control for Calendar 2. If set in conjunction with GFCEN2, traffic on calendar 2 will be controlled. If reset, traffic is uncontrolled.
21	1	GFCCON1	GFC Control for Calendar 1. If set in conjunction with GFCEN1, traffic on calendar 1 will be controlled. If reset, traffic is uncontrolled.
20	1	GFCCON0	GFC Control for Calendar 0. If set in conjunction with GFCEN0, traffic on calendar 0 will be controlled. If reset, traffic is uncontrolled.
19	1	GFCEN3	GFC Enable for Calendar 3. If set, GFC algorithm is enabled.
18	1	GFCEN2	GFC Enable for Calendar 2. If set, GFC algorithm is enabled.
17	1	GFCEN1	GFC Enable for Calendar 1. If set, GFC algorithm is enabled.
16	1	GFCEN0	GFC Enable for Calendar 0. If set, GFC algorithm is enabled.
15-0	16	GFCCR	GFC Credit Refresh. Used to update the GFC credit refresh counter on initialisation or after receiving the Set command.

Register 35 - Reserved

Register 36 - Receive Buffer Free Pool 0 Configuration

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RBS																RBSVAL	0		CME	DLP	BFP0WT										

Bit(s)	Size	Name	Description
31-16	16	RBS	This 16 bit number indicates the size in bytes of buffers contained in Receive Buffer Free Pool 0.
15	1	RBSVAL	RBS is valid. If set the **FireStream155** assumes that all buffers in Receive Buffer Free Pool 0 are of size RBS. Otherwise the buffer size in the receive descriptor will be used.
14-13	2	0	Program to 0.
12	1	CME	Count/Count Update Mechanism enable.
11	1	DLP	Force Discard of Low Priority Traffic for VCs using this pool.
10-0	11	BFP0WT	This 11-bit threshold value defines the number of free entries left in the pool below which the **BFP0-NE** interrupt is generated when using the count / count update mechanism. In this mode, the threshold is also used to automatically trigger the discard of packets on low priority circuits.

Register 37 - Receive Buffer Free Pool 0 Start Address

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RBFP0SA																												0			

Bit(s)	Size	Name	Description
31-4	28	RBFP0SA	Defines the upper 28-bits of the Receive Buffer Free Pool start address. This is a linked list of free buffers. When the **FireStream155** requires a buffer, it updates the pointer to the next free buffer in the linked list.
3-0	4	0	Program to 0.

Register 38 - Receive Buffer Free Pool 0 End Address

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RBRQ0EA																												0			

Bit(s)	Size	Name	Description
31-4	28	RBRQ0EA	Defines the upper 28-bits of the Receive Buffer Ready Queue 0 end address.
3-0	4	0	Program to 0.

Register 39 - Receive Buffer Free Pool 0 Count

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								RBPFP0C																							

Bit(s)	Size	Name	Description
31-16	16	0	Program to 0.
23-0	24	RBFP0C	This is a 24 bit counter which contains a count of the number of descriptors in free pool 0. The **FireStream155** will decrement this free counter by one when it removes a descriptor from the pool, and will be added to by the Host via the Receive Buffer Free Pool 0 Count Update register. The value of this register is used by the **FireStream155** to generate the BFP0_NE interrupt.

Register 40 - Receive Buffer Free Pool 0 Count Update

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0																RBFP0CU															

Bit(s)	Size	Name	Description
31-16	16	0	Program to 0.
15-0	16	RBFP0CU	This 16-bit field will be added to the Receive Buffer Free Pool 0 Count register when the Host writes to it, when adding to Buffer Free Pool 0. Note that writing to this register is optional.

Register 41 - Receive Buffer Free Pool 1 Configuration

The format of this register is as Receive Buffer Free Pool 0 Configuration.

Register 42 - Receive Buffer Free Pool 1 Start Address

The format of this register is as Receive Buffer Free Pool 0 Start Address.

Register 43 - Receive Buffer Free Pool 1 End Address

The format of this register is as Receive Buffer Free Pool 0 End Address.

Register 44 - Receive Buffer Free Pool 1 Count

The format of this register is as Receive Buffer Free Pool 0 Count.

Register 45 - Receive Buffer Free Pool 1 Count Update

The format of this register is as Receive Buffer Free Pool 0 Count Update.

Register 46 - Receive Buffer Free Pool 2 Configuration

The format of this register is as Receive Buffer Free Pool 0 Configuration.

Register 47 - Receive Buffer Free Pool 2 Start Address

The format of this register is as Receive Buffer Free Pool 0 Start Address.

Register 48 - Receive Buffer Free Pool 2 End Address

The format of this register is as Receive Buffer Free Pool 0 End Address.

Register 49 - Receive Buffer Free Pool 2 Count

The format of this register is as Receive Buffer Free Pool 0 Count.

Register 50 - Receive Buffer Free Pool 2 Count Update

The format of this register is as Receive Buffer Free Pool 0 Count Update.

Register 51 - Receive Buffer Free Pool 3 Configuration

The format of this register is as Receive Buffer Free Pool 0 Configuration.

Register 52 - Receive Buffer Free Pool 3 Start Address

The format of this register is as Receive Buffer Free Pool 0 Start Address.

Register 53 - Receive Buffer Free Pool 3 End Address

The format of this register is as Receive Buffer Free Pool 0 End Address.

Register 54 - Receive Buffer Free Pool 3 Count

The format of this register is as Receive Buffer Free Pool 0 Count.

Register 55 - Receive Buffer Free Pool 3 Count Update

The format of this register is as Receive Buffer Free Pool 0 Count Update.

Register 56 - Receive Buffer Free Pool 4 Configuration

The format of this register is as Receive Buffer Free Pool 0 Configuration.

Register 57 - Receive Buffer Free Pool 4 Start Address

The format of this register is as Receive Buffer Free Pool 0 Start Address.

Register 58 - Receive Buffer Free Pool 4 End Address

The format of this register is as Receive Buffer Free Pool 0 End Address.

Register 59 - Receive Buffer Free Pool 4 Count

The format of this register is as Receive Buffer Free Pool 0 Count.

Register 60 - Receive Buffer Free Pool 4 Count Update

The format of this register is as Receive Buffer Free Pool 0 Count Update.

Register 61 - Receive Buffer Free Pool 5 Configuration

The format of this register is as Receive Buffer Free Pool 0 Configuration.

Register 62 - Receive Buffer Free Pool 5 Start Address

The format of this register is as Receive Buffer Free Pool 0 Start Address.

Register 63 - Receive Buffer Free Pool 5 End Address

The format of this register is as Receive Buffer Free Pool 0 End Address.

Register 64 - Receive Buffer Free Pool 5 Count

The format of this register is as Receive Buffer Free Pool 0 Count.

Register 65 - Receive Buffer Free Pool 5 Count Update

The format of this register is as Receive Buffer Free Pool 0 Count Update.

Register 66 - Receive Buffer Free Pool 6 Configuration

The format of this register is as Receive Buffer Free Pool 0 Configuration.

Register 67 - Receive Buffer Free Pool 6 Start Address

The format of this register is as Receive Buffer Free Pool 0 Start Address.

Register 68 - Receive Buffer Free Pool 6 End Address

The format of this register is as Receive Buffer Free Pool 0 End Address.

Register 69 - Receive Buffer Free Pool 6 Count

The format of this register is as Receive Buffer Free Pool 0 Count.

Register 70 - Receive Buffer Free Pool 6 Count Update

The format of this register is as Receive Buffer Free Pool 0 Count Update.

Register 71 - Receive Buffer Free Pool 7 Configuration

The format of this register is as Receive Buffer Free Pool 0 Configuration.

Register 72 - Receive Buffer Free Pool 7 Start Address

The format of this register is as Receive Buffer Free Pool 0 Start Address.

Register 73 - Receive Buffer Free Pool 7 End Address

The format of this register is as Receive Buffer Free Pool 0 End Address.

Register 74 - Receive Buffer Free Pool 7 Count

The format of this register is as Receive Buffer Free Pool 0 Count.

Register 75 - Receive Buffer Free Pool 7 Count Update

The format of this register is as Receive Buffer Free Pool 0 Count Update.

Register 76 - Receive Buffer Free Pool Status

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	BFP7_EMPTY	BFP7_NE	BFP7_NEOLL	0	BFP6_EMPTY	BFP6_NE	BFP6_NEOLL	0	BFP5_EMPTY	BFP5_NE	BFP5_NEOLL	0	BFP4_EMPTY	BFP4_NE	BFP4_NEOLL	0	BFP3_EMPTY	BFP3_NE	BFP3_NEOLL	0	BFP2_EMPTY	BFP2_NE	BFP2_NEOLL	0	BFP1_EMPTY	BFP1_NE	BFP1_NEOLL	0	BFP0_EMPTY	BFP0_NE	BFP0_NEOLL

Bit(s)	Size	Name	Description
31	1	0	This bit will be 0 when read.
30	1	BFP7_EMPTY	Buffer Free Pool 7 Empty indication.
29	1	BFP7_NE	Buffer Free Pool 7 Nearly Empty.
28	1	BFP7_NEOLL	Buffer Free Pool 7 Marker bit found in Receive Descriptor list.
27	1	0	This bit will be 0 when read.
26	1	BFP6_EMPTY	Buffer Free Pool 6 Empty indication.
25	1	BFP6_NE	Buffer Free Pool 6 Nearly Empty.
24	1	BFP6_NEOLL	Buffer Free Pool 6 Marker bit found in Receive Descriptor list.
23	1	0	This bit will be 0 when read.
22	1	BFP5_EMPTY	Buffer Free Pool 5 Empty indication.
21	1	BFP5_NE	Buffer Free Pool 5 Nearly Empty.
20	1	BFP5_NEOLL	Buffer Free Pool 5 Marker bit found in Receive Descriptor list.
19	1	0	This bit will be 0 when read.
18	1	BFP4_EMPTY	Buffer Free Pool 4 Empty indication.
17	1	BFP4_NE	Buffer Free Pool 4 Nearly Empty.
16	1	BFP4_NEOLL	Buffer Free Pool 4 Marker bit found in Receive Descriptor list.
15	1	0	This bit will be 0 when read.
14	1	BFP3_EMPTY	Buffer Free Pool 7 Empty indication.
13	1	BFP3_NE	Buffer Free Pool 7 Nearly Empty.
12	1	BFP3_NEOLL	Buffer Free Pool 7 Marker bit found in Receive Descriptor list.
11	1	0	This bit will be 0 when read.
10	1	BFP2_EMPTY	Buffer Free Pool 7 Empty indication.
9	1	BFP2_NE	Buffer Free Pool 7 Nearly Empty.

Bit(s)	Size	Name	Description
8	1	BFP2_NEOLL	Buffer Free Pool 7 Marker bit found in Receive Descriptor list.
7	1	0	This bit will be 0 when read.
6	1	BFP1_EMPTY	Buffer Free Pool 1 Empty indication.
5	1	BFP1_NE	Buffer Free Pool 1 Nearly Empty.
4	1	BFP1_NEOLL	Buffer Free Pool 1 Marker bit found in Receive Descriptor list.
3	1	0	This bit will be 0 when read.
2	1	BFP0_EMPTY	Buffer Free Pool 0 Empty indication.
1	1	BFP0_NE	Buffer Free Pool 0 Nearly Empty.
0	1	BFP0_NEOLL	Buffer Free Pool 0 Marker bit found in Receive Descriptor list.

Register 77 - Receive Buffer Ready Queue 0 Start Address

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RBRQ0SA																												0			

Bit(s)	Size	Name	Description
31-4	28	RBRQ0SA	Defines the upper 28-bits of the Receive Buffer Ready Queue 0 start address, by which the **FireStream155** indicates to the Host that Receive Descriptors are available.
3-0	4	0	Program to 0.

Register 78 - Receive Buffer Ready Queue 0 End Address

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RBRQ0EA																												0			

Bit(s)	Size	Name	Description
31-4	28	RBRQ0EA	Defines the upper 28-bits of the Receive Buffer Ready Queue 0 end address.
3-0	4	0	Program to 0.

Register 79 - Receive Buffer Ready Queue 0 Read Pointer

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RBRQ0RP																												0	INCWRAP	EMPTY	FULL

Bit(s)	Size	Name	Description
31-4	28	RBRQ0RP	Defines the upper 28-bits of the Receive Buffer Ready Queue 0 read pointer.
3	1	0	Program to 0.
2	1	INCWRAP	When set, the Host will increment the value of the read pointer, irrespective of the RBRQ0RP field specified on the data bus. This bit is write only and reads 0.
1	1	EMPTY	When set, indicates that the Receive Buffer Ready Queue 0 contains no data. This bit is read only
0	1	FULL	When set, indicates that the Receive Buffer Ready Queue 0 is full. This bit is read only

Register 80 - Receive Buffer Ready Queue 0 Write Pointer

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RBRQ0WP																												0	INCWRAP	EMPTY	FULL

Bit(s)	Size	Name	Description
31-4	28	RBRQ0WP	Defines the upper 28-bits of the Receive Buffer Ready Queue 0 write pointer. Updated by the **FireStream155** when adding entries to the RBRQ0.
3	1	0	Program to 0.
2	1	INCWRAP	When set, the Host will increment the value of the read pointer, irrespective of the RBRQ0WP field specified on the data bus. This bit is write only and reads 0.
1	1	EMPTY	When set, indicates that the Receive Buffer Ready Queue 0 contains no data. This bit is read only
0	1	FULL	When set, indicates that the Receive Buffer Ready Queue 0 is full. This bit is read only

Register 81 - Receive Buffer Ready Queue 0 Configuration

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0																TIME OUT		RBRIF			RBRWT										

Bit(s)	Size	Name	Description
31-16	10	0	Program to 0.
15-14	2	TIMEOUT	This value determines the maximum time before the Receive Buffer Ready Queue forces an interrupt. Only valid if RBRIF is not 0. 00 - 100us 01 - 1ms 10 - 10ms 11 - 100ms
13-11	3	RBRIF	Status Interrupt Frequency. This count specifies, in powers of 2, the frequency of Receive Buffer Ready interrupts.
10-0	11	RBRWT	This 11-bit threshold value defines the number of free entries left on the queue below which the **RBR0-NF** interrupt is generated.

Register 82 - Receive Buffer Ready Queue 1 Start Address

The format of this register is as Receive Buffer Ready Queue 0 Start Address.

Register 83 - Receive Buffer Ready Queue 1 End Address

The format of this register is as Receive Buffer Ready Queue 0 End Address.

Register 84 - Receive Buffer Ready Queue 1 Read Pointer

The format of this register is as Receive Buffer Ready Queue 0 Read Pointer.

Register 85 - Receive Buffer Ready Queue 1 Write Pointer

The format of this register is as Receive Buffer Ready Queue 0 Write Pointer.

Register 86 - Receive Buffer Ready Queue 1 Configuration

The format of this register is as Receive Buffer Ready Queue 0 Configuration.

Register 87 - Receive Buffer Ready Queue 2 Start Address

The format of this register is as Receive Buffer Ready Queue 0 Start Address.

Register 88 - Receive Buffer Ready Queue 2 End Address

The format of this register is as Receive Buffer Ready Queue 0 End Address.

Register 89 - Receive Buffer Ready Queue 2 Read Pointer

The format of this register is as Receive Buffer Ready Queue 0 Read Pointer.

Register 90 - Receive Buffer Ready Queue 2 Write Pointer

The format of this register is as Receive Buffer Ready Queue 0 Write Pointer.

Register 91 - Receive Buffer Ready Queue 2 Configuration

The format of this register is as Receive Buffer Ready Queue 0 Configuration.

Register 92 - Receive Buffer Ready Queue 3 Start Address

The format of this register is as Receive Buffer Ready Queue 0 Start Address.

Register 93 - Receive Buffer Ready Queue 3 End Address

The format of this register is as Receive Buffer Ready Queue 0 End Address.

Register 94 - Receive Buffer Ready Queue 3 Read Pointer

The format of this register is as Receive Buffer Ready Queue 0 Read Pointer.

Register 95 - Receive Buffer Ready Queue 3 Write Pointer

The format of this register is as Receive Buffer Ready Queue 0 Write Pointer.

Register 96 - Receive Buffer Ready Queue 3 Configuration

The format of this register is as Receive Buffer Ready Queue 0 Configuration.

Register 97 - Packet Ageing Timeout Interval

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0																								VATI				PATI			

Bit(s)	Size	Name	Description
31-8	24	0	Program to 0.
7-4	4	VATI	This is set to the required value of the VC timeout. The timeout value is 4ms x 2^{VATI} (range 4ms to approx. 2 minutes)
3-0	4	PATI	This is set to the required value of the packet timeout. The time-out value is 1ms x 2^{PATI} (range1ms to approx. 1/2 minute)

Register 98 - Statistics Configuration 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0																										RBRQFI	DPLOAD	DPPCE	DPPCM	DPBCE	DPBCM

Bit(s)	Size	Name	Description
31-6	26	0	Program to 0.
5	1	RBRQFI	Receive Buffer Ready Queue Full Inhibit. When set causes the the Receive Buffer Manager to discard all cells that would cause an overflow write to a full RBRQ.
4	1	DPLOAD	Dropped packet Counts load. When this bit is set it causes the values held in the statistics counters to be loaded into their respective registers. This bit resets itself after the load has been performed.
3	1	DPPCE	Dropped packets due to Low Priority Count Enable
2	1	DPPCM	Dropped packets due to Low Priority Count Mode. If set the interrupt will occur when the MSB of the counter is first set. Otherwise the counter will interrupt on the first occurrence of the error.
1	1	DPBCE	Dropped packets due to No Buffers Count Enable.
0	1	DPBCM	Dropped packets due to No Buffers Count Mode. If set the interrupt will occur when the MSB of the counter is first set. Otherwise the counter will interrupt on the first occurrence of the error.

Register 99 - Dropped Packet - No Buffers Counter

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0																								DPBC							

Bit(s)	Size	Name	Description
31-8	24	0	These bits will be 0 when read.
7-0	8	DPBC	Dropped Packet - No Buffers Count

Register 100 - Dropped Packet - Low Priority Discard Counter

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0																								DPPC							

Bit(s)	Size	Name	Description
31-8	24	0	These bits will be 0 when read.
7-0	8	DPPC	Dropped Packet - Low Priority Discard

Register 101 - Receive Timebase Counter

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0																RTC															

Bit(s)	Size	Name	Description
31-16	16	0	These bits will be 0 when read.
15-0	16	RTC	This register shows the value of the receive timebase counter in 7.68us steps (based on 33MHz LCLK). . This can be used by the host for its own purposes.

Register 102 - Reserved

Register 103 - HEC Error Counter

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0																								HECC							

Bit(s)	Size	Name	Description
31-8	24	0	These bits will be 0 when read.
7-0	8	HECC	HEC Error Count

Register 104 - CRC-10 Error Counter

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0																								CRCC							

Bit(s)	Size	Name	Description
31-8	24	0	These bits will be 0 when read.
7-0	8	CRCC	CRC-10 Error Count

Register 105 - UTOPIA Short/Long Cell Error Counter

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0																								USCC							

Bit(s)	Size	Name	Description
31-8	24	0	These bits will be 0 when read.
7-0	8	USCC	UTOPIA Short Cell Error Count

Register 106 - UTOPIA Parity Error Counter

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0																								UPRTC							

Bit(s)	Size	Name	Description
31-8	24	0	These bits will be 0 when read.
7-0	8	UPRTC	UTOPIA Parity Error Count

Register 107 - VP/VC Filter Mismatch Counter

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0																								VPFC							

Bit(s)	Size	Name	Description
31-8	24	0	These bits will be 0 when read.
7-0	8	VPFC	VP/VC Filter Mismatch Count

Register 108 - Statistics Configuration 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0																				STATS_SEL	DCLOAD	VPFCE	VPFCM	UPARCE	UPARCM	USCCE	USCCM	CRCCE	CRCCM	HECCE	HECCM

Bit(s)	Size	Name	Description
31-12	19	0	Program to 0.
11	1	STATS_SEL	Stats select. Alternative statistics can be gathered in the statistics counters if this bit is set as follows : USC : Packets discarded due to low priority threshold UPAR: Cells discarded due to buffer overflow HEC : Cells discarded for other reasons
10	1	DCLOAD	Dropped cell Counts Load.When this bit is set it causes the values held in the statistics counters to be loaded into their respective registers. This bit resets itself after the load has been performed.
9	1	VPFCE	VP/VC Filter Mismatch Count Enable.
8	1	VPFCM	VP/VC Filter Mismatch Count Mode. If set the interrupt will occur when the MSB of the counter is first set. Otherwise the counter will interrupt on the first occurrence of the error.
7	1	UPARCE	UTOPIA Parity Error Count Enable.
6	1	UPARCM	UTOPIA Parity Error Count Mode. If set the interrupt will occur when the MSB of the counter is first set. Otherwise the counter will interrupt on the first occurrence of the error.
5	1	USCCE	UTOPIA Short Cell Error Count Enable.
4	1	USCCM	UTOPIA Short Cell Error Count Mode. If set the interrupt will occur when the MSB of the counter is first set. Otherwise the counter will interrupt on the first occurrence of the error.
3	1	CRCCE	CRC-10 Error Count Enable.
2	1	CRCCM	CRC-10 Error Count Mode. If set the interrupt will occur when the MSB of the counter is first set. Otherwise the counter will interrupt on the first occurrence of the error.
1	1	HECCE	HEC Error Count Enable.
0	1	HECCM	HEC Error Count Mode. If set the interrupt will occur when the MSB of the counter is first set. Otherwise the counter will interrupt on the first occurrence of the error.

Register 109 - Reserved

Register 110 - Maximum Received Packet Length

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0																MRPL															

Bit(s)	Size	Name	Description
31-16	16	0	Program to 0.
15-0	16	MRPL	This value indicates a maximum packet length that can be selectively applied to receive channels. On enabled channels packets which exceed this length are discarded.

Register 111 - Receive Address Select 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DCD_XHLT	PRI_MODE		IVC	VPSEL												VCSEL															

Bit(s)	Size	Name	Description
31	1	DCD_XHLT	Discard(set) or Halt(clear) mode. In discard mode cells are thrown away at the input to the 96 cell buffer if it is full. In halt mode the receive path is stalled and data will be backed up to the UTOPIA interface which will in turn signal full.
30-29	2	PRI_MODE	Priority handling at input to 96 cell buffer. 00 - No cells are discarded 01 - 50% full - stop assembling new packets on low priority channels - 75% full - discard all cells on low priority channels 10 - 75% full - stop assembling new packets on low priority channels 11 - All cells on low priority channels are discarded
28	1	IVC	Interpret VC bits when checking for cell types. This allows the device to decode UNI pre-assigned cell types by comparing the VP and VC to specific combinations (e.g. This allows F4 OAM cells to be recognised and, if Dump Enable set, to be sent to the host as transparent cells using buffers from free pool 6 and are reported on ready queue 3 with F4 OAM status codes).
27-16	12	VPSEL	Bits within this field (which corresponds to the VP part of the ATM Header) should be set to indicate that they should be used as part of the receive address lookup
15-0	16	VCSEL	Bits within this field (which corresponds to the VC part of the ATM Header) should be set to indicate that they should be used as part of the receive address lookup

Register 112 - Receive Address Select 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0																						UTREG					UTSEL				

Bit(s)	Size	Name	Description
31-10	22	0	Program to 0.
9-5	5	UTREG	**UTOPIA ATM** - This field should be set to indicate the limit on the UTOPIA polling counter. **UTOPIA PHY** - The value in this register is the UTOPIA address of the **FireStream155**.
4-0	5	UTSEL	Bits within this field (which corresponds to the Receive UTOPIA address) should be set to indicate that they should be used as part of the receive address lookup.

Register 113 - Receive Address Mask

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0									MASK																						

Bit(s)	Size	Name	Description
31-23	9	0	Program to 0.
22-0	23	MASK	These bits are used to define a filter mask for those bits in the ATM header not covered by the select bits. If set the equivalent bit in the compare register is tested for equality with the corresponding bit in the ATM Header.

Register 114 - Receive Address Compare

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0									COMP																						

Bit(s)	Size	Name	Description
31-23	9	0	Program to 0.
22-0	23	COMP	These bits are compared against corresponding bits in the ATM Header if the associated Receive Address Mask Register bit is set.

Register 115 - DMA Mode Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0																														TX_MODE	

Bit(s)	Size	Name	Description	
1:0	2	TX_MODE	Defines the TX Pipeline mode of operation.	
			`00`	Full TX Pipeline Operation allows up to 3 outstanding TX Payload Requests to be active at any one time. (recommended).
			`01`	Partial TX Pipeline Operation allows upto 2 outstanding TX Payload Requests to be active at any time.
			`10`	No TX Pipeline Operation
			`11`	No TX Pipeline Operation
31:2	30	0	Program to 0.	

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C Ratings

C.1 DC Characteristics

Parameter		Symbol	Test Condition	Ratings			Unit
				Min	Typ	Max	
Positive Supply Current		$+I_{DDS1}$	Static no load	-	-	1.0	mA
Positive Supply Current PCI		$+I_{DDS2}$	Static no load	-	-	0.2	mA
Input High Voltage		V_{IH1}		V_{DD1} x 0.65	-	V_{DD1}	V
Input High Voltage (5V tolerant pin)		V_{IH2}		V_{DD1} x 0.65	-	5.25	V
Input High Voltage PCI	V_{DD2} 5V	V_{IH3}		2.0	-	V_{DD2} + 0.5	V
	V_{DD2} 3.3V	V_{IH4}		V_{DD2} x 0.5	-	V_{DD2} + 0.5	V
Input Low Voltage		V_{IL1}		0	-	V_{DD1} x 0.25	V
Input Low Voltage PCI	V_{DD2} 5V	V_{IL2}		-0.5	-	0.8	V
	V_{DD2} 3.3V	V_{IL3}		-0.5	-	V_{DD2} x 0.3	V
Input Leakage Current		I_{LI}	$0<=V_I<=+V_{DD}$	-10	-	10	µA
Output Low Voltage		V_{OL1}	I_{OL}=8mA	V_{SS}	-	0.4	V
Output High Voltage		V_{OH1}	I_{OH}=-8mA	V_{DD}-0.5	-	V_{DD1}	V
Output Low Voltage		V_{OL2}	I_{OL}=4mA	V_{SS}	-	0.4	V
Output High Voltage		V_{OH2}	I_{OH}=-4mA	V_{DD1}-0.5	-	V_{DD1}	V
Output Low Voltage PCI	V_{DD2} 3.3V	V_{OL3}	I_{OL}=1.5mA	V_{SS}	-	$0.1V_{DD2}$	V
	V_{DD2} 5V	V_{OL4}	I_{OL}=6mA	V_{SS}	-	0.55	V
Output High Voltage PCI	V_{DD2} 3.3V	V_{OH3}	I_{OH}=-0.5mA	$0.9V_{DD2}$	-	V_{DD2}	V
	V_{DD2} 5V	V_{OH4}	I_{OH}=-2mA	2.4	-	V_{DD2}	V
Output Off Leakage Current		I_{LO}		-10	-	10	µA
Power Dissipation (operating)		P_O		-	1.4	-	W

Note: All PCI output drivers conform to $V_{OL/OH3/4}$. Pins LD[31:0], EDO, ECS, ECK and TDO have 4mA drive and conform to $V_{OH/OL2}$. All other output drivers are 8mA drive and conform to $V_{OH/OL1}$.

C.2 Recommended Operating Conditions

Parameter	Symbol	Ratings			Units
		Min	Typ	Max	
Positive Supply Voltage	V_{DD1}	3.0	3.3	3.6	V
Positive Supply Voltage (PCI)	V_{DD2}	3.0	3.3/5.0	5.25	V
Ambient Operating Temperature	T_A	-40		85	°C

C.3 Absolute Maximum Ratings

Parameter	Symbol	Ratings		Units
		Min	Max	
Positive Supply Voltage	V_{DD1}	-0.5	4.0	V
Positive Supply Voltage (PCI)	V_{DD2}	-0.5	6.0	V
Input Voltage (5V tolerant pin) (See Note)	V_{DIN5}	-0.5	6.0	V
Input Voltage (normal pin)	V_{DIN}	-0.5	4.0	V
Output Voltage	V_{O1}	-0.5	V_{DD1}+0.5	V
Output Voltage (PCI)	V_{O2}	-0.5	V_{DD2}+0.5	V
Storage Temperature	T_{STG}	-55	125	^oC

Note: All input pins are 5V tolerant but bidirectional pins (LD[31:0], CSIPADR[4:0] and CSOPADR[4:0]) are not. All output/bidirectional pins can drive into 5V TTL inputs.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.
Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.
No warranty is made with respect to uses , operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

D AC Timing Characteristics

D.1 PCI Interface

Parameter	Signal	Abbrev.	Values			Units
			Min	Typ	Max	
PCI Clock Period	PCLK	t_{PCLKP}	30			ns
PCI Clock Low Time	PCLK	t_{PCLKL}	11			ns
PCI Clock High Time	PCLK	t_{PCLKH}	11			ns
PCI Input Setup (bussed signals)	AD[31:0], C/$\overline{BE}$[3:0], PAR, $\overline{FRAME}$, $\overline{TRDY}$, $\overline{IRDY}$ $\overline{STOP}$, IDSEL, $\overline{DEVSEL}$, $\overline{PERR}$	t_{PS}	7			ns
PCI Input Setup (point-to-point signals)	$\overline{GNT}$	t_{PSP}	10			ns
PCI Input Hold	AD[31:0], C/$\overline{BE}$[3:0], PAR, $\overline{FRAME}$, $\overline{TRDY}$, $\overline{IRDY}$ $\overline{STOP}$, IDSEL, $\overline{DEVSEL}$, $\overline{GNT}$, $\overline{PERR}$	t_{PH}	0			ns
PCI Output Delay	AD[31:0], C/$\overline{BE}$[3:0], PAR, $\overline{FRAME}$, $\overline{TRDY}$, $\overline{IRDY}$, $\overline{STOP}$, $\overline{DEVSEL}$, REQ, $\overline{PERR}$, $\overline{SERR}$	t_{PD}	2		11	ns

Table 119 PCI Interface Timings

D.2 UTOPIA Interface

Parameter	Signal	Abbrev.	Values			Units
			Min	Typ	Max	
UTOPIA Clock Period	CSOPCLK CSIPCLK	t_{UCLKP}	20			ns
UTOPIA Clock Low Time	CSOPCLK CSIPCLK	t_{UCLKL}	8			ns
UTOPIA Clock High Time	CSOPCLK CSIPCLK	t_{UCLKH}	8			ns
UTOPIA Input Setup	CSIPDATA[15:0] CSIPSOC CSIPPAR CSIPFCI CSOPFCI CSIPADDR[4:0] CSOPADDR[4:0]	t_{US}	4			ns
UTOPIA Input Hold	CSIPDATA[15:0] CSIPSOC CSIPPAR CSIPFCI CSOPFCI CSIPADDR[4:0] CSOPADDR[4:0]	t_{UH}	1			ns
UTOPIA Output Delay	CSOPDATA[15:0] CSOPSOC CSOPPAR CSIPFCO CSOPFCO CSIPADDR[4:0] CSOPADDR[4:0]	t_{UD}	2		15	ns

Table 120 UTOPIA Interface Timings

D.3 Local Interface

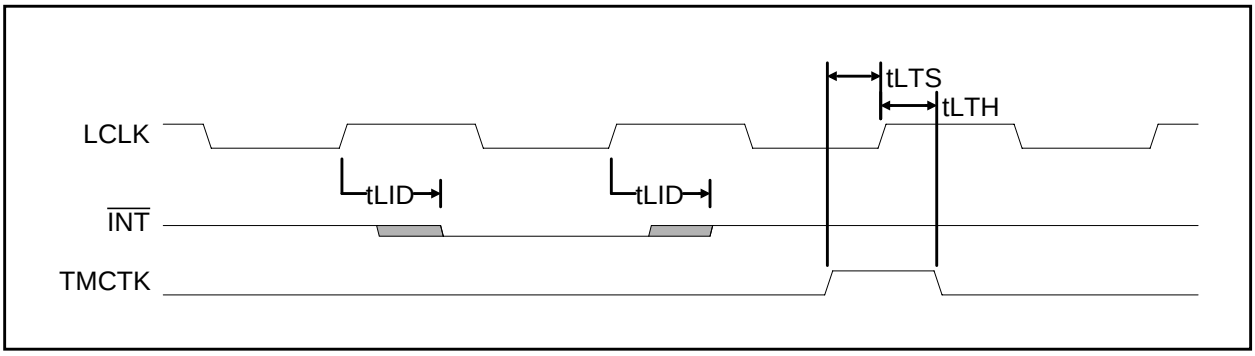

Figure 12 Local Interface Timings

Parameter	Signal	Abbrev.	Values			Units
			Min	Typ	Max	
Local Clock Period	LCLK	t_{LCLKP}	30			ns
Local Clock Low Time	LCLK	t_{LCLKL}	12			ns
Local Clock High Time	LCLK	t_{LCLKH}	12			ns
Interrupt Delay	$\overline{INT}$	t_{LID}	2		15	ns
TM Tick Setup	TMTK	t_{LTS}	10			ns
TM Tick Hold	TMTK	t_{LTH}	0			ns

Table 121 Local Interface Timings

D.4 SRAM Interface

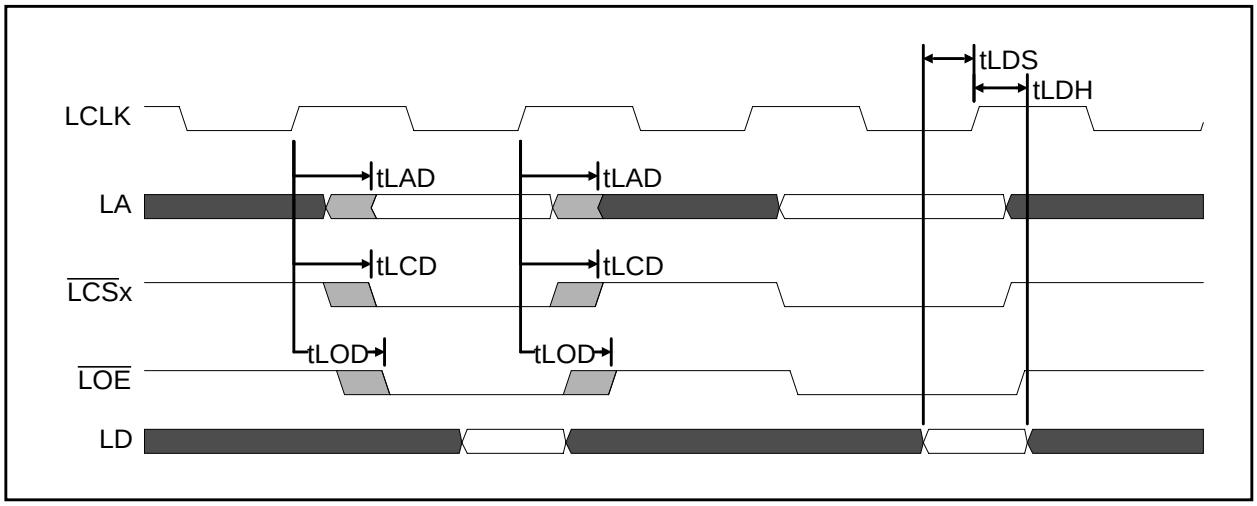

Figure 13 SRAM Read Timing

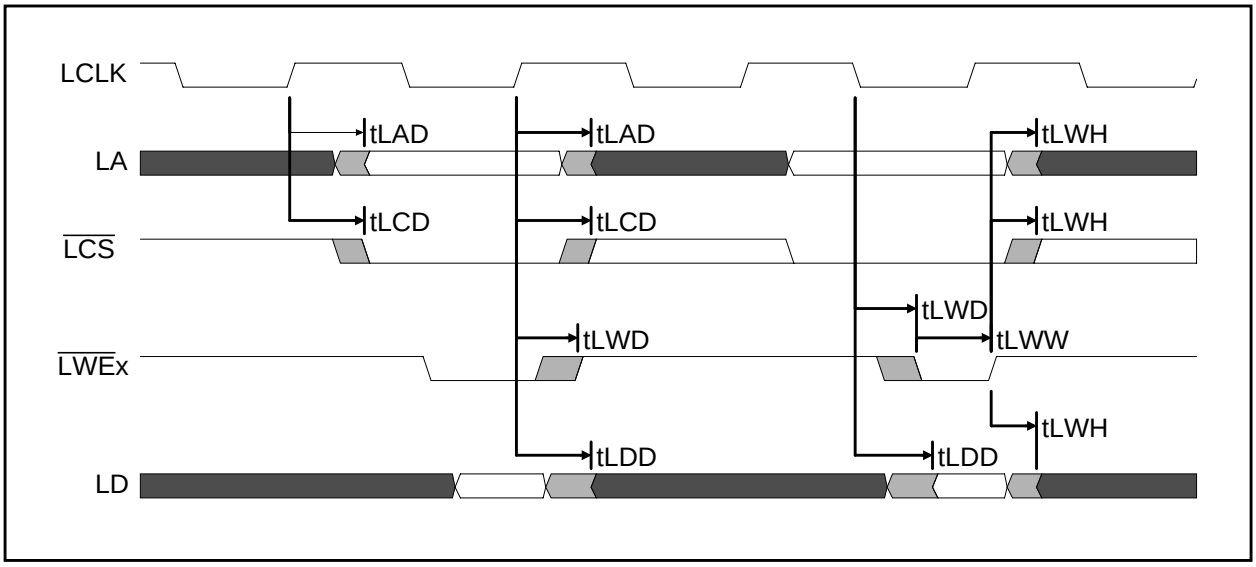

Figure 14 SRAM Write Timing

Parameter	Signal	Abbrev.	Values			Units
			Min	Typ	Max	
LRAM Data Setup	LD[31:0]	t_{LDS}	0.5			ns
LRAM Data Hold	LD[31:0]	t_{LDH}	3.5			ns
LRAM Data Delay	LD[31:0]	t_{LDD}	3		11	ns
LRAM Address Delay	LA[18:0]	t_{LAD}	2		9.5	ns
LRAM $\overline{OE}$ Delay	$\overline{LOE}$	t_{LOD}	5		14	ns
LRAM $\overline{CS}$ Delay	$\overline{LCS}$[3:0]	t_{LCD}	2		10	ns
LRAM $\overline{WE}$ Delay	$\overline{LWE}$[1:0]	t_{LWD}	1		6	ns
LRAM $\overline{WE}$ Width	$\overline{LWE}$[1:0]	t_{LWW}	12		18	ns
LRAM Address / Data / $\overline{CS}$ Hold from $\overline{WE}$	LA[1:0], LD[31:0], $\overline{LCS}$[3:0]	t_{LWH}	1			ns

Table 122 SRAM Interface Timings

D.5 EEPROM Interface

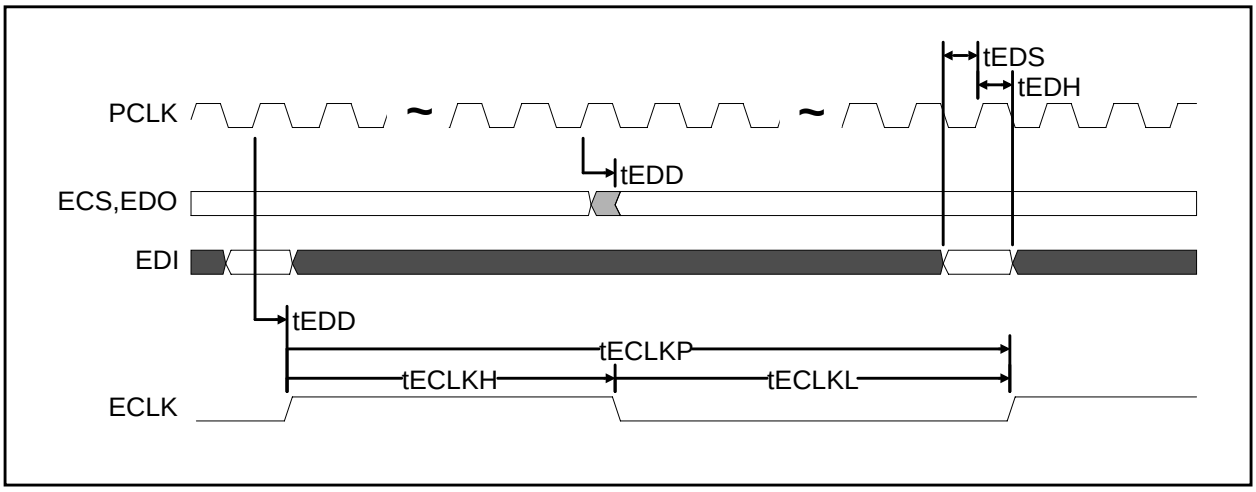

Figure 15 EEPROM Interface Timings

Parameter	Signal	Abbrev.	Values			Units
			Min	Typ	Max	
EEPROM Data Setup	EDI	t_{EDS}	5			ns
EEPROM Data Hold	EDI	t_{EDH}	5			ns
EEPROM Data Delay	EDO, ECK, ECS	t_{EDD}	3		20	ns
EEPROM Clock Period	ECK	t_{ECLKP}	1000			ns
EEPROM Clock Low Time	ECK	t_{ECLKL}	500			ns
EEPROM Clock High Time	ECK	t_{ECLKH}	500			ns

Table 123 EEPROM Interface Timings

D.6 JTAG Interface

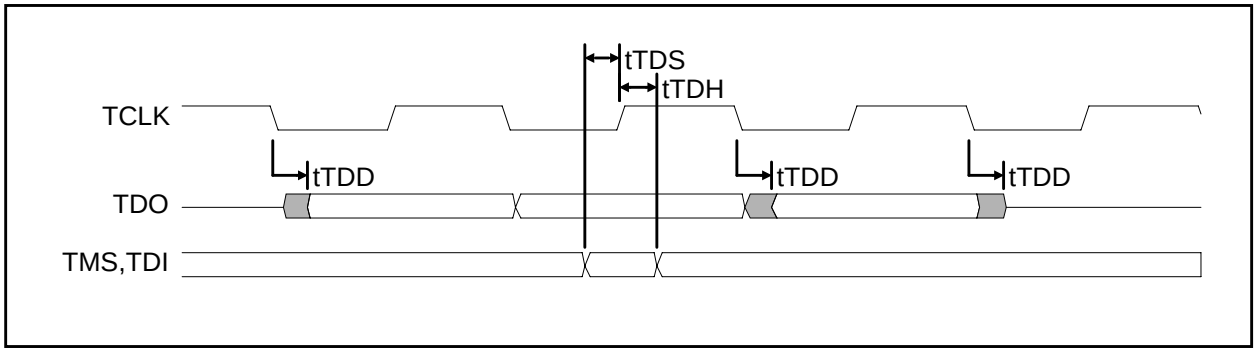

Figure 16 JTAG Interface Timings

Parameter	Signal	Abbrev.	Values			Units
			Min	Typ	Max	
JTAG Clock Period	TCLK	t_{TCLKP}	50			ns
JTAG Clock Low Time	TCLK	t_{TCLKL}	20			ns
JTAG Clock High Time	TCLK	t_{TCLKH}	20			ns
JTAG Data Setup	TMS, TDI	t_{TDS}	10			ns
JTAG Data Hold	TMS, TDI	t_{TDH}	10			ns
JTAG Data Delay	TDO	t_{TDD}	2		15	ns

Table 124 JTAG Interface Timings

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E JTAG

The **FireStream155** conforms to IEEE JTAG Test Port and Boundary Scan architecture 1149.1 (1990). The **FireStream155** supports the JTAG ports specified in section 2.2.4.1 - JTAG Interface.

The **FireStream155** supports the following mandatory JTAG instructions;

- Bypass (11)
- Sample / Preload (01)
- Extest (00)

A full BSDL file describing the JTAG connectivity can be supplied on request by contacting your local Fujitsu representative.

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F Pin Assignments

F.1 Pin Diagram

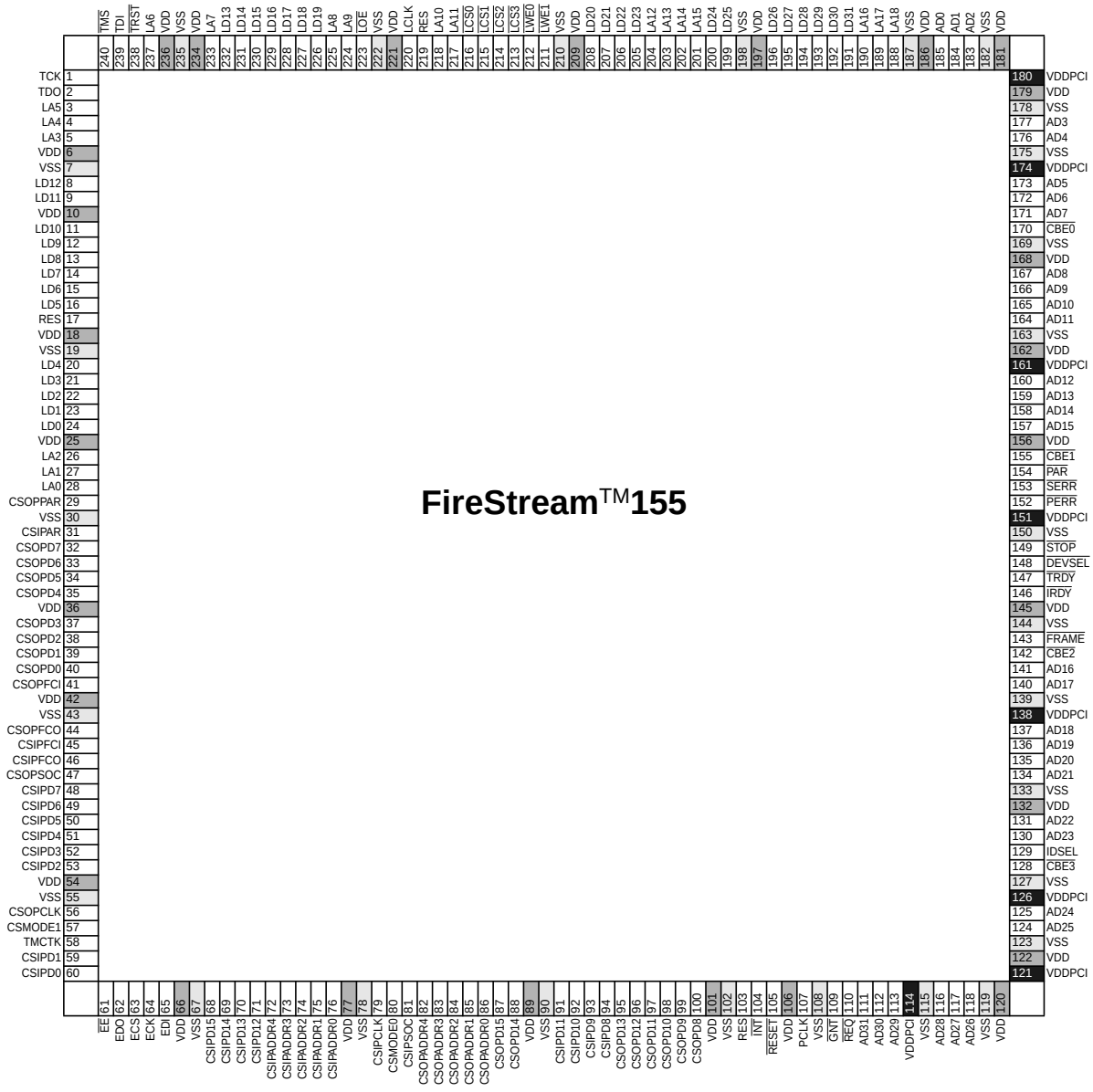

Figure 17 Pin Assignments

F.2 Pin Assignments

Package Pad Number	Pin Name	Type	Description
1	TCK	I	JTAG Clock
2	TDO	T	JTAG Test Data Output
3	LA5	O	SRAM Address Bit 5
4	LA4	O	SRAM Address Bit 4
5	LA3	O	SRAM Address Bit 3
6	VDD	-	
7	VSS	-	
8	LD12	B	SRAM Data Bit 12
9	LD11	B	SRAM Data Bit 11
10	VDD	-	
11	LD10	B	SRAM Data Bit 10
12	LD9	B	SRAM Data Bit 9
13	LD8	B	SRAM Data Bit 8
14	LD7	B	SRAM Data Bit 7
15	LD6	B	SRAM Data Bit 6
16	LD5	B	SRAM Data Bit 5
17	Reserved	I(D)	Tie to VSS
18	VDD	-	
19	VSS	-	
20	LD4	B	SRAM Data Bit 4
21	LD3	B	SRAM Data Bit 3
22	LD2	B	SRAM Data Bit 2
23	LD1	B	SRAM Data Bit 1
24	LD0	B	SRAM Data Bit 0
25	VDD	-	
26	LA2	O	SRAM Address Bit 2
27	LA1	O	SRAM Address Bit 1
28	LA0	O	SRAM Address Bit 0
29	CSOPPAR	T	UTOPIA Output Parity
30	VSS	-	
31	CSIPPAR	I	UTOPIA Input Parity
32	CSOPD7	T	UTOPIA Output Data Bit 7
33	CSOPD6	T	UTOPIA Output Data Bit 6
34	CSOPD5	T	UTOPIA Output Data Bit 5
35	CSOPD4	T	UTOPIA Output Data Bit 4
36	VDD	-	
37	CSOPD3	T	UTOPIA Output Data Bit 3
38	CSOPD2	T	UTOPIA Output Data Bit 2
39	CSOPD1	T	UTOPIA Output Data Bit 1
40	CSOPD0	T	UTOPIA Output Data Bit 0

Table 125 Pin Assignments

Package Pad Number	Pin Name	Type	Description
41	CSOPFCI	I	UTOPIA Flow Control
42	VDD	-	
43	VSS	-	
44	CSOPFCO	T	UTOPIA Flow Control
45	CSIPFCI	I	UTOPIA Flow Control
46	CSIPFCO	T	UTOPIA Flow Control
47	CSOPSOC	T	UTOPIA Output Start of Cell
48	CSIPD7	I	UTOPIA Input Data Bit 7
49	CSIPD6	I	UTOPIA Input Data Bit 6
50	CSIPD5	I	UTOPIA Input Data Bit 5
51	CSIPD4	I	UTOPIA Input Data Bit 4
52	CSIPD3	I	UTOPIA Input Data Bit 3
53	CSIPD2	I	UTOPIA Input Data Bit 2
54	VDD	-	
55	VSS	-	
56	CSOPCLK	I	UTOPIA Output Clock
57	CSMODE1	I	UTOPIA Mode Bit 1
58	TMCTK	I	Traffic Manager Calendar Tick
59	CSIPD1	I	UTOPIA Input Data Bit 1
60	CSIPD0	I	UTOPIA Input Data Bit 0
61	$\overline{EE}$	I(D)	EEPROM Enable
62	EDO	O	EEPROM Data Out
63	ECS	O	EEPROM Chip Select
64	ECK	O	EEPROM Clock
65	EDI	I	EEPROM Data in
66	VDD	-	
67	VSS	-	
68	CSIPD15	I	UTOPIA Input Data Bit 15
69	CSIPD14	I	UTOPIA Input Data Bit 14
70	CSIPD13	I	UTOPIA Input Data Bit 13
71	CSIPD12	I	UTOPIA Input Data Bit 12
72	CSIPADDR4	B	UTOPIA Input Address Bit 4
73	CSIPADDR3	B	UTOPIA Input Address Bit 3
74	CSIPADDR2	B	UTOPIA Input Address Bit 2
75	CSIPADDR1	B	UTOPIA Input Address Bit 1
76	CSIPADDR0	B	UTOPIA Input Address Bit 0
77	VDD	-	
78	VSS	-	
79	CSIPCLK	I	UTOPIA Input Clock
80	CSMODE0	I	UTOPIA Mode Bit 0
81	CSIPSOC	I	UTOPIA Input Start of Cell
82	CSOPADDR4	B	UTOPIA Output Address Bit 4
83	CSOPADDR3	B	UTOPIA Output Address Bit 3

Table 125 Pin Assignments

Package Pad Number	Pin Name	Type	Description
84	CSOPADDR2	B	UTOPIA Output Address Bit 2
85	CSOPADDR1	B	UTOPIA Output Address Bit 1
86	CSOPADDR0	B	UTOPIA Output Address Bit 0
87	CSOPD15	T	UTOPIA Output Data Bit 15
88	CSOPD14	T	UTOPIA Output Data Bit 14
89	VDD	-	
90	VSS	-	
91	CSIPD11	I	UTOPIA Input Data Bit 11
92	CSIPD10	I	UTOPIA Input Data Bit 10
93	CSIPD9	I	UTOPIA Input Data Bit 9
94	CSIPD8	I	UTOPIA Input Data Bit 8
95	CSOPD13	T	UTOPIA Output Data Bit 13
96	CSOPD12	T	UTOPIA Output Data Bit 12
97	CSOPD11	T	UTOPIA Output Data Bit 11
98	CSOPD10	T	UTOPIA Output Data Bit 10
99	CSOPD9	T	UTOPIA Output Data Bit 9
100	CSOPD8	T	UTOPIA Output Data Bit 8
101	VDD	-	
102	VSS	-	
103	Reserved	I	Connect to VSS
104	$\overline{\text{INT}}$	T(D)	PCI Interrupt
105	$\overline{\text{RESET}}$	I	PCI Reset
106	VDD	--	
107	PCLK	I	PCI Clock
108	VSS	-	
109	$\overline{\text{GNT}}$	I	PCI Grant
110	$\overline{\text{REQ}}$	T	PCI Request
111	AD31	B	PCI Address/Data Bit 31
112	AD30	B	PCI Address/Data Bit 30
113	AD29	B	PCI Address/Data Bit 29
114	VDDPCI	-	
115	VSS	-	
116	AD28	B	PCI Address/Data Bit 28
117	AD27	B	PCI Address/Data Bit 27
118	AD26	B	PCI Address/Data Bit 26
119	VSS	-	
120	VDD	-	
121	VDDPCI	-	
122	VDD	-	
123	VSS	-	
124	AD25	B	PCI Address/Data Bit 25
125	AD24	B	PCI Address/Data Bit 24
126	VDDPCI	-	

Table 125 Pin Assignments

Package Pad Number	Pin Name	Type	Description
127	VSS	-	
128	$\overline{CBE3}$	B	PCI Command/Byte Enable Bit 3
129	IDSEL	I	PCI IDSEL
130	AD23	B	PCI Address/Data Bit 23
131	AD22	B	PCI Address/Data Bit 22
132	VDD	-	
133	VSS	-	
134	AD21	B	PCI Address/Data Bit 21
135	AD20	B	PCI Address/Data Bit 20
136	AD19	B	PCI Address/Data Bit 19
137	AD18	B	PCI Address/Data Bit 18
138	VDDPCI	-	
139	VSS	-	
140	AD17	B	PCI Address/Data Bit 17
141	AD16	B	PCI Address/Data Bit 16
142	$\overline{CBE2}$	B	PCI Command/Byte Enable Bit 2
143	$\overline{FRAME}$	B	PCI Frame
144	VSS	-	
145	VDD	-	
146	$\overline{IRDY}$	B	PCI IRDY
147	$\overline{TRDY}$	B	PCI TRDY
148	$\overline{DEVSEL}$	B	PCI DEVSEL
149	$\overline{STOP}$	B	PCI STOP
150	VSS	-	
151	VDDPCI	-	
152	$\overline{PERR}$	B	PCI PERR
153	$\overline{SERR}$	T(D)	PCI SERR
154	$\overline{PAR}$	B	PCI PAR
155	$\overline{CBE1}$	B	PCI Command/Byte Enable Bit 1
156	VDD	-	
157	AD15	B	PCI Address/Data Bit 15
158	AD14	B	PCI Address/Data Bit 14
159	AD13	B	PCI Address/Data Bit 13
160	AD12	B	PCI Address/Data Bit 12
161	VDDPCI	-	
162	VDD	-	
163	VSS	-	
164	AD11	B	PCI Address/Data Bit 11
165	AD10	B	PCI Address/Data Bit 10
166	AD9	B	PCI Address/Data Bit 9
167	AD8	B	PCI Address/Data Bit 8
168	VDD	-	
169	VSS	-	

Table 125 Pin Assignments

Package Pad Number	Pin Name	Type	Description
170	CBE0	B	PCI Command/Byte Enable Bit 0
171	AD7	B	PCI Address/Data Bit 7
172	AD6	B	PCI Address/Data Bit 6
173	AD5	B	PCI Address/Data Bit 5
174	VDDPCI	-	
175	VSS	-	
176	AD4	B	PCI Address/Data Bit 4
177	AD3	B	PCI Address/Data Bit 3
178	VSS	-	
179	VDD	-	
180	VDDPCI	-	
181	VDD	-	
182	VSS	-	
183	AD2	B	PCI Address/Data Bit 2
184	AD1	B	PCI Address/Data Bit 1
185	AD0	B	PCI Address/Data Bit 0
186	VDD	-	
187	VSS	-	
188	LA18	O	SRAM Address Bit 18
189	LA17	O	SRAM Address Bit 17
190	LA16	O	SRAM Address Bit 16
191	LD31	B	SRAM Data Bit 31
192	LD30	B	SRAM Data Bit 30
193	LD29	B	SRAM Data Bit 29
194	LD28	B	SRAM Data Bit 28
195	LD27	B	SRAM Data Bit 27
196	LD26	B	SRAM Data Bit 26
197	VDD	-	
198	VSS	-	
199	LD25	B	SRAM Data Bit 25
200	LD24	B	SRAM Data Bit 24
201	LA15	O	SRAM Address Bit 15
202	LA14	O	SRAM Address Bit 14
203	LA13	O	SRAM Address Bit 13
204	LA12	O	SRAM Address Bit 12
205	LD23	B	SRAM Data Bit 23
206	LD22	B	SRAM Data Bit 22
207	LD21	B	SRAM Data Bit 21
208	LD20	B	SRAM Data Bit 20
209	VDD	-	
210	VSS	-	
211	$\overline{\text{LWE1}}$	O	SRAM Upper Word Write Enable
212	$\overline{\text{LWE0}}$	O	SRAM Lower Word Write Enable

Table 125 Pin Assignments

Package Pad Number	Pin Name	Type	Description
213	LCS3	O	SRAM Bank 3 Chip Select
214	$\overline{\text{LCS2}}$	O	SRAM Bank 2 Chip Select
215	$\overline{\text{LCS1}}$	O	SRAM Bank 1 Chip Select
216	$\overline{\text{LCS0}}$	O	SRAM Bank 0 Chip Select
217	LA11	O	SRAM Address Bit 11
218	LA10	O	SRAM Address Bit 10
219	Reserved	I(D)	Tie to VSS
220	LCLK	I	SRAM Clock
221	VDD	-	
222	VSS	-	
223	$\overline{\text{LOE}}$	O	SRAM Output Enable
224	LA9	O	SRAM Address Bit 9
225	LA8	O	SRAM Address Bit 8
226	LD19	B	SRAM Data Bit 19
227	LD18	B	SRAM Data Bit 18
228	LD17	B	SRAM Data Bit 17
229	LD16	B	SRAM Data Bit 16
230	LD15	B	SRAM Data Bit 15
231	LD14	B	SRAM Data Bit 14
232	LD13	B	SRAM Data Bit 13
233	LA7	O	SRAM Address Bit 7
234	VDD	-	
235	VSS	-	
236	VDD	-	
237	LA6	O	SRAM Address Bit 6
238	$\overline{\text{TRST}}$	I(U)	JTAG Reset
239	TDI	I(U)	JTAG Data Input
240	$\overline{\text{TMS}}$	I(U)	JTAG Mode Select

Table 125 Pin Assignments

Notes:

- **I** Input (U) Pull-up (D) Pull Down.
- **O** Output
- **T**Tri-state (D) Open Drain.
- **B** Bidirectional.
- VDDPCI can be 3.3V or 5V depending on the PCI system environment. VDD must be 3.3V only

INTENTIONALLY

LEFT

BLANK

G Package Dimensions

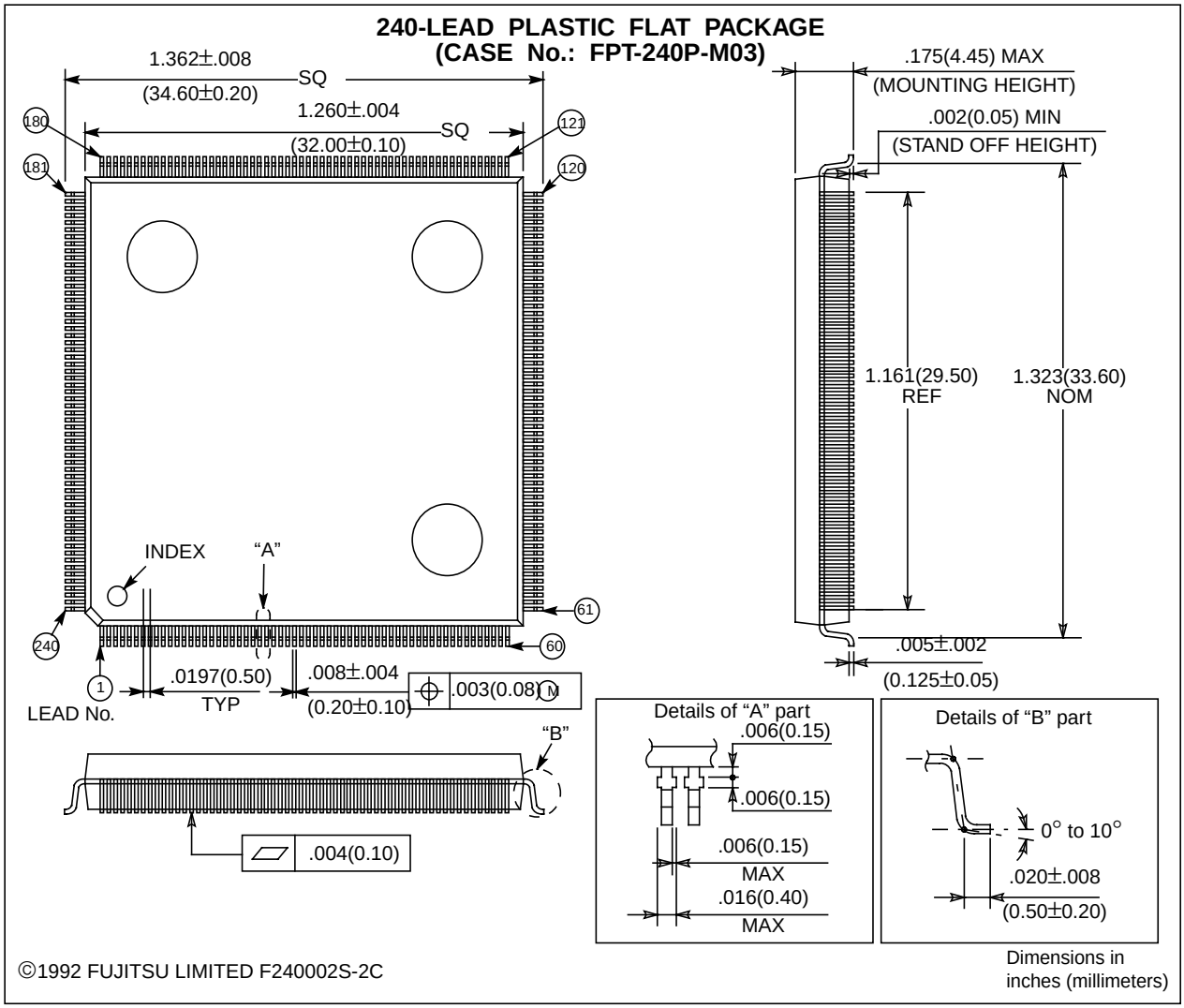

Figure 18 Package Dimensions

INTENTIONALLY

LEFT

BLANK

H Glossary of Terms

Buffer Free Pool - A linked list of Descriptors associated with empty data buffers. The SAR Device will acquire buffers from a Buffer Free Pool to write receive data to.

CD - See Command Descriptor

Channel Queue - The SAR Device maintains a linked list of scheduled commands and transmit data in Shared Memory for a particular channel. This is known as a Channel Queue.

CIF Mode - **Cells in Frames Mode.** A mode of operation whereby receive data buffers are terminated due to changes in the ATM Header or Overhead cells.

Command Descriptor - A Descriptor containing a pointer to a buffer containing commands rather than data

CSQ - See Command Status Queue.

Command Status Queue - When the SAR Device executes a command, it will pass the status of the command execution, along with any returned parameters, to the Host via an entry on the Command Status Queue.

Descriptor - An area of shared memory containing the linked list control information associated with a data buffer. Limited control information is also be provided in a descriptor.

Double-Word (DWord) - 32 bits; 4 bytes.

Host - User Software providing Control of the SAR Device.

HTPQ - High Priority Transmit Pending Queue

LRAM - See Local RAM.

Local RAM - An area of SRAM accessed by the SAR Device which is used to store current channel configuration and status information.

LTPQ - Low Priority Transmit Pending Queue

OTPQ - On-chip Transmit Pending Queue

Packet Mode - A mode of operation whereby only complete packets are passed between the Host and the SAR Device. The packet may be in a single buffer, or multiple buffers.

Quad-Word (QWord) - 64 bits; 8 bytes.

RBRQ - See Receive Buffer Ready Queue.

RD	-	Receive Descriptor.
Receive Buffer Ready Queue	-	Information regarding received data is passed from the SAR Device to the Host via this queue.
Reserved	-	A field in a data structure that is reserved for future expansion. This field will not be used either by the SAR Device, nor by the Host software. Any read-modify-write operation of a word must preserve the contents of this field.
Shared Memory	-	An area of memory accessible by both the Host and the SAR.
Streaming Mode	-	A mode of operation whereby partial packets are passed.
TBRQ	-	See Transmit Buffer Release Queue.
TD	-	Transmit Descriptor.
TRANSP	-	Transparent Payload Mode. A mode of operation whereby no AAL processing is performed.
TRANSPC	-	Transparent Cell Mode. A mode of operation whereby the Host provides cell data for Transmission, including the Cell header.
Transmit Buffer Release Queue	-	When the **FireStream155** has transmitted data, it will inform the Host via an entry on the Transmit Buffer Release Queue. This entry also returned the used data buffer to the Host.
Transparent Mode	-	A mode of operation where the SAR Device performs no AAL processing.
Unused	-	A field in a data structure that is not used by the SAR device. It is available for Host software use.
Word	-	16 bits; 2 bytes.

Revision Control

Revision Number	Date	Description of the Changes
1.0	14:08:98	Initial Release
1.1	17:11:98	Corrections to Table1, Table11, Fig120 and Table122
2.0	10:02:99	Change to MB86697A plus corrections
2.1	07:04:99	Finalised AC timings, corrected pin 144 in Table125 to VSS
2.2	09:08:99	Updated Appendix C
2.3	04.04.00	Clarified appendix C, various minor corrections.

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