LPC2104/2105/2106

Single-chip 32-bit microcontrollers; 128 kB ISP/IAP flash with 16/32/64 kB RAM

Rev. 07 — 20 June 2008 Product data sheet

1. General description

The UART are based on a 16/32-bit ARM7TDMI-S CPU with real-time emulation and embedded trace support, together with 128 kB of embedded high speed flash memory. A 128-bit wide memory interface and a unique accelerator architecture enable 32-bit code execution at maximum clock rate. For critical code size applications, the alternative 16-bit Thumb mode reduces code by more than 30 % with minimal performance penalty.

Due to their tiny size and low power consumption, these microcontrollers are ideal for applications where miniaturization is a key requirement, such as access control and point-of-sale. With a wide range of serial communications interfaces and on-chip SRAM options up to 64 kB, they are very well suited for communication gateways and protocol converters, soft modems, voice recognition and low end imaging, providing both large buffer size and high processing power. Various 32-bit timers, PWM channels, and 32 GPIO lines make these microcontrollers particularly suitable for industrial control and medical systems.

Remark: Throughout the data sheet, the term LPC2104/2105/2106 will apply to devices with and without /00 and /01 suffixes. Suffixes will be used to differentiate devices whenever they include new features.

2. Features

2.1 New features implemented in LPC2104/2105/2106/01 devices

- Fast GPIO port enables port pin toggling up to 3.5 times faster than the original device and also allows for a port pin to be read at any time regardless of its function.
- UART 0/1 include fractional baud rate generator, autobauding capabilities, and handshake flow-control fully implemented in hardware.
- Buffered SSP serial controller supporting SPI, 4-wire SSI, and Microwire formats.
- SPI programmable data length and master mode enhancement.
- Diversified Code Read Protection (CRP) enables different security levels to be implemented.
- General purpose timers can operate as external event counters.

2.2 Key common features

- 16/32-bit ARM7TDMI-S processor.
- 16/32/64 kB on-chip static RAM.
- 128 kB on-chip flash program memory. 128-bit-wide interface/accelerator enables high speed 60 MHz operation.

founded by Philips

- In-System Programming (ISP) and In-Application Programming (IAP) via on-chip bootloader software. Flash programming takes 1 ms per 512 B line. Single sector or full chip erase takes 400 ms.
- Vectored Interrupt Controller with configurable priorities and vector addresses.
- EmbeddedICE-RT interface enables breakpoints and watch points. Interrupt service routines can continue to execute whilst the foreground task is debugged with the on-chip RealMonitor software.
- Embedded Trace Macrocell enables non-intrusive high speed real-time tracing of instruction execution.
- Multiple serial interfaces including two UARTs (16C550), Fast I^2C-bus (400 kbit/s), and SPI.
- Two 32-bit timers (7 capture/compare channels), PWM unit (6 outputs), Real Time Clock and Watchdog.
- Up to thirty-two 5 V tolerant general purpose I/O pins in a tiny LQFP48 (7 mm $\times$ 7 mm) package.
- 60 MHz maximum CPU clock available from programmable on-chip Phase-Locked Loop with settling time of 100 µs.
- The on-chip crystal oscillator should have an operating range of 1 MHz to 25 MHz.
- Two low power modes, Idle and Power-down.
- Processor wake-up from Power-down mode via external interrupt.
- Individual enable/disable of peripheral functions for power optimization.
- Dual power supply:
  - CPU operating voltage range of 1.65 V to 1.95 V (1.8 V $\pm$ 8.3 %).
  - I/O power supply range of 3.0 V to 3.6 V (3.3 V $\pm$ 10 %) with 5 V tolerant I/O pads.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC2104BBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 $\times$ 7 $\times$ 1.4 mm	SOT313-2
LPC2104FBD48/00	LQFP48	plastic low profile quad flat package; 48 leads; body 7 $\times$ 7 $\times$ 1.4 mm	SOT313-2
LPC2104FBD48/01	LQFP48	plastic low profile quad flat package; 48 leads; body 7 $\times$ 7 $\times$ 1.4 mm	SOT313-2
LPC2105BBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 $\times$ 7 $\times$ 1.4 mm	SOT313-2
LPC2105FBD48/00	LQFP48	plastic low profile quad flat package; 48 leads; body 7 $\times$ 7 $\times$ 1.4 mm	SOT313-2
LPC2105FBD48/01	LQFP48	plastic low profile quad flat package; 48 leads; body 7 $\times$ 7 $\times$ 1.4 mm	SOT313-2
LPC2106BBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 $\times$ 7 $\times$ 1.4 mm	SOT313-2
LPC2106FBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 $\times$ 7 $\times$ 1.4 mm	SOT313-2

© NXP B.V. 2008. All rights reserved.

Table 1. Ordering information *…continued*

Type number	Package		
	Name	Description	Version
LPC2106FBD48/00	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC2106FBD48/01	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC2106FHN48	HVQFN48	plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 × 7 × 0.85 mm	SOT619-1
LPC2106FHN48/00	HVQFN48	plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 × 7 × 0.85 mm	SOT619-1
LPC2106FHN48/01	HVQFN48	plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 × 7 × 0.85 mm	SOT619-1

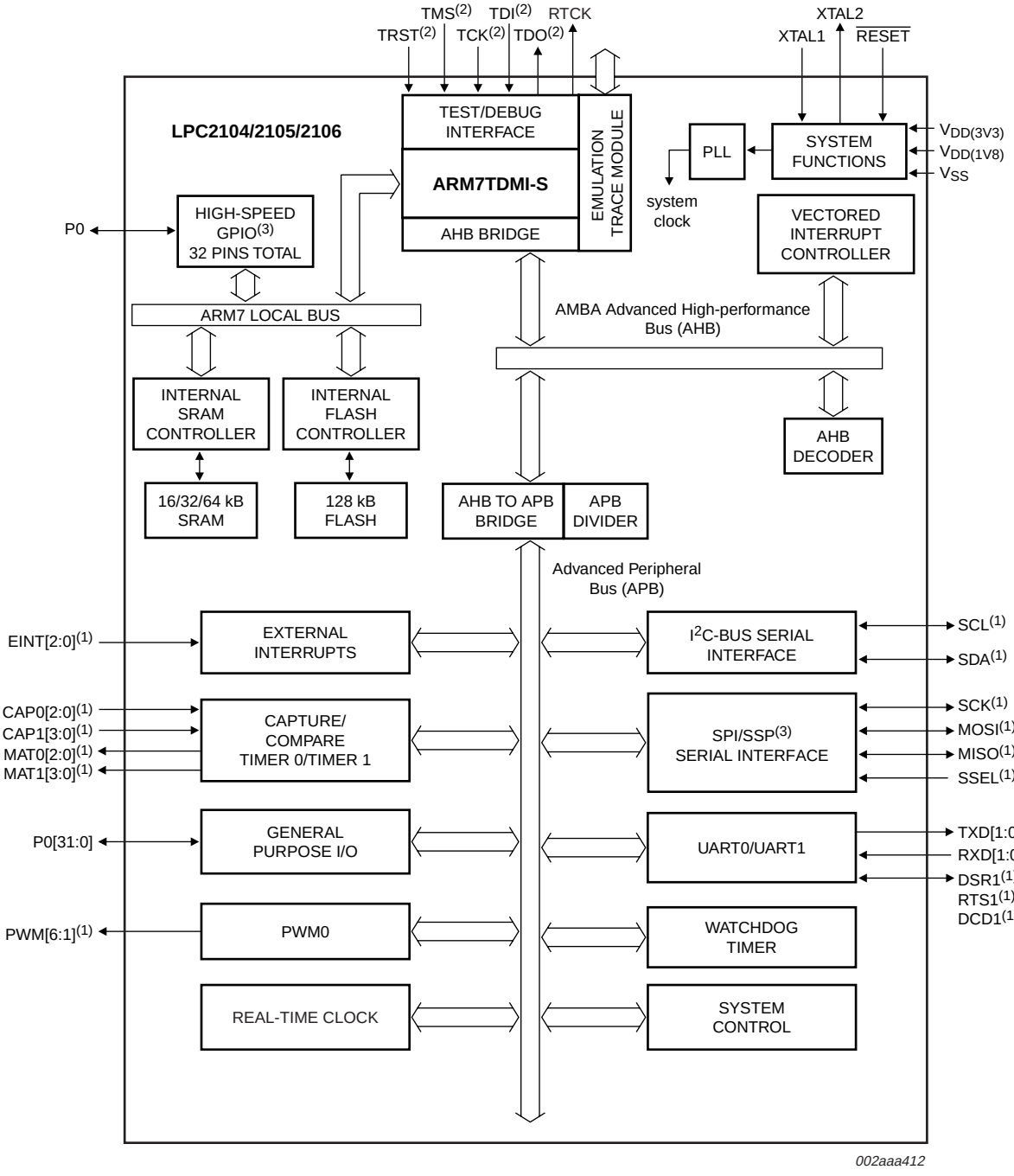
3.1 Ordering options

Table 2. Ordering options

Type number	Flash memory	RAM	Temperature range
LPC2104BBD48	128 kB	16 kB	0 °C to +70 °C
LPC2104FBD48/00	128 kB	16 kB	–40 °C to +85 °C
LPC2104FBD48/01	128 kB	16 kB	–40 °C to +85 °C
LPC2105BBD48	128 kB	32 kB	0 °C to +70 °C
LPC2105FBD48/00	128 kB	32 kB	–40 °C to +85 °C
LPC2105FBD48/01	128 kB	32 kB	–40 °C to +85 °C
LPC2106BBD48	128 kB	64 kB	0 °C to +70 °C
LPC2106FBD48	128 kB	64 kB	–40 °C to +85 °C
LPC2106FBD48/00	128 kB	64 kB	–40 °C to +85 °C
LPC2106FBD48/01	128 kB	64 kB	–40 °C to +85 °C
LPC2106FHN48	128 kB	64 kB	–40 °C to +85 °C
LPC2106FHN48/00	128 kB	64 kB	–40 °C to +85 °C
LPC2106FHN48/01	128 kB	64 kB	–40 °C to +85 °C

© NXP B.V. 2008. All rights reserved.

4. Block diagram



(1) Shared with GPIO.

(2) When test/debug interface is used, GPIO/other functions sharing these pins are not available.

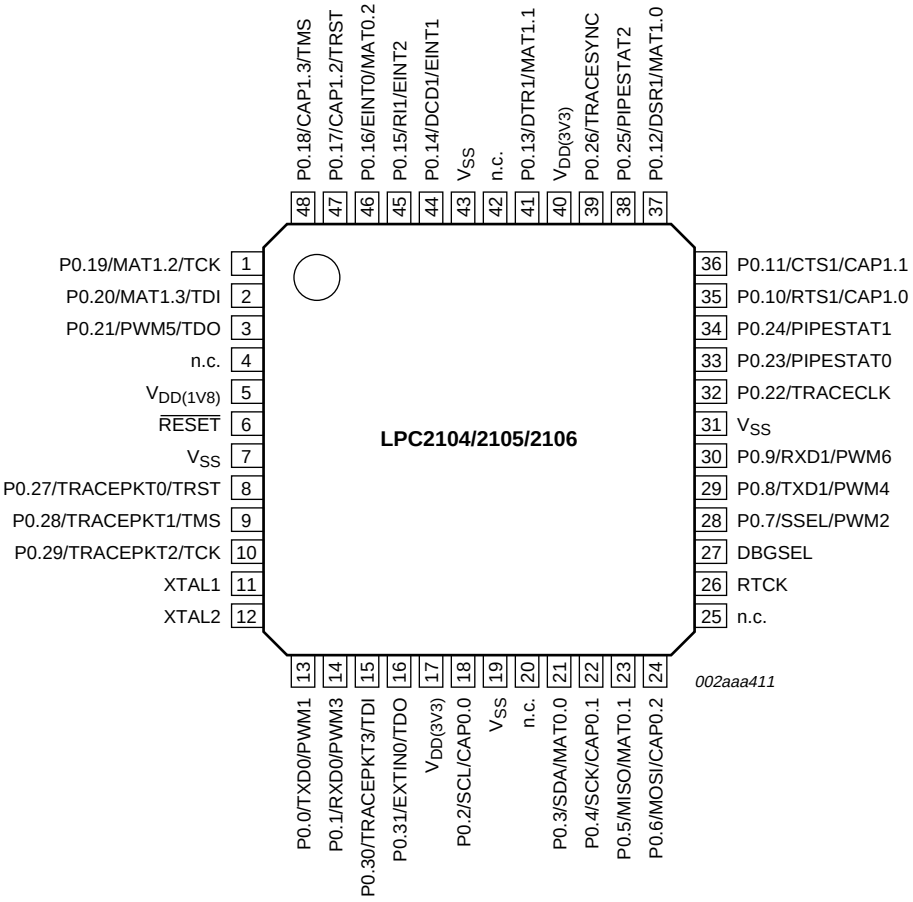
(3) Available on LPC2104/2105/2106/01 only.

Fig 1. Block diagram

© NXP B.V. 2008. All rights reserved.

5. Pinning information

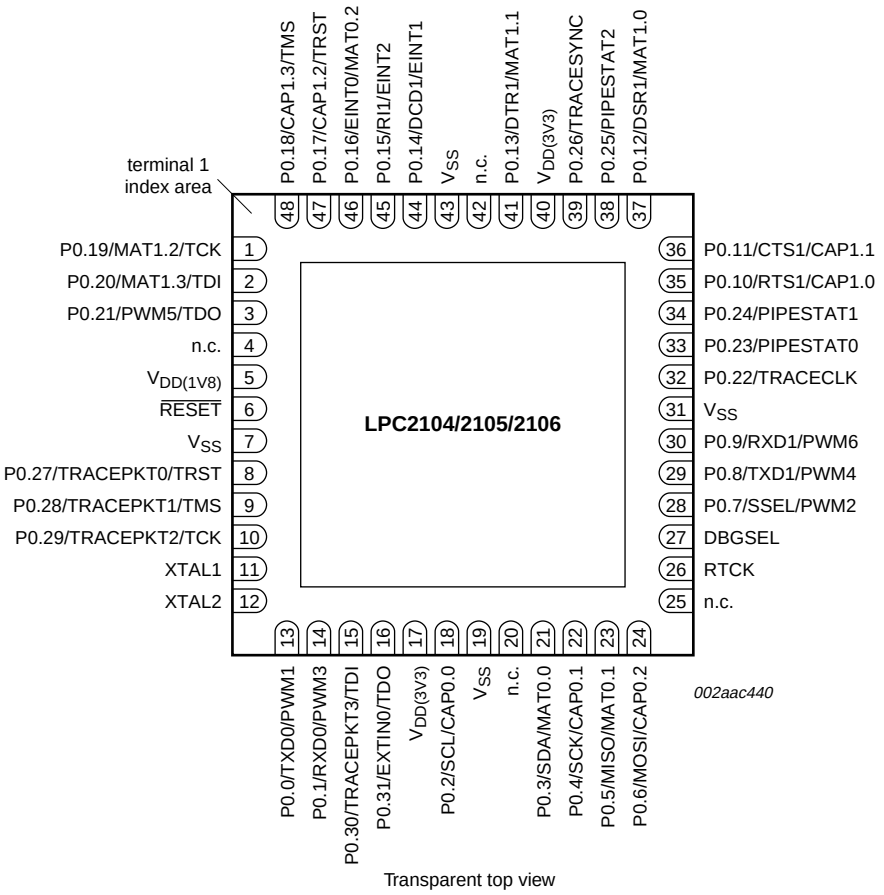
5.1 Pinning



Pin configuration is identical for all LQFP48 packages.

Fig 2. Pin configuration (LQFP48)

© NXP B.V. 2008. All rights reserved.



Pin configuration is identical for LPC2106FHN48, LPC2106FHN48/00, and LPC2106FHN48/01.

Fig 3. Pin configuration (HVQFN48)

© NXP B.V. 2008. All rights reserved.

5.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
P0.0 to P0.31		I/O	**Port 0:** Port 0 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 0 pins depends upon the pin function selected via the Pin Connect Block.
P0.0/TXD0/PWM1	13[1]	I/O	**P0.0 —** Port 0 bit 0.
		O	**TXD0 —** Transmitter output for UART 0.
		O	**PWM1 —** Pulse Width Modulator output 1.
P0.1/RXD0/PWM3	14[1]	I/O	**P0.1 —** Port 0 bit 1.
		I	**RXD0 —** Receiver input for UART 0.
		O	**PWM3 —** Pulse Width Modulator output 3.
P0.2/SCL/CAP0.0	18[2]	I/O	**P0.2 —** Port 0 bit 2. The output is open-drain.
		I/O	**SCL —** I^2C-bus clock input/output. Open-drain output (for I^2C-bus compliance).
		I	**CAP0.0 —** Capture input for Timer 0, channel 0.
P0.3/SDA/MAT0.0	21[2]	I/O	**P0.3 —** Port 0 bit 3. The output is open-drain.
		I/O	**SDA —** I^2C-bus data input/output. Open-drain output (for I^2C-bus compliance).
		O	**MAT0.0 —** Match output for Timer 0, channel 0. The output is open-drain.
P0.4/SCK/CAP0.1	22[1]	I/O	**P0.4 —** Port 0 bit 4.
		I/O	**SCK —** Serial clock for SPI/SSP[3]. Clock output from master or input to slave.
		I	**CAP0.1 —** Capture input for Timer 0, channel 1.
P0.5/MISO/MAT0.1	23[1]	I/O	**P0.5 —** Port 0 bit 5.
		I/O	**MISO —** Master In Slave Out for SPI/SSP[3]. Data input to SPI/SSP master or data output from SPI/SSP slave.
		O	**MAT0.1 —** Match output for Timer 0, channel 1.
P0.6/MOSI/CAP0.2	24[1]	I/O	**P0.6 —** Port 0 bit 6.
		I/O	**MOSI —** Master Out Slave In for SPI/SSP[3]. Data output from SPI/SSP master or data input to SPI/SSP slave.
		I	**CAP0.2 —** Capture input for Timer 0, channel 2.
P0.7/SSEL/PWM2	28[1]	I/O	**P0.7 —** Port 0 bit 7.
		I	**SSEL —** Slave Select for SPI/SSP[3]. Selects the SPI/SSP interface as a slave.
		O	**PWM2 —** Pulse Width Modulator output 2.
P0.8/TXD1/PWM4	29[1]	I/O	**P0.8 —** Port 0 bit 8.
		O	**TXD1 —** Transmitter output for UART 1.
		O	**PWM4 —** Pulse Width Modulator output 4.
P0.9/RXD1/PWM6	30[1]	I/O	**P0.9 —** Port 0 bit 9.
		I	**RXD1 —** Receiver input for UART 1.
		O	**PWM6 —** Pulse Width Modulator output 6.
P0.10/RTS1/CAP1.0	35[1]	I/O	**P0.10 —** Port 0 bit 10.
		O	**RTS1 —** Request to Send output for UART 1.
		I	**CAP1.0 —** Capture input for Timer 1, channel 0.

© NXP B.V. 2008. All rights reserved.

Table 3. Pin description *...continued*

Symbol	Pin	Type	Description
P0.11/CTS1/CAP1.1	36[1]	I/O	**P0.11 —** Port 0 bit 11.
		I	**CTS1 —** Clear to Send input for UART 1.
		I	**CAP1.1 —** Capture input for Timer 1, channel 1.
P0.12/DSR1/MAT1.0	37[1]	I/O	**P0.12 —** Port 0 bit 12.
		I	**DSR1 —** Data Set Ready input for UART 1.
		O	**MAT1.0 —** Match output for Timer 1, channel 0.
P0.13/DTR1/MAT1.1	41[1]	I/O	**P0.13 —** Port 0 bit 13.
		O	**DTR1 —** Data Terminal Ready output for UART 1.
		O	**MAT1.1 —** Match output for Timer 1, channel 1.
P0.14/DCD1/EINT1	44[1]	I/O	**P0.14 —** Port 0 bit 14.
		I	**DCD1 —** Data Carrier Detect input for UART 1.
		I	**EINT1 —** External interrupt 1 input.
P0.15/RI1/EINT2	45[1]	I/O	**P0.15 —** Port 0 bit 15.
		I	**RI1 —** Ring Indicator input for UART 1.
		O	**EINT2 —** External interrupt 2 input.
P0.16/EINT0/MAT0.2	46[1]	I/O	**P0.16 —** Port 0 bit 16.
		I	**EINT0 —** External interrupt 0 input.
		O	**MAT0.2 —** Match output for Timer 0, channel 2.
P0.17/CAP1.2/TRST	47[1]	I/O	**P0.17 —** Port 0 bit 17.
		I	**CAP1.2 —** Capture input for Timer 1, channel 2.
		I	**TRST —** Test Reset for JTAG interface, primary JTAG pin group.
P0.18/CAP1.3/TMS	48[1]	I/O	**P0.18 —** Port 0 bit 18.
		I	**CAP1.3 —** Capture input for Timer 1, channel 3.
		I	**TMS —** Test Mode Select for JTAG interface, primary JTAG pin group.
P0.19/MAT1.2/TCK	1[1]	I/O	**P0.19 —** Port 0 bit 19.
		O	**MAT1.2 —** Match output for Timer 1, channel 2.
		I	**TCK —** Test Clock for JTAG interface, primary JTAG pin group.
P0.20/MAT1.3/TDI	2[1]	I/O	**P0.20 —** Port 0 bit 20.
		O	**MAT1.3 —** Match output for Timer 1, channel 3.
		I	**TDI —** Test Data In for JTAG interface, primary JTAG pin group.
P0.21/PWM5/TDO	3[1]	I/O	**P0.21 —** Port 0 bit 21.
		O	**PWM5 —** Pulse Width Modulator output 5.
		O	**TDO —** Test Data Out for JTAG interface, primary JTAG pin group.
P0.22/TRACECLK	32[4]	I/O	**P0.22 —** Port 0 bit 22.
		O	**TRACECLK —** Trace Clock. Standard I/O port with internal pull-up.
P0.23/PIPESTAT0	33[4]	I/O	**P0.23 —** Port 0 bit 23.
		O	**PIPESTAT0 —** Pipeline Status, bit 0. Standard I/O port with internal pull-up.
P0.24/PIPESTAT1	34[4]	I/O	**P0.24 —** Port 0 bit 24.
		O	**PIPESTAT1 —** Pipeline Status, bit 1. Standard I/O port with internal pull-up.
P0.25/PIPESTAT2	38[4]	I/O	**P0.25 —** Port 0 bit 25.
		O	**PIPESTAT2 —** Pipeline Status, bit 2. Standard I/O port with internal pull-up.

© NXP B.V. 2008. All rights reserved.

Table 3. Pin description *...continued*

Symbol	Pin	Type	Description
P0.26/TRACESYNC	39[4]	I/O	**P0.26 —** Port 0 bit 26.
		O	**TRACESYNC —** Trace Synchronization Standard I/O port with internal pull-up.
P0.27/TRACEPKT0/ TRST	8[4]	I/O	**P0.27 —** Port 0 bit 27.
		O	**TRACEPKT0 —** Trace Packet, bit 0. Standard I/O port with internal pull-up.
		I	**TRST —** Test Reset for JTAG interface, secondary JTAG pin group.
P0.28/TRACEPKT1/ TMS	9[4]	I/O	**P0.28 —** Port 0 bit 28.
		O	**TRACEPKT1 —** Trace Packet, bit 1. Standard I/O port with internal pull-up.
		I	**TMS —** Test Mode Select for JTAG interface, secondary JTAG pin group.
P0.29/TRACEPKT2/ TCK	10[4]	I/O	**P0.29 —** Port 0 bit 29.
		O	**TRACEPKT2 —** Trace Packet, bit 2. Standard I/O port with internal pull-up.
		I	**TCK —** Test Clock for JTAG interface, secondary JTAG pin group. This clock must be slower than 1/6 of the CPU clock (CCLK) for the JTAG interface to operate.
P0.30/TRACEPKT3/ TDI	15[4]	I/O	**P0.30 —** Port 0 bit 30.
		O	**TRACEPKT3 —** Trace Packet, bit 3. Standard I/O port with internal pull-up.
		I	**TDI —** Test Data In for JTAG interface, secondary JTAG pin group.
P0.31/EXTIN0/TDO	16[4]	I/O	**P0.31 —** Port 0 bit 31.
		I	**EXTIN0 —** External Trigger Input. Standard I/O port with internal pull-up.
		O	**TDO —** Test Data out for JTAG interface, secondary JTAG pin group.
RTCK	26[4]	I/O	Returned Test Clock output: Extra signal added to the JTAG port. Assists debugger synchronization when processor frequency varies. Also used during debug mode entry to select primary or secondary JTAG pins with the 48-pin package. Bidirectional pin with internal pull-up.
DBGSEL	27	I	Debug Select: When LOW, the part operates normally. When HIGH, debug mode is entered. Input pin with internal pull-down.
$\overline{\text{RESET}}$	6[5]	I	external reset input; a LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. TTL with hysteresis, 5 V tolerant.
XTAL1	11	I	input to the oscillator circuit and internal clock generator circuits.
XTAL2	12	O	output from the oscillator amplifier.
V_{SS}	7, 19, 31, 43	I	ground: 0 V reference.
$V_{DD(1V8)}$	5	I	1.8 V core power supply; this is the power supply voltage for internal circuitry.
$V_{DD(3V3)}$	17, 40	I	3.3 V pad power supply; this is the power supply voltage for the I/O ports.
n.c.	4, 20, 25, 42	-	not connected; these pins are not connected in the 48-pin package.

[1] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control.

[2] Open-drain 5 V tolerant digital I/O pad, compatible with I^2C-bus 400 kHz specification. It requires external pull-up to provide an output functionality. Open-drain configuration applies to all functions on this pin.

[3] SSP interface available on LPC2104/2105/2106/01 only.

[4] 5 V tolerant pad with built-in pull-up resistor providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control. The pull-up resistor's value ranges from 60 kΩ to 300 kΩ.

[5] 5 V tolerant pad providing digital input (with TTL levels and hysteresis) function only.

© NXP B.V. 2008. All rights reserved.

6. Functional description

6.1 Architectural overview

The ARM7TDMI-S is a general purpose 32-bit microprocessor, which offers high performance and very low power consumption. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed Complex Instruction Set Computers. This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM7TDMI-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue.

The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM7TDMI-S processor has two instruction sets:

- The standard 32-bit ARM set.
- A 16-bit Thumb set.

The Thumb set's 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM's performance advantage over a traditional 16-bit processor using 16-bit registers. This is possible because Thumb code operates on the same 32-bit register set as ARM code.

Thumb code is able to provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM processor connected to a 16-bit memory system.

6.2 On-chip flash program memory

The LPC2104/2105/2106 incorporate a 128 kB flash memory system. This memory may be used for both code and data storage. Programming of the flash memory may be accomplished in several ways. It may be programmed In System via the serial port. The application program may also erase and/or program the flash while the application is running, allowing a great degree of flexibility for data storage field firmware upgrades, etc. When on-chip bootloader is used, 120 kB of flash memory is available for user code.

The LPC2104/2105/2106 flash memory provides a minimum of 100000 erase/write cycles and 20 years of data retention.

6.3 On-chip static RAM

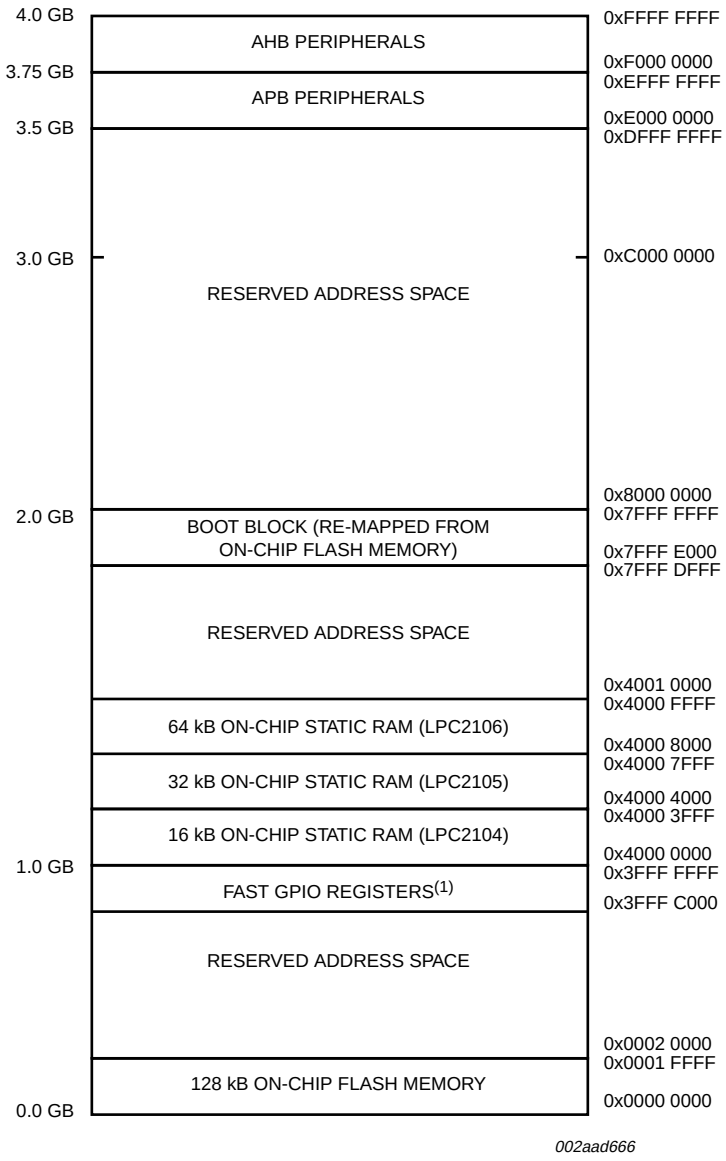
On-chip static RAM may be used for code and/or data storage. The SRAM may be accessed as 8 bit, 16 bit, and 32 bit. The LPC2104/2105/2106 provide 16/32/64 kB of static RAM, respectively.

© NXP B.V. 2008. All rights reserved.

6.4 Memory map

The LPC2104/2105/2106 memory maps incorporate several distinct regions, as shown in the following figures.

In addition, the CPU interrupt vectors may be re-mapped to allow them to reside in either flash memory (the default) or on-chip static RAM. This is described in Section 6.18 "System control".



(1) LPC2104/2105/2106/01 only.

Fig 4. LPC2104/2105/2106 memory map

© NXP B.V. 2008. All rights reserved.

6.5 Interrupt controller

The Vectored Interrupt Controller (VIC) accepts all of the Interrupt Request (IRQ) inputs and categorizes, them as FIQ, vectored IRQ, and non-vectored IRQ as defined by programmable settings. The programmable assignment scheme means that priorities of interrupts from the various peripherals can be dynamically assigned and adjusted.

Fast Interrupt reQuest (FIQ) has the highest priority. If more than one request is assigned to FIQ, the VIC combines the requests to produce the FIQ signal to the ARM processor. The fastest possible FIQ latency is achieved when only one request is classified as FIQ, because then the FIQ service routine can simply start dealing with that device. But if more than one request is assigned to the FIQ class, the FIQ service routine can read a word from the VIC that identifies which FIQ source(s) is (are) requesting an interrupt.

Vectored IRQs have the middle priority. Sixteen of the interrupt requests can be assigned to this category. Any of the interrupt requests can be assigned to any of the 16 vectored IRQ slots, among which slot 0 has the highest priority and slot 15 has the lowest.

Non-vectored IRQs have the lowest priority.

The VIC combines the requests from all the vectored and non-vectored IRQs to produce the IRQ signal to the ARM processor. The IRQ service routine can start by reading a register from the VIC and jumping there. If any of the vectored IRQs are requesting, the VIC provides the address of the highest-priority requesting IRQs service routine, otherwise it provides the address of a default routine that is shared by all the non-vectored IRQs. The default routine can read another VIC register to see what IRQs are active.

6.5.1 Interrupt sources

Table 4 lists the interrupt sources for each peripheral function. Each peripheral device has one interrupt line connected to the Vectored Interrupt Controller, but may have several internal interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Table 4. Interrupt sources

Block	Flag(s)	VIC channel #
WDT	Watchdog Interrupt (WDINT)	0
-	Reserved for software interrupts only	1
ARM Core	EmbeddedICE, DbgCommRx	2
ARM Core	EmbeddedICE, DbgCommTx	3
Timer 0	Match 0 to 3 (MR0, MR1, MR2, MR3) Capture 0 to 2 (CR0, CR1, CR2)	4
Timer 1	Match 0 to 3 (MR0, MR1, MR2, MR3) Capture 0 to 3 (CR0, CR1, CR2, CR3)	5
UART 0	Rx Line Status (RLS) Transmit Holding Register empty (THRE) Rx Data Available (RDA) Character Time-out Indicator (CTI) Auto-Baud Time-Out (ABTO)[1] End of Auto-Baud (ABEO)[1]	6

© NXP B.V. 2008. All rights reserved.

Table 4. Interrupt sources *...continued*

Block	Flag(s)	VIC channel #
UART 1	Rx Line Status (RLS)	7
	Transmit Holding Register empty (THRE)	
	Rx Data Available (RDA)	
	Character Time-out Indicator (CTI)	
	Modem Status Interrupt (MSI)	
	Auto-Baud Time-Out (ABTO)[1]	
	End of Auto-Baud (ABEO)[1]	
PWM0	Match 0 to 6 (MR0, MR1, MR2, MR3, MR4, MR5, MR6)	8
I^2C-bus	SI (state change)	9
SPI and SSP[1]	SPIF, MODF (SPI)	10
	TXRIS, RXRIS, RTRIS, RORRIS (SSP)[1]	
-	reserved	11
PLL	PLL Lock (PLOCK)	12
RTC	RTCCIF (Counter Increment), RTCALF (Alarm)	13
System Control	External Interrupt 0 (EINT0)	14
System Control	External Interrupt 1 (EINT1)	15
System Control	External Interrupt 2 (EINT2)	16

[1] Available on LPC2104/2105/2106/01 only.

6.6 Pin connect block

The pin connect block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on chip peripherals. Peripherals should be connected to the appropriate pins prior to being activated, and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

The Pin Control Module contains two registers as shown in Table 5.

Table 5. Pin control module registers

Address	Name	Description	Access
0xE002 C000	PINSEL0	Pin function select register 0	Read/Write
0xE002 C004	PINSEL1	Pin function select register 1	Read/Write

6.7 Pin function select register 0 (PINSEL0 - 0xE002 C000)

The PINSEL0 register controls the functions of the pins as per the settings listed in Table 6. The direction control bit in the IODIR register is effective only when the GPIO function is selected for a pin. For other functions, direction is controlled automatically. Settings other than those shown in Table 6 are reserved, and should not be used

© NXP B.V. 2008. All rights reserved.

Table 6. Pin function select register 0 (PINSEL0 - 0xE002 C000)

PINSEL0	Pin name	Value		Function	Value after reset
1:0	P0.0	0	0	GPIO Port 0.0	0
		0	1	TXD (UART 0)	
		1	0	PWM1	
3:2	P0.1	0	0	GPIO Port 0.1	0
		0	1	RXD (UART 0)	
		1	0	PWM3	
5:4	P0.2	0	0	GPIO Port 0.2	0
		0	1	SCL (I^2C-bus)	
		1	0	Capture 0.0 (Timer 0)	
7:6	P0.3	0	0	GPIO Port 0.3	0
		0	1	SDA (I^2C-bus)	
		1	0	Match 0.0 (Timer 0)	
9:8	P0.4	0	0	GPIO Port 0.4	0
		0	1	SCK (SPI/SSP)	
		1	0	Capture 0.1 (Timer 0)	
11:10	P0.5	0	0	GPIO Port 0.5	0
		0	1	MISO (SPI/SSP)	
		1	0	Match 0.1 (Timer 0)	
13:12	P0.6	0	0	GPIO Port 0.6	0
		0	1	MOSI (SPI/SSP)	
		1	0	Capture 0.2 (Timer 0)	
15:14	P0.7	0	0	GPIO Port 0.7	0
		0	1	SSEL (SPI/SSP)	
		1	0	PWM2	
17:16	P0.8	0	0	GPIO Port 0.8	0
		0	1	TXD (UART 1)	
		1	0	PWM4	
19:18	P0.9	0	0	GPIO Port 0.9	0
		0	1	RXD (UART 1)	
		1	0	PWM6	
21:20	P0.10	0	0	GPIO Port 0.10	0
		0	1	RTS (UART 1)	
		1	0	Capture 1.0 (Timer 1)	
23:22	P0.11	0	0	GPIO Port 0.11	0
		0	1	CTS (UART 1)	
		1	0	Capture 1.1 (Timer 1)	
25:24	P0.12	0	0	GPIO Port 0.12	0
		0	1	DSR (UART 1)	
		1	0	Match 1.0 (Timer 1)	

© NXP B.V. 2008. All rights reserved.

Table 6. Pin function select register 0 (PINSEL0 - 0xE002 C000) *...continued*

PINSEL0	Pin name	Value		Function	Value after reset
27:26	P0.13	0	0	GPIO Port 0.13	0
		0	1	DTR (UART 1)	
		1	0	Match 1.1 (Timer 1)	
29:28	P0.14	0	0	GPIO Port 0.14	0
		0	1	DCD (UART 1)	
		1	0	EINT1	
31:30	P0.15	0	0	GPIO Port 0.15	0
		0	1	RI (UART 1)	
		1	0	EINT2	

6.8 Pin function select register 1 (PINSEL1 - 0xE002 C004)

The PINSEL1 register controls the functions of the pins as per the settings listed in Table 7. The direction control bit in the IODIR register is effective only when the GPIO function is selected for a pin. For other functions direction is controlled automatically.

Remark: The primary JTAG port and the trace port can be selected only through the DBGSEL pin at reset (Debug mode). Function control for the pins P0[31:17] is effective only when the DBGSEL input is pulled LOW during reset.

Table 7. Pin function select register 1 (PINSEL1 - 0xE002 C004)

PINSEL1	Pin name	Value		Function	Value after reset
1:0	P0.16	0	0	GPIO Port 0.16	0
		0	1	EINT0	
		1	0	Match 0.2 (Timer 0)	
3:2	P0.17	0	0	GPIO Port 0.17	0
		0	1	Capture 1.2 (Timer 1)	
5:4	P0.18	0	0	GPIO Port 0.18	0
		0	1	Capture 1.3 (Timer 1)	
7:6	P0.19	0	0	GPIO Port 0.19	0
		0	1	Match 1.2 (Timer 1)	
9:8	P0.20	0	0	GPIO Port 0.20	0
		0	1	Match 1.3 (Timer 1)	
11:10	P0.21	0	0	GPIO Port 0.21	0
		0	1	PWM5	
13:12	P0.22	0	0	GPIO Port 0.22	0
15:14	P0.23	0	0	GPIO Port 0.23	0
17:16	P0.24	0	0	GPIO Port 0.24	0
19:18	P0.25	0	0	GPIO Port 0.25	0
21:20	P0.26	0	0	GPIO Port 0.26	0
23:22	P0.27	0	0	GPIO Port 0.27	0
		0	1	TRST	

© NXP B.V. 2008. All rights reserved.

Table 7. Pin function select register 1 (PINSEL1 - 0xE002 C004) *...continued*

PINSEL1	Pin name	Value		Function	Value after reset
25:24	P0.28	0	0	GPIO Port 0.28	0
		0	1	TMS	
27:26	P0.29	0	0	GPIO Port 0.29	0
		0	1	TCK	
29:28	P0.30	0	0	GPIO Port 0.30	0
		0	1	TDI	
31:30	P0.31	0	0	GPIO Port 0.31	0
		0	1	TDO	

6.9 General purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back, as well as the current state of the port pins.

6.9.1 Features

- Direction control of individual bits.
- Separate control of output set and clear.
- All I/O default to inputs after reset.

6.9.2 Features added with the Fast GPIO set of registers available on LPC2104/2105/2106/01 only

- Fast GPIO registers are relocated to the ARM local bus for the fastest possible I/O timing, enabling port pin toggling up to 3.5 times faster than earlier LPC2000 devices.
- Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
- All Fast GPIO registers are byte addressable.
- Entire port value can be written in one instruction.
- Ports are accessible via either the legacy group of registers (GPIOs) or the group of registers providing accelerated port access (Fast GPIOs).

6.10 UARTs

The LPC2104/2105/2106 each contain two UARTs. One UART provides a full modem control handshake interface, the other provides only transmit and receive data lines.

6.10.1 Features

- 16 byte Receive and Transmit FIFOs
- Register locations conform to 16C550 industry standard
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B
- Built-in baud rate generator

© NXP B.V. 2008. All rights reserved.

- Standard modem interface signals included on UART 1.

6.10.2 UART features available in LPC2104/2105/2106/01 only

Compared to previous LPC2000 microcontrollers, UARTs in LPC2104/2105/2106/01 introduce a fractional baud rate generator for both UARTs, enabling these microcontrollers to achieve standard baud rates such as 115200 Bd with any crystal frequency above 2 MHz. In addition, auto-CTS/RTS flow-control functions are fully implemented in hardware.

- Fractional baud rate generator enables standard baud rates such as 115200 Bd to be achieved with any crystal frequency above 2 MHz.
- Autobauding.
- Auto-CTS/RTS flow-control fully implemented in hardware.

6.11 I^2C-bus serial I/O controller

I^2C is a bidirectional bus for inter-IC control using only two wires: a serial clock line (SCL), and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g. an LCD driver or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. I^2C is a multi-master bus, it can be controlled by more than one bus master connected to it.

The I^2C-bus implemented in LPC2104/2105/2106 supports bit rate up to 400 kbit/s (Fast I^2C-bus).

6.11.1 Features

- Standard I^2C compliant bus interface.
- Easy to configure as Master, Slave or Master/Slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus may be used for test and diagnostic purposes.

© NXP B.V. 2008. All rights reserved.

6.12 SPI serial I/O controller

The SPI is a full duplex serial interface, designed to be able to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends a byte of data to the slave, and the slave always sends a byte of data to the master.

6.12.1 Features

- Compliant with Serial Peripheral Interface (SPI) specification.
- Synchronous, serial, full duplex communication.
- Combined SPI master and slave.
- Maximum data bit rate of one eighth of the input clock rate.

6.12.2 Features available in LPC2104/2105/2106/01 only

- Selectable transfer width of eight to 16 bit per frame.
- When the SPI interface is used in Master mode, the SSEL pin is not needed (can be used for a different function).

6.13 SSP controller (LPC2104/2015/2106/01 only)

The SSP is a controller capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. Data transfers are in principle full duplex, with frames of four to 16 bits of data flowing from the master to the slave and from the slave to the master.

Because the SSP and SPI peripherals share the same physical pins, it is not possible to have both of these two peripherals active at the same time. Application can switch on the fly from SPI to SSP and back.

6.13.1 Features

- Compatible with Motorola’s SPI, Texas Instrument’s 4-wire SSI, and National Semiconductor’s Microwire buses.
- Synchronous serial communication.
- Master or slave operation.
- 8-frame FIFOs for both transmit and receive.
- Four to 16 bits per frame.

6.14 General purpose timers

The Timer is designed to count cycles of the peripheral clock (PCLK) and optionally generate interrupts or perform other actions at specified timer values, based on four match registers. It also includes up to four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

© NXP B.V. 2008. All rights reserved.

6.14.1 Features

- A 32-bit Timer/Counter with a programmable 32-bit Prescaler.
- Up to four (Timer 1) and three (Timer 0) 32-bit capture channels, that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four (Timer 1) and three (Timer 0) external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

6.14.2 Features available in LPC2104/2105/2106/01 only

The LPC2104/2105/2106/01 can count external events on one of the capture inputs if the external pulse lasts at least one half of the period of the PCLK. In this configuration, unused capture lines can be selected as regular timer capture inputs or used as external interrupts.

- Timer can count cycles of either the peripheral clock (PCLK) or an externally supplied clock.
- When counting cycles of an externally supplied clock, only one of the timer's capture inputs can be selected as the timer's clock. The rate of such a clock is limited to $^{PCLK}/_{4}$. Duration of HIGH/LOW levels on the selected CAP input cannot be shorter than $^{1}/_{(2PCLK)}$.

6.15 Watchdog timer

The purpose of the Watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the Watchdog will generate a system reset if the user program fails to 'feed' (or reload) the Watchdog within a predetermined amount of time.

6.15.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect/Incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.

© NXP B.V. 2008. All rights reserved.

- Programmable 32-bit timer with internal pre-scaler.
- Selectable time period from ($T_{cy(PCLK)} \times 256 \times 4$) to ($T_{cy(PCLK)} \times 2^{32} \times 4$) in multiples of $T_{cy(PCLK)} \times 4$.

6.16 Real time clock

The Real Time Clock (RTC) is designed to provide a set of counters to measure time when normal or idle operating mode is selected. The RTC has been designed to use little power, making it suitable for battery powered systems where the CPU is not running continuously (Idle mode).

6.16.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra Low Power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Programmable Reference Clock Divider allows adjustment of the RTC to match various crystal frequencies.

6.17 Pulse width modulator

The PWM is based on the standard Timer block and inherits all of its features, although only the PWM function is pinned out on the LPC2104/2105/2106. The Timer is designed to count cycles of the peripheral clock (PCLK) and optionally generate interrupts or perform other actions when specified timer values occur, based on seven match registers. It also includes four capture inputs to save the timer value when an input signal transitions, and optionally generate an interrupt when those events occur. The PWM function is in addition to these features, and is based on match register events.

The ability to separately control rising and falling edge locations allows the PWM to be used for more applications. For instance, multi-phase motor control typically requires three non-overlapping PWM outputs with individual control of all three pulse widths and positions.

Two match registers can be used to provide a single edge controlled PWM output. One match register (MR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an MR0 match occurs.

Three match registers can be used to provide a PWM output with both edges controlled. Again, the MR0 match register controls the PWM cycle rate. The other match registers control the two PWM edge positions. Additional double edge controlled PWM outputs require only two match registers each, since the repetition rate is the same for all PWM outputs.

© NXP B.V. 2008. All rights reserved.

With double edge controlled PWM outputs, specific match registers control the rising and falling edge of the output. This allows both positive going PWM pulses (when the rising edge occurs prior to the falling edge), and negative going PWM pulses (when the falling edge occurs prior to the rising edge).

6.17.1 Features

- Seven match registers allow up to six single edge controlled or three double edge controlled PWM outputs, or a mix of both types.
- The match registers also allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Supports single edge controlled and/or double edge controlled PWM outputs. Single edge controlled PWM outputs all go HIGH at the beginning of each cycle unless the output is a constant LOW. Double edge controlled PWM outputs can have either edge occur at any position within a cycle. This allows for both positive going and negative going pulses.
- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.
- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must “release” new match values before they can become effective.
- May be used as a standard timer if the PWM mode is not enabled.
- A 32-bit Timer/Counter with a programmable 32-bit Prescaler.

6.18 System control

6.18.1 Crystal oscillator

The oscillator supports crystals in the range of 1 MHz to 25 MHz. The oscillator output frequency is called FOSC and the ARM processor clock frequency is referred to as CCLK for purposes of rate equations, etc. FOSC and CCLK are the same value unless the PLL is running and connected. Refer to Section 6.18.2 “PLL” for additional information.

6.18.2 PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up into the range of 10 MHz to 60 MHz with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32 (in practice, the multiplier value cannot be higher than 6 on this family of microcontrollers due to the upper frequency limit of the CPU). The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide

© NXP B.V. 2008. All rights reserved.

by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle.The PLL is turned off and bypassed following a chip Reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to Lock, then connect to the PLL as a clock source. The PLL settling time is 100 μs.

6.18.3 Reset and wake-up timer

Reset has two sources on the LPC2104/2105/2106: the $\overline{\text{RESET}}$ pin and Watchdog Reset. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin with an additional glitch filter. Assertion of chip Reset by any source starts the wake-up timer (see wake-up timer description below), causing the internal chip reset to remain asserted until the external Reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the on-chip flash controller has completed its initialization.

When the internal Reset is removed, the processor begins executing at address 0, which is the Reset vector. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

The wake-up timer ensures that the oscillator and other analog functions required for chip operation are fully functional before the processor is allowed to execute instructions. This is important at power on, all types of Reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the wake-up timer.

The wake-up timer monitors the crystal oscillator as the means of checking whether it is safe to begin code execution. When power is applied to the chip, or some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of V_{DD} ramp (in the case of power on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g. capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

6.18.4 Code security (Code Read Protection - CRP)

This feature of the LPC2104/2105/2106/01 allows the user to enable different levels of security in the system so that access to the on-chip flash and use of the JTAG and ISP can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

There are three levels of the Code Read Protection:

1. CRP1 disables access to the chip via the JTAG and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors can not be erased.
2. CRP2 disables access to the chip via the JTAG and only allows full flash erase and update using a reduced set of the ISP commands.

© NXP B.V. 2008. All rights reserved.

3. Running an application with level CRP3 selected fully disables any access to chip via the JTAG pins and the ISP. This mode effectively disables ISP override using P0[14] pin, too. It is up to the user's application to provide (if needed) a flash update mechanism using IAP calls or a call to reinvoke ISP command to enable flash update via UART 0.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

6.18.5 External interrupt inputs

The LPC2104/2105/2106 include three external interrupt inputs as selectable pin functions. The external interrupt inputs can optionally be used to wake up the processor from Power-down mode.

6.18.6 Memory mapping control

The Memory mapping control alters the mapping of the interrupt vectors that appear beginning at address 0x0000 0000. Vectors may be mapped to the bottom of the on-chip flash memory, or to the on-chip static RAM. This allows code running in different memory spaces to have control of the interrupts.

6.18.7 Power control

The LPC2104/2105/2106 support two reduced power modes: Idle mode and Power-down mode. In Idle mode, execution of instructions is suspended until either a Reset or interrupt occurs. Peripheral functions continue operation during Idle mode and may generate interrupts to cause the processor to resume execution. Idle mode eliminates power used by the processor itself, memory systems and related controllers, and internal buses.

In Power-down mode, the oscillator is shut down and the chip receives no internal clocks. The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Power-down mode and the logic levels of chip output pins remain static. The Power-down mode can be terminated and normal operation resumed by either a Reset or certain specific interrupts that are able to function without clocks. Since all dynamic operation of the chip is suspended, Power-down mode reduces chip power consumption to nearly zero.

The power can be controlled for each peripheral individually allowing peripherals to be turned off if they are not needed in the application and resulting in additional power savings.

6.18.8 APB

The APB divider determines the relationship between the processor clock (CCLK) and the clock used by peripheral devices (PCLK). The APB divider serves two purposes. The first is to provide peripherals with the desired PCLK via APB so that they can operate at the speed chosen for the ARM processor. In order to achieve this, the APB may be slowed down to $\frac{1}{2}$ to $\frac{1}{4}$ of the processor clock rate. Because the APB must work properly at power-up (and its timing cannot be altered if it does not work since the APB divider control registers reside on the APB), the default condition at reset is for the APB to run at $\frac{1}{4}$ of the

© NXP B.V. 2008. All rights reserved.

processor clock rate. The second purpose of the APB divider is to allow power savings when an application does not require any peripherals to run at the full processor rate. Because the APB divider is connected to the PLL output, the PLL remains active (if it was running) during Idle mode.

6.19 Emulation and debugging

The LPC2104/2105/2106 support emulation and debugging via a JTAG serial port. A trace port allows tracing program execution. Each of these functions requires a trade-off of debugging features versus device pins. Because the LPC2104/2105/2106 are provided in a small package, there is no room for permanently assigned JTAG or Trace pins. An alternate JTAG port allows an option to debug functions assigned to the pins used by the primary JTAG port (see Section 6.8).

6.19.1 EmbeddedICE

Standard ARM EmbeddedICE logic provides on-chip debug support. The debugging of the target system requires a host computer running the debugger software and an EmbeddedICE protocol convertor. EmbeddedICE protocol convertor converts the Remote Debug Protocol commands to the JTAG data needed to access the ARM core.

The ARM core has a Debug Communication Channel function built-in. The debug communication channel allows a program running on the target to communicate with the host debugger or another separate host without stopping the program flow or even entering the debug state. The debug communication channel is accessed as a co-processor 14 by the program running on the ARM7TDMI-S core. The debug communication channel allows the JTAG port to be used for sending and receiving data without affecting the normal program flow. The debug communication channel data and control registers are mapped in to addresses in the EmbeddedICE logic.

The JTAG clock (TCK) must be slower than $\frac{1}{6}$ of the CPU clock (CCLK) for the JTAG interface to operate.

6.19.2 Embedded trace

Since the LPC2104/2105/2106 have significant amounts of on-chip memory, it is not possible to determine how the processor core is operating simply by observing the external pins. The Embedded Trace Macrocell (ETM) provides real-time trace capability for deeply embedded processor cores. It outputs information about processor execution to the trace port.

The ETM is connected directly to the ARM core and not to the main AMBA system bus. It compresses the trace information and exports it through a narrow trace port. An external trace port analyzer must capture the trace information under software debugger control. Instruction trace (or PC trace) shows the flow of execution of the processor and provides a list of all the instructions that were executed. Instruction trace is significantly compressed by only broadcasting branch addresses as well as a set of status signals that indicate the pipeline status on a cycle by cycle basis. Trace information generation can be controlled by selecting the trigger resource. Trigger resources include address comparators, counters and sequencers. Since trace information is compressed the software debugger requires a static image of the code being executed. Self-modifying code cannot be traced because of this restriction.

© NXP B.V. 2008. All rights reserved.

6.19.3 RealMonitor

RealMonitor is a configurable software module, developed by ARM Inc., which enables real time debug. It is a lightweight debug monitor that runs in the background while users debug their foreground application. It communicates with the host using the DCC (Debug Communications Channel), which is present in the EmbeddedICE logic. The LPC2104/2105/2106 contain a specific configuration of RealMonitor software programmed into the on-chip flash memory.

© NXP B.V. 2008. All rights reserved.

7. Limiting values

Table 8. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(1V8)}$	supply voltage (1.8 V)		[2]	–0.5	+2.5	V
$V_{DD(3V3)}$	supply voltage (3.3 V)		[3]	–0.5	+3.6	V
V_I	input voltage	5 V tolerant I/O pins	[4][5]	–0.5	+6.0	V
		other I/O pins	[4][6]	–0.5	$V_{DD(3V3)}$ + 0.5	V
I_{DD}	supply current		[7][8]	-	100	mA
I_{SS}	ground current		[8][9]	-	100	mA
T_{stg}	storage temperature		[10]	–65	+150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{esd}	electrostatic discharge voltage	human body model	[11]			
		all pins		–2000	+2000	V
		machine model	[12]			
		all pins		–200	+200	V

[1] The following applies to Table 8:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Internal rail.

[3] External rail.

[4] Including voltage on outputs in 3-state mode.

[5] Only valid when the $V_{DD(3V3)}$ supply voltage is present.

[6] Not to exceed 4.6 V.

[7] Per supply pin.

[8] The peak current is limited to 25 times the corresponding maximum current.

[9] Per ground pin.

[10] Dependent on package type.

[11] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[12] Machine model: equivalent to discharging a 200 pF capacitor through a 0.75 µH coil and a 10 Ω series resistor.

© NXP B.V. 2008. All rights reserved.

8. Static characteristics

Table 9. Static characteristics

T_{amb} = 0 °C to +70 °C for commercial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$V_{DD(1V8)}$	supply voltage (1.8 V)		[2]	1.65	1.8	1.95	V
$V_{DD(3V3)}$	supply voltage (3.3 V)		[3]	3.0	3.3	3.6	V
Standard port pins, $\overline{\text{RESET}}$, RTCK, and DBGSEL							
I_{IL}	LOW-state input current	V_I = 0 V; no pull-up		-	-	3	µA
I_{IH}	HIGH-state input current	$V_I = V_{DD(3V3)}$; no pull-down		-	-	3	µA
I_{OZ}	OFF-state output current	V_O = 0 V, $V_O = V_{DD(3V3)}$; no pull-up/down		-	-	3	µA
I_{latch}	I/O latch-up current	$-(0.5V_{DD(3V3)}) < V_I < (1.5V_{DD(3V3)})$; T_j < 125 °C		100	-	-	mA
V_I	input voltage		[4][5] [6]	0	-	5.5	V
V_O	output voltage	output active		0	-	$V_{DD(3V3)}$	V
V_{IH}	HIGH-state input voltage			2.0	-	-	V
V_{IL}	LOW-state input voltage			-	-	0.8	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-state output voltage	I_{OH} = –4 mA	[7]	$V_{DD(3V3)} - 0.4$	-	-	V
V_{OL}	LOW-state output voltage	I_{OL} = 4 mA	[7]	-	-	0.4	V
I_{OH}	HIGH-state output current	$V_{OH} = V_{DD(3V3)} - 0.4$ V	[7]	–4	-	-	mA
I_{OL}	LOW-state output current	V_{OL} = 0.4 V	[7]	4	-	-	mA
I_{OHS}	HIGH-state short-circuit output current	V_{OH} = 0 V	[8]	-	-	–45	mA
I_{OLS}	LOW-state short-circuit output current	$V_{OL} = V_{DD(3V3)}$	[8]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V; applies to DBGSEL	[9]	20	50	100	µA
LPC2104/2105/2106 and LPC2104/2105/2106/00							
I_{pu}	pull-up current	V_I = 0 V	[10]	–25	–50	–65	µA
		$V_{DD(3V3)} < V_I < 5$ V	[9][10]	0	0	0	µA
LPC2104/2105/2106/01							
I_{pu}	pull-up current	V_I = 0 V	[10]	–15	–50	–85	µA
		$V_{DD(3V3)} < V_I < 5$ V	[9][10]	0	0	0	µA

© NXP B.V. 2008. All rights reserved.

Table 9. Static characteristics *…continued*

T_{amb} = 0 °C to +70 °C for commercial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
LPC2104/2105/2106 and LPC2104/2105/2106/00 power consumption							
$I_{DD(act)}$	active mode supply current	$V_{DD(1V8)}$ = 1.8 V; CCLK = 60 MHz; T_{amb} = 25 °C; code `while(1){}` executed from flash; all peripherals enabled via PCONP register but not configured to run		-	35	-	mA
$I_{DD(pd)}$	Power-down mode supply current	$V_{DD(1V8)}$ = 1.8 V; T_{amb} = 25 °C,		-	10	-	µA
		$V_{DD(1V8)}$ = 1.8 V; T_{amb} = 85 °C		-	50	500	µA
LPC2104/2105/2106/01 power consumption							
$I_{DD(act)}$	active mode supply current	$V_{DD(1V8)}$ = 1.8 V; CCLK = 60 MHz; T_{amb} = 25 °C; code `while(1){}` executed from flash; all peripherals enabled via PCONP register but not configured to run[11]		-	40	-	mA
$I_{DD(idle)}$	Idle mode supply current	$V_{DD(1V8)}$ = 1.8 V; CCLK = 60 MHz; T_{amb} = 25 °C; executed from flash; all peripherals enabled via PCONP register but not configured to run[11]		-	7	-	mA
$I_{DD(pd)}$	Power-down mode supply current	$V_{DD(1V8)}$ = 1.8 V; T_{amb} = 25 °C,		-	10	-	µA
		$V_{DD(1V8)}$ = 1.8 V; T_{amb} = 85 °C		-	-	300	µA
I^2C-bus pins							
V_{IH}	HIGH-state input voltage			$0.7V_{DD(3V3)}$	-	-	V
V_{IL}	LOW-state input voltage			-	-	$0.3V_{DD(3V3)}$	V
V_{hys}	hysteresis voltage			-	$0.5V_{DD(3V3)}$	-	V
V_{OL}	LOW-state output voltage	I_{OLS} = 3 mA	[7]	-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{DD(3V3)}$	[12]	-	2	4	µA
		V_I = 5 V		-	10	22	µA

© NXP B.V. 2008. All rights reserved.

Table 9. Static characteristics *…continued*

T_{amb} = 0 °C to +70 °C for commercial applications, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
Oscillator pins						
$V_{i(XTAL1)}$	input voltage on pin XTAL1		0	-	1.8	V
$V_{o(XTAL2)}$	output voltage on pin XTAL2		0	-	1.8	V

[1] Typical ratings are not guaranteed. The values listed are at room temperature (+25 °C), nominal supply voltages.

[2] Internal rail.

[3] External rail.

[4] Including voltage on outputs in 3-state mode.

[5] $V_{DD(3V3)}$ supply voltages must be present.

[6] 3-state outputs go into 3-state mode when $V_{DD(3V3)}$ is grounded.

[7] Accounts for 100 mV voltage drop in all supply lines.

[8] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[9] Minimum condition for V_I = 4.5 V, maximum condition for V_I = 5.5 V.

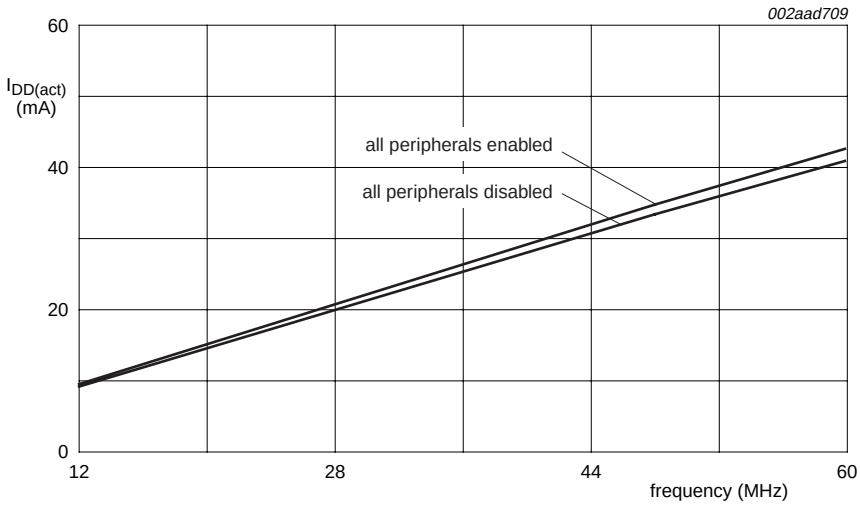
[10] Applies to P0[31:22].

[11] SPI is enabled and SSP is disabled in the PCONP register (*see LPC2104/2105/2106 user manual*).

[12] To V_{SS}.

8.1 Power consumption measurements for LPC2104/2105/2106/01

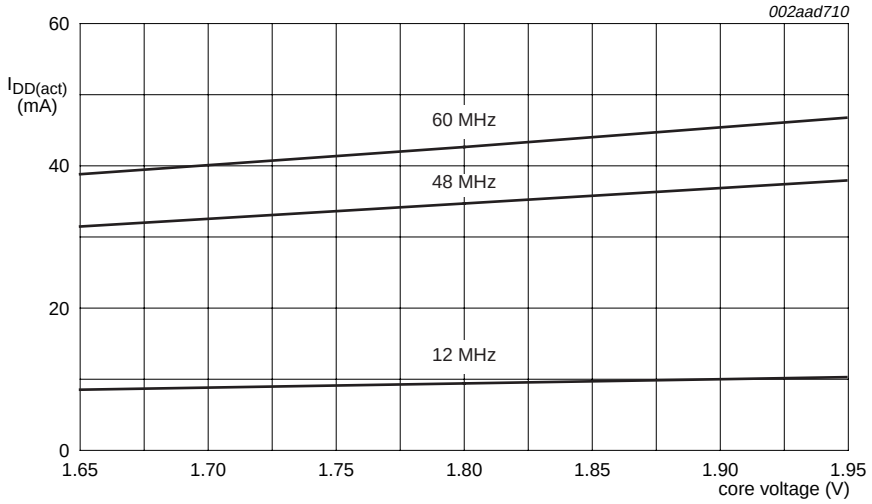
The power consumption measurements represent typical values for the given conditions. The peripherals were enabled through the PCONP register, but for these measurements the peripherals were not configured to run. Power measurements with all peripherals enabled were performed with the SPI enabled and the SSP disabled. Peripherals were disabled through the PCONP register. Refer to the *LPC2104/2105/2106 User Manual* for a description of the PCONP register.



Test conditions: Active mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$; T_{amb} = 25 °C; core voltage 1.8 V.

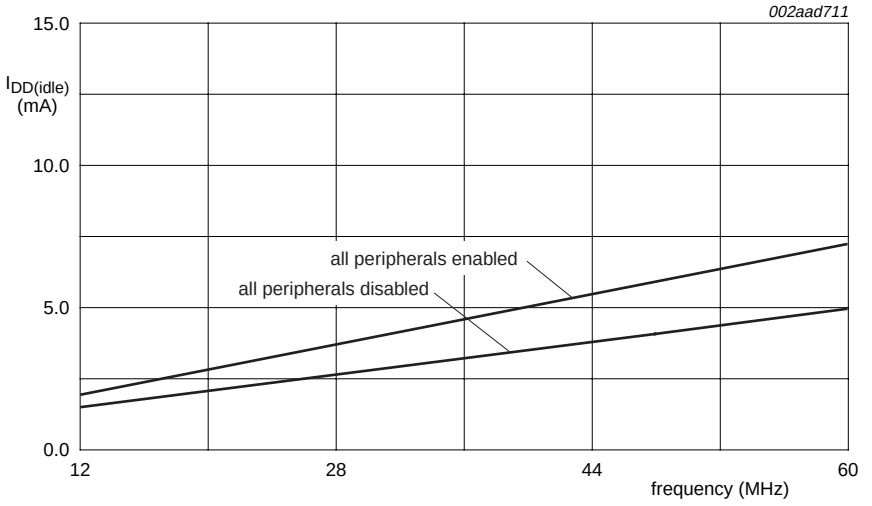
Fig 5. Typical LPC2104/2105/2106/01 $I_{DD(act)}$ measured at different frequencies

© NXP B.V. 2008. All rights reserved.



Test conditions: Active mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$; T_{amb} = 25 °C; all peripherals enabled.

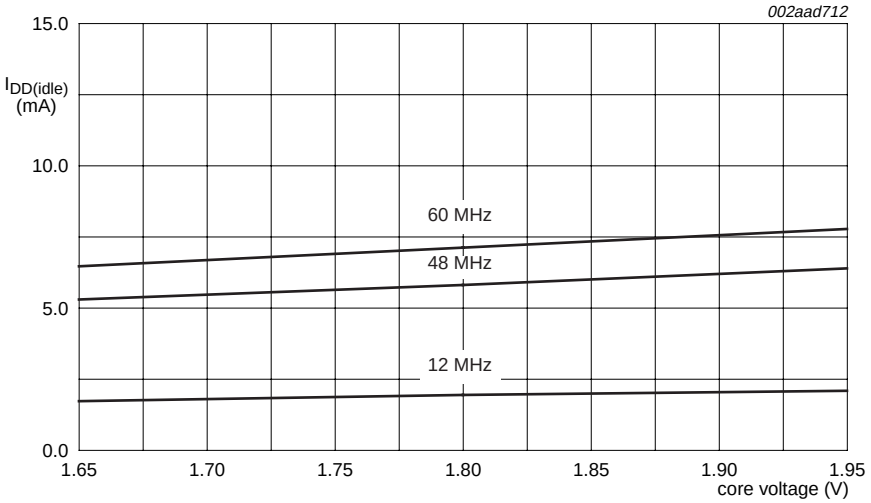
Fig 6. Typical LPC2104/2105/2106/01 $I_{DD(act)}$ measured at different core voltages



Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$; T_{amb} = 25 °C; core voltage 1.8 V.

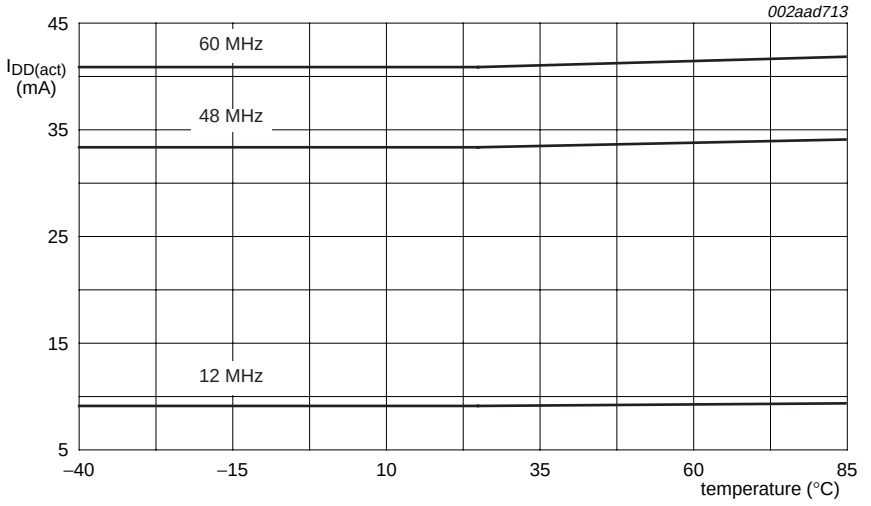
Fig 7. Typical LPC2104/2105/2106/01 $I_{DD(idle)}$ measured at different frequencies

© NXP B.V. 2008. All rights reserved.



Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$; T_{amb} = 25 °C; all peripherals enabled.

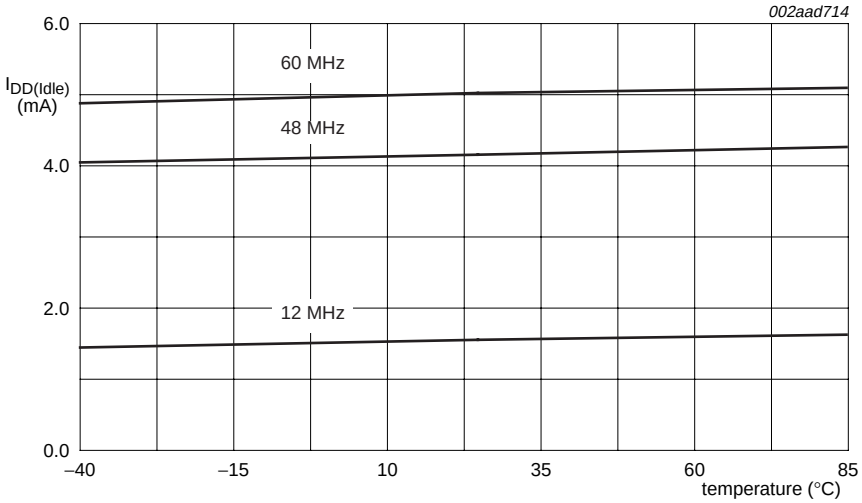
Fig 8. Typical LPC2104/2105/2106/01 $I_{DD(idle)}$ measured at different core voltages



Test conditions: Active mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$; core voltage 1.8 V; all peripherals disabled.

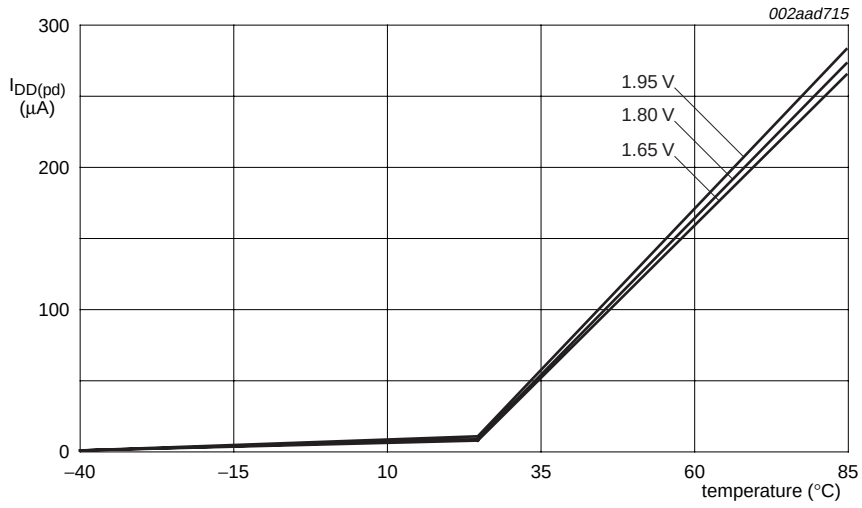
Fig 9. Typical LPC2104/2105/2106/01 $I_{DD(act)}$ measured at different temperatures

© NXP B.V. 2008. All rights reserved.



Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$; core voltage 1.8 V; all peripherals disabled.

Fig 10. Typical LPC2104/2105/2106/01 $I_{DD(idle)}$ measured at different temperatures



Test conditions: Power-down mode entered executing code from on-chip flash.

Fig 11. Typical LPC2104/2105/2106/01 core power-down current $I_{DD(pd)}$ measured at different temperatures

Table 10. Typical LPC2104/2105/2106/01 peripheral power consumption in Idle mode

Core voltage 1.8 V; T_{amb} = 25 °C; all measurements in mA; PCLK = $^{CCLK}/_{4}$

Peripheral	CCLK = 60 MHz
Timer 0	0.258
Timer 1	0.254
UART 0	0.494
UART 1	0.561

© NXP B.V. 2008. All rights reserved.

Table 10. Typical LPC2104/2105/2106/01 peripheral power consumption in Idle mode
…continued

Peripheral	CCLK = 60 MHz
PWM0	0.511
I^2C-bus	0.078
SPI	0.060
RTC	0.109
SSP	0.377

© NXP B.V. 2008. All rights reserved.

9. Dynamic characteristics

Table 11. Dynamic characteristics

T_{amb} = 0 °C to +70 °C for commercial applications, −40 °C to +85 °C for industrial applications; $V_{DD(1V8)}$, $V_{DD(3V3)}$ over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
External clock						
f_{osc}	oscillator frequency	supplied by an external oscillator (signal generator)	1	-	25	MHz
		external clock frequency supplied by an external crystal oscillator	1	-	25	MHz
		external clock frequency if on-chip PLL is used	10	-	25	MHz
		external clock frequency if on-chip bootloader is used for initial code download	10	-	25	MHz
$T_{cy(clk)}$	clock cycle time		20	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns
Port pins (except P0.2 and P0.3)						
t_r	rise time		-	10	-	ns
t_f	fall time		-	10	-	ns
I^2C-bus pins (P0.2 and P0.3)						
t_f	fall time	V_{IH} to V_{IL} [2]	$20 + 0.1 \times C_b$	-	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Bus capacitance C_b in pF, from 10 pF to 400 pF.

© NXP B.V. 2008. All rights reserved.

9.1 Timing

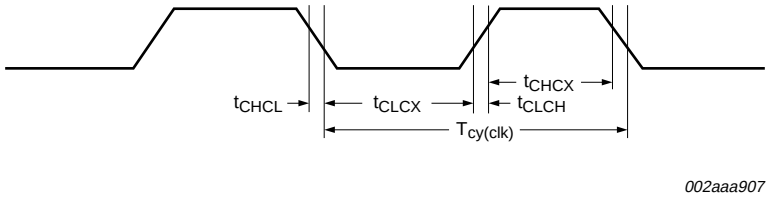
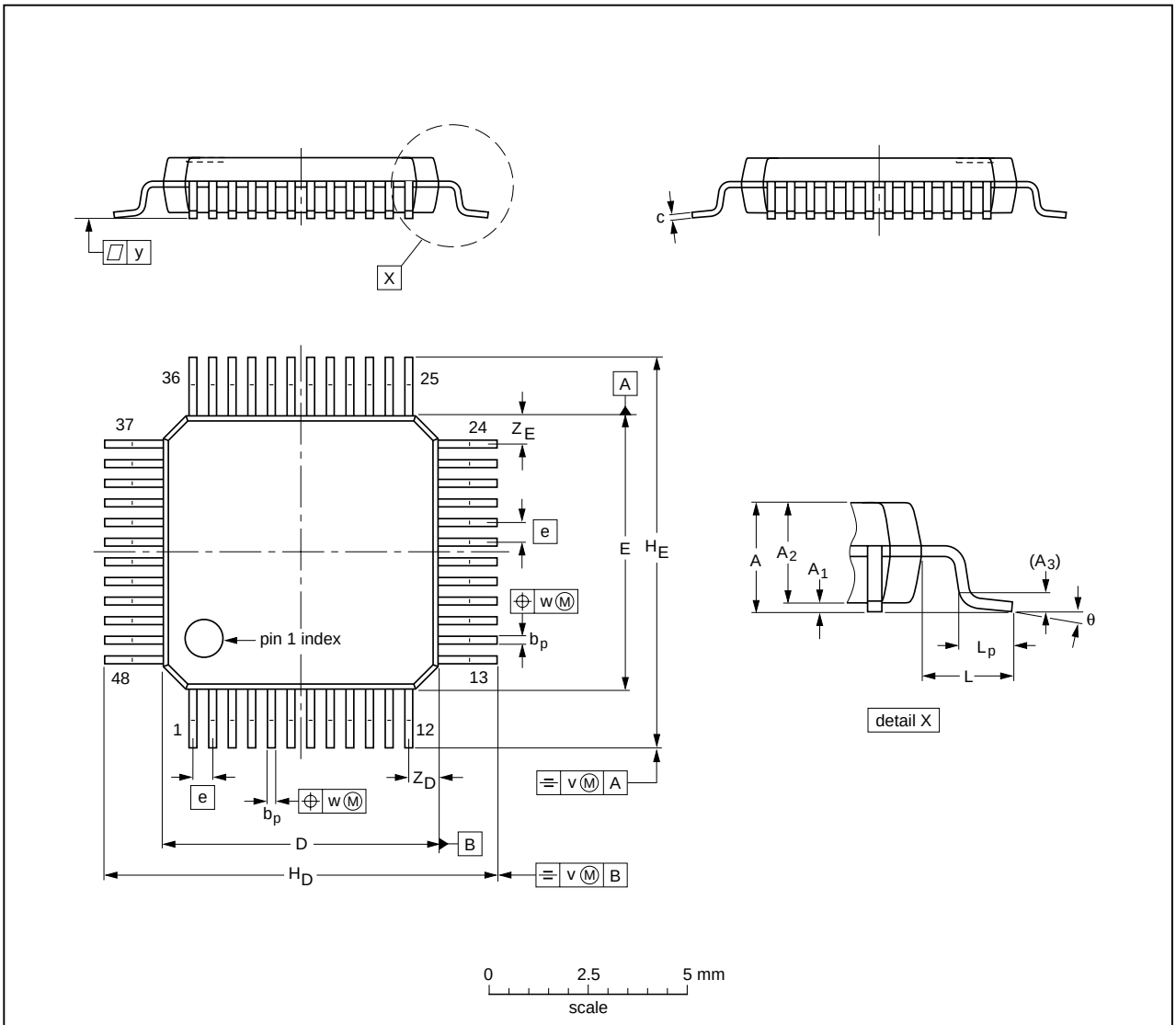


Fig 12. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

© NXP B.V. 2008. All rights reserved.

10. Package outline

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

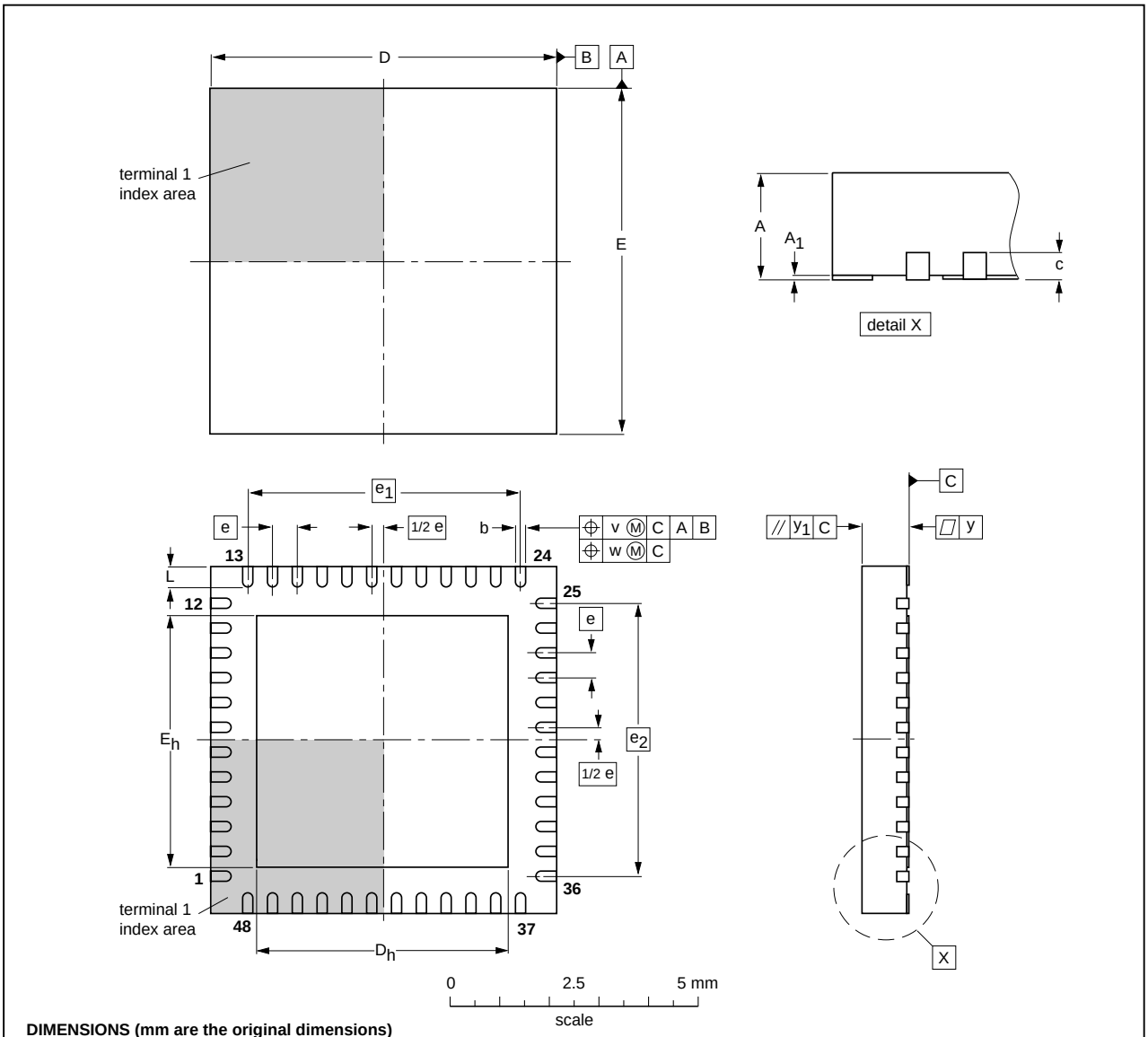
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT313-2	136E05	MS-026				~~00-01-19~~ 03-02-25

Fig 13. Package outline SOT313-2 (LQFP48)

© NXP B.V. 2008. All rights reserved.

HVQFN48: plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 x 7 x 0.85 mm **SOT619-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	7.1 6.9	5.25 4.95	7.1 6.9	5.25 4.95	0.5	5.5	5.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT619-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-18

Fig 14. Package outline SOT619-1 (HVQFN48)

© NXP B.V. 2008. All rights reserved.

11. Abbreviations

Table 12. Abbreviations

Acronym	Description
AMBA	Advanced Microcontroller Bus Architecture
APB	ARM Peripheral Bus
CPU	Central Processing Unit
DCC	Debug Communications Channel
FIFO	First In, First Out
GPIO	General Purpose Input/Output
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
RAM	Random Access Memory
SPI	Serial Peripheral Interface
SSI	Synchronous Serial Interface
SSP	Synchronous Serial Port
SRAM	Static Random Access Memory
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter

© NXP B.V. 2008. All rights reserved.

12. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC2104_2105_2106_7	20080620	Product data sheet	-	LPC2104_2105_2106_6
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Section 3 “Ordering information”; corrected temperature range for LPC2104FBD48/00, LPC2105FBD48/00. • Parts LPC2104FBD48/01, LPC2105FBD48/01, LPC2106BBD48, LPC2106FBD48/01, and LPC2106FHN48/01 added. • Description of /01 features added. • LPC2104/2105/2106/01 power consumption measurements added. • Maximum frequency f_{osc} for external oscillator and external crystal updated. • Figure 12 “External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)” updated. • Condition for I_{OHS} and I_{OLS} updated in Table 9 “Static characteristics”.			
LPC2104_2105_2106_6	20060725	Product data sheet	-	LPC2104_2105_2106-05
LPC2104_2105_2106-05	20041222	Product data	-	LPC2104_2105_2106-04
LPC2104_2105_2106-04	20040205	Product data	-	LPC2104_2105_2106-03
LPC2104_2105_2106-03	20031007	Product data	-	LPC2104_2105_2106-02
LPC2104_2105_2106-02	20030611	Product data	-	LPC2104_2105_2106-01
LPC2104_2105_2106-01	20030425	Product data	-	-

© NXP B.V. 2008. All rights reserved.

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

13.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

13.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

13.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

I^2C-bus — logo is a trademark of NXP B.V.

14. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

© NXP B.V. 2008. All rights reserved.

15. Contents

1 General description 1
2 Features 1
2.1 New features implemented in LPC2104/2105/2106/01 devices 1
2.2 Key common features 1
3 Ordering information 2
3.1 Ordering options 3
4 Block diagram 4
5 Pinning information 5
5.1 Pinning 5
5.2 Pin description 7
6 Functional description 10
6.1 Architectural overview 10
6.2 On-chip flash program memory 10
6.3 On-chip static RAM 10
6.4 Memory map 11
6.5 Interrupt controller 12
6.5.1 Interrupt sources 12
6.6 Pin connect block 13
6.7 Pin function select register 0 (PINSEL0 - 0xE002 C000) 13
6.8 Pin function select register 1 (PINSEL1 - 0xE002 C004) 15
6.9 General purpose parallel I/O 16
6.9.1 Features 16
6.9.2 Features added with the Fast GPIO set of registers available on LPC2104/2105/2106/01 only 16
6.10 UARTs 16
6.10.1 Features 16
6.10.2 UART features available in LPC2104/2105/2106/01 only 17
6.11 I^2C-bus serial I/O controller 17
6.11.1 Features 17
6.12 SPI serial I/O controller 18
6.12.1 Features 18
6.12.2 Features available in LPC2104/2105/2106/01 only 18
6.13 SSP controller (LPC2104/2015/2106/01 only) 18
6.13.1 Features 18
6.14 General purpose timers 18
6.14.1 Features 19
6.14.2 Features available in LPC2104/2105/2106/01 only 19
6.15 Watchdog timer 19
6.15.1 Features 19
6.16 Real time clock 20
6.16.1 Features 20
6.17 Pulse width modulator 20
6.17.1 Features 21
6.18 System control 21
6.18.1 Crystal oscillator 21
6.18.2 PLL 21
6.18.3 Reset and wake-up timer 22
6.18.4 Code security (Code Read Protection - CRP) 22
6.18.5 External interrupt inputs 23
6.18.6 Memory mapping control 23
6.18.7 Power control 23
6.18.8 APB 23
6.19 Emulation and debugging 24
6.19.1 EmbeddedICE 24
6.19.2 Embedded trace 24
6.19.3 RealMonitor 25
7 Limiting values 26
8 Static characteristics 27
8.1 Power consumption measurements for LPC2104/2105/2106/01 29
9 Dynamic characteristics 34
9.1 Timing 35
10 Package outline 36
11 Abbreviations 38
12 Revision history 39
13 Legal information 40
13.1 Data sheet status 40
13.2 Definitions 40
13.3 Disclaimers 40
13.4 Trademarks 40
14 Contact information 40
15 Contents 41

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2008. **All rights reserved.**

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 20 June 2008
Document identifier: LPC2104_2105_2106_7

founded by

PHILIPS